A 114-dB 68-mW Chopper-Stabilized Stereo Multibit Audio ADC in 5.62 mm^2

YuQing Yang, Amiya Chokhawala, Mark Alexander, John Melanson, and Dylan Hester

***Abstract*—A multibit delta-sigma audio stereo analog-to-digital converter has been developed. It employs a fifth-order single-loop 17-level delta-sigma modulator with an input feedforward gain stage. A second-order mismatch shaping (DEM) circuit is utilized to remove tones and nonlinearities caused by capacitor mismatch of the feedback digital-to-analog converter. The implementation of the DEM block introduces minimum latency into the delta-sigma feedback loop. Chopper stabilization is applied to the first integrator to eliminate the $1/f$ noise. The converter achieves 114-dB dynamic range and −105-dB total harmonic distortion over the 20-kHz audio band. This single chip includes stereo analog modulators, bandgap reference, serial interface, and a two-stage decimation filter, occupies 5.62-mm^2 active area in a 0.35-μm double-poly, three-metal CMOS process and dissipates only 55-mW power in the analog circuits.**

***Index Terms*—Chopping technique, delta-sigma modulation, dynamic element matching, feedforward, latency, multibit delta-sigma modulation, switched capacitor.**

I. Introduction

THE proliferation of mainstream consumer digital audio equipment such as DVD recording systems, multichannel A/V processors and receivers, and digital room correction systems, has generated increasingly stringent requirements for analog-to-digital converters (ADCs) used in the audio signal processing chain. Wide dynamic range and low distortion are needed to capture an analog input signal in its most original form, which is crucial to achieving the high sound quality that consumers increasingly demand. An audio ADC noise floor needs to be exceptionally stable, free from tones as the input level is varied, and ideally flat throughout the audio signal band. This requirement arises mainly because human hearing is very sensitive to the audibility of noise floor modulation and spurious tones. Due to the cost constraints of the consumer audio market, a stereo audio ADC must have small die size for low cost, multiple operating modes and unique features, plus low power consumption. Several audio converters [1]–[3] have been developed throughout the years, however, no single-chip stereo ADC meeting all the requirements has been previously reported.

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This paper presents a low-cost low-distortion stereo audio ADC intended for the mainstream consumer audio market. It includes two stereo analog modulators, a bandgap derived bias generator, a two-stage decimation filter, serial interface logic and noise managed clock generation/control logic. A multibit topology extension of conventional single bit $\Delta\Sigma$ modulation has proven to be especially suitable for such an application. Compared with single-bit topologies, a multibit design further relaxes the design requirements for critical analog subcircuits as well as the decimation filter. A second-order dynamic element matching (DEM) circuit has been employed to remove the nonlinearity and tones caused by the capacitor mismatch of the feedback digital-to-analog converter (DAC), while introducing minimum latency into the delta-sigma feedback loop. As far as converter linearity is concerned, a common belief is that a single-bit topology is inherently linear and a multibit topology is inferior. This paper demonstrates that with proper analog modulator and DEM design, a multibit design can achieve equal to or higher linearity compared to a single-bit design, with substantially less die area and power dissipation. These benefits arise mainly because the multibit $\Delta\Sigma$ approach relaxes the design requirements for critical analog subcircuits, which are the main contributors to the converter nonlinearity [4], [5].

One popular method to reduce power dissipation in low-end ADCs is to lower the oversampling ratio, thus slowing down the sampling clock rate. Unfortunately, a low oversampling ratio will increase the sampling capacitor size substantially. In this design, an oversampling ratio of 128 was chosen as a good tradeoff between die area and power consumption. Switched-capacitor techniques are employed to implement the analog subcircuits mainly because of their high immunity to clock jitter effects.

The overall modulator topology and DEM circuits will be covered in Section II. Section III will discuss analog subcircuit design. Layout and measurement results will be covered in Section IV.

II. System Level Details

A. Delta-Sigma Modulator Topology

Classical multistage architectures are able to achieve high-order noise shaping with excellent modulator stability by cascading second (or lower)-order $\Delta\Sigma$ stages [6]–[8]. The feedback DAC nonlinearity in the downstream stages is suppressed by the noise cancellation logic that processes the outputs of multiple quantizers in the cascade. Also, the feedback DACs of downstream stages do not contribute thermal noise directly

to the input sampling capacitors. These facts greatly reduce the DEM logic complexities and overall die area required for the feedback DAC. However, quantization noise and tones from the low-order loop of the first stage are likely to leak to the converter output due to stage-to-stage mismatch. This stage-to-stage mismatch also limits the achievable dynamic range of the converter.

Classical single-loop multibit architectures are more immune to tone problems, and have better potential to achieve high dynamic range. Unlike the multistage topology, where downstream feedback DAC linearity errors are noise shaped, in a single-loop multibit case, the DEM circuit must suppress the entire static nonlinearity of the feedback DAC. Complex design issues in a single-loop DEM circuit also increase potential latency problems, and these have to be considered when evaluating different architectural approaches in the mismatch shaping logic. Since the DEM circuitry is placed inside the modulator feedback loop, it is crucial to minimize its latency, otherwise stability will be compromised. One option is to use simple first-order mismatch shaping logic such as data weighted averaging (DWA) [9], [10], which uses low delay pointer rotation shifters. In order to achieve low distortion performance with first-order DWA-based DEM, the feedback DAC unit capacitor size has to be kept large enough to maintain good element-to-element matching. The other option is to lower the oversampling ratio [11], thus providing more time for the DEM logic to complete its calculation and output the result to the feedback DAC. For a switched-capacitor circuit, lowering the oversampling ratio will increase the sampling capacitor and overall chip size significantly. Both options mentioned above are not practical for high performance ADCs. When designing a high-order modulator, such as a fifth-order single-loop design, it is still very difficult to push the modulation index over 0.85 unless a large number of quantization levels (such as 32), are employed in the quantizer. The integrator output swings also do not scale down linearly with an increasing number of quantization levels. Since the first integrator receives the least noise shaping, compared with the downstream integrators, a high dc gain and slew rate are still required for the first integrator operational amplifier (opamp).

With many quantization levels available, however, the effective multibit quantizer gain is much more constant than that of a single-bit quantizer. If a DEM circuit is employed to remove the DAC nonlinearity, a single-loop multibit modulator can be viewed as a linear system. An improved single-loop multibit architecture is shown in Fig. 1, where an input feedforward gain stage is introduced to relax the design requirements of the analog subcircuits. The gain A6 is defined as $1/(\text{quantizer gain} \times \text{feedback DAC gain})$. Since the multilevel quantizer gain is roughly constant during normal operation, input signal energy will largely be cancelled at the first integrator summing junction node, without leaking into the loop at any given operational cycle. This results in smaller and less signal-dependent voltage swings at the first integrator output, relaxing design requirements such as dc gain and slew rate for the first integrator opamp. In other words, this modulator can tolerate incomplete settling error during the integration phase, since the integrator output is dominated by quantization noise.

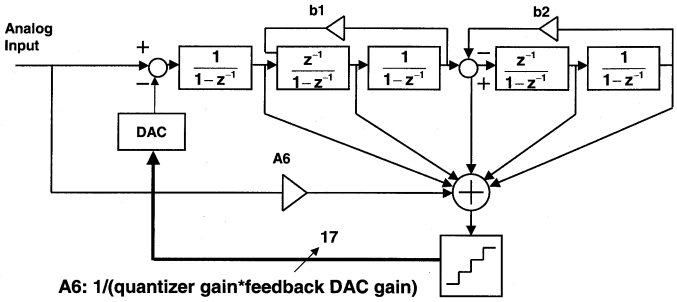

Fig. 1. Multibit delta-sigma analog modulator with feedforward gain stage.

TABLE I
MAXIMUM INTEGRATOR OUTPUT SWING AND VOLTAGE STEP

Output	Int1	Int2	Int3	Int4	Int5
Max. Swing	0.62	0.78	1.1	1.5	1.45
Max. Step	0.36	0.22	0.21	0.22	0.15

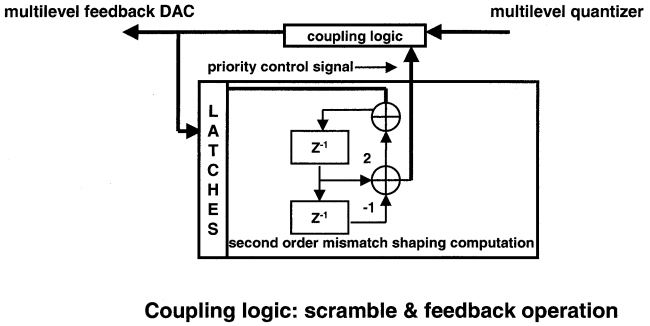

Fig. 2. Second-order DEM top-level architecture.

The superposition principle of linear system can be employed to easily demonstrate that the input feedforward gain stage results in a unity signal transfer function (STF), but does not alter the noise transfer function (NTF). The feedforward stage also serves as a rough conversion path to force the multibit quantizer output to track the input signal to first order, especially for large input signals. This allows quick recovery from input overload conditions. The modulator is designed with a fifth-order loop filter and symmetric seventeen-level quantization (including a zero level output code), to avoid system mismatch. Alternating delayed and nondelayed integrators are used to reduce peaking of the noise shaping function, thus maximizing loop stability. In Matlab simulations, this modulator achieves 130-dB signal-to-noise ratio for an oversampling ratio of 128, within the 20-kHz audio signal band. The modulation index reaches 0.95, while the first integrator maximum output voltage swing is reduced by 35% and maximum output voltage step by 40%, compared with a similar multibit modulator without the feedforward gain stage. The integrator output swings and steps are shown in Table I. Simulation also shows this analog modulator can tolerate a relaxed first integrator opamp dc gain of around 60 dB, with no degradation of performance.

B. Second-Order Dynamic Element Matching

A DEM circuit with second-order noise shaping is implemented in this design, and it introduces minimum latency into the delta-sigma feedback loop. Capacitors are fabricated in a

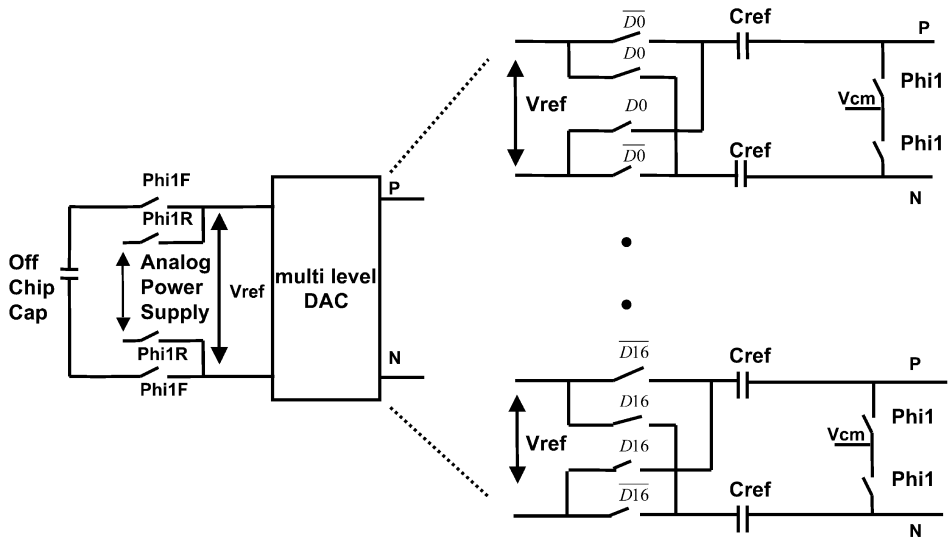

Fig. 3. Feedback DAC with rough and fine sampling schemes.

double poly process, with thin oxide option. It is difficult, however, to guarantee good matching in low cost, high volume, CMOS processes with small capacitor size. Thus, a second-order DEM approach is needed to handle the worst-case scenario, with potentially larger than 5% gradient mismatch. It also eliminates unwanted signal-dependent tones associated with the first-order DEM circuit, which can be rather troublesome in audio converters.

As shown in Fig. 2, the DEM logic is divided into two subcircuits. One is the coupling logic, which is connected between the thermometer-coded quantizer and multilevel feedback DAC. The other is the second-order mismatch-shaping calculator [12]–[15], which determines the priority control signals for the coupling logic. Only the coupling logic, which incurs a small amount of delay, is placed inside the modulator feedback loop. As shown in Fig. 7, the multilevel quantization takes place in the middle of the integration phase (Phase 2); thus the quantization is performed before complete settling of the integrator outputs. The quantizer and the coupling logic have the remaining half of the Phase 2 cycle to finish the scrambling and feedback operation. The second-order mismatch shaping calculator latches the coupling logic output at the beginning of the Phase 1, allowing the DEM calculator a full Phase 1 cycle to accomplish its computation. This approach does introduce additional nonidealities into the modulator. However, the improved multibit analog modulator discussed above suppresses most of the nonlinearity.

III. Analog Circuits Implementation

A. First Integrator With Chopper-Stabilized Opamp and Feedback DAC

The first integrator and feedback DAC are implemented in a fully differential switched-capacitor configuration. For the DAC, it is crucial that a clean reference voltage is established, and its thermal noise contribution to the sampling capacitor is reduced at the same time. As shown in Fig. 3, a rough-and-fine charging scheme [14] is used in this design. The capacitive feedback DAC samples either the analog power supply or analog power ground, depending on the code output from the DEM coupling logic, during the rough phase. During the fine phase, the DAC is connected to an off-chip bypass capacitor that effectively filters out high frequency noise components. The low pass corner frequency is set around 2 Hz, well below the audio band, and this configuration achieves reasonably good power supply rejection (in the range of 60 dB at 1 kHz). A fully differential configuration also allows the analog power supply to see the same capacitive load during each clock cycle, thus avoiding signal-dependent setting behavior inside the feedback DAC. Compared with a conventional approach to generate stable DAC charging voltages, this method eliminates the need for buffer circuits, while still providing the high power-supply rejection ratio (PSRR) of a stable on-chip bandgap-derived reference. Combined with a high modulation index, the reference voltage of typically 5 V (in this design) substantially reduces the overall DAC capacitor size.

The first integrator schematic is shown in Fig. 4. The input sampling capacitors employed a double sampling scheme to double the effective sampled input signal charge. This scheme increases the thermal noise tolerance of the converter, to further reduce sampling capacitor size. One major concern of the first integrator design is the linearity of its front-end *RC* sampling network. The dominant nonlinear source is the variation of input switch-on resistance as a function of the input signal level. Due to the double sampling scheme, and minimized DAC thermal noise contribution, the sampling capacitor size is reduced to merely 3.5 pF in this design, allowing a relatively large sampling switch-on resistance. This approach eliminates the need for additional circuit complexities such as bootstrapped switch drive, or low threshold devices, in the sampling network.

Because of the time constant difference between the input sampling and DAC *RC* networks, the sampled input and the feedback DAC charge packets may not arrive at the opamp summing nodes at the same time. Even though the net charge transferred to the integrating capacitors during each cycle is small, the integrator opamp would have to settle a large disturbance

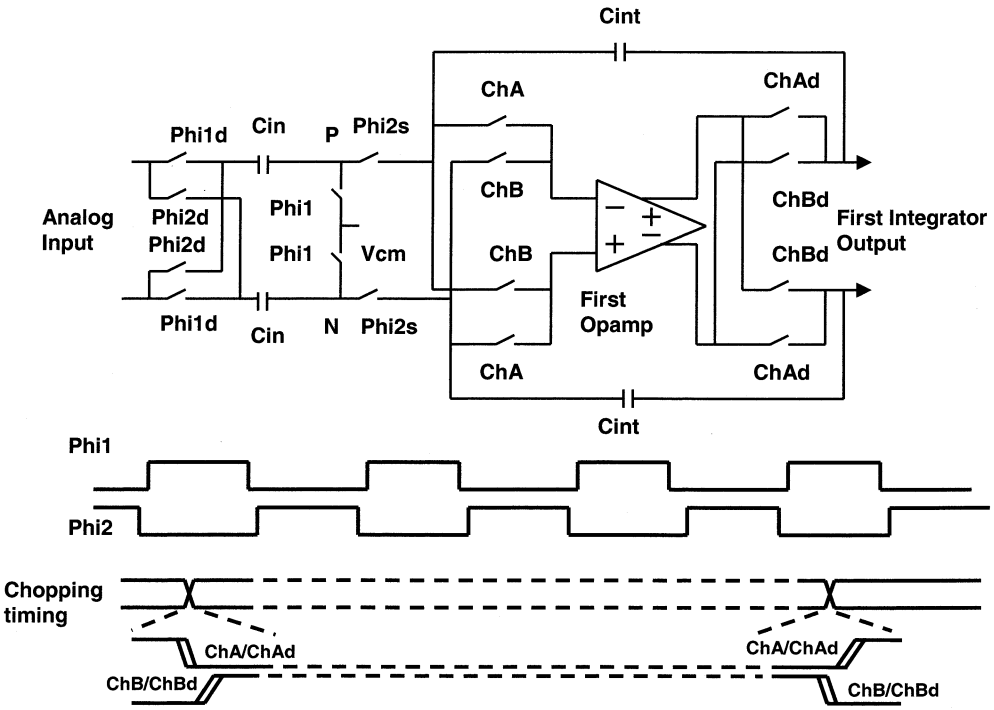

Fig. 4. First integrator and chopping timing diagram.

caused by this phenomena, if charge packets from the input sampling network and feedback DAC were non-time-aligned. Therefore, during the integration phase (Phase 2), the summing junction switches at nodes P and N are turned on after both the Phase 2 switches of the input network and the DAC switches are turned on. This arrangement allows charge from input sampling and feedback networks to be passively mixed beforehand, and ensures that the summing node switches and opamp outputs pass only the net overall settled charge. This modified clocking scheme results in smaller summing node switch sizes, and reduced opamp power consumption. Also, a small switch size leads to less charge injection, which further improves converter linearity.

A chopper stabilization technique is employed to reduce the high $1/f$ noise of the 5-V digital CMOS process used for fabrication of the converter [16]. It also lowers the effective input referred offset voltage of the first integrator amplifier. The opamp $1/f$ noise is modulated once, and moved up to the chopping frequency, at $8F_s$, away from the baseband. The input signal, however, is modulated up to the chopping frequency and then demodulated back down to baseband. Therefore, there exists the possibility that spectrally shaped HF quantization noise could be demodulated down, thus coupling additional noise into the ADC baseband. In this design, chopping is performed in the middle of the integrator holding phase (Phase 1), which will prevent the first integrator from sampling additional noise. The ChA switches of Fig. 4 are opened first, and then ChAd switches are opened. Subsequently, the ChB switches are closed. Charge injection from the ChA switches is signal independent, and will largely be cancelled by the ChB switches. It is also extremely important to properly balance and shield the chopping network switch layout, to minimize unwanted coupling from switched nodes to nonswitched nodes. Great care was taken in this design

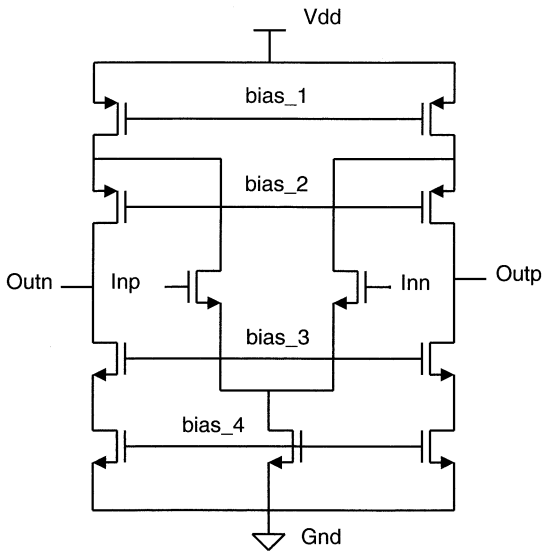

Fig. 5. Opamp of first integrator.

to ensure that adequate shielding and isolation was maintained in the chopper switch layout.

B. Opamp Design

As shown in Fig. 5, a fully differential folded cascade structure is used for the first integrator opamp [17]. Because of the architectural level improvements described above, the design requirements are greatly relaxed. The simulated open-loop dc gain is 68 dB, and settling during the integration phase (Phase 2) only occurs to a 7-τ accuracy. An NMOS differential input pair is used to effectively attenuate the thermal noise from the loading devices because of its high transconductance. The chopping technique removes the usual concern for high

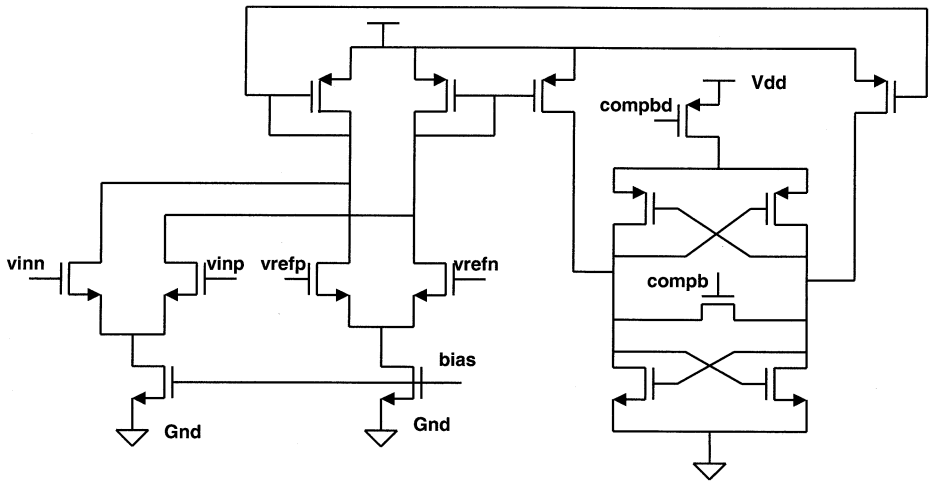

Fig. 6. Comparator of multibit quantizer.

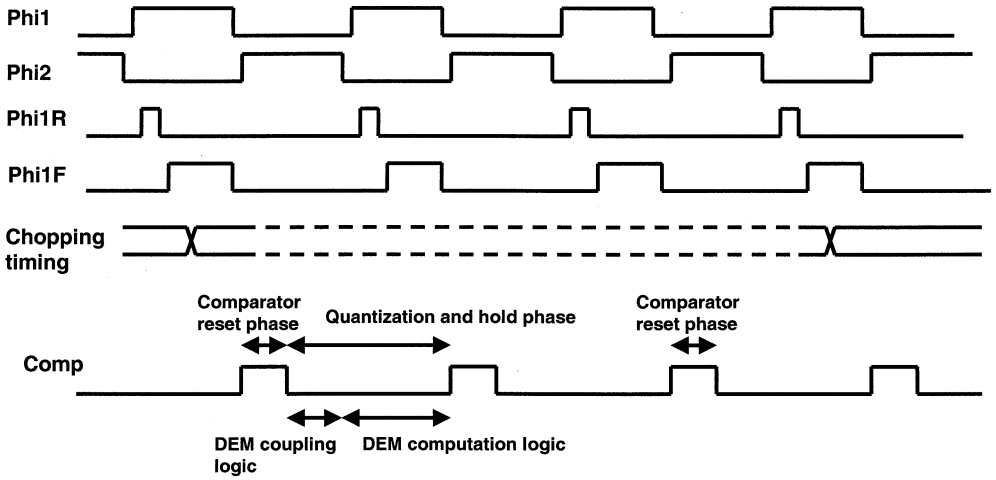

Fig. 7. Analog timing diagram.

NMOS flicker noise, since it allows a much smaller opamp input differential pair size. Thus, the summing node parasitic capacitances are greatly reduced, further improving power efficiency.

C. Multibit Quantizer Design

The multibit quantizer is adapted from a CMOS flash ADC architecture. Fast operation is necessary, so that the DEM coupling logic is able to accomplish its operation before the critical SC sampling edge. It is also important to prevent "kickback" noise among comparators (the schematic of which is shown in Fig. 6). One pair of current mirrors is added between the input differential pair and the regeneration stage, to provide better isolation between them [18], [19]. Bias current and transistor size are optimized to meet the speed requirements, while injecting the least amount of noise into the substrate.

The overall analog timing diagram is shown in Fig. 7. It should be noted that the DEM circuitry operates on the digital power supply, not the analog. At the beginning of Phase 1, the DEM block latches the coupling logic output. It then has the whole Phase 1 clock cycle to complete its computation for the following cycle. The latched coupling logic output is then level shifted to the analog power supply, to serve as the feedback DAC control signals. The feedback DAC starts its rough and fine sampling operation after the control signals are fully stabilized. As mentioned previously, the chopping operation is performed in the middle of feedback DAC fine sampling phase. This gives the first integrator enough time to settle the input/output disturbance caused by a chopping operation, before the next critical sampling clock edge. All comparators in the multibit quantizer are reset during the first portion of the Phase 2. Priority control signals in the DEM circuits are also updated during the same period. Quantization takes place in the middle of Phase 2, and the 17-level thermometer output code is level-shifted to the digital power supply prior to being fed to the DEM circuit.

IV. Layout and Measurement Results

This chip integrates the stereo analog $\Delta\Sigma$ modulators, bandgap bias generator, multifunction serial interface, decimation filter, and a high-pass filter. It supports 48-, 96-, and 192-kHz sampling rates, with 24-bit two's complement output. The analog modulator output is decimated by a factor of 128, 64, or 32, depending on the final sampling rate. The decimation

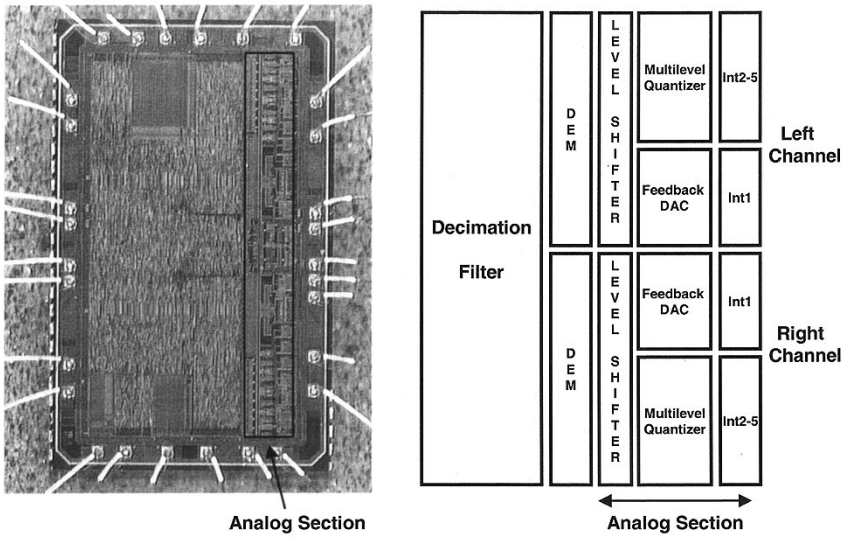

Fig. 8. Floor plan and die photo.

filter consists of a cascade of two digital low-pass filters: one that decimates the incoming data by 64 or 32, and a second that can decimate by an additional factor of 2 if necessary. The first decimation stage employs a time interleaved, pipelined finite impulse response (FIR) structure. Furthermore, the same filter coefficients are used for decimation by 64 and 32, by decimating the filter coefficients, themselves, to save die area. The final output rate filter is implemented in a general purpose multiply and accumulate (MAC) engine. The overall decimation filter stop band attenuation is -95 dB, and a first-order high-pass filter with -3-dB corner frequency at 0.5 Hz is also implemented in the MAC engine to remove any system level dc offset. All digital sections operate from 1.8–3.3 V. Overall chip performance data is summarized in Table II.

This stereo ADC was implemented in a 0.35-μm double-poly three-metal CMOS process. A great deal of attention was given to analog floor planning, which is shown in Fig. 8, to allow a very compact modulator layout with adequate shielding between sensitive analog nodes and clock lines. The clock generator is placed between two analog modulators, next to the shared bias generator, to minimize clock skew between the channels. The layout effort was primarily focused on the first integrator and capacitive feedback DAC. The layout of these sections is fully symmetric, and nodal parasitics were carefully minimized through optimal placement of the switches and capacitors adjacent to each integrator's opamp. Sensitive nodes such as loop summing junctions and the reference-sampling path were very carefully routed, and shielded from interfering signals. Physical edge matching structures are used to reduce overall layout related mismatch effects on the feedback DAC unit capacitors, first integrator sampling, and integration capacitors.

Measurements were taken for chips assembled in both ceramic and plastic package. Chips built in plastic packages showed better linearity because of smaller bondwire inductance, and lower package parasitics (measurement results shown in this paper are for chips assembled in a plastic package). All measurements were taken with a 5-V analog supply and 1.8-V digital power supply, resulting in a total chip power consumption of 68 mW. Two 16 384-point fast Fourier transform (FFT) plots of -60-dBFS and -1-dBFS input signals are shown in Figs. 9 and 10, respectively. No spurious tones or harmonics are observed in Fig. 9, which indicates good low-level linearity. The second and third harmonics in

TABLE II
STEREO ADC PERFORMANCE SUMMARY

Full Scale Input Range	2Vrms
Clock Frequency	6.144MHz
Dynamic Range	114dB(A weighted, 20kHz bandwidth)
THD+Noise	-105dB(20kHz bandwidth)
Analog Power Supply	5V
Digital Power Supply	1.8V-3.3V
Power Dissipation	55mW(analog) 13mW(digital at 1.8V)
Process	0.35μm DP, three metal
Active area	5.62 mm^2

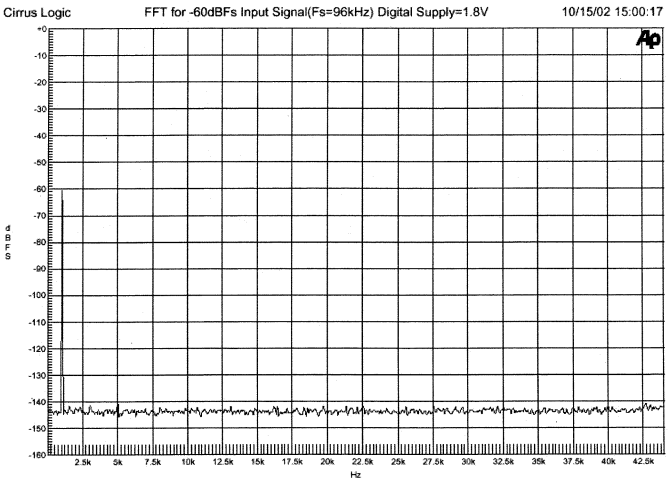

Fig. 9. FFT for -60 dBFS input ($F_s = 96$ kHz.)

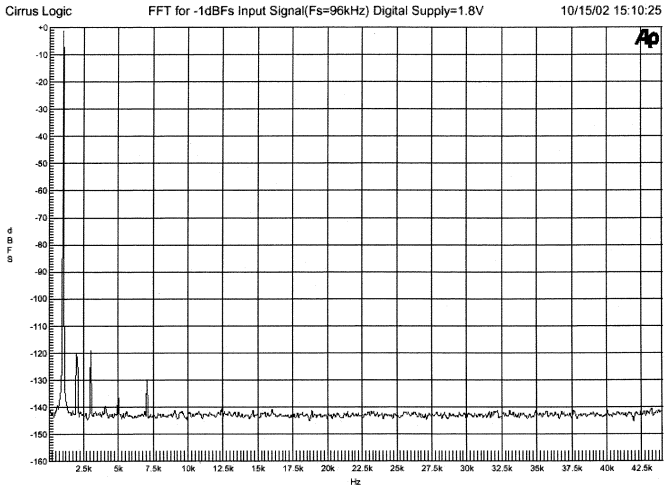

Fig. 10. FFT for -1 dBFS input ($F_S =$ 96 kHz).

Fig. 11. THD+N versus input signal level.

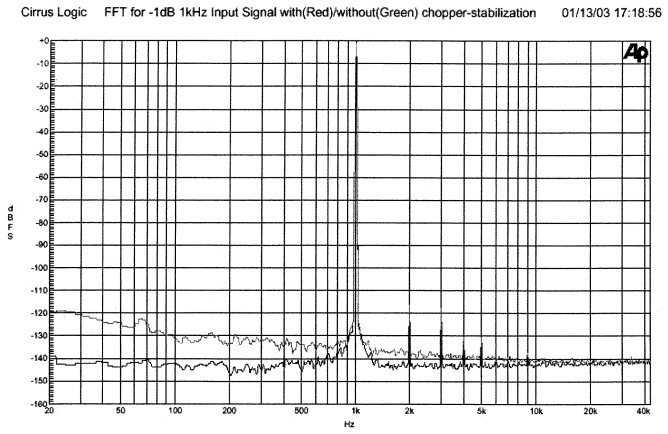

Fig. 12. FFT of -1-dB 1-kHz input signal with/without chopper stabilization.

Fig. 10 only reach the -120-dB range, indicating very good full-scale linearity. The observed noise floor is flat across the spectrum due to the chopping techniques employed in the first integrator. A minimum of noise floor modulation is observed between these two input levels, and is very desirable in an audio converter. A plot of total harmonic distortion and noise (THD+N) versus input level is shown in Fig. 11, which demonstrates the design maintains good linearity across the full input signal range. FFT plots of chopping turned on and chopping turned off are shown in Fig. 12. The baseband noise floor is flat without any evidence of excess high-frequency noise being folded down into the low-frequency band. The stereo ADC performance is summarized in Table II.

V. Conclusion

This paper presented a new low-power stereo multibit audio ADC. The DEM circuit introduces minimum latency into the delta-sigma feedback loop, which enables the use of second-order DAC capacitor mismatch shaping logic. This design also demonstrated an improved multibit modulator that is able to tolerate incomplete settling in the integrator opamps, which further relaxes other design requirements such as dc gain of the first integrator. A chopper stabilization technique is employed to remove high $1/f$ noise associated with low-cost digital CMOS processes. This stereo audio ADC achieves 114-dB dynamic range, and -105-dB THD+N, at 68-mW power consumption. The die area, including pad ring, is only 5.62 mm^2. Compared with previously reported high-performance stereo audio ADCs, this converter achieves the best power efficiency versus noise with the smallest die area. It has been demonstrated that with second-order DEM and proper analog modulator design, a multibit $\Delta\Sigma$ topology can achieve high dynamic range and linearity with much lower power dissipation and die area than a single-bit design. The overall architecture and circuit design techniques shown in this paper can be easily scaled up to achieve higher dynamic range, or can be applied to higher speed applications with much less die area and power dissipation.

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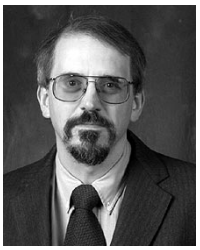

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