A New CMOS 4Q-Multiplier Using Linear and Saturation Regions Complementally

Tsutomu Suzuki, Takao Oura, Teru Yoneyama, Hideki Asai
Department of Systems Engineering, Faculty of Engineering, Shizuoka University
seabass@tzasai7.sys.eng.shizuoka.ac.jp

Abstract

A New Four-Quadrant (4Q) Multiplier complementally using linear and saturation regions of MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is proposed. This multiplier operates in the region except for the threshold voltage V_T to zero, using a novel non-linearity cancellation method. The validity of proposed circuit is confirmed through HSPICE simulation.

1. Introduction

A multiplication of two signals is one of the most important signal operations in analog signal processing. The multiplier is used not only as computational building blocks but also as a programming element in systems such as filters, neural networks, mixers and modulators in communication systems. Thus far, several 4Q-multipliers have been reported [1][2][3]. However these 4Q-multipliers utilize only either in the saturation region or the linear region of MOSFET. Therefore the input range of 4Q-multipliers has been restricted and narrow. On the other hand, rail-to-rail components have been proposed to expand the input range of OTA circuit. One of them is the novel rail-to-rail VCCS (Voltage Controlled Current Sources) [4].

In this paper, we propose a novel non-linearity cancellation method and 4Q-multiplier, which operates in the saturation and linear regions of MOSFET in which the input range of the multiplier is expanded [6]. We have simulated the proposed circuit by using HSPICE. Finally, we confirm that the proposed circuit is useful as the 4Q-multiplier.

2. Non-linearity cancellation

The drain current I_{DS} of the simple MOSFET model is expressed as

$$I_{DS} = K(V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS} \quad (1)$$

for the linear region($V_{GS}-V_T>V_{DS}$), and

$$I_{DS} = \frac{K}{2}(V_{GS} - V_T)^2 \quad (2)$$

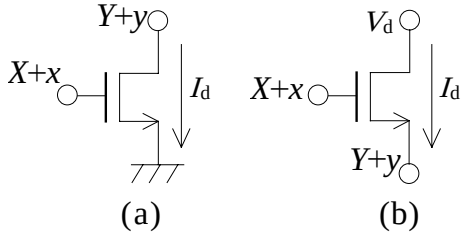

Fig.1 Operating conditions of the multipliers.
(a) Using $V_{GS}V_{DS}$ (b) Using V_{GS}^2

for the saturation region($0<V_{GS}-V_T<V_{DS}$), respectively, where V_{GS}, V_{DS} and V_T are the gate-source, drain-source and the threshold voltages, and K ($=(W/L)\mu_0 C_{OX}$) is the transconductance parameter. When V_{GS} is lower than V_T, the transistor in the cut-off region.

The conventional architecture of MOS 4Q-multiplier is categorized in a few types, namely, multipliers that utilize the term $V_{GS}V_{DS}$ or V_{DS}^2 of the drain current model (1) of MOSFET operating in the linear region, multipliers which utilize the term V_{GS}^2 of the drain current model (2) of MOSFET operating in the saturation region, and the Gilbert cells [5] etc. In the following sections, we discuss two conventional multiplier topologies and their dynamic ranges. One is the multiplier operating in the linear region using the term $V_{GS}V_{DS}$ in (1) and another is the multiplier operating in the saturation region using the term V_{GS}^2 in (2).

2.1. Multiplier Using $V_{GS}V_{DS}$

Fig.1 (a) shows the operating condition of 4Q-multiplier using the term $V_{GS}V_{DS}$ in (1). In Fig. 1 (a), the transistor operates in the linear region when proper bias voltages X and Y are provided, where x and y indicate the input signals. In this configuration, the drain current I_d of the transistor is given by

$$I_d = K\left\{X + x - V_T - \frac{1}{2}(Y + y)\right\}(Y + y), \quad (3)$$

according to the drain current model of MOSFET operating in the linear region (1). Then the desired term ***xy*** can be obtained in (3). All the higher order terms and common-mode components (X, Y and V_T) can be

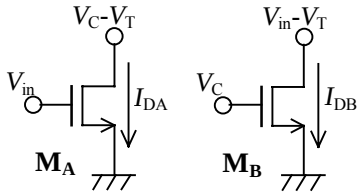

Fig.2 Basic elements of proposed circuits.

cancelled with the subtractions of the currents by using current mirrors circuits.

2.2. Multiplier Using V_{GS}^2

Fig.1 (b) shows the operating condition of 4Q-multiplier using the term V_{GS}^2 in (2). In Fig.1 (b) the transistor M_B operates in the saturation region, where x and y are the input voltages, and X and Y indicate the bias voltages. The drain current is given by

$$I = K\{(X+x)-(Y+y-V_T)-V_T\}^2, \qquad (4)$$

from the substitutions the voltages into the drain current model of MOSFET operating in the saturation region (2). Then the desired term $\boldsymbol{xy}$ can be obtained in (4). Undesired terms can be cancelled with differential configuration by using current mirrors circuits.

2.3. Input Range of Multipliers

The input voltages for the configurations of Fig.1 (a) and Fig. 1 (b) have the following restrictions.

In Fig.1 (a), the input voltages must be satisfied with (5) to make the transistor operate in the linear region.

$$V_{SS} < X + x - V_T < Y + y < V_{DD}, \qquad (5)$$

where V_{DD} and V_{SS} represent the positive and negative power supply voltages.

In Fig.1 (b), on the other hand, the input voltages have to be satisfied with (6) to make the transistor operate in the saturation region, where V_d is the drain voltage of the transistor.

$$V_{SS} < Y + y < X + x - V_T < V_d < V_{DD}. \qquad (6)$$

Due to the restrictions mentioned above, the input ranges of the multipliers are restricted and narrowed.

3. VCCS circuit

Fig.2 shows the basic elements of proposed circuit, which consists of the transistors M_A and M_B. In this figure, V_{in}, V_C, I_{DA} and I_{DB} are the input voltage, the control voltage, the drain current flowing in the transistor M_A and the drain current flowing in the transistor M_B respectively. To make the transistors M_A and M_B operate complementally, the drain voltages V_{DA} and V_{DB} are determined as follows,

$$V_{DA} = V_C - V_T,$$
$$V_{DA} = V_C - V_T. \qquad (7)$$

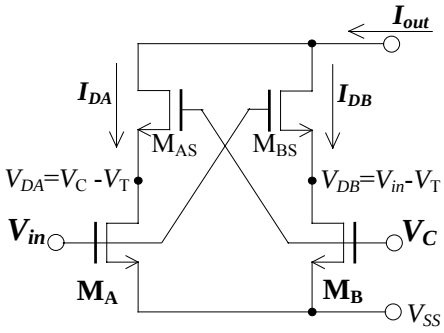

Fig.3 The proposed VCCS.

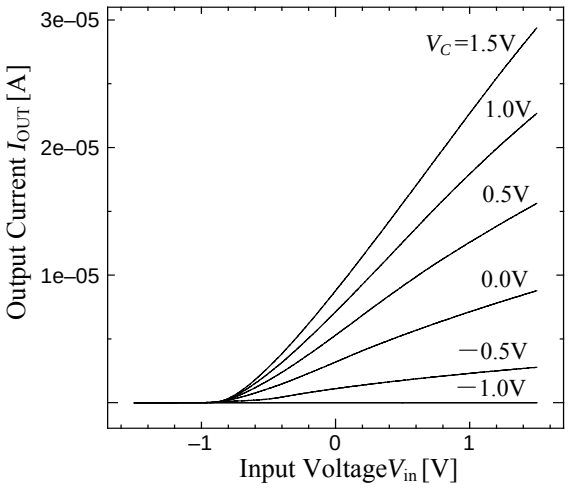

Fig.4 I/V Characteristics of VCCS.

For (7), let the point of transition from saturation region to linear one for M_A be equal to that from linear region to saturation one for M_B.

Now we name the element as VCCS, which consists of the transistors M_A and M_B, whose output current I_{out} is the sum of the drain currents I_{DA} and I_{DB} flowing in the transistors M_A and M_B.

When the input voltage V_{in} is less than the control voltage V_C, the transistor M_A operates in the saturation region and the transistor M_B operates in the linear region.

Therefore the output current I_{out} is given by

$$\begin{aligned} I_{out} &= I_{DA} + I_{DB} \\ &= \frac{K}{2}(V_{in} - V_T)^2 \\ &\quad + K(V_C - V_T - \frac{V_{in}\text{-}V_T}{2})(V_{in} - V_T) \\ I_{out} &= K(V_{in} - V_T)(V_C - V_T). \end{aligned} \qquad (8)$$

On the other hand, in the case of the input voltage V_{in} is higher than the control voltage V_C, the transistor M_A operates in the linear region and the transistor M_B operates in the saturation region. Therefore the output current I_{out} is given by

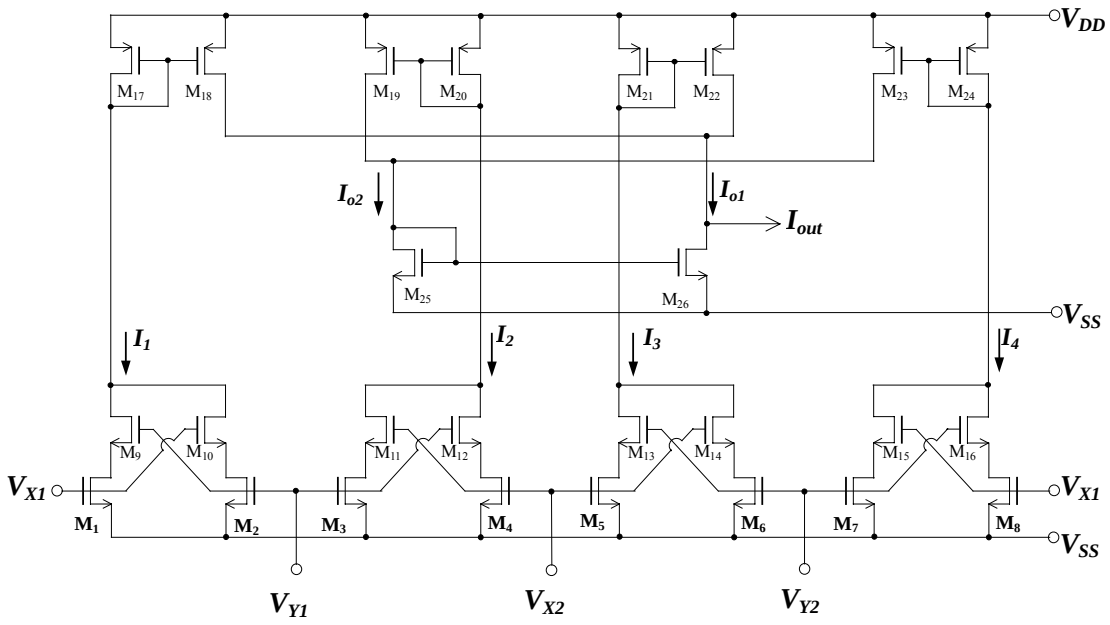

Fig.5 proposed 4Q-multiplier circuits.

$$I_{out} = I_{DA} + I_{DB}$$
$$= K(V_{in} - V_T - \frac{V_C - V_T}{2})(V_C - V_T)$$
$$+ \frac{K}{2}(V_C - V_T)^2$$
$$I_{out} = K(V_{in} - V_T)(V_C - V_T) . \quad (9)$$

From (8) and (9), the undesired terms are cancelled so that the output current I_{out} yields a multiplication of V_{in} and V_C. Therefore this VCCS operates as the multiplier between the threshold voltage V_T and the supply voltage V_{DD}. The proposed VCCS circuit is shown in Fig.3. Here the transistors M_{AS} and M_{BS} are fixed to operate in the saturation region. Then the drain voltages of the transistors M_A and M_B are

$$V_{DA} = V_C - V_T - \sqrt{\frac{2I_{DA}}{K_S}} , \quad (10)$$

$$V_{DB} = V_{in} - V_T - \sqrt{\frac{2I_{DB}}{K_S}} , \quad (11)$$

from (2), where K_S represents the aspect ratio of the transistors M_{AS} and M_{BS}.

Substituting (1) or (2) into (10), the drain voltage V_{DA} of the transistor M_A is given by

$$V_{DA} = V_C - V_T - \sqrt{\frac{K}{K_S}}(V_{in} - V_T) , \quad (12)$$

when the transistor M_A operates in the saturation region, and

$$V_{DA} = V_C - V_T - \sqrt{\frac{K}{K_S}}\sqrt{(V_{in} - V_T - \frac{V_C - V_T}{2})(V_C - V_T)} \quad (13)$$

when the transistor M_A operates in the linear region.

If K_S is sufficiently larger than K, the third term $(K/K_S)^{1/2}$ of (12) and (13) can be assumed to be zero. Then the drain voltage of transistor M_A becomes $V_C - V_T$. Similarly the drain voltage of transistor M_B becomes $V_{in} - V_T$, thus these are satisfied with (7). When V_{in} is lower than the threshold voltage V_T, the transistors M_A and M_{SB} are in the cut-off region and the output currents become zeros.

The performances of the proposed VCCS circuits are analysed through the use of HSPICE simulator. Fig. 4 shows the *I-V* curves of the proposed VCCS circuit in Fig.3. The power supply voltages V_{DD} and V_{SS} for the circuit in Fig. 3 are 1.5V and –1.5V respectively. Here, the input voltage V_{in} and the control voltage V_C are varied from –1.0V to 1.5V. From Fig.4, it is clear that the proposed VCCS circuit operates as the multiplier between the threshold voltage V_T and the supply voltage V_{DD}.

4. 4Q-Multiplier

We propose the 4Q-multiplier, which consists of 4 similar VCCS circuits. Fig.5 shows the proposed 4Q-multiplier. The output currents I_1, I_2, I_3, and I_4 of VCCS are shown as follows,

$$I_1 = K(V_{X1} - V_T)(V_{Y1} - V_T) , \quad (14)$$
$$I_2 = K(V_{X2} - V_T)(V_{Y1} - V_T) , \quad (15)$$

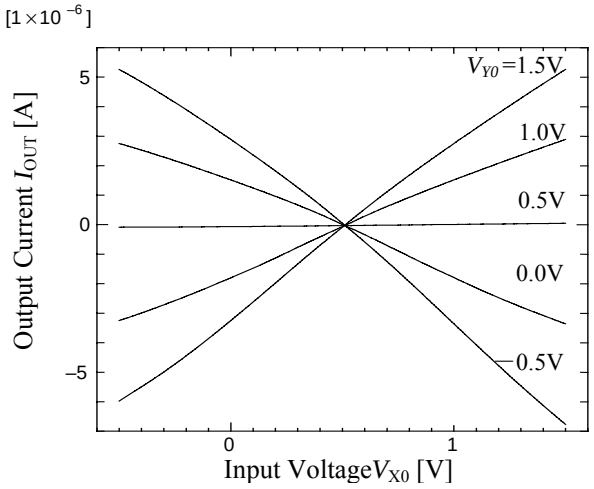

Fig.6 I-V Characteristics of VCCS.

$$I_3 = K(V_{X2} - V_T)(V_{Y2} - V_T), \quad (16)$$

$$I_4 = K(V_{X1} - V_T)(V_{Y2} - V_T). \quad (17)$$

Here, we define the current I_{o1} as sum of the output currents I_1 and I_3, whereas I_{o2} as of I_2 and I_4. Therefore the difference between output currents I_{o1} and I_{o2} yields a multiplication of (V_{X1}-V_{X2}) and (V_{Y1}-V_{Y2}).

$$\begin{aligned} I_{out} &= I_{o1} - I_{o2} \\ &= (I_1 + I_3) - (I_2 + I_4) \\ &= K(V_{X1} - V_{X2})(V_{Y1} - V_{Y2}) \end{aligned} \quad (18)$$

From (18), the output current I_{out} can be realized precisely, because it is independent of the threshold voltage V_T. Fig.6 shows the *I-V* curves of 4Q-multiplier in Fig.5. The power supply voltages V_{DD} and V_{SS} are 1.5V and –1.5V respectively. Here, the input voltages V_{X1} and V_{Y1} are varied from –1.0V to 1.5V and the input voltage V_{X2} and V_{Y2} are 0.5V. From Fig.6, we have confirmed that the proposed 4Q-multiplier operates as the 4Q-multiplier for wide input ranges compared to the power supply voltages. Fig.7 shows the multiplications of two sinusoidal waves, which are 25kHz(dashed) and 2.5kHz(solid). In this simulation, the input voltages V_{X1}, V_{X2}, V_{Y1} and V_{Y2} are set as below,

$$V_{X1} = V_{DC} + A\sin(2\pi f_1), \quad (19)$$

$$V_{X2} = V_{DC} - A\sin(2\pi f_1), \quad (20)$$

$$V_{Y1} = V_{DC} + A\sin(2\pi f_2), \quad (21)$$

$$V_{Y2} = V_{DC} - A\sin(2\pi f_2), \quad (22)$$

where the bias voltage V_{DC}=0.5[V], the amplitude A=1.0[V], frequency f_1=25[kHz], frequency f_2=2.5[kHz] respectively. As a result we confirmed that the proposed circuit carries out the multiplication of two signals.

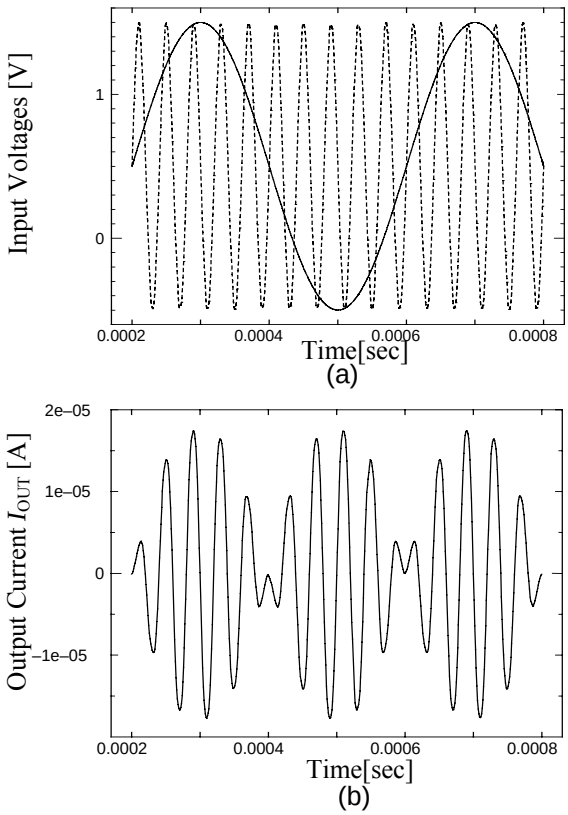

Fig.7 Multiplication of two sinusoidal waves.

6. Conclusion

In this paper, we have proposed a novel 4Q-multiplier, which uses complementally in the saturation and linear regions of MOSFET. Thus the proposed 4Q-multiplier operates between the threshold voltage V_T and the supply voltage V_{DD}. Furthermore we have simulated the proposed circuit by using HSPICE. As a result, we have confirmed that the proposed circuits are useful as the 4Q-multiplier.

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