TECHNOLOGY ROADMAP of DRAM for Three Major manufacturers: Samsung, SK-Hynix and Micron

Oct 2014
Introduction

The ITRS roadmap calls for continued scaling of DRAMS from the present 2X nm node down to sub-20 nm in next few years. Hynix, among others have brought 21 nm DRAM into production. This continued scaling requires high-k dielectrics for the DRAM cell capacitor and materials like HfO$_2$, ZrO$_2$ and AlO$_2$ are being used now, with perovskite-based dielectrics (i.e. SrTiO$_3$) being considered for future applications.

Reorganizing the DRAM cell layout from 6F$^2$ to a 4F$^2$ layout is an option for scaling, though likely difficult to achieve. 4F$^2$ scaling may possible to implement for sub-20 nm nodes by using a capacitorless 1T DRAM cell architecture.

The *memory wall* has been a topic for some time due to limited I/O bandwidth and power consumption constraints.

3D stacking of DRAM dies on a processor core and connected by TSV’s can yield massive inter-die bandwidths and dramatic reductions in access latency.

3D integration is in the works as stand-alone DRAM packages with Samsung and Micron disclosing details of their hybrid memory cubes (HMC), while Hynix’s is offering high bandwidth memory (HBM) modules. We think these stand-alone DRAMs may be a precursor to full integration of stacked DRAM on processor cores.
ITRS Tech. Roadmap

Source: ITRS

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Major Players

DRAM Market Share (4Q13)

Samsung 40%
Micron 30%
SK-Hynix 20%
Nanya 10%
Winbond 5%
PowerChip 5%

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DRAM Production Capacity

Figure 20. Contracting DRAM Capacity Trend

- Samsung
- Hynix
- Micron
- Elpida
- Qimonda
- Others

(8", kwpn)

## DRAM Technology

### As of Today: Samsung

<table>
<thead>
<tr>
<th>Tech. Node</th>
<th>Die Floor Plan</th>
<th>Cell Architecture</th>
<th>Key Technology</th>
</tr>
</thead>
</table>
| 3X (31 nm) | ![Die Floor Plan](image1) | ![Cell Architecture](image2) | - 59nm/93nm/93nm (STI/WL/BL Pitch)  
- 2Gb/Die (DDR3)  
- 36 mm²/Die Area  
- 0.0086 μm²/cell (6F²)  
- TiN Buried WL  
- Single W BL  
- Single SiN MESH  
- ZAZ HK Dielectrics |
| 2X (26 nm) | ![Die Floor Plan](image3) | ![Cell Architecture](image4) | - 52nm/66nm/76nm (STI/WL/BL Pitch)  
- 4Gb/Die (LPDDR3)  
- 40 mm²/Die Area  
- 0.005 μm²/cell (6F²)  
- W/TiN Buried WL  
- Double W BL  
- Double SiN MESH  
- ZAZ HK Dielectrics |

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## DRAM Technology

### As of Today: Micron/Nanya

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</tr>
</thead>
</table>
| **3X (35 nm)** | ![Die Floor Plan](image1.png) | ![Cell Architecture](image2.png) | - 79nm/70nm/87nm (STI/WL/BL Pitch)  
- 2Gb/Die (LPDDR2)  
- 72 mm²/Die Area  
- 0.0086 µm²/cell(6F²)  
- W/TiN Buried WL  
- Single W BL  
- Single SiN MESH  
- ZAZ HK Dielectrics |
| **3X (31 nm)** | ![Die Floor Plan](image3.png) | ![Cell Architecture](image4.png) | - 80nm/62nm/90nm (STI/WL/BL Pitch)  
- 512Mb/Die (DDR3)  
- 68 mm²/Die Area  
- 0.0084 µm²/cell(6F²)  
- W/TiN Buried WL  
- Double W BL  
- Double SiN MESH  
- ZAZ HK Dielectrics |

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DRAM Technology

- **As of Today: SK-Hynix**

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<thead>
<tr>
<th>Tech. Node</th>
<th>Die Floor Plan</th>
<th>Cell Architecture</th>
<th>Key Technology</th>
</tr>
</thead>
</table>
| **3X (31 nm)** | ![3X Die Floor Plan](image) | ![Cell Architecture](image) | - 62nm/88nm/100nm (STI/WL/BL Pitch)  
- 2Gb/Die (DDR3)  
- 35 mm²/Die Area  
- 0.0093 μm²/cell(6F²)  
- W/TiN Buried WL  
- Double W BL  
- Single SiN MESH  
- ZAZ HK Dielectrics |

<table>
<thead>
<tr>
<th>Tech. Node</th>
<th>Die Floor Plan</th>
<th>Tech. Node</th>
<th>Die Floor Plan</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>2X (26 nm)</strong></td>
<td><img src="image" alt="2X Die Floor Plan" /></td>
<td><strong>2Y (21 nm)</strong></td>
<td><img src="image" alt="2Y Die Floor Plan" /></td>
</tr>
</tbody>
</table>

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Key DRAM Technologies

- As of Today: Key Technologies

1. **Fin-type 3D Channel Engineering**
   - Channel & S/D IIP, Raised Si(Ge) S/D
   - Low damage process
   - Bulk-Fin $\rightarrow$ PD Fin $\rightarrow$ FD Fin

2. **RCAT 3D Buried WL Integration**
   - Uniform Recess Channel
   - Low damage (recess surface)
   - Uniform gate oxide thickness/quality
   - Buried WL materials (Metal gate)

3. **High-K Dielectric Cap. & MESH**
   - Quantum Engineering (Multi-layer HKD)
   - Ultra-thin layer depo./annealing tools
   - Cell cap. 20~30fF/cell, Stable MESH

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DRAM Technology

- Further Scaling Down: 1X, 1Y or 0X nm?

1. Fin-type 3D Channel Engineering?
2. RCAT 3D Buried WL Integration?
3. High-K Dielectric Cap. & MESH?

@1T/1C, 6F²

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DRAM Technology

- Further Scaling Down: 1X, 1Y or 0X nm?

Any Other Candidates?

- UTBOX
- FD-SOI
- Capacitorless DRAM (4F²)

1Y, 1Z, 0X nm

by Fujitsu Lab.
DRAM Technology

- Near Future DRAM Technology: Scalability
  - 1T/1C DRAM with FinFET

![Diagram of DRAM Technology](image)

Silicide
SOI (< 10 nm, Channel region < 7 nm)
BOX (< 10 nm)

BJT-Type on SOI
FED-Type on SOI
BJT-Type (Vertical)

T. Imamoto, JJAP 2014
DRAM Technology

- DRAM Technology Roadmap

Cell Layout
- 8F²
- 6F²
- 4F²

Tech. Node
- 100nm
- 80nm
- 65nm
- 45nm
- 26nm
- 15nm
- 10nm
- 70nm
- 57nm
- 31nm
- 21nm

Cell TR
- 2D Planar
- Vertical Gate
- RCAT
- S-Fin/RCAT/BWL
- 1T DRAM
- S-Fin/RCAT
- UTB-SOI/Fin

Mobile DRAM
- LPDDR 1.8V, <512MB
- LPDDR2 1.2V, <2GB
- LPDDR3 1.2V, <3GB
- LPDDR4, Wide IO2 1.1V, >4GB
- LPDDR5 1.0V, >16GB

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## DRAM Technology Roadmaps (by manufacturer)

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>2014</th>
<th>2015</th>
<th>2016</th>
</tr>
</thead>
<tbody>
<tr>
<td>ITRS DRAM Roadmap (2013 Ver.)</td>
<td>26 nm</td>
<td>24 nm</td>
<td>22 nm</td>
</tr>
<tr>
<td><strong>Samsung</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>20 nm 4GB DDR3</td>
<td></td>
<td>1X nm</td>
<td>1X nm</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td><strong>Micron</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2X nm Sampling 2 GB HMC</td>
<td></td>
<td>1X nm</td>
<td>1Y nm</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Intel</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>21 nm LPDDR3</td>
<td></td>
<td></td>
<td>1Y nm</td>
</tr>
<tr>
<td></td>
<td>20 nm DDR4</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Micron Memory Roadmap

Memory Technology Timelines

- **Calendar Years**: 2013, 2014, 2015, 2016, 2017
- **DRAM**: 2013 - 25nm, 2014 - 20nm, 2015 - 1Xnm, 2016 - 1Ynm
- **NAND**: 2013 - 16nm, 2014 - 3D NAND Gen 1, 2015 - 3D NAND Gen 2
- **Emerging**: 2013 - PCM, 2014 - New Memory A Gen 1, 2015 - New Memory A Gen 2, 2016 - New Memory B Gen 1

Position in time indicates expectation of volume capability

- Increased focus on DRAM technology position enabled following Elpida acquisition
- Maintain strong planar NAND position with 16nm volume ramp in 2014
- Market enablement with vertical NAND in 2014, ramp in 2015
- Enable disruptive new memory technology and position for ramp in 2015
- Core technology leadership well positioned to enable Micron's diverse product portfolio

Source: http://www.enterprisetech.com/2014/02/20/micron-pushes-memory-roadmap-several-routes/

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Future DRAM Technologies
Hybrid Memory Cube
High Bandwidth Memory

SK Hynix HBM
Micron HMC

Source: http://www.memcon.com/pdfs/proceedings2013/keynotes/New_Directions_in_Memory_Architecture.pdf

Source: http://www.enterprisetech.com/2014/02/20/micron-pushes-memory-roadmap-several-routes/

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At the high-performance end of the memory market, Micron is poised to deliver on its Hybrid Memory Cube (HMC) promise, with initial interest coming from the supercomputing and networking communities; high frequency traders are also probably interested, but generally don’t talk about their plans.

The company has 2 GB and 4 GB options currently shipping as engineering samples and multiple partner demo platforms are up and running.
SK-Hynix said today that it has developed a next generation HBM, or high bandwidth memory DRAM chips using a 3D TSV, or through silicon via chip packaging technology.

Source: [http://itersnews.com/?p=62940](http://itersnews.com/?p=62940)

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SK-Hynix High Bandwidth Memory (HBM)

Increased demand for high bandwidth DRAM is driving the development of TSV technology.

Hynix’s HBM comprises 4-hi core DRAM and a base logic die at the bottom.


“A 1.2V 8GB 8-channel 128GB/s High Bandwidth Memory (HBM) Stacked DRAM with Effective Microbump I/O Test Methods Using 29nm Process and TSV” Dong Uk Lee et al. ISSC 2014 pp 432-434

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## LPDDR4 and WIO2 Overview

<table>
<thead>
<tr>
<th></th>
<th>LPDDR3 &amp; LPDDR3E</th>
<th>LPDDR4</th>
<th>Wide IO2</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Die Organization</strong></td>
<td>1ch X 8 banks X 32 IO</td>
<td>2ch X 8 banks X 16 IO</td>
<td>4ch X 8 banks X 64 IO</td>
</tr>
<tr>
<td><strong>Channel #</strong></td>
<td>1</td>
<td>2</td>
<td>4 &amp; 8</td>
</tr>
<tr>
<td><strong>Bank #</strong></td>
<td>8</td>
<td>8 per channel (16 per die)</td>
<td>32 per die</td>
</tr>
<tr>
<td><strong>Density</strong></td>
<td>4Gb – 32Gb</td>
<td>4Gb – 32Gb</td>
<td>8Gb – 32Gb</td>
</tr>
<tr>
<td><strong>Page Size</strong></td>
<td>4KByte</td>
<td>2KByte</td>
<td>4KByte (4ch die), 2K (8 ch die)</td>
</tr>
<tr>
<td><strong>Max BW per die</strong></td>
<td>6.4GB/s, 8.5GB/s (overclocking)</td>
<td>12.8GB/s, 17GB/s (overclocking)</td>
<td>25.6GB/s &amp; 51.2GB/s, 34GB/s &amp; 68GB/s (overclocking)</td>
</tr>
<tr>
<td><strong>Max IO Speed</strong></td>
<td>2133Mbps</td>
<td>4266Mbps</td>
<td>1066Mbps</td>
</tr>
<tr>
<td><strong>Signal Pin #</strong></td>
<td>62 per die</td>
<td>66 per die</td>
<td>~430 per die (4 ch die), ~850 per die (8 ch die)</td>
</tr>
<tr>
<td><strong>Package</strong></td>
<td>POP, MCP</td>
<td>POP, MCP</td>
<td>KGD</td>
</tr>
</tbody>
</table>

Source: “Memory Technology Roadmap” Hung Vuong Qualcomm Technologies (2013)  
H_Vuong_Mobile_Forum_May_2013 Mobile

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Summary

**DRAM**
- 1T/1C DRAM until y2018 (12 nm, Fin & UTB-SOI)
- 1T DRAM or vertical DRAM until y2022 with sub-0.8V