TECHNOLOGY ROADMAP of DRAM for Three Major manufacturers: Samsung, SK-Hynix and Micron

Oct 2014

Introduction

The ITRS roadmap calls for continued scaling of DRAMS from the present 2X nm node down to sub-20 nm in next few years. Hynix, among others have brought 21 nm DRAM into production. This continued scaling requires high-k dielectrics for the DRAM cell capacitor and materials like HfO_2, ZrO_2 and AlO_2 are being used now, with perovskite-based dielectrics (i.e. $SrTiO_3$) being considered for future applications.

Reorganizing the DRAM cell layout from $6F^2$ to a $4F^2$ layout is an option for scaling, though likely difficult to achieve. $4F^2$ scaling may possible to implement for sub-20 nm nodes by using a capacitorless 1T DRAM cell architecture.

The *memory wall* has been a topic for some time due to limited I/O bandwidth and power consumption constraints.

3D stacking of DRAM dies on a processor core and connected by TSV's can yield massive inter-die bandwidths and dramatic reductions in access latency.

3D integration is in the works as stand-alone DRAM packages with Samsung and Micron disclosing details of their hybrid memory cubes (HMC), while Hynix's is offering high bandwidth memory (HBM) modules. We think these stand-alone DRAMs may be a precursor to full integration of stacked DRAM on processor cores.

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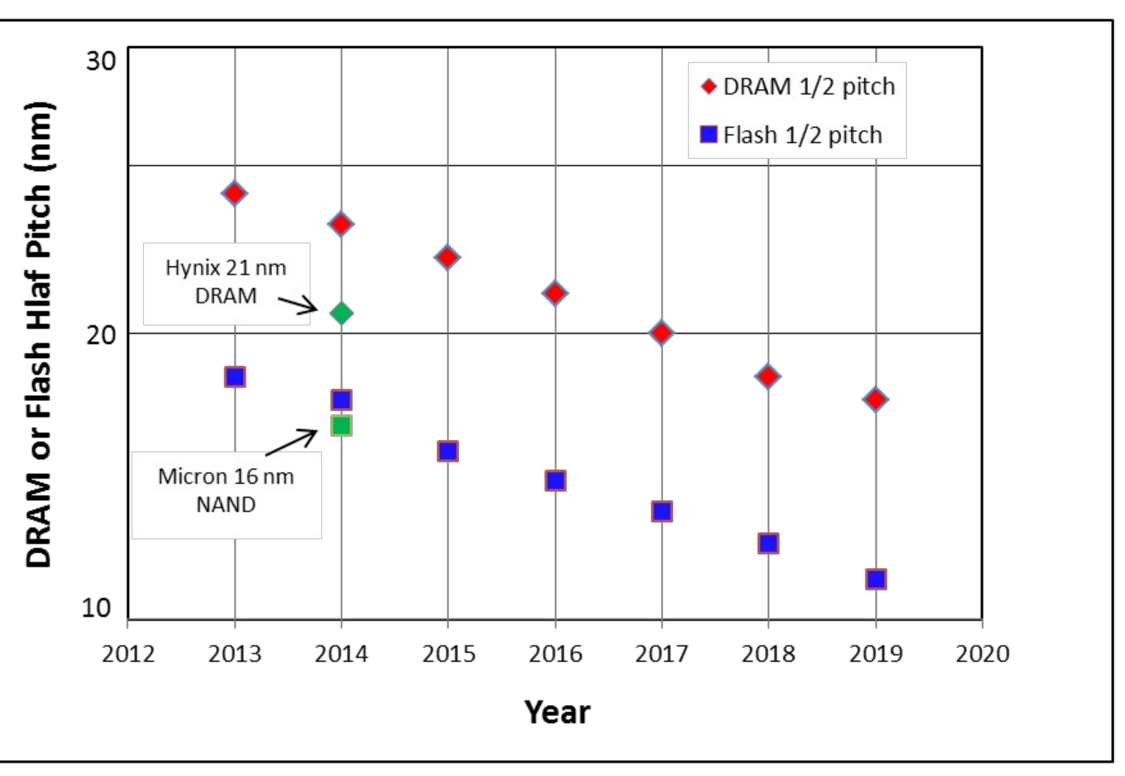
ITRS Tech. Roadmap



Source: ITRS

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Major Players

DRAM Market Share (4Q13)

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(%)
50
40
30
20
10

SAMSUNG
Micron + ELPIDA
SK hynix
NANYA
winbond
Powerchip

Samsung Micron SK-Hynix Nanya Winbond PowerChip

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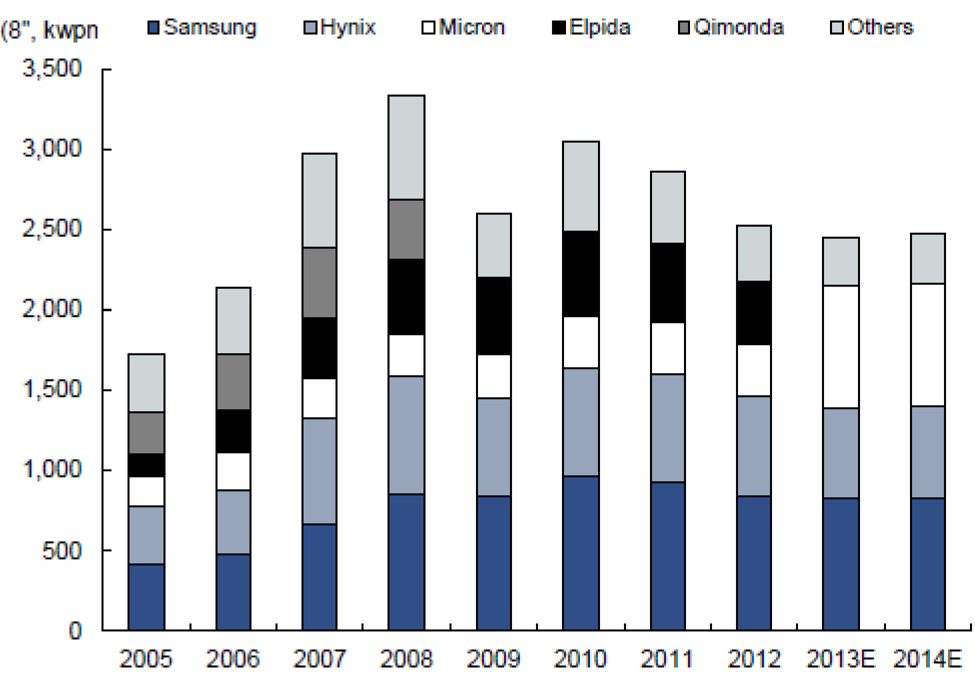
DRAM Production Capacity



26 September 2013 | 36 pages

Global Memory Sector

Supply Discipline: Paradigm Shift to Lead to Multi-Year Growth

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DRAM Technology

❑ As of Today: Samsung

Tech. Node	Die Floor Plan	Cell Architecture	Key Technology
3X (31 nm)			▪ 59nm/93nm/93nm (STI/WL/BL Pitch) ▪ 2Gb/Die (DDR3) ▪ 36 mm^2/Die Area ▪ 0.0086 μm^2/cell ($6F^2$) ▪ TiN Buried WL ▪ Single W BL ▪ Single SiN MESH ▪ ZAZ HK Dielectrics
2X (26 nm)			▪ 52nm/66nm/76nm (STI/WL/BL Pitch) ▪ 4Gb/Die (LPDDR3) ▪ 40 mm^2/Die Area ▪ 0.005 μm^2/cell ($6F^2$) ▪ W/TiN Buried WL ▪ Double W BL ▪ Double SiN MESH ▪ ZAZ HK Dielectrics

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DRAM Technology

❑ As of Today: Micron/Nanya

Tech. Node	Die Floor Plan	Cell Architecture	Key Technology
3X (35 nm)			▪ 79nm/70nm/87nm (STI/WL/BL Pitch) ▪ 2Gb/Die (LPDDR2) ▪ 72 mm^2/Die Area ▪ 0.0086 μm^2/cell($6F^2$) ▪ W/TiN Buried WL ▪ Single W BL ▪ Single SiN MESH ▪ ZAZ HK Dielectrics
3X (31 nm)			▪ 80nm/62nm/90nm (STI/WL/BL Pitch) ▪ 512Mb/Die (DDR3) ▪ 68 mm^2/Die Area ▪ 0.0084 μm^2/cell($6F^2$) ▪ W/TiN Buried WL ▪ Double W BL ▪ Double SiN MESH ▪ ZAZ HK Dielectrics

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DRAM Technology

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❑ As of Today: SK-Hynix

Tech. Node	Die Floor Plan	Cell Architecture	Key Technology
3X (31 nm)			▪ 62nm/88nm/100nm (STI/WL/BL Pitch) ▪ 2Gb/Die (DDR3) ▪ 35 mm²/Die Area ▪ 0.0093 µm²/cell(6F²) ▪ W/TiN Buried WL ▪ Double W BL ▪ Single SiN MESH ▪ ZAZ HK Dielectrics

Tech. Node	Die Floor Plan	Tech. Node	Die Floor Plan
2X (26 nm)		2Y (21 nm)	

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Key DRAM Technologies

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❑ As of Today: Key Technologies

1 Fin-type 3D Channel Engineering

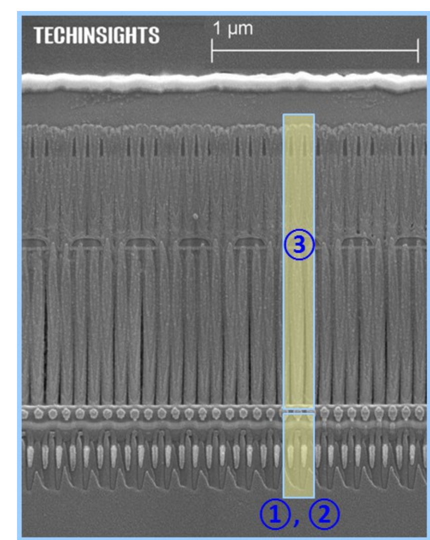
- ✓Channel & S/D IIP, Raised Si(Ge) S/D
- ✓Low damage process
- ✓Bulk-Fin → PD Fin → FD Fin

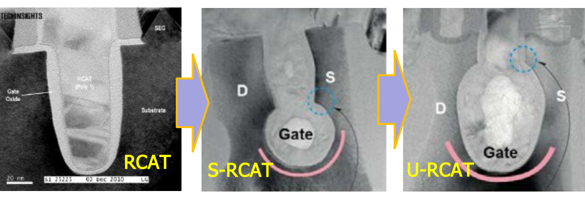
2 RCAT 3D Buried WL Integration

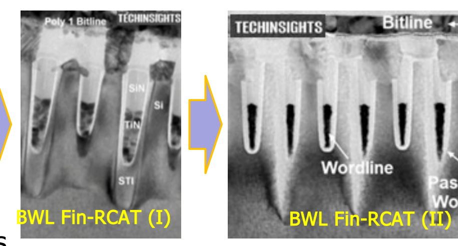
- ✓Uniform Recess Channel
- ✓Low damage (recess surface)
- ✓Uniform gate oxide thickness/quality
- ✓Buried WL materials (Metal gate)

3 High-K Dielectric Cap. & MESH

- ✓Quantum Engineering (Multi-layer HKD)
- ✓Ultra-thin layer depo./annealing tools
- ✓Cell cap. 20~30fF/cell, Stable MESH







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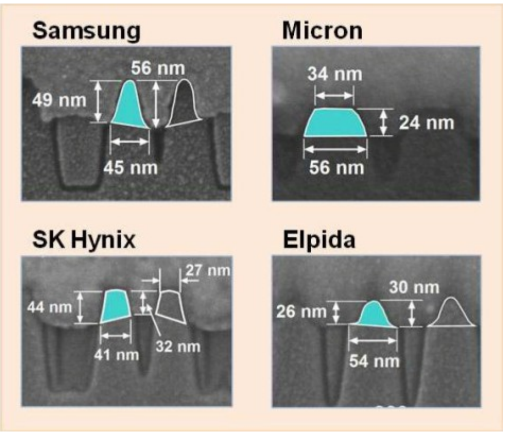
DRAM Technology

❑ Further Scaling Down: 1X, 1Y or 0X nm?

1. Fin-type 3D Channel Engineering ?
2. RCAT 3D Buried WL Integration ?
3. High-K Dielectric Cap. & MESH ?

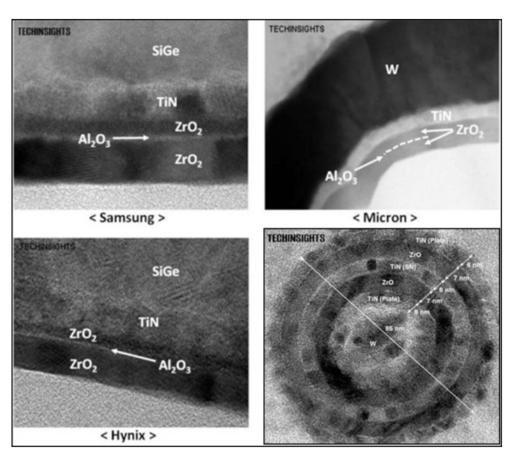
@1T/1C, $6F^2$



<Fin Structure>

Samsung Micron SK Hynix Elpida

<RCAT Structure>



<HK Dielectrics/Capacitor>

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DRAM Technology

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❑ Further Scaling Down: 1X, 1Y or 0X nm?

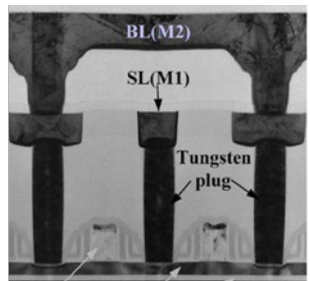
4 Any Other Candidates ?

UTBOX

FD-SOI

Capacitorless DRAM ($4F^2$)

1Y, 1Z, 0X nm



by Fujitsu Lab.

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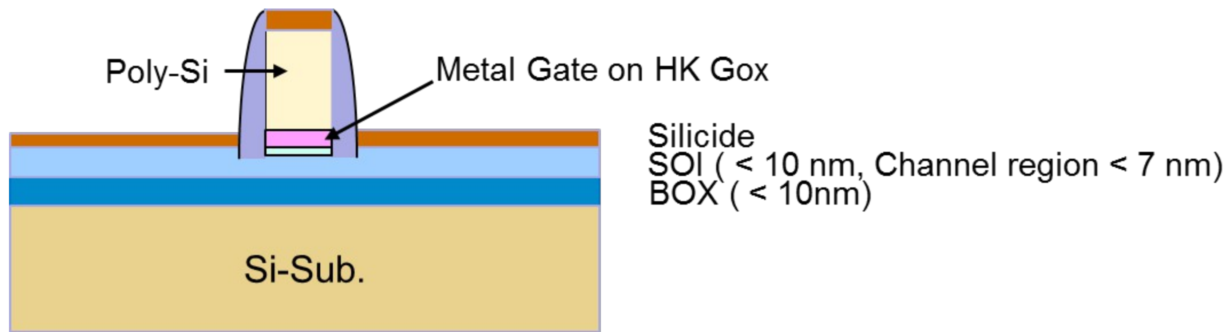
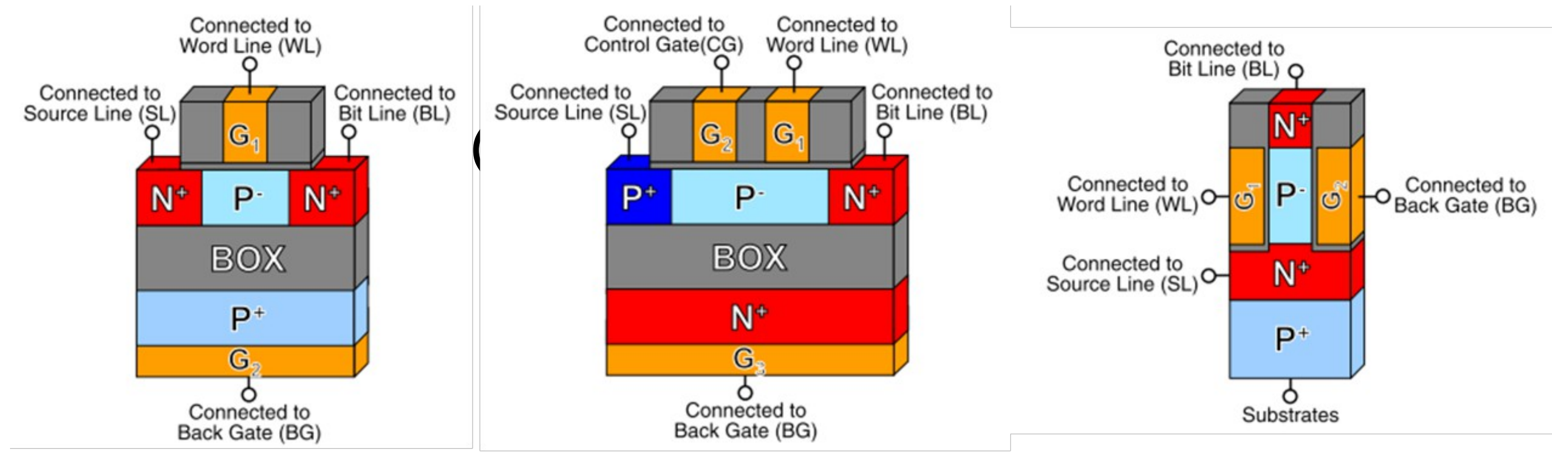
DRAM Technology

❑ Near Future DRAM Technology: Scalability

✓ 1T/1C DRAM with FinFET





BJT-Type on SOI

FED-Type on SOI

BJT-Type (Vertical)

T. Imamoto, JJAP 2014

DRAM Technology

❑ DRAM Technology Roadmap

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Cell Layout

$8F^2$

$6F^2$

$4F^2$

Tech. Node

100nm
80nm
70nm
65nm
57nm
45nm
31nm
26nm
21nm
15nm
10nm

Cell TR

2D Planar
RCAT
S-Fin/RCAT
S-Fin/RCAT/BWL
Vertical Gate
1T DRAM
UTB-SOI/Fin

Mobile DRAM

LPDDR
1.8V, <512MB

LPDDR2
1.2V, <2GB

LPDDR3
1.2V, <3GB

LPDDR4, Wide IO2
1.1V, >4GB

LPDDR5
1.0V, >16GB

2000 2005 2010 2015 2020

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DRAM Technology Roadmaps (by manufacturer)

Manufacturer	2014	2015	2016
ITRS DRAM Roadmap (2013 Ver.)	26 nm	24 nm	22 nm
SAMSUNG	20 nm 4GB DDR3	1X nm	1X nm
Micron / intel	2X nm Sampling 2 GB HMC	1X nm	1Y nm
SK hynix	21 nm LPDDR3	1X 20 nm DDR4	1Y nm

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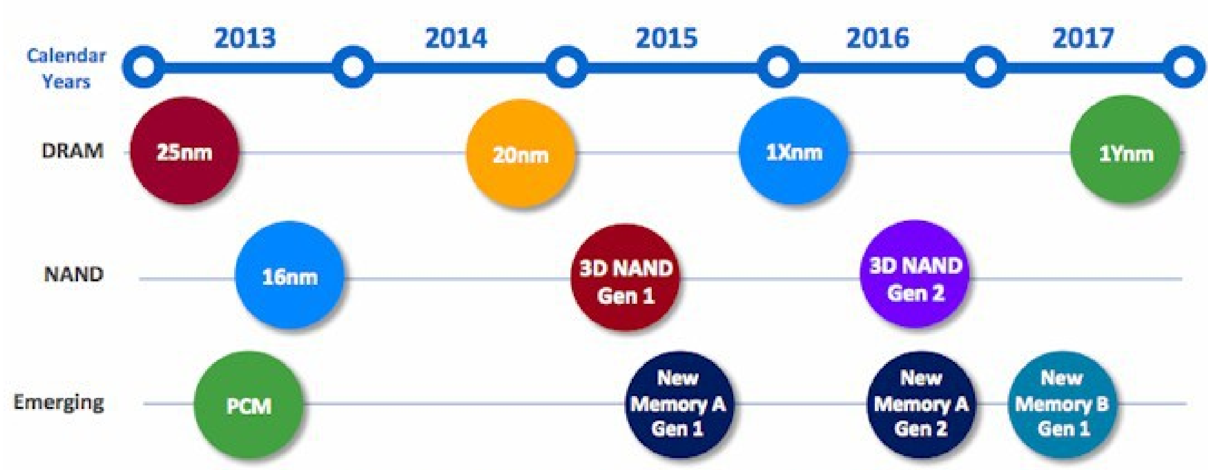
Micron Memory Roadmap

Memory Technology Timelines



Position in time indicates expectation of volume capability

- Increased focus on DRAM technology position enabled following Elpida acquisition
- Maintain strong planar NAND position with 16nm volume ramp in 2014
- Market enablement with vertical NAND in 2014, ramp in 2015
- Enable disruptive new memory technology and position for ramp in 2015
- Core technology leadership well positioned to enable Micron's diverse product portfolio

Source: http://www.enterprisetech.com/2014/02/20/micron-pushes-memory-roadmap-several-routes/

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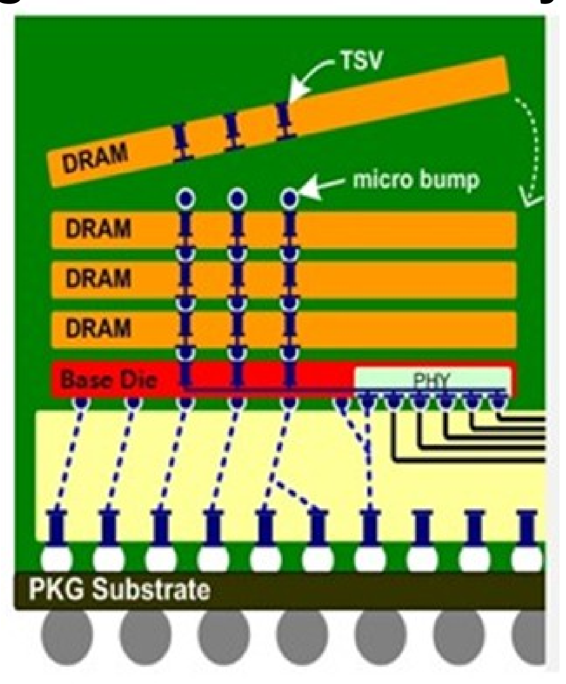
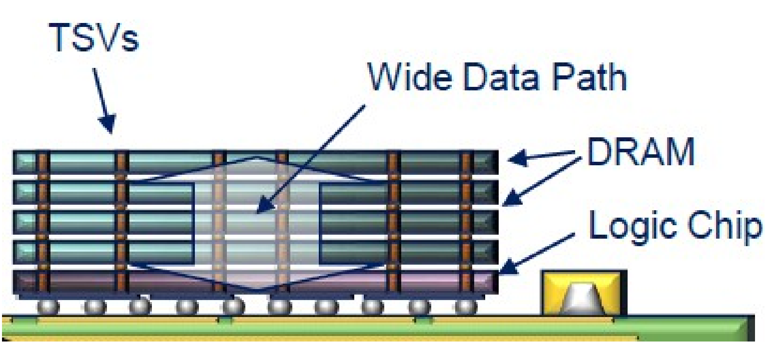
Future DRAM Technologies

Hybrid Memory Cube
High Bandwidth Memory



SK Hynix HBM



Micron HMC

Source: http://www.memcon.com/pdfs/proceedings2013/keynotes/New_Directions_in_Memory_Architecture.pdf

Source: http://www.enterprisetech.com/2014/02/20/micron-pushes-memory-roadmap-several-routes/
http://www.hotchips.org/wp-content/uploads/hc_archives/hc23/HC23.18.3-memory-FPGA/HC23.18.320-HybridCube-Pawlowski-Micron.pdf

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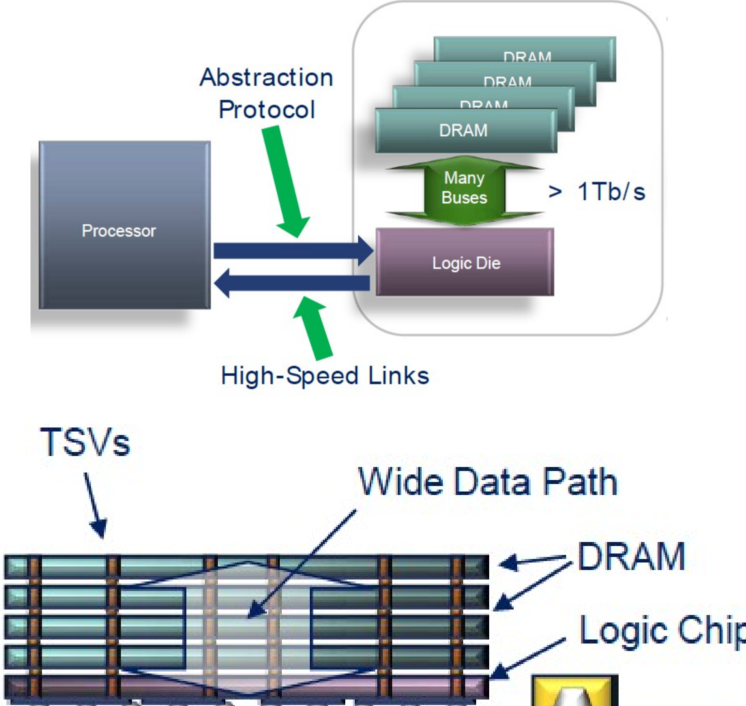
Micron Hybrid Memory Cube

At the high-performance end of the memory market, Micron is poised to deliver on its Hybrid Memory Cube (HMC) promise, with initial interest coming from the supercomputing and networking communities; high frequency traders are also probably interested, but generally don't talk about their plans.

The company has 2 GB and 4 GB options currently shipping as engineering samples and multiple partner demo platforms are up and running.



Source: http://www.enterprisetech.com/2014/02/20/micron-pushes-memory-roadmap-several-routes/
http://www.hotchips.org/wp-content/uploads/hc_archives/hc23/HC23.18.3-memory-FPGA/HC23.18.320-HybridCube-Pawlowski-Micron.pdf

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SK-Hynix High Bandwidth Memory (HBM)

SK-Hynix said today that it has developed a next generation HBM, or high bandwidth memory DRAM chips using a 3D TSV, or through silicon via chip packaging technology.

Source: http://itersnews.com/?p=62940
https://www.skhynix.com/gl/products/graphics/graphics_info.jsp

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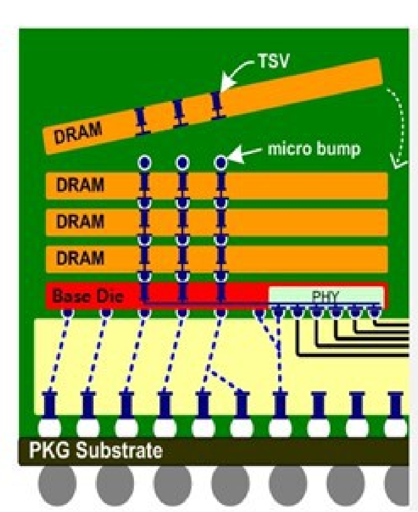
SK-Hynix High Bandwidth Memory (HBM)

Increased demand for high bandwidth DRAM is driving the development of TSV technology.

Hynix's HBM comprises 4-hi core DRAM and a base logic die at the bottom.



ITEM	TARGET
Burst Length	2, 4
Stack Density	1GByte per stack (2Gbit per slice)
Channel / Slice	2
Banks / Channel	8
IO / Channel	128
Prefetch / Channel	32B (128x2bit)
Channels / Stack	8
Total TSV Data IO Width	1024
Clock Speed	500MHz
Peak Read BW / Stack	128 GB/s
Page Size	2KB
Data Parity	1 bit / 32 bit
DRAM Core Voltage	1.2V
Logic Buffer IO Voltage	1.2V

Source: http://www.i-micronews.com/news/SK-Hynix-readying-3D-stacked-memory-commercialization-closer,10000.html

"A 1.2V 8GB 8-channel 128GB/s High Bandwidth Memory (HBM) Stacked DRAM with Effective Microbump I/O Test Methods Using 29nm Process and TSV" Dong Uk Lee et al. ISSC 2014 pp 432-434

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LPDDR4 and WIO2 Overview

	LPDDR3 & LPDDR3E	LPDDR4	Wide IO2
Die Organization	1ch X 8 banks X 32 IO	2ch X 8banks X16 IO	4ch X 8banks X 64 IO
Channel #	1	2	4 & 8
Bank #	8	8 per channel (16 per die)	32 per die
Density	4Gb – 32Gb	4Gb – 32Gb	8Gb – 32Gb
Page Size	4KByte	2KByte	4KByte (4ch die), 2KB (8ch die)
Max BW per die	6.4GB/s, 8.5GB/s (overclocking)	12.8GB/s, 17GB/s (overclocking)	25.6GB/s & 51.2GB/s 34GB/s & 68GB/s(overclocking)
Max IO Speed	2133Mbps	4266Mbps	1066Mbps
Signal Pin #	62 per die	66 per die	~430 per die (4ch die), ~850 per die(8ch die)
Package	POP, MCP	POP, MCP	KGD,

JEDEC Global Standards for the Microelectronics Industry

Source: "Memory Technology Roadmap" Hung Vuong Qualcomm Technologies (2013) H_Vuong_Mobile_Forum_May_2013 Mobile

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Summary

DRAM

- ✓ 1T/1C DRAM until y2018 (12 nm, Fin & UTB-SOI)
- ✓ 1T DRAM or vertical DRAM until y2022 with sub-0.8V

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