

SIMPLIS User's Guide

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SIMetrix / SIMPLIS

- SIMetrix / SIMPLIS is developed by **Transim**.
- It's a software package which contains two different software : SIMetrix and SIMPLIS.



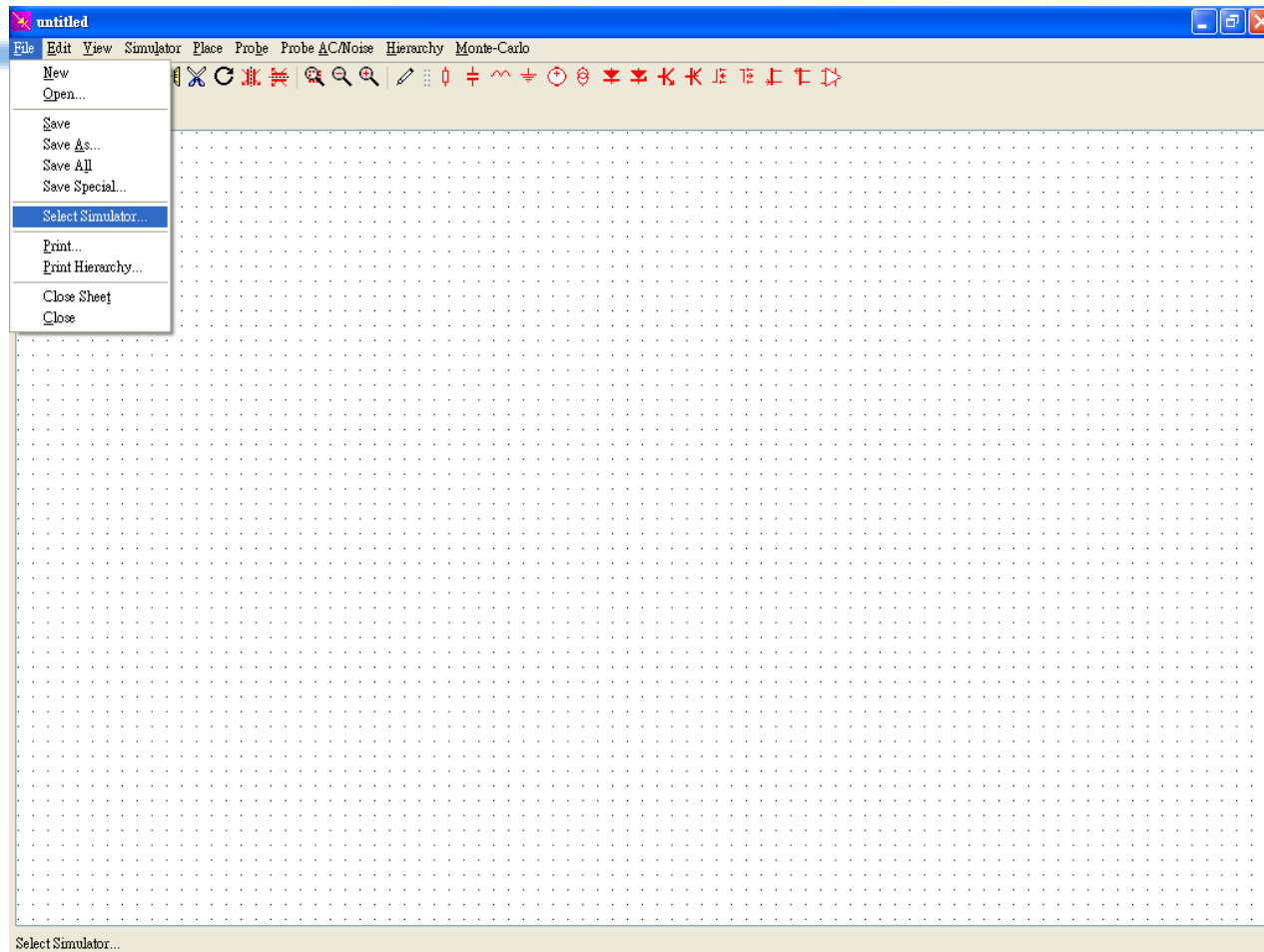
SiMetrix / SIMPLIS

- SiMetrix is more like an enhanced mode of traditional SPICE simulators. Faster analysis speed compared to traditional SPICEs.
- SIMPLIS is developed especially for **switching power supplies**. Its fast AC analysis is the reason why it is popular used by PE designers.

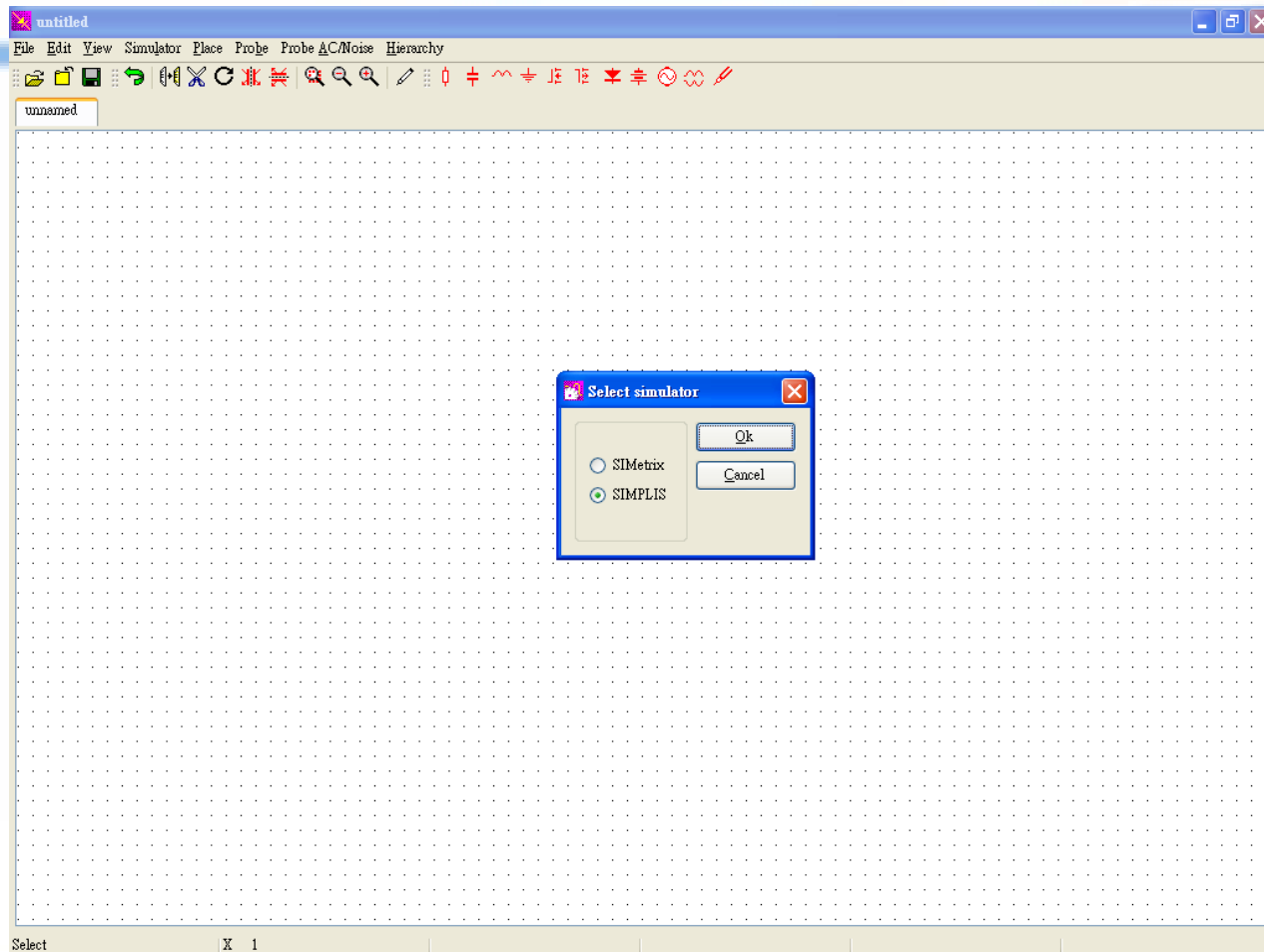
Why SIMPLIS?

- There are 2 reformations of SIMPLIS compared with traditional SPICEs □
 - 1.Can run AC simulation in switch model
 - 2.Faster Bias Point simulation achieved by POP simulation

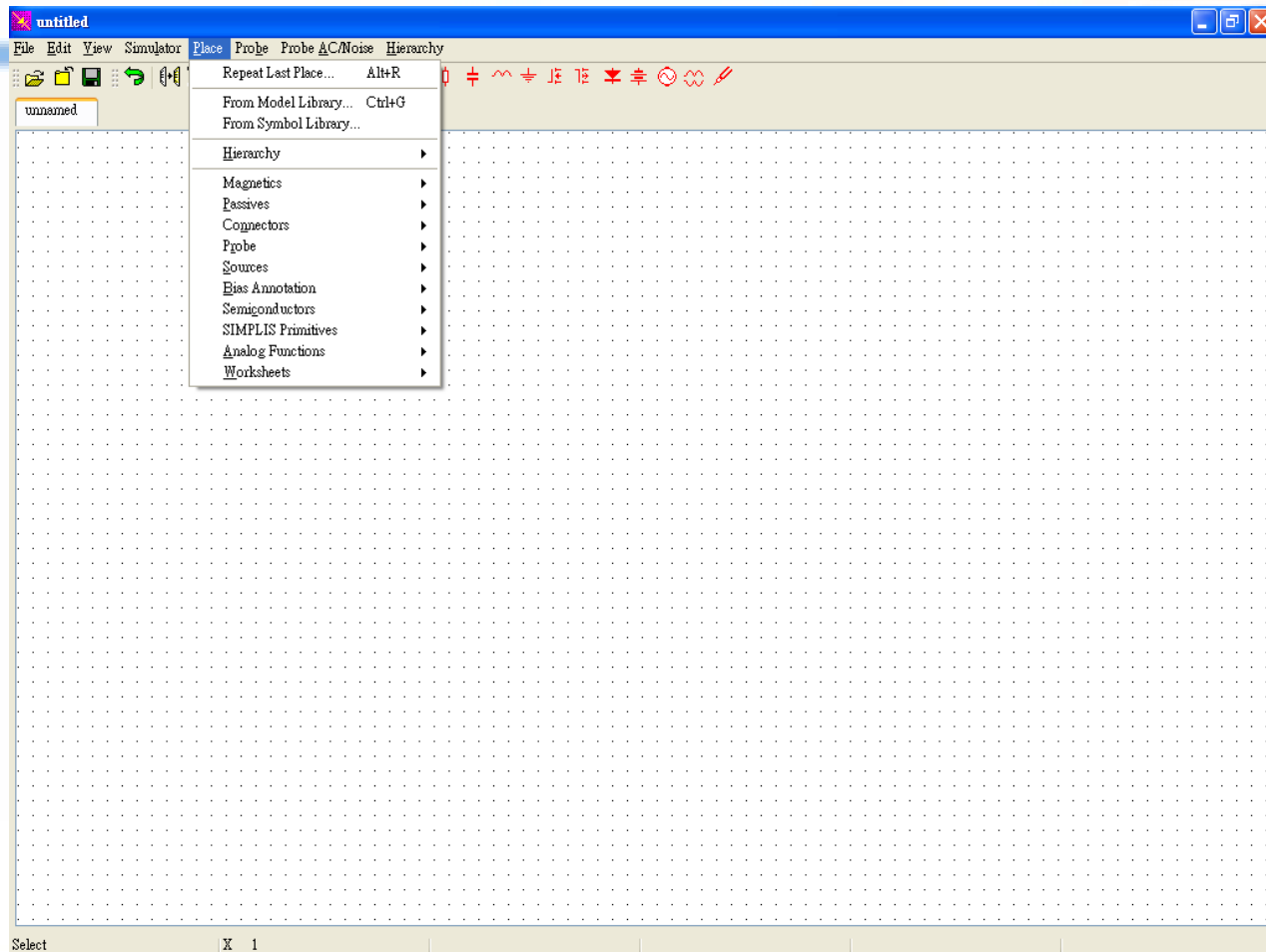
Buck Converter (Open Loop)



Buck Converter (Open Loop)

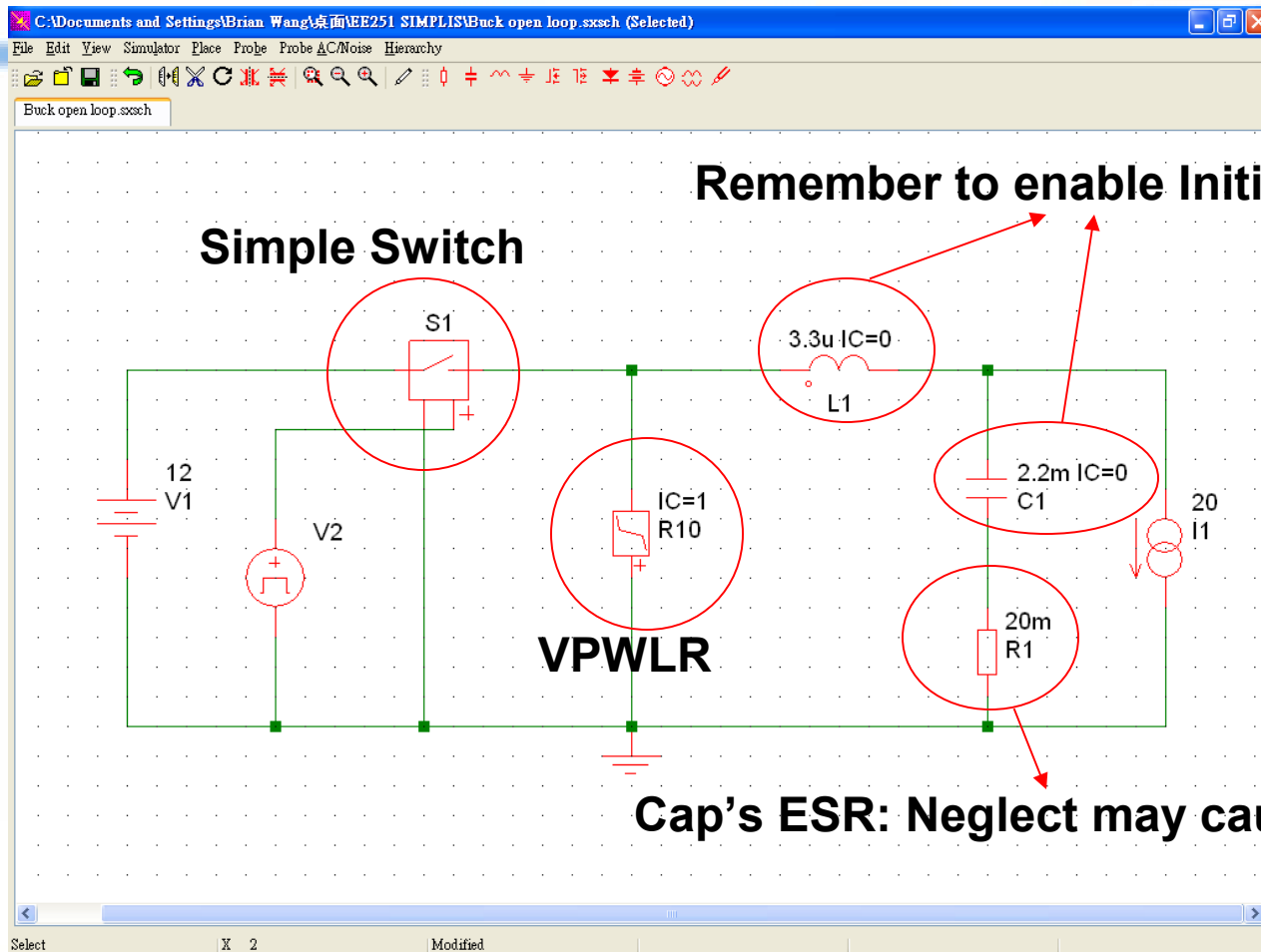


Buck Converter (Open Loop)



All the components needed can be found in “Place” 9

Buck Converter (Open Loop)

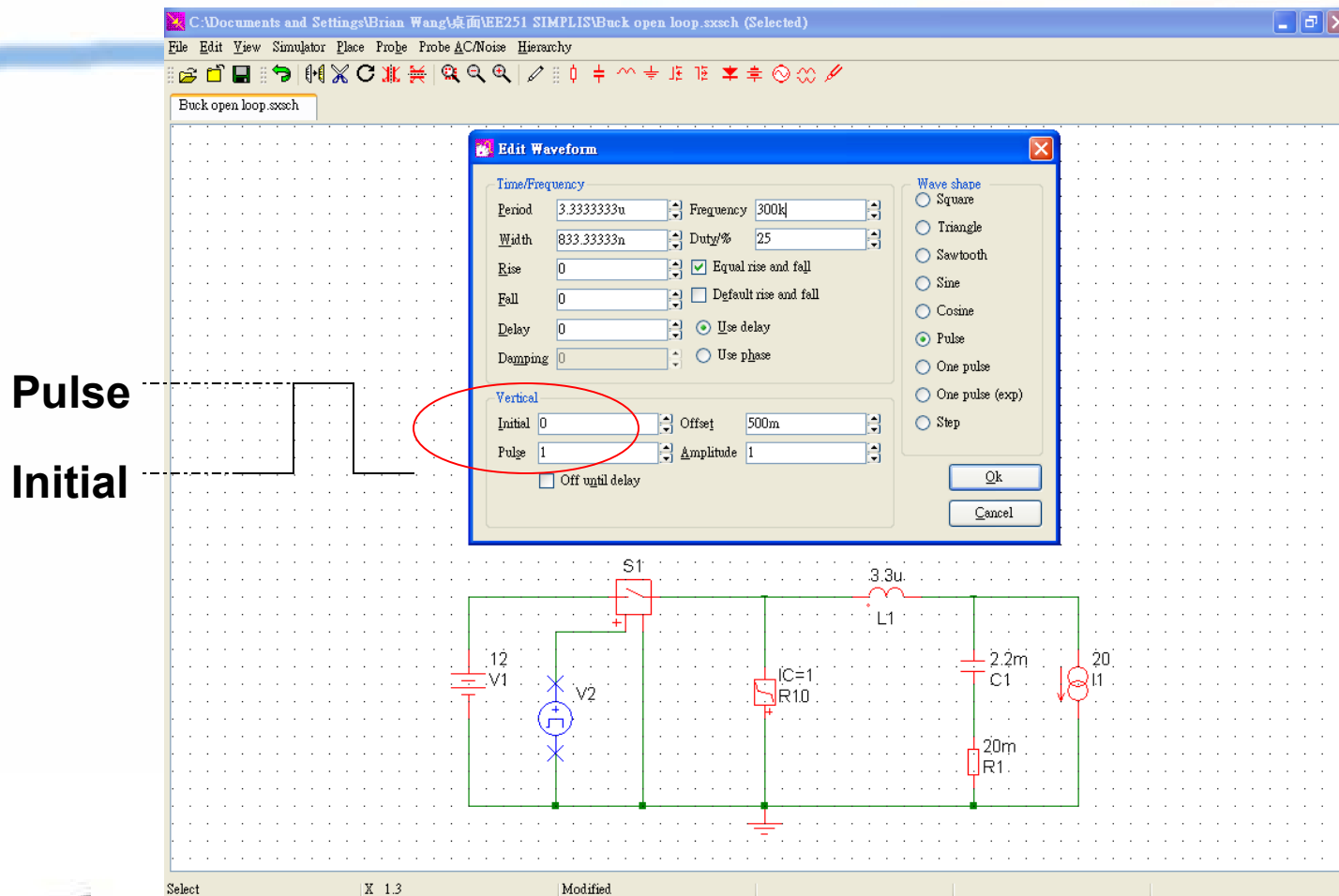


Remember to enable Initial conditions

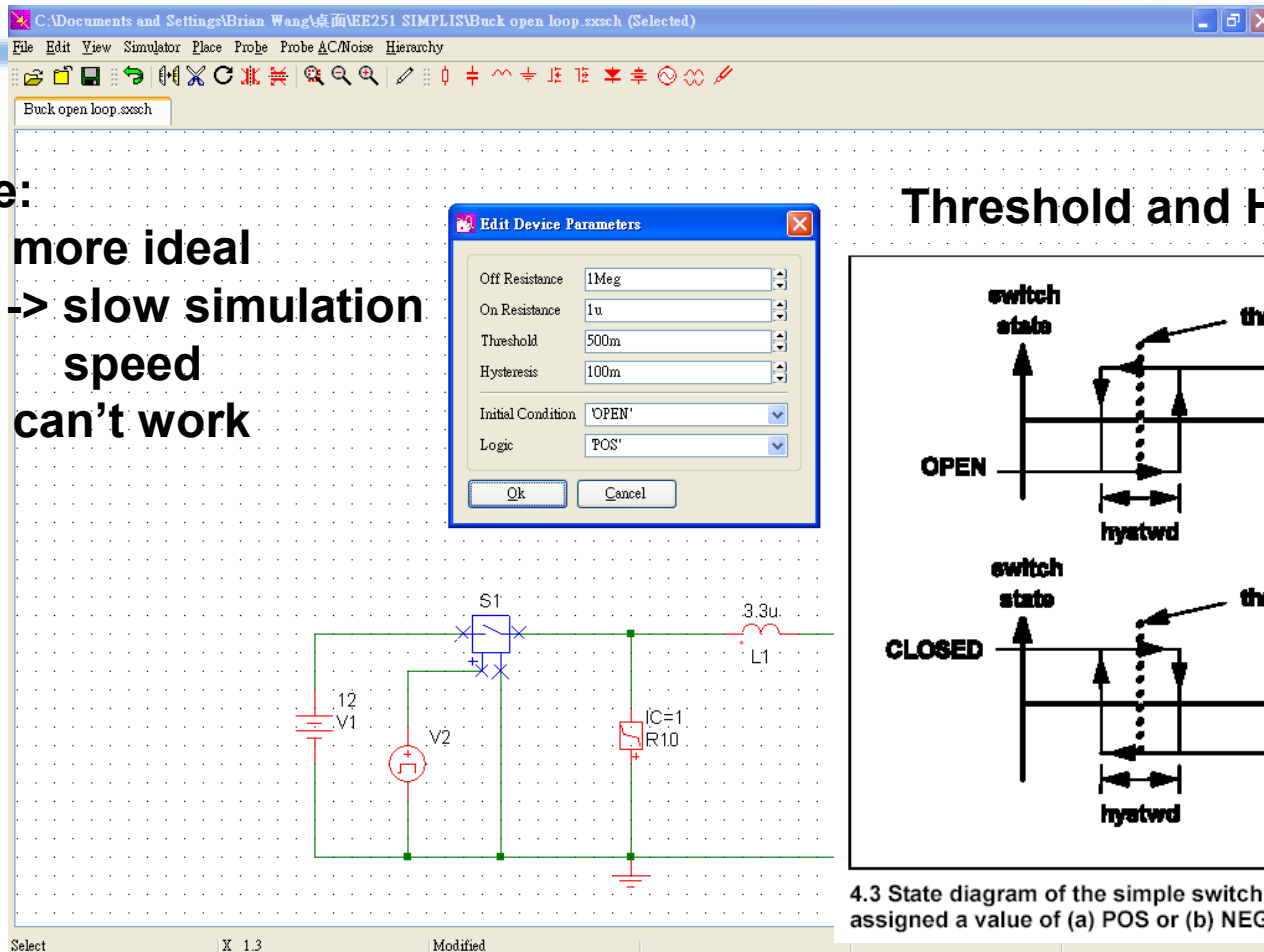
Cap's ESR: Neglect may cause errors

Ideal components (Simple switch and VPWL resistor)

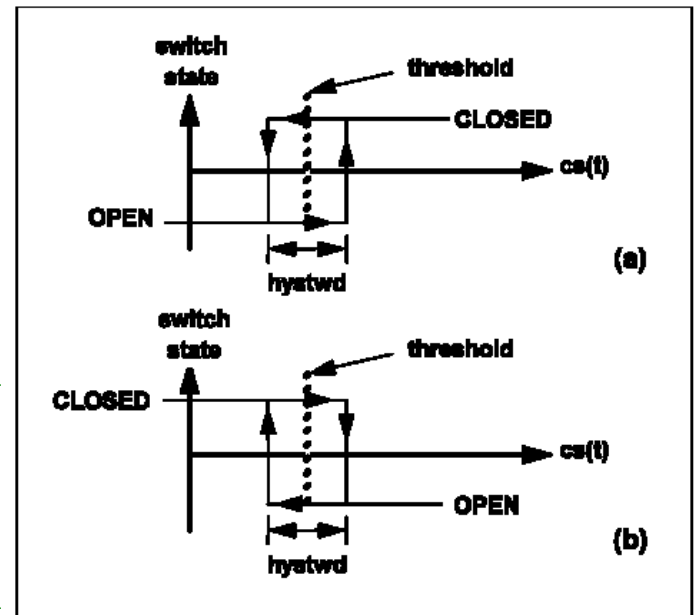
Buck Converter (Open Loop)



Buck Converter (Open Loop)

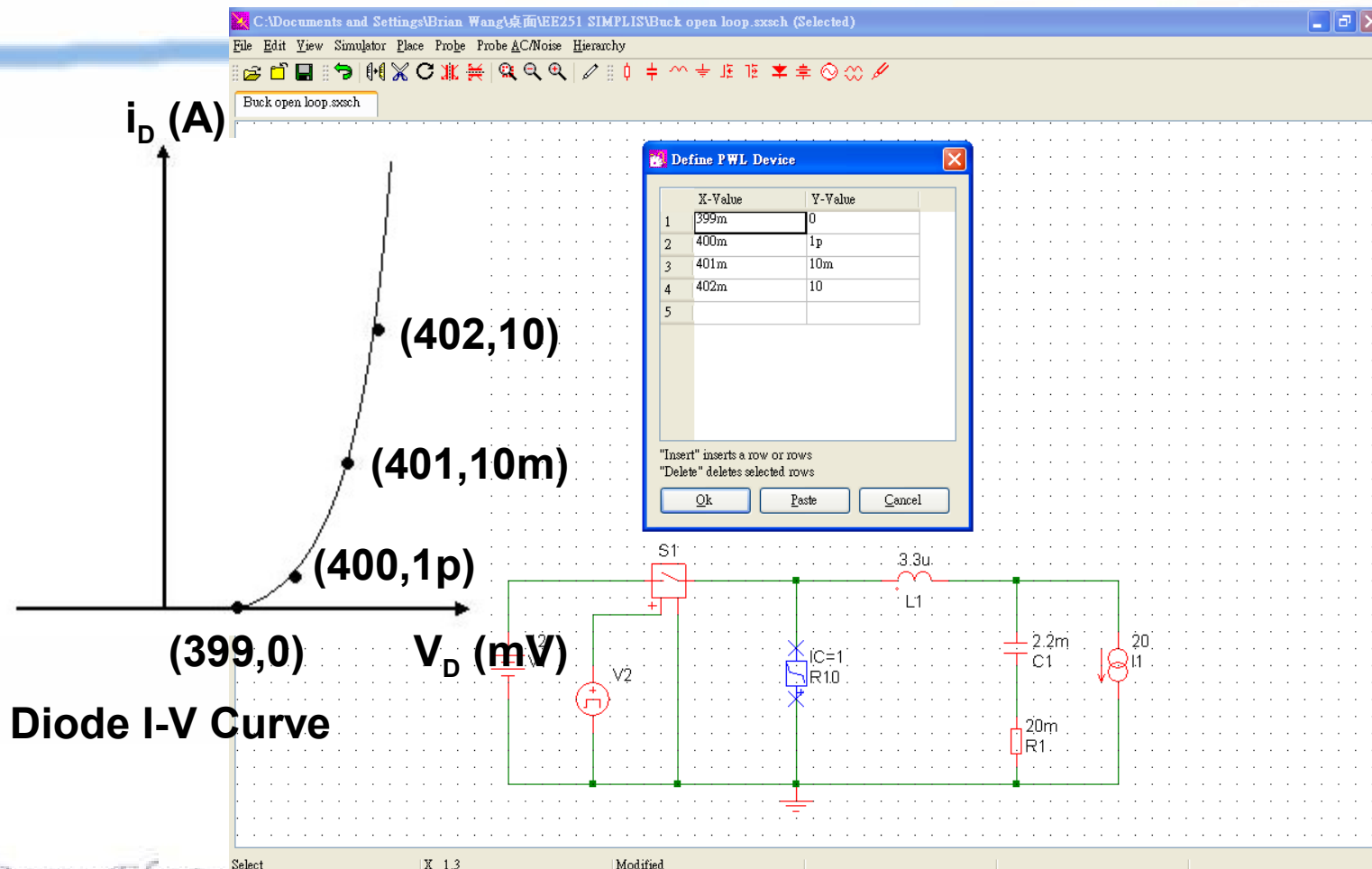


Threshold and Hysteresis:



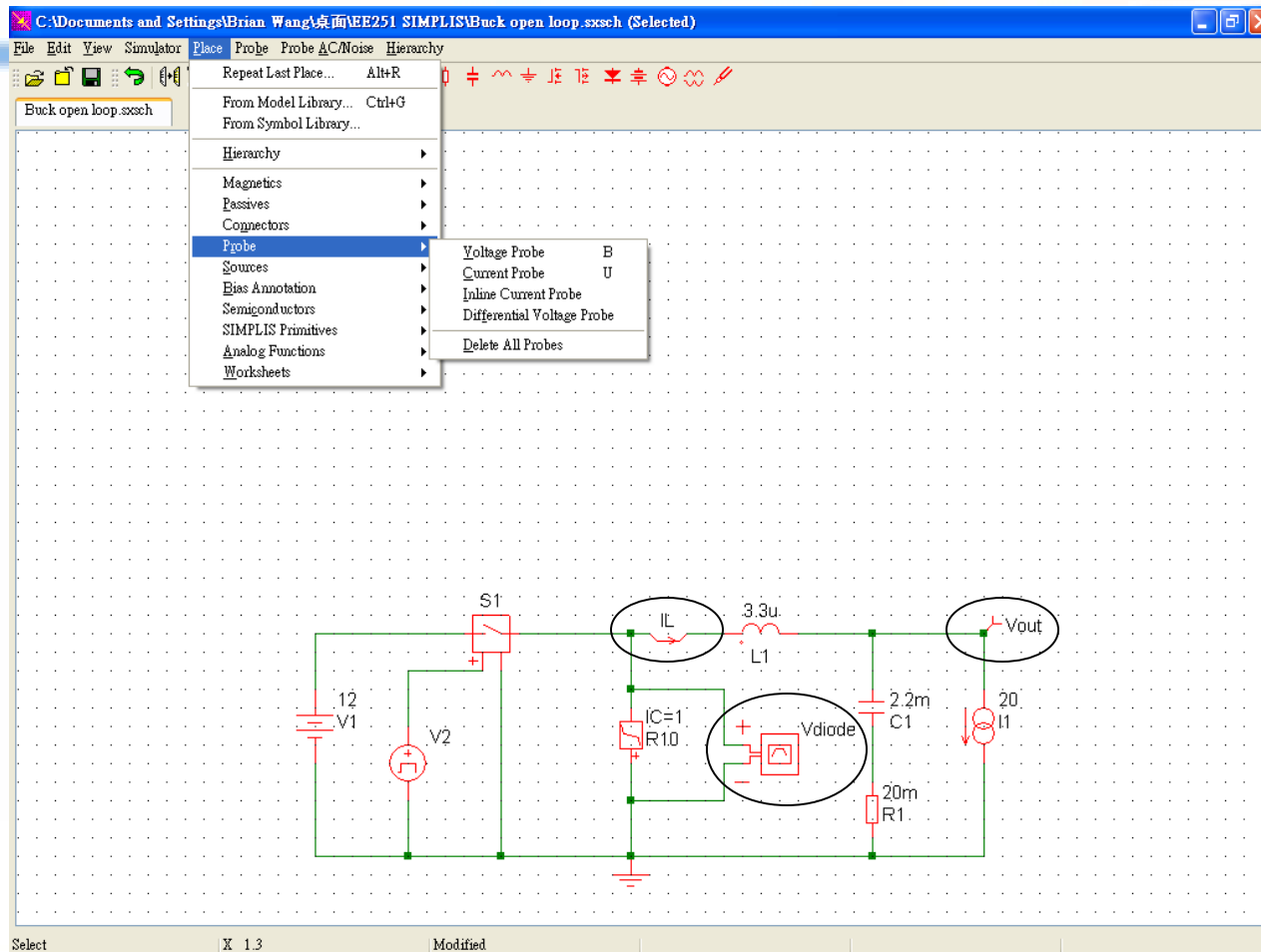
4.3 State diagram of the simple switch when the parameter LOGIC is assigned a value of (a) POS or (b) NEG

Buck Converter (Open Loop)



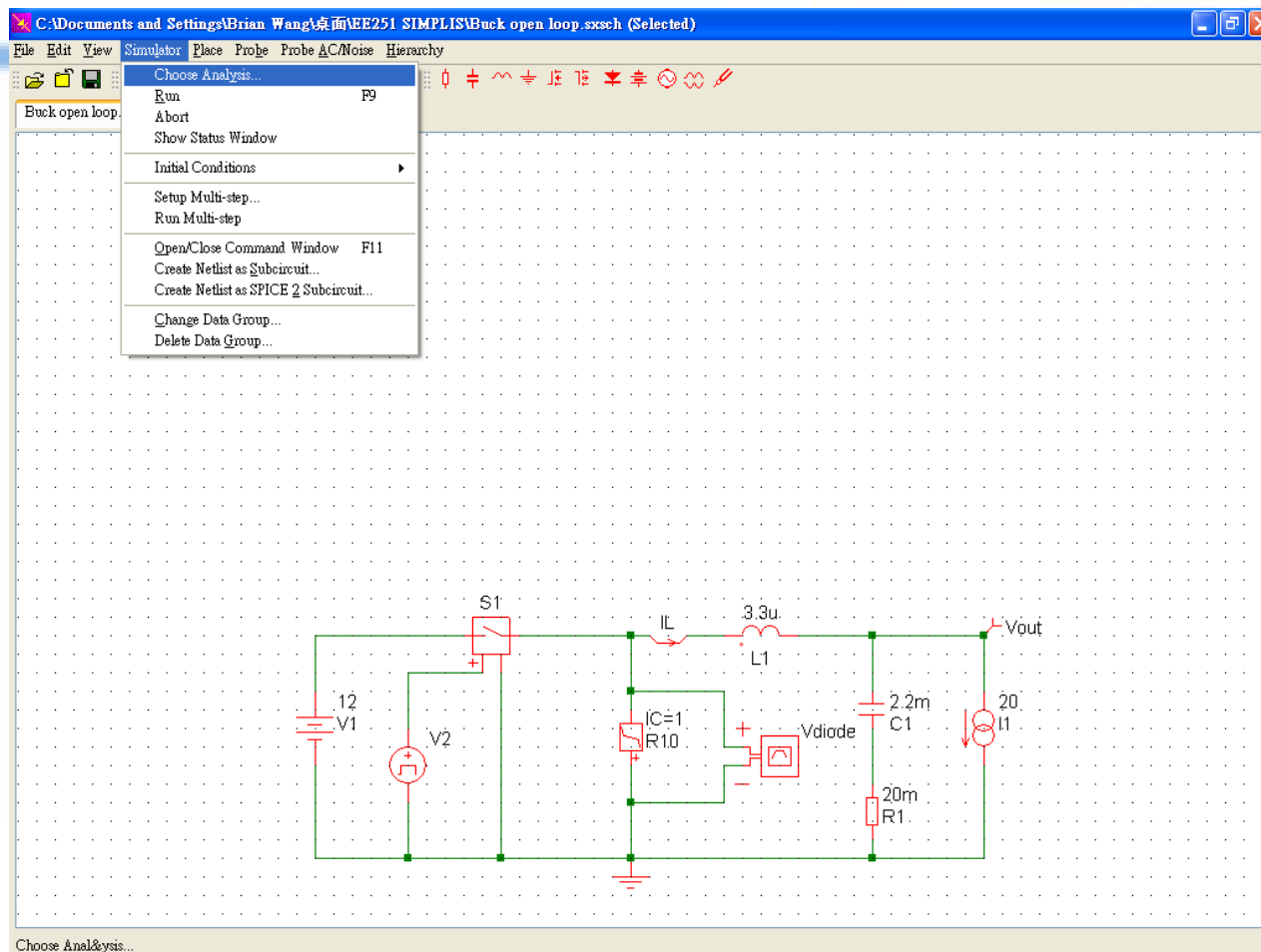
Use a VPWL resistor to replace a diode

Buck Converter (Open Loop)



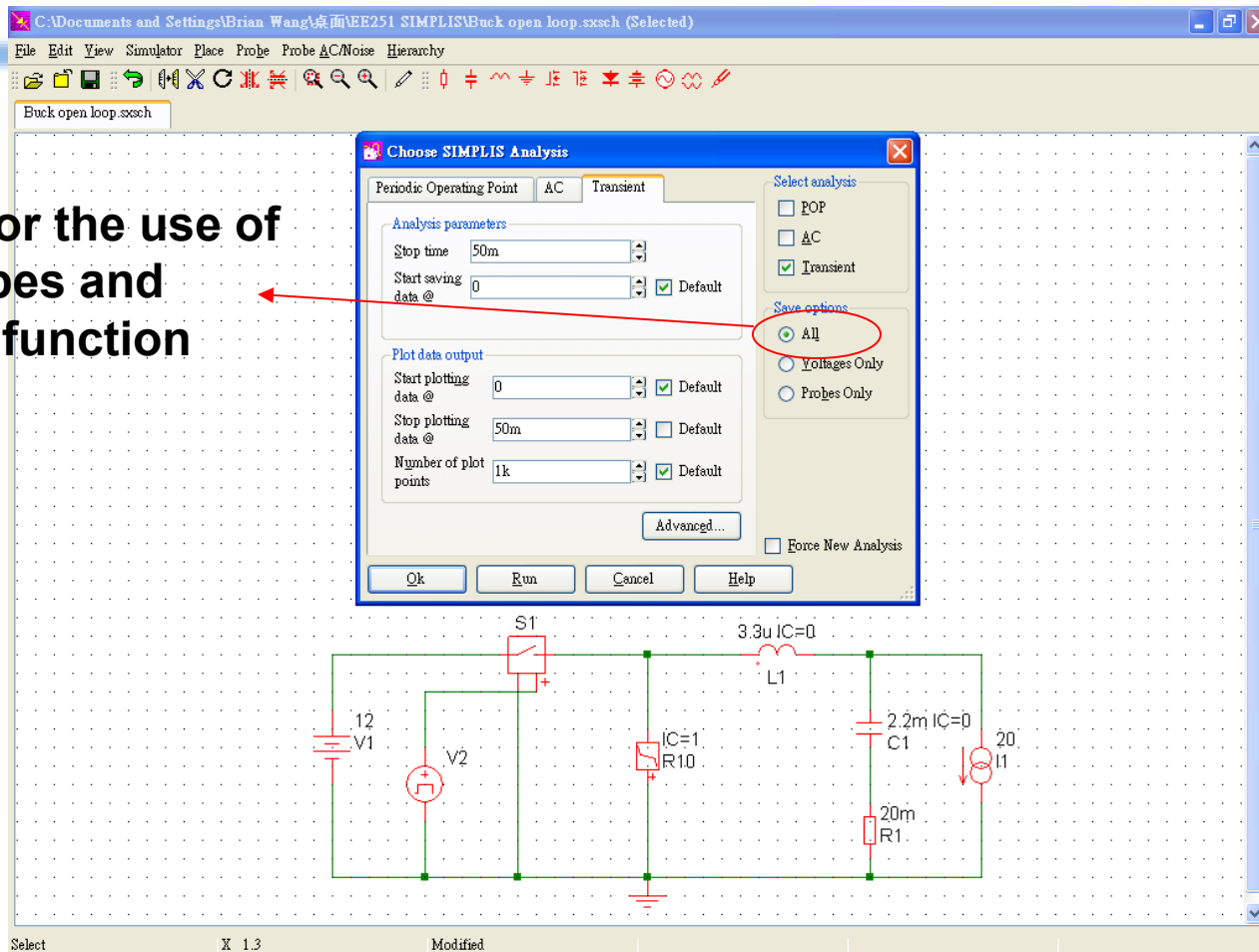
Add Probes to observe waveforms

Buck Converter (Open Loop)

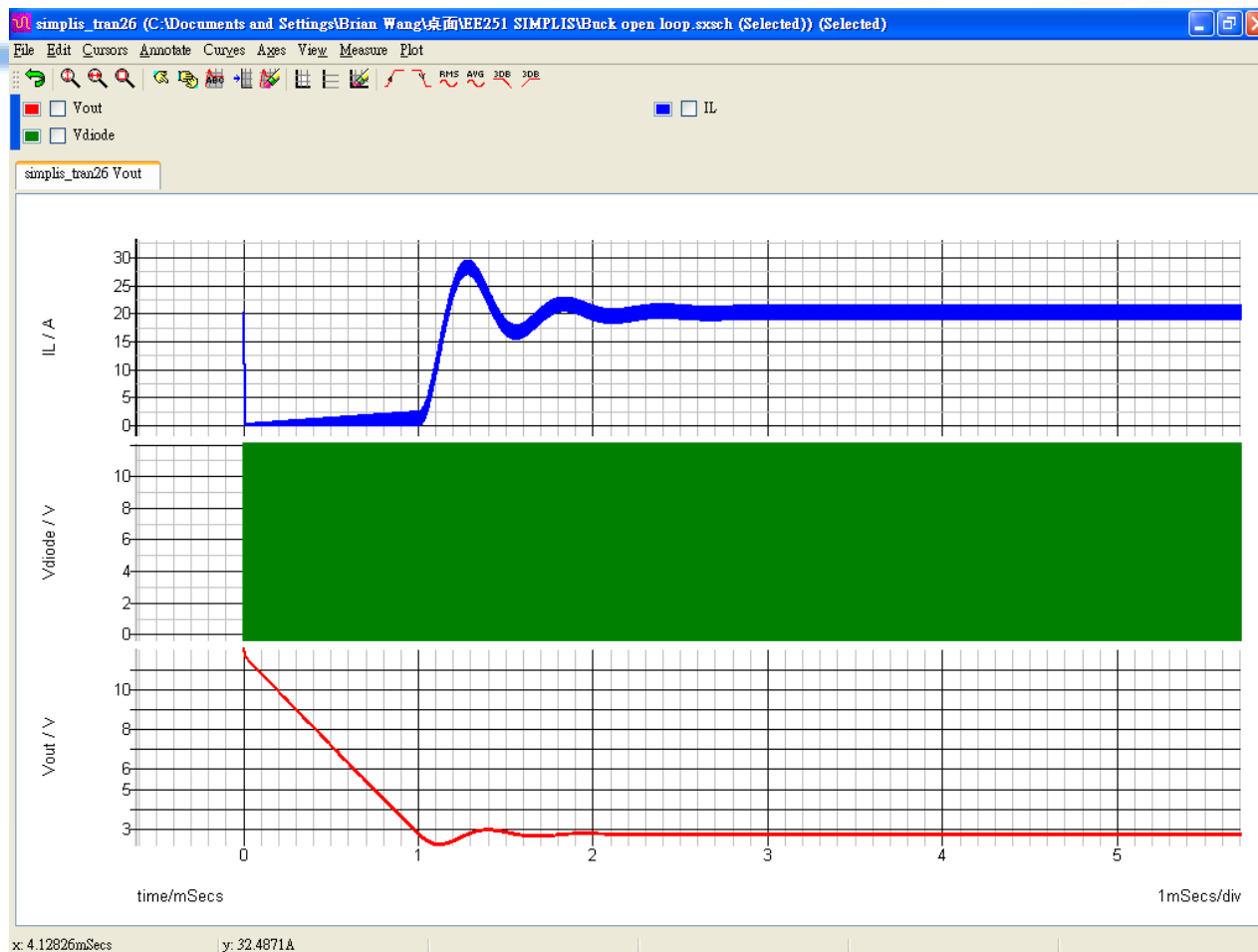


Buck Converter (Open Loop)

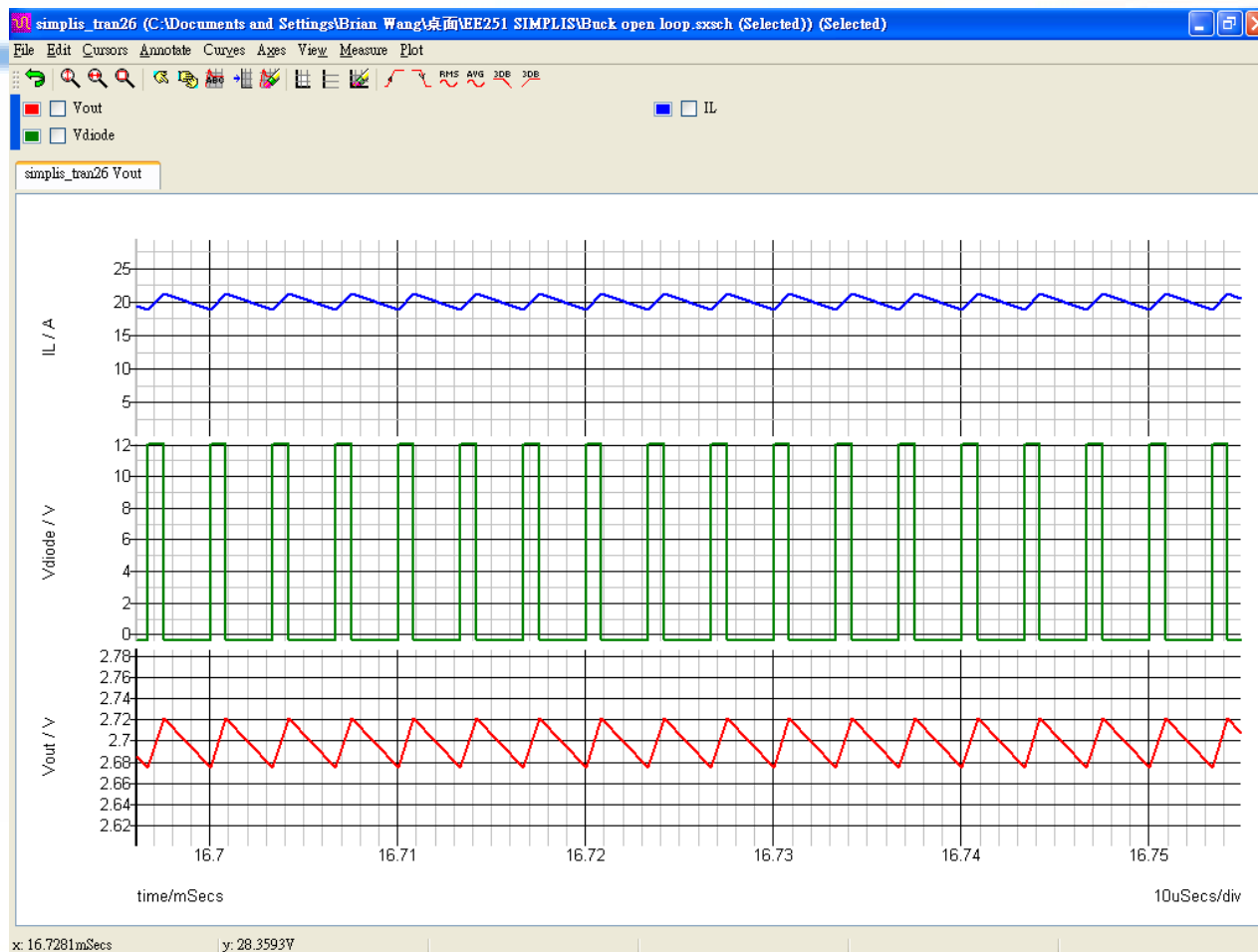
Select “All” for the use of Random probes and “Add Curve” function



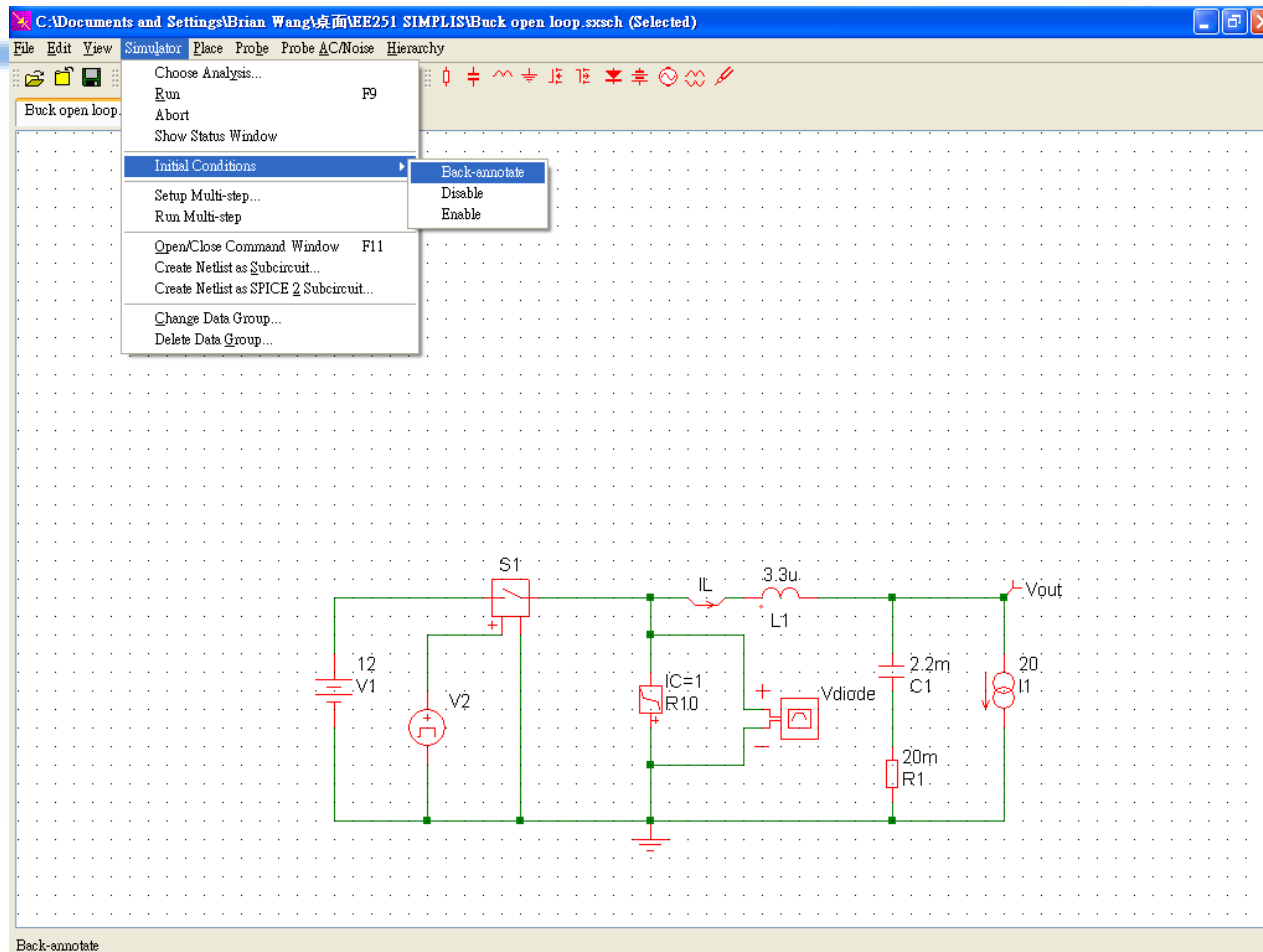
Buck Converter (Open Loop)



Buck Converter (Open Loop)

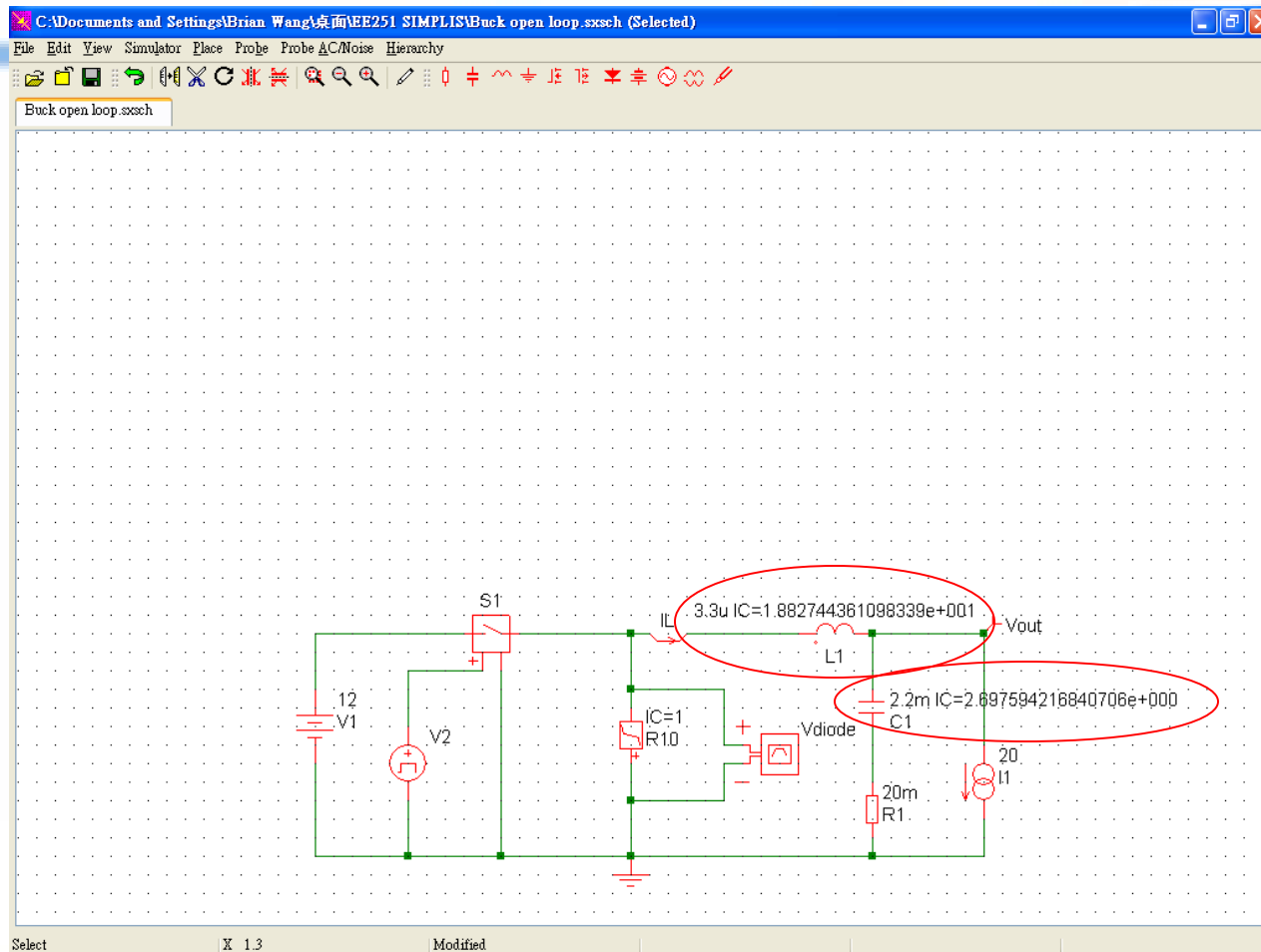


Buck Converter (Open Loop)



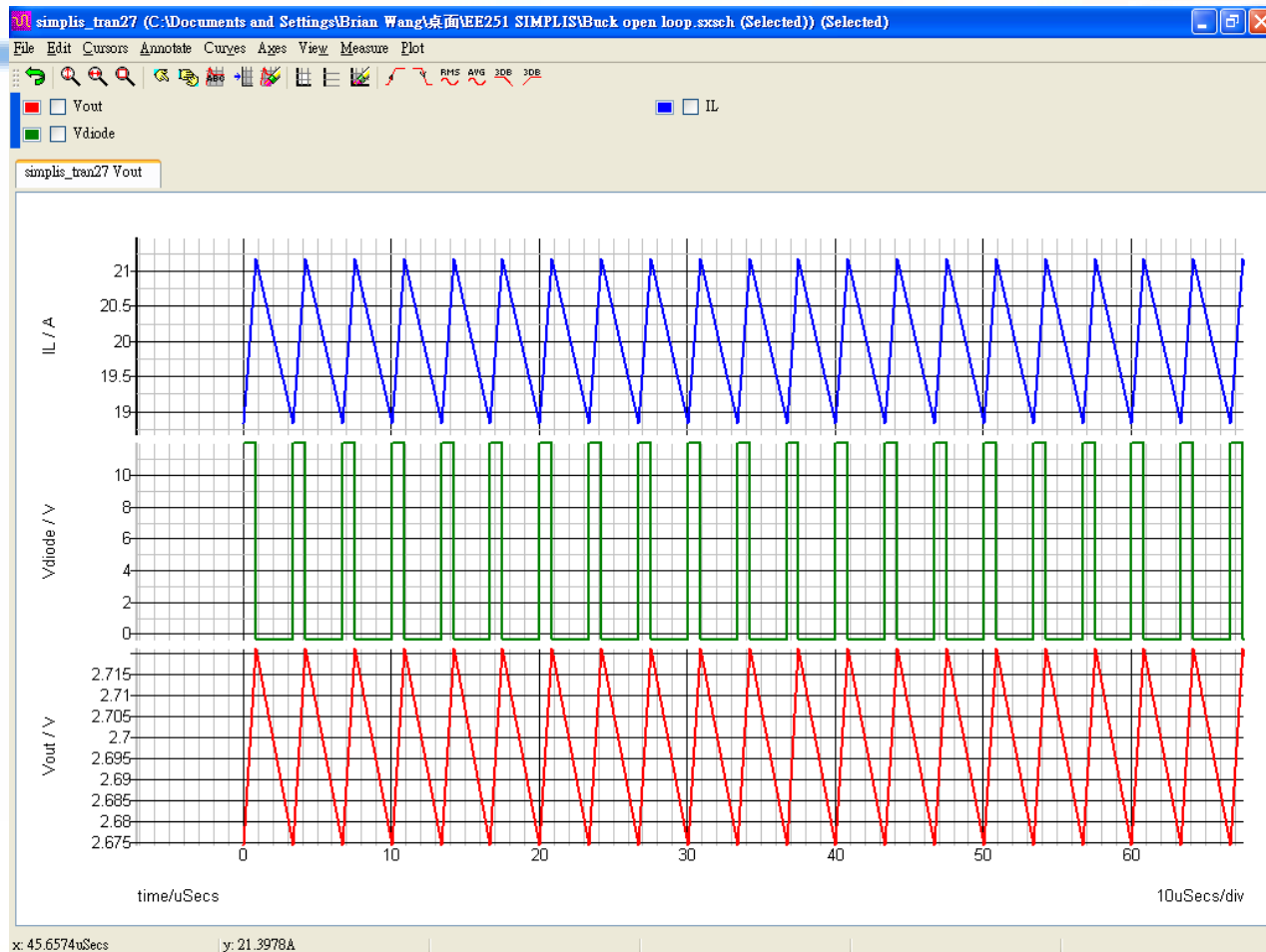
Choose **Back-annotate** to memorize Operating Point

Buck Converter (Open Loop)



Operating Point Memorized (equals Soft-Start)

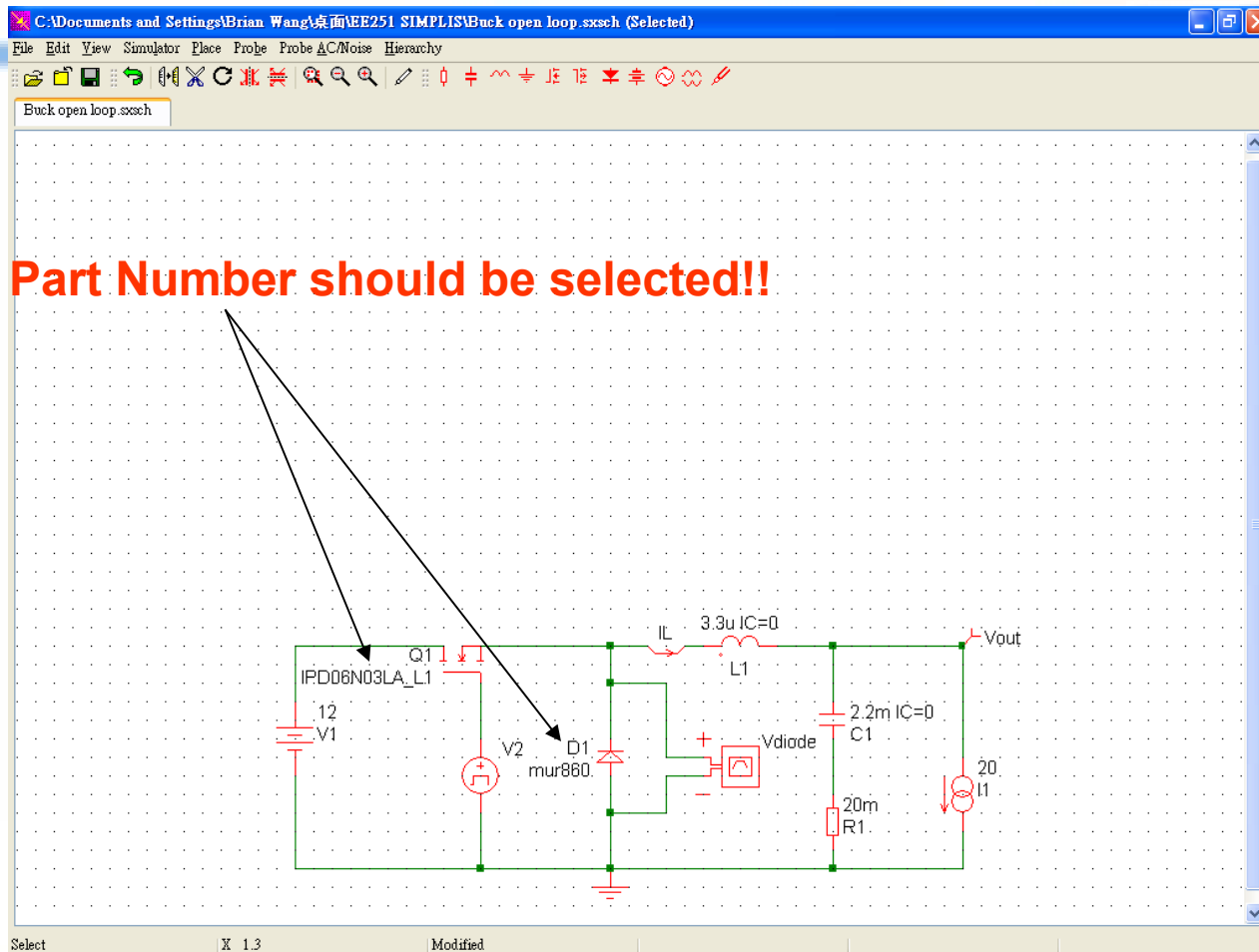
Buck Converter (Open Loop)



After Back-annotate: No damping during start up

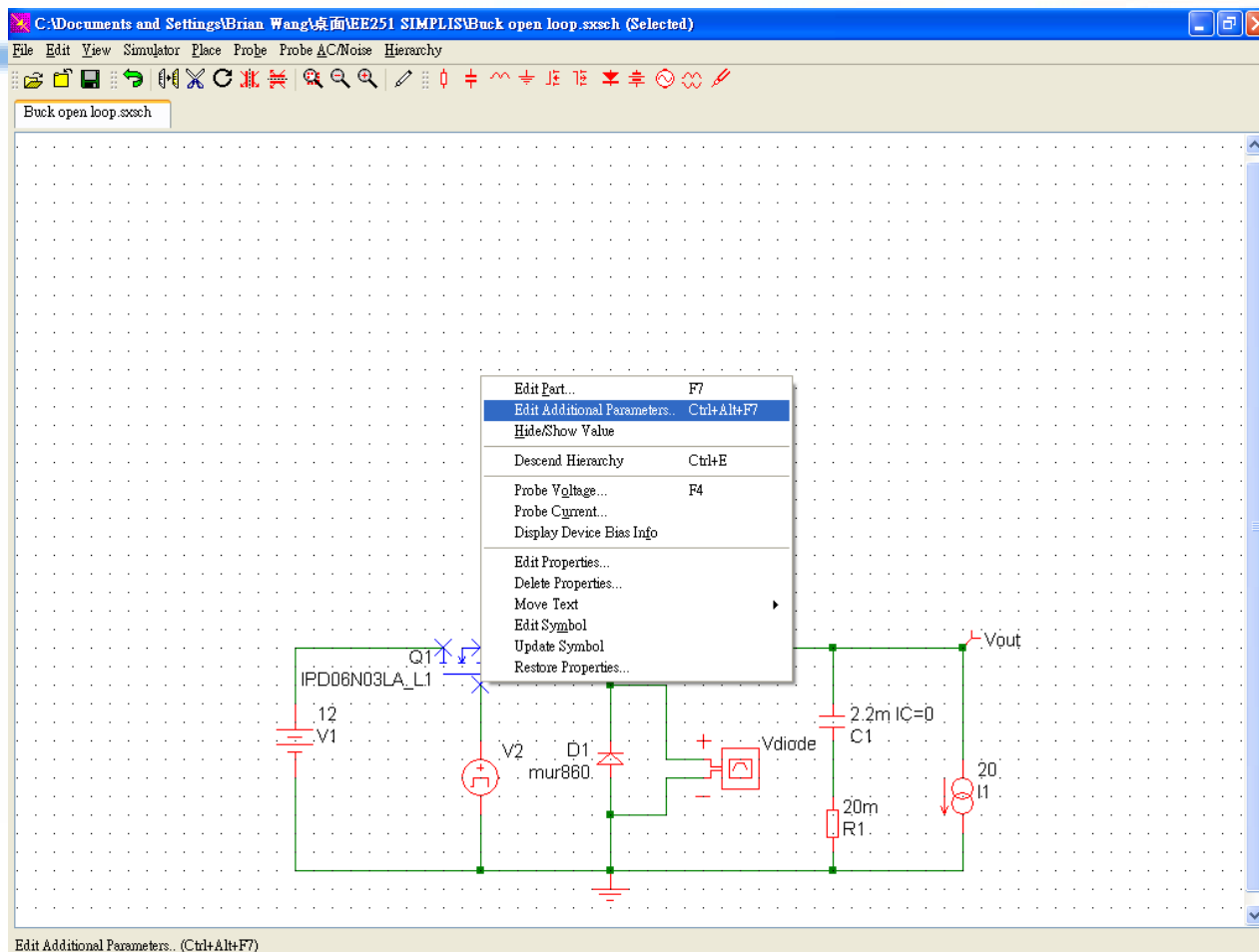
Buck Converter (Open Loop)

Correct Part Number should be selected!!



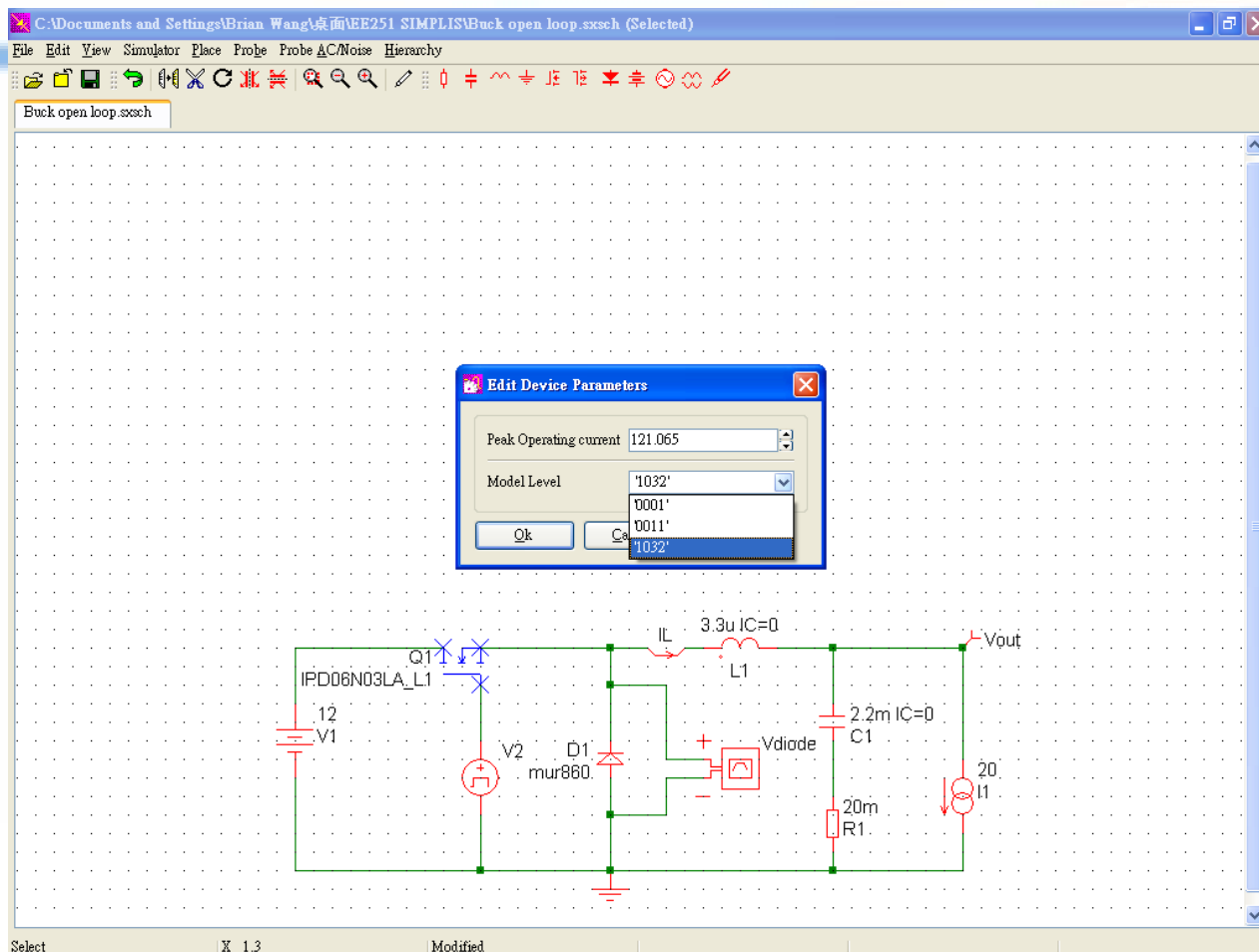
Use MOSFET and Diode: realistic condition

Buck Converter (Open Loop)



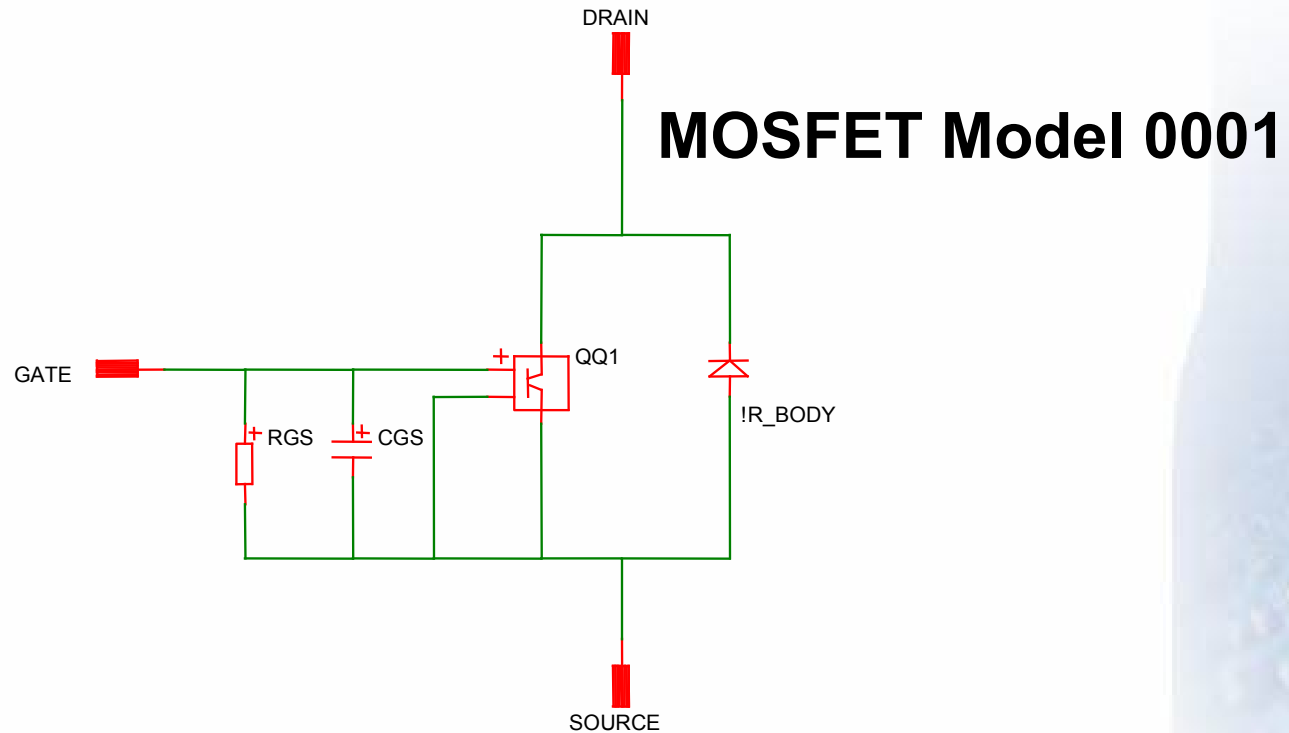
MOSFET Model selection: Additional Parameters

Buck Converter (Open Loop)



3 types of MOSFET Model in SIMPLIS

Buck Converter (Open Loop)

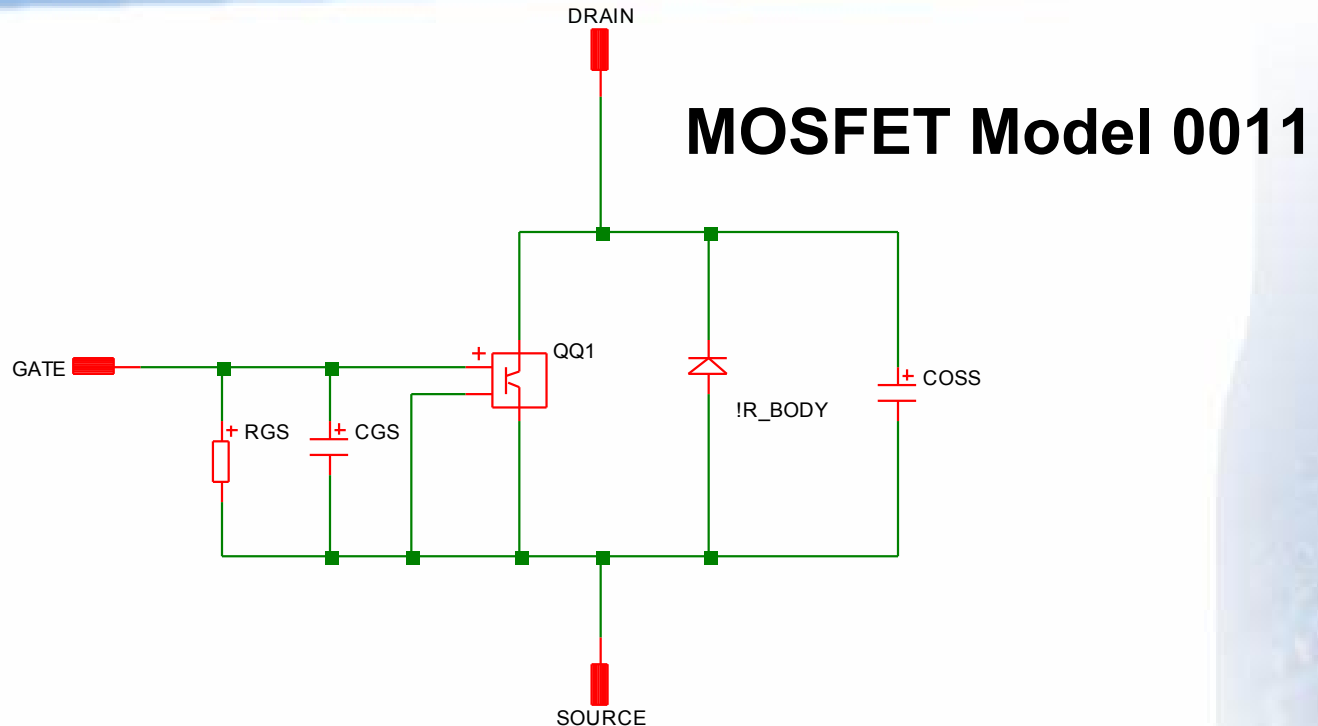


CGS : Linear capacitance

QQ1 : Ideal Switch

!R_BODY : Body diode modeled by PWL resistor

Buck Converter (Open Loop)



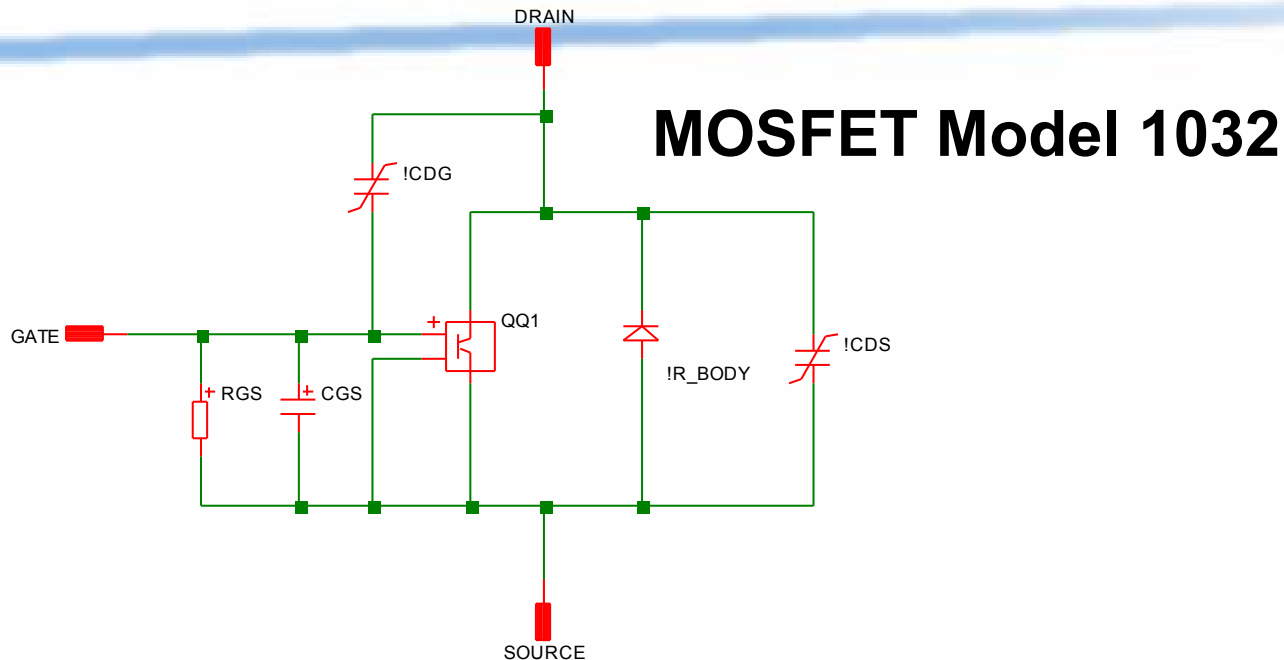
CGS : Linear capacitance

QQ1 : Ideal switch

!R_BODY : Body diode, modeled by PWL Resistor

C_{OSS} : Lumped linear output capacitance

Buck Converter (Open Loop)



CGS : Linear capacitance

QQ1 : SIMPLIS Switch modeling I_d vs V_{ds} with I_d normally proportional to voltage exceeding V_{TO}

!R_BODY : Body diode, modeled by PWL Resistor

!CDG : PWL capacitance

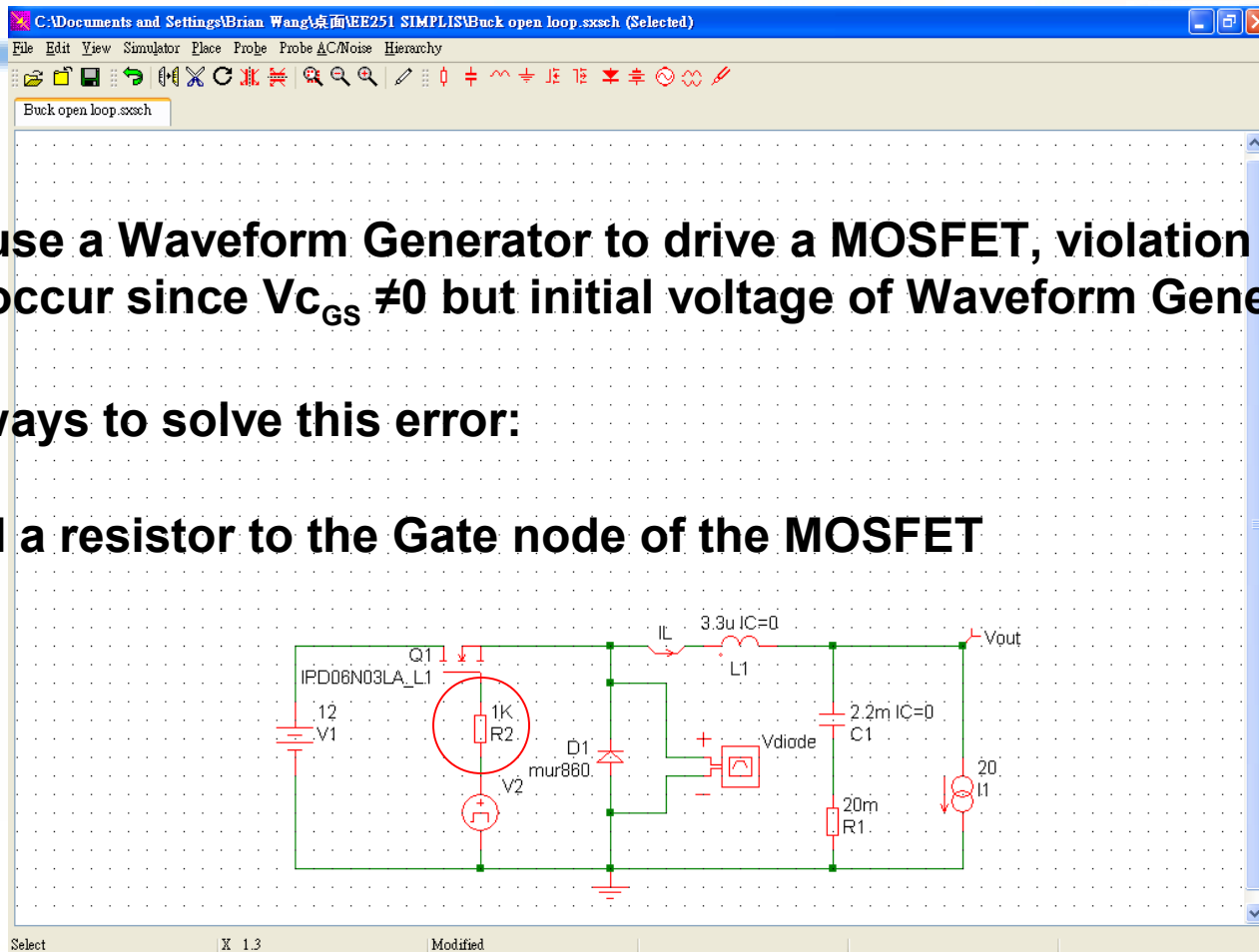
!CDS : PWL capacitance

Buck Converter (Open Loop)

If we use a Waveform Generator to drive a MOSFET, violation of KVL/KCL may occur since $V_{GS} \neq 0$ but initial voltage of Waveform Generator = 0.

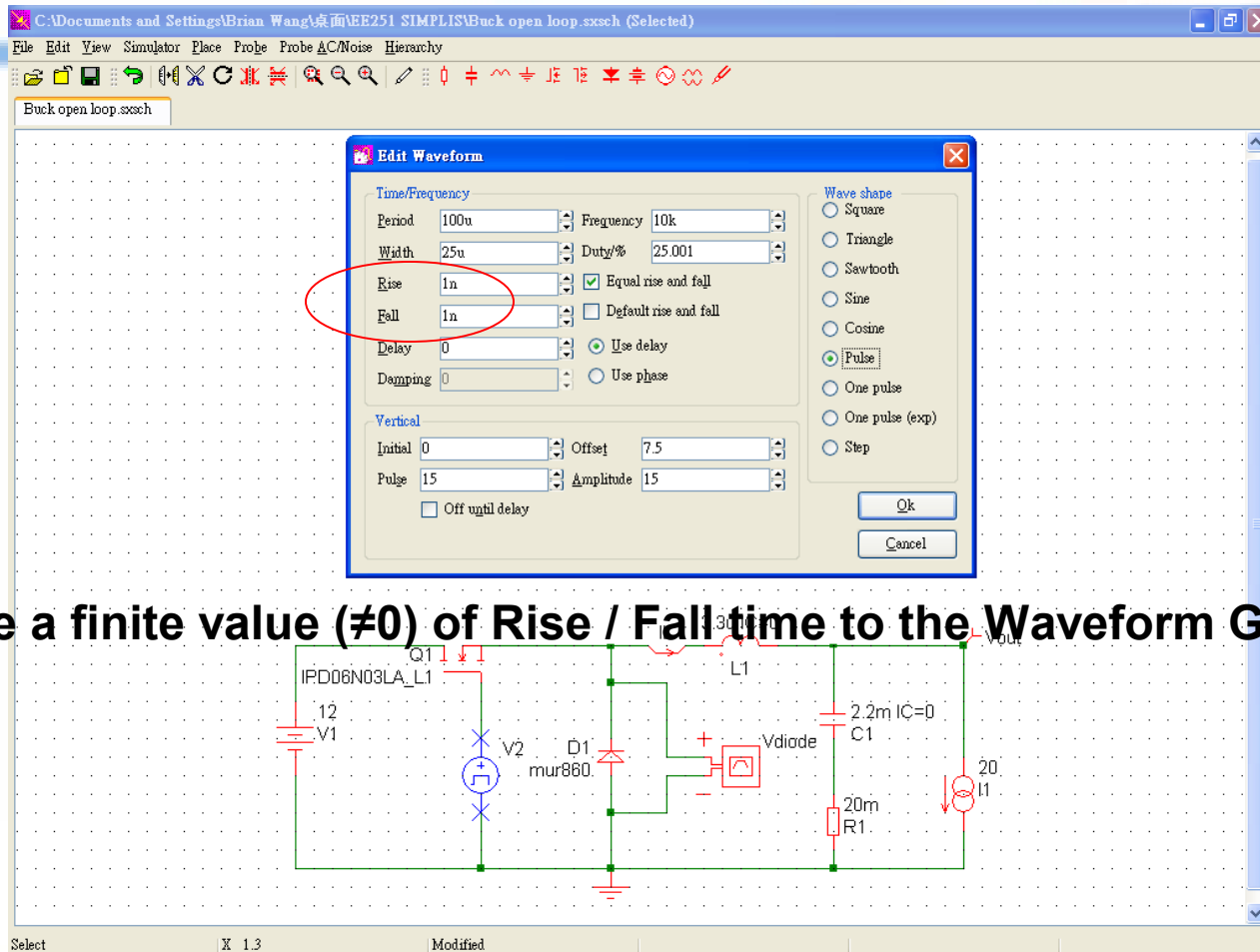
Two ways to solve this error:

1. Add a resistor to the Gate node of the MOSFET



Problems in using MOSFET

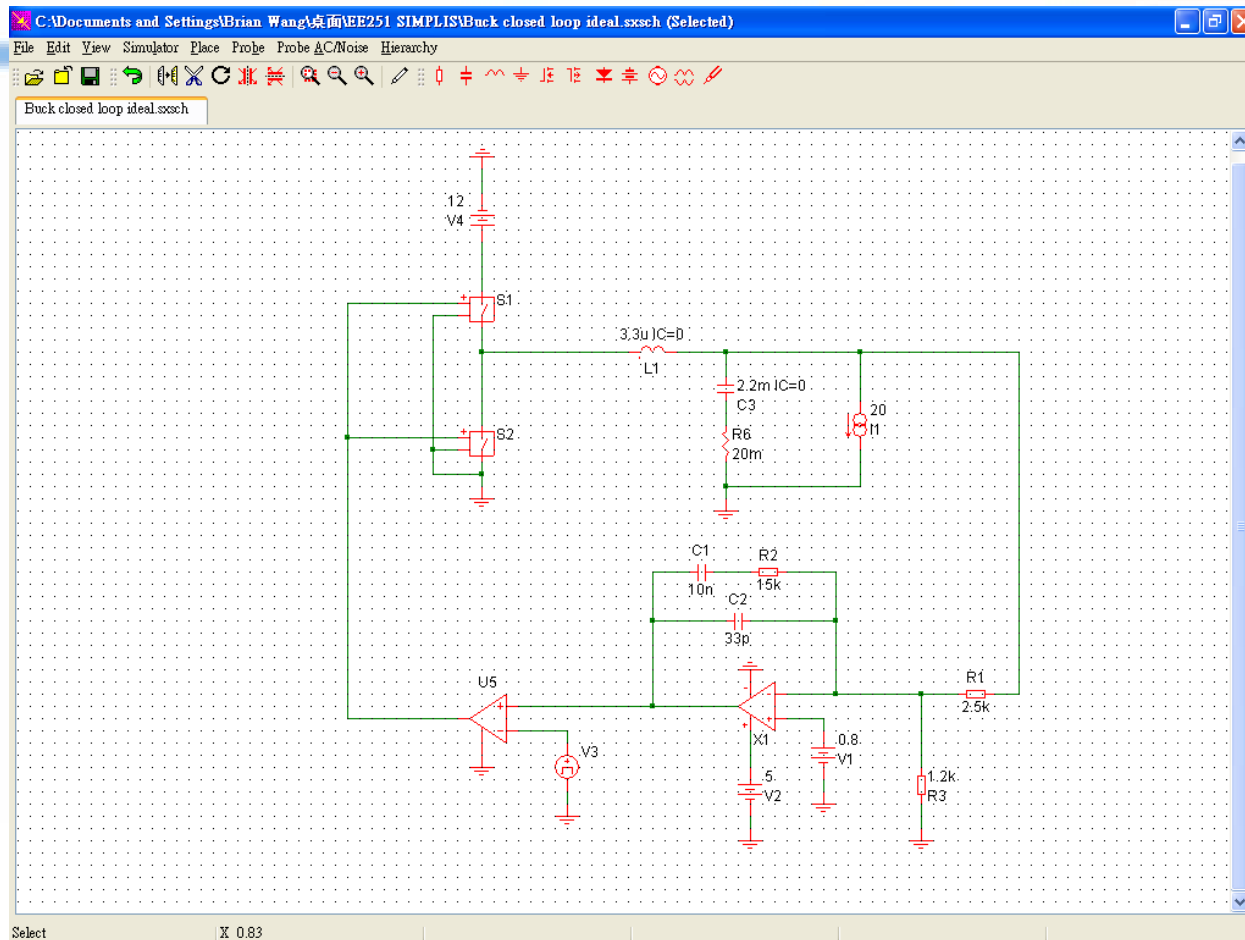
Buck Converter (Open Loop)



2. Give a finite value ($\neq 0$) of Rise / Fall time to the Waveform Generator

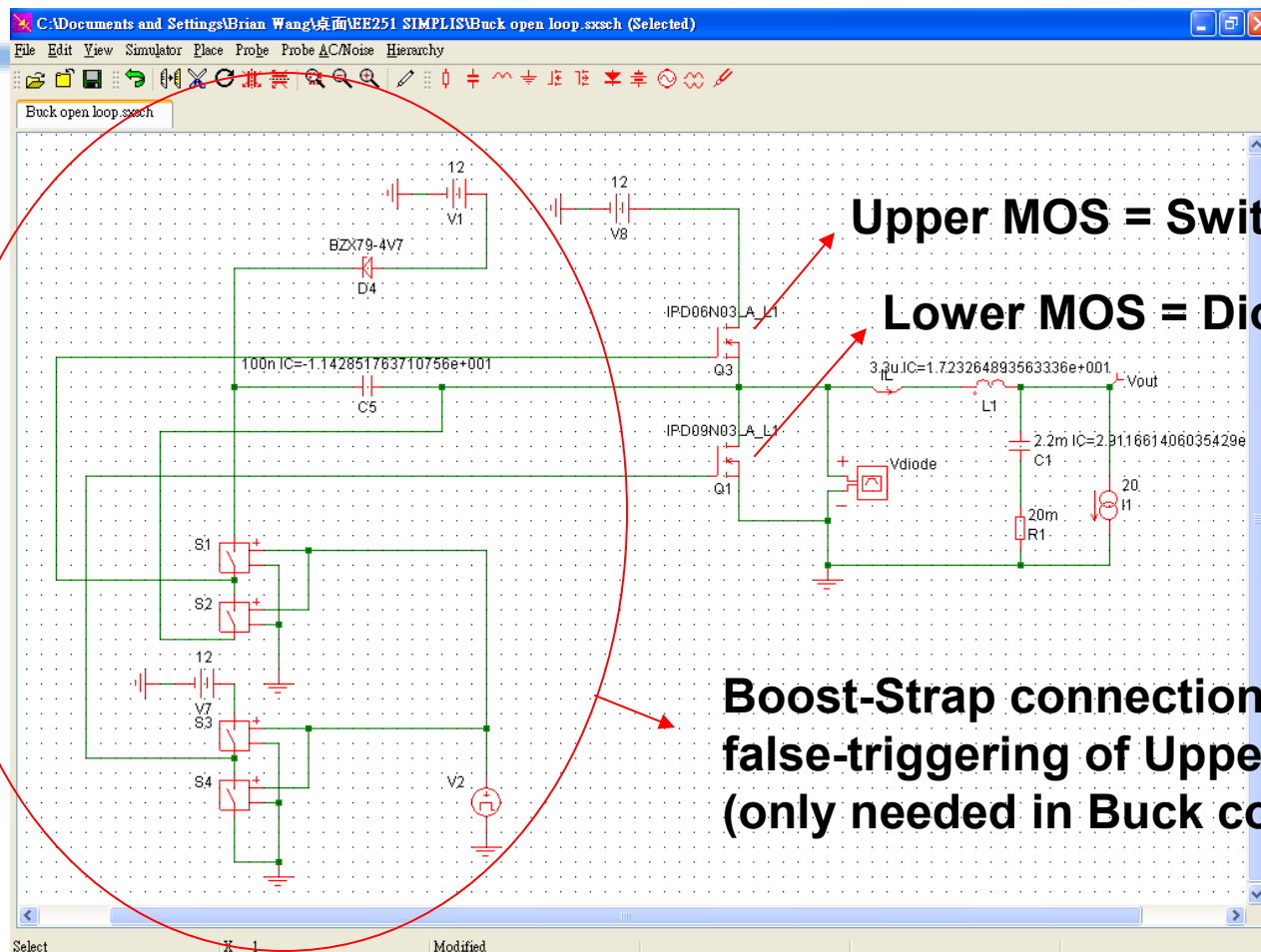
Problems in using MOSFET

Buck Converter (Open Loop)



Synchronous rectifying switch using only Simple Switches (Recommended)

Buck Converter (Open Loop)



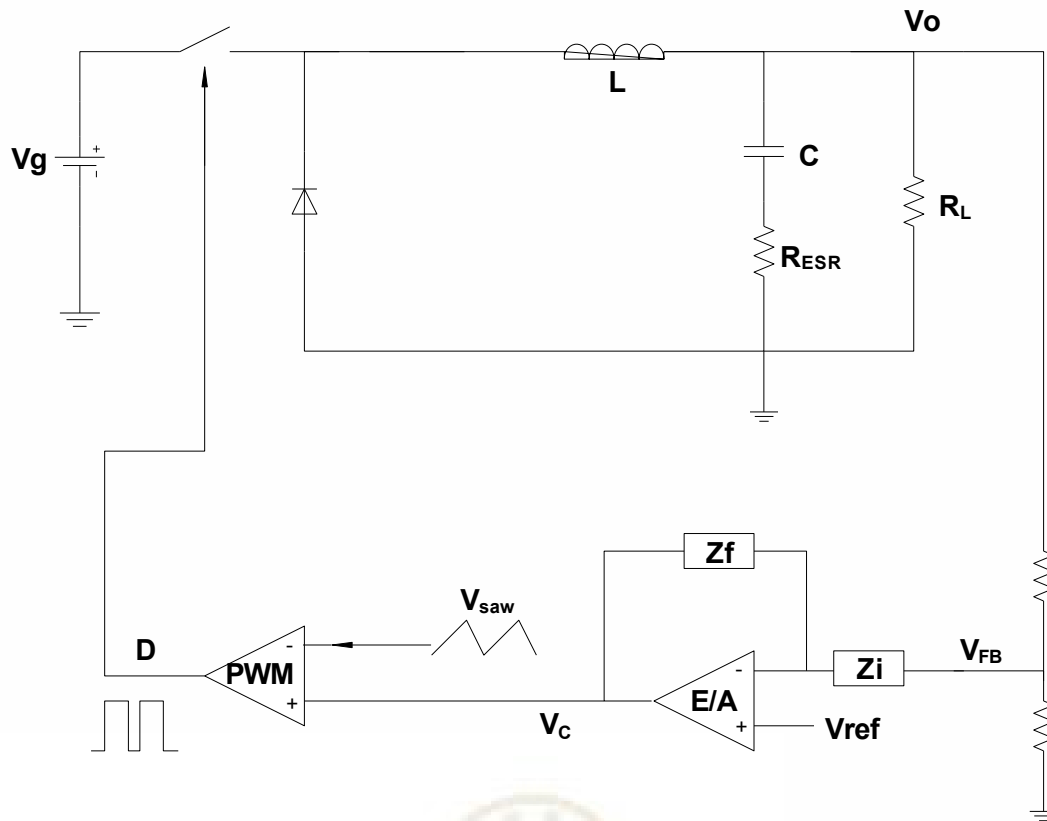
Upper MOS = Switch

Lower MOS = Diode

Boost-Strap connection to avoid false-triggering of Upper MOS (only needed in Buck converters)

Synchronous rectifying switch using MOSFETs

Buck Converter (Closed Loop)



Buck converters: $\frac{V_o}{V_g} = D$

$D \uparrow$ then V_o goes $\uparrow$

Check: When V_o goes high

$\downarrow$
 V_c goes low

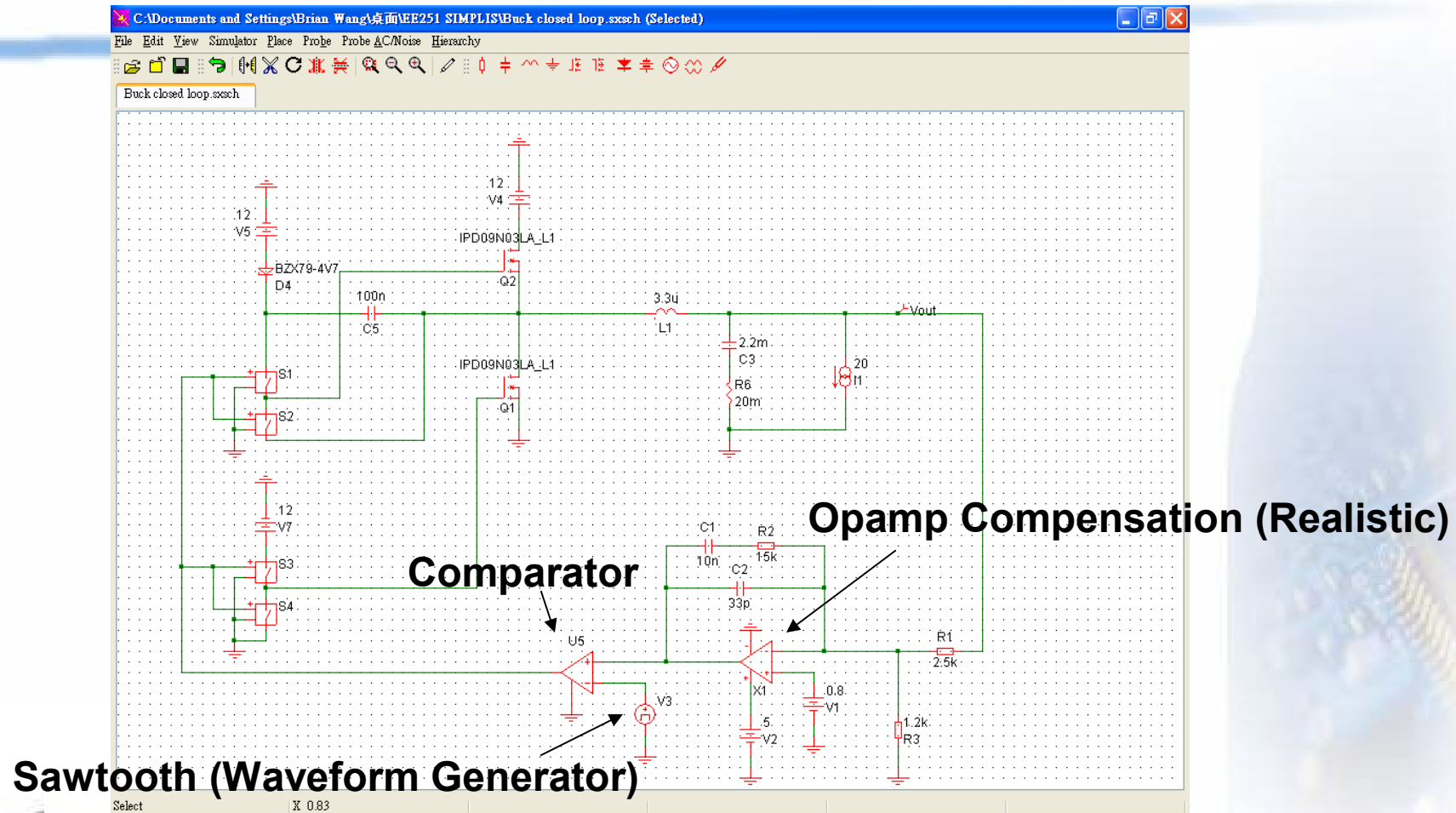
$\downarrow$
 D goes low

$\downarrow$
 V_o goes low

$\downarrow$
Stable

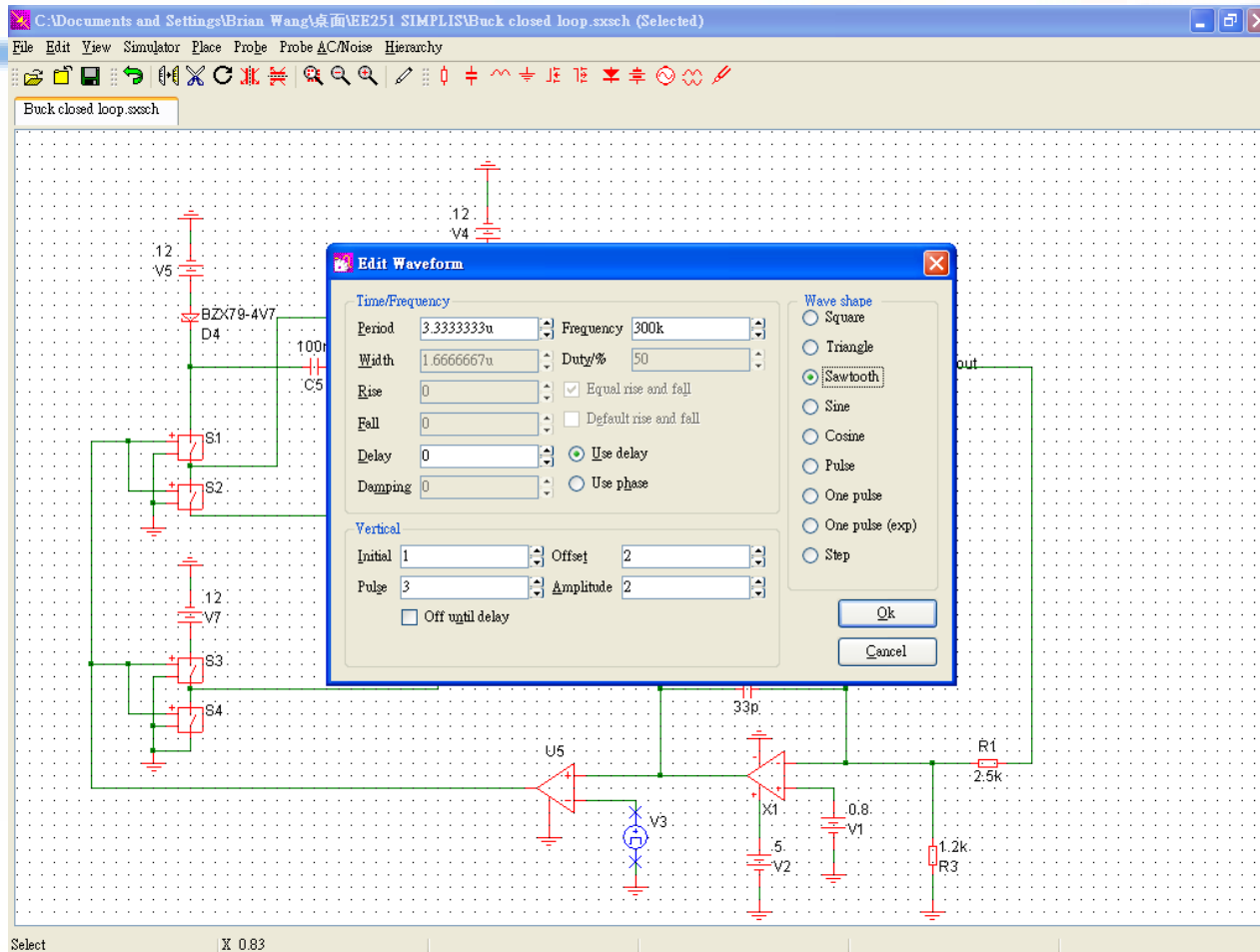
E/A's output should be connected to Comparator's + node!!

Buck Converter (Closed Loop)



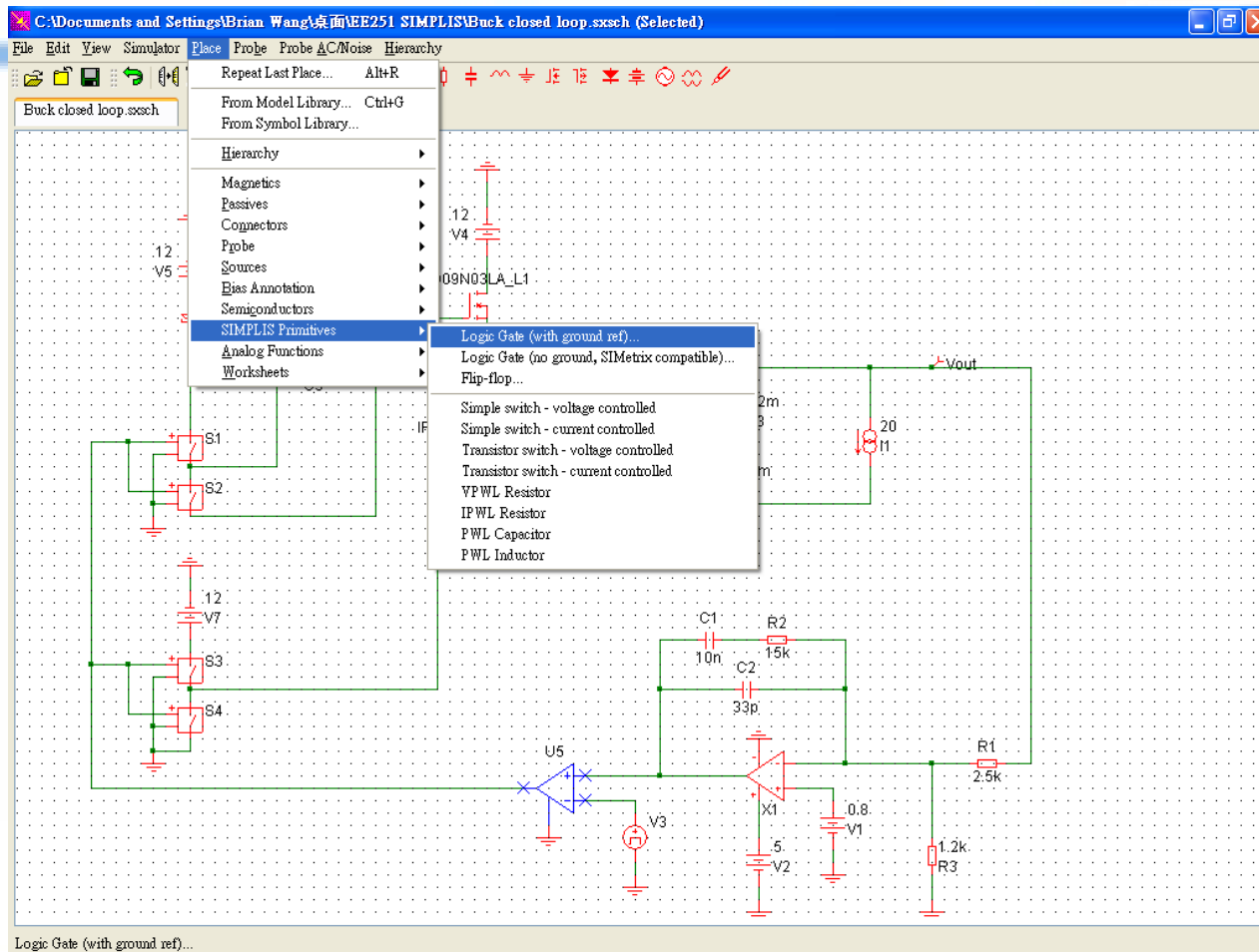
Connections of closed-loop Buck

Buck Converter (Closed Loop)

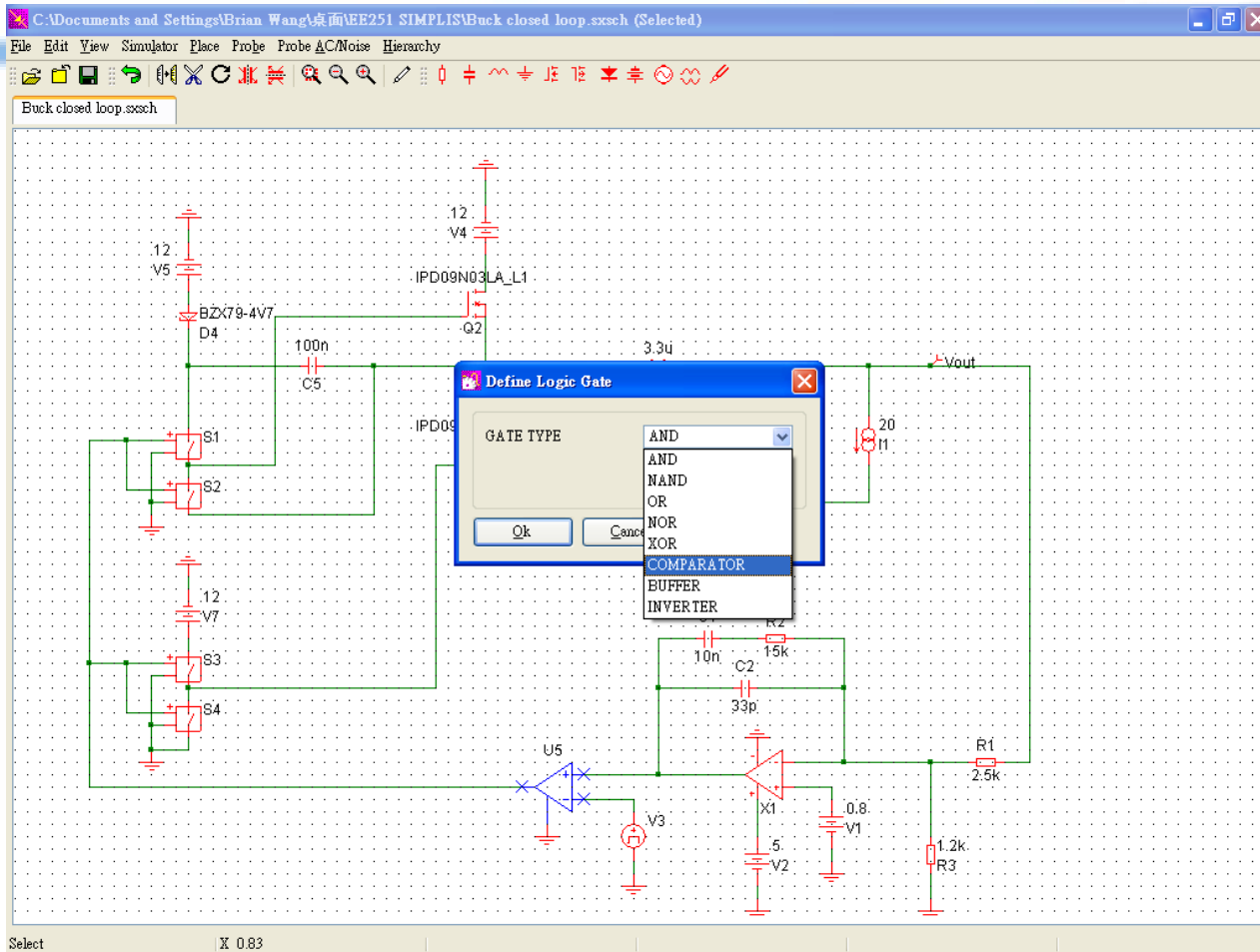


Sawtooth (Waveform Generator) settings

Buck Converter (Closed Loop)



Buck Converter (Closed Loop)

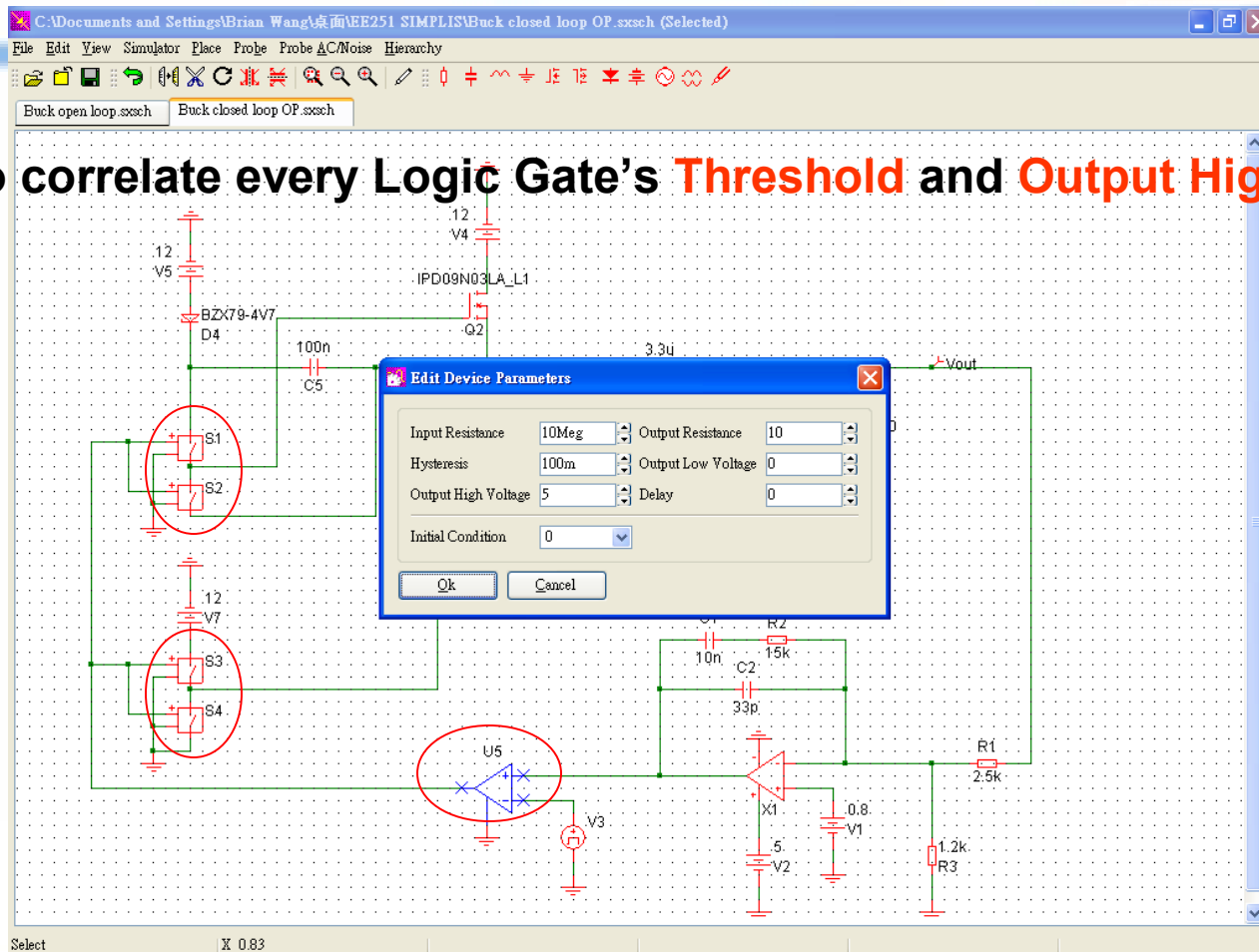


Power Electronics LAB 251
Department of Electrical Engineering, MIT

Comparator settings

Boost Converter (Closed Loop)

Remember to correlate every Logic Gate's **Threshold** and **Output High Voltage**



Buck Converter (Closed Loop)

C:\Documents and Settings\Brian Wang\桌面\EE251 SIMPLIS\Buck closed loop.sxsch (Selected)

File Edit View Simulator Place Probe Probe A/C/Noise Hierarchy

Buck closed loop.sxsch

: Larger = More ideal

Edit Device Parameters

Model Level	2	Offset Voltage	0	Bias Current	0
Offset Current	0	Open-loop Gain	500Meg ↑	Gain-bandwidth (Level 2)	5G ↑
Pos. Slew Rate (Level 2)	30Meg	Neg. Slew Rate (Level 2)	30Meg	CMRR	100k ↑
PSRR	100k ↑	Input Resistance	2Meg	Out. Source Current (Level 2)	5m ↑
Out. Sink Current (Level 2)	5m ↑	Output Res.	100	Output Res. AC	50
Power Diss.	2.5m	Headroom Pos. (Level 2)	500u	Headroom Neg. (Level 2)	500u

☐ Use back-annotated info. for init. cond. if available

Ok Cancel Help

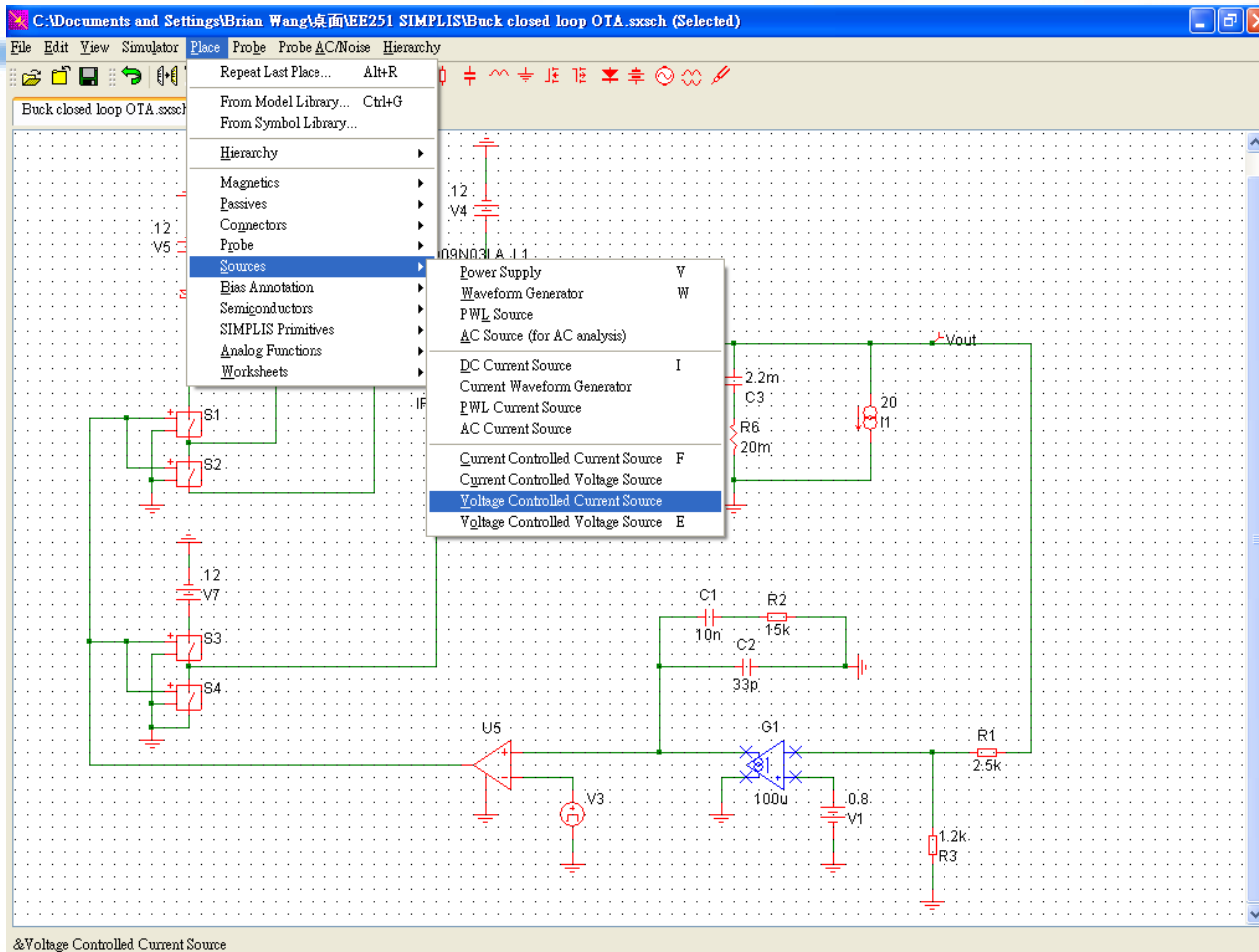
Swing

$(V_{cc}^{+}) - (\text{Headroom Pos.})$

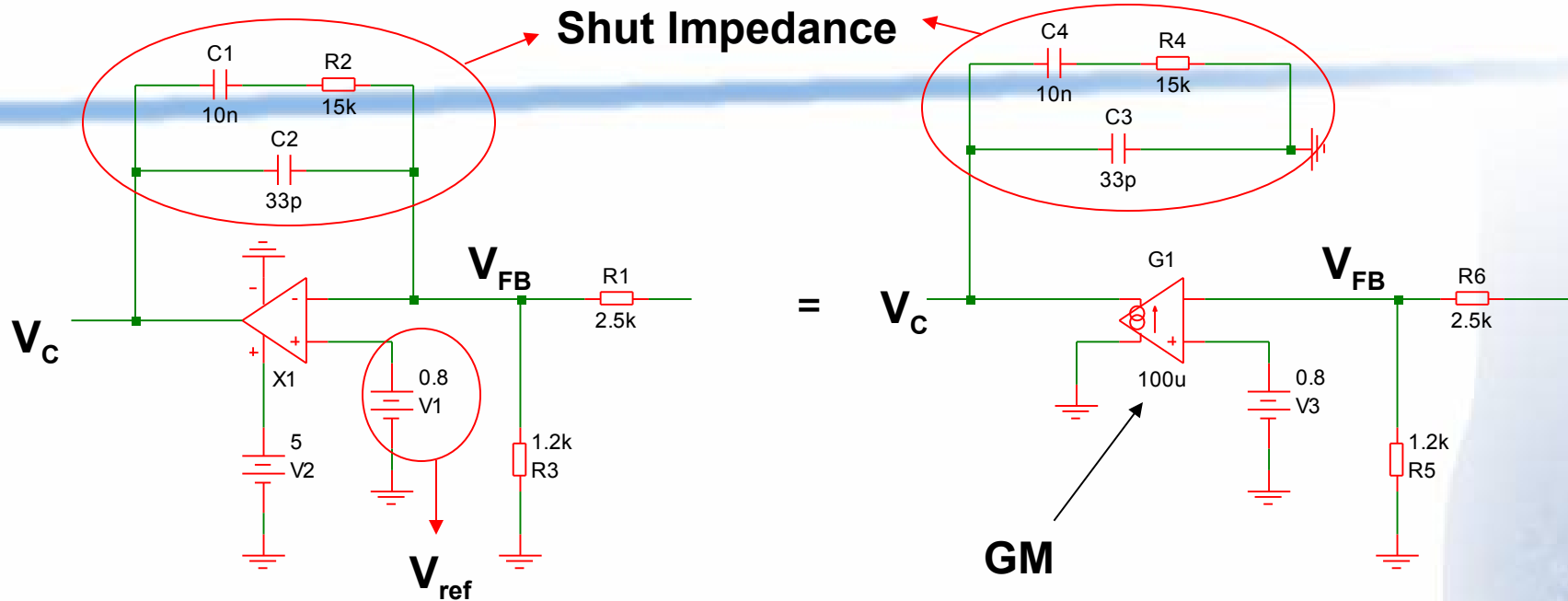
$(V_{cc}^{-}) + (\text{Headroom Neg.})$

Parameterised Opamp settings

Buck Converter (Closed Loop)



Buck Converter (Closed Loop)



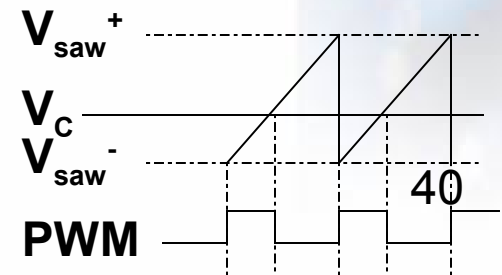
$$\frac{V_C}{V_{FB}} = GM \times Z_{out}$$

V_C : Depends on comparator connections and duty cycle

In this case = $(V_{saw}^+ - V_{saw}^-) \cdot \text{Duty} + V_{saw}^-$

$$V_{FB} = V_{ref}$$

Z_{out} : Shut Impedance



Boost Converter (Closed Loop)

Boost converters: $\frac{V_o}{V_g} = \frac{1}{1 - D}$

$D \uparrow$ then V_o goes $\uparrow$

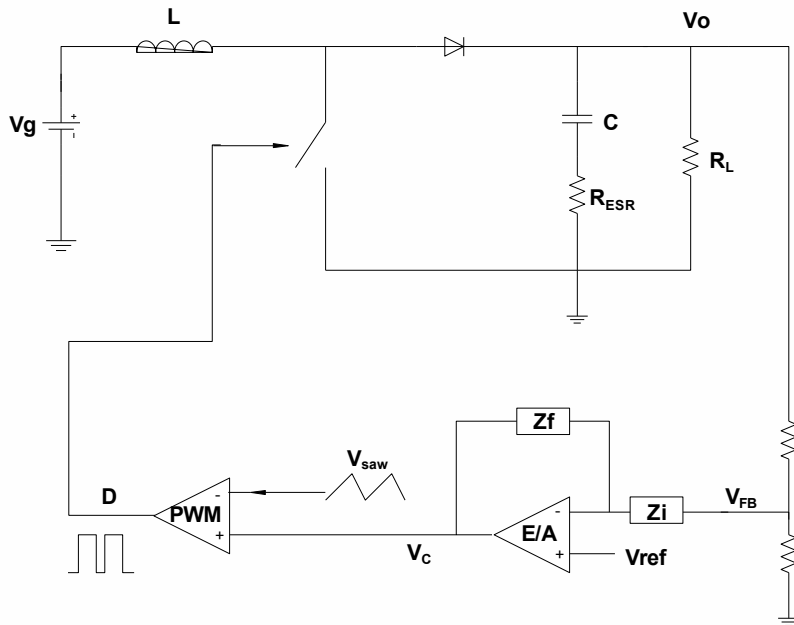
Check: When V_o goes high

V_c goes low

D goes low

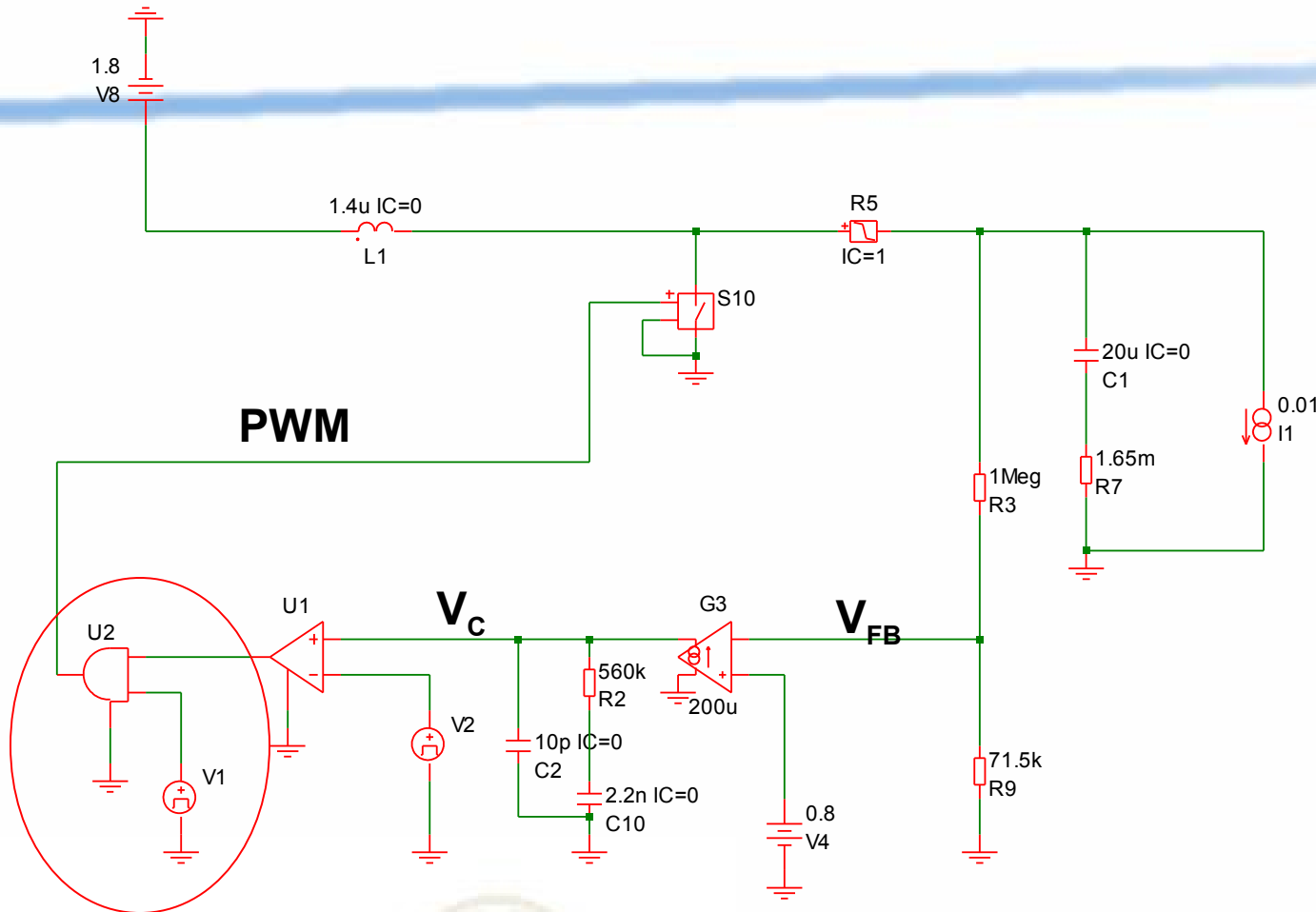
V_o goes low

Stable



E/A's output should be connected to Comparator's + node!!

Boost Converter (Closed Loop)



Start up: $V_{out} = 0$

$V_{FB} = \text{low}$

$V_C = \text{high}$

PWM = high

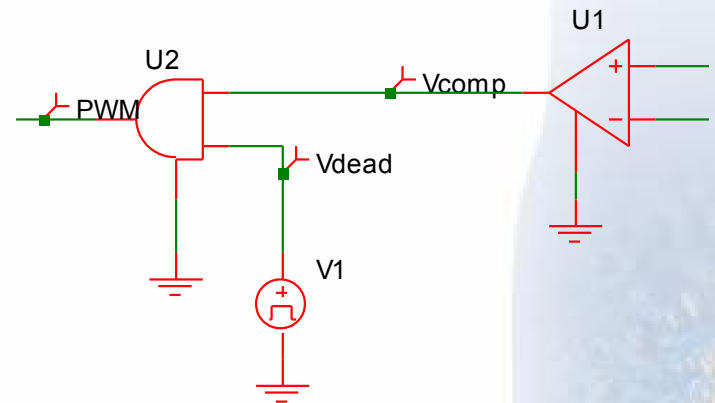
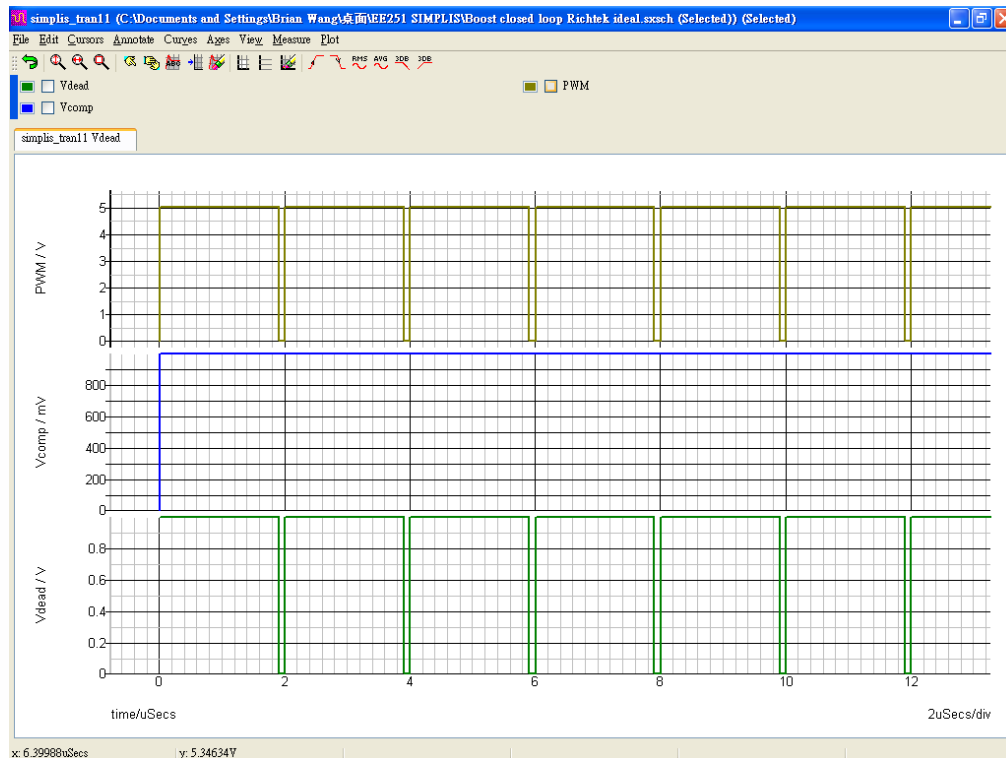
Switch always on

V_{out} still = 0

Can't work without
soft start circuit

Require a dead time control circuit during start up (Soft Start)

Boost Converter (Closed Loop)



Power Electronics LAB Force PWM to have 5% duty off
Department of Electrical Engineering, NTU

Buck/Boost Converter (Closed Loop)

Buck/Boost converters: $\frac{V_o}{V_g} = \frac{D}{1 - D}$

$D \uparrow$ then V_o goes $\uparrow$

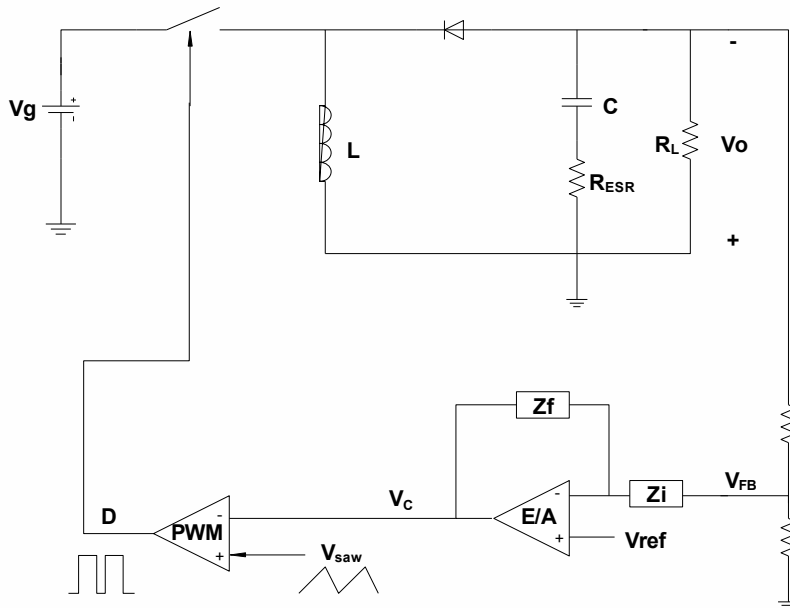
Check: When $(-V_o)$ goes high

V_c goes low

D goes low

V_o goes low

Stable

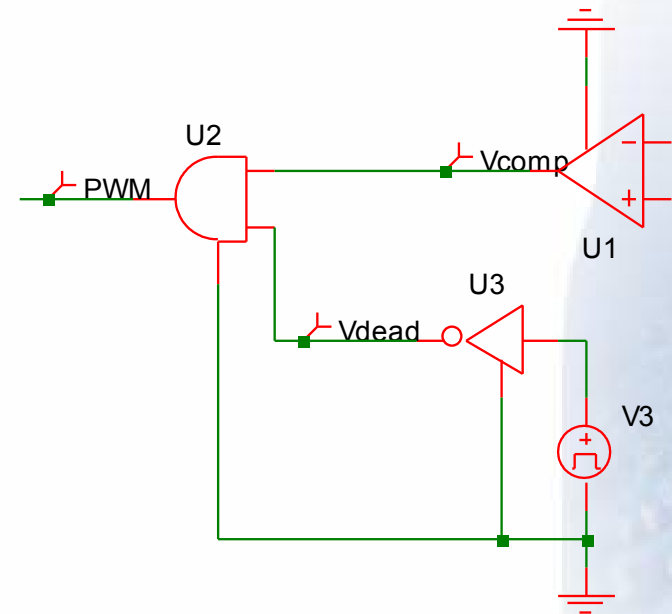
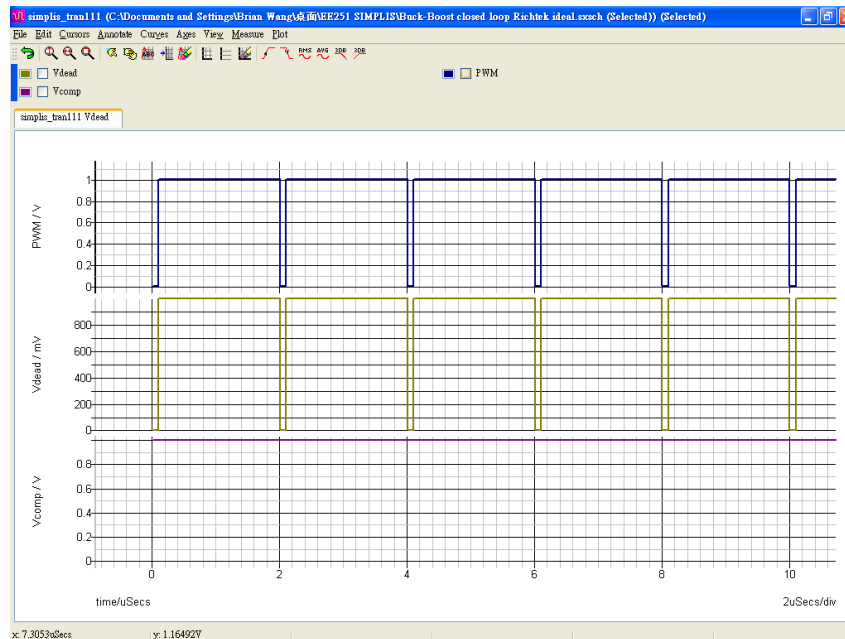


E/A's output should be connected to Comparator's - node!!

Require a dead time



Buck/Boost Converter (Closed Loop)

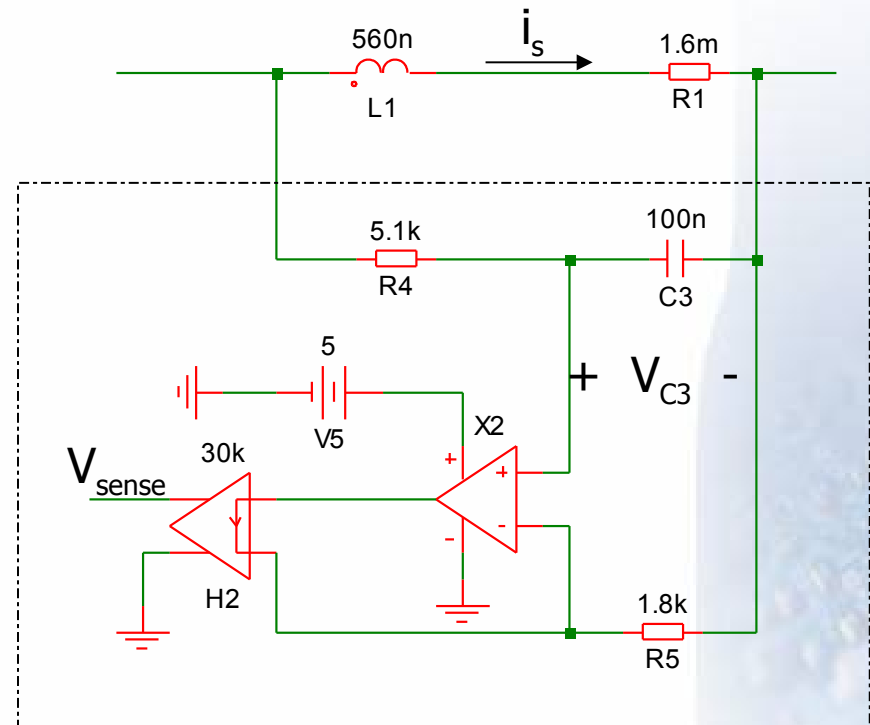


Frequently used sub-circuits

- RC current sensing (in Current-mode control)
- Use OPamp and CCVS to enhance and transmute sensed signal

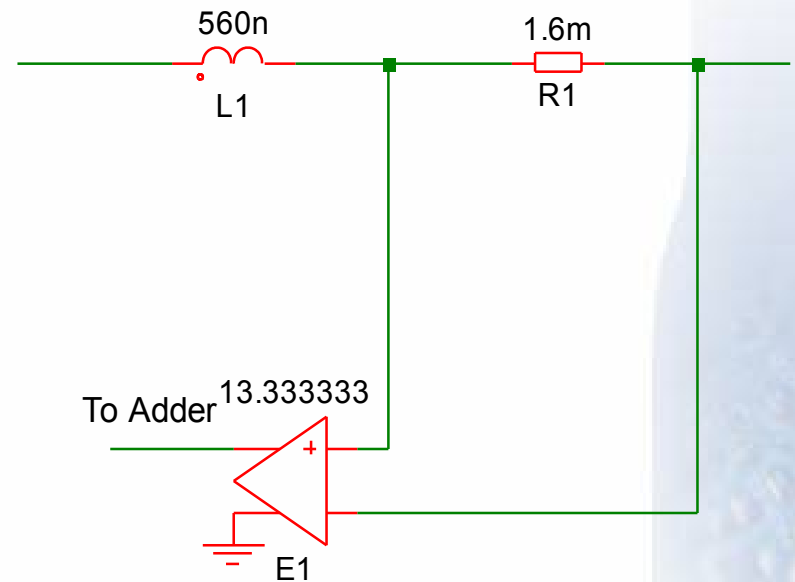
When $\frac{L_1}{R_1} = R_4 \cdot C_3$,

$$V_{sense} = K \cdot i_s = K \cdot \frac{V_{C3}}{R_1} = \left(\frac{R_1}{R_5} \cdot H_2 \right) \cdot i_s$$



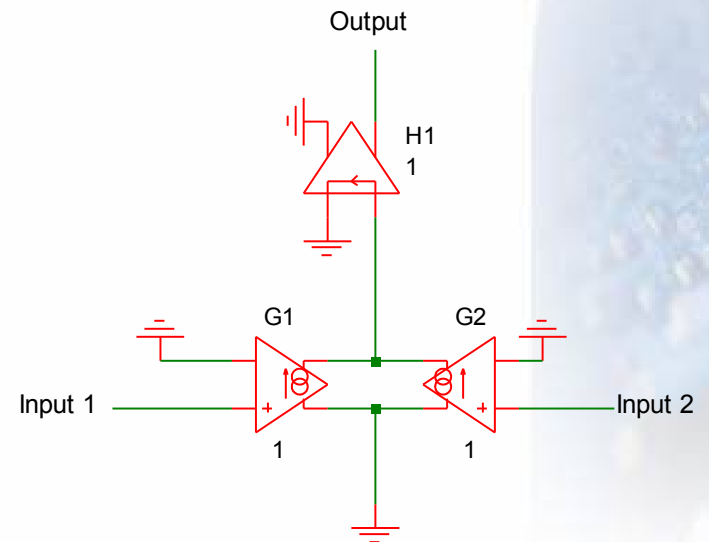
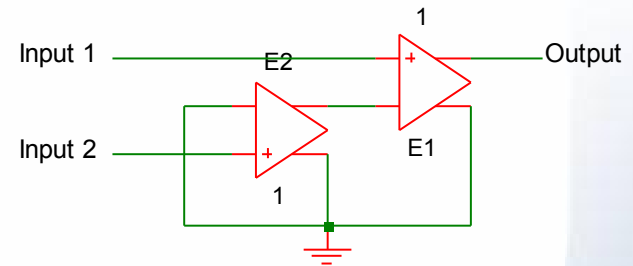
Frequently used sub-circuits

- Direct current sensing
- Ideal way, but maybe too ideal



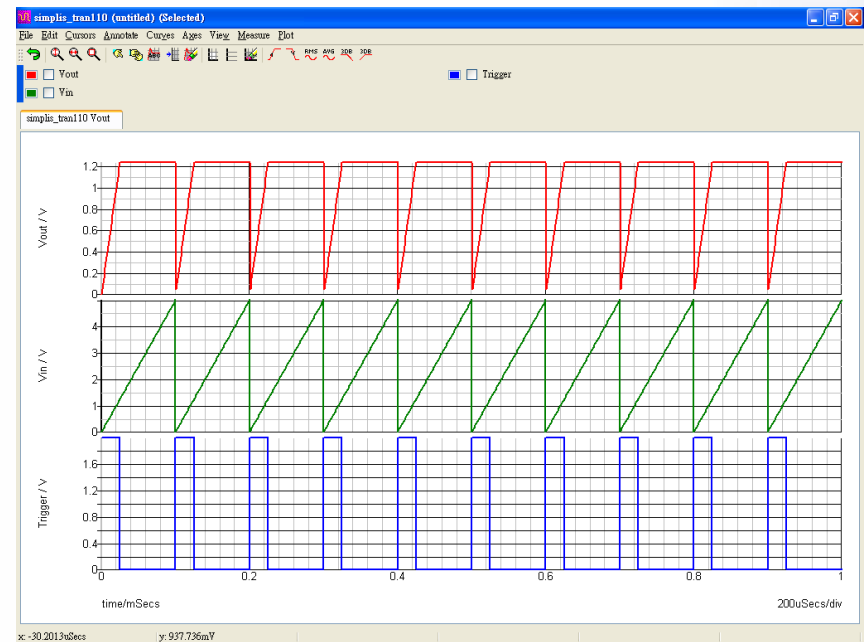
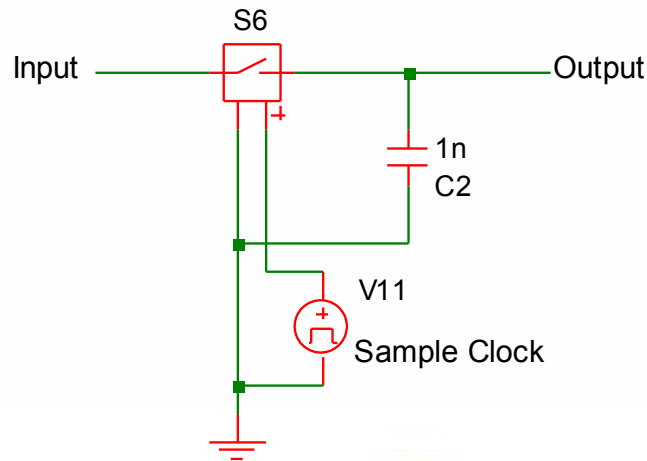
Frequently used sub-circuits

- Voltage Adder
- Many ways to implement, only driven sources needed

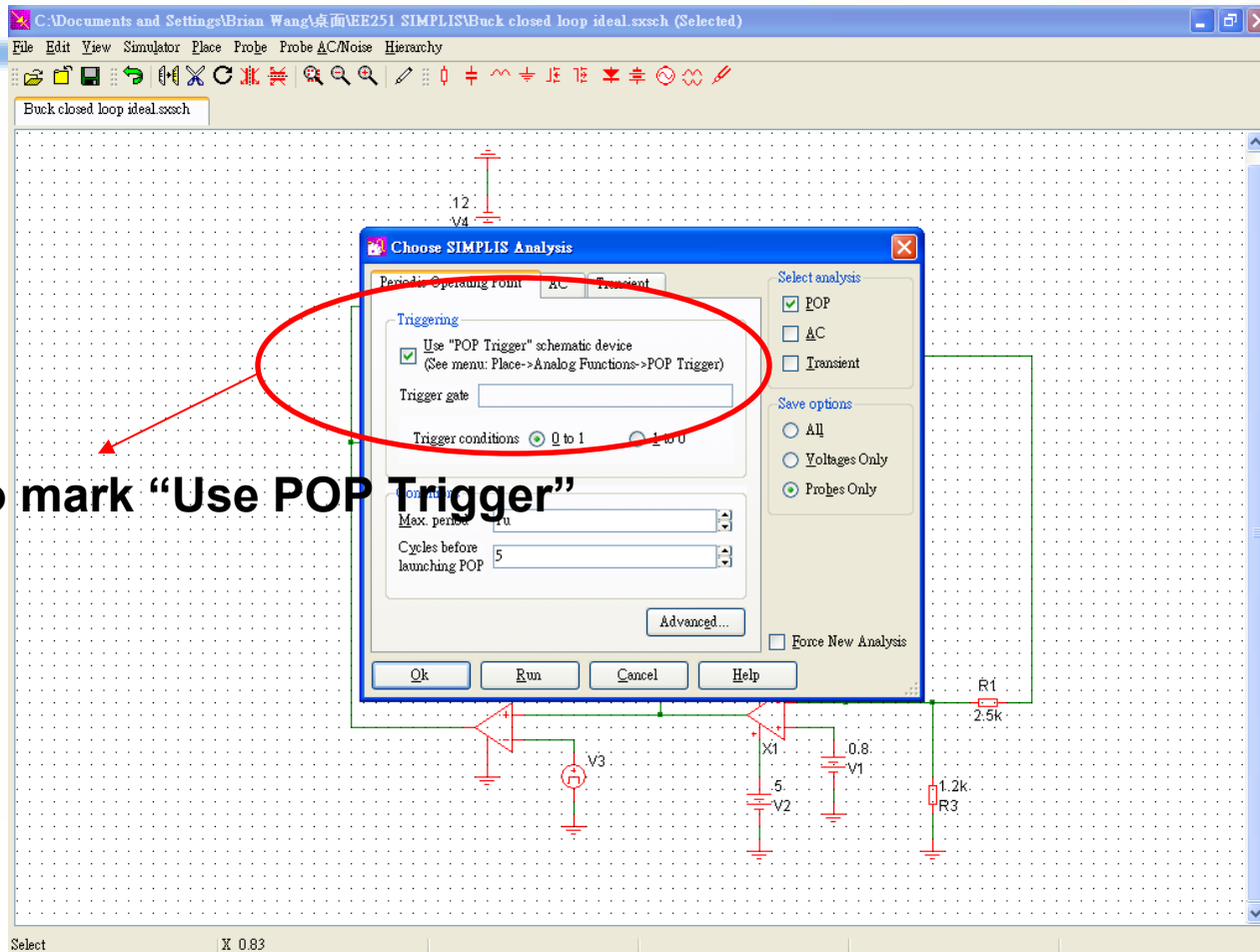


Frequently used sub-circuits

- Sample and Hold
- Trigger = high: sample
Trigger = low: hold



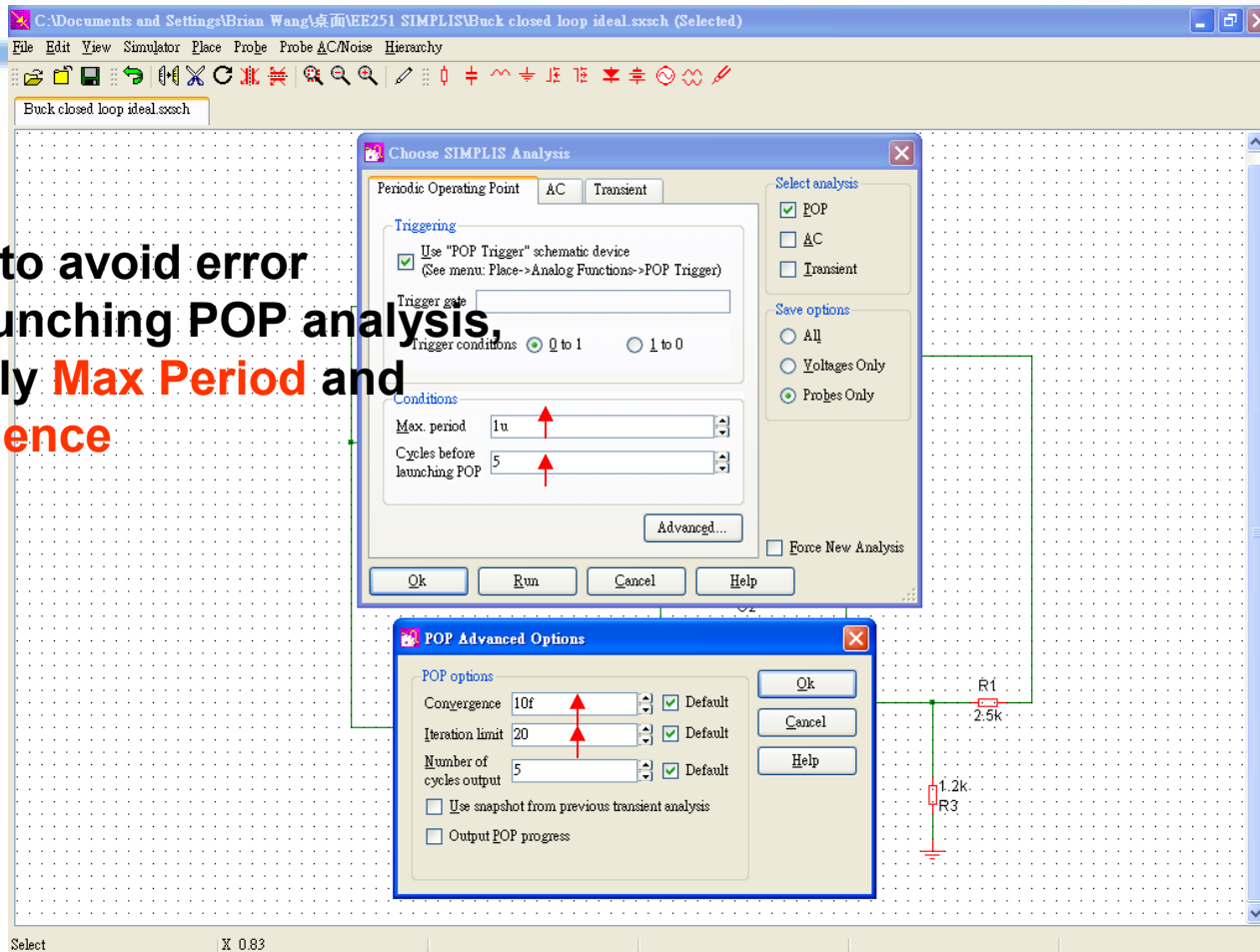
Periodic Operating Point (POP) analysis



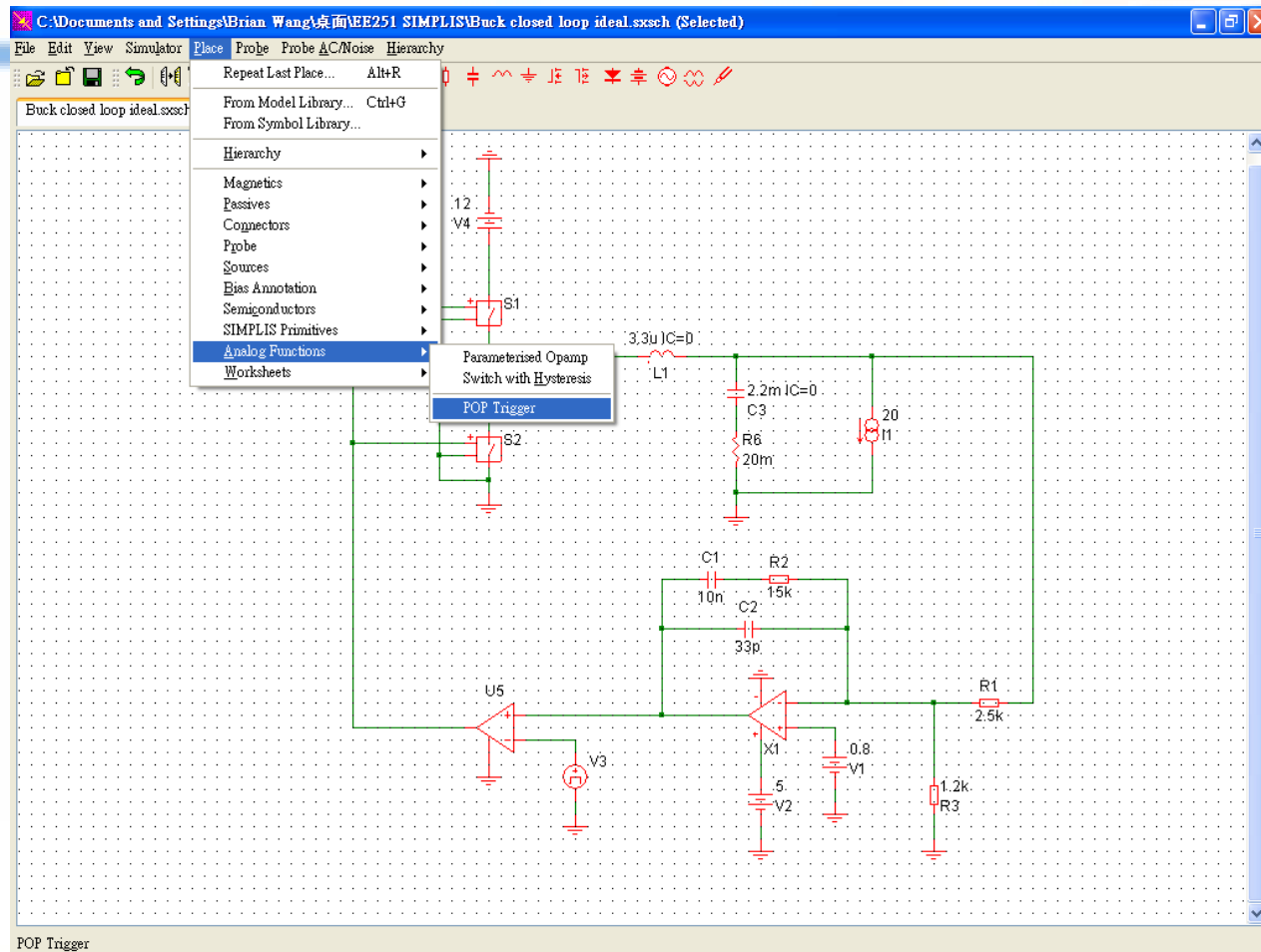
POP analysis settings

Periodic Operating Point (POP) analysis

↑ : higher to avoid error
when launching POP analysis,
especially **Max Period** and
Convergence

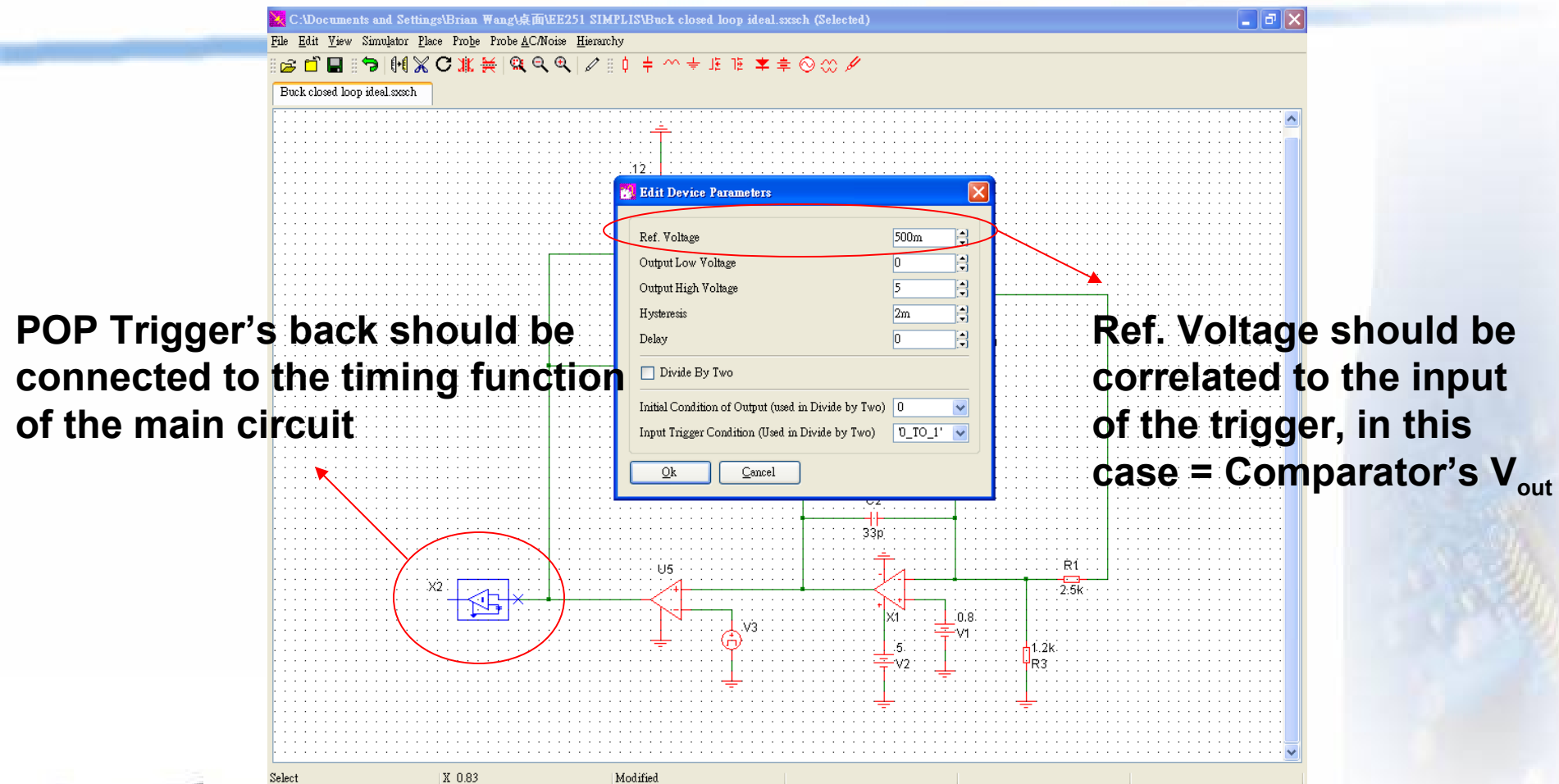


Periodic Operating Point (POP) analysis



Put POP Trigger into the circuit

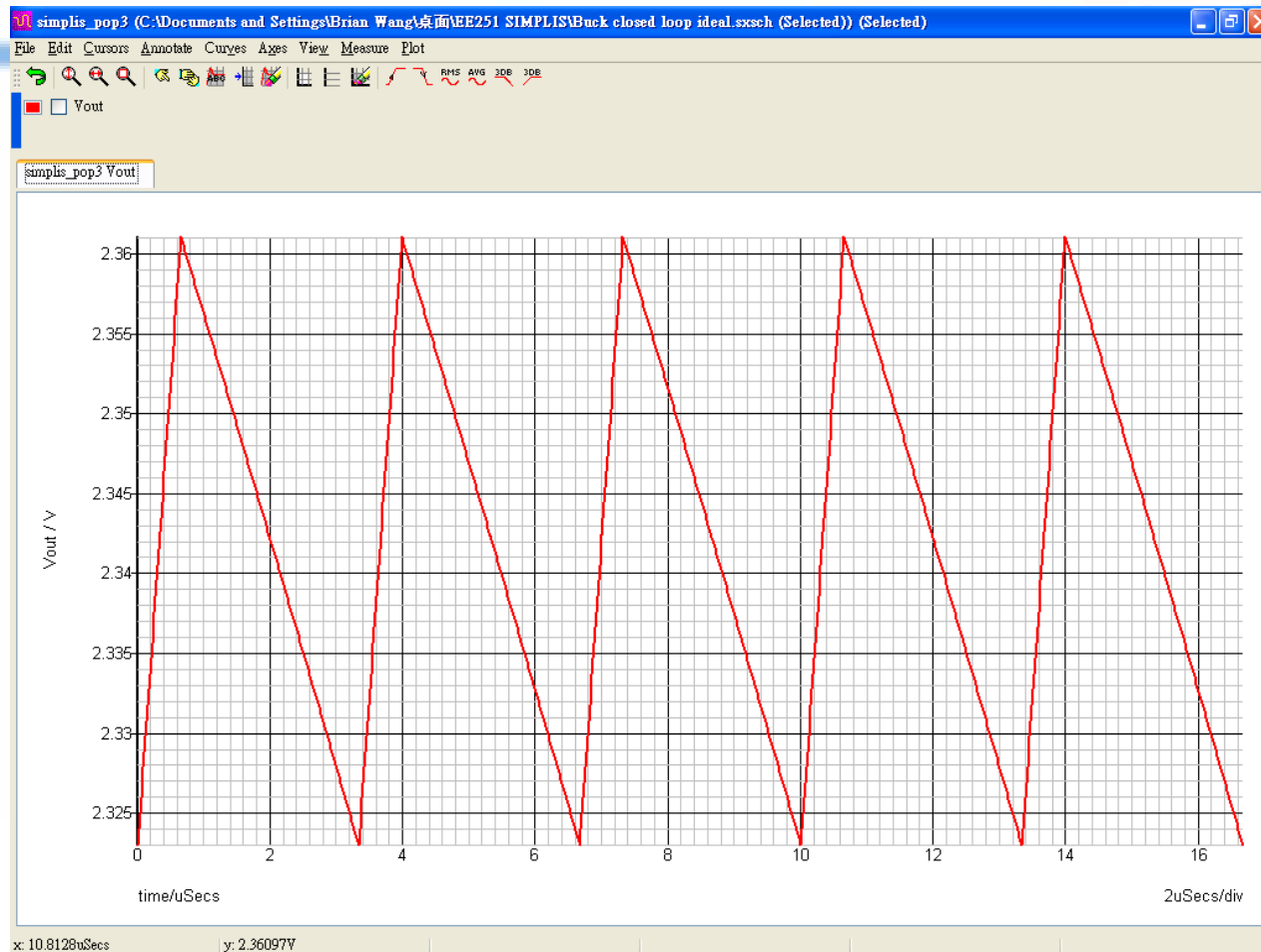
Periodic Operating Point (POP) analysis



POP Trigger's back should be connected to the timing function of the main circuit

Ref. Voltage should be correlated to the input of the trigger, in this case = Comparator's V_{out}

Periodic Operating Point (POP) analysis

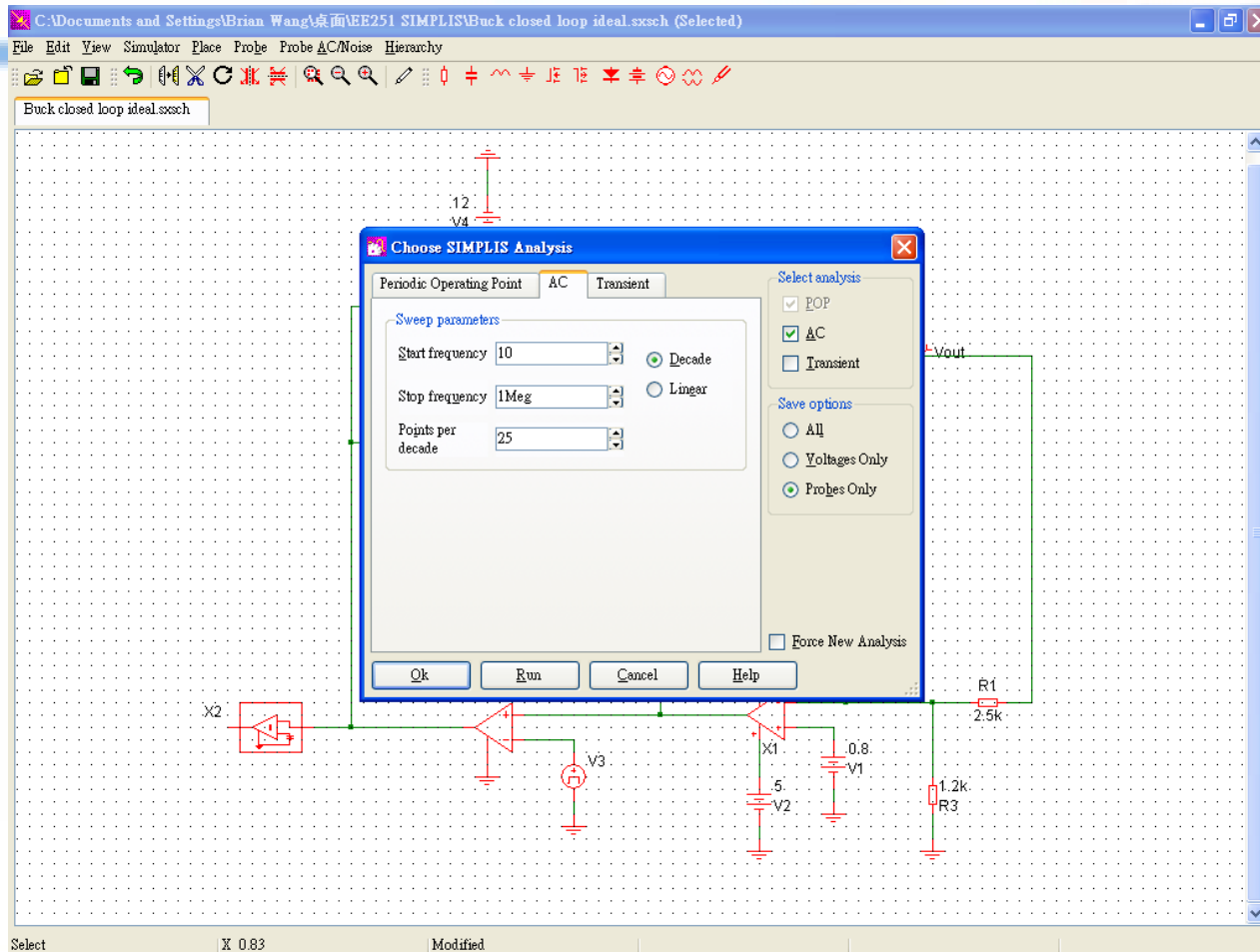


POP analysis waveform: no importance

Periodic Operating Point (POP) analysis

- In SIMPLIS, users have to perform following simulation steps before launching AC simulation:
 1. Transient analysis and back-annotated
 2. POP simulation (add POP trigger)
 3. Add AC source and Bode Plot Probe

AC analysis



AC analysis

- Measuring loop gain in the simulator :
Different ways in different software

PSPICE V.S. SIMPLIS

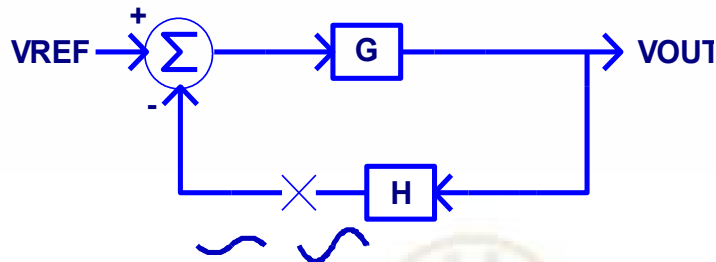


AC analysis

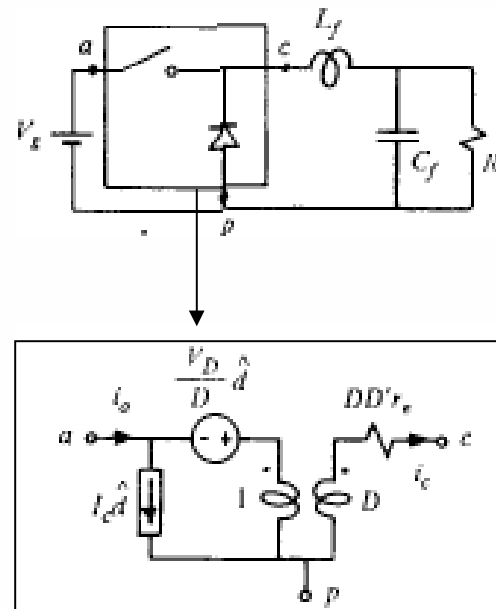
1. In PSPICE —

- (1) Breaking the feedback loop and inserting an AC source.
- (2) **Must replace switches into averaged models [4]**

(1)



(2)



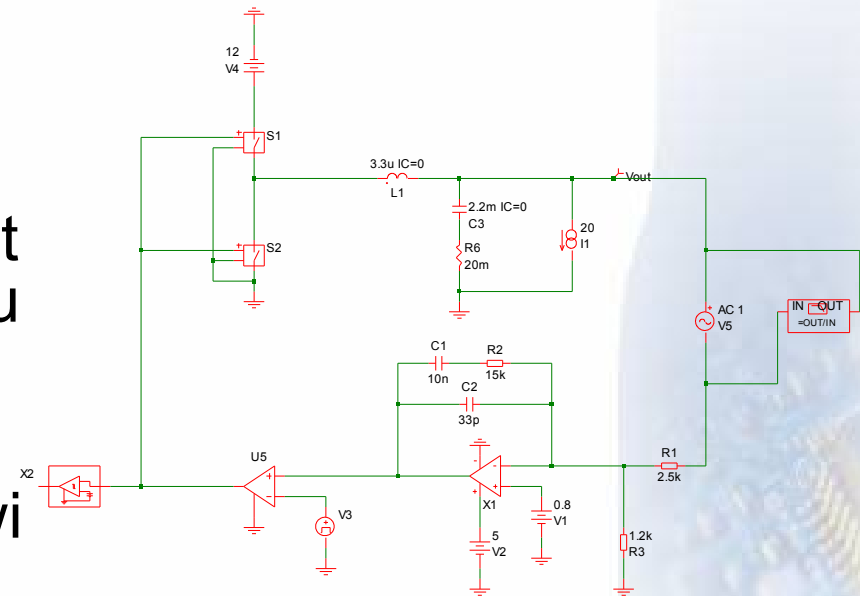
AC analysis

2. In SIMPLIS —

(1) Just add AC source in any place of the loop

(2) Add Bode Plot probe at the place we want to measure

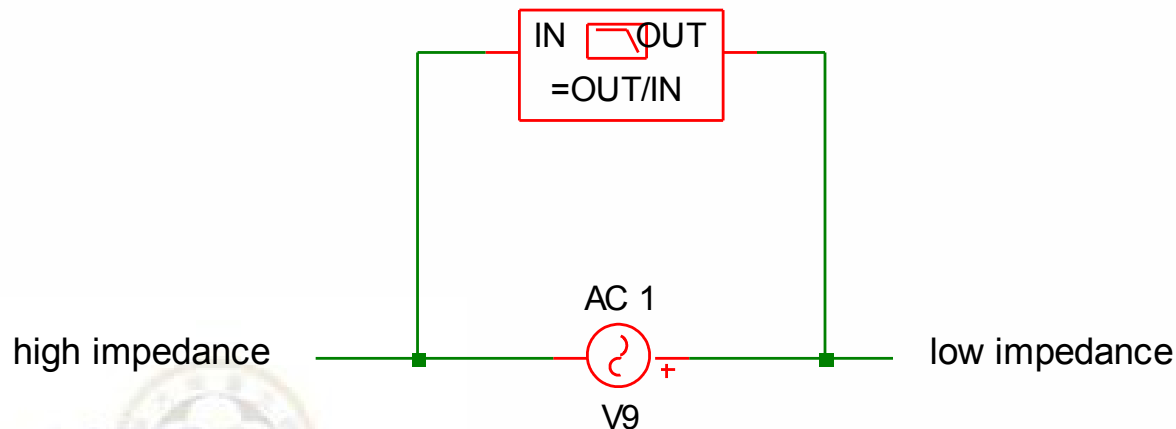
(3) Switches can be used without any average modeling



We don't have to change any part of the circuit

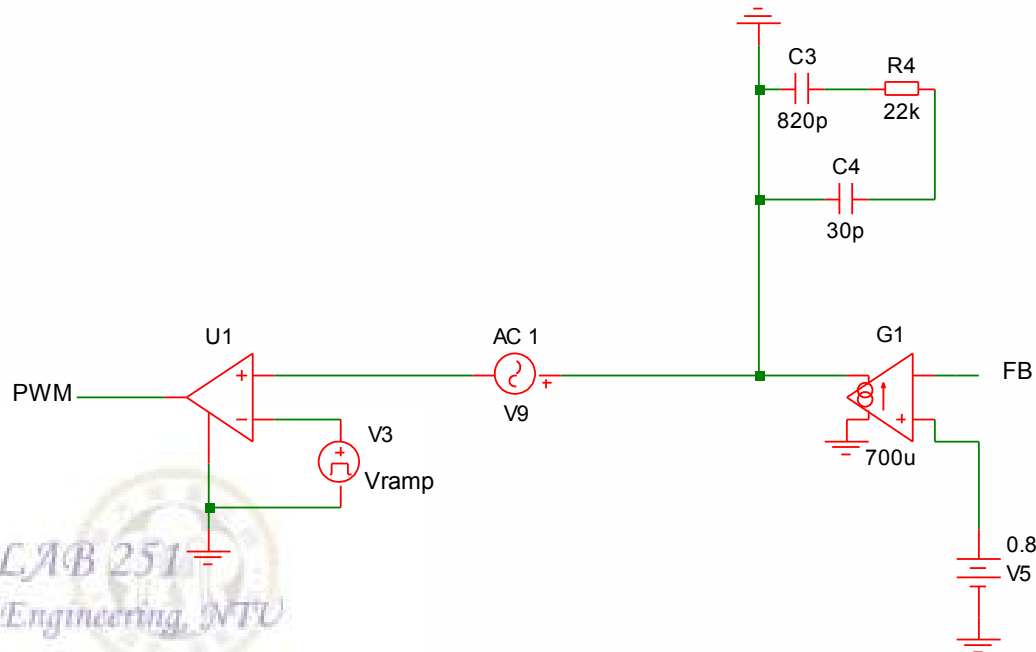
AC analysis: Disturbance Injection Point

- In Practical measurement, rules will be:
Injection point — high impedance
Measurement point — low impedance
- In SIMPLIS: many points can be injected



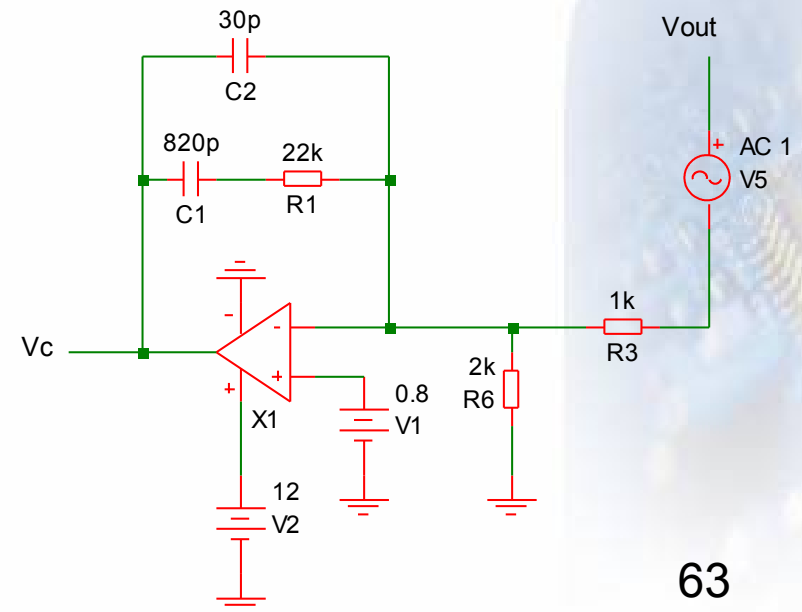
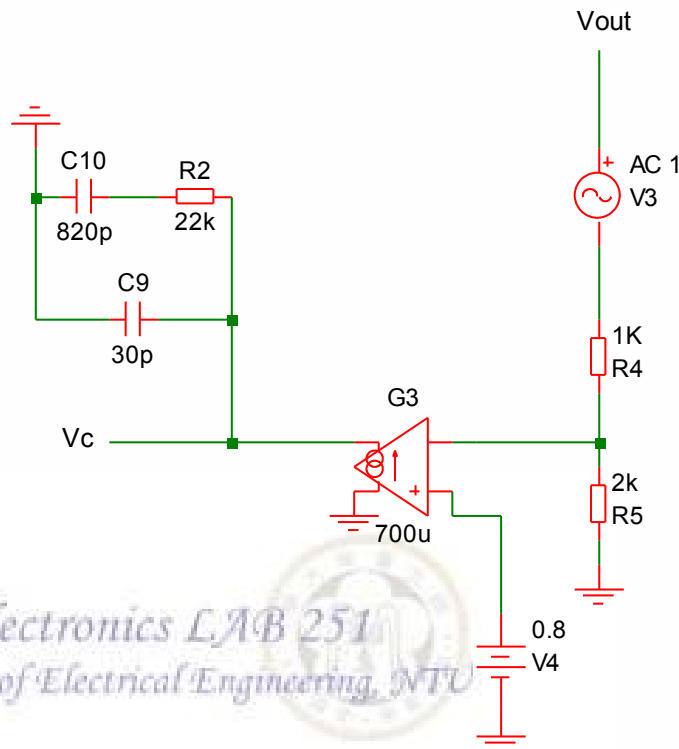
AC analysis: Disturbance Injection Point

- Injection between error Amp and Comparator:
The best injection point
- Cannot be found in real ICs

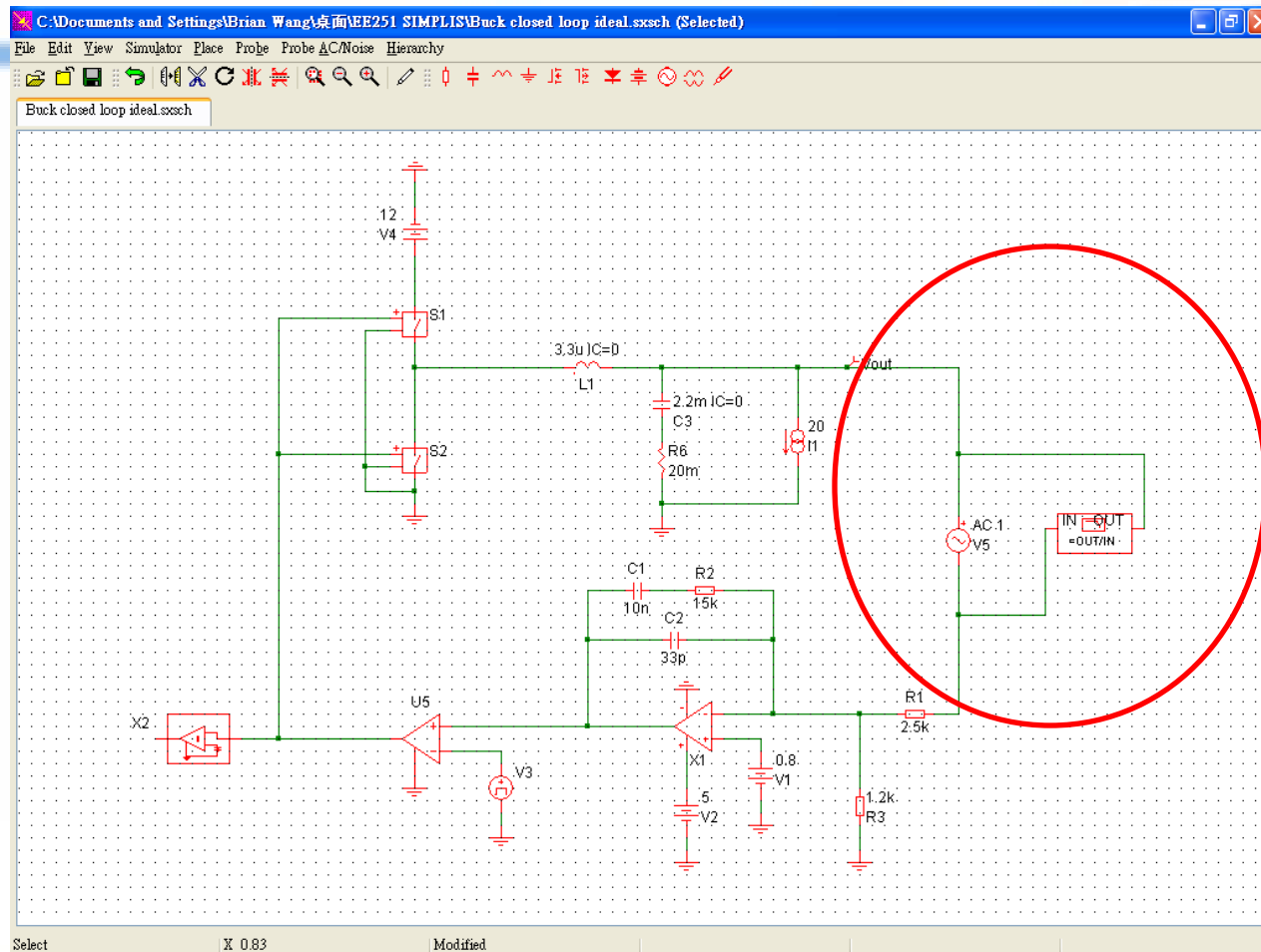


AC analysis: Disturbance Injection Point

- Injection between V_{out} and Compensation: Good injection point
- Can be found in real ICs



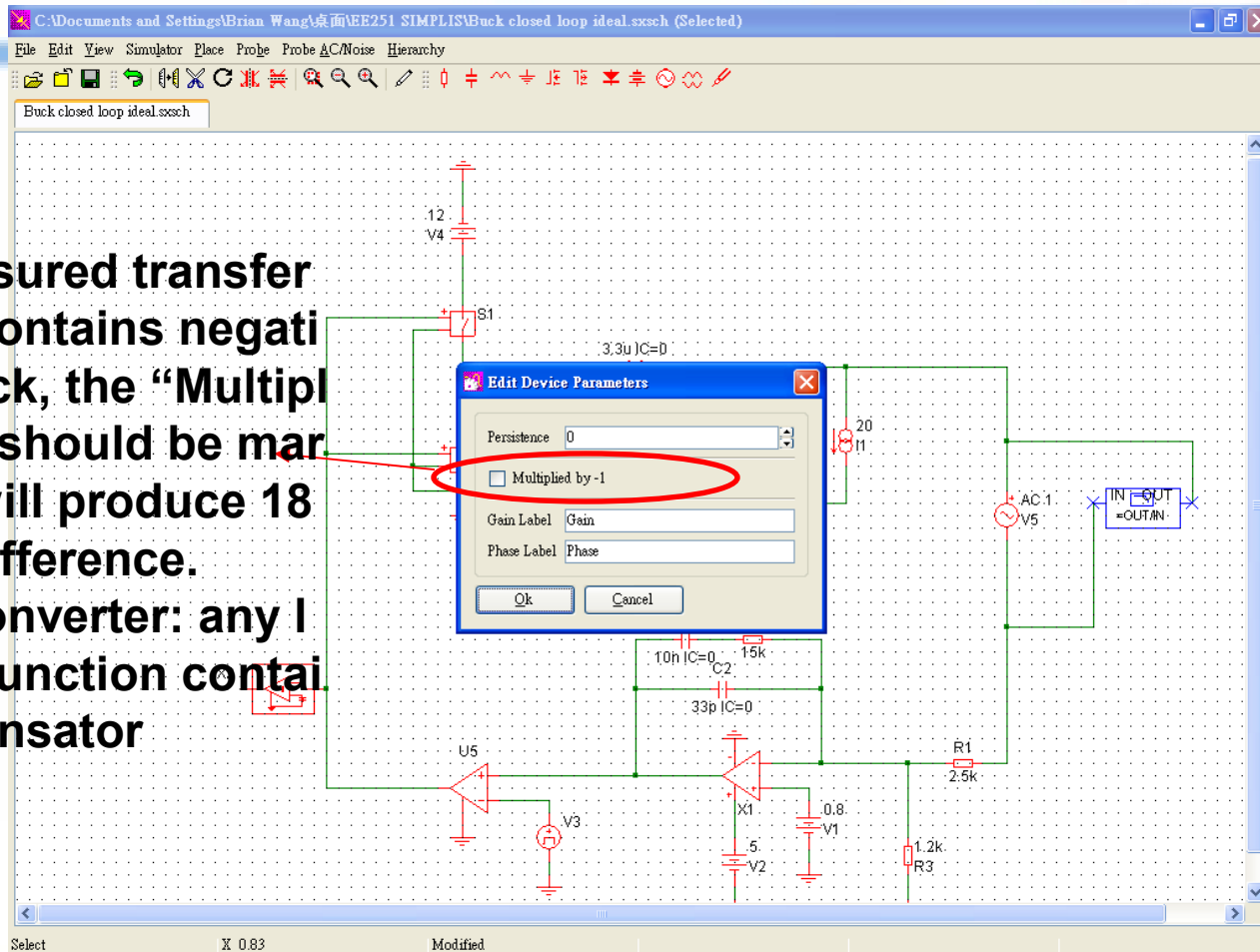
AC analysis: Buck converter (closed-loop)



Method 1: Add AC source and Bode Plot Probe into the circuit

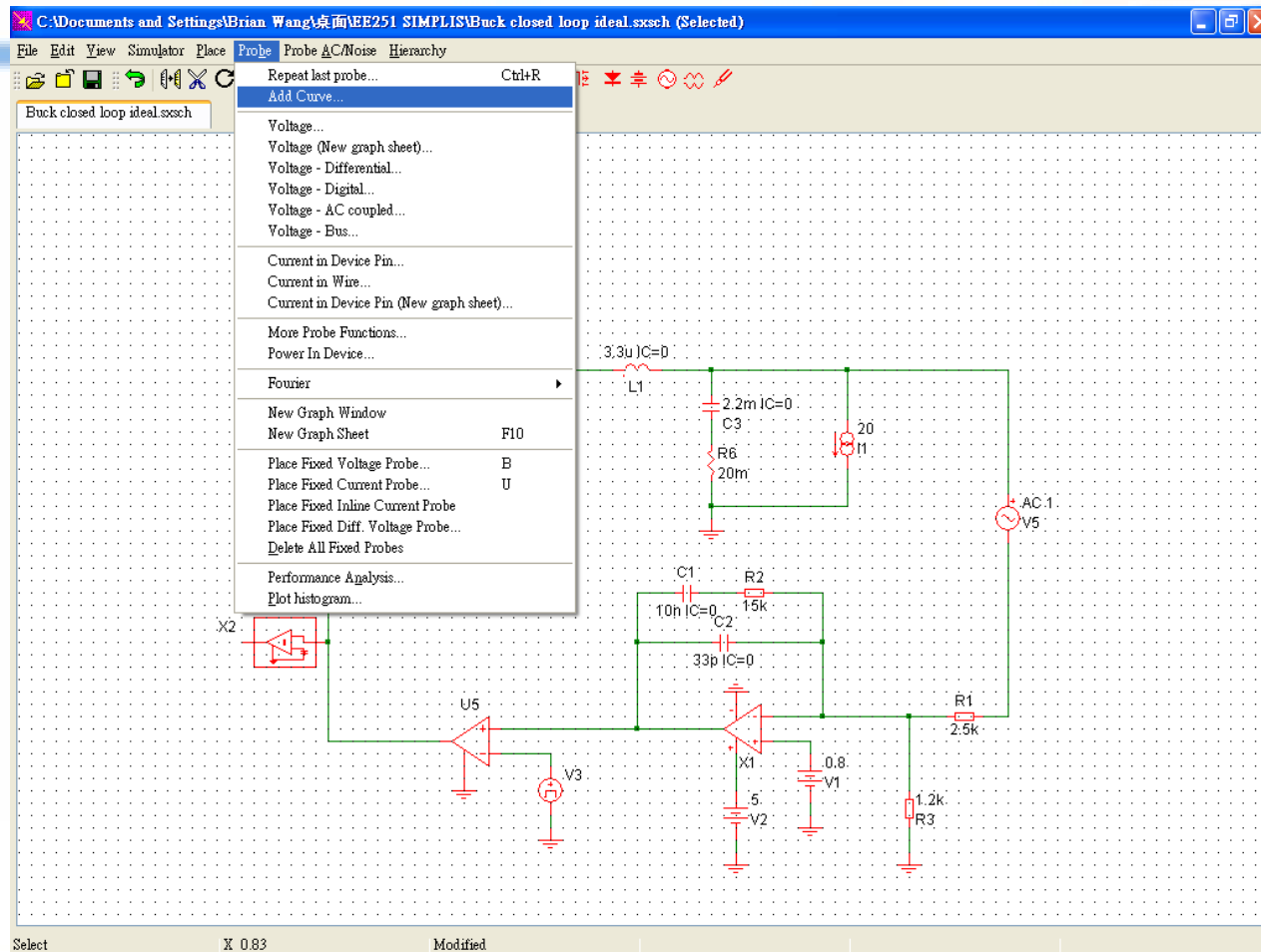
AC analysis: Buck converter (closed-loop)

If the measured transfer function contains negative feedback, the “Multiplied by -1” should be marked or it will produce 180 phase difference.
In Buck converter: any loop gain function contains Compensator



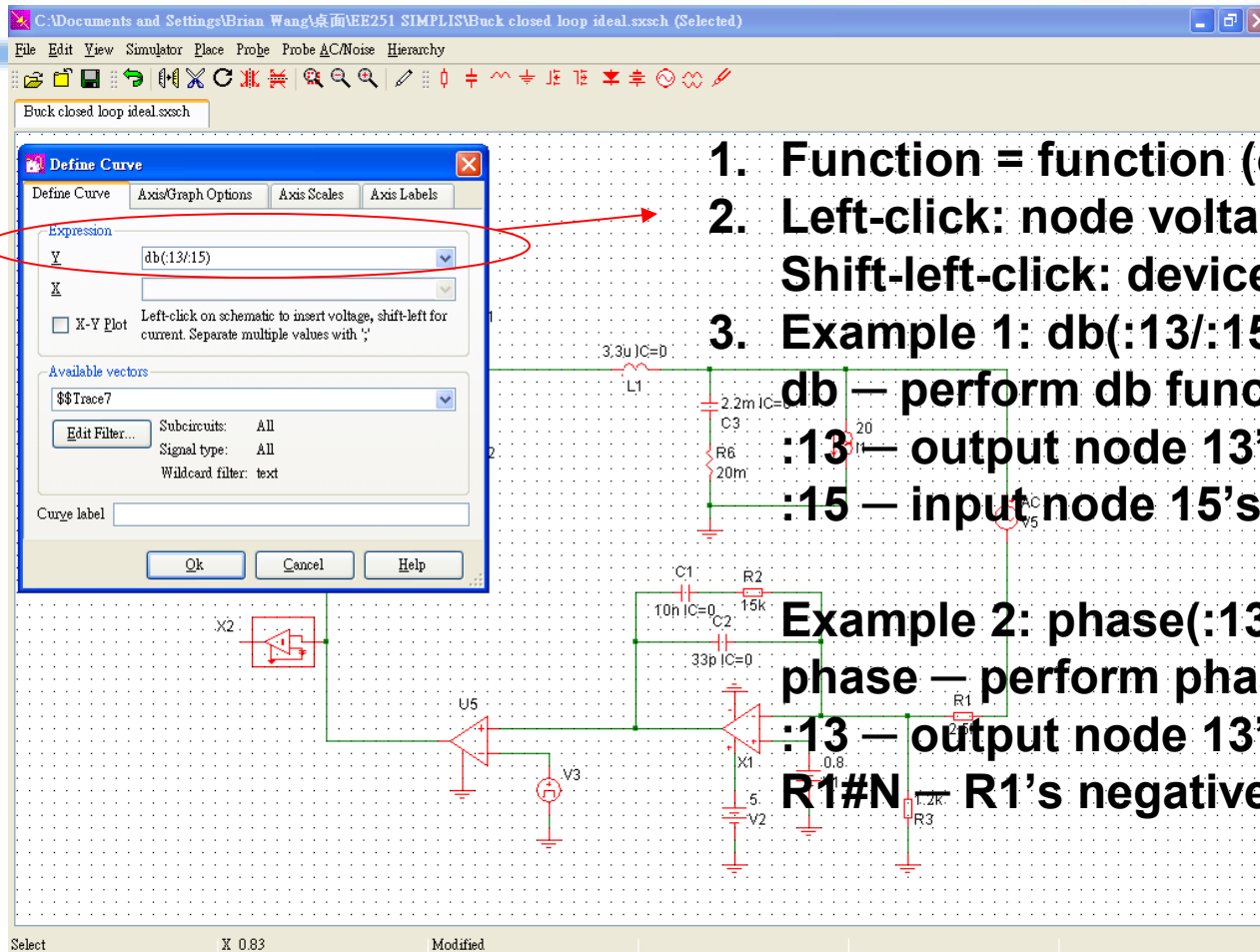
Method 1: Bode plot probe settings

AC analysis: Buck converter (closed-loop)



Method 2: Add AC source into the circuit and use the function “Add Curve” after running AC analysis

AC analysis: Buck converter (closed-loop)



1. Function = function (output / input)
2. Left-click: node voltage
Shift-left-click: device current
3. Example 1: db(:13/:15)

db — perform db function

:13 — output node 13's voltage

:15 — input node 15's voltage

Example 2: phase(:13/R1#N)

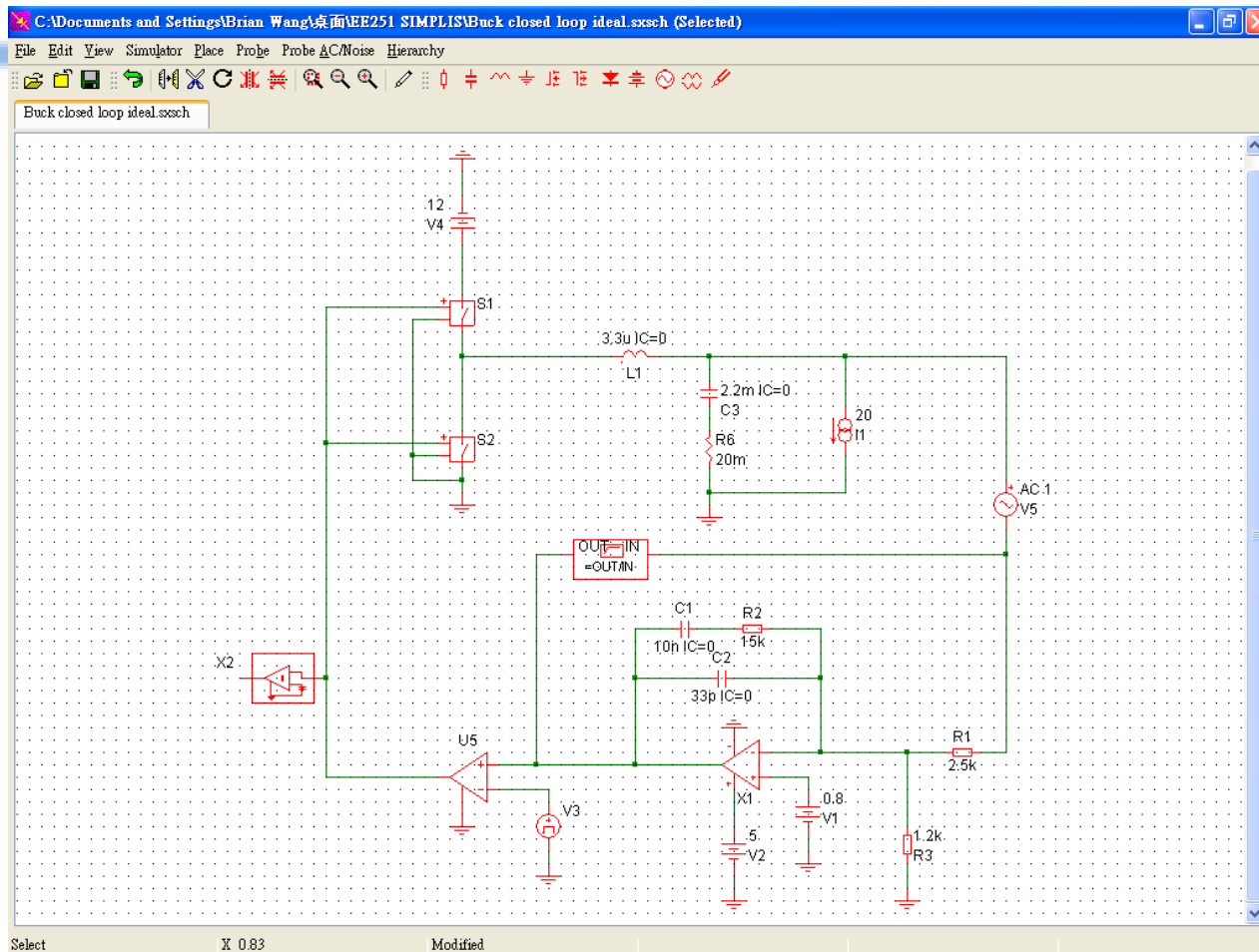
phase — perform phase function

:13 — output node 13's voltage

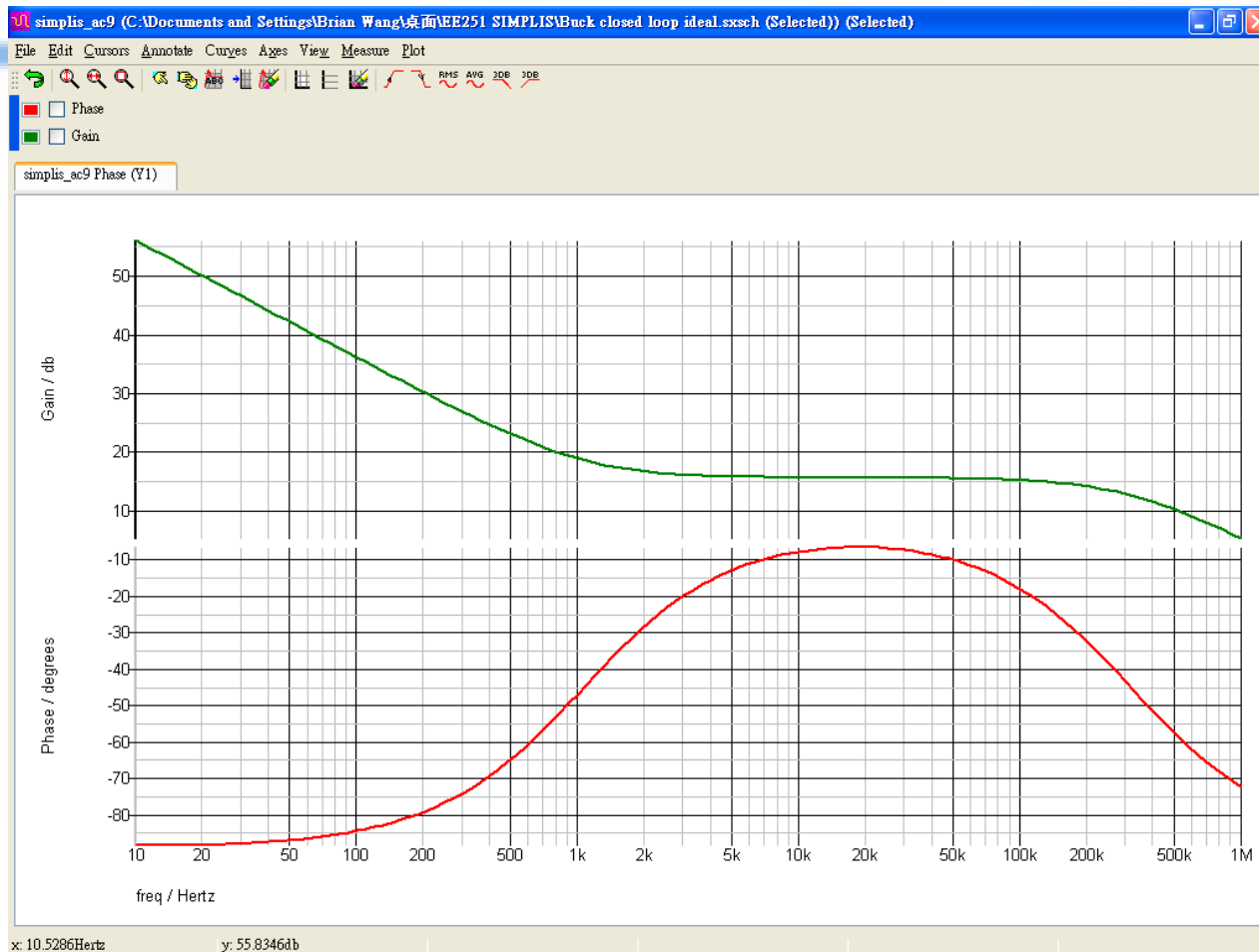
R1#N — R1's negative current

Method 2: Define required curve's function at Y Expression

AC analysis: Buck converter (closed-loop)

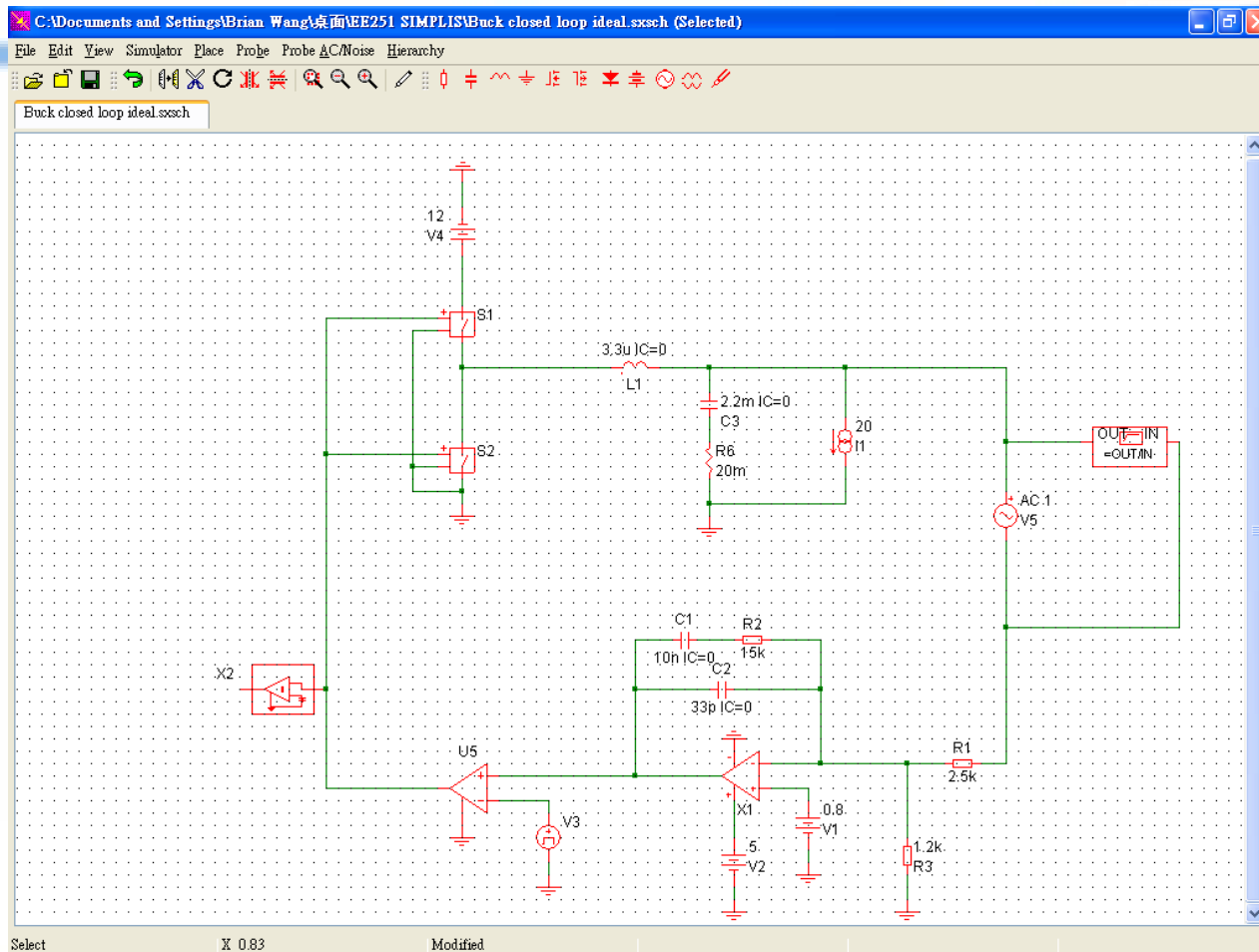


AC analysis: Buck converter (closed-loop)



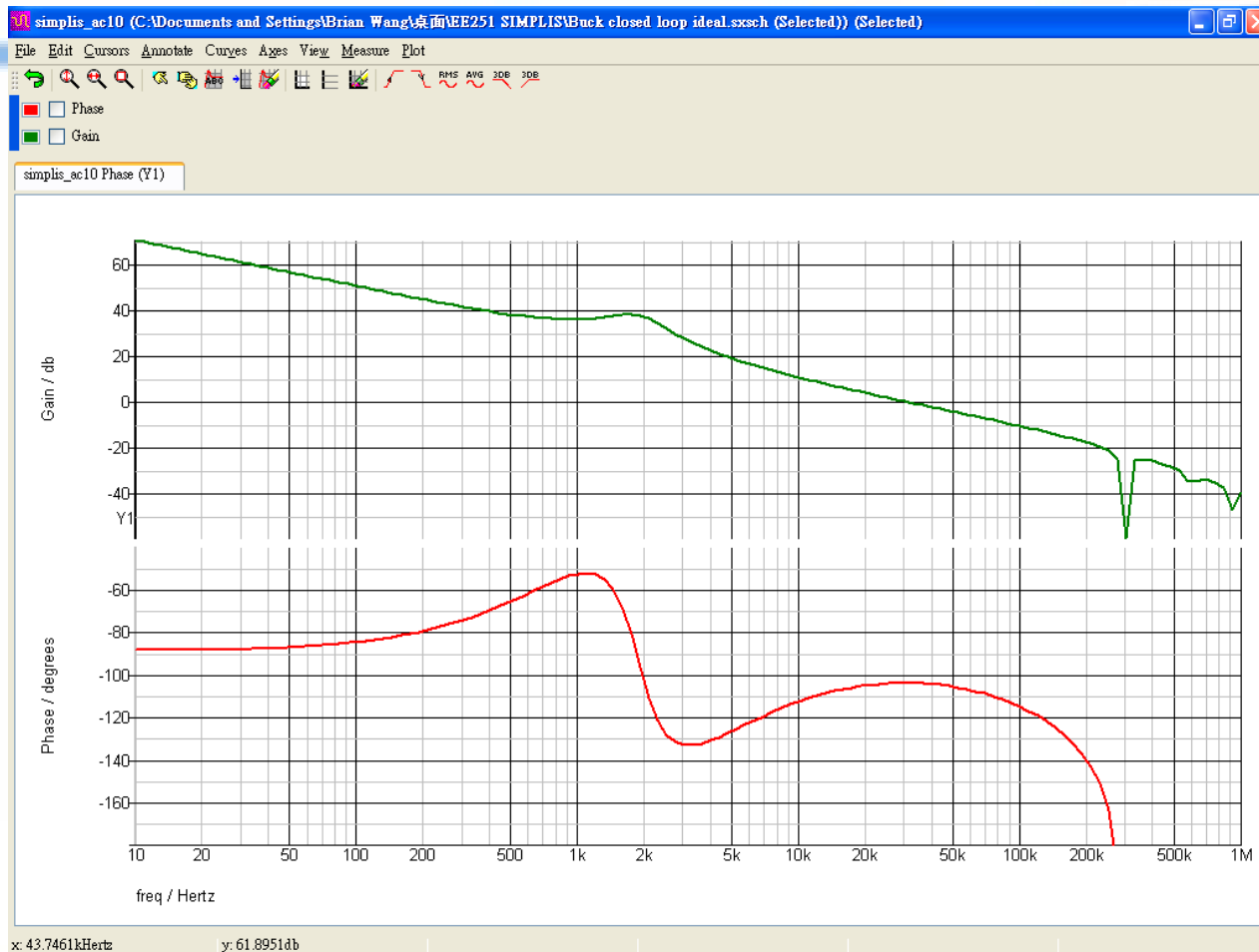
Code plots of Compensation (A)

AC analysis: Buck converter (closed-loop)



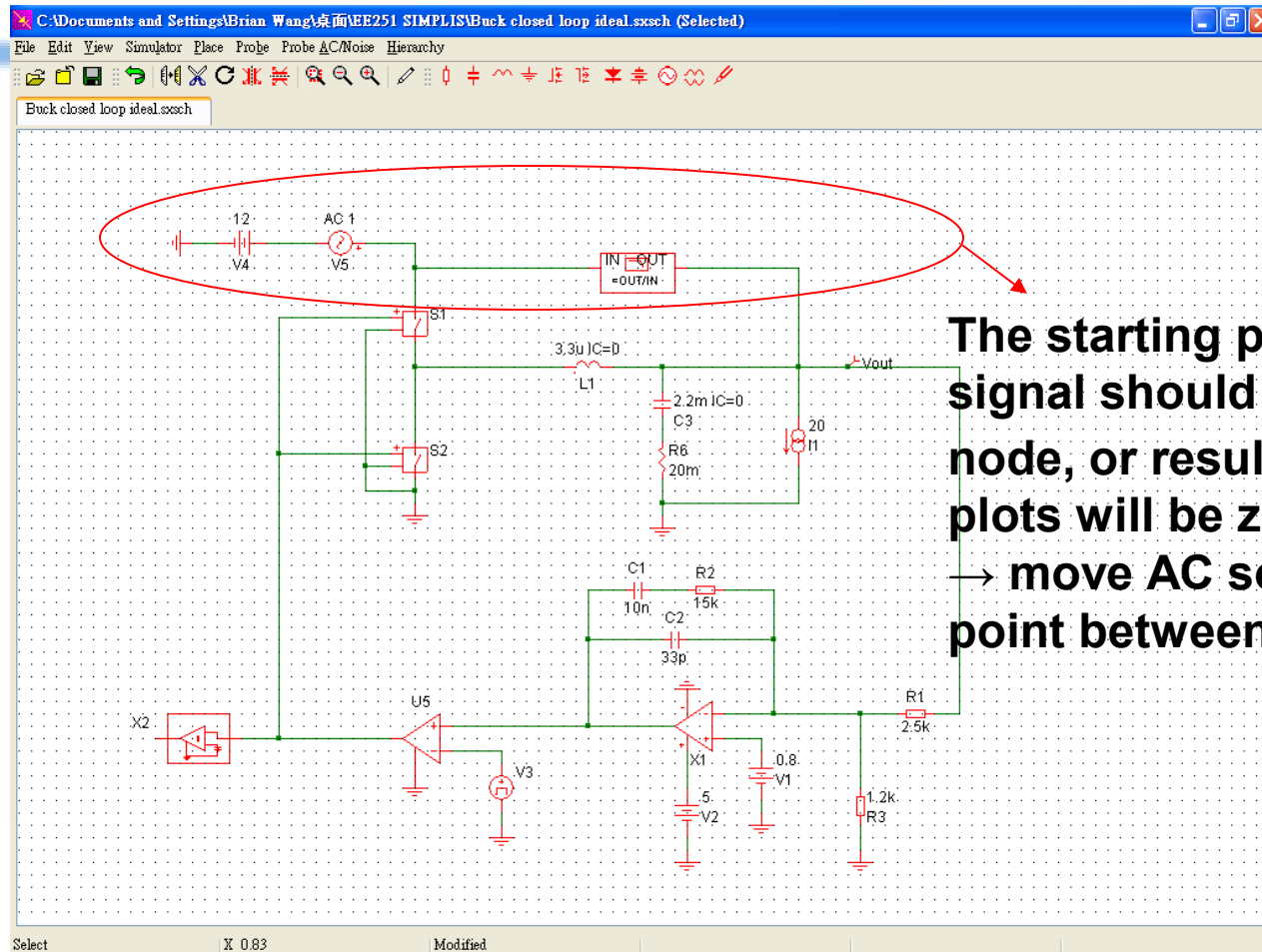
Measurement: Loop Gain ($T = G_d * F_m * A$)

AC analysis: Buck converter (closed-loop)



Bode plots of Loop Gain ($T = G_d * F_m * A$)

AC analysis: Buck converter (closed-loop)



The starting point of AC signal should be at V_g node, or resultant Bode plots will be zero
 → move AC source to the point between V_g and Probe

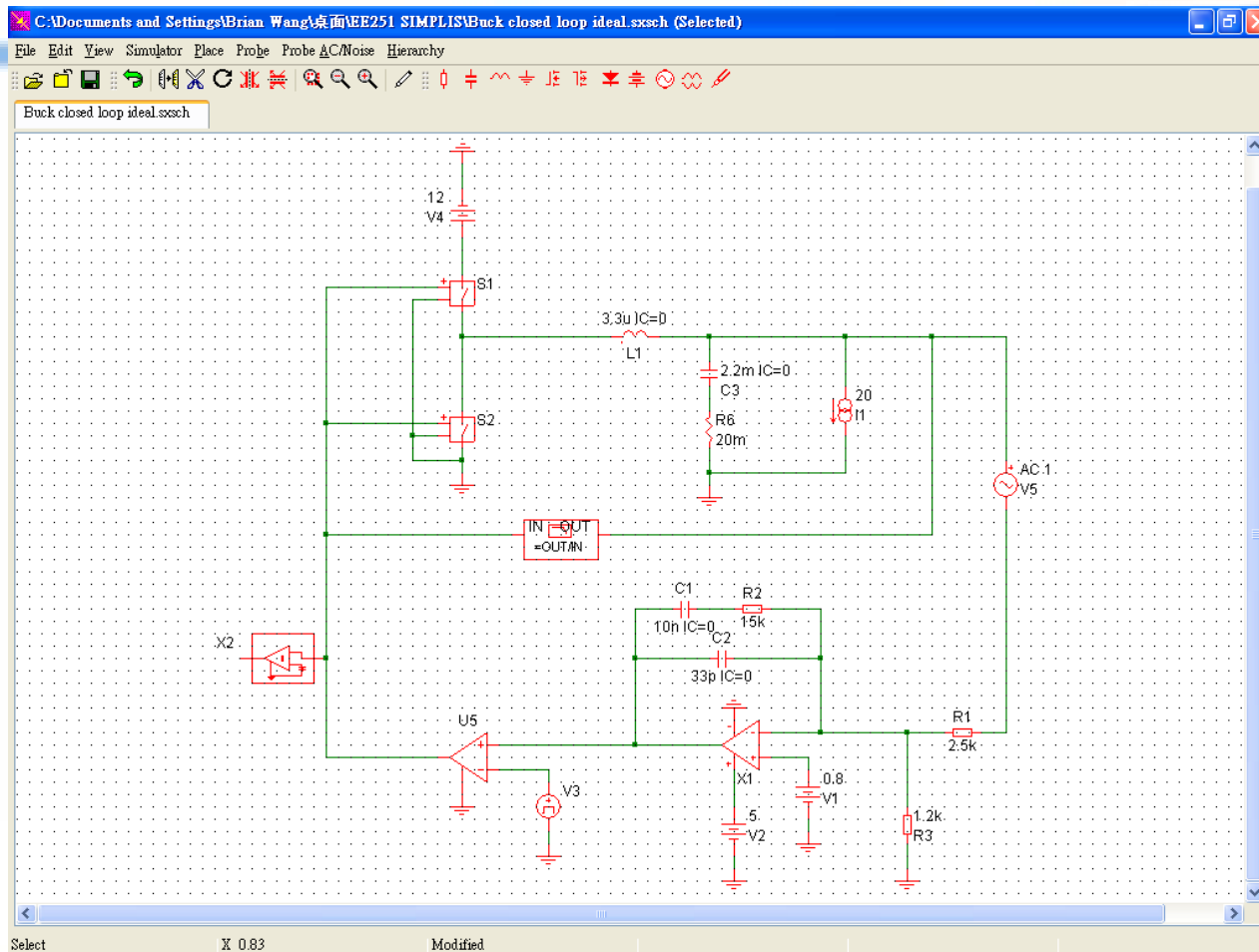
Measurement: $G_{V(\text{closed loop})} = V_o/V_g$

AC analysis: Buck converter (closed-loop)

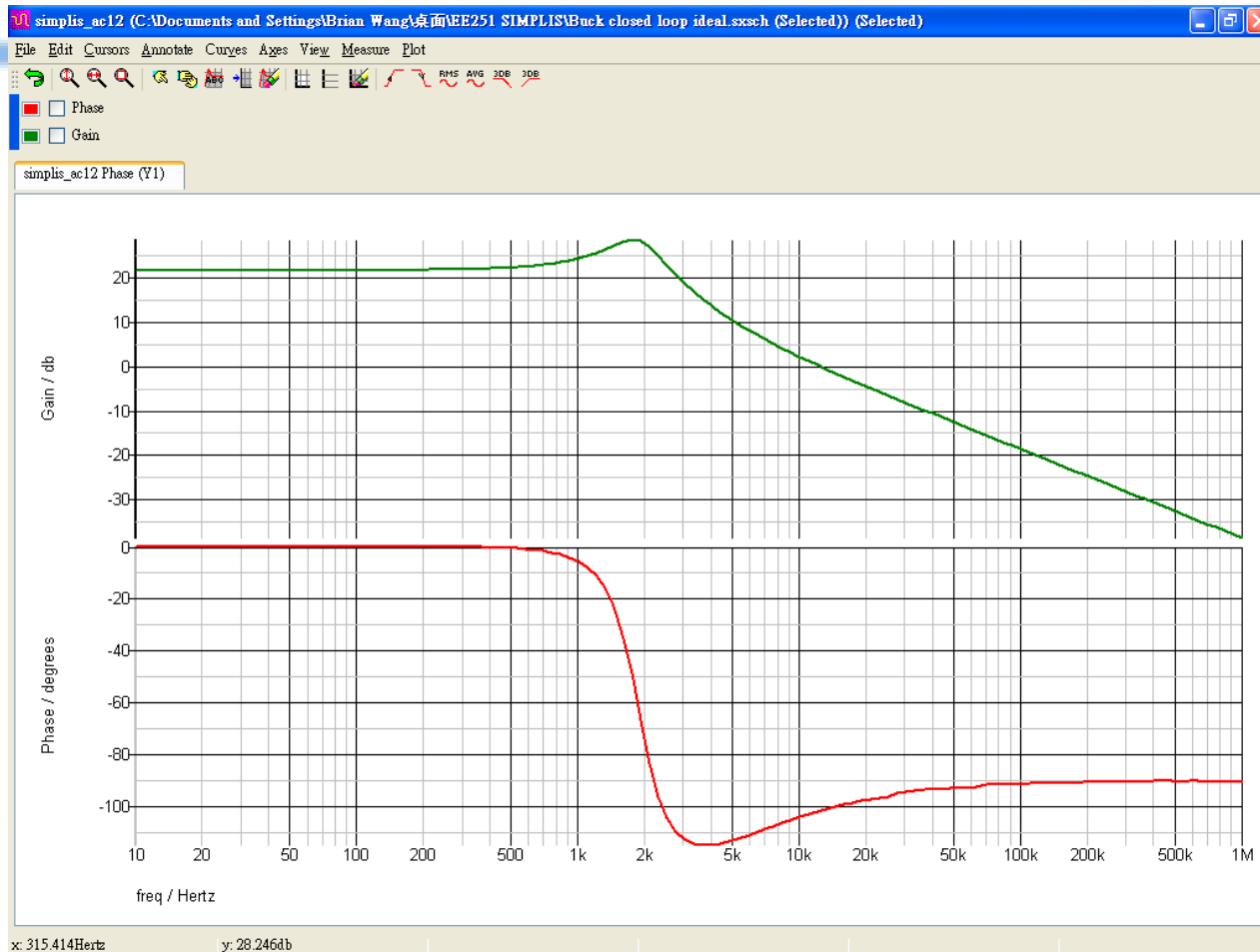


Code plots of $G_{V(\text{closed loop})} = V_o/V_g$

AC analysis: Buck converter (closed-loop)



AC analysis: Buck converter (closed-loop)



AC analysis: Buck converter (closed-loop)

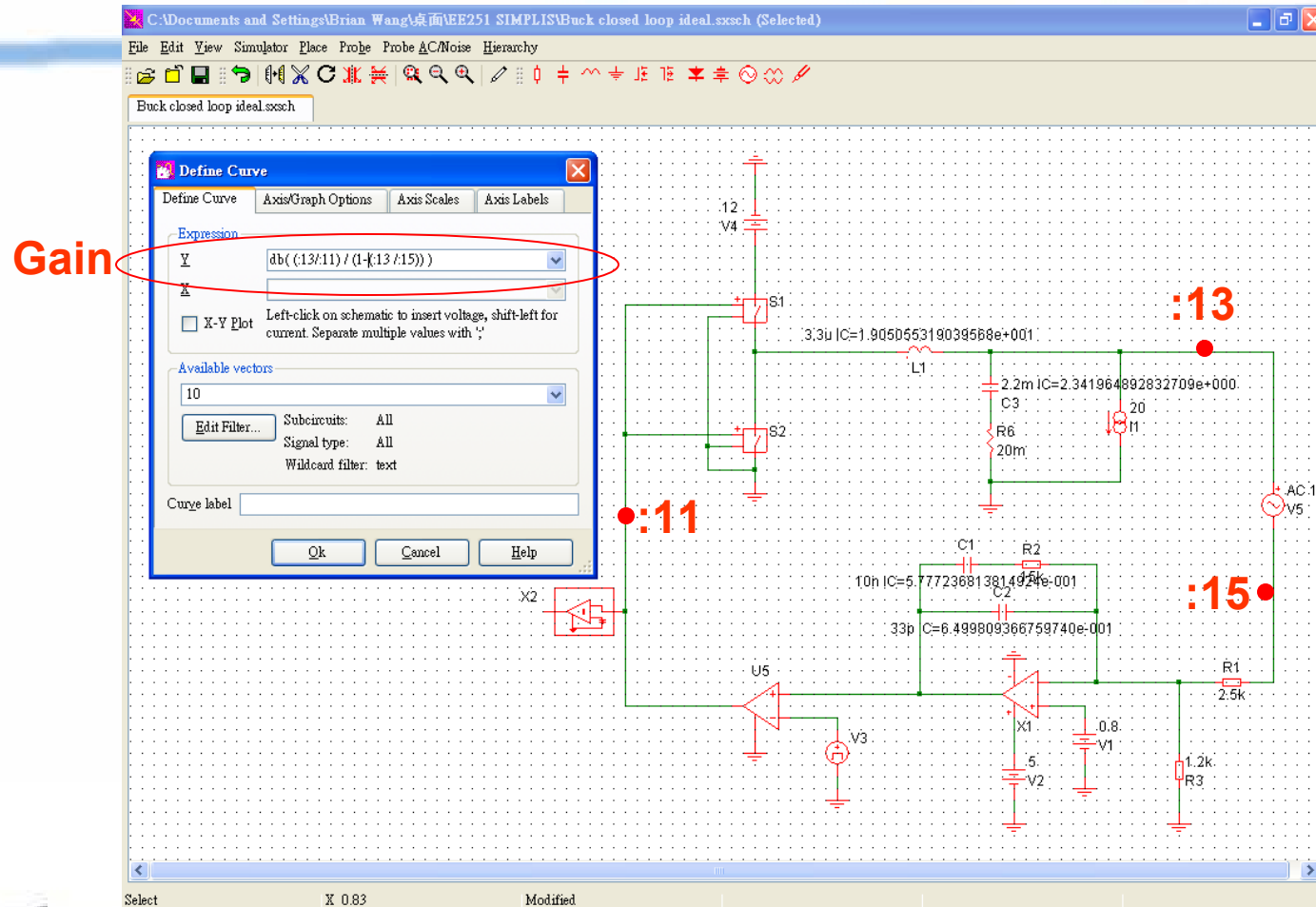
We have known the starting and ending points of $G_{d(open\ loop)}$ and T , so we use the equation:

$$G_{d(closed_loop)} = \frac{G_{d(open_loop)}}{1 + T} = \frac{G_{d(open_loop)}}{1 + G_{d(open_loop)} \times F_m \times A}$$

to get the information of $G_{d(closed\ loop)}$ using “Add Curve”

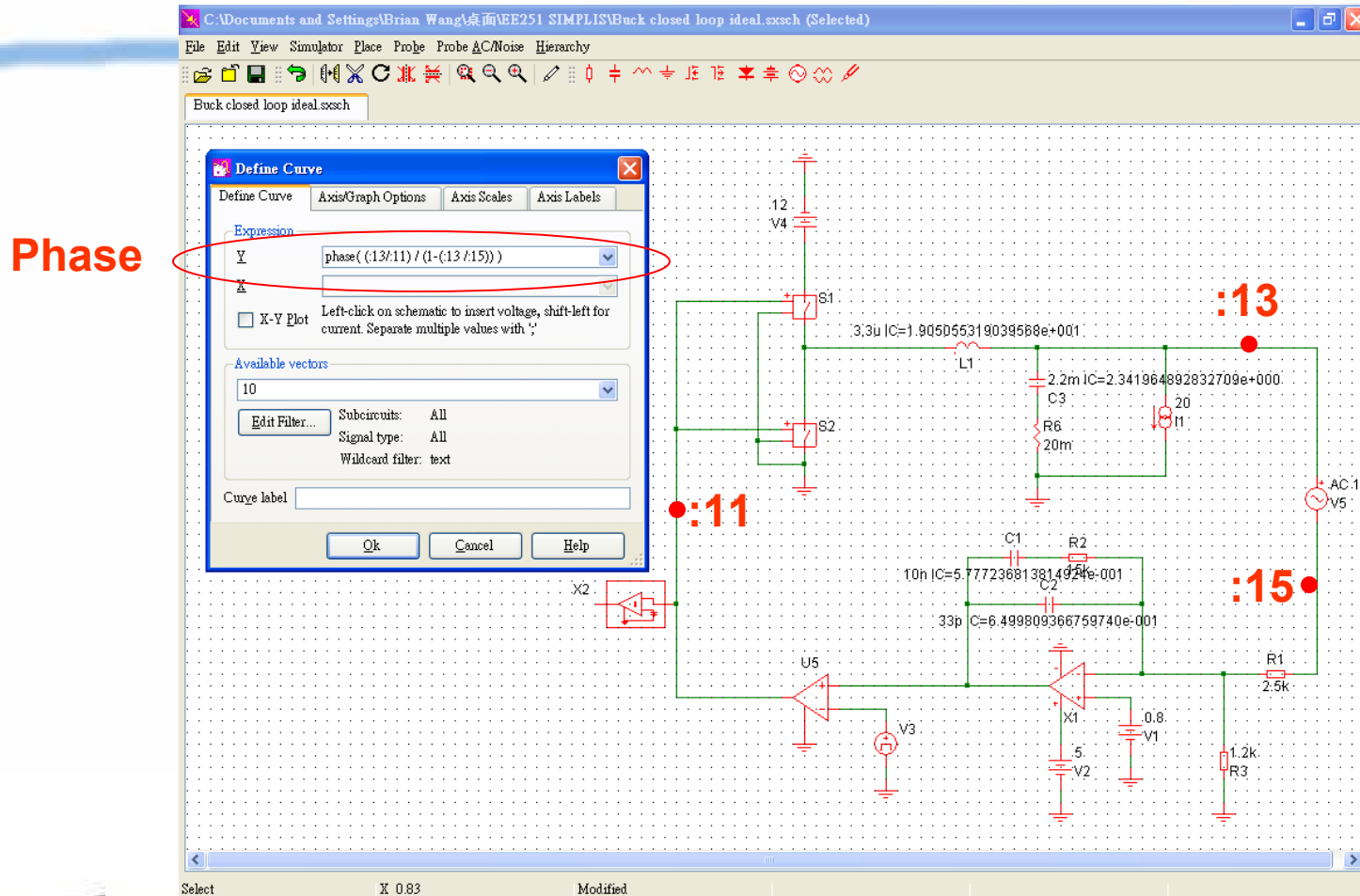
Directly using a Bode plot probe to measure $G_{d(closed\ loop)}$ is impossible!

AC analysis: Buck converter (closed-loop)



Measurement: $G_{d(\text{closed loop})} = V_o/d$ (Using "Add Curve") 77

AC analysis: Buck converter (closed-loop)



Measurement: $G_{d(\text{closed loop})} = V_o/d$ (Using "Add Curve") 78

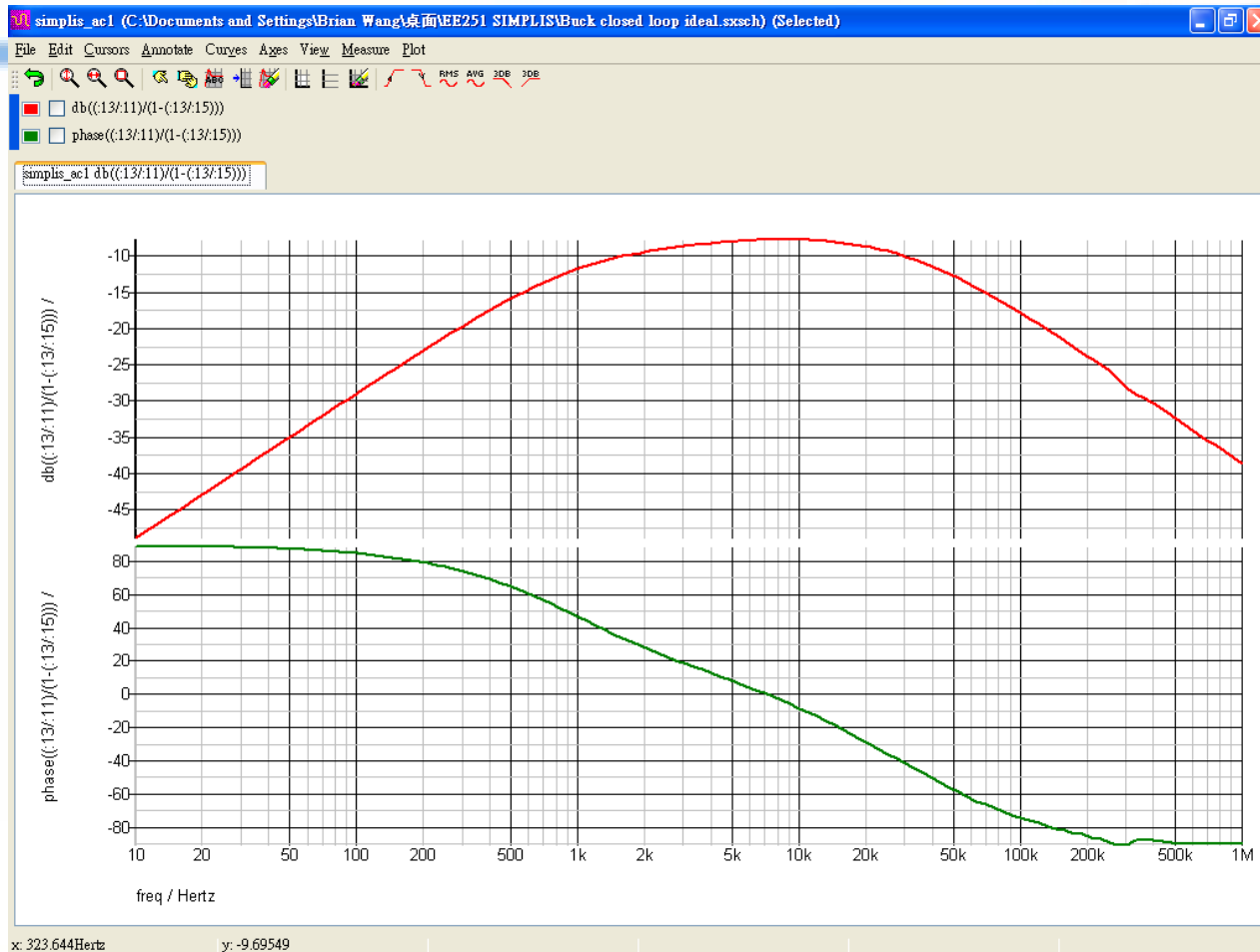
AC analysis: Buck converter (closed-loop)

$$\text{Gain}_{G_{d(\text{closed_loop})}} = \text{db}\left(\frac{G_{d(\text{open_loop})}}{1+T}\right) = \text{db}\left(\frac{(\angle 13/\angle 11)}{1 - (\angle 13/\angle 15)}\right)$$

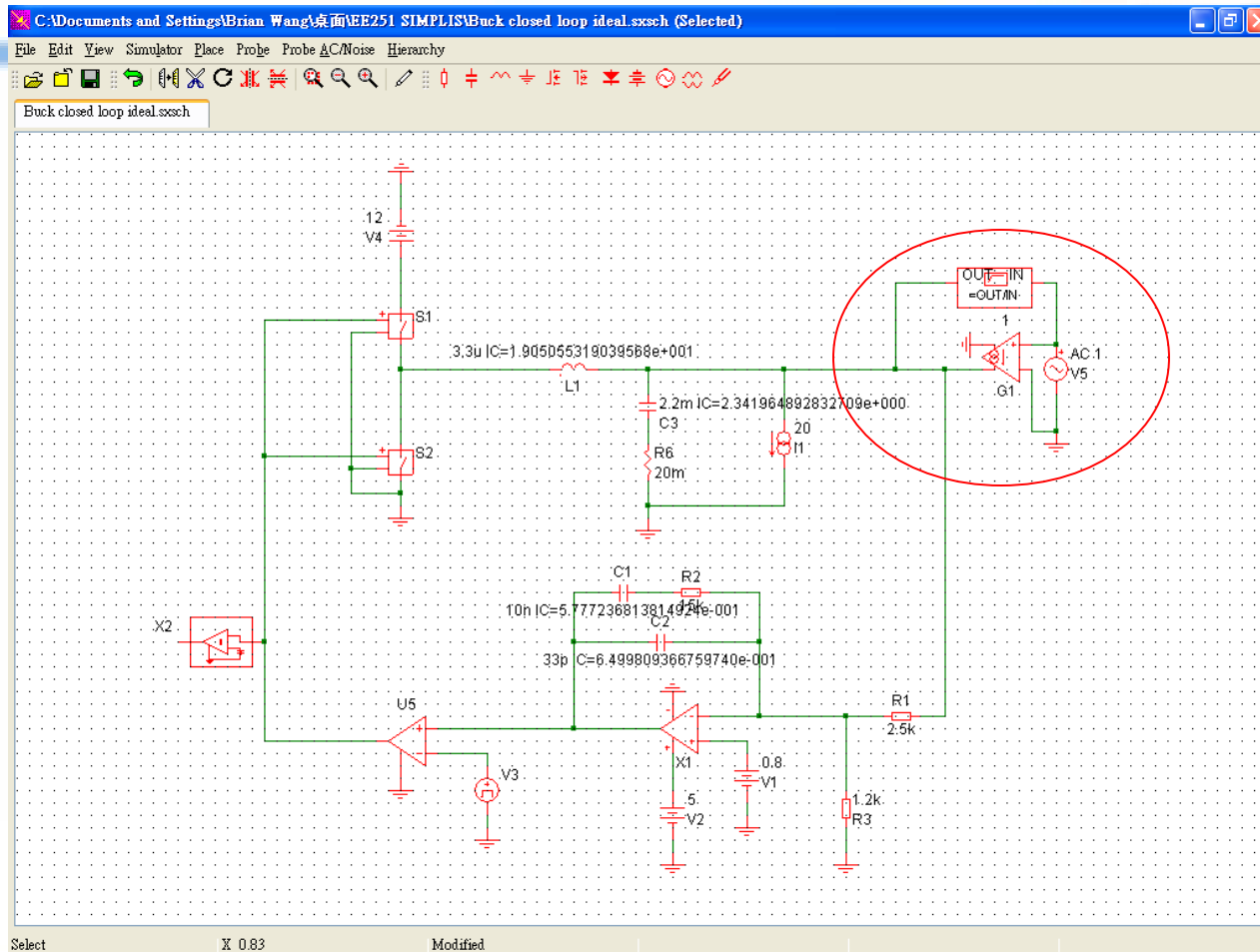
$$\text{Phase}_{G_{d(\text{closed_loop})}} = \text{phase}\left(\frac{G_{d(\text{open_loop})}}{1+T}\right) = \text{phase}\left(\frac{(\angle 13/\angle 11)}{1 - (\angle 13/\angle 15)}\right)$$

The denominator of $G_{d(\text{closed loop})}$ contains – signal because T contains negative feedback loop

AC analysis: Buck converter (closed-loop)

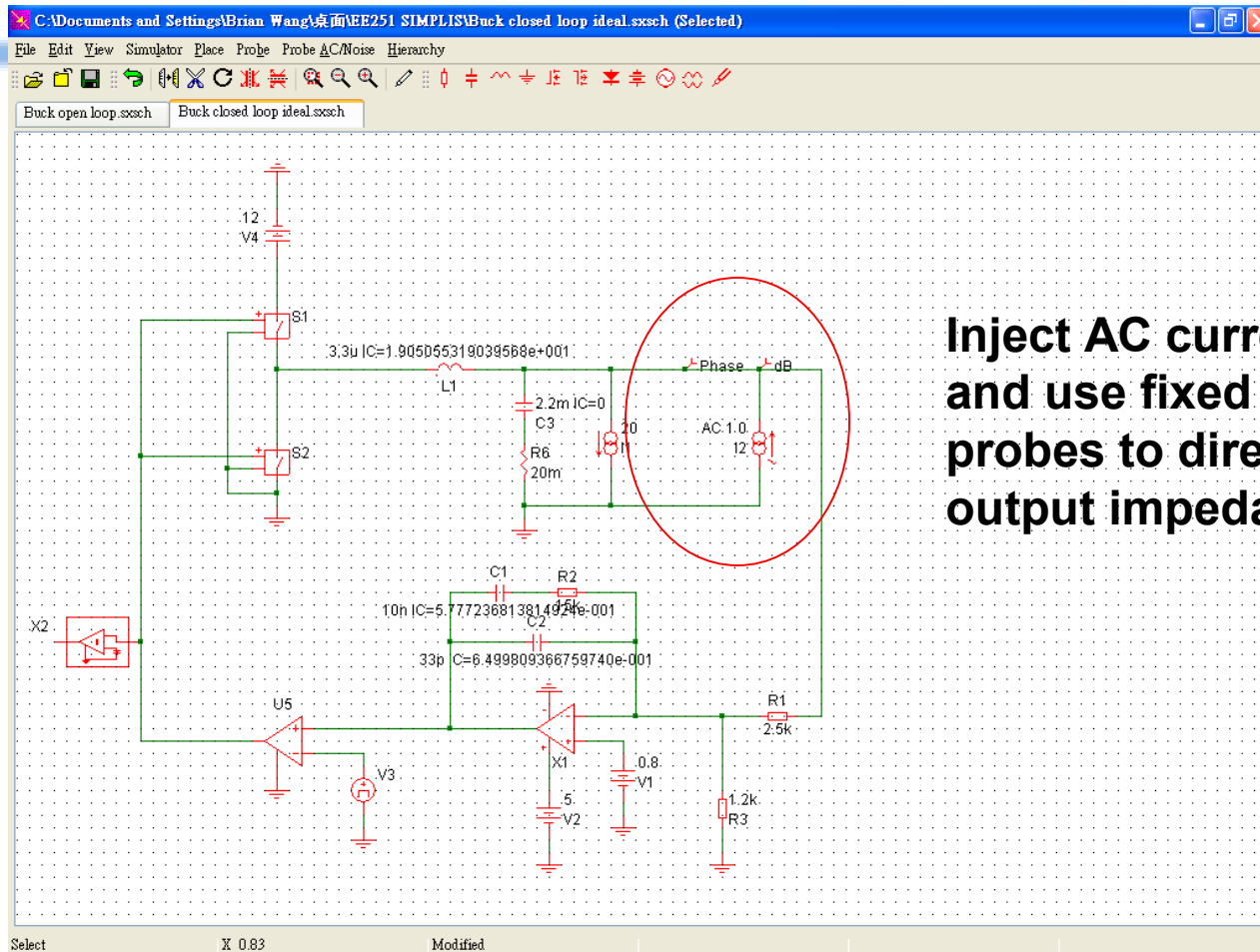


AC analysis: Buck converter (closed-loop)



Measurement: $Z_{p(\text{closed loop})} = V_o / i_o$ (Sub-circuit method) 81

AC analysis: Buck converter (closed-loop)



Inject AC current source and use fixed db and phase probes to directly measure output impedance

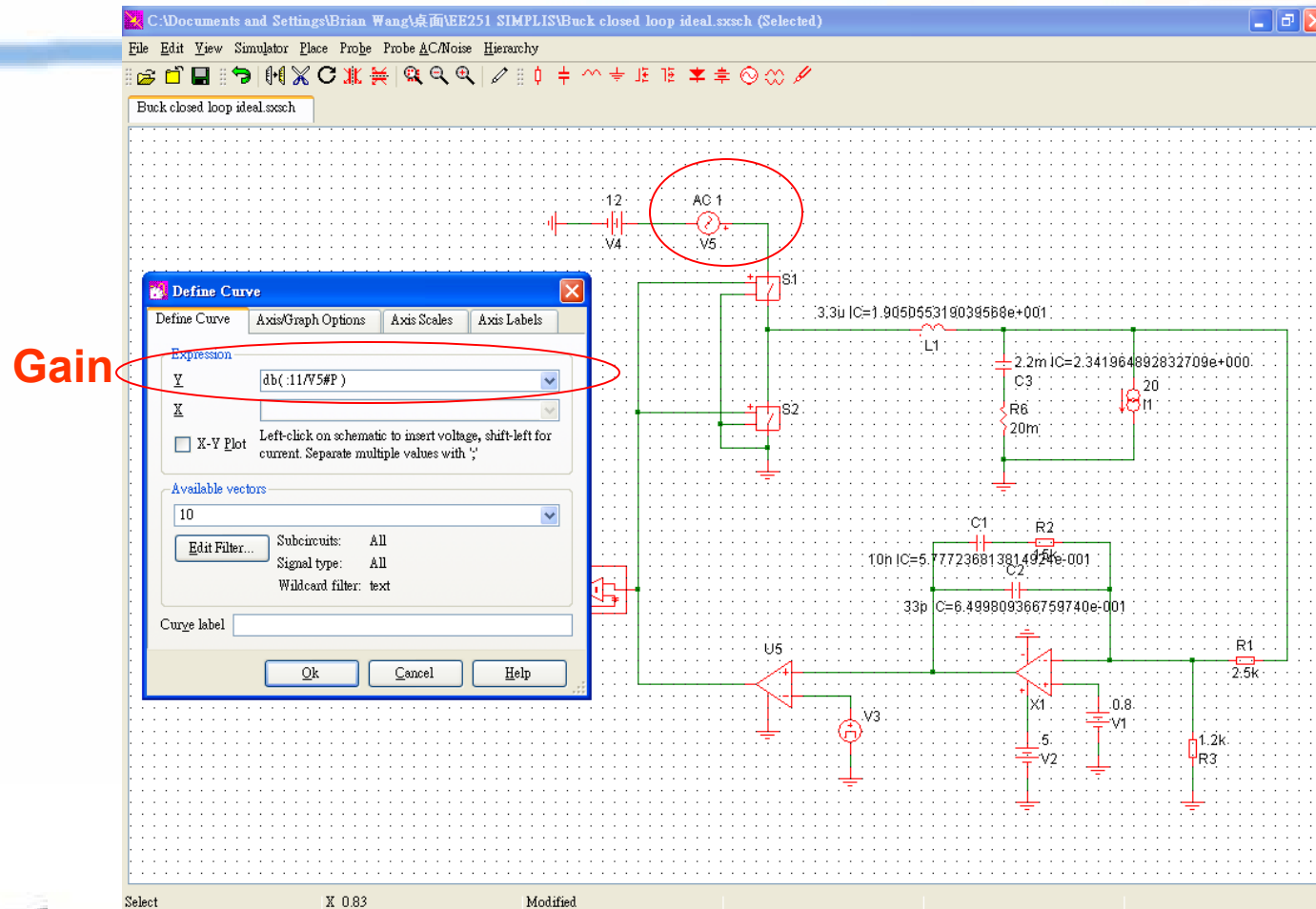
Measurement: $Z_{p(\text{closed loop})} = V_o / i_o$ (AC current source method)

AC analysis: Buck converter (closed-loop)



Bode plots of $Z_{p(\text{closed loop})} = V_o/i_o$

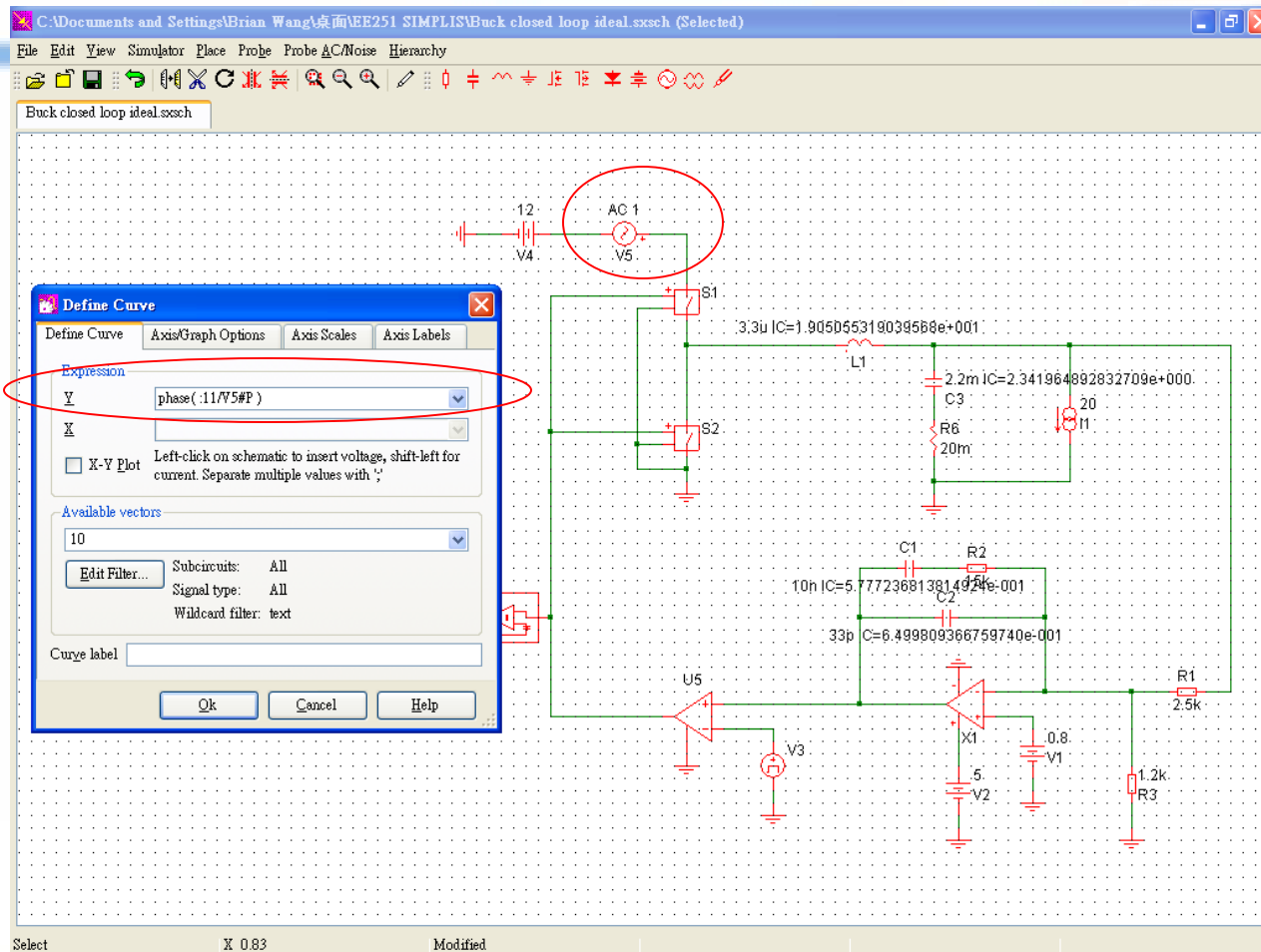
AC analysis: Buck converter (closed-loop)



Measurement: $Z_{\text{in(closed loop)}} = V_g / i_g$ (using "Add Curve")

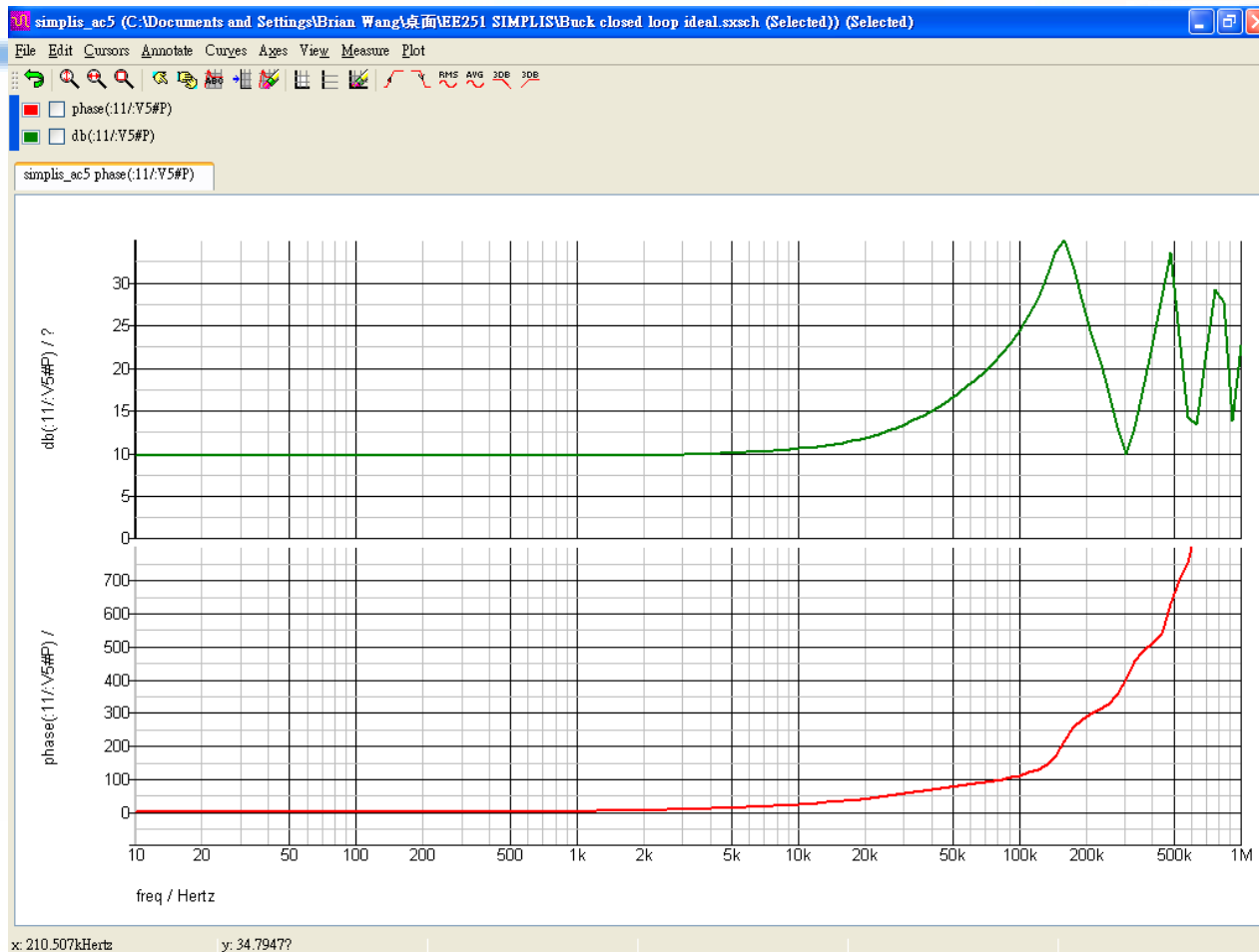
AC analysis: Buck converter (closed-loop)

Phase



Measurement: $Z_{in(closed\ loop)} = V_g / i_g$ (using "Add Curve")⁸⁵

AC analysis: Buck converter (closed-loop)



Code plots of $Z_{in(closed\ loop)} = V_g/i_g$

AC analysis verification: SIMPLIS v.s. Mathcad

$$\begin{aligned}
 \min &:= 10 & \max &:= 10^8 & r &:= \log\left[\frac{\max}{\min}\right] & n &:= 3000 & j &:= 0..n \\
 & & & & & & & & & j \frac{r}{n} \\
 f(j) &:= \min \cdot 10^{\frac{r}{n}} & w(j) &:= 2 \cdot \pi \cdot f(j) & s(j) &:= i \cdot w(j) \\
 V_g &:= 12 & V_o &:= 3 & L &:= 3.3 \cdot 10^{-6} & C &:= 2.2 \cdot 10^{-3} \\
 R &:= 0.15 & R_c &:= 20 \cdot 10^{-3} & D &:= 0.25 & D_x &:= 1 - D \\
 T_s &:= \frac{10 \cdot 10^{-6}}{3} & w_z &:= \frac{1}{R_c \cdot C} & w_o &:= \frac{1}{\sqrt{L \cdot C}} \\
 Q &:= \frac{1}{w_o} \cdot \frac{1}{\frac{L}{R} + C \cdot R_c}
 \end{aligned}$$

AC analysis verification: SIMPLIS v.s. Mathcad

$$R1 := 2.5 \cdot 10^3 \quad R2 := 15 \cdot 10^3 \quad C1 := 10 \cdot 10^{-9} \quad C2 := 33 \cdot 10^{-12}$$

$$wz1 := \frac{1}{R2 \cdot C1} \quad wp1 := \frac{C1 + C2}{R2 \cdot C1 \cdot C2} \quad wi := \frac{1}{R1 \cdot C1} \quad A(j) := \frac{wi}{s(j)} \cdot \frac{\left[1 + \frac{s(j)}{wz1} \right]}{\left[1 + \frac{s(j)}{wp1} \right]}$$

$$Gv(j) := D \cdot \frac{1 + \frac{s(j)}{wz}}{1 + \left[\frac{s(j)}{wo} \right]^2 + \frac{s(j)}{Q \cdot wo}}$$

$$Gd(j) := Vg \cdot \frac{1 + \frac{s(j)}{wz}}{1 + \frac{s(j)}{Q \cdot wo} + \left[\frac{s(j)}{wo} \right]^2}$$

$$Zp(j) := \frac{Rc}{wo^2} \cdot \frac{wz \cdot s(j) + s(j)^2}{1 + \frac{s(j)}{Q \cdot wo} + \left[\frac{s(j)}{wo} \right]^2}$$

$$Zin(j) := \left[\frac{R}{D^2} \right] \cdot \frac{1 + \frac{s(j)}{Q \cdot wo} + \frac{R + Rc}{R} \left[\frac{s(j)}{wo} \right]^2}{1 + C \cdot (Rc + R) \cdot s(j)}$$

AC analysis verification: SIMPLIS v.s. Mathcad

$$F_m := \frac{1}{2}$$

$$T(j) := G_d(j) \cdot F_m \cdot A(j)$$

$$G_{dc}(j) := \frac{G_d(j)}{1 + T(j)}$$

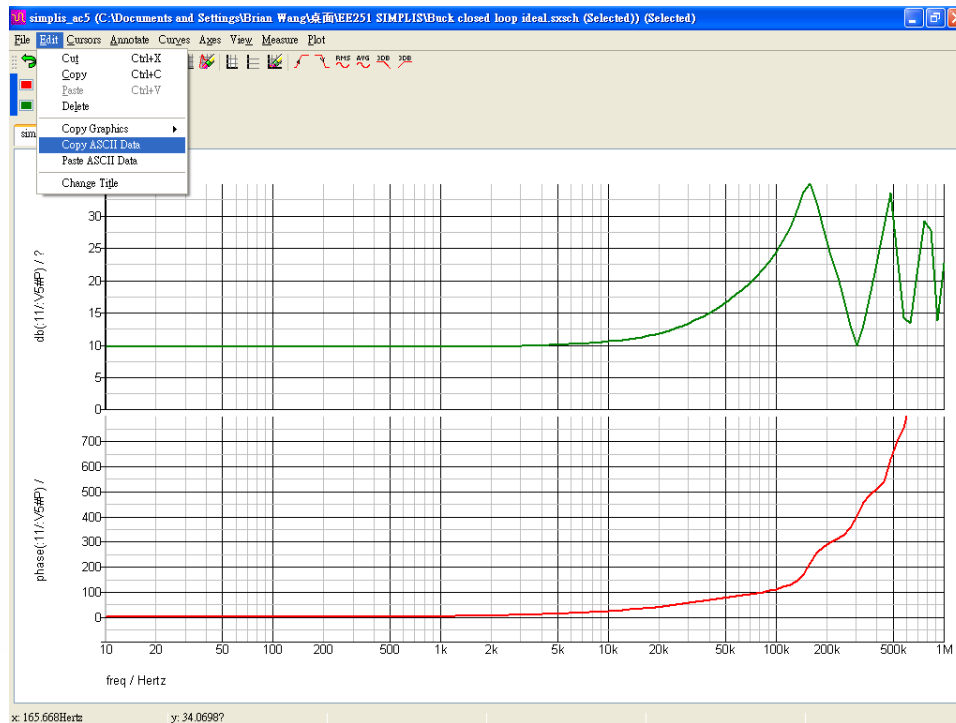
$$G_{vc}(j) := \frac{G_v(j)}{1 + T(j)}$$

$$Z_{pc}(j) := \frac{Z_p(j)}{1 + T(j)}$$

$$Z_{inc}(j) := \frac{1}{\frac{1}{Z_{in}(j) \cdot (1 + T(j))} - \frac{D^2}{R} \cdot \frac{T(j)}{1 + T(j)}}$$

□ **Reference about Z_{inc} :** Zamierczuk, M.K.; Cravens, R.C., II; Reatti, A. , “Close d-loop input impedance of PWM buck-derived DC-DC converters,” *Circuits and Systems*, 1994. ISCAS '94., 1993 IEEE International Symposium on Volume 6, 30 May-2 June 1994 Page(s):61 - 64 vol.6

AC analysis verification: SIMPLIS S v.s. Mathcad



Zinc.txt - 記事本

freq	Phase	Gain
10	-179.982727	9.753631518
10.96478196	-179.98106	9.753628029
12.02264435	-179.979232	9.753623834
13.18256739	-179.977228	9.75361879
14.45439771	-179.975031	9.753612727
15.84893192	-179.972621	9.753605439
17.37800829	-179.969978	9.753596677
19.05460718	-179.96708	9.753586144
20.89296131	-179.963902	9.753573483
22.90867653	-179.960417	9.753558265
25.11886432	-179.956594	9.753539972
27.54228703	-179.952402	9.753517985
30.1995172	-179.947804	9.753491559
33.11311215	-179.94276	9.753459802
36.30780548	-179.937227	9.753421639
39.81071706	-179.931157	9.753375783
43.65158322	-179.924497	9.753320691
47.86300923	-179.917188	9.753254511
52.48074602	-179.909167	9.753175024
57.54399373	-179.900361	9.753079575
63.09573445	-179.890693	9.752964985
69.18309709	-179.880075	9.752827457
75.8577575	-179.868409	9.752662456
83.17637711	-179.855588	9.752464578
91.20108394	-179.841491	9.752227391
100	-179.825981	9.751943258
109.6478196	-179.808907	9.751603136

SIMPLIS: Copy curves' ASCII data and save to a txt file

AC analysis verification: SIMPLIS v.s. Mathcad

Zinc.txt - 記事本

Freq	Phase	Gain
10	-179.982727	9.753631518
10.96478196	-179.98106	9.753628029
12.02264435	-179.979232	9.753623834
13.18256739	-179.977228	9.75361879
14.45439771	-179.975031	9.753612727
15.84893192	-179.972621	9.753605439
17.37800829	-179.969978	9.753596677
19.05460718	-179.96708	9.753586144
20.89296131	-179.963902	9.753573483
22.90867653	-179.960417	9.753558265
25.11886432	-179.956594	9.753539972
27.54228703	-179.952402	9.753517985
30.1995172	-179.947804	9.753491559
33.11311215	-179.94276	9.753459802
36.30780548	-179.937227	9.753421639
39.81071706	-179.931157	9.753375783
43.65158322	-179.924497	9.753320691
47.86300923	-179.917188	9.753254511
52.48074602	-179.909167	9.753175024
57.54399373	-179.900361	9.753079575
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69.18309709	-179.880075	9.752827457
75.8577575	-179.868409	9.752662456
83.17637711	-179.855588	9.752464578
91.20108394	-179.841491	9.752227391
100	-179.825981	9.751943258
109.6478196	-179.808907	9.751603136

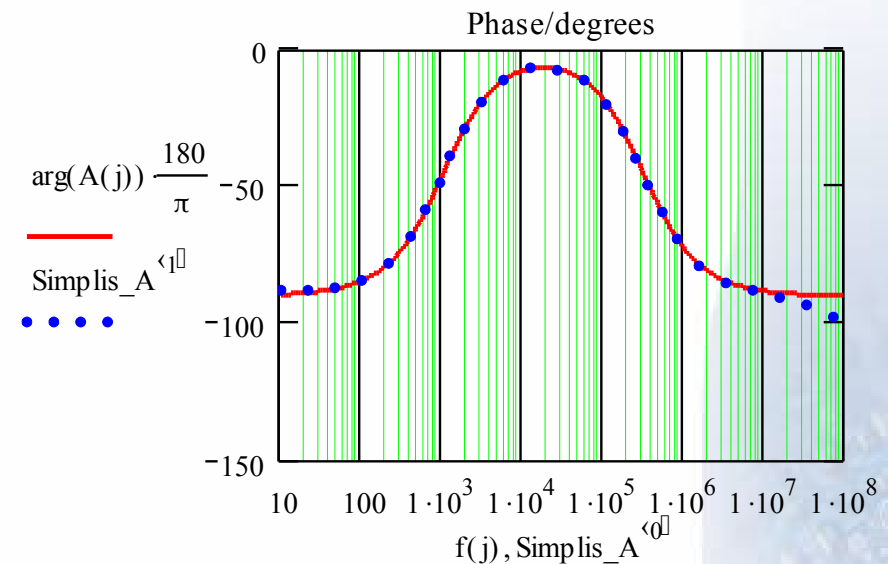
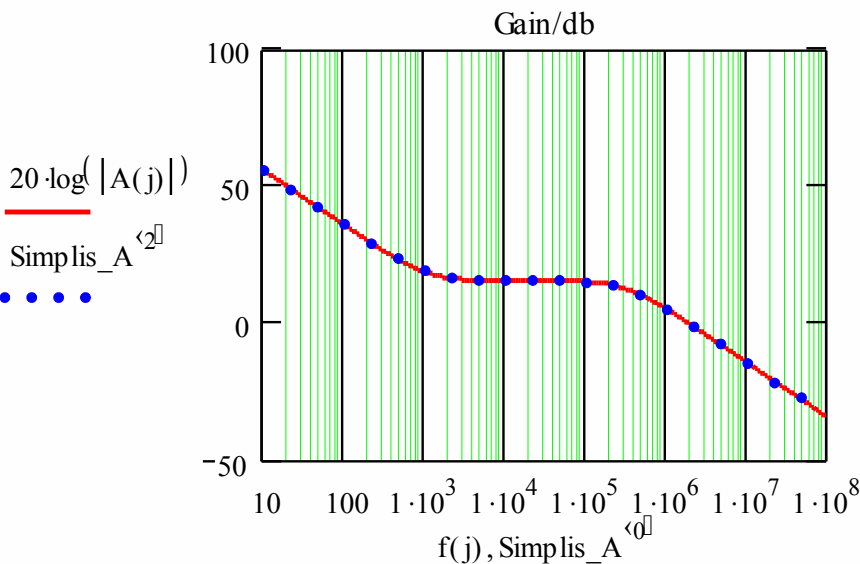


Simplis_Zinc :=
C:\Zinc.txt

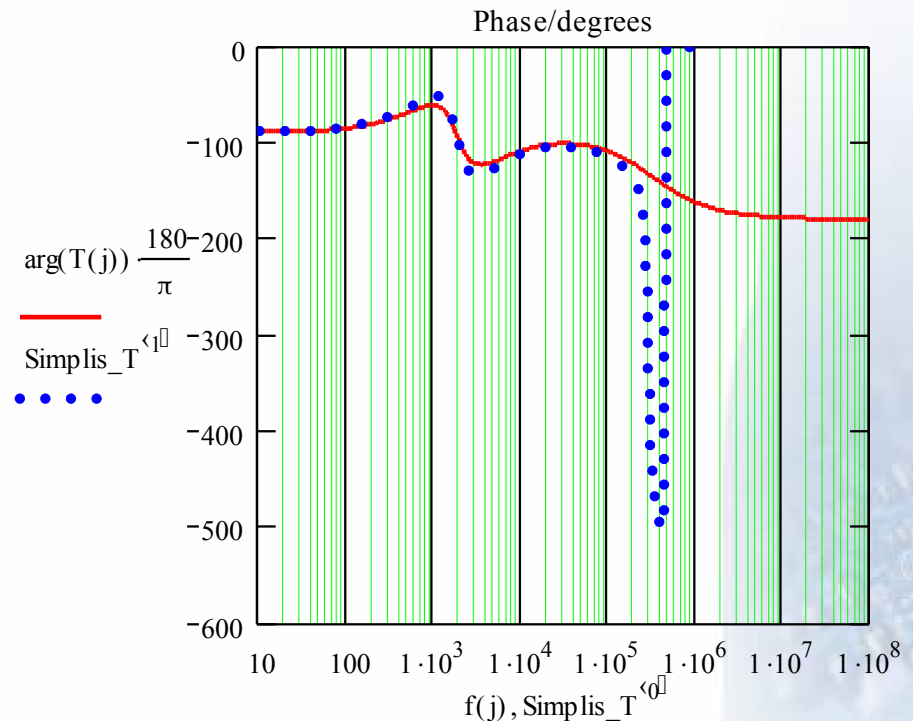
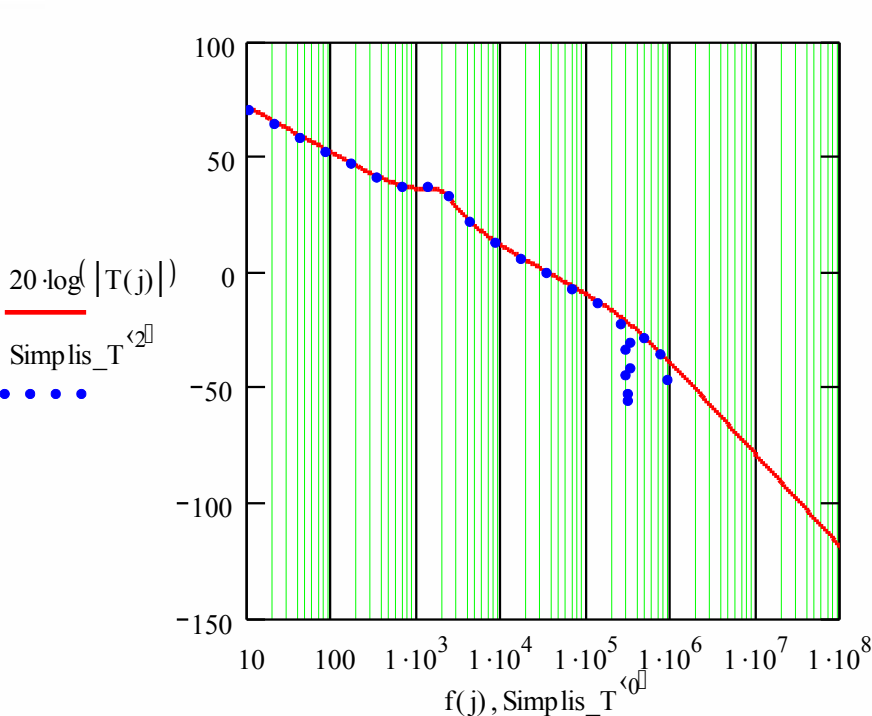
(In Mathcad)

Mathcad: Insert the saved SIMPLIS ASCII data file

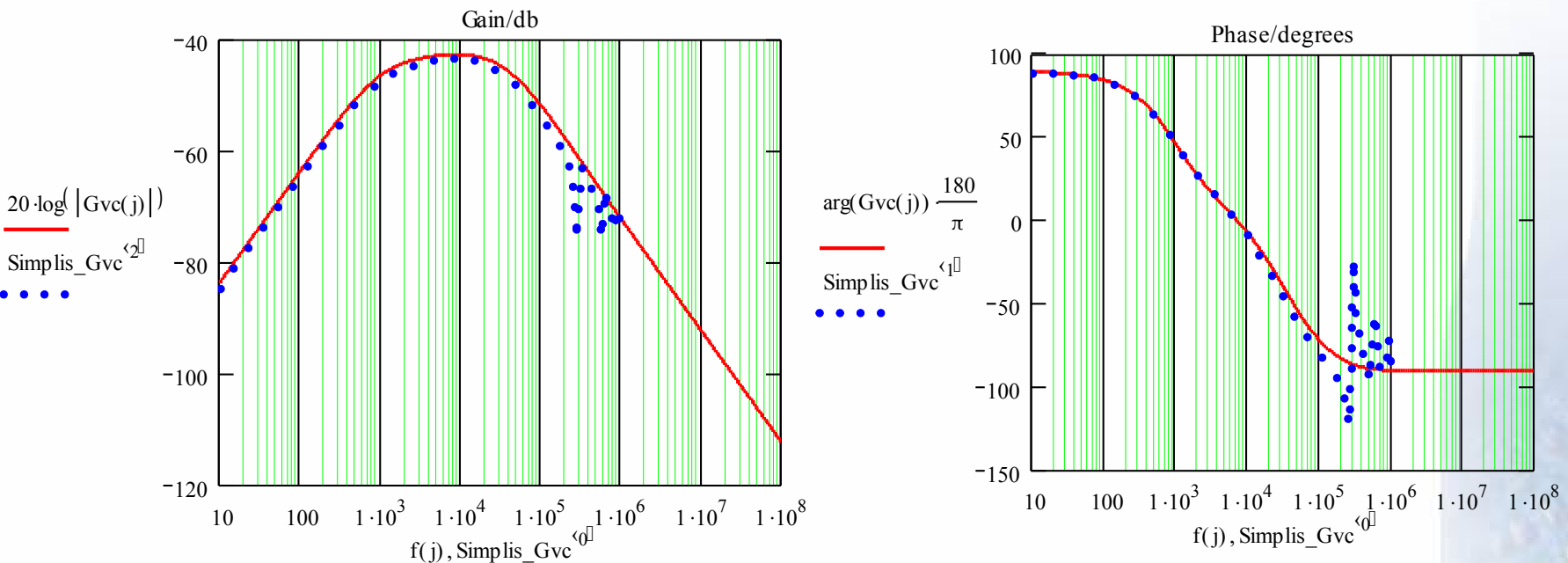
AC analysis verification: SIMPLIS S v.s. Mathcad



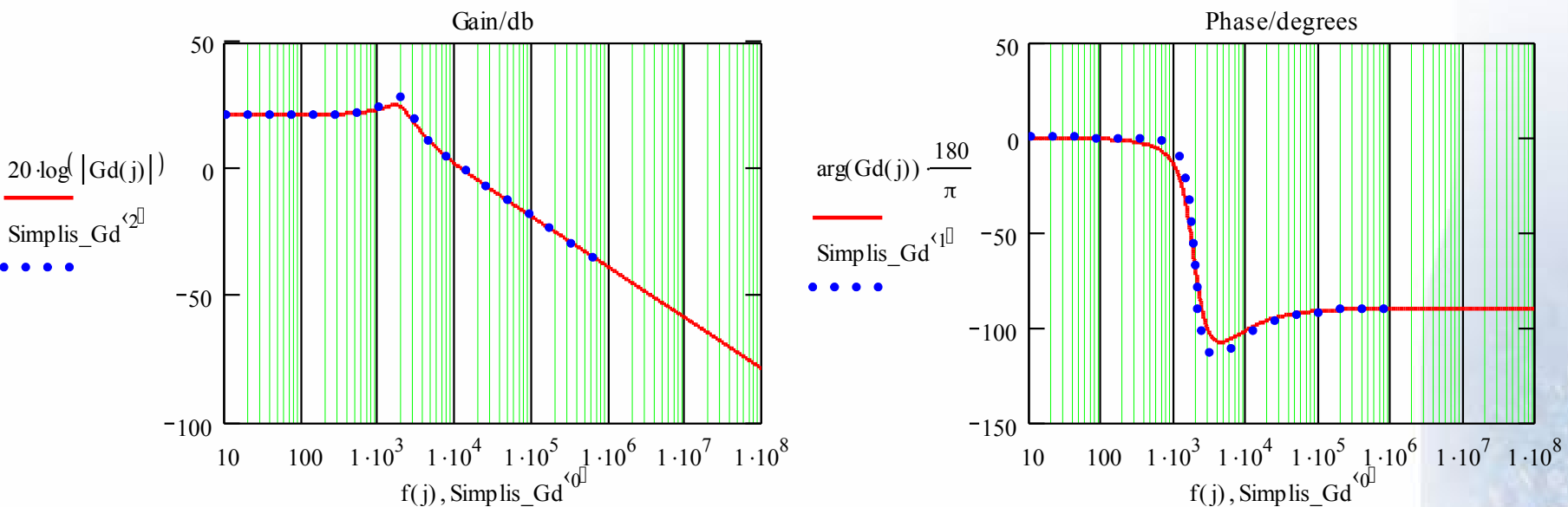
AC analysis verification: SIMPLIS v.s. Mathcad



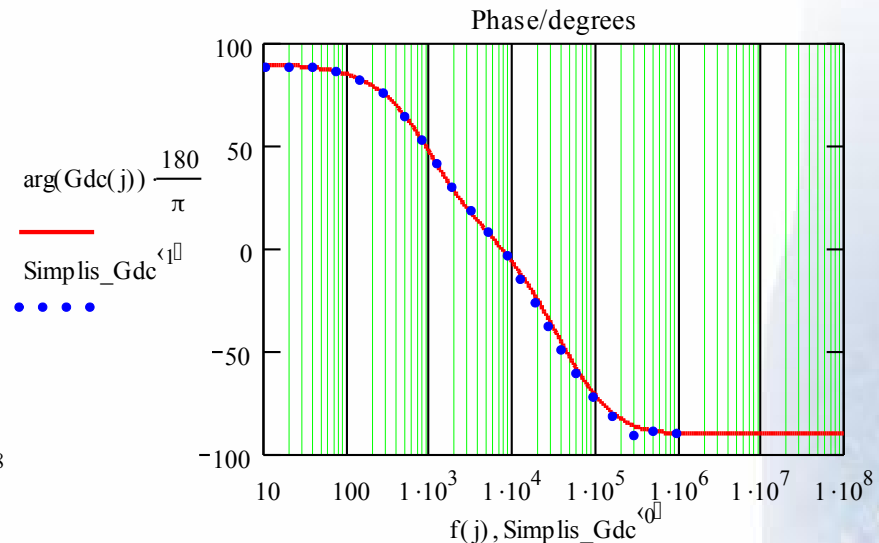
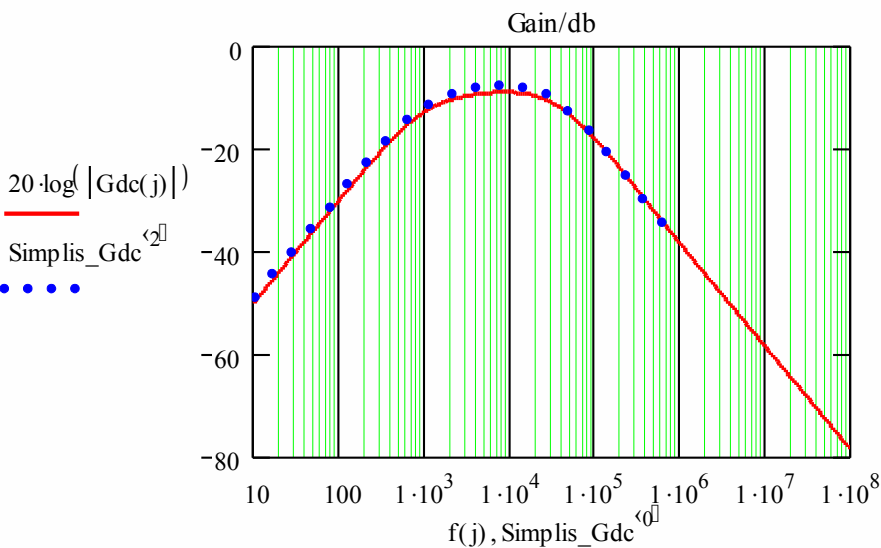
AC analysis verification: SIMPLIS S v.s. Mathcad



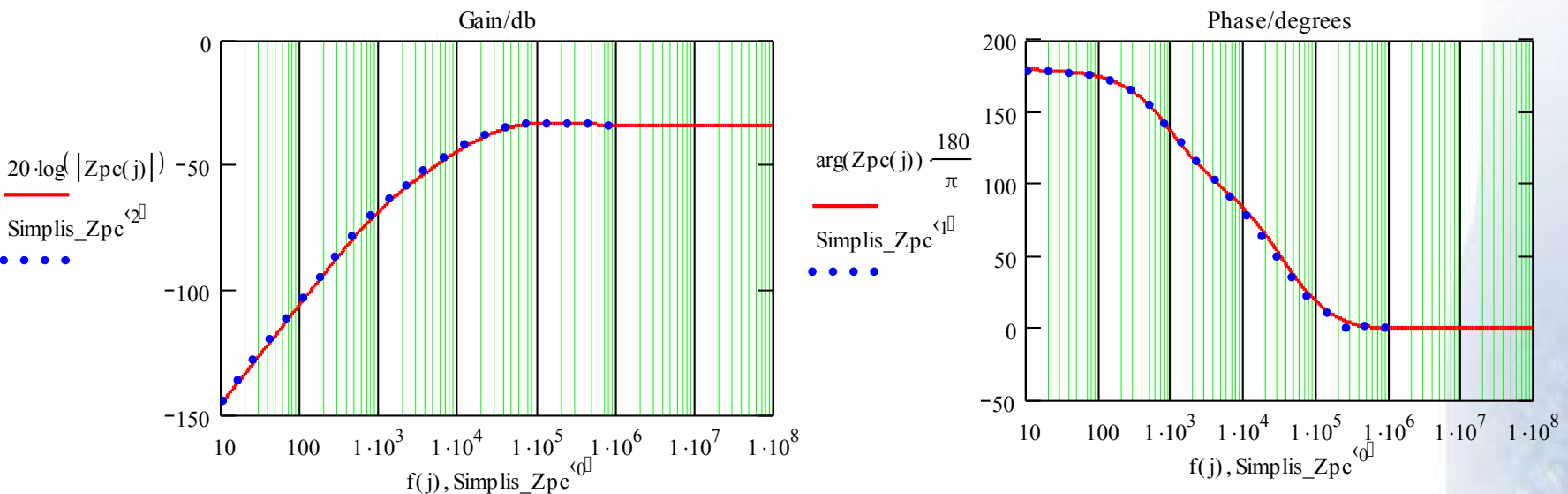
AC analysis verification: SIMPLIS S v.s. Mathcad



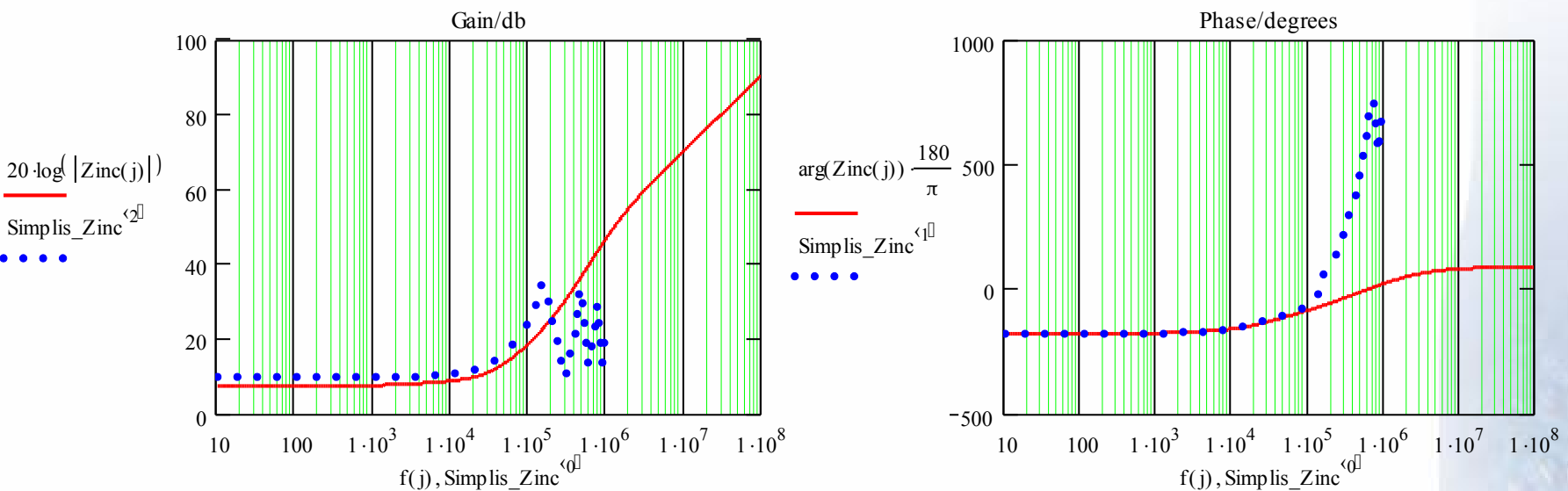
AC analysis verification: SIMPLIS S v.s. Mathcad



AC analysis verification: SIMPLIS v.s. Mathcad

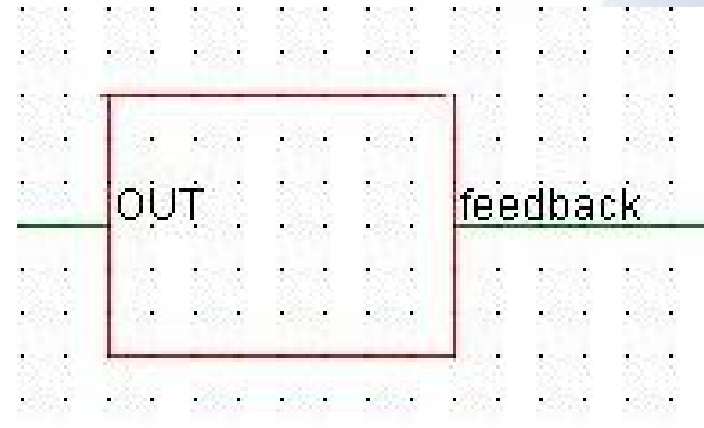
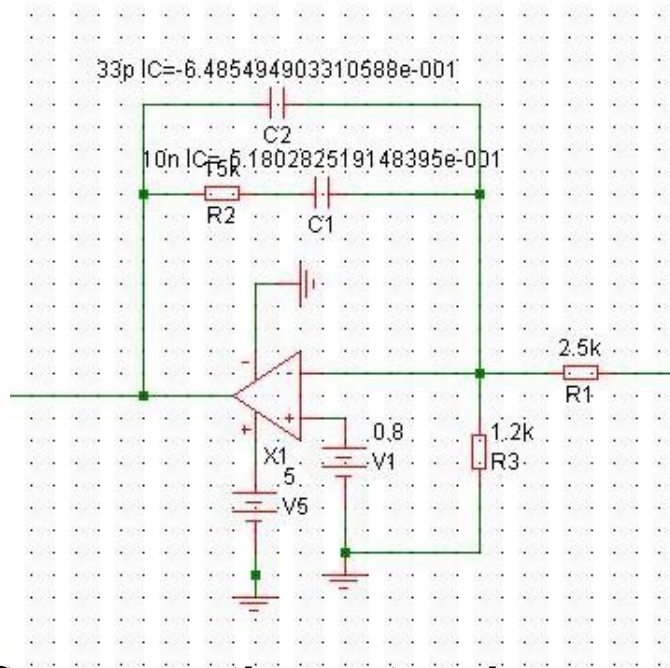


AC analysis verification: SIMPLIS v.s. Mathcad



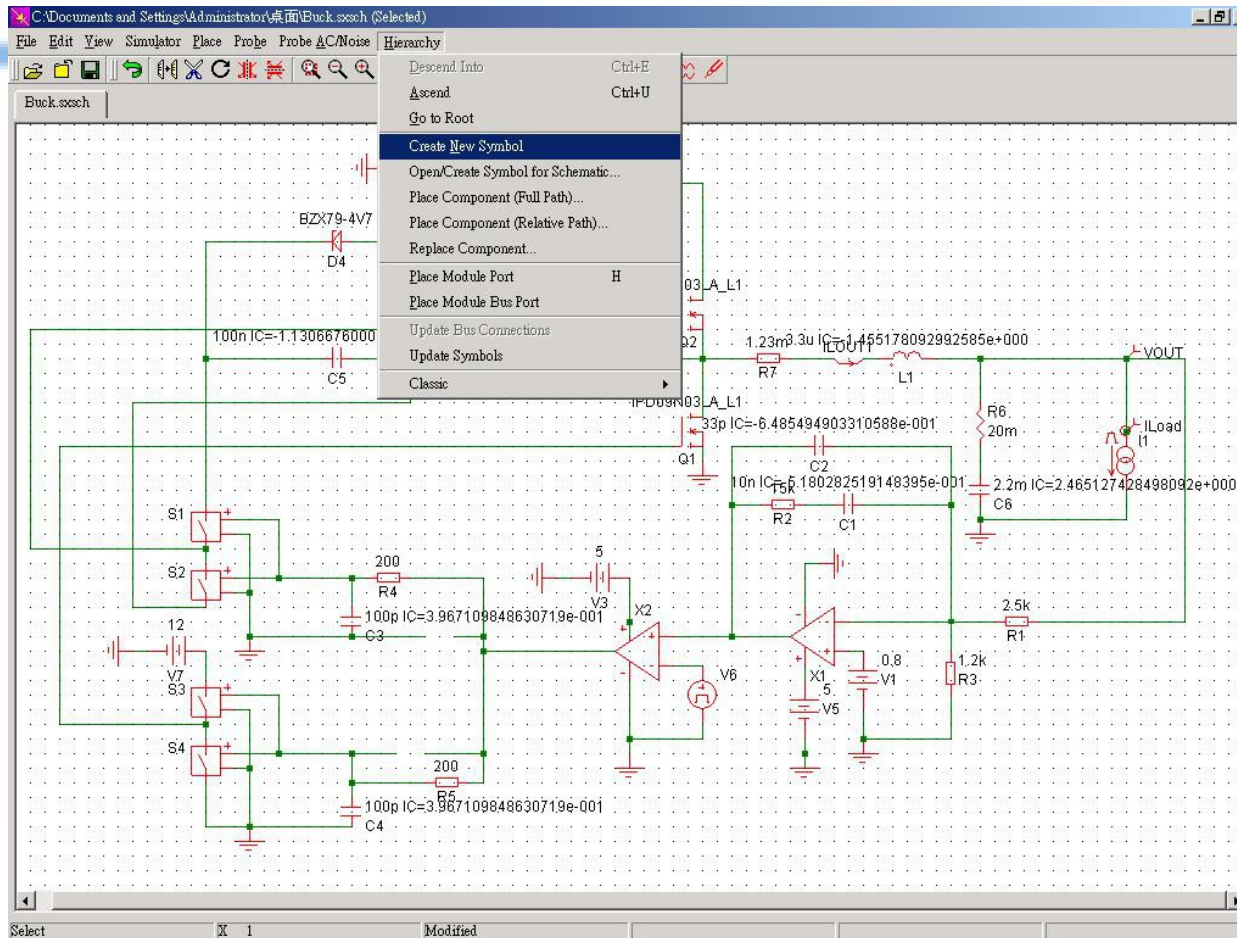
Create Hierarchy

- In SIMPLIS, we can create a small block which equals to a sub-circuit of the main circuit.

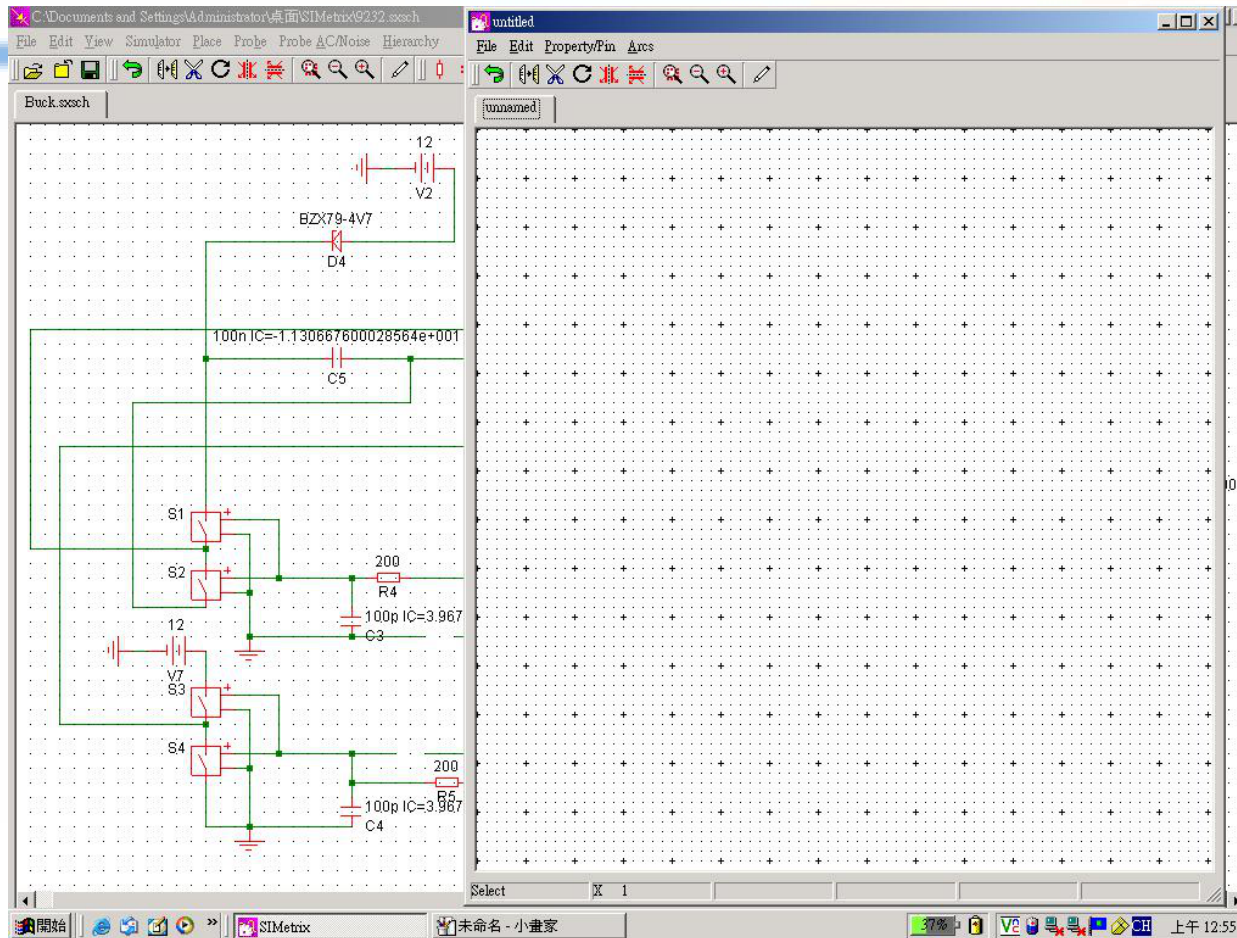


**Compensation network
sub-circuit**

Create Hierarchy

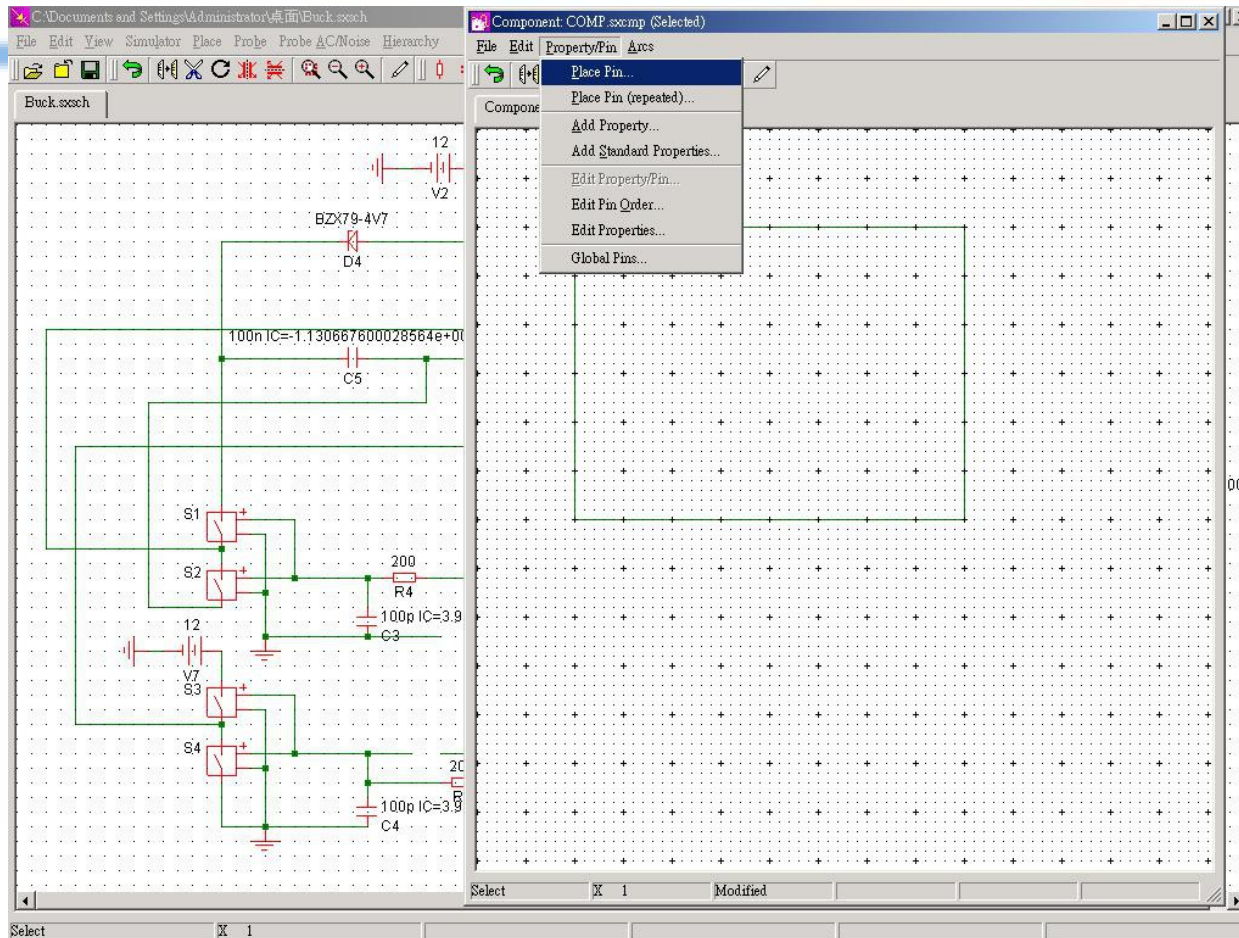


Create Hierarchy

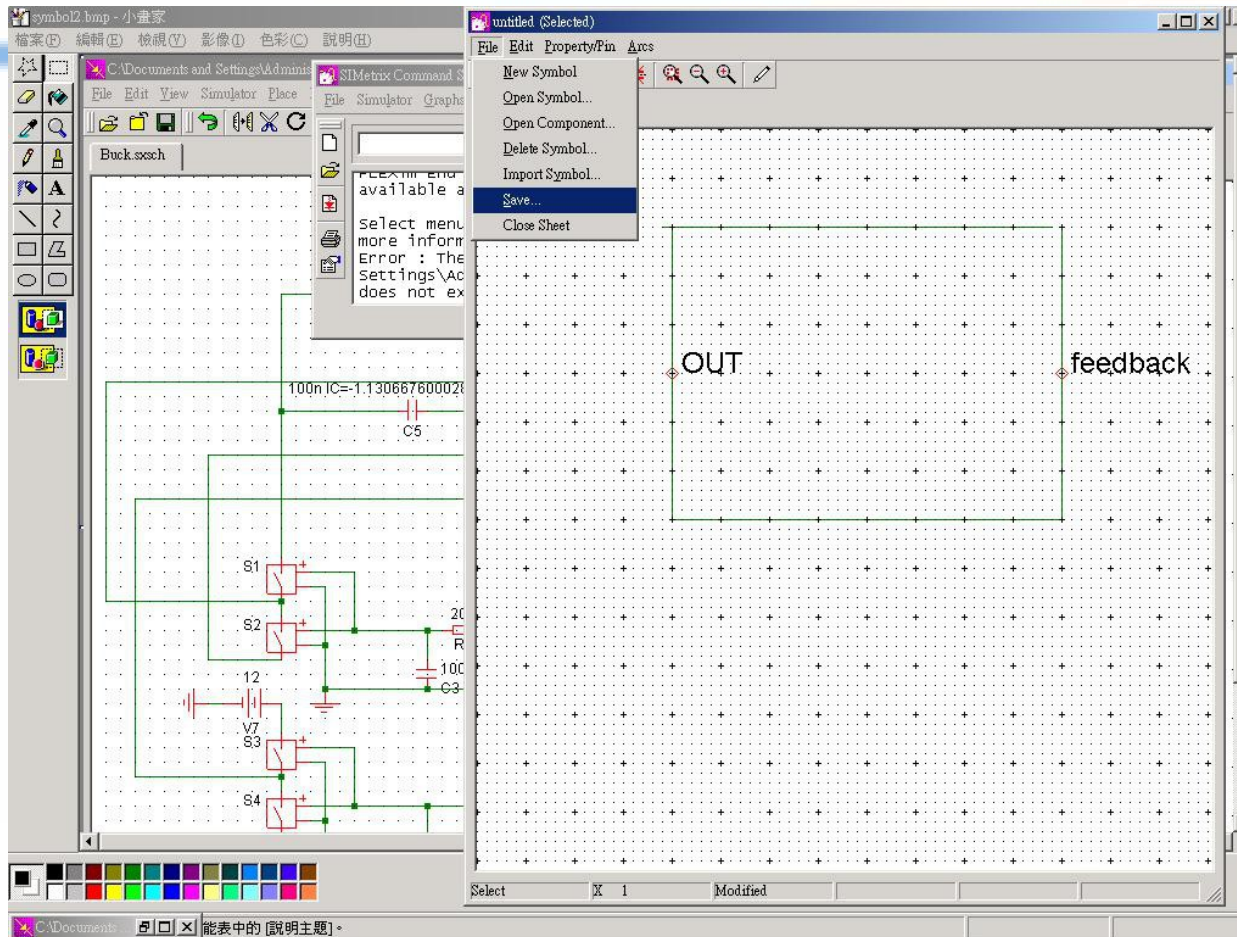


Draw a block on the blank sheet

Create Hierarchy

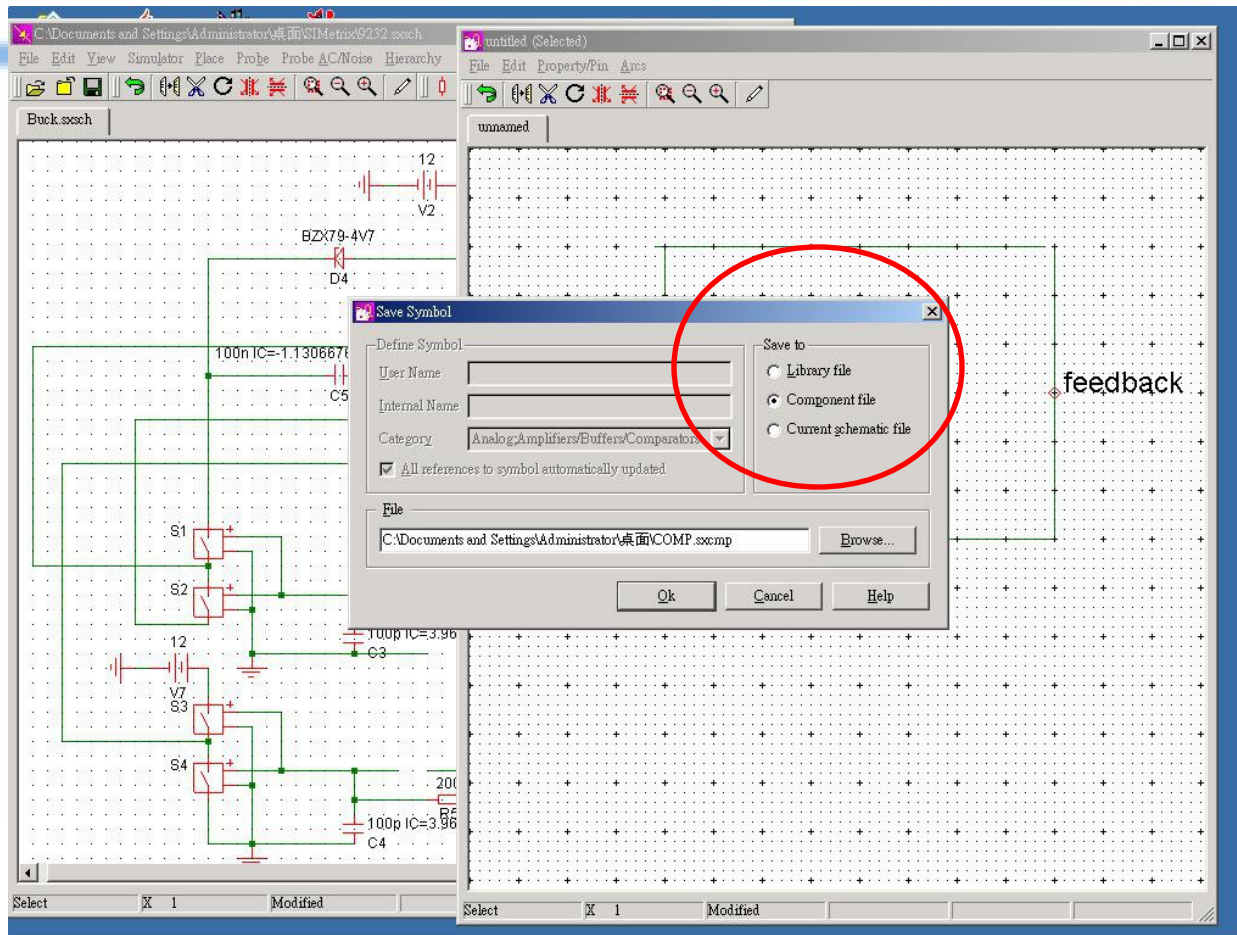


Create Hierarchy



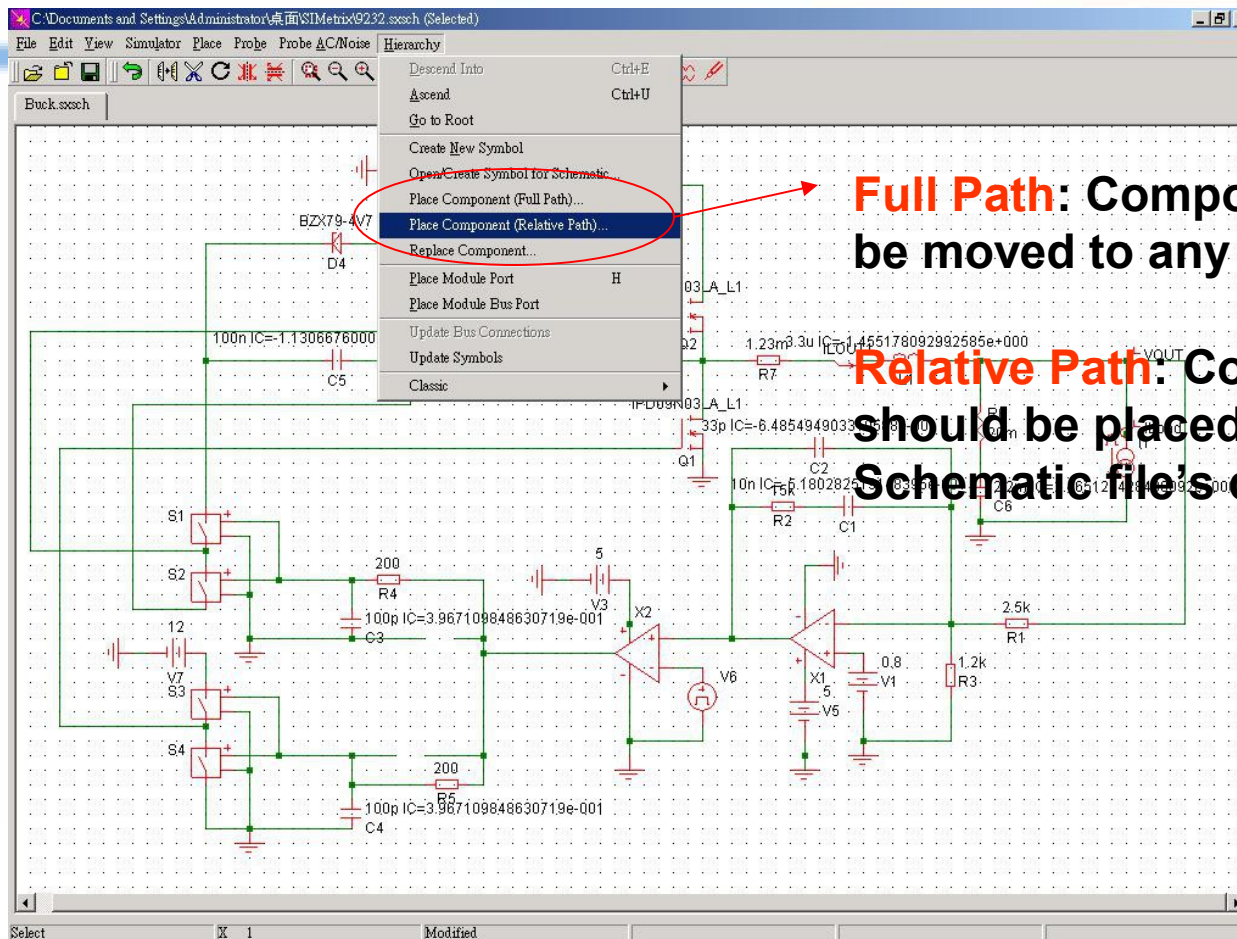
Save the drawn block for future use

Create Hierarchy



Save settings: Choose “Component file”

Create Hierarchy

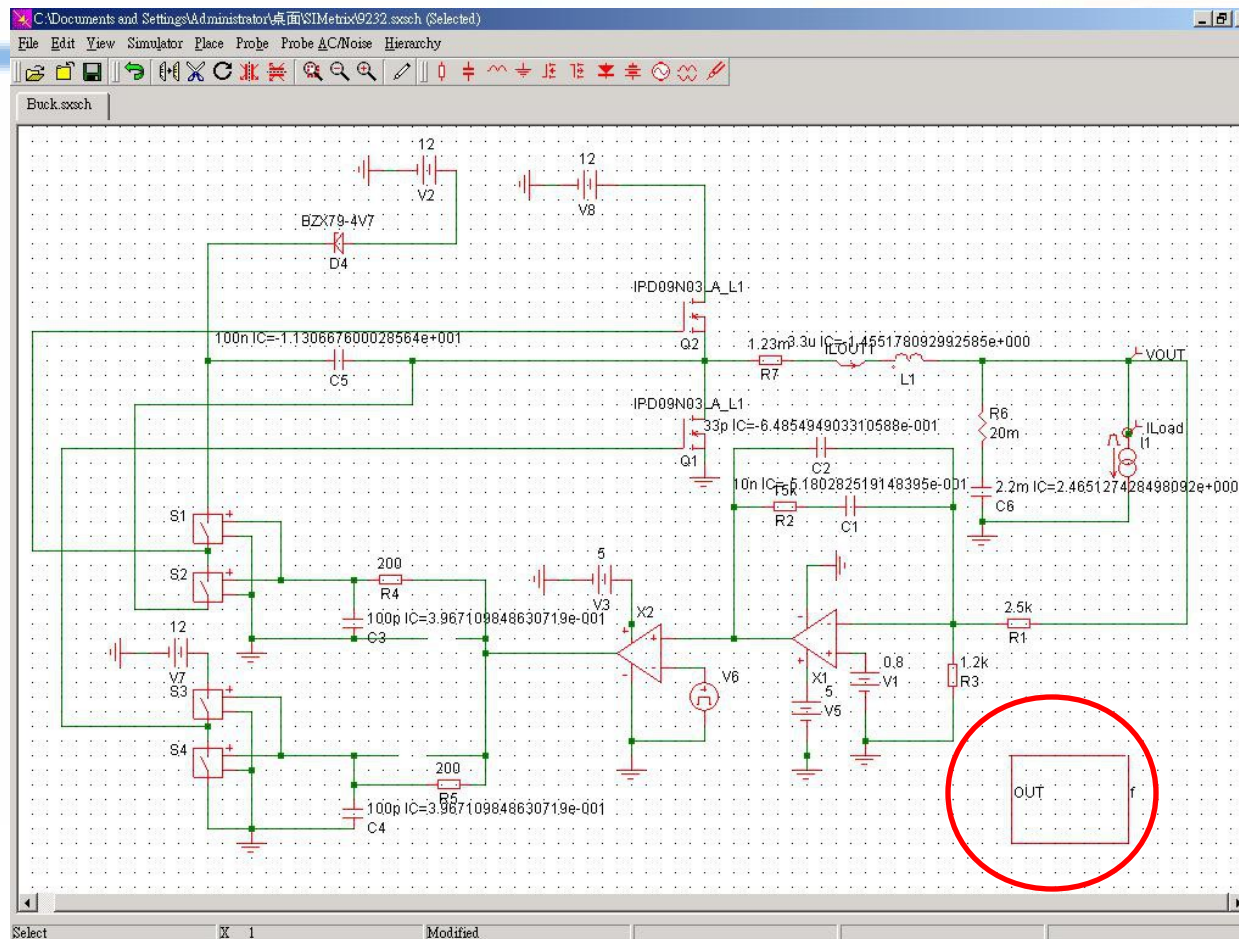


Full Path: Component file can be moved to any directory

Relative Path: Component file should be placed in the Schematic file's directory

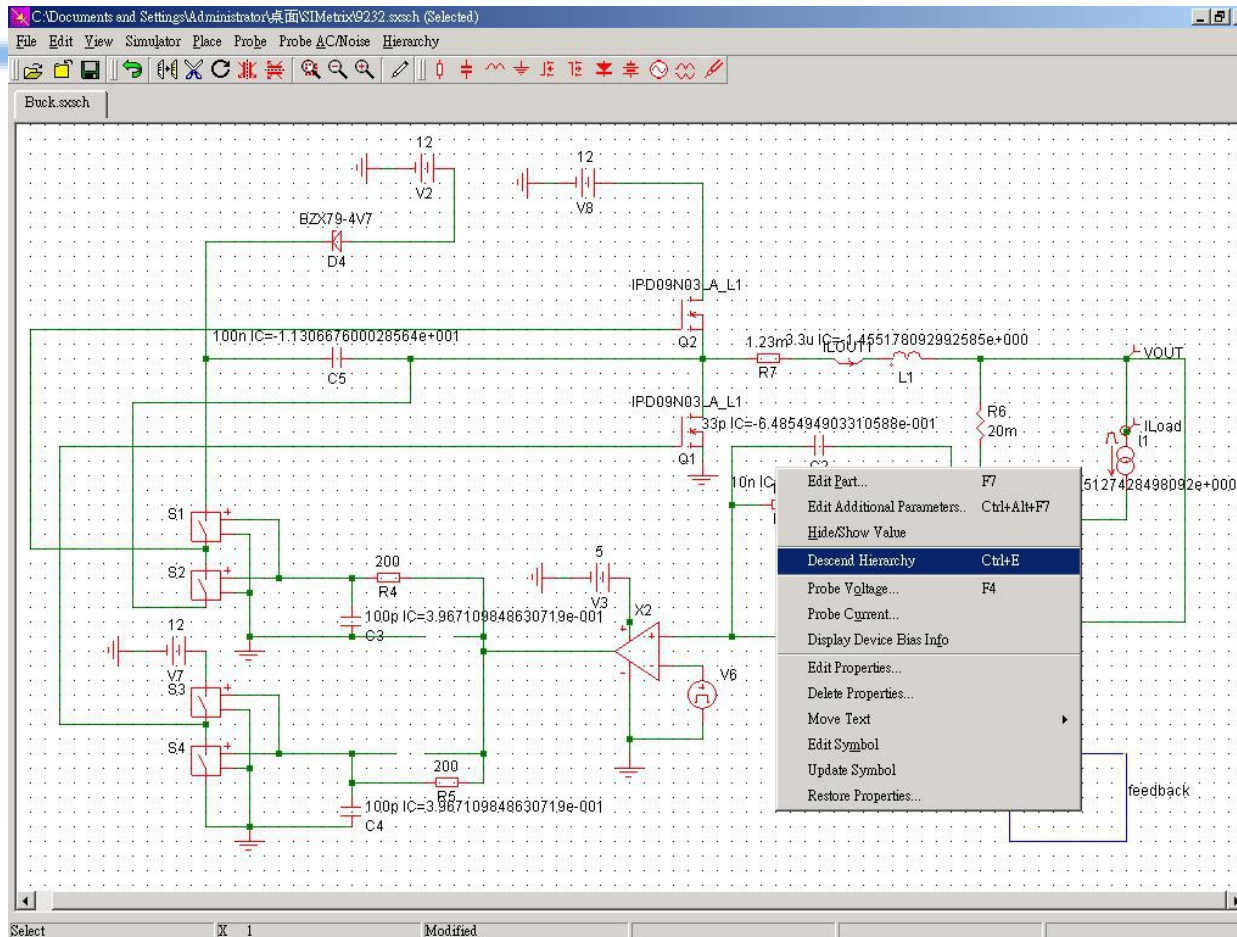
Place the drawn block into the main circuit

Create Hierarchy

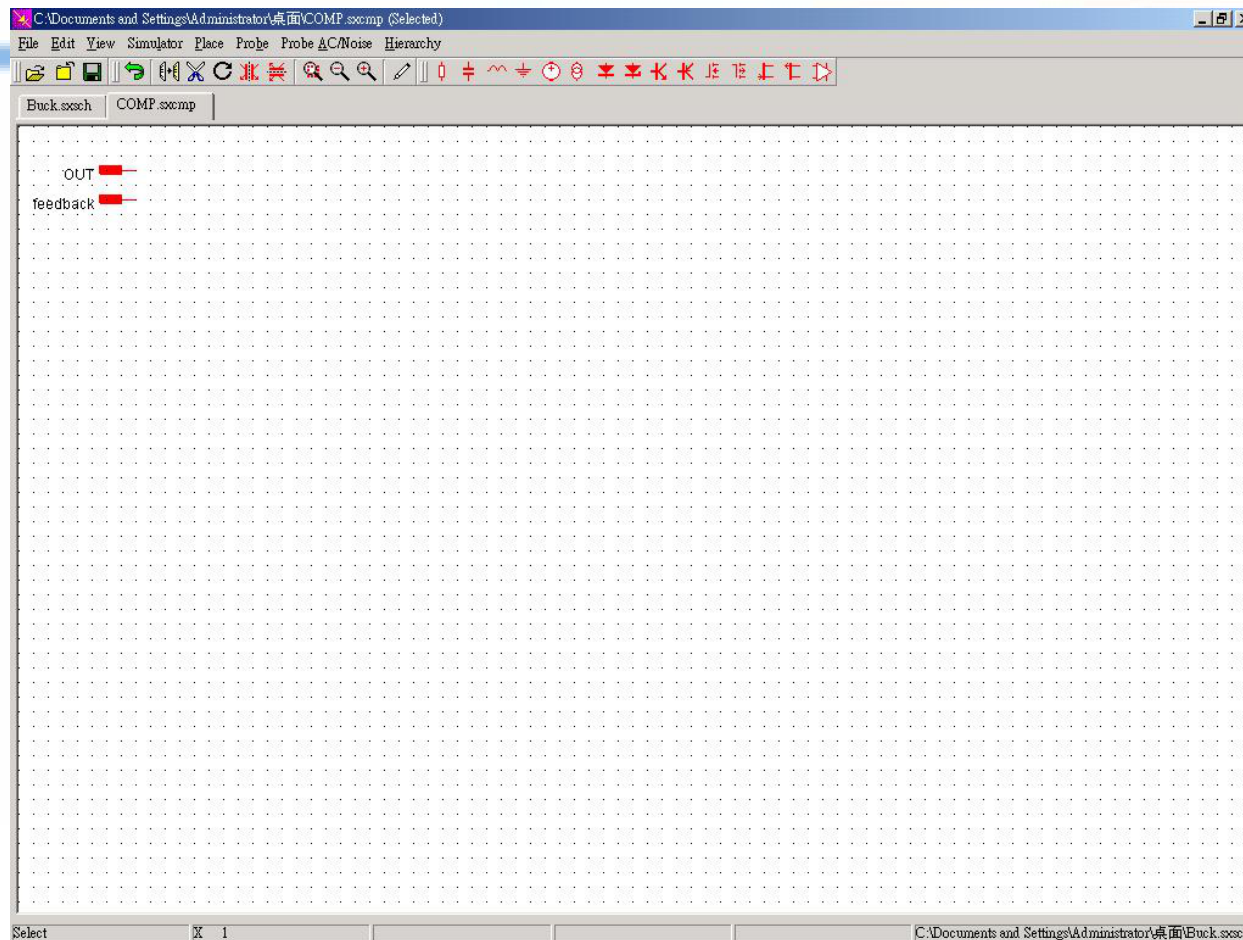


Place the drawn block into the main circuit

Create Hierarchy

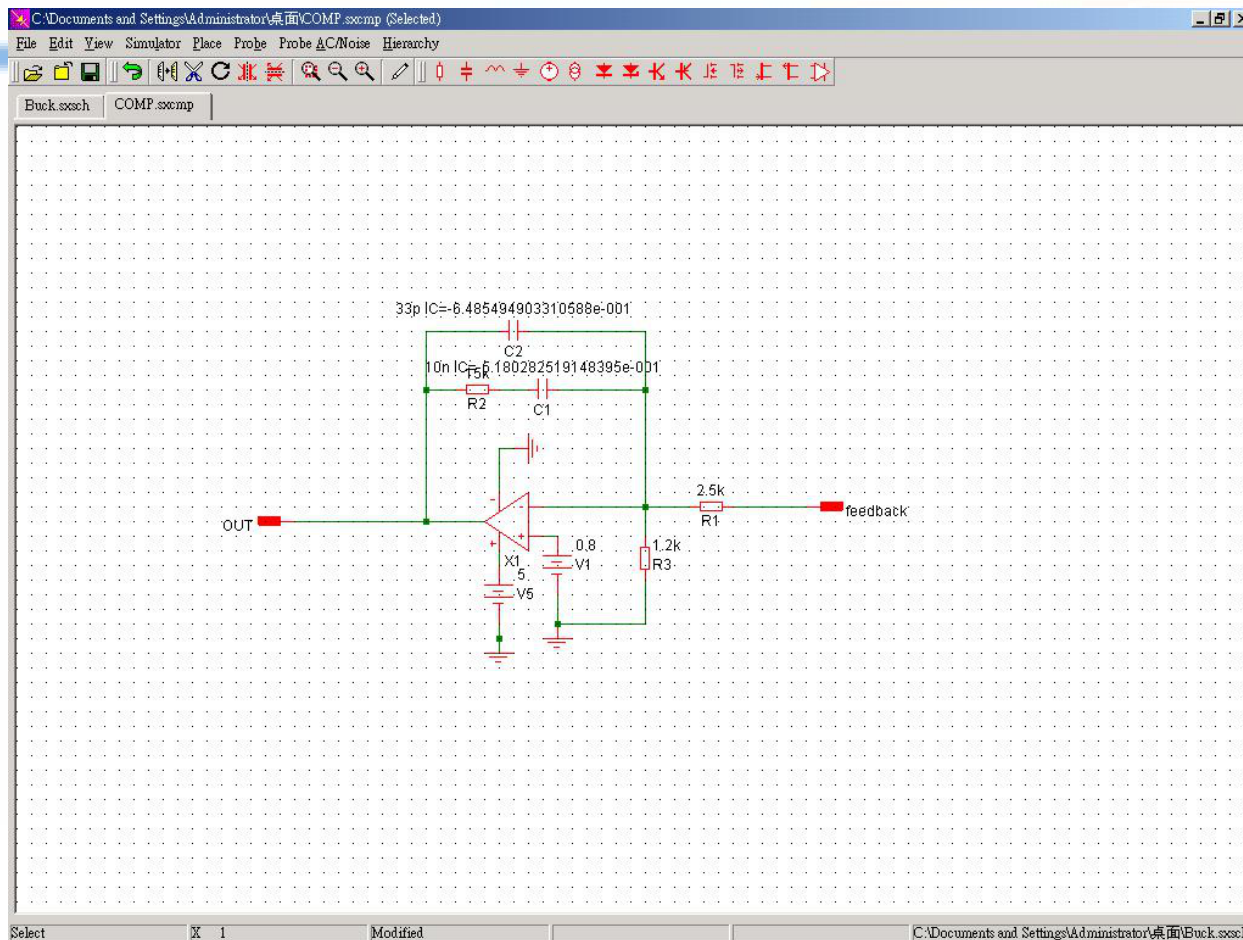


Create Hierarchy



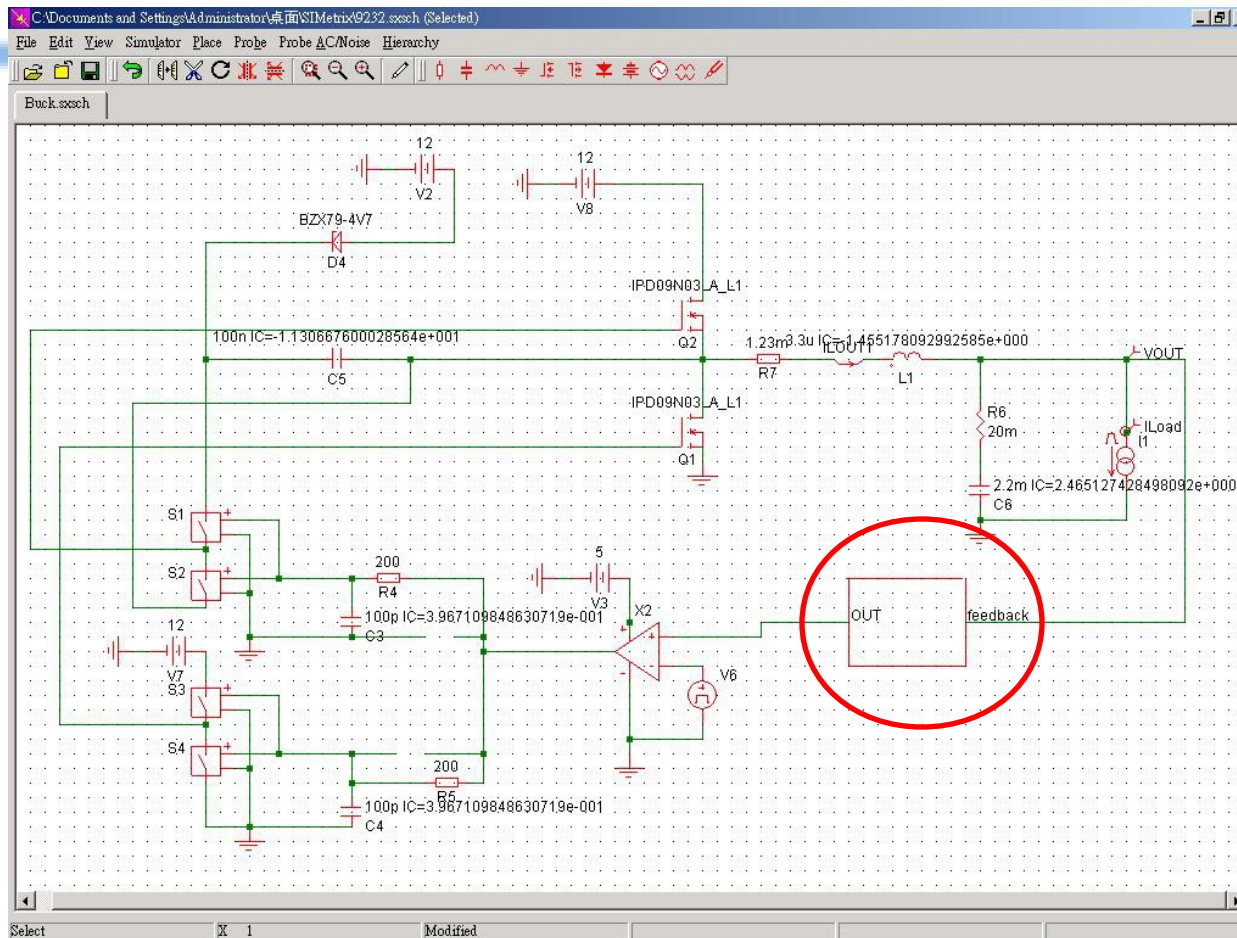
Edit the sub-circuit into the drawn block

Create Hierarchy



Copy and save the desired sub-circuit into the block

Create Hierarchy



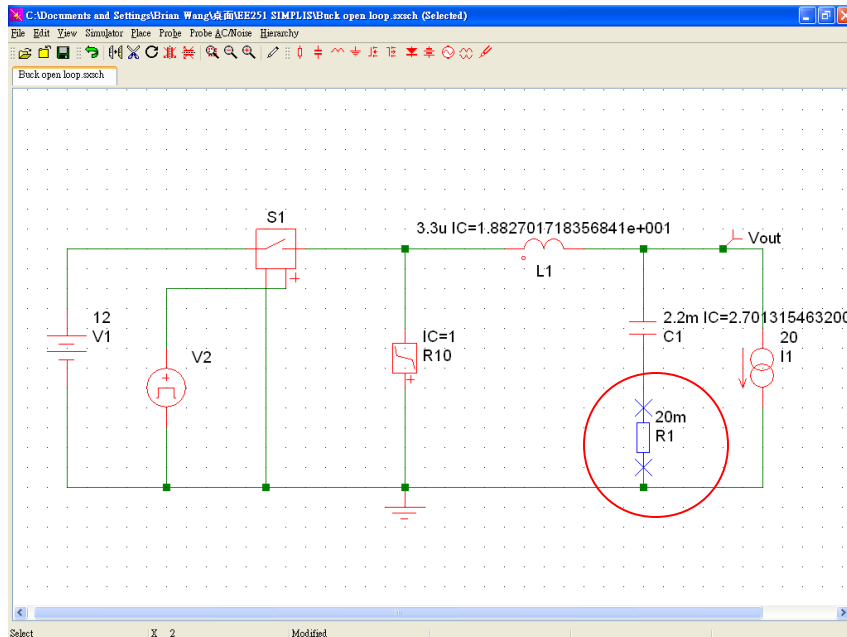
Compensation network replaced

Advanced Simulation Types

- **Monte-Carlo simulation**: a repeating simulation runs with random variables to component parameters
- **Multi-step simulation**: a repeating simulation runs while setting equal distributed parameters of the component

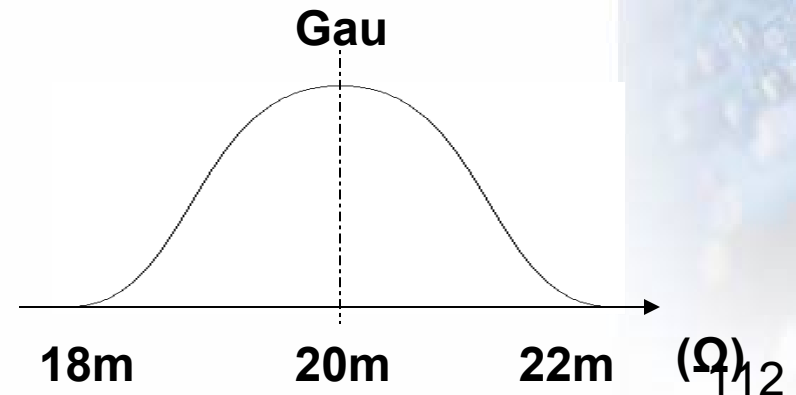
Monte-Carlo Simulation

- **Monte-Carlo example: Select Cap's ESR to observe**

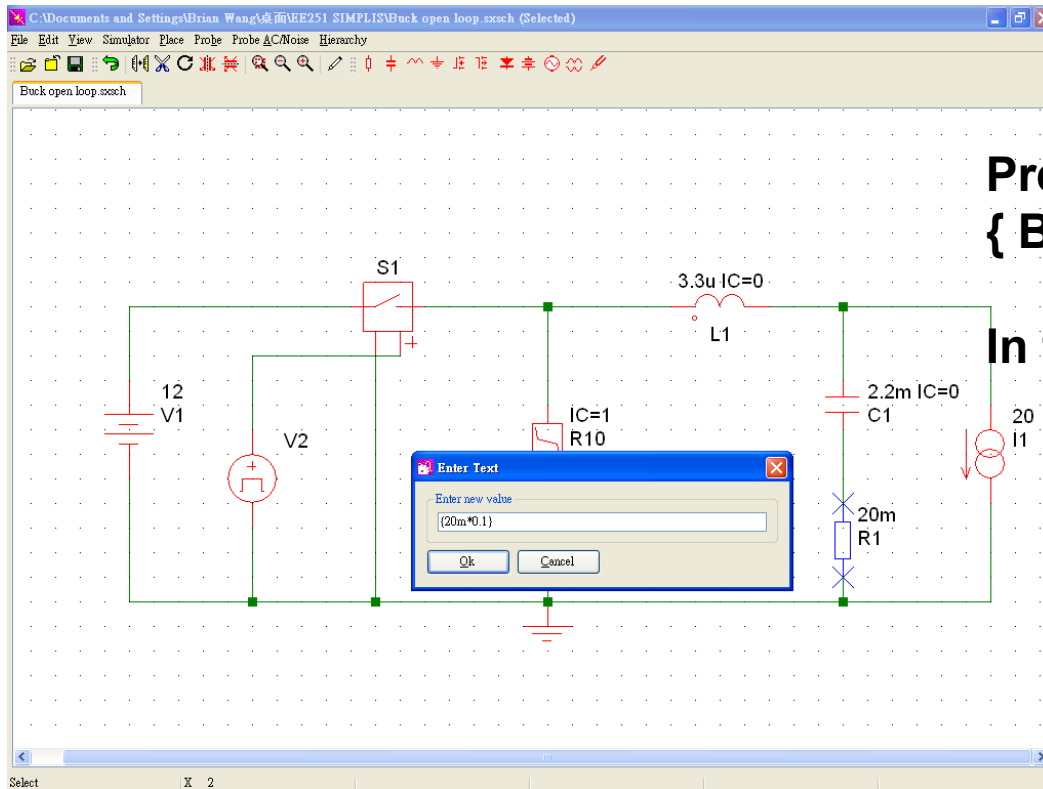


ESR base value = 20m
Choose variation = 10%

→ **ESR value will vary from 18m to 22m and the probability is a Gaussian distribution**



Monte-Carlo Simulation

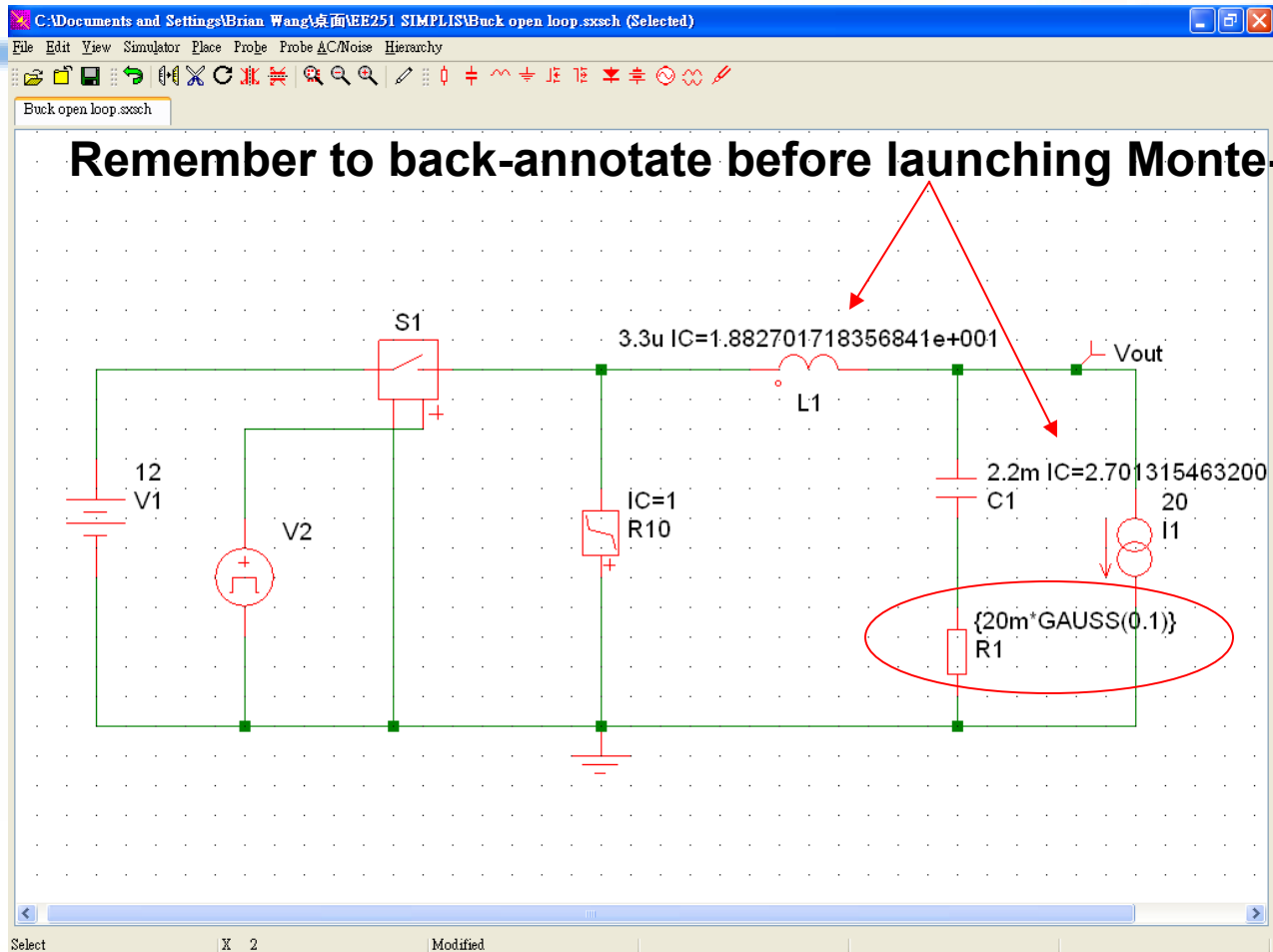


**Press Shift-F7 at the ESR and type
{ Base Value * GAUSS (Variation) }**

In this example = {20m*GAUSS(0.1)}

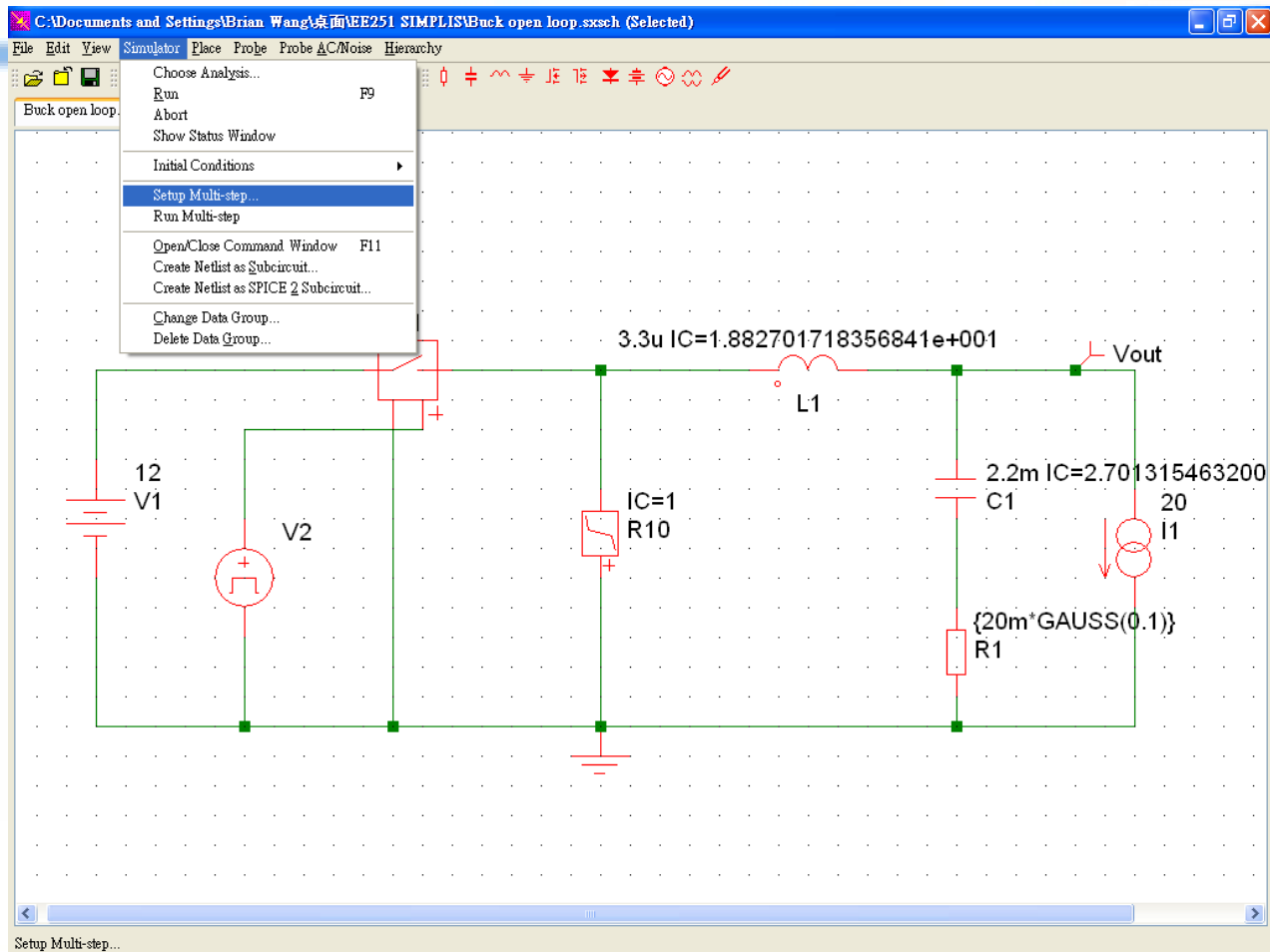
Determine component's parameter

Monte-Carlo Simulation



Component's parameter has determined

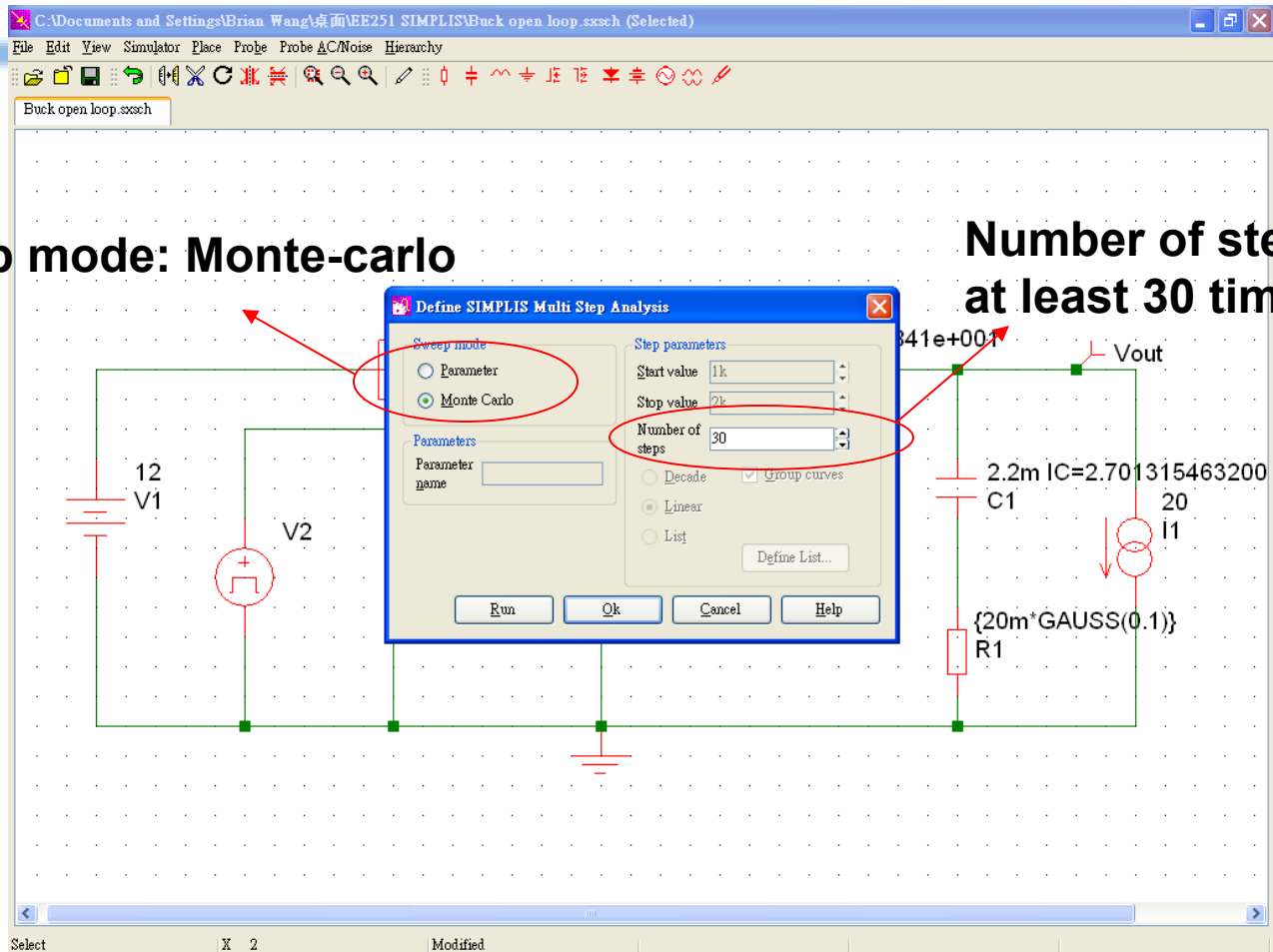
Monte-Carlo Simulation



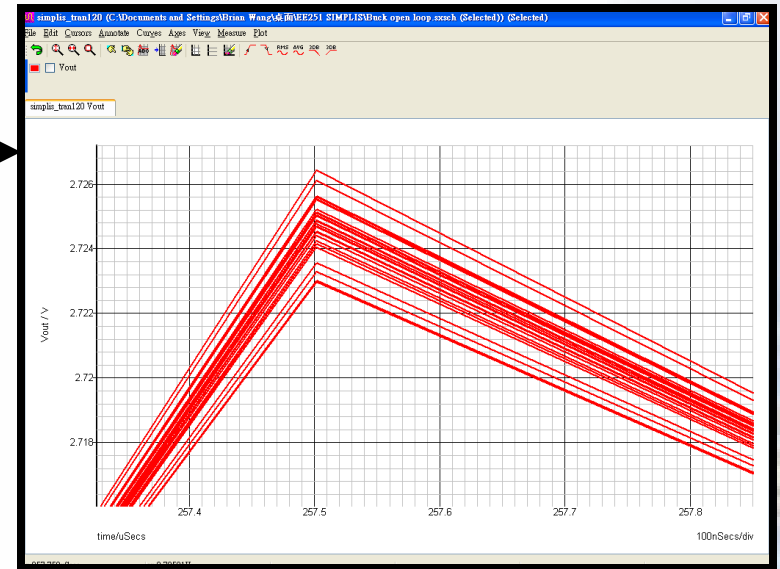
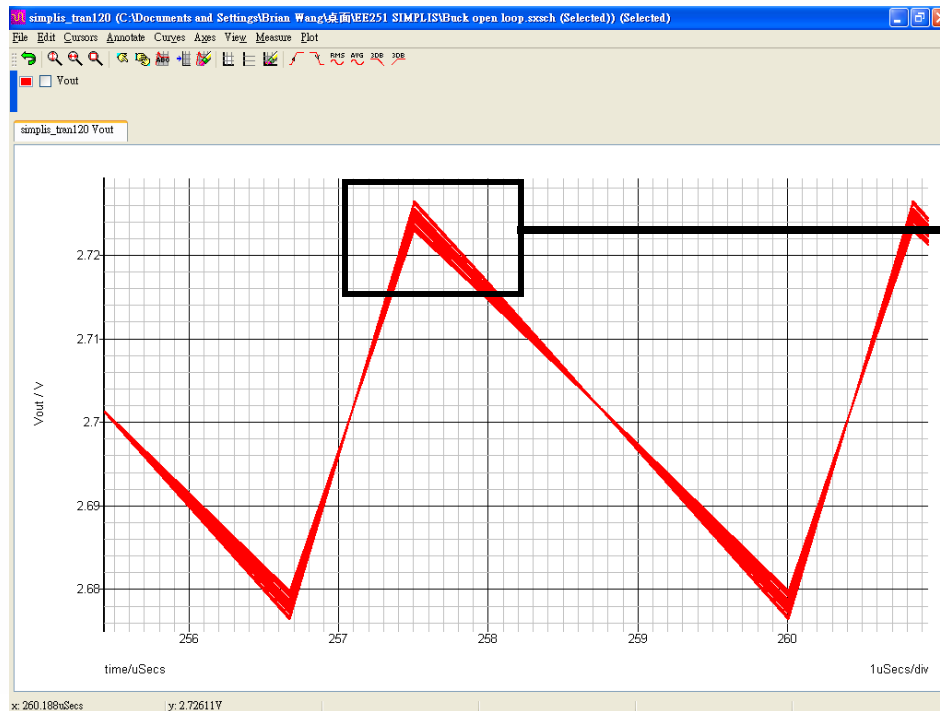
Monte-Carlo Simulation

Sweep mode: Monte-carlo

Number of step:
at least 30 times



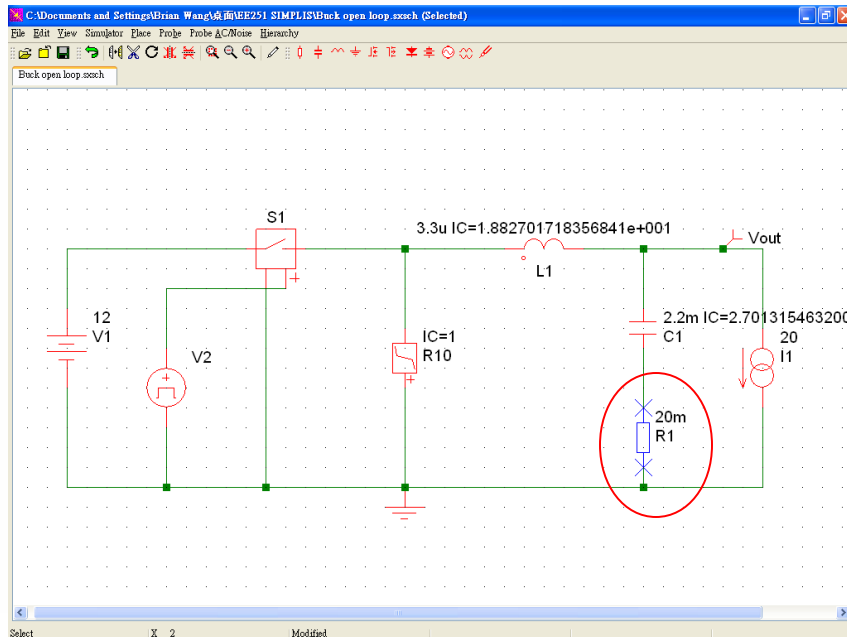
Monte-Carlo Simulation



Monte-carlo waveforms: 30 V_{out} lines of random ESR value

Multi-Step Simulation

- **Multi-step example: Select Cap's ESR to observe**

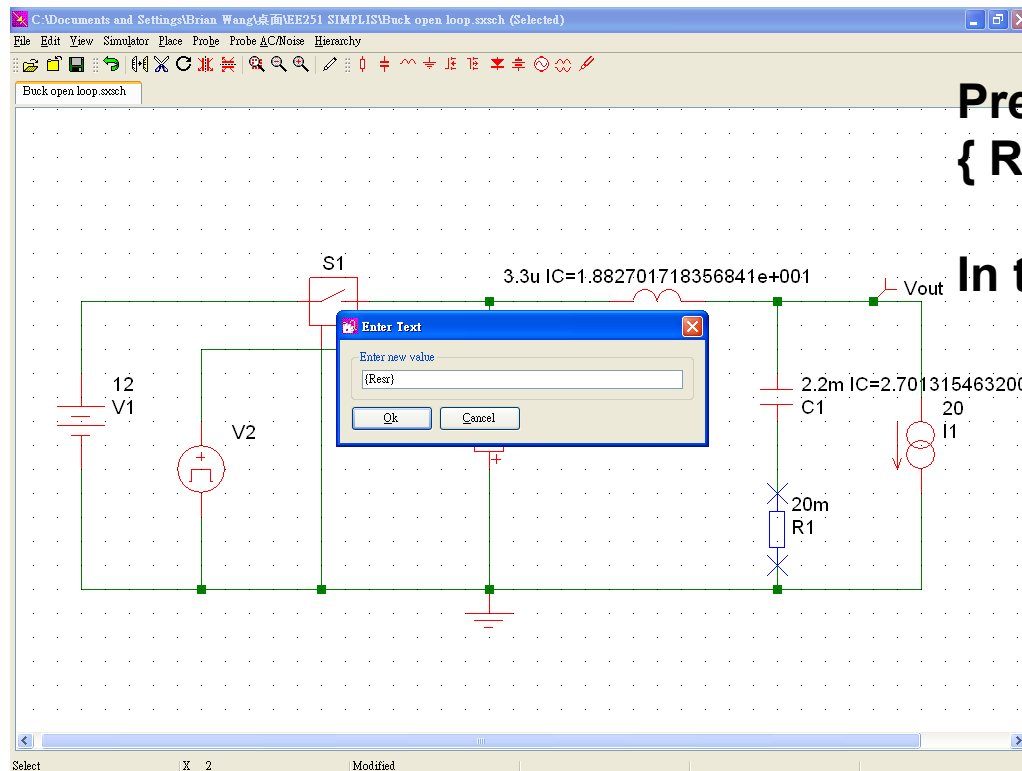


ESR base value = 20m
Choose random name to enter,
like “Resr” to replace “20m”

Set the range and distribution of
Resr, for example, from 10m to 30
m, number of steps =21

→ESR value will vary as:
10m,11m,12m,13m.....,29m,30m

Multi-Step Simulation

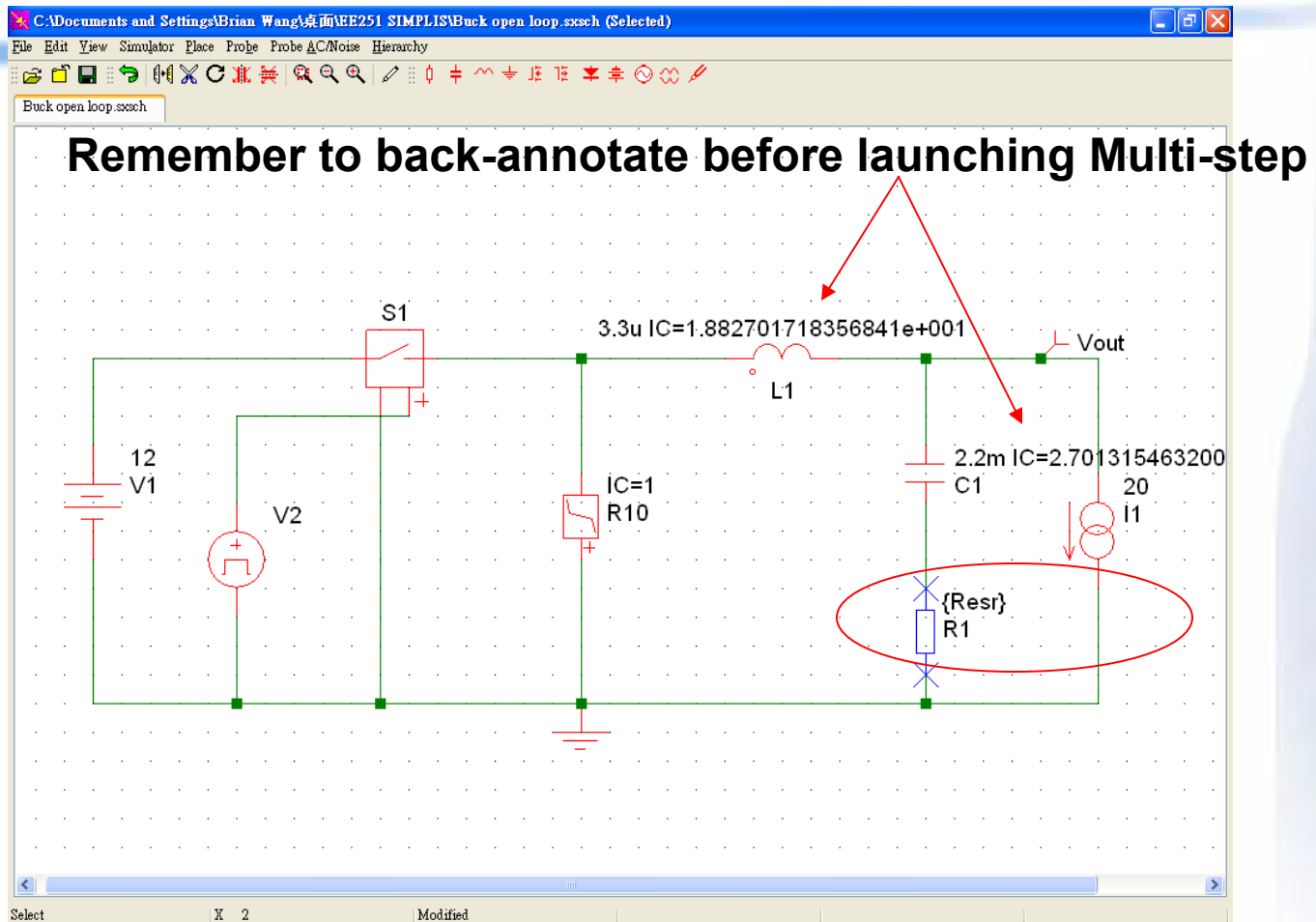


**Press Shift-F7 at the ESR and type
{ Random Name }**

In this example = {Resr}

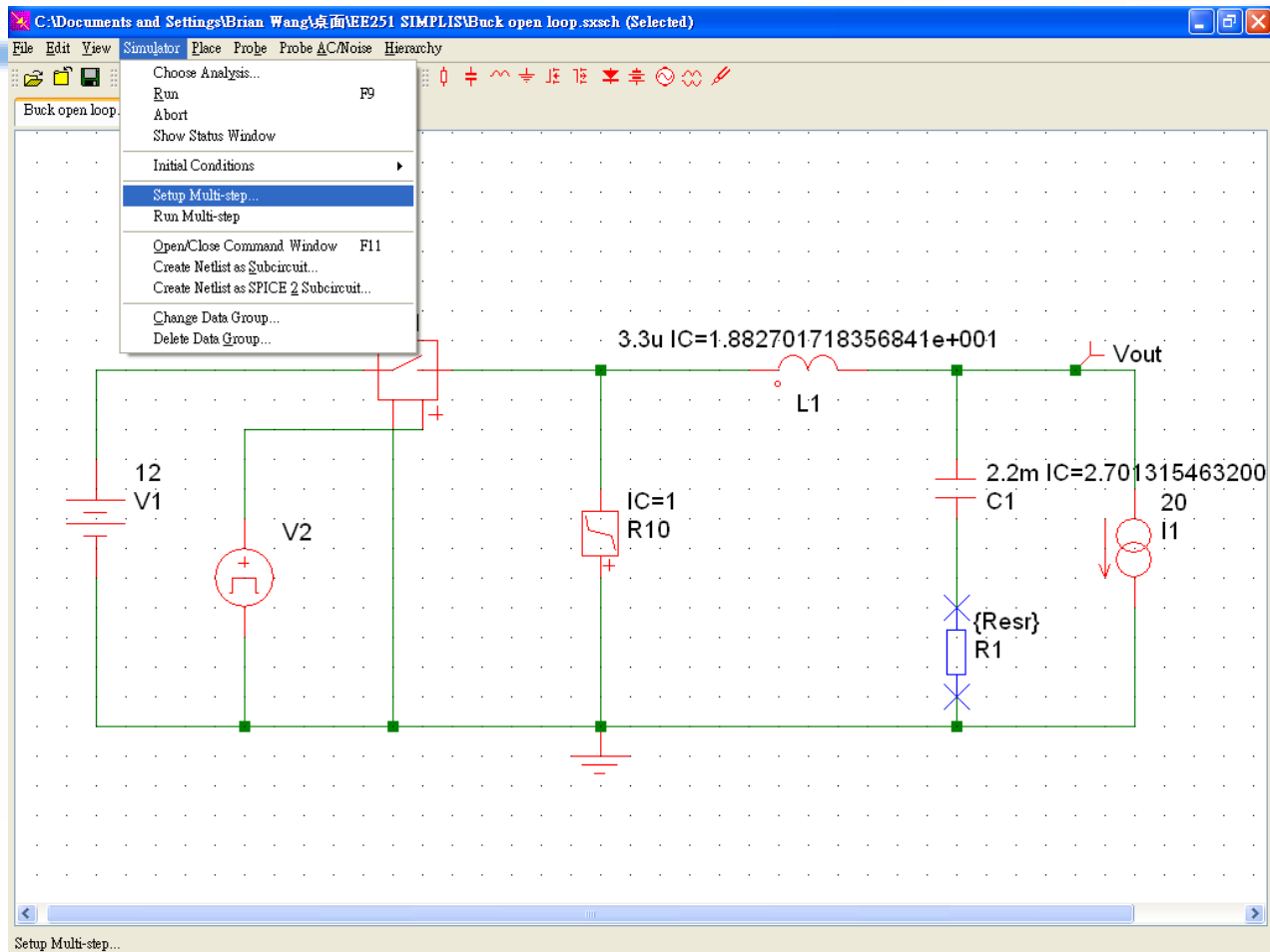
Determine component's name

Multi-Step Simulation

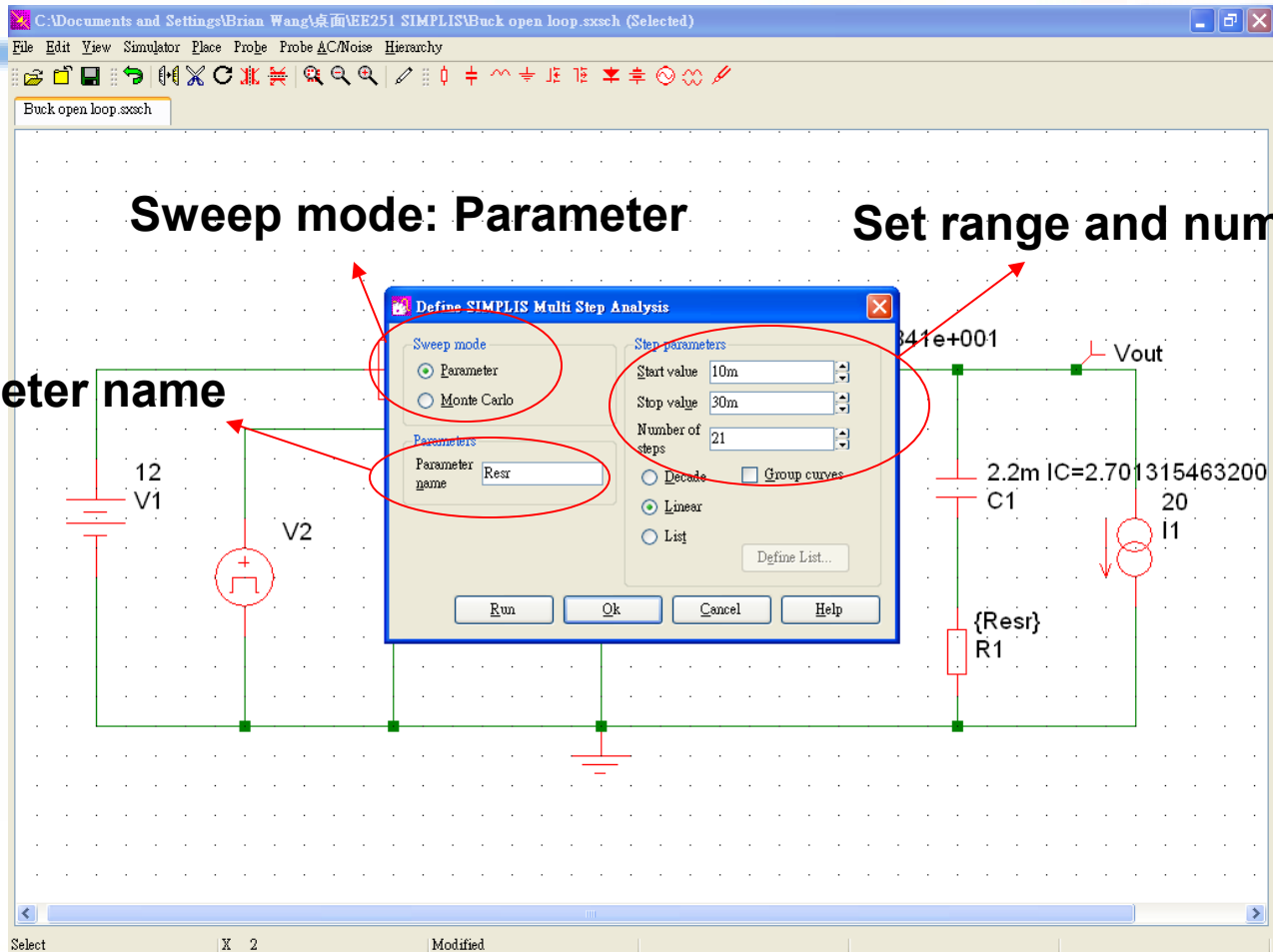


Component's name has determined

Multi-Step Simulation



Multi-Step Simulation

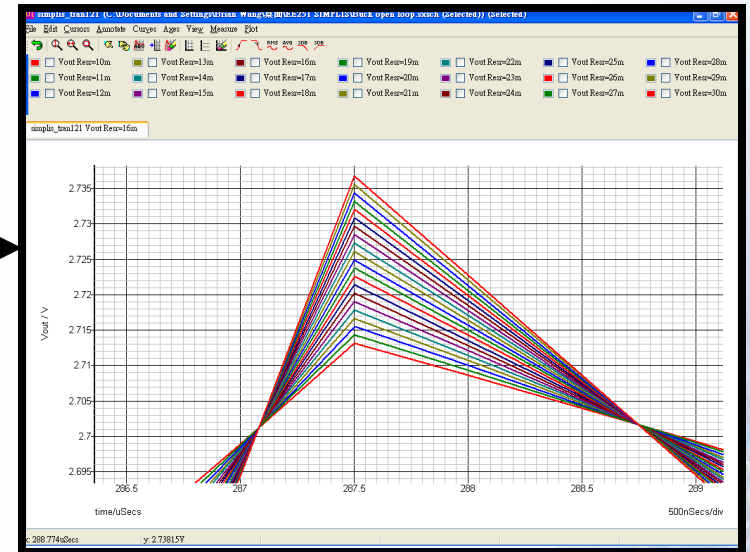
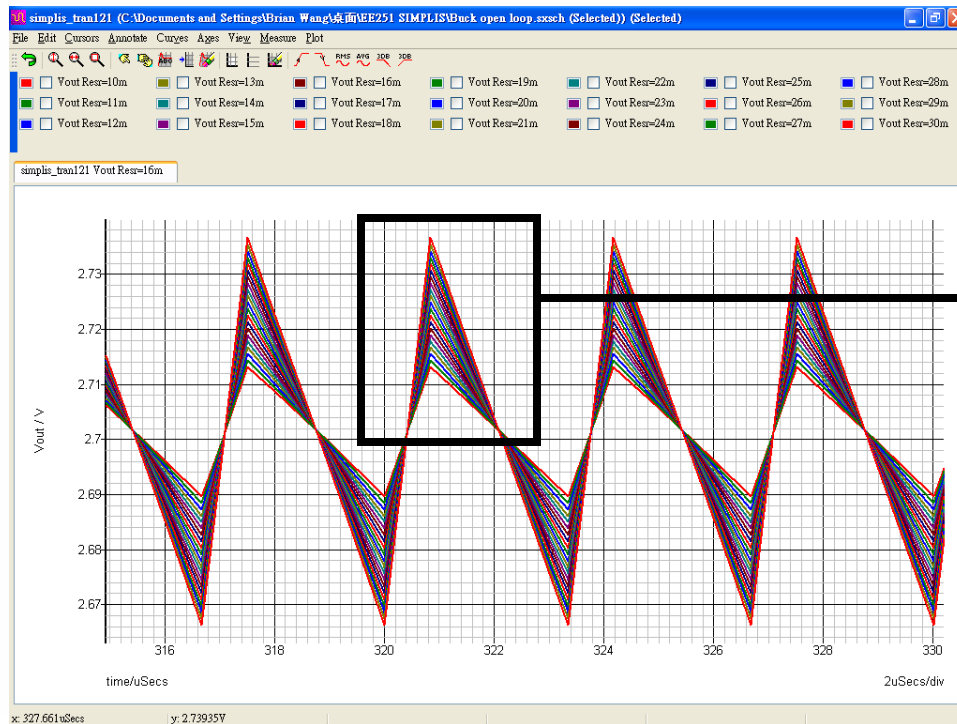


Type Parameter name

Sweep mode: Parameter

Set range and number of step

Multi-Step Simulation



Multi-step waveforms: 30 V_{out} lines of specified ESR value

Hotkey List

- F3: wire
- F5: Rotate
- F7: Edit Part
- F9: Run simulation
- Ctrl-Alt-F7: Edit Additional Parameters
- Ctrl-E: Descend Hierarchy
- Shift-F7: Edit Parameter (Only in multi-step and Monte-carlo simulations)

Conclusion

- Advantages in using SIMPLIS simulator:
 1. Faster simulation process
 2. Easier to use , harder to make faults
 3. Can run both DC and AC without changing our circuit

Thank you for listening!!

