# A 32 GSample/sec SiGe HBT Comparator for Ultra-High-Speed Analog-to-Digital Conversion

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***Abstract*—This paper presents a monolithic master-slave comparator in an ECL configuration with series-gating for ultra-high-speed medium-resolution analog-to-digital conversion. Implemented in a 200 GHz SiGe HBT technology, the complete chip die, including bondpads, is 1.731 x 1.141 mm$^2$, with the comparator occupying only 0.0226 mm$^2$ when integrated as part of an ADC. It dissipates a total of 405 mW from a 3.5 V power supply. Operating with an input frequency of 5 GHz, the circuit can oversample up to 32 GS/s, with input sensitivity ranging from 5 mV$_{pp}$ at 15 GS/s to 37 mV$_{pp}$ at 32 GS/s. Operating at Nyquist, the comparator can sample up to 30 GS/s, with input sensitivity ranging from 12 mV$_{pp}$ at 20 GS/s to 30 mV$_{pp}$ at 30 GS/s. To our knowledge, this comparator achieves the best input sensitivity-sampling rate combination when compared with other stand-alone comparators in literature.**

## I. Introduction

Numerous advantages can be achieved by digitizing radio-frequency (RF) signals early-on in the receiver path of next generation transceivers. With the increase in performance of digital signal processing (DSP) circuits, substantial area savings and power reduction can be obtained when more functionalities are processed in digital domain. To realize this goal, analog-to-digital converters (ADCs) with high sampling rates, wide input bandwidths, and modest bit resolutions are required. The comparators in these ADCs play a crucial role in determining the overall performance of the converter, including sampling rates and bit resolutions.

In this paper, we present the design and implementation of an ultra-high-speed (up to 32 GS/s) comparator suitable for either oversampled or Nyquist ADCs with medium resolution (5.0 to 7.9 bits). The comparator employs a preamplifier and master-slave (M/S) latches [1]. The 200 GHz silicon germanium (SiGe) heterojunction bipolar transistor (HBT) technology used to fabricate this comparator is discussed in Section II. Section III describes the details of the comparator design. Measurement results of the comparator are presented in Section IV, followed by a summary.

## II. SiGe HBT Technology

The SiGe HBT technology used to implement the comparator features state-of-the-art transistors with 200 GHz peak unity current gain cutoff frequency ($f_T$) and 200 GHz peak maximum oscillation frequency ($f_{max}$). It provides four levels of aluminum interconnects (with the top layer being a thick metal), a full suite of RF passive elements (including metal-insulator-metal (MIM) capacitors and spiral inductors), and a complete set of 0.25 μm digital CMOS devices. The advancement in SiGe HBT performance is only achieved by radically altering the device structure via: (1) forming the whole HBT structure in one active area without shallow trench isolation between emitter and collector contact to lower collector resistance and to reduce collector-substrate junction area; and (2) eliminating deep trench isolation to improve heat dissipation and reduce thermal resistance [2]. A schematic cross-section of the 200 GHz SiGe HBT is shown in Fig. 1.

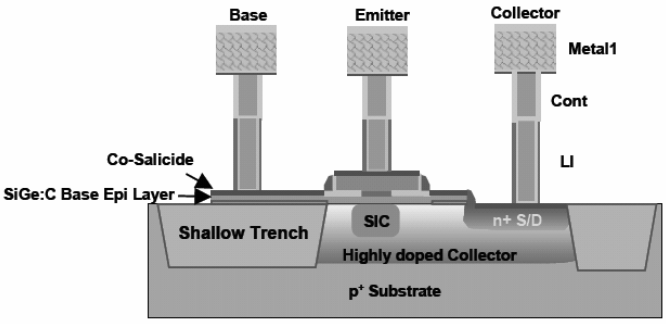


Fig. 1. Schematic cross-section of the 200 GHz SiGe HBT.

## III. Circuit Design

The comparator consists of a preamplifier, a clock buffer, a master latch, a slave latch, and an output buffer. The schematic of the preamplifier, M/S latches, and output buffer is shown in Fig. 2. The preamplifier is terminated on-chip with 50 Ω resistors to reduce jitter introduced by multiple reflections. The preamplifier serves to: (1) suppress kick-back noise from the latch [3]; (2) reduce offset voltage due to device mismatch of the following stages; and (3) improve sensitivity to small input voltages. Simulation shows the preamplifier delivering over 11 dB of gain and over 18 GHz of -3 dB bandwidth. The master and slave latch are formed with two cross-coupled differential

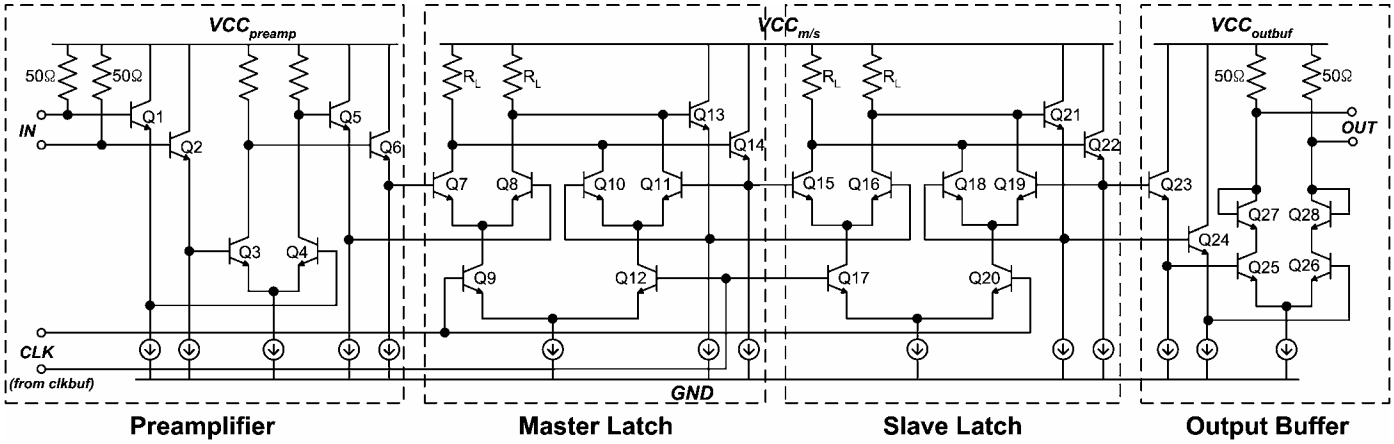


Fig. 2. Schematic of the preamplifier, master latch, slave latch, and output buffer.

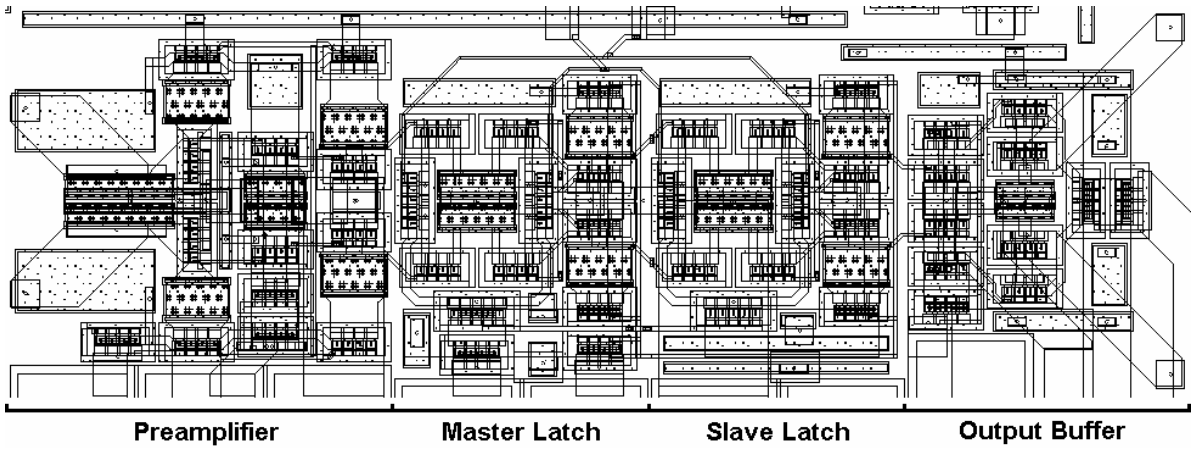


Fig. 3. Symmetrical and compact layout of the preamplifier, master latch, slave latch, and output buffer, occupying 210 x 62 μm$^2$.

pairs current switched by a series-gated clock in an ECL configuration. The maximum sampling rate of the latch is determined by the recovery time

$$t_{rec} = R_L C_{total} \left( 1 + \frac{1}{\tanh\left(V_{in}/2V_T\right)} \right), \quad (1)$$

where $R_L$ is the load resistance, $C_{total}$ is the total capacitance at collector of first differential pair ($Q_7$-$Q_8$ and $Q_{15}$-$Q_{16}$), $V_{in}$ is the differential input voltage of the latch, and $V_T$ is the thermal voltage, as well as the regeneration time constant

$$\tau_{reg} = \frac{R_L C_{total}}{g_m R_L - 1}, \quad (2)$$

where $g_m$ is the transconductance of the HBTs in the second differential pair ($Q_{10}$-$Q_{11}$ and $Q_{18}$-$Q_{19}$), with the $t_{rec}$ being the dominating factor [4]. Thus to shorten $t_{rec}$, a small $R_L$ is desired. However, a small $R_L$ will also reduce the output voltage swing of the latch and in turn degrade the current switch operation of the second differential pair [5]. Based on simulations, a compromise was made with $R_L$ of 90 Ω, resulting in a $t_{rec}$ of 19 ps for a $V_{in}$ of 7 mV. The output buffer, also on-chip 50 Ω terminated, is introduced to drive the test equipment without loading the output of the slave latch.

Proper layout is critical as circuit performance increases to the tens of GHz frequency range. High-speed operation can be strongly degraded by the parasitics introduced during layout, and special care must be taken to control their impact. To minimize common-mode noise, the layout is made as symmetrical as possible. Crossing area between metal routing are kept small to reduce crossing capacitance without increasing series resistance or violating electromigration rules. Interconnects in the critical path are kept short to curve layout parasitics. Auto-filler blocking layer are added to prevent unintentionally altering the microwave behavior of the propagating signals. Tapered lines are used, and 90° turns are avoided to minimize internal reflections. Fig. 3 shows the symmetrical and compact layout of the preamplifier, M/S latches, and output buffer. On-chip by-pass MIM capacitors are used on *dc* supply lines for high-frequency decoupling. Connections from the preamplifier, clock buffer, and output buffer to the bondpads are distributed towards the left, top, and right side, respectively, to facilitate on-wafer testing. Twelve

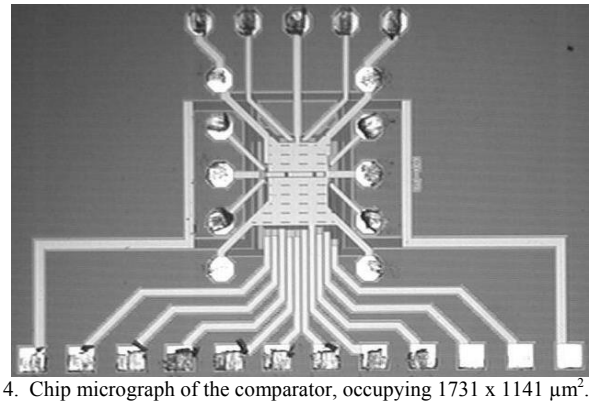

Fig. 4. Chip micrograph of the comparator, occupying 1731 x 1141 μm$^2$.

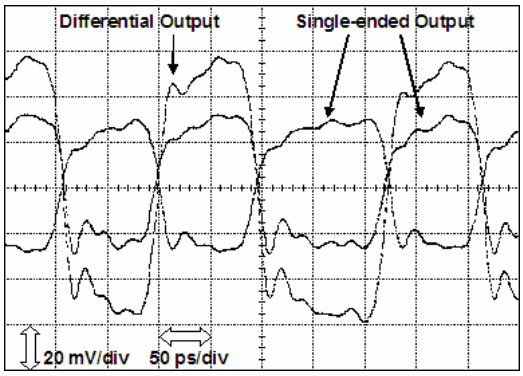


Fig. 5. Measured output waveforms of the comparator with a 5 GHz input oversampled at 32 GS/s (20 mV/div, 50 ps/div).

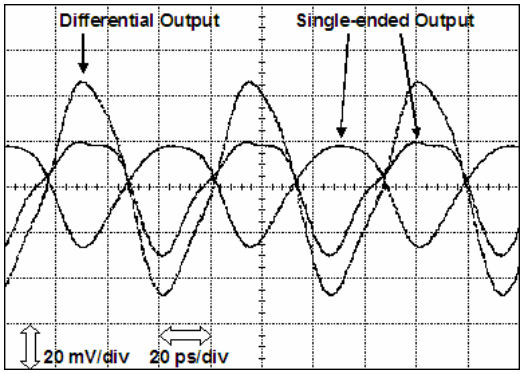


Fig. 6. Measured output waveforms of the comparator operating at Nyquist with a sampling rate of 30 GS/s (20 mV/div, 20 ps/div).

*dc* supply lines, used for current monitoring, are dispersed to the bottom side.

## IV. Measurement Results

The chip micrograph of the comparator is shown in Fig. 4. The total die area is 1731 x 1141 μm$^2$ (including bondpads). The large width of the chip is determined by the footprint of the 12 pin *dc* probes (for current monitoring). The active area of the preamplifier, M/S latches, and output buffer is 210 x 62 μm$^2$, and 82 x 116 μm$^2$ for the clock buffer.

The comparator is characterized on-wafer using 40 GHz

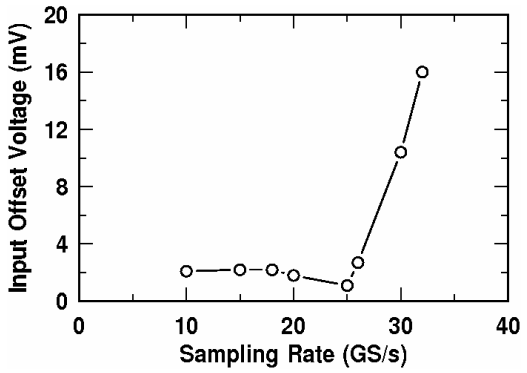


Fig. 7. Measured input offset voltage of the comparator as a function of sampling rate.

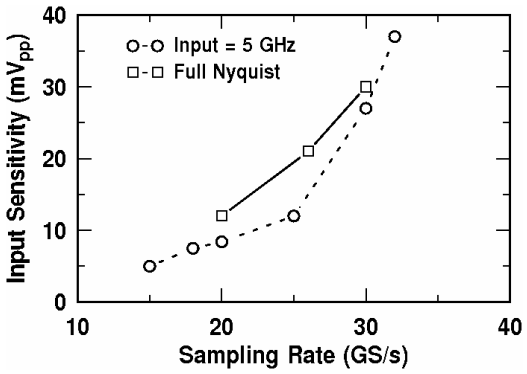


Fig. 8. Measured input sensitivity of the comparator as a function of sampling rate.

probes and cables. Hybrids and baluns are used to convert single-ended signals into differential ones. Phase tuners are used to compensate for different cable phase characteristics before connecting them into the test setup to ensure that the phase of complementary signals are properly maintained since any asymmetry caused by external testing equipments will degrade the performance of the comparator at high frequencies. Operating off a 3.5 V power supply, the comparator dissipates a total power of 405 mW, with the M/S latch core consuming 136 mW.

The comparator was tested with sine wave input and clock under two different conditions: (1) a 5 GHz input oversampled up to 32 GS/s; and (2) full Nyquist with sampling rates up to 30 GS/s. The output waveforms (both differential and single-ended) of the comparator operating with a 5 GHz input oversampled at 32 GS/s, shown in Fig. 5, measured a rise/fall time (20% to 80%) of 12.3/11.2 ps and a random (RMS)/deterministic (peak-to-peak) jitter of 1.15/5.59 ps. The output waveforms of the comparator operating at Nyquist with a sampling rate of 30 GS/s, shown in Fig. 6, measured a rise/fall time of 13.0/9.5 ps and a random/deterministic jitter of 1.09/5.80 ps.

The measured input offset voltage of the comparator, caused by device mismatch, as a function of sampling rate with *dc* input is shown in Fig. 7. The offset remains relatively constant at 2.2 mV when sampled below 18 GS/s, reaches a

TABLE II
COMPARISON WITH PUBLISHED STAND-ALONE COMPARATORS OPERATING AT SIMILAR SAMPLING RATE

| Reference | Maximum Sampling Rate [GS/s] | Sensitivity @ Input / Clock [@ GHz / GS/s] | Input Offset [mV] | Supply Voltage [V] | Total Power Consumption [mW] | Process / $f_T$ [- / GHz] | Active Area [mm$^2$] |
|---|---|---|---|---|---|---|---|
| This work | 32 | 8.4 $mV_{pp}$ @ 5 / 20 | < 2.2 up to 25 GS/s | 3.5 | 405 | SiGe / 200 | 0.0226 |
| [6] | 25 | N/A | 1.5 typical / 6 max | 3.3 | 550 | InP / N/A | N/A |
| [7] | 20 | 8.9 $mV_{pp}$ @ 3 / 18 | 4.2 max | 3.5 | 82[a] | SiGe / 120 | 0.0455 |
| [8] | 16 | N/A | N/A | N/A | 221 | SiGe / 55 | 0.0960 |
| [9] | 8 | 30 mV @ 4 / 8 | N/A | -6 | N/A | GaAs / 30 | N/A |

[a] Preamplifier and M/S latches only.

TABLE I
PERFORMANCE SUMMARY OF THE COMPARATOR

| | |
|---|---|
| Supply Voltage | 3.5 V |
| Power Consumption | 405 mW |
| Preamplifier | 133 mW |
| Clock Buffer | 90 mW |
| M/S Latches | 136 mW |
| Output Buffer | 46 mW |
| Input Range | 1.2 $V_{pp}$ max |
| Sampling Rate | 32 GS/s max |
| Rise/Fall Time (20% to 80%) | 12.3 / 11.2 ps (in/clk = 5 GHz / 32 GS/s) |
| Random/Deterministic Jitter | 1.09 / 5.80 ps (Nyquist, clk = 30 GS/s) |
| Input Offset Voltage | < 2.2 mV up to 25 GS/s |
| Input Sensitivity | 8.4 $mV_{pp}$ (in/clk = 5 GHz / 20 GS/s) |

minimum of 1.1 mV at 25 GS/s, and then increases to 16.7 mV at 32 GS/s.

Fig. 8 shows the input sensitivity of the comparator, defined as the minimum differential peak-to-peak input voltage that can be detected, as a function of sampling rate operating with a 5 GHz input and at Nyquist. With the 5 GHz input, the measured sensitivity ranges from 5 $mV_{pp}$ at 15 GS/s to 37 $mV_{pp}$ at 32 GS/s, equivalent to 7.9 bits and 5.0 bits of ADC resolution, respectively, for the full input range of 1.2 $V_{pp}$. At Nyquist, the sensitivity ranges from 12 $mV_{pp}$ at 20 GS/s to 30 $mV_{pp}$ at 30 GS/s, equivalent to 6.6 bits and 5.3 bits of ADC resolution, respectively. This demonstrates that the comparator is well-suited for ultra-high-speed medium-resolution oversampled or Nyquist ADCs. The performance of the comparator is summarized in Table I.

Numerous comparators, either stand-alone or integrated into full ADCs, have been published in literature. Comparisons of this work to other high-speed stand-alone comparators are shown in Table II. Integrated comparators are omitted due to lack of direct measurement results on the comparators themselves. To our knowledge, this comparator achieves the best input sensitivity-sampling rate combination, offering significant benefit to the design of ultra-high-speed oversampled or Nyquist ADCs.

## V. SUMMARY

An ultra-high-speed comparator has been designed and fabricated in a 200 GHz SiGe HBT technology. The comparator can oversample a 5 GHz input up to 32 GS/s or sample at Nyquist up to 30 GS/s, while attaining 5.0 to 7.9 bits of ADC resolution. To our knowledge, this comparator achieves the best input sensitivity-sampling rate combination when compared with other published stand-alone comparators.

## ACKNOWLEDGMENT

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