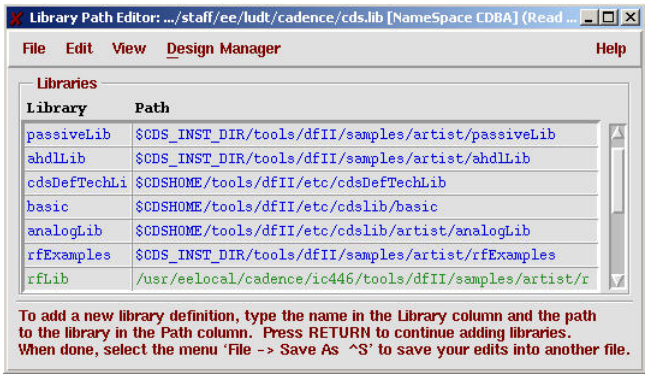
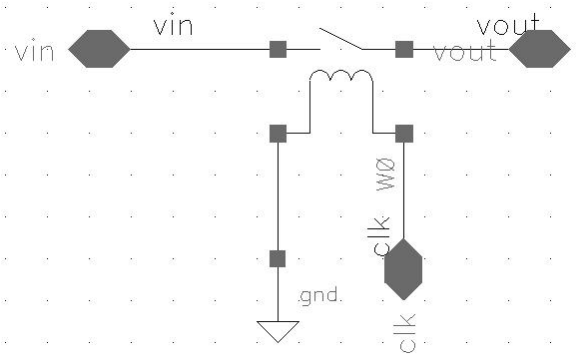
Simulating Switched-Cap Filter in CADENCE

- Pre-Setups
  - Add 'ahdl' library to your path
    - In library manager→Edit→library path→add "ahdlLib".

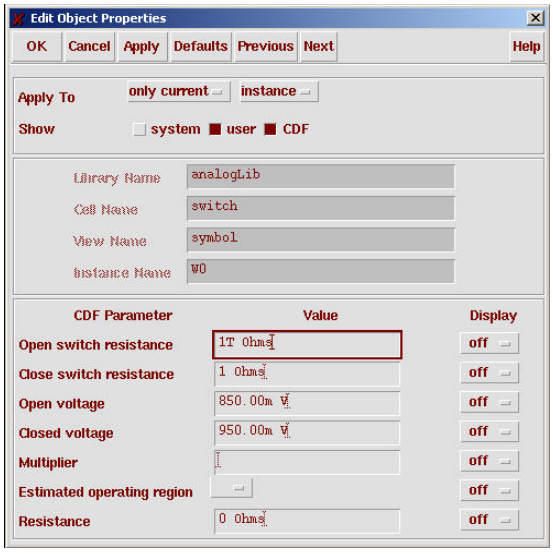


    - If the library already exists, go on to the next step.

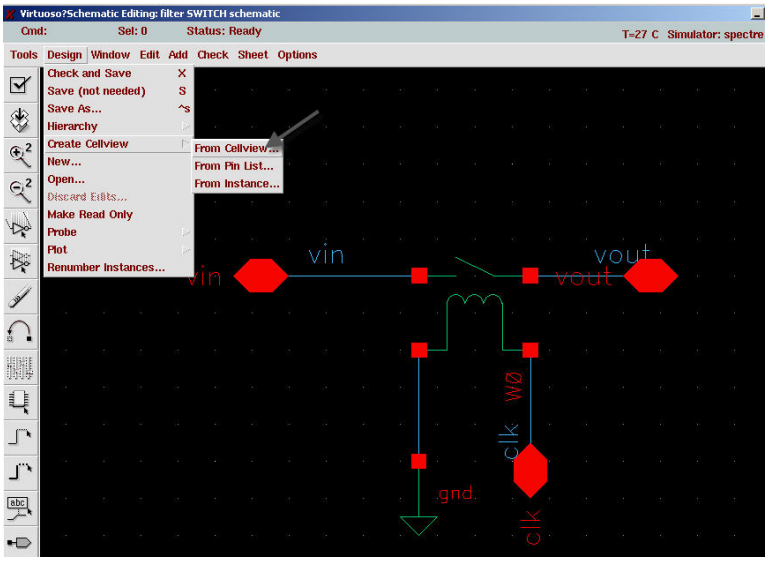
- Using Ideal Components
  - Ideal Switch
    - The ideal switch is in the library -- "Analoglib→ switch"
    - Add an Switch into schematic
      - In the schematic window, press 'i' (or 'add' → 'instance'); press 'p' to add pin.



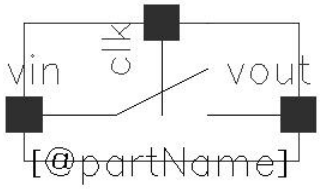
      - Select the switch and press 'q' to edit object properties.



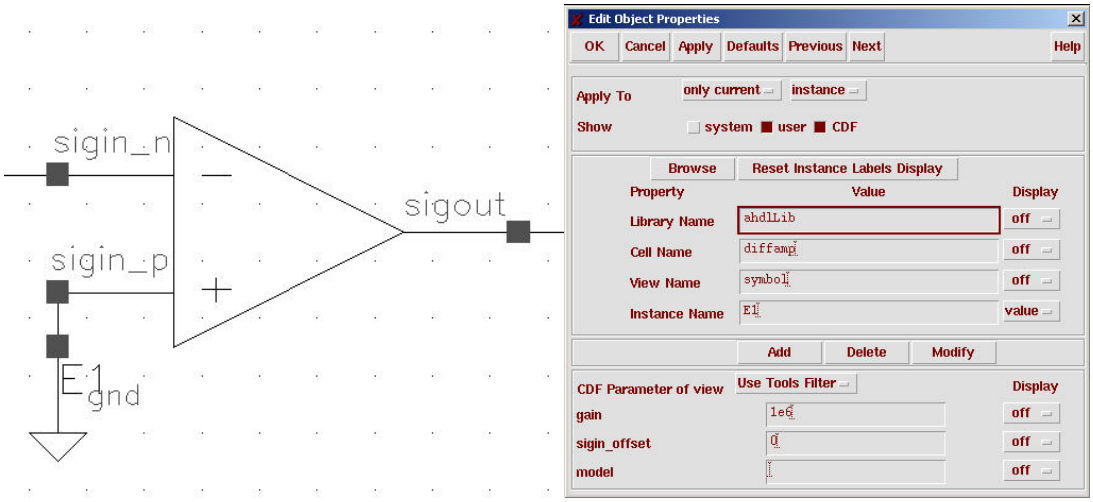
- Some parameters to modify.
  - *Open Switch Resistance* → Turn on Resistance
  - *Close Switch Resistance* → Turn on Resistance
  - The switch turns on when control voltage larger than *Close Voltage*
  - The switch turns off when control voltage smaller than *open Voltage*
- Make an symbol for the Switch (*optional, just for convenience*)
  - Create a symbol from cellview



  - Draw a symbol as you like



- Ideal OPAMP
  - The ideal OPAMP is in the library -- "ahdllib→ diffamp"
  - Add an OPAMP to schematic and edit property.

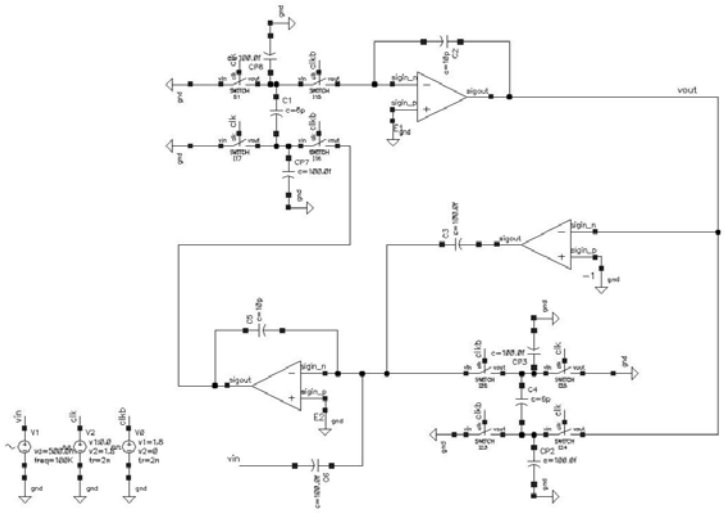


- gain → the gain of the OPAMP
- sigin_offset → the input referred offset of the OPAMP

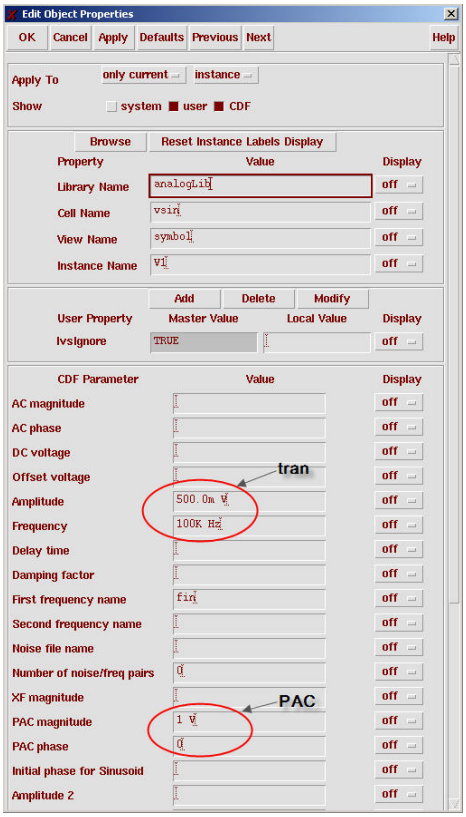
✧ Schematic using Ideal Components

Before implementing everything in transistor level, ideal components can be used to check the functionality. The ideal switch and OPAMP can be replaced with real components later.

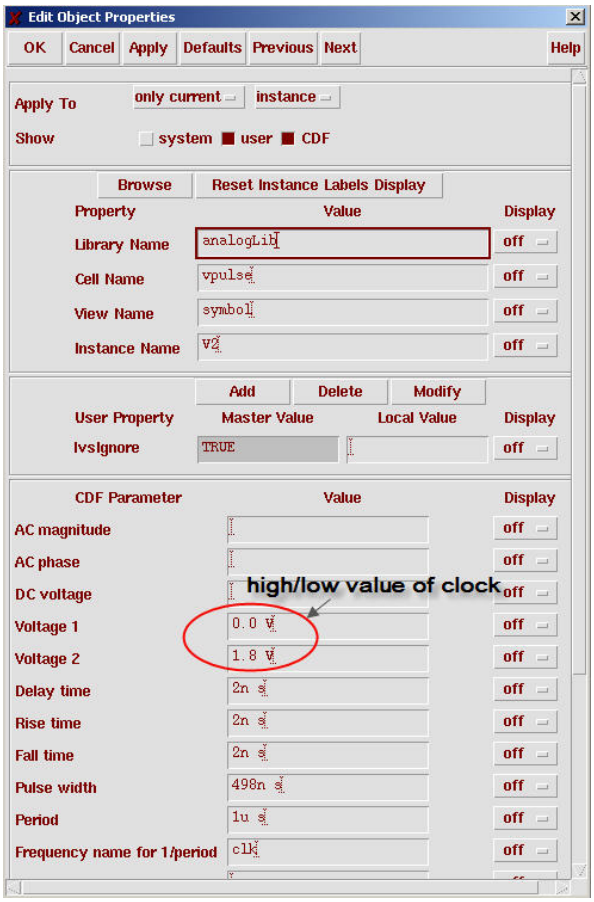
- Draw schematic according to the filter in behavior level obtained by Matlab, switcap or other tools.



- Use 'vsin' to give input
  - Location: 'analoglib'→'vsin'
  - Parameters:



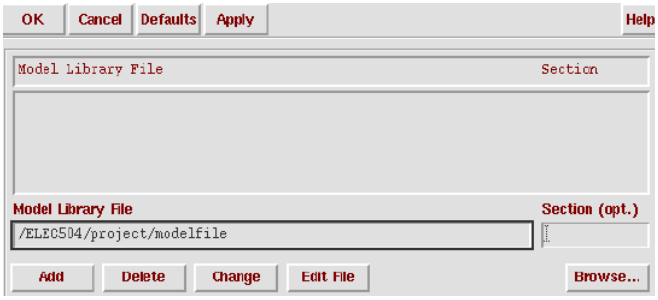
- Use 'vpulse' to give clock
  - Location: 'analoglib'→'vpulse'
  - Parameters:



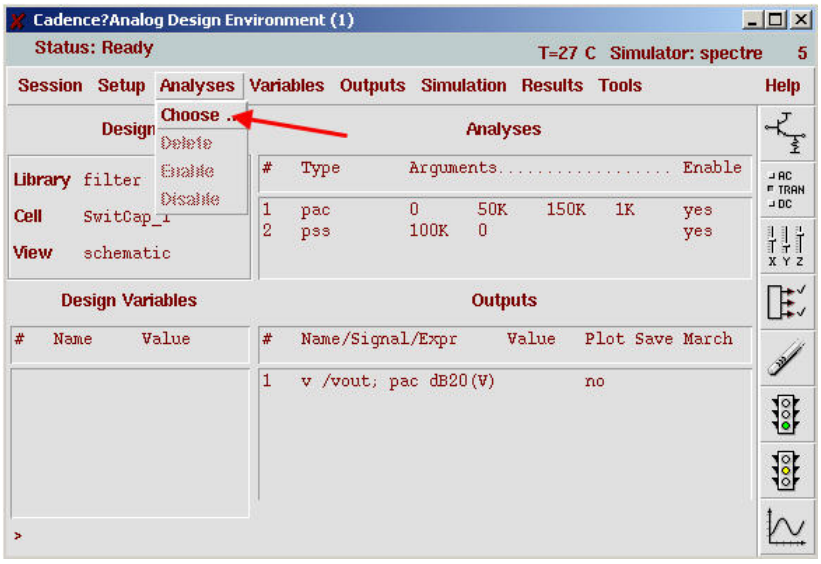
  - Make sure the two clocks are non-overlap, better to check it before doing further simulation.

✧ Simulation using ideal components.

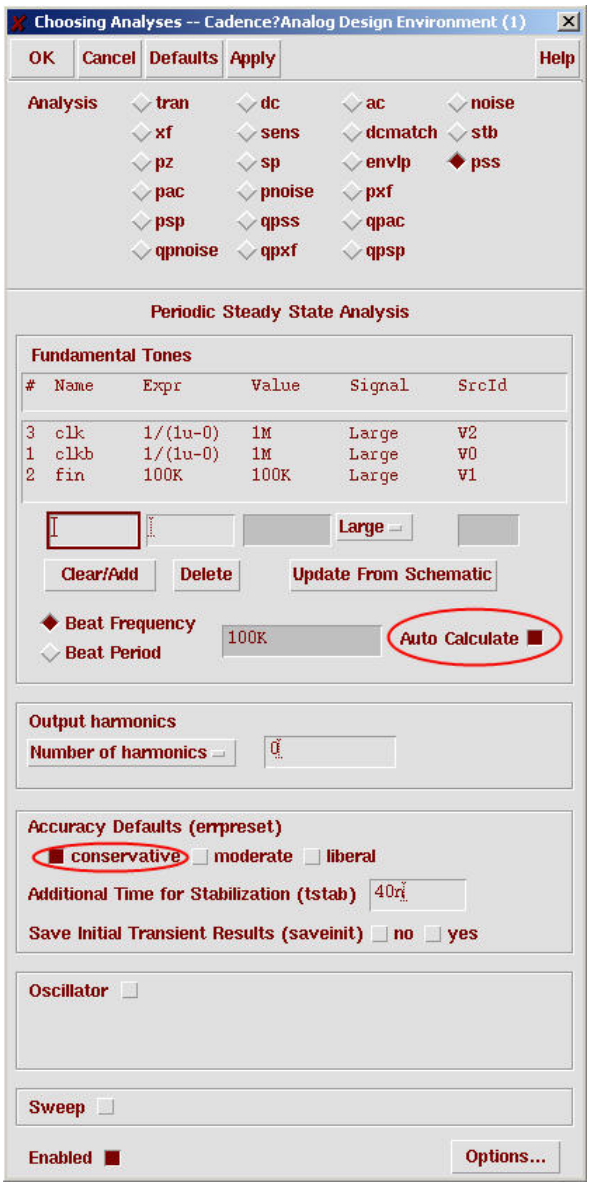
- Set model library (only useful for transistor level simulation)
  - Obtain the model file, put it in one directory.
  - In schematic window, Tools→Analog Environment→Setup→Model Libraries,



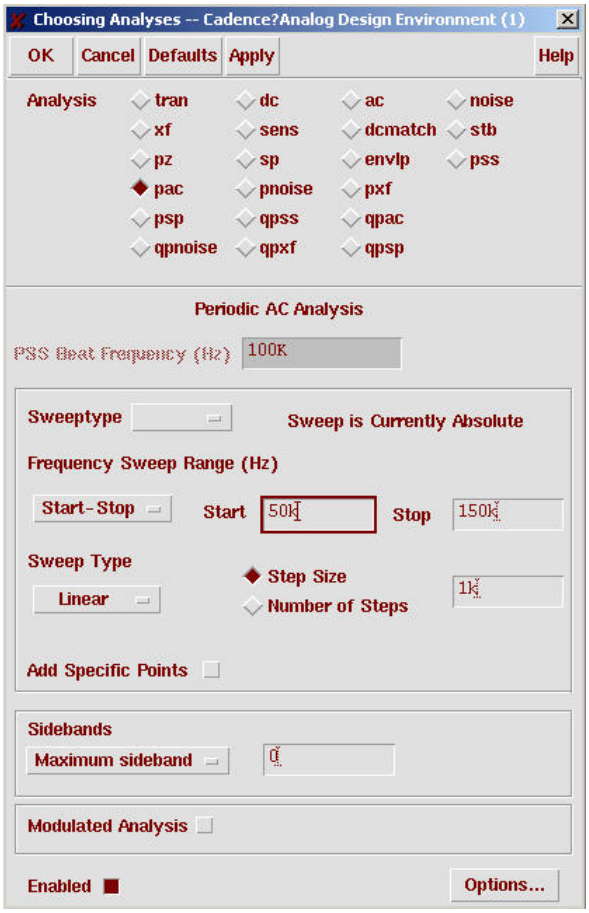
- Setup for PSS and PAC simulation
  - Used to obtain the frequency response of the filter
  - In schematic window, Tools→Analog Environment


Cadence?Analog Design Environment (1)
Status: Ready
T=27 C Simulator: spectre 5
Session Setup Analyses Variables Outputs Simulation Results Tools Help
Choose ...
Delete
Enable
Disable
Design
Analyses
Library filter
Cell SwitCap_1
View schematic
Type Arguments Enable
1 pac 0 50K 150K 1K yes
2 pss 100K 0 yes
Design Variables
Outputs
Name Value
Name/Signal/Expr Value Plot Save March
1 v /vout; pac dB20(V) no
>

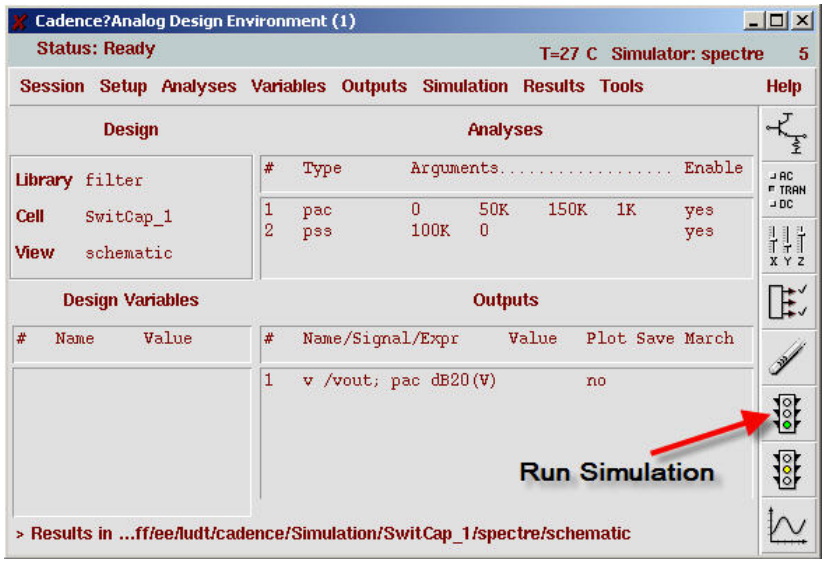
- PSS setup


Choosing Analyses -- Cadence?Analog Design Environment (1)
OK Cancel Defaults Apply Help
Analysis tran dc ac noise
xf sens dcmatch stb
pz sp envlp pss
pac pnoise pxf
psp qpss qpac
qpnoise qpxf qpsp
Periodic Steady State Analysis
Fundamental Tones
Name Expr Value Signal SrcId
3 clk 1/(1u-0) 1M Large V2
1 clkb 1/(1u-0) 1M Large V0
2 fin 100K 100K Large V1
Large
Clear/Add Delete Update From Schematic
Beat Frequency
Beat Period
100K
Auto Calculate
Output harmonics
Number of harmonics
0
Accuracy Defaults (errpreset)
conservative moderate liberal
Additional Time for Stabilization (tstab) 40n
Save Initial Transient Results (saveinit) no yes
Oscillator
Sweep
Enabled
Options...

- PAC setup

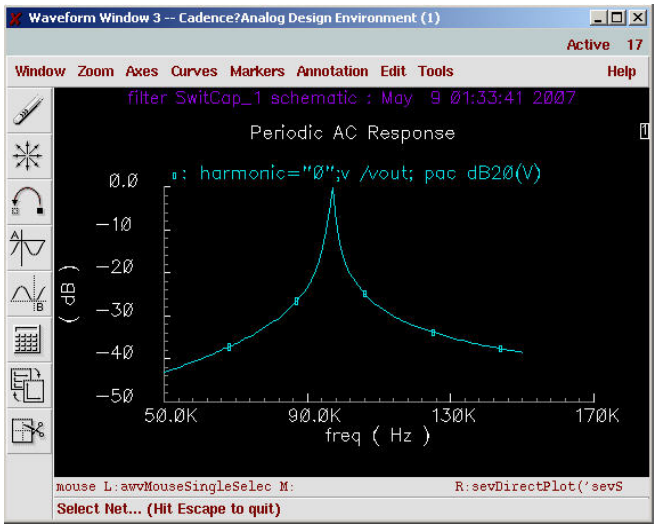


- Run Simulation



- View Result

Select the output net on the schematic, and press ‘esc’ to see the waveform



- ✧ Use non-ideal components to do the simulation
  - ■ Replace ideal switch with transistor level switch, observe the change of the result.
  - ■ Replace ideal OPAMP with non-ideal OPAMP, observe the change of the result.