Simulating Switched-Cap Filter in CADENCE

- ♦ Pre-Setups
 - Add 'ahdl' library to your path
 - In library manager \rightarrow Edit \rightarrow library path \rightarrow add "ahdlLib".

Libraries		
Library	Path	
passiveLib	<pre>\$CDS_INST_DIR/tools/dfII/samples/artist/passiveLib</pre>	12
ahdlLib	<pre>\$CDS_INST_DIR/tools/dfII/samples/artist/ahdlLib</pre>	T F
cdsDefTechLi	<pre>\$CDSHOME/tools/dfII/etc/cdsDefTechLib</pre>	
basic	<pre>\$CDSHOME/tools/dfII/etc/cdslib/basic</pre>	
analogLib	<pre>\$CDSHOME/tools/dfII/etc/cdslib/artist/analogLib</pre>	Ī
rfExamples	<pre>\$CDS_INST_DIR/tools/dfII/samples/artist/rfExamples</pre>	1
rfLib	/usr/eelocal/cadence/ic446/tools/dfII/samples/artist/r	1 5

- If the library already exists, go on to the next step.
- ♦ Using Ideal Components
 - Ideal Switch

- The ideal switch is in the library -- "Analoglib \rightarrow switch"
- Add an Switch into schematic
 - In the schematic window, press 'i' (or 'add' \rightarrow 'instance'); press 'p' to add pin.

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• Select the switch and press 'q' to edit object properties.

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- Some parameters to modify.
 - Open Switch Resistance \rightarrow Turn on Resistance
 - $\blacksquare Close Switch Resistance \rightarrow Turn on Resistance$
 - The switch turns on when control voltage larger than *Close Voltage*
 - The switch turns off when control voltage smaller than *open Voltage*
- Make an symbol for the Switch (*optional*, *just for convenience*)
 - Create a symbol from cellview



Draw a symbol as you like



- Ideal OPAMP
 - The ideal OPAMP is in the library -- "ahdllib \rightarrow diffamp"
 - Add an OPAMP to schematic and edit property.

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- gain \rightarrow the gain of the OPAMP
- sigin_offset \rightarrow the input referred offset of the OPAMP

♦ Schematic using Ideal Components

Before implementing everything in transistor level, ideal components can be used to check the functionality. The ideal switch and OPAMP can be replaced with real components later.

Draw schematic according to the filter in behavior level obtained by Matlab, switcap or other tools.



- Use 'vsin' to give input
 - ◆ Location: 'analoglib' → 'vsin'
 - Parameters:

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- Use 'vpulse' to give clock
 - ◆ Location: 'analoglib' → 'vpulse'
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- Make sure the two clocks are non-overlap, better to check it before doing further simulation.
- ♦ Simulation using ideal components.
 - Set model library (only useful for transistor level simulation)
 - Obtain the model file, put it in one directory.
 - In schematic window, Tools \rightarrow Analog Environment \rightarrow Setup \rightarrow Model Libraries,

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- Setup for PSS and PAC simulation
 - Used to obtain the frequency response of the filter
 - ◆ In schematic window, Tools→Analog Environment

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Select the output net on the schematic, and press 'esc' to see the waveform



- ♦ Use non-ideal components to do the simulation
 - Replace ideal switch with transistor level switch, observe the change of the result.
 - Replace ideal OPAMP with non-ideal OPAMP, observe the change of the result.