Metastability

赵启林 klin

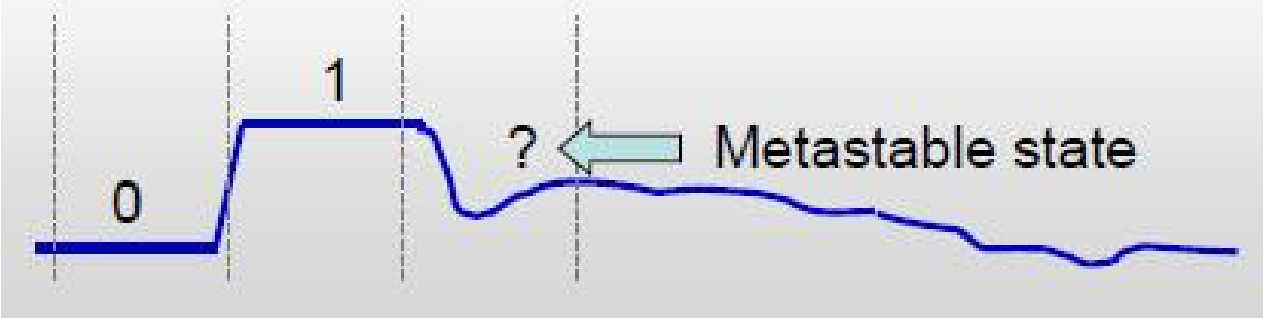
forqilin@163.com

Goal

- Define metastability
- Demonstrate various techniques to address metastability
- Discuss aspects of metastability that will need to be validated

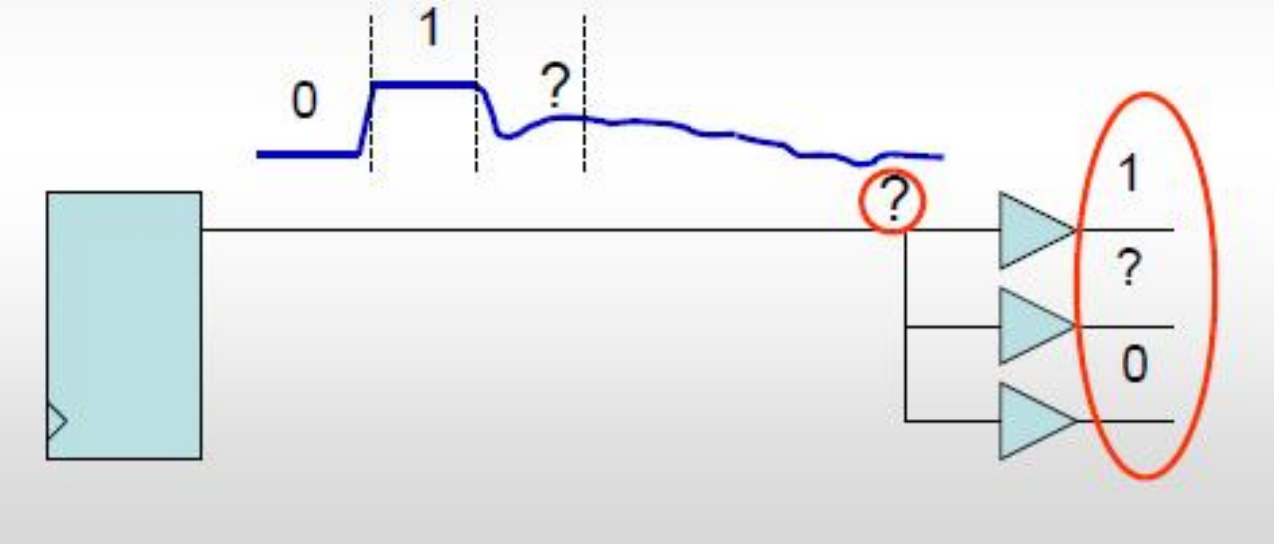
What is metastability?

- Metastability is an undesirable non-equilibrium electronic state that can persist for a long period of time
- For example, a flip-flop is a device that has two well-defined states, traditionally designated 0 and 1
- Under certain conditions, the device can hover between these two states

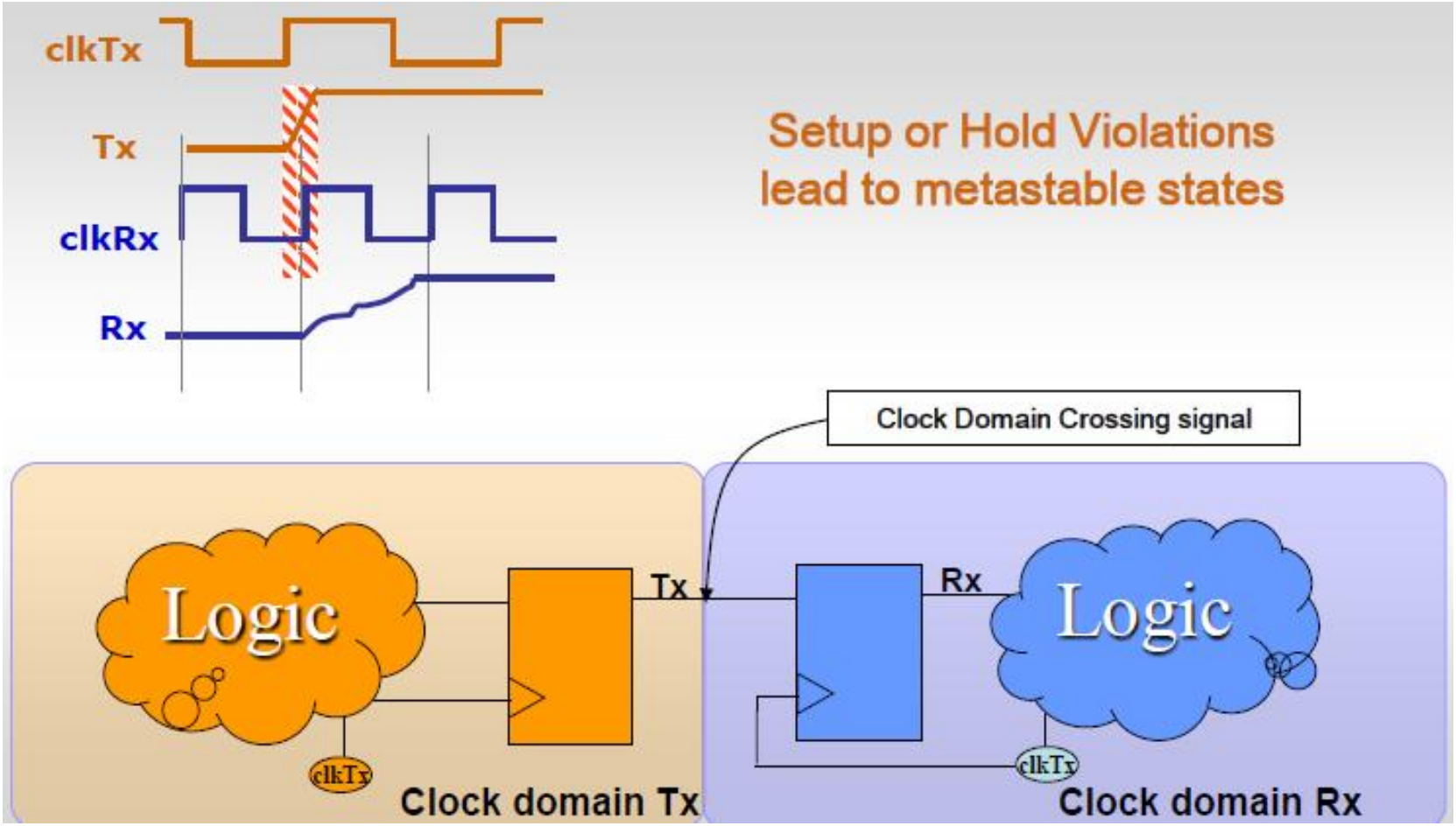


What is the problem?

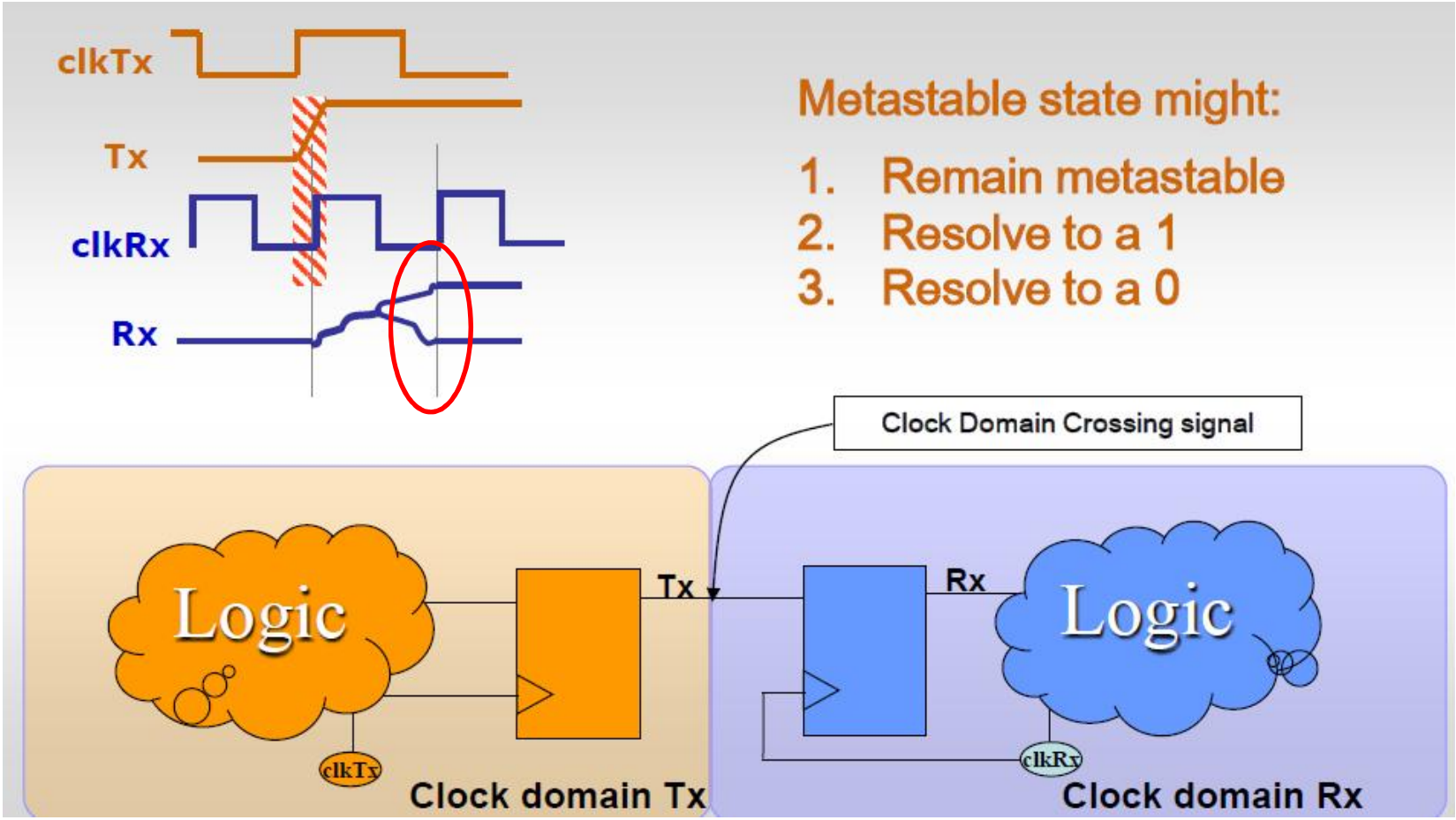
- Metastable values can cause illegal signal values to propagate throughout the rest of the design



What causes metastability?



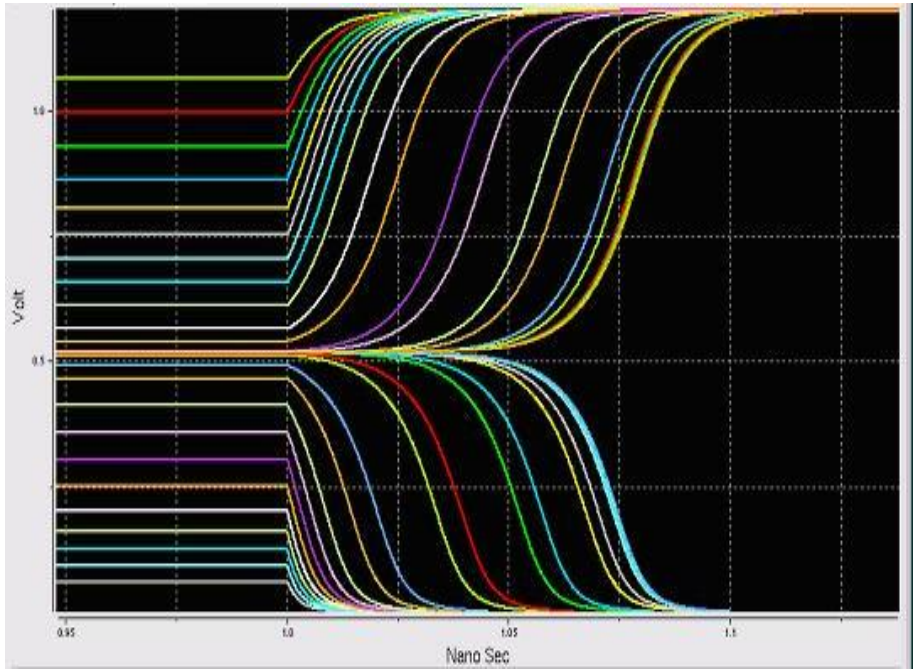
Non-deterministic resolution



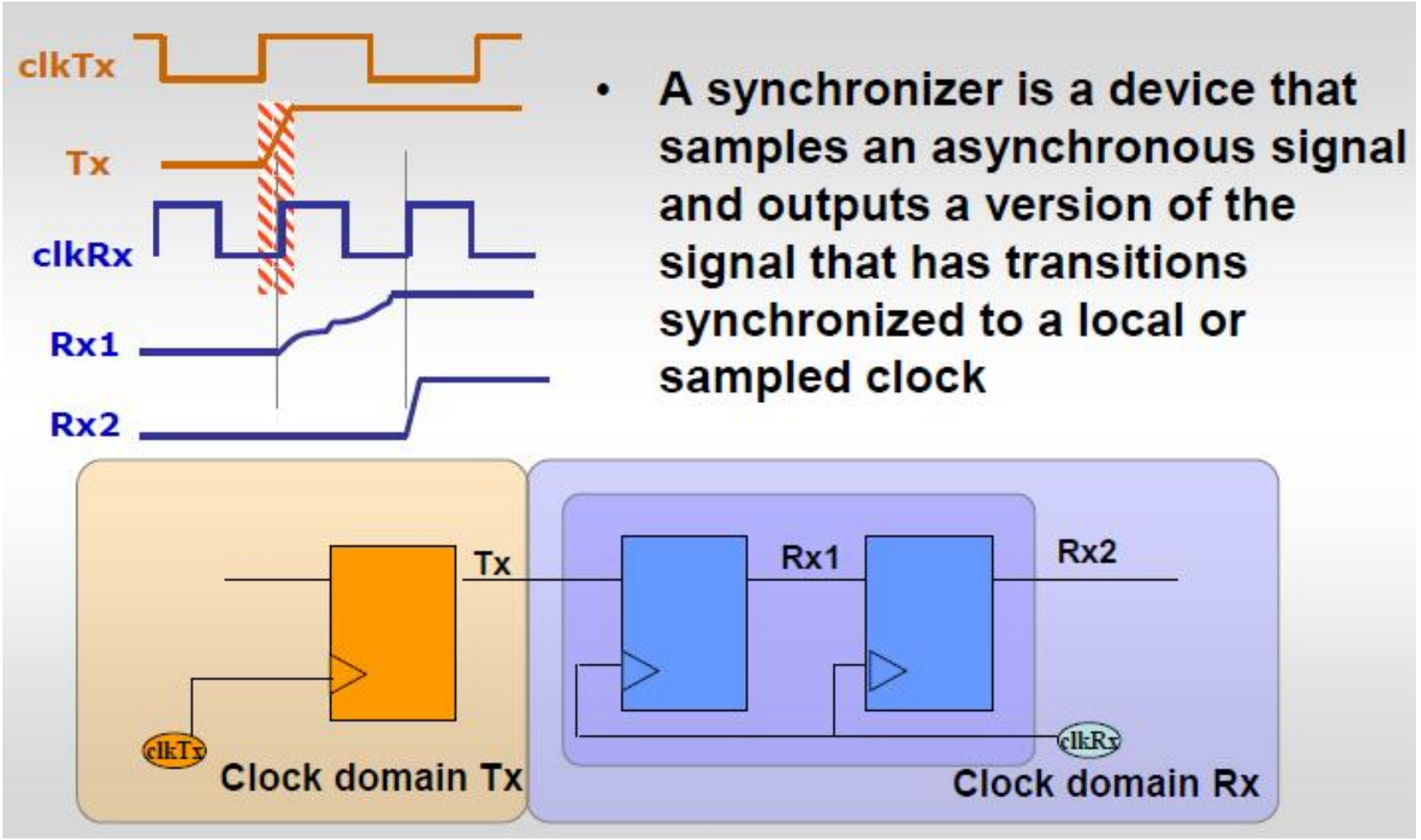
Metastability Time

Effect factors:

- Process
- Temperature
- Voltage Sampled
- Electromagnetic wave



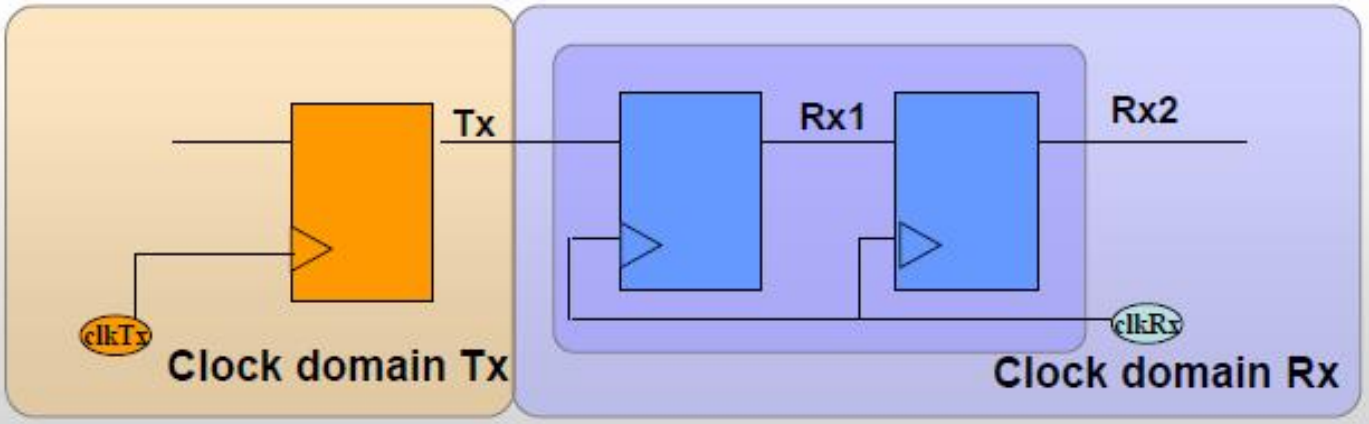
How to tolerate metastability?



MTBF: Mean Time Between Failure

$$MTBF = \frac{\Sigma\,(\text{Up Time})}{\text{Number of Failures}} \cong \frac{e^{T/\tau}}{f_d \times f_c \times T_w}$$

- T = settling window
- τ = setting constant of flop
- Tw = parameter related to the time window of susceptibility
- f_d = rate of input data change
- f_c = frequency of receiving clock

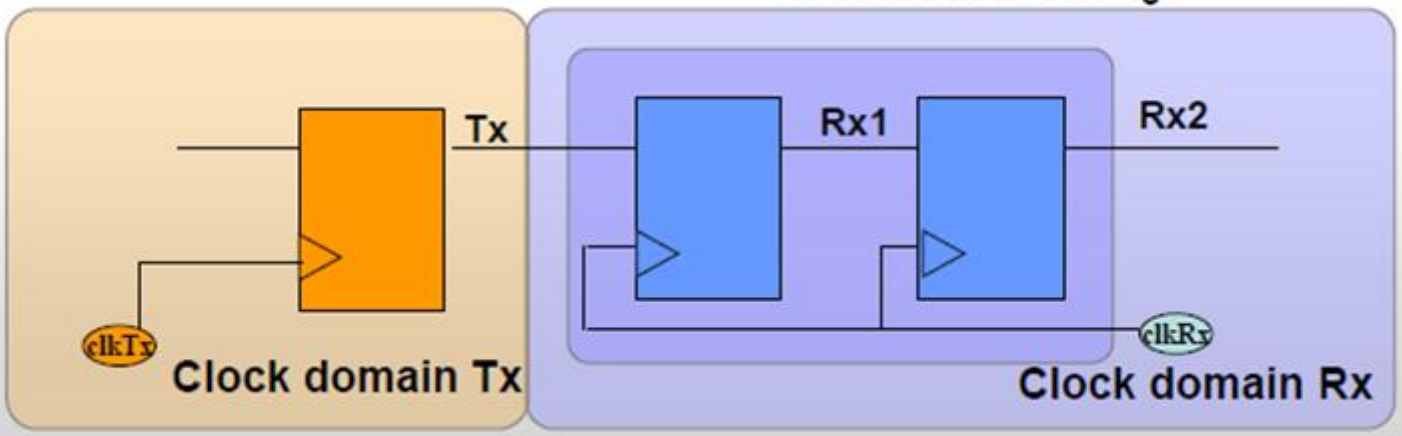


MTBF example

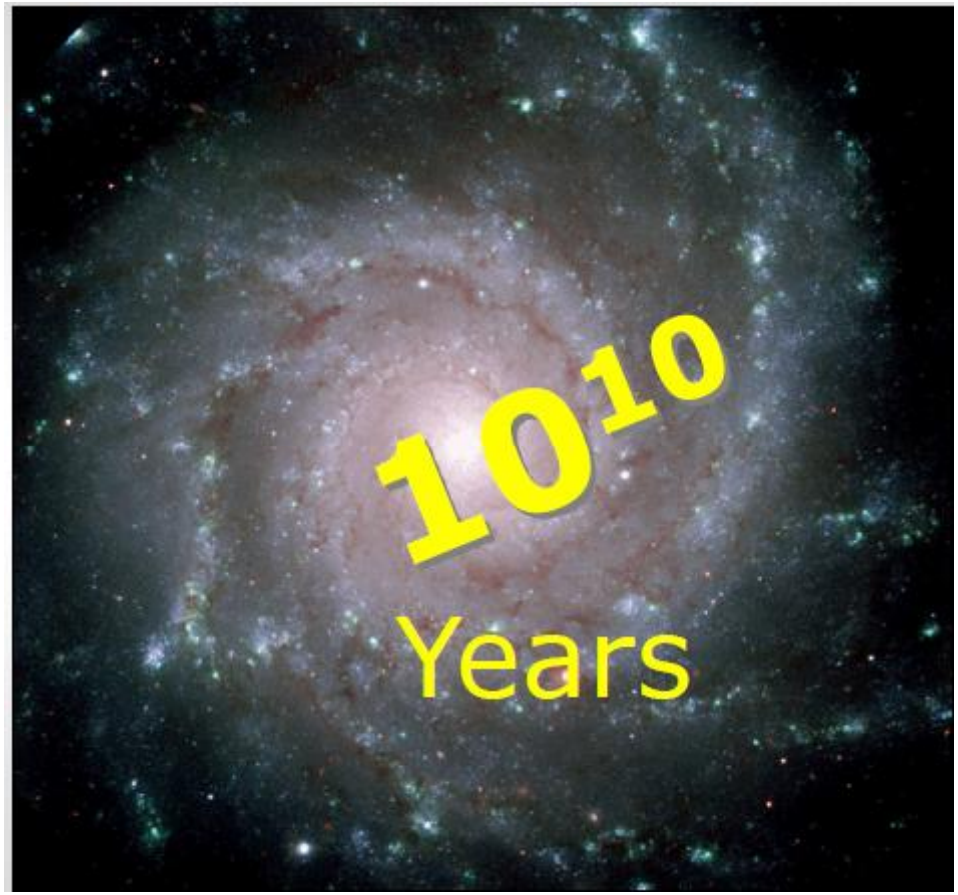
$$MTBF = \frac{e^{500}}{2 \times 10^{-5}}$$

10^{204} years

- τ = 10ps setting constant of flop
- T_w = 50ps parameter related to the time window of susceptibility
- f_c = 200 MHz
- f_d = 20 MHz
- T settling window obviously derived from f_c



Synchronizer Reliability



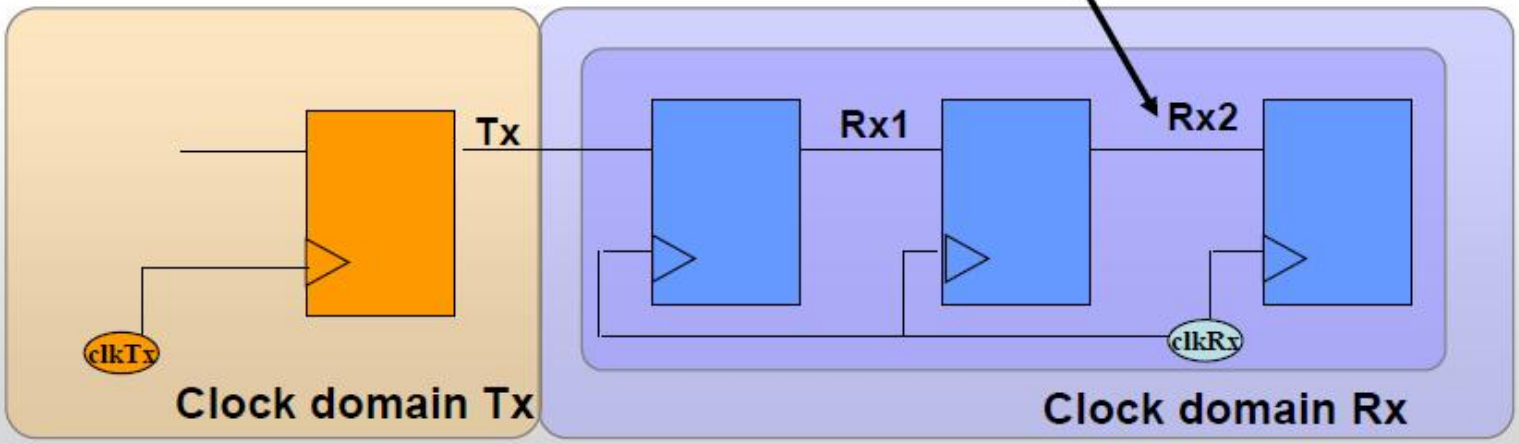
Synchronizer Reliability

$$MTBF \cong \frac{e^{T/\tau}}{f_d \times f_c \times T_w} + \frac{e^{T/\tau}}{f_d \times f_c \times T_w} \cdots$$

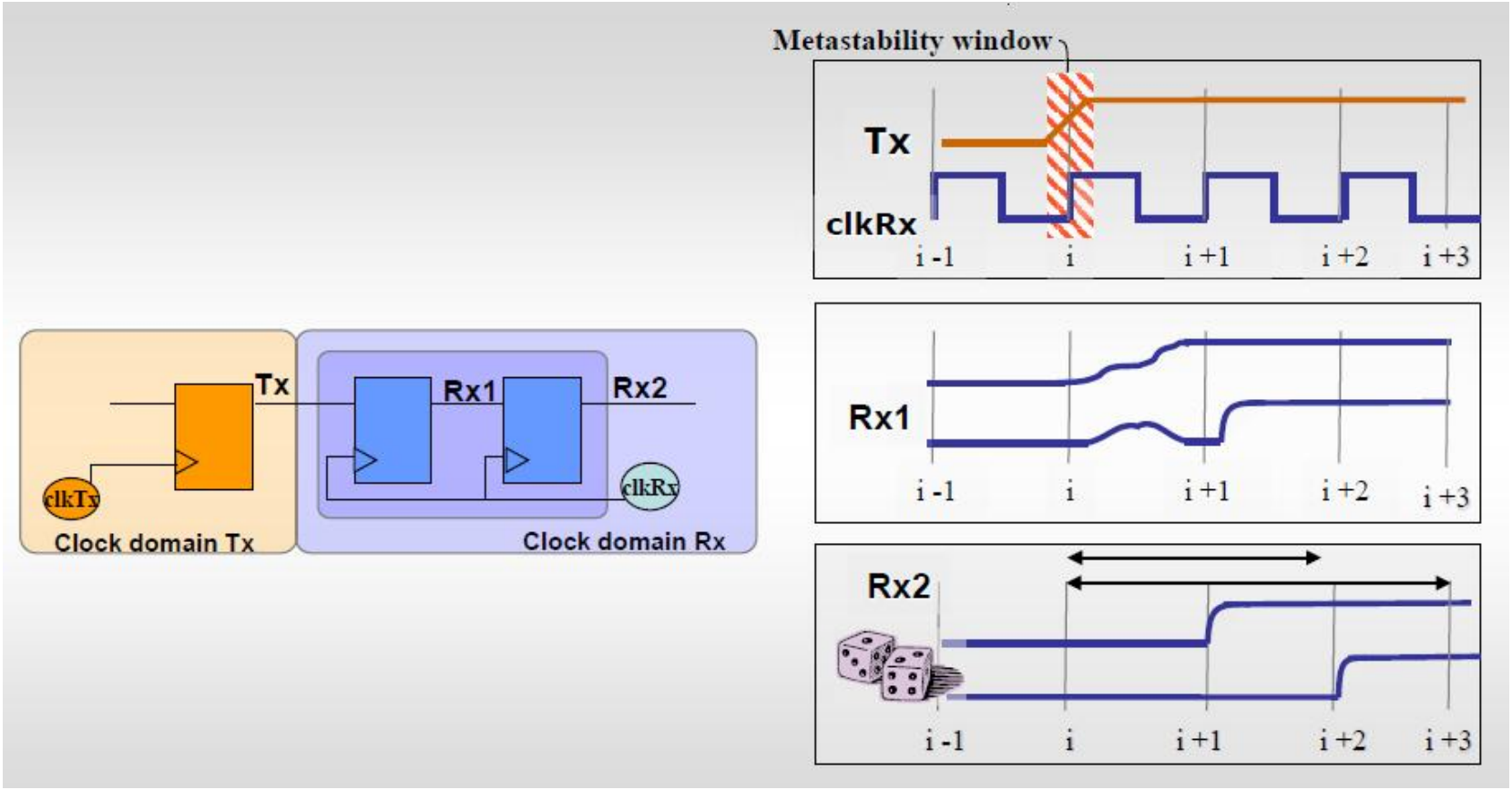
T = settling window

τ = setting constant of flop

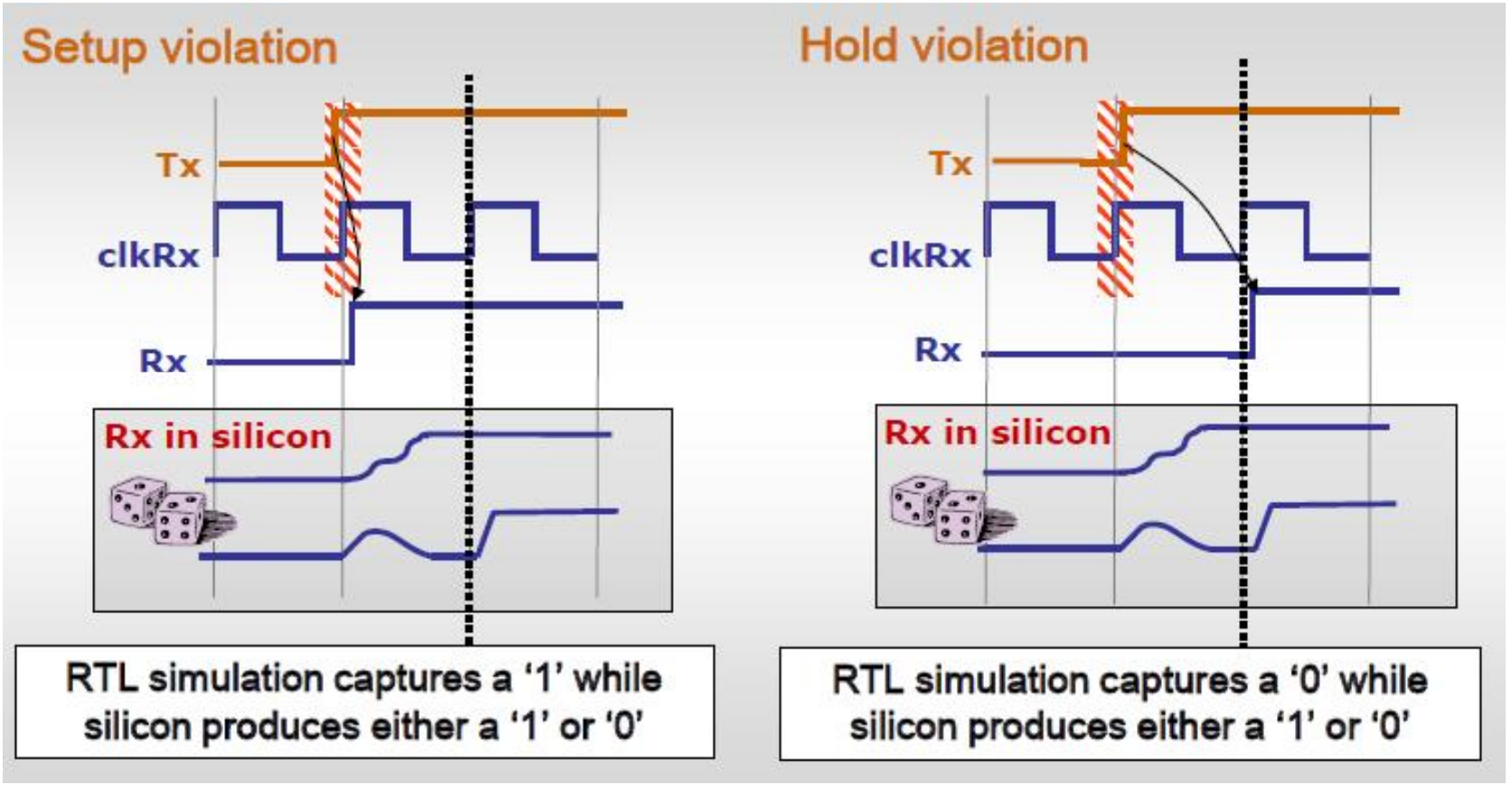
$\cong 10^{408}$



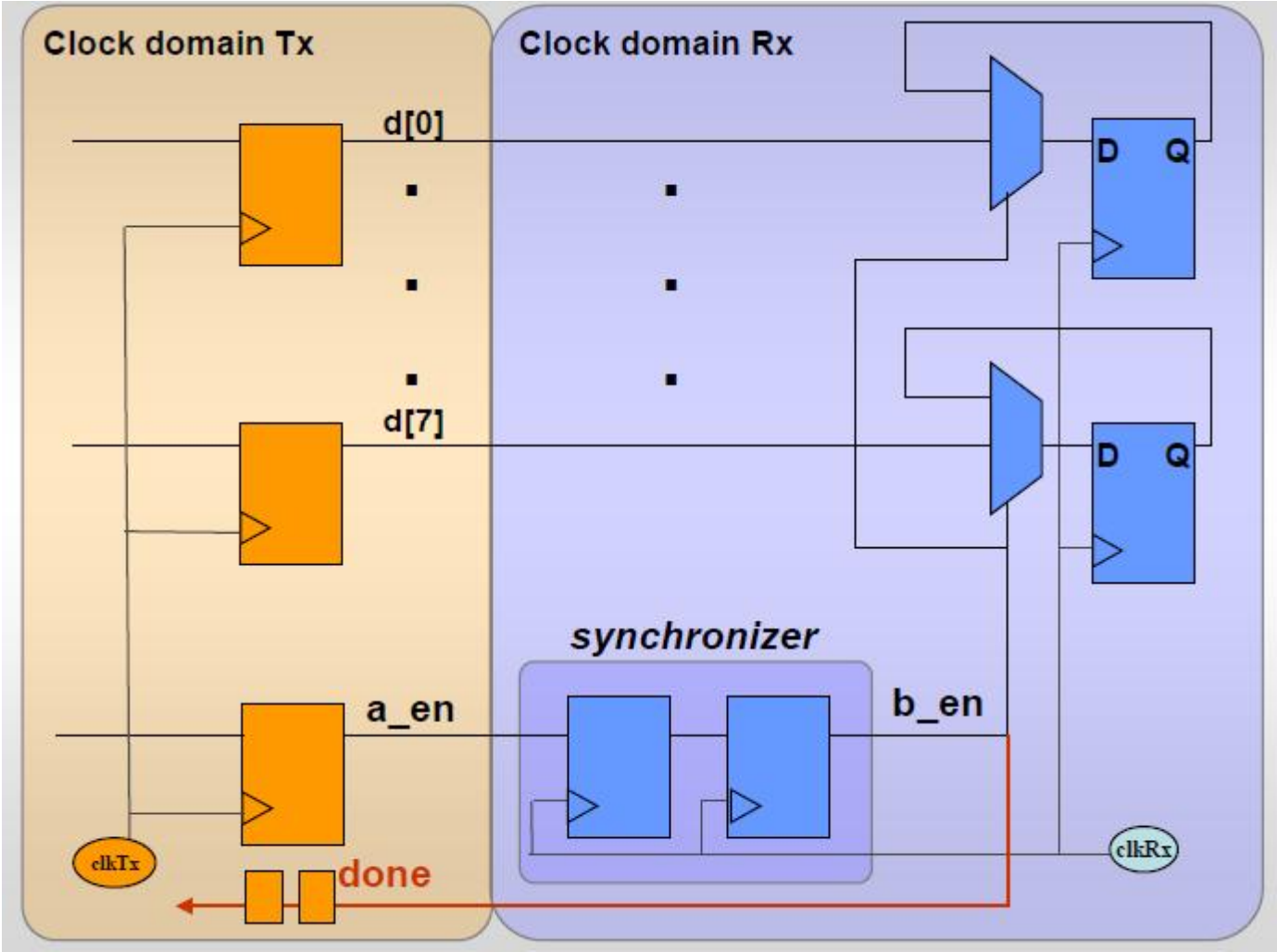
Synchronizer effect – latency uncertainty



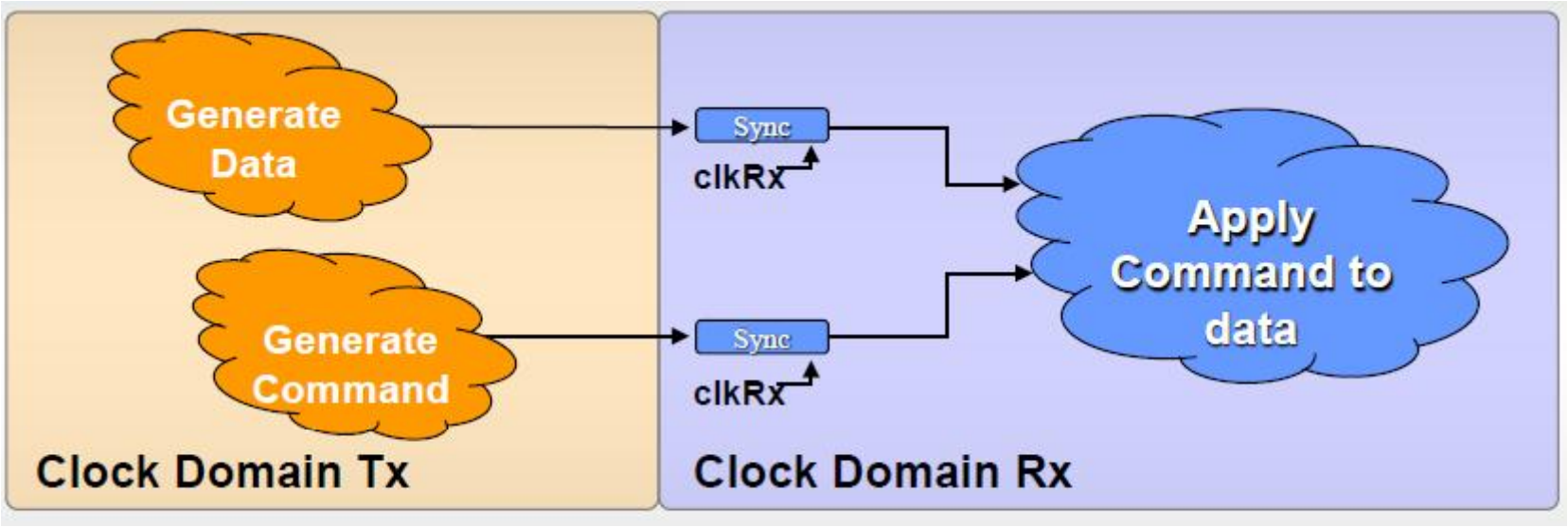
RTL simulation does not model silicon behavior accurately



Synchronizing multiple data bits

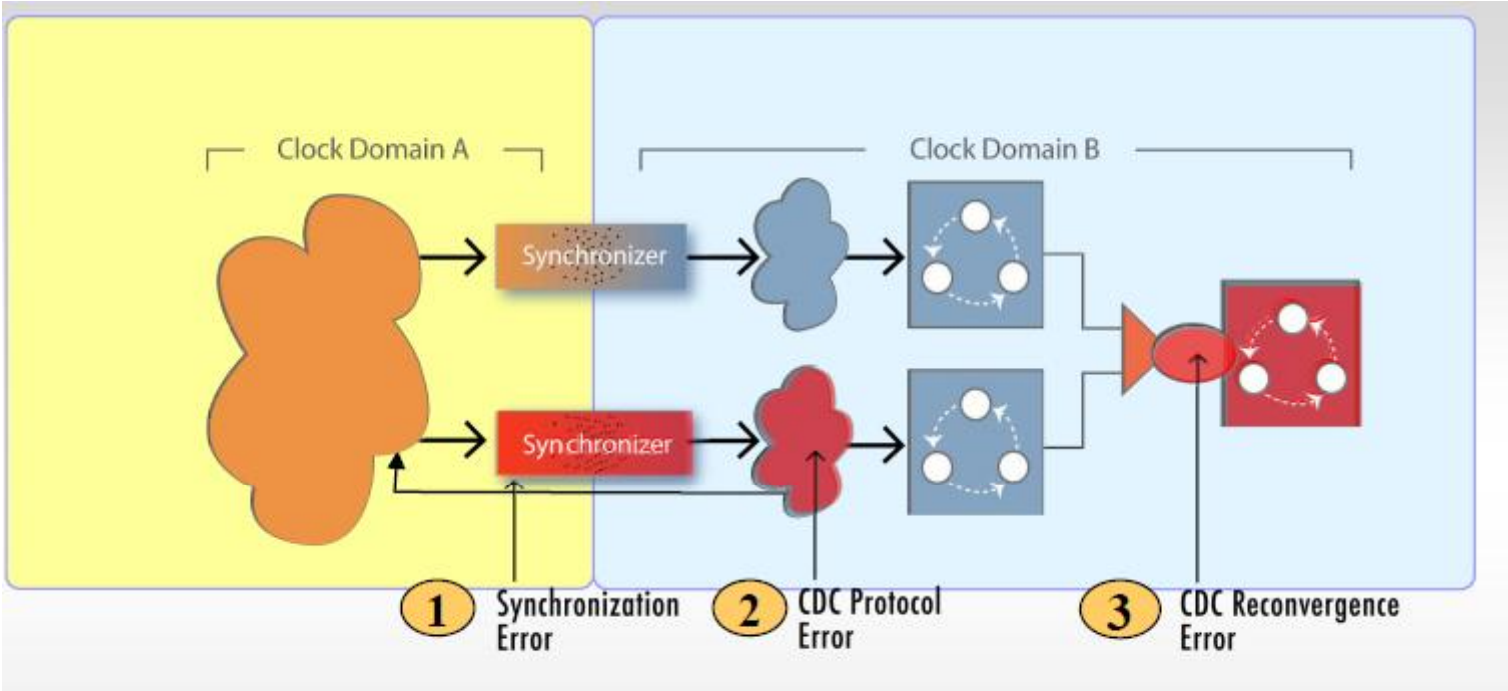


Reconvergence Problem



- Assume two signals must be mutually exclusive
- Cannot guarantee that the signals received in the Rx clock domain will be mutually exclusive!

CDC Verification Solution



1. Static analysis to identify synchronization errors
2. Protocol assertion generation to ensure correct transfer of data
3. Reconvergence verification with metastability injection

Any questions ?

Thank you !