A MISMATCH INSENSITIVE CMOS DYNAMIC COMPARATOR FOR PIPELINE A/D CONVERTERS

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ABSTRACT

A new fully differential CMOS dynamic comparator topology suitable for pipeline A/D converters with a low stage resolution is proposed. A thorough analysis of its function and a comparison to a widely used dynamic comparator [1] are given in this paper. The proposed topology, based on two cross coupled differential pairs and switchable current sources, has a small power and area dissipation and it is shown to be very robust against transistor mismatch.

1. INTRODUCTION

The main benefits of the pipeline A/D converter architecture are its capability to a high resolution and very large bandwidth with low power consumption in a small area. This is achieved by cascading stages of 1 to 3 bits resolution working concurrently [1]-[2]. The comparator forms the core of the sub-ADCs, which are usually flash A/D converters, of such pipeline ADC stages. The design of the comparator has an essential effect on the ADC accuracy and power consumption. The comparator offset is not so critical a parameter because of the commonly used Redundant Sign Digit (RSD) digital correction algorithm, which can tolerate comparator offset voltages up to $\pm V_{ref}/2^b$ for a b-bit stage when the reference voltage is V_{ref} [2]. Even for a low supply voltage design this is usually in the order of hundreds of millivolts if $b \leq 3$. This allows the use of dynamic comparators without any continuous time pre-amplification, which reduces the power dissipation considerably. In spite of the loose offset specification this requirement might become a limiting factor without careful consideration of all possible mismatches.

The most important comparator specifications are offset, power consumption and immunity to noise and mismatches. In a mixed mode circuit, which an ADC always is, fully differential analog signals are preferred to get a better power supply rejection and immunity to common mode noise. This implies that also the comparator should be fully differential — even with differential reference voltages. Into great extent the comparator offset is in turn due to transistor mismatch, which indicates that the comparator topology should be robust for matching. A very low power dissipation can be obtained with dynamic comparators, which are turned off when they are inactive. Such comparator topologies have inevitably fairly large offset voltages, because no static pre-amplification exists in the front of a latch part. Nevertheless, due to their low power dissipation the use of these dynamic comparators is preferred whenever possible.

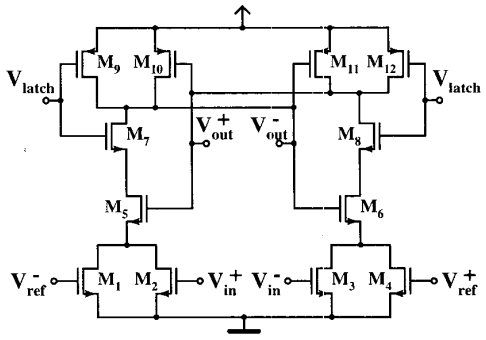

Figure 1: Lewis-Gray comparator.

In the next chapter the function and matching properties of the commonly used 'Lewis-Gray' comparator are described. In chapter 3 a new comparator topology based on two cross coupled differential pairs is introduced. Its operation and inherit robustness against transistor mismatches are described and the theory is verified with simulations in chapter 4.

2. LEWIS-GRAY COMPARATOR

A widely used dynamic comparator in pipeline A/D converters is based on a differential sensing amplifier used in static RAM's. This so called 'Lewis-Gray' dynamic comparator, presented in Fig. 1, was introduced in [1]. The main advantages of this circuit are its zero DC power consumption and a linear built-in threshold adjusting circuit. Transistors M_1 - M_4 adjust the threshold and above them transistors M_5 - M_{12} form a latch.

The operation of the comparator is as follows. When

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the latch control signal is low ($V_{latch} = 0V$) the transistors M_9 and M_{12} are conducting and M_7 and M_8 are cut off, which forces both differential outputs to V_{dd} and no current path exists between the supply voltages. Simultaneously M_{10} and M_{11} are cut off and the transistors M_5 and M_6 conduct. This implies that M_7 and M_8 have a voltage of V_{dd} over them. When the comparator is latched the control signal goes up ($V_{latch} = V_{dd}$), which turns M_7 and M_8 on. Immediately after the switching moment the gates of the transistors M_5 and M_6 are still at V_{dd} and they enter saturation. If all transistors M_5 - M_{12} are assumed to be perfectly matched the imbalance of the conductances of the left and right input branches, formed by M_1 - M_2 and M_3 - M_4, determines which of the outputs goes to V_{dd} and which to $0V$. After a static situation is reached when $V_{latch} = V_{dd}$, both branches are cut off and the outputs preserve their values until the comparator is reseted again by switching V_{latch} to $0V$.

The transistors connected to the input and reference ($M_1 - M_4$) are in the triode region and act like voltage controlled resistors. If no mismatch is present the comparator changes its output when the conductances of the left and right input branches are equal $g_L = g_R$. By denoting $W_A = W_2 = W_4$ and $W_B = W_1 = W_3$ the input voltage where the comparator changes the state is [1]:

$$V_{in}^{+} - V_{in}^{-} = \frac{W_B}{W_A}\left(V_{ref}^{+} - V_{ref}^{-}\right) \qquad (1)$$

By dimensioning of the transistor widths W_A and W_B the threshold of the comparator can be adjusted to the desired level.

Eq. (1) implies that the offset of the comparator depends on the mismatch of transistors M_1 - M_4. This is true only when all other transistors M_5 - M_{12} are assumed to match perfectly. The transconductance of the transistors M_1 - M_4 operating in the linear region can be approximately written:

$$g_{m1,2,3,4} = \mu_0 C_{ox} \frac{W_{1,2,3,4}}{L} V_{ds1,2,3,4} \qquad (2)$$

where $V_{ds1,2,3,4}$ is the drain-source voltage of the corresponding transistor. For the transistors M_5 - M_6 the transconductance can be written:

$$g_{m5,6} = \mu_0 C_{ox} \frac{W_{5,6}}{L} \left(V_{gs5,6} - V_T\right) \qquad (3)$$

where V_T is the threshold voltage and $V_{gs5,6}$ are the corresponding gate-source voltages of transistors M_5 and M_6. At the beginning of the latching process $V_{ds1,2,3,4} \approx 0$ while $V_{gs5,6} - V_T \approx V_{dd}$. The magnitude of the transconductances g_{m5} and g_{m6} is thus much larger than the conductances of the left and right input branches, which makes it dominant in determining the latching balance. Any mismatch between the transistors M_5 and M_6 causes large offset voltages. In order to minimize power and area consumption almost minimum size transistors are preferred, which easily results in offset voltages of a few hundred millivolts. In addition to that transistors M_5 and M_6 amplify the mismatches of the input transistors M_1 - M_4. Mismatches in transistors M_7 - M_{12} are attenuated by the gain of M_5 and M_6 and are thus not so critical for the offset voltage.

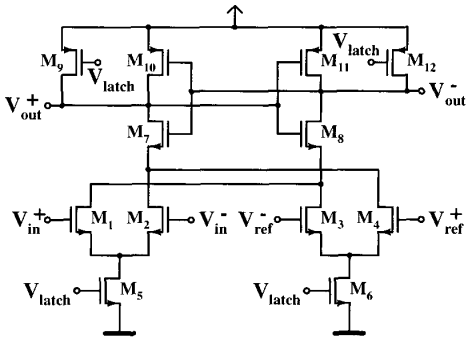

Figure 2: Differential pair comparator.

To scope with the mismatch problem the layout of the critical transistors must be drawn as symmetric as possible. In addition to the mismatch sensitivity the latch is also very sensitive to an asymmetry in the load capacitance. This can be avoided by adding an extra latch or inverters as a buffering stage after the comparator core outputs. The conductances of the branches depend also from the common mode voltage of the input and reference voltages: the lower the common mode voltage the larger the conductances g_L and g_R are.

3. PROPOSED DIFFERENTIAL PAIR COMPARATOR

In order to make a dynamic comparator more robust against mismatch and process variations all transistors should be in saturation straight after the latching signal. A fully differential dynamic comparator based on two differently sized cross coupled differential pairs, shown in Fig. 2, was developed based on the comparator described in [4]. In this proposed new topology the current sources are switchable and the latch circuit is connected directly between the source coupled pairs and the supply voltage.

3.1. Operation of the Comparator

The operation of the comparator is as follows. When the comparator is inactive the latch signal V_{latch} is at $0V$, which means that the current source transistors M_5 and M_6 are switched off and no current path between the supply voltages exists. Simultaneously the PMOS switch transistors M_9 and M_{12} reset the outputs by shorting them to V_{dd}. The NMOS transistors M_7 and M_8 of the latch conduct and force also the drains of all the input transistors M_1 - M_4 to V_{dd} potential. When V_{latch} is

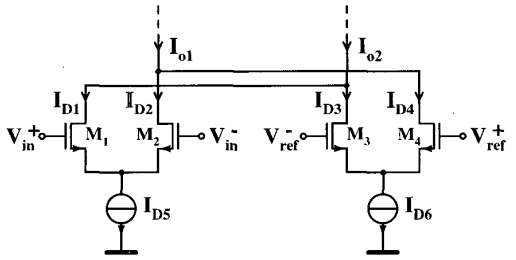

Figure 3: Simplified model of the differential pair comparator.

risen to V_{dd} the outputs are disconnected from the positive supply and the switching current sources M_5 and M_6 enter saturation and begin to conduct. These two transistors determine the bias currents of the two differential pairs M_1 - M_2 and M_3 - M_4, respectively. The threshold voltage of the comparator is determined by the current division in the differential pairs and between the cross coupled branches.

The determination of the switching point of the comparator can be modeled with the simplification of Fig.3 for the two cross coupled differential pairs. Using the symbols indicated in the figure and having $W_1 = W_2$, $W_3 = W_4$ the transistors M_1 - M_4 follow the large signal current equations:

$$I_{D1} - I_{D2} = \beta_1 V_{in} \sqrt{\frac{2I_{D5}}{\beta_1} - V_{in}^2} \qquad (4)$$

$$I_{D4} - I_{D3} = \beta_3 V_{ref} \sqrt{\frac{2I_{D6}}{\beta_3} - V_{ref}^2} \qquad (5)$$

where $\beta_i = \frac{1}{2}K'\frac{W_i}{L} = \frac{1}{2}\mu_0 C_{ox}\frac{W_i}{L}$, $V_{in} = V_{in}^+ - V_{in}^-$ and $V_{ref} = V_{ref}^+ - V_{ref}^-$. The comparator changes its stage when the currents I_{o1} and I_{o2} of the both output branches are equal. Assuming the relation of the source coupled pair bias currents to be $I_{D5} = d \cdot I_{D6}$ and by marking the threshold point with parameter e so that $V_{in} = e \cdot V_{ref}$, this results in a condition:

$$2de^2 I_{D6}\frac{W_1}{L} - K'e^4 V_{ref}^2 \left(\frac{W_1}{L}\right)^2 = 2I_{D6}\frac{W_3}{L} - K'V_{ref}^2\left(\frac{W_3}{L}\right)^2 \qquad (6)$$

When the parameters d and e are chosen according to the wanted threshold point of the comparator, the transistor dimensions W_1 and W_3 can be interpolated from Eq. (6). The comparator is used in a 10-bit 200 MS/s parallel pipeline A/D converter [3].

3.2. Effect of the Transistor Mismatch

It can be concluded that as there are terms dependent on the transistor dimensions with different signs in both sides of the Eq. (6), transistor mismatches are partly canceled, which makes the topology robust.

As mentioned above the comparator core consists of two differential pairs. This can be exploited when calculating the comparator offset voltage. The total offset voltage of the comparator consists of the sum of the offsets of both source coupled pairs. The offset of one differential pair has the well known dependency on the mismatch of the threshold voltage ΔV_T, load resistance ΔR_L and transistor dimensions $\Delta\beta$ and their corresponding average values (V_T, R_L, β):

$$V_{os} = \Delta V_T + \frac{V_{gs} - V_T}{2}\left(\frac{\Delta R_L}{R_L} + \frac{\Delta\beta}{\beta}\right) \qquad (7)$$

The offset voltage is in this case dominated by the mismatch of the transistor dimensions $\Delta\beta$, which suggests that the lower the common mode voltage (V_{gs} low) the smaller the offset.

The effect of the mismatches of the other transistors M_7 - M_{12} is in this comparator topology not very critical. The drain nodes of the cross coupled differential pairs are high impedance nodes and the transconductances of the threshold voltage determining transistors M_1 - M_4 large.

Table 1: Transistor dimensions.

	Lewis-Gray		Diff. pair	
Trans.	W [μm]	L [μm]	W [μm]	L [μm]
M_1	5.0	1.0	15.0	1.0
M_2	20.0	1.0	15.0	1.0
M_3	20.0	1.0	5.2	1.0
M_4	5.0	1.0	5.2	1.0
M_5	3.0	0.5	16.0	1.0
M_6	3.0	0.5	4.0	1.0
M_7	3.0	0.5	4.0	0.5
M_8	3.0	0.5	4.0	0.5
M_9	8.0	0.5	5.0	0.5
M_{10}	8.0	0.5	8.0	0.5
M_{11}	8.0	0.5	8.0	0.5
M_{12}	8.0	0.5	5.0	0.5

4. SIMULATION RESULTS

The performance of the proposed differential pair comparator was verified and compared to that of the 'Lewis-Gray' comparator by simulations using a standard 0.5-μm CMOS process parameters. Transistors are dimensioned so that the area of both comparators are in the same size range and the input and current source transistors have a channel length L=1.0 μm. The supply voltage was 3.0 V and a signal swing of 1.6 $V_{pp,diff}$ was assumed with a common mode voltage of 1.5 V giving $V_{ref}^- = 1.1$ V and $V_{ref}^+ = 1.9$ V. The comparator threshold levels are set with the input transistor dimensioning to $V_{in} = \frac{1}{4}V_{ref}$ corresponding to the situation in a 1.5-

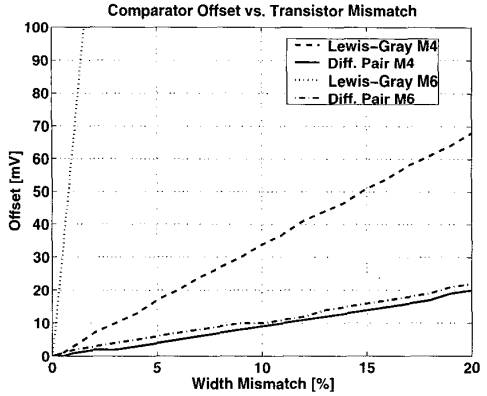

Figure 4: Offset as a function of the transistor mismatch.

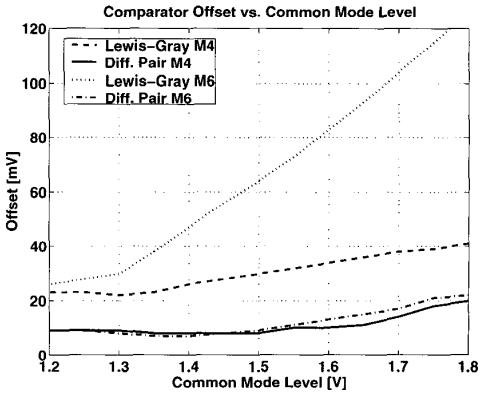

Figure 5: Offset as a function of the common mode voltage.

bit ($b = 2$) pipeline stage with a resistor string sub-ADC. The transistor dimensions are presented in Tab. 1.

In Fig. 4 the change in the comparator threshold voltage is plotted as a function of one transistor mismatch at a time while all the others are left perfectly matched. For both comparators the mismatch of the widths ($\frac{\Delta W}{W}$) of the two most critical transistors are given, M_4 and M_6 for the 'Lewis-Gray' comparator and M_4 and M_6 for the proposed differential pair comparator. The former seems to be very sensitive especially to the mismatch of the transistor M_6, which causes an offset of 195 mV for a width deviation of 3 %. On the other hand the proposed new comparator has an offset less than 22 mV for transistor mismatches up to 20 %. It can also be seen that M_4 and M_6 have an almost identical effect on the offset voltage.

The effect of the common mode voltage level is illustrated in Fig. 5. The offset voltage is plotted as a function of the common mode voltage of V_{in} and V_{ref} for both comparators for the same transistors as above. The mismatch of the widths is kept at 9.0 % for M_4 and 1.0 % for M_6 in the Lewis-Gray comparator and at 9.0 % for M_4 and M_6 in the differential pair comparator. The offset of the former topology decreases significantly with the common mode voltage. The dependency is linear down to 1.3 V. The differential pair comparator shows an almost constant offset for the whole operation range of the input pairs.

Power dissipation and area of the two comparators differ very little from each other. Both topologies have twelve transistors, the size of which are in the same range. Simulated current consumption at 200 MHz clock rate to a 20 pF load for the Lewis-Gray and differential pair comparators are 268 μA and 279 μA, respectively.

5. CONCLUSIONS

In this paper a new mismatch insensitive dynamic comparator was proposed. It consists of two cross coupled , switchable current source differential pairs loaded with a CMOS latch. The threshold voltage of the comparator can be adjusted with the dimensions of the input and current source transistors. The proposed topology utilizes low power and small area and is inherently very insensitive to transistor mismatch.

6. REFERENCES

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