Integrated Circuits for Analog Signal Processing

Esteban Tlelo-Cuautle
Editor

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Springer

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Esteban Tlelo-Cuautle
INAOE
Luis Enrique Erro No. 1.
Tonantzintla
Mexico

ISBN 978-1-4614-1382-0 ISBN 978-1-4614-1383-7 (eBook)
DOI 10.1007/978-1-4614-1383-7
Springer New York Heidelberg Dordrecht London

Library of Congress Control Number: 2012938259

Printed on acid-free paper

Springer is part of Springer Science+Business Media (www.springer.com)

Preface

Analog integrated circuits encounter applications in signal amplification, filtering, data acquisition systems, sensor conditioning, biomedical implants, actuator conditioning, oscillators, mixers, and so on. Those applications are possible, thanks to the availability of a huge plethora of active devices/elements, and thanks to the appropriate exploitation of their electrical characteristics. For instance, active devices can be classified according to the kind of signal (voltage/current) and port characteristics. Some examples are: voltage operational amplifier, current operational amplifier, operational transconductance amplifier, operational transresistance amplifier, current conveyor, current differencing transconductance amplifier, and so on. In this manner, this book collects recent theories and design methods and applications of active devices/elements (working in voltage-, current-, and/or mixed-mode) and summarizes challenges imposed by the nanometer technology.

The book consists of 13 chapters focused on: analysis, design, and optimization of active devices; nullors, their bipolar and CMOS implementations and applications in analog circuit synthesis and design; current feedback op-amps, their variants, integratable implementations and applications in analog signal processing; generation of grounded capacitors minimumcomponent oscillators; active filter design using a two-graph based transformation technique; analog baseband filter design considerations for wireless receivers; flexible nanometer CMOS low-noise amplifiers for the next-generation software-defined-radio, mobile systems; clocked nanometer CMOS comparators; low-power electronics for biomedical sensors; sensor conditioning circuits; steady-state simulation of mixed analog/digital circuits; variability-aware optimization of RF integrated inductors in nanometer-scale technologies; and a survey on the static and dynamic translinear paradigm.

The topics covered in this book are intended for people in academy and industry, as well as a key guidance for students and practitioners in the very wide field of analog integrated circuits.

Contents

Contributors

Edwin C. Becerra-Alvarez CUCEI, University of Guadalajara, Guadalajara, México

D. R. Bhaskar Department of Electronics and Communication Engineering, Jamia Millia Islamia, New Delhi, India

Federico Bizzarri Dipartimento di Elettronica e Informazione, Politecnico di Milano, pza. Leonardo da Vinci, Milano, Italy

Angelo Brambilla Dipartimento di Elettronica e Informazione, Politecnico di Milano, pza. Leonardo da Vinci, Milano, Italy

Fernando Coito DEE, Faculdade de Ciências e Tecnologia, UNL, Caparica, Portugal

Carlos A. De La Cruz Blas Departamento de Ingeniería Eléctrica y Electrónica, Universidad Pública de Navarra, España, CP, Spain

José M. de la Rosa IMSE-CNM, CSIC/University of Seville, Seville, Spain

Miguel Aurelio Duarte Villaseñor INAOE, Tonantzintla, Puebla, México

Mourad Fakhfakh University of Sfax, Sfax, Tunisia

Helena Fino DEE, Faculdade de Ciências e Tecnologia, UNL, Caparica, Portugal

Giancarlo Storti Gajani Dipartimento di Elettronica e Informazione, Politecnico di Milano, pza. Leonardo da Vinci, Milano, Italy

Bernhard Goll Vienna University of Technology, EMCE, Vienna, Austria

Giambattista Gruosso Dipartimento di Elettronica e Informazione, Politecnico di Milano, pza. Leonardo da Vinci, Milano, Italy

Ivick Guerra-Gómez INAOE, Tonantzintla, Puebla, Mexico

S. S. Gupta Department of Industrial policy and promotion, Ministry of Commerce and Industry, New Delhi, Government of India

Julia Hsin-Lin Lu Purdue University, West Lafayette, IN, USA

Byunghoo Jung Purdue University, West Lafayette, IN, USA

Syed Kamrul Islam The University of Tennessee, Knoxville, TN, USA

Raghavendra Kulkarni Texas A&M University, College Station, TX, USA

Pragati Kumar Department of Electrical Engineering, Delhi Technological University, New Delhi, India

Pedro Pereira DEE, Faculdade de Ciências e Tecnologia, UNL, Caparica, Portugal

Marian Pierzchala Wroclaw University of Technology, Wroclaw, Poland

Melika Roknsharifi The University of Tennessee, Knoxville, TN, USA

Carlos Sánchez-López Universidad Autónoma de Tlaxcala, Tlaxcala, México

Federico Sandoval-Ibarra Cinvestav-Unidad Guadalajara, Guadalajara, México

Raj Senani Division of Electronics and Communication Engineering, Netaji Subhas Institute of Technology, New Delhi, India

Fahmida Shaheen Tulip The University of Tennessee, Knoxville, TN, USA

R. K. Sharma Department of Electronics and Communication Engineering, Ambedakar Institute of Technology, New Delhi, India

Jose Silva-Martinez Texas A&M University, College Station, TX, USA

A. K. Singh Department of Electronics and Communication Engineering, ITS Engineering College, Greater Noida, India

V. K. Singh Department of Electronics Engineering, Institute of Engineering & Technology, Lucknow, UP, India

A.M. Soliman Department of Electronics and Communication Engineering, Cairo University, Giza, Egypt

Esteban Tlelo-Cuautle INAOE, Tonantzintla, Puebla, México

Rafael Vargas-Bernal Departamento de Ingeniería en Materiales, Instituto Tecnológico Superior de Irapuato, Guanajuato, México

Kai Zhu The University of Tennessee, Knoxville, TN, USA

Horst Zimmermann Vienna University of Technology, EMCE, Vienna, Austria

Chapter 1
Analysis, Design and Optimization of Active Devices

I. Guerra-Gómez, E. Tlelo-Cuautle, M.A. Duarte-Villaseñor, and C. Sánchez-López

1.1 Introduction

This chapter describes three computational techniques for the design automation of analog integrated circuits (ICs): Symbolic nodal analysis using the nullor concept and pathological elements, systematic design of active devices from a binary genetic encoding approach, and circuit biasing and sizing by applying evolutionary algorithms.

Symbolic analysis techniques are very useful in generating analytical expressions of analog ICs. Their main characteristics can be identified by the kind of models they use. For instance, in the case of symbolic nodal analysis techniques, the use of active devices models based on pathological elements has demonstrated advantages in the formulation of small and sparse matrices [1]. In fact, using the pathological elements accompanied of passive circuit elements, e.g. resistances, one can model the behavior of almost all active devices, as already shown in [1–3]. It is also possible to include parasitic circuit elements into the models [4], and performances characteristics such as input and output impedances and gain [5].

In performing symbolic analysis one is interested in generating exact or approximated symbolic expressions [6]. However, using detailed models of active devices, the generated expressions can be too large, while by using compact models the expression may be very compact or reduced. In both cases, the generated symbolic expression approximates the exact response with some error tolerance [7, 8]. To generate compact expressions, a big circuit can be partitioned so that some blocks

I. Guerra-Gómez (✉) • E. Tlelo-Cuautle • M.A. Duarte-Villaseñor
INAOE, Tonantzintla, México
e-mail: ivickguerra@gmail.com; etlelo@inaoep.mx; miauduvi@gmail.com

C. Sánchez-López
Universidad Autónoma de Tlaxcala, Tlaxcala, México,
e-mail: carlsanmx@yahoo.com.mx

E. Tlelo-Cuautle (ed.), *Integrated Circuits for Analog Signal Processing*,
DOI 10.1007/978-1-4614-1383-7_1,

can be replaced by their dominant characteristics, and the symbolic analysis is accelerated by applying determinant decision diagrams (DDD) [9], and parallel DDD-based analysis [10]. For instance, in [5] is presented the symbolic nodal analysis of ICs containing current mirrors (CMs). The nullor-equivalent of the CM is very useful in formulating a reduced system of equations, as shown in the following section by performing symbolic nodal analysis of an all-pole third-order low-pass filter implemented with dual-output CMs [11]. Symbolic nodal analysis can also be applied in the synthesis of analog ICs through deriving performance-analytical-expressions of the active devices [6].

Recently, a binary genetic encoding (BGE) representation for the automatic synthesis of mixed-mode circuit topologies was introduced in [12]. The chromosomal representation of the four unity-gain cells was generated from nullator/norator descriptions, and the binary strings are represented by hexadecimal numbers in order to have a unique meaning when they are decoded to create transistor-based circuits. In Sect. 1.3, a summary on the synthesis of the voltage and current followers, and voltage and current mirros, is presented. The synthesis of more complex active devices is also described by combining and/or superimposing unity-gain cells. This kind of synthesis methodology is part of evolutionary electronics, because this research area involves applications of evolutionary computation in the domain of electronics. On this direction, analog design is much amenable for evolutionary techniques, because contrasting with the digital design, there is no solid set of design rules or procedures to automate circuit synthesis. For instance, analog synthesis begins by selecting a specific topology and its design is performed by finding parameter values (e.g. transistor lengths and widths). Furthermore, to have an idea among all the currently available design methodologies, a classification of design strategies developed by researchers in recent history over more than 20 years is presented in [13]. That way, yet there is a founded interest in the development of automatic techniques capable to find new circuit topologies and optimum component values.

In general, the design of analog ICs requires the use of different kinds of active devices, as the ones summarized in [1,4,14]. Moreover, to improve the performances of those analog ICs, optimized active devices are required. In this manner, Sect. 1.4 summarizes the application of three evolutionary algorithms to compute the biases and sizes of analog ICs. That way, several active devices are optimized taking into account design constraints, and linking HSPICE^{TM} like circuit simulator to evaluate electrical characteristics.

1.2 Symbolic Nodal Analysis

This section summarizes several models of active devices using the nullor concept and pathological elements [1, 4, 5]. Those models are used to derive symbolic expressions of analog ICs.

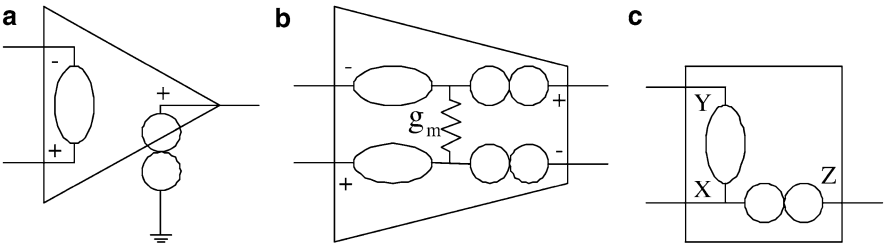


Fig. 1.1 (**a**) Operational amplifier, (**b**) operational transconductance amplifier, and (**c**) negative-type second generation current conveyor modeled by using nullors

1.2.1 Modeling Active Devices Using Nullors and Pathological Elements

The symbolic behavioral model generation of analog ICs can be found in [1, 4–6], where it is demonstrated that when using nullors and/or pathological elements, one not only can describe the dominant behavior of analog ICs, but also one can add or remove parasitic elements to generate models at different abstraction levels. The transfer relationships of the models are expressed by two kinds of signals: voltage and current. When the signals are voltages, the circuit works in voltage-mode, when they are currents, it works in current-mode, and when they are both voltage and current signals, it works in mixed-mode. Therefore, in general four transfer relationships are obtained.

One mixed-mode active device was introduced in 1968 [15], it was named first-generation current conveyor (CCI). Nowadays, the current conveyor has evolved into three generations [4], basically composed of unity-gain cells [12], to drive voltages and currents. The models of several active devices by using controlled-sources are given in [14]. Those models have the drawback of generating systems of equations bigger than by using nullors or pathological elements [1]. For instance, Fig. 1.1 shows the ideal models of the operational amplifier (opamp), operational transconductance amplifier (OTA) and negative-type second generation current conveyor (CCII− [4]). These nullor equivalents are quite useful to derive simplified symbolic expressions.

Lets us consider the active RC filter shown by Fig. 1.2. The modified nodal analysis (MNA) [6], generates one equation for each node plus one equation for each opamp, leading to a system of order 15. On the other hand, the symbolic nodal analysis using nullors generates a system equal to the number of nodes minus the number of nullors, leading to a system of order 6, as shown by (1.1). The symbolic transfer function is obtained by applying the symbolic technique presented in [1], and it is given by (1.2) [6].

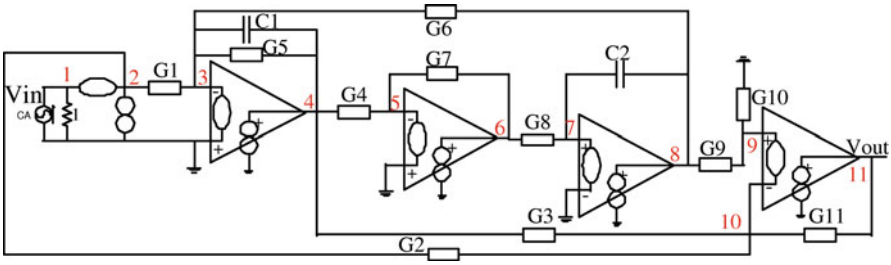


Fig. 1.2 RC filter

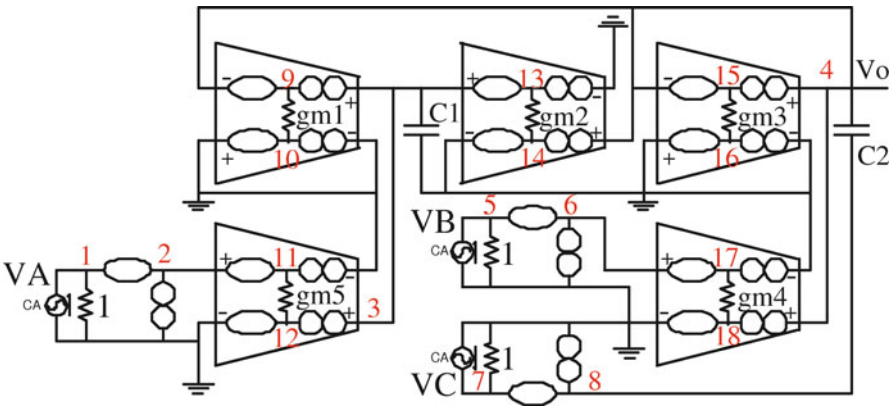


Fig. 1.3 OTA-C filter

$$\begin{bmatrix} v_{in} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ -G1 & -G5-sC1 & 0 & -G6 & 0 & 0 \\ 0 & -G4 & -G7 & 0 & 0 & 0 \\ 0 & 0 & -G8 & -sC2 & 0 & 0 \\ 0 & 0 & 0 & -G9 & G9+G10 & 0 \\ -G2 & -G3 & 0 & 0 & G2+G3+G11 & -G11 \end{bmatrix} \begin{bmatrix} v_{1,2} \\ v_4 \\ v_6 \\ v_8 \\ v_{9,10} \\ v_{11} \end{bmatrix} \tag{1.1}$$

$$\frac{v_{\text{out}}}{v_{\text{in}}} = \frac{\begin{array}{c} -(G9+G10)C1G2C2G7s^2+((G1G3-G2G5)(G9+G10)) \\ C2G7s-G4G8(G9G1(G2+G3+G11)+G2G6(G9+G10)) \end{array}}{G11(G9+G10)(G6G8G4+sC2G7G5+s^2C2G7C1)}. \tag{1.2}$$

The OTA-C filters [16], can also be modeled using nullors. Lets us consider the one shown by Fig. 1.3, the system is given in [6], and the expression by (1.3).

$$v_4 = \frac{s^2C1C2v_C+sC1gm4v_B+gm2gm5v_A}{s^2C1C2+sC1gm3+gm2gm1}. \tag{1.3}$$

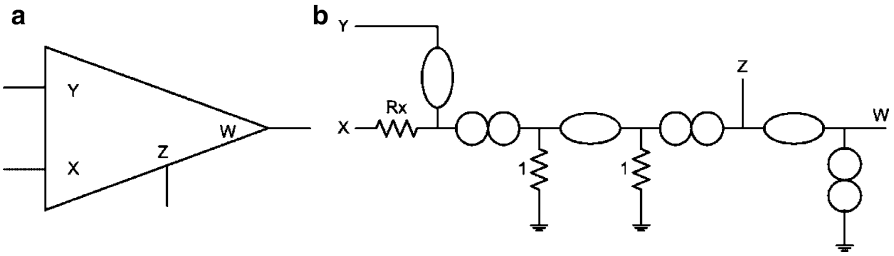


Fig. 1.4 (**a**) CFOA description, and its (**b**) nullor-equivalent including R_x [4]

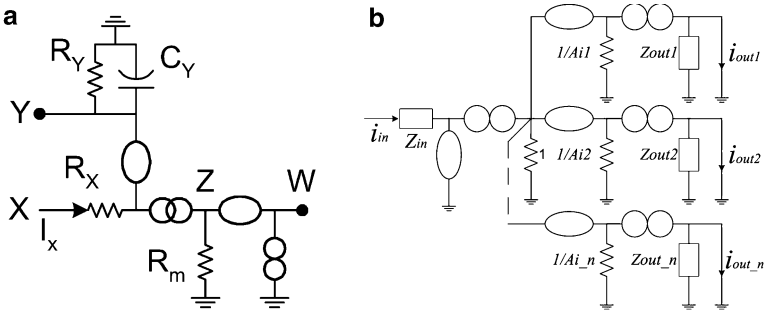


Fig. 1.5 (**a**) Pathological-equivalent of the CFOA including dominant parasitics [1], and (**b**) Nullor-equivalent of the multiple-outputs current mirror including input impedance and independent gain and output impedances [5]

The current-feedback opamp (CFOA) is another active device quite useful in linear and nonlinear applications [17–20]. It has four ports as shown in Fig. 1.4a, and basically, it can be designed by cascading a positive-type second generation current conveyor (CCII+) with a voltage follower (VF) [12]. That way, its nullor-equivalent is shown in Fig. 1.4b [4]. Besides, by using the pathological CM element [21], a compact model can be derived, as shown in Fig. 1.5a [1], where the dominant parasitics are included.

In a similar manner, other kinds of active devices, such as the current differencing buffered amplifier (CDBA) [22], operational transresistance amplifier (OTRA) [23], current operational amplifier (COA) [24], and the ones summarized in [14], can be modeled by using nullors and pathological elements, as already shown in [1, 4].

1.2.2 Current-Mode Filter Based on Current Mirror Arrays

The CM can be modeled as shown in Fig. 1.5b, including multiple-outputs, input impedance and independent gain and output impedance at each output current-path. To highlight its usefulness, lets us consider the active filter shown in Fig. 1.6.

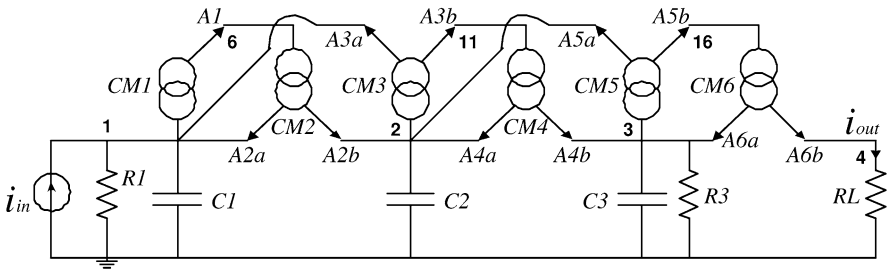


Fig. 1.6 All-pole low-pass filter implemented with dual-output CMs [11]

This filter can easily be simulated using hardware description languages [25], but it is necessary to generate the symbolic behavioral model including the gains of each CM (CM1-CM6). By applying symbolic nodal analysis [1], the admittance matrix is computed by (1.4).

$$\begin{bmatrix}
g_1+g_{i1}+g_{o2a}+g_{o3a}+sC_1 & g_{i3}A_{3a} & 0 & 0 & g_{i2}A_{2a} & 0 & 0 \\
0 & g_{o2b}+g_{i3}+sC_2+g_{o4a}+g_{o5a} & g_{i5}A_{5a} & 0 & g_{i2}A_{2b} & g_{i4}A_{4a} & 0 \\
0 & 0 & g_3+g_{o6a}+sC_3+g_{i5}+g_{o4b} & 0 & 0 & g_{i4}A_{4b} & g_{i6}A_{6a} \\
0 & 0 & 0 & g_L+g_{o6b} & 0 & 0 & g_{i6}A_{6b} \\
g_{i1}A_1 & 0 & 0 & 0 & g_{o1}+g_{i2} & 0 & 0 \\
0 & g_{i3}A_{3b} & 0 & 0 & 0 & g_{o3b}+g_{i4} & 0 \\
0 & 0 & g_{i5}A_{5b} & 0 & 0 & 0 & g_{o5b}+g_{i6}
\end{bmatrix}. \tag{1.4}$$

When the output impedances of the CMs are ideal and the gains unitary, the symbolic expression becomes,

$$\frac{i_{\text{out}}}{i_{\text{in}}} = \frac{g_i^6}{\left(C_2 {g_i}^3 C_3 g_1 + C_2 {g_i}^3 g_3 C_1\right) s^2 + \left({g_i}^5 C_3 + {g_i}^5 C_1 + C_2 {g_i}^3 g_3 g_1\right) s + {g_i}^5 g_1 + {g_i}^5 g_3 + C_2 {g_i}^3 C_3 C_1 s^3}. \tag{1.5}$$

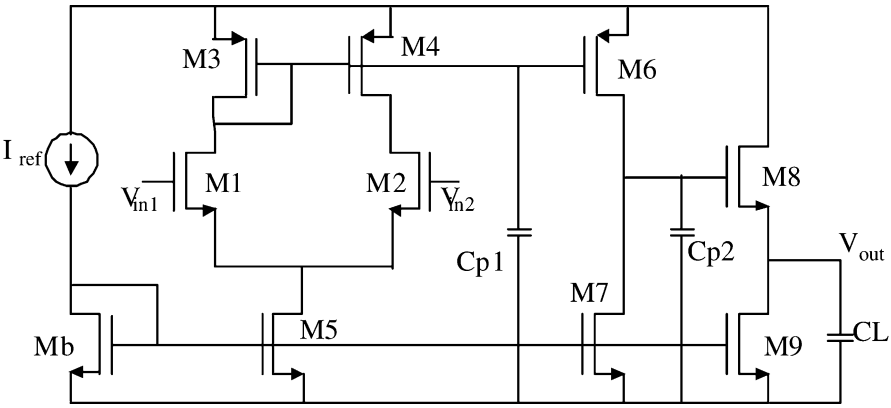


Fig. 1.7 Three stages uncompensated low voltage amplifier

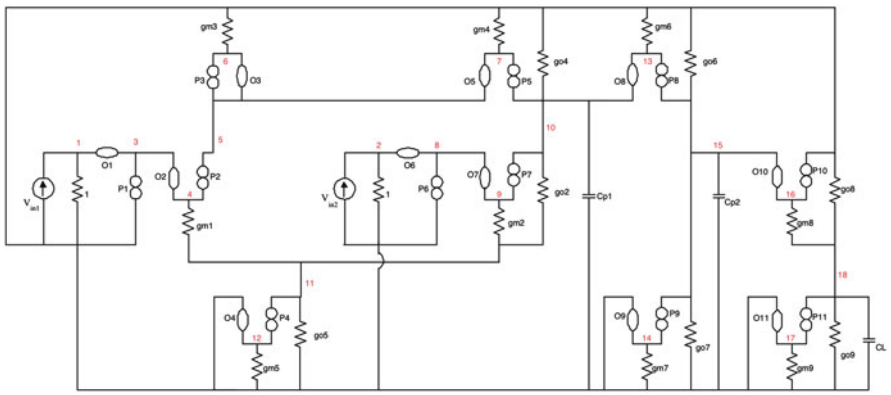


Fig. 1.8 Nullor equivalent of Fig. 1.7

1.2.3 Symbolic Behavioral Modeling of Amplifiers and Oscillators

Lets us consider the three stages uncompensated low-voltage amplifier shown in Fig. 1.7. Its nullor equivalent is given in Fig. 1.8. The nodal admittance matrix has an order 7×7 [7]. The exact symbolic transfer function is given in [26], which is too large, so that a further step should be performed to simplify large symbolic expressions [6].

If the low voltage amplifier is designed with standard CMOS IC technology, its gain performance comparison with respect to its behavioral model is shown in Fig. 1.9. The noise analysis of CMOS amplifiers using nullor-equivalents and DDDs is presented in [8].

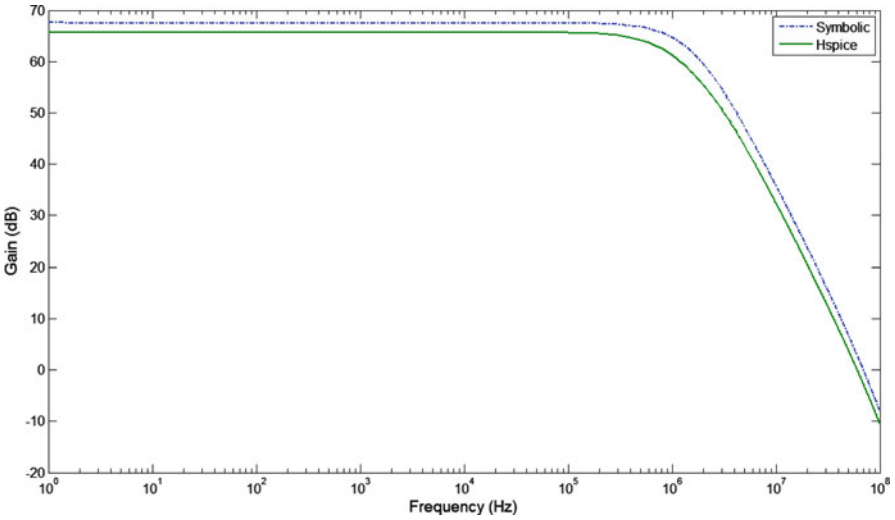


Fig. 1.9 Comparison between HSPICE and the derived symbolic expression [7]

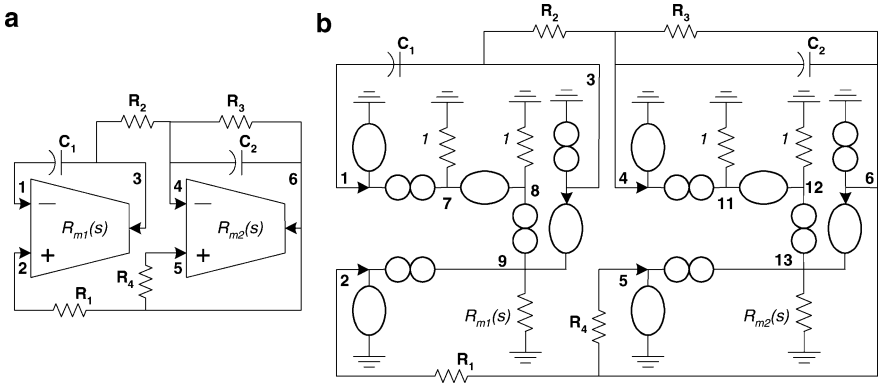


Fig. 1.10 (**a**) OTRAs-based oscillator, and (**b**) its nullor-equivalent [23]

The symbolic behavioral modeling of sinusoidal oscillators is quite useful for design purposes. Lets us consider the oscillator composed of OTRAs, as shown in Fig. 1.10. The system of equations by applying symbolic nodal analysis is derived in [23], where the characteristic equation is approached by (1.6), and the condition and frequency of oscillation are given by (1.7). By choosing $R_1 = R_2 = 2\,\mathrm{k}\Omega$, $R_3 = R_4 = 10\,\mathrm{k}\Omega$, the value of the frequencies of oscillation are shown in Fig. 1.11 as: f_1 =2.65 MHz (Dashed-line) with $C_1 = C_2 = 24\,\mathrm{pF}$, $f_2 = 6.29\,\mathrm{MHz}$ with $C_1 = C_2 = 6.46\,\mathrm{pF}$ (Dotted-line), and $f_3 = 12\,\mathrm{MHz}$ (Solid line) with $C_1 = C_2 = 0.1\,\mathrm{pF}$.

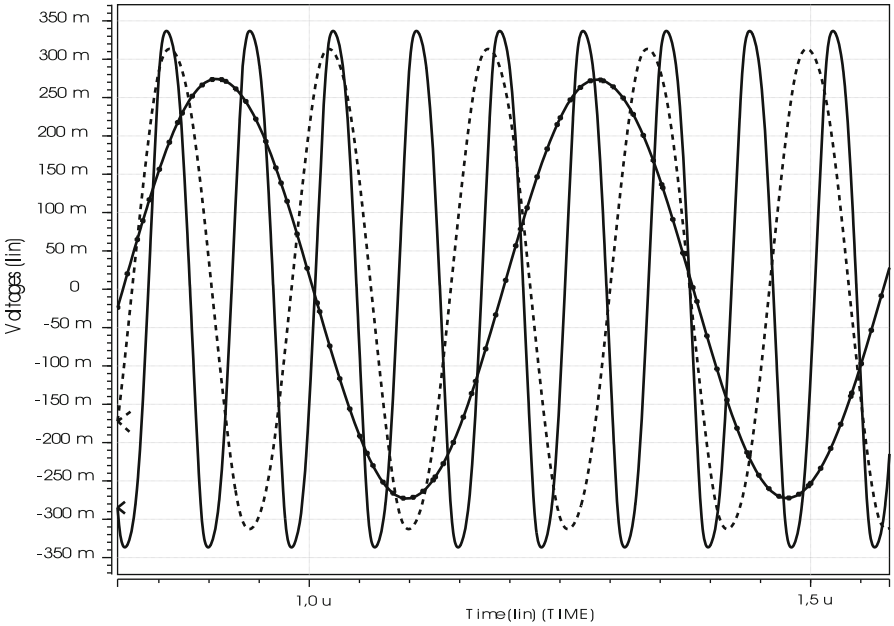


Fig. 1.11 Time responses of the OTRA-based sinusoidal oscillator

The parasitic capacitances are approximated to $C_{m1} = C_{m2} = 6.46$ pF. From Fig. 1.11 one can observe that the maximum frequency of oscillation ($f_3 = 12$ MHz) is limited by $C_{m1,2} = C_{Z2}$.

$$s^2 + \frac{1}{C_2 + C_{m2}}\left(\frac{1}{R_s} - \frac{1}{R_4}\right)s + \frac{1}{R_1 R_2 (C_1 + C_{m1})(C_2 + C_{m2})}. \tag{1.6}$$

$$C.O. : R_3 = R_4, \quad \omega_o = \frac{1}{\sqrt{R_1 R_2 (C_1 + C_{m1})(C_2 + C_{m2})}}. \tag{1.7}$$

1.3 Systematic Design of Active Devices

In the field of analog CAD, recent developments on the computational synthesis of analog ICs are given in [13]. Another recent technique is given in [12], where the VF is evolved to a voltage mirror (VM), and the dual topology of the VF leads us to design a current follower (CF). These are three unity-gain cells, and the fourth one is the CM.

In summary, the computational synthesis of the VF includes [27]: generation of the small-signal circuitry, addition of the bias circuitry, replacement of nullator-norator pairs by transistors, and replacement of current biases by CMs. That is, since

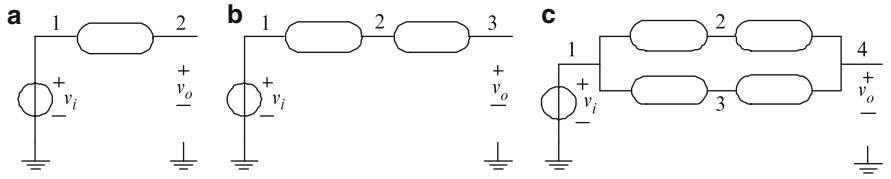


Fig. 1.12 Nullator-equivalent circuits to describe a VF

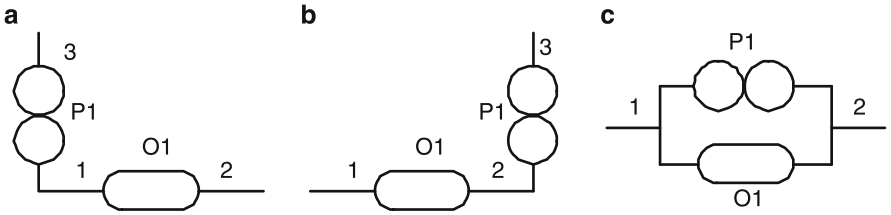


Fig. 1.13 Addition of a norator P_1 at: (**a**) node 1, (**b**) node 2, and (**c**) between nodes 1 and 2 of the nullator O_1

the voltage across a nullator is zero [1], the VF is modeled as shown by Fig. 1.12. A norator is joined to each nullator to form nullator-norator joined-pairs, as shown by Fig. 1.13. The combinations for the descriptions in Fig. 1.12 are given in [12].

The bias circuitry is generated by addition of DC voltage and current bias levels to each nullator-norator joined-pair. That way, global DC voltage sources (VDD and VSS) are added, and ideal DC current sources are added to each norator P_i, as shown by Fig. 1.14. Besides, several bias sources can be eliminated as shown in [12, 27].

Each nullator-norator joined-pair (O_i-P_i) is replaced by a MOSFET, where the joined terminals are associated to the source, and the other terminals of the nullator and norator, are associated to the gate and drain, as shown by Fig. 1.15. The kind of MOSFET, i.e. channel N or P, is determined by the direction of the current biases from VDD to VSS. In the same manner, an ideal current source is replaced by either a CMOS current mirror or a single MOSFET, as shown by Fig. 1.15. For instance, the biased circuits shown by Fig. 1.14c, d, are synthesized in Fig. 1.16 [27]. One can note that the VF topology in Fig. 1.16e is the flipped VF [28].

Figure 1.17 shows three well-known CMOS VFs. They can be evolved to design VMs, as the ones shown in Fig. 1.18, where the VF topologies for Fig. 1.17a, b are embedded into topologies Fig. 1.18a, b, respectively [12].

1.3.1 Computational Synthesis of CMs

The synthesis of a CM begins by using four nullators (O) and four norators (P), as shown by Fig. 1.19a. Each gate (G1, G2, G3, G4) in Fig. 1.19a can be connected

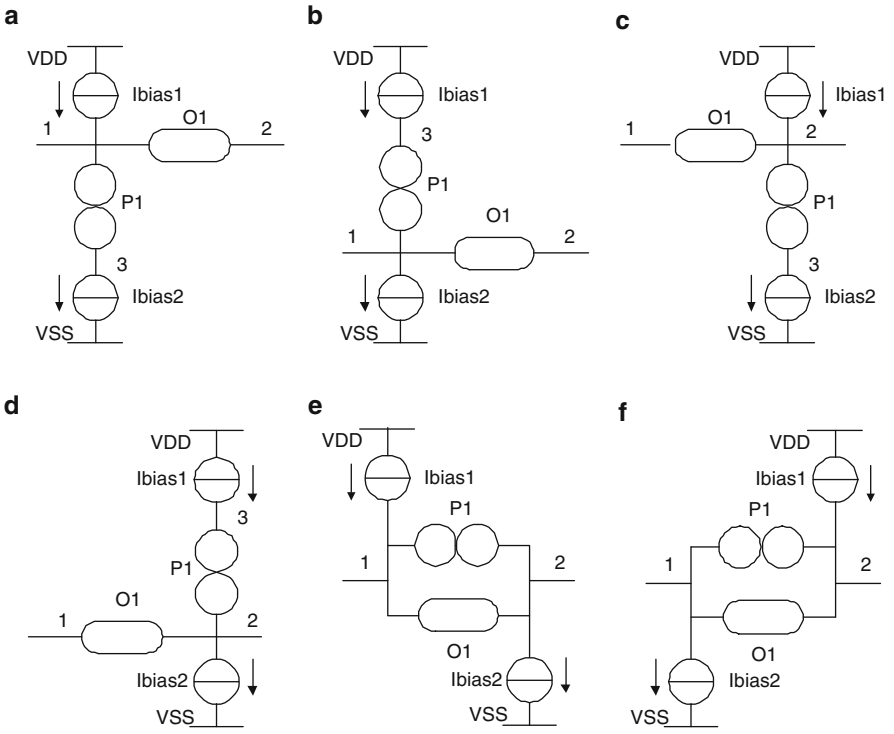


Fig. 1.14 Addition of current biases to Fig. 1.13

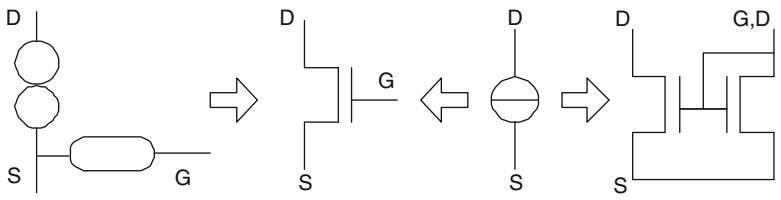


Fig. 1.15 Synthesis of the nullor by a MOSFET, and of a current source by a CM

to nodes: A, B, C, D, V_{BIAS}, Vdd or to an extra node (NG1, NG2, NG3, NG4) who is also used to add level shifters. The chromosomal representation consists of three genes [12]: genBias, genIO, and genLS. Lets us consider the chromosome 611669. Its BGE is shown in Fig. 1.19d. Figure 1.19e shows its generic description. Six synthesized CMs are shown in Table 1.1.

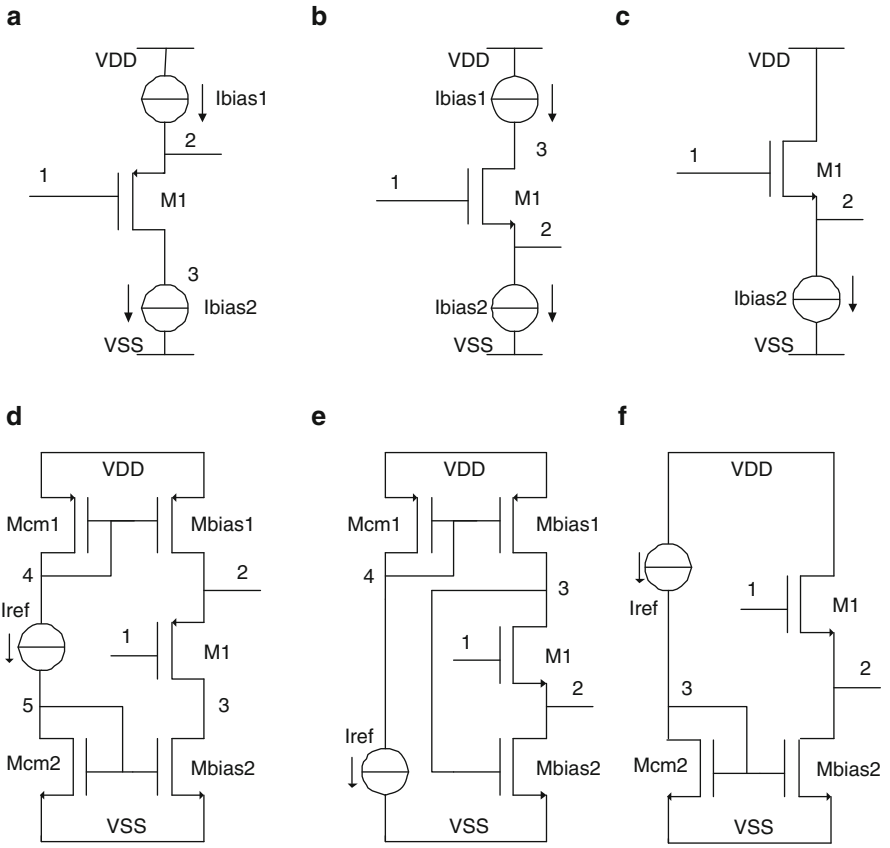


Fig. 1.16 Synthesis of the VFs from Fig. 1.14c, d

1.3.2 Computational Synthesis of Mixed-Mode Active Devices

The four unity-gain cells find applications in filter and oscillator design [29–31]. Furthermore, the interconnection or superimposing of two or more of them [12], leads us to create known or new active devices. For instance, several combinations among two unity-gain cells are shown in Fig. 1.20.

From Fig. 1.20, the negative and positive types second generation current conveyors (CCII−/+) [4], are generated by Figs. 1.20e, f, and their inverting realizations (ICCII−/+) by Fig. 1.20g, h. Other topologies like the OTRA, CBDA and inverting current conveyors can be synthesized by augmenting the interconnection strategies from [12]. For example, the superimposing of Fig. 1.20f, k generates the CFOA, i.e., it is the connection of three blocks VF-CM-VF, or equivalently, the CCII+ in cascade connection with a VF [4].

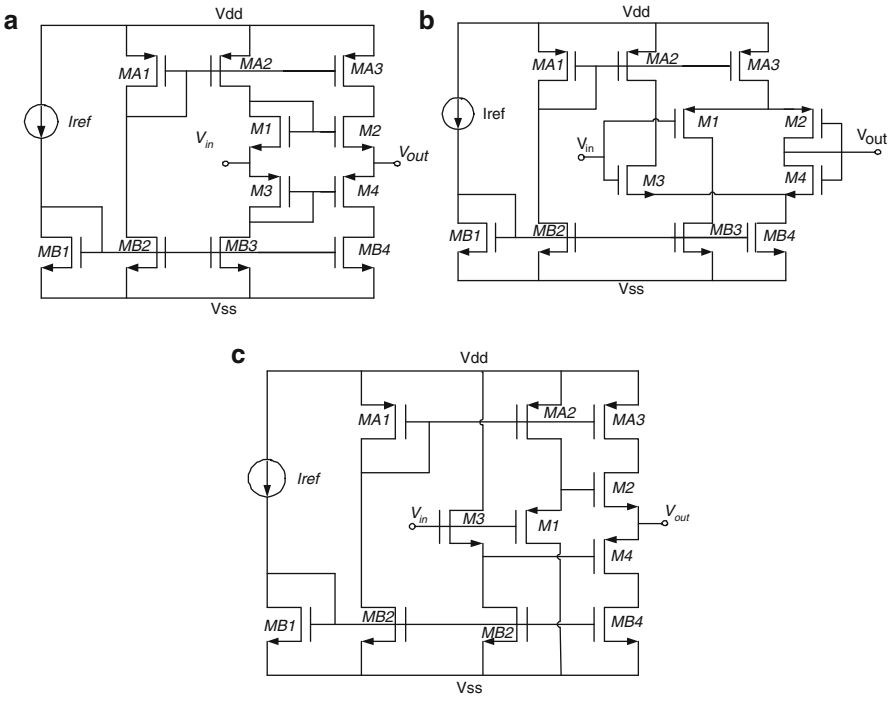


Fig. 1.17 Three VFs already synthesized in [27]

By combining the three VFs depicted in Fig. 1.17 with a simple CM, nine CFOAs arise. The VFs are labeled with capital letters A, B and C.

1.4 Circuit Optimization

The biasing and sizing of analog ICs is a challenge in the development of electronic design automation tools [26]. Multi-objective evolutionary algorithms have demonstrated their usefulness in generating suitable/feasible solutions [32–34]. In this manner, we summarize three evolutionary algorithms for the multi-objective optimization of the nine CFOA-topologies synthesized in Fig. 1.21.

A multi-objective optimization problem (MOP) can formally be defined as the problem of finding the vector:

$\mathbf{x} = [x_1, x_2, \ldots, x_n]^{\mathrm{T}}$, satisfying k inequality constraints:

$$g_i(\mathbf{x}) < 0; \text{ for } i = 1, 2, \ldots k$$

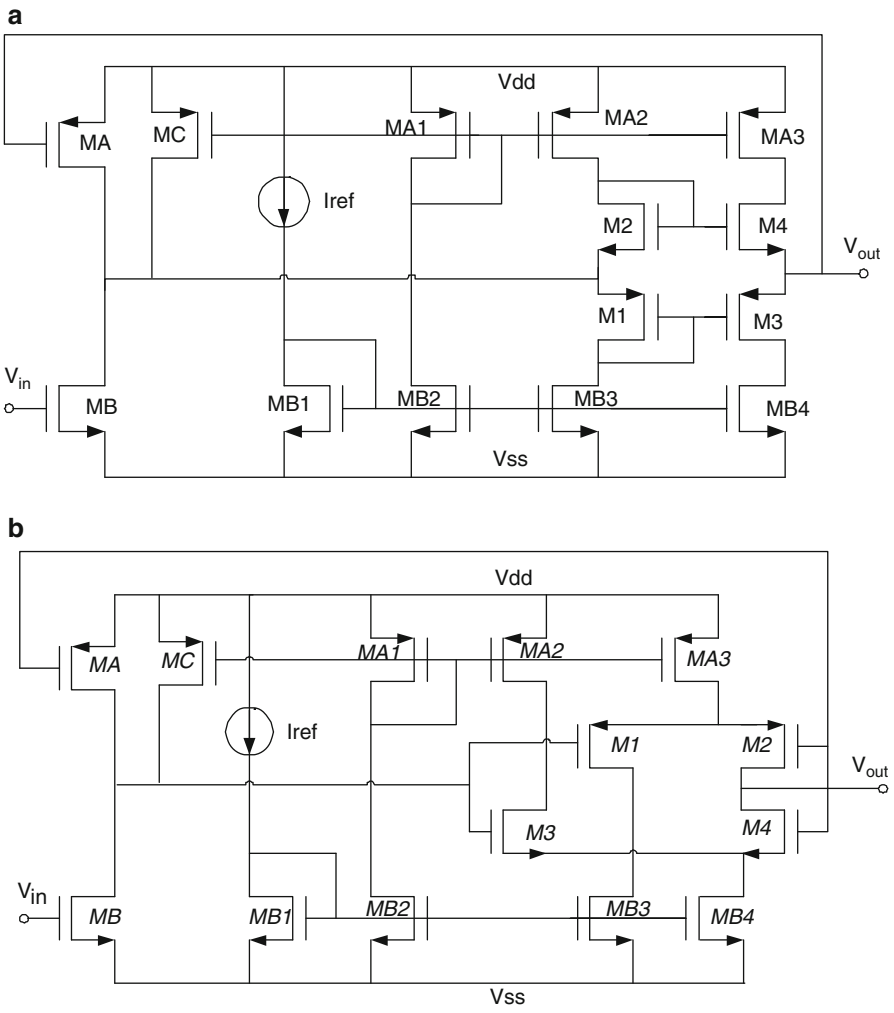


Fig. 1.18 Two VMs synthesized from the VFs in Fig. 1.17

the p equality constraints

$$h_j(\mathbf{x}) = 0; \text{ for } j = 1, 2, \ldots p$$

and minimizing the vector function

$$\mathbf{f} : \mathbb{R}^n \rightarrow \mathbb{R}^m$$

$$\mathbf{f}(\mathbf{x}) = [f_1(\mathbf{x}), f_2(\mathbf{x}), \ldots, f_m(\mathbf{x})]^{\mathrm{T}}.$$

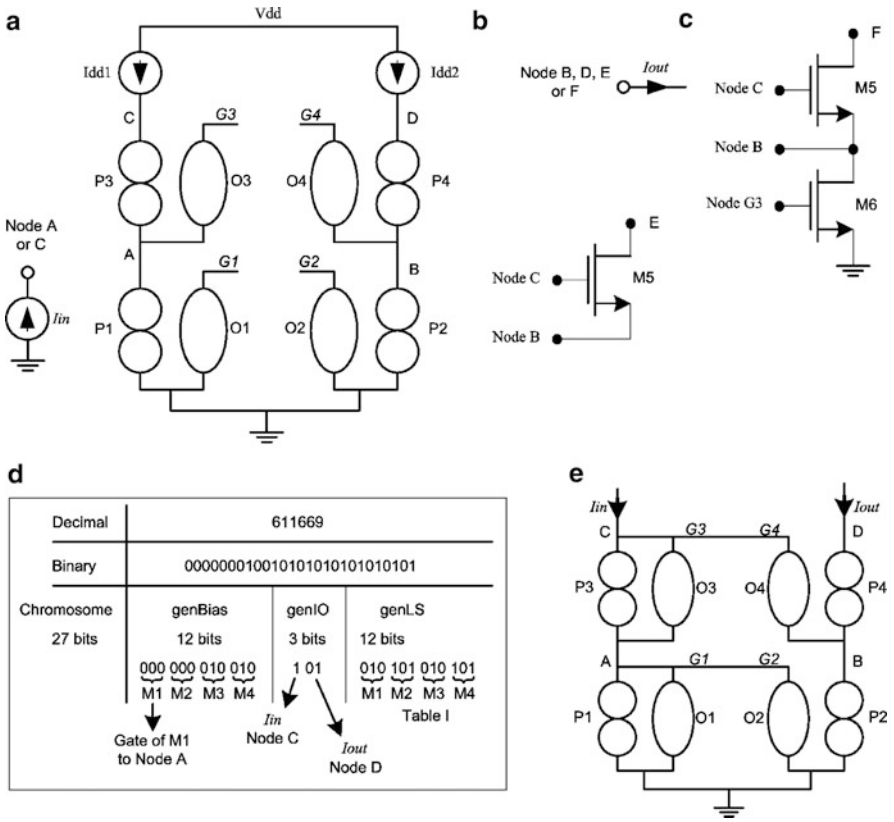


Fig. 1.19 (**a**) Modeling a CM; (**b**) and (**c**) extra circuits for I_{OUT}; (**d**) codification of chromosome: 611669; (**e**) generic model of the CM 611669 [12]

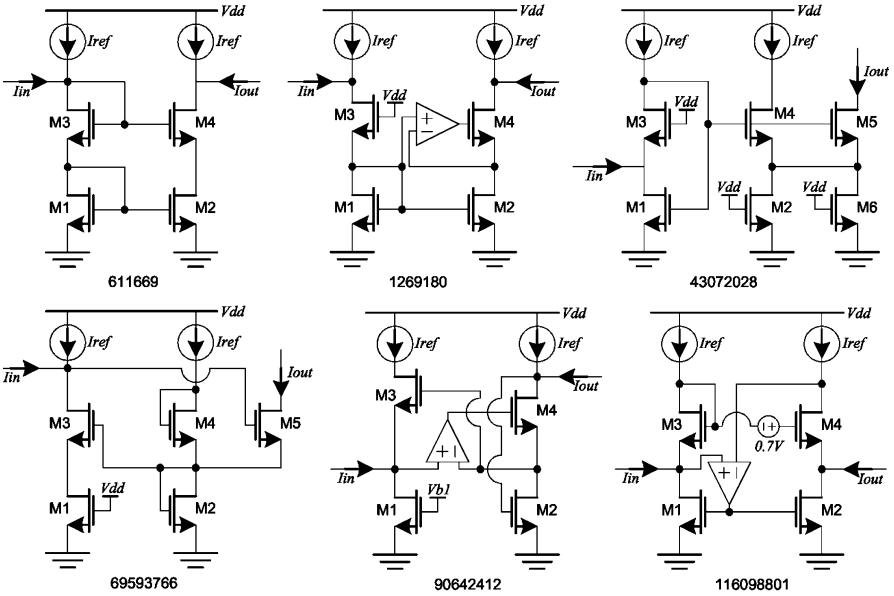
The goal is focused on determining from the set S, all vectors (points) satisfying the constraints that yield the optimum values for all the m objective functions simultaneously. The constraints define the feasible region S, and any point $\mathbf{x}$ in the feasible region is called a feasible point.

Pareto dominance: A vector $\mathbf{u} \in \mathbb{R}^m$ is said to dominate a vector $\mathbf{v} \in \mathbb{R}^m$, $\mathbf{u} \prec \mathbf{v}$, if and only if $\mathbf{u}$ is partially less than $\mathbf{v}$, i.e., $\forall i \in \{1, \ldots m\}$, $u_i \leq v_i \wedge \exists i \in \{1, \ldots m\}$: $u_i < v_i$, (assuming minimization). One solution dominates another one when it is strictly better in at least one objective, and not worse in any of them.

Formal definition of Pareto optimality: A solution $\mathbf{x}_u \in S$ (where S is the feasible region) is said to be Pareto optimal if and only if there is no $x_v \in S$ for which $\mathbf{v} = \mathbf{f}(\mathbf{x}_v) \in \mathbb{R}^m$ dominates $\mathbf{u} = \mathbf{f}(\mathbf{x}_u) \in \mathbb{R}^m$, where m is the number of objectives.

This definition says that $\mathbf{x}_u$ is Pareto optimal if there exists no feasible vector $\mathbf{x}_v$ which would decrease some objective without causing a simultaneous increase in at least one another objective (assuming minimization). This definition does

Table 1.1 Six synthesized CMs



CM chromosome	611669	1269180	43072028	69593766	90642412	116098801
Gain	1.001	1.000	1.002	0.997	1.002	0.999
BW MHz	195	196	36.6	106	546	86
Rin KΩ	4.88	8.16	5.91	74	1.03	0.029
Rout KΩ	67000	4e7	12.3	7.37	7.45	920
Offset nA	8	0.02	0 (in 60 µA)	652	7840	15
SettlingT ns	2.03	1.85	3.14	1.26	0.39	–
Slew Rate A/ms	6.25	6.30	2.62	12.97	19.88	–
Dynamic Range µA	−10 to 270	−10 to 61	45 to 80	−0.75 to 50	−10 to 210	−10 to 5,000

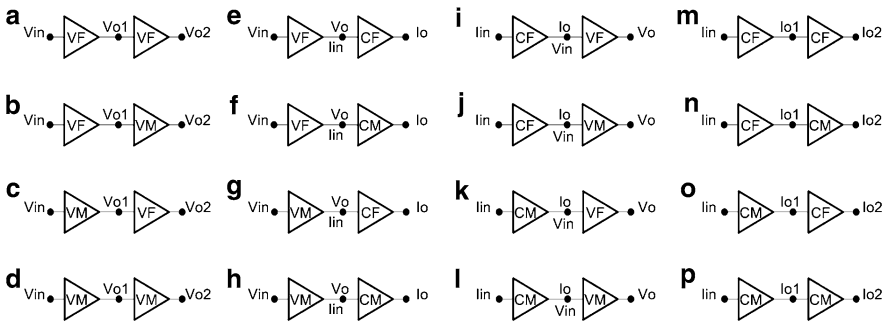


Fig. 1.20 Combinations among two unity-gain cells [12]

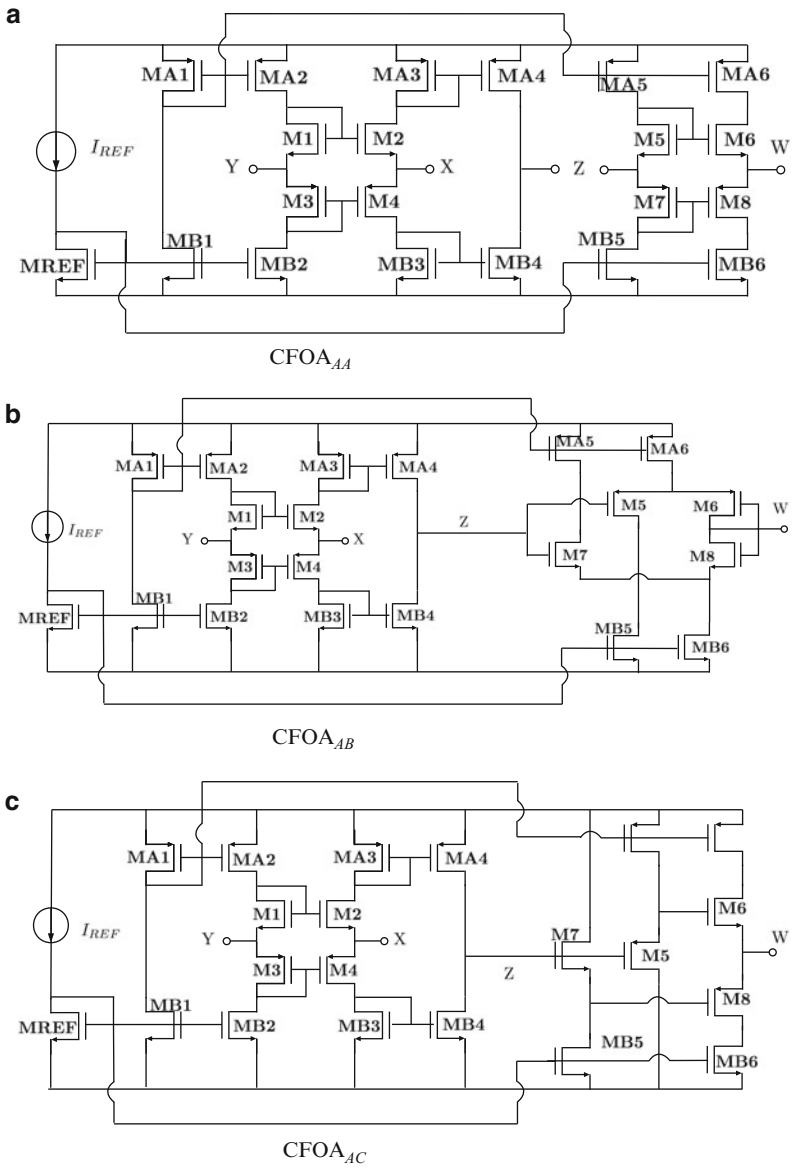


Fig. 1.21 CFOAs synthesized by combining the VFs in Fig. 1.17 with a simple CM

not provide us a single solution (in decision variable space), but a set of solutions which form the so-called Pareto Optimal Set or Pareto Front. All the vectors that correspond to the solutions included in the Pareto Front are non-dominated.

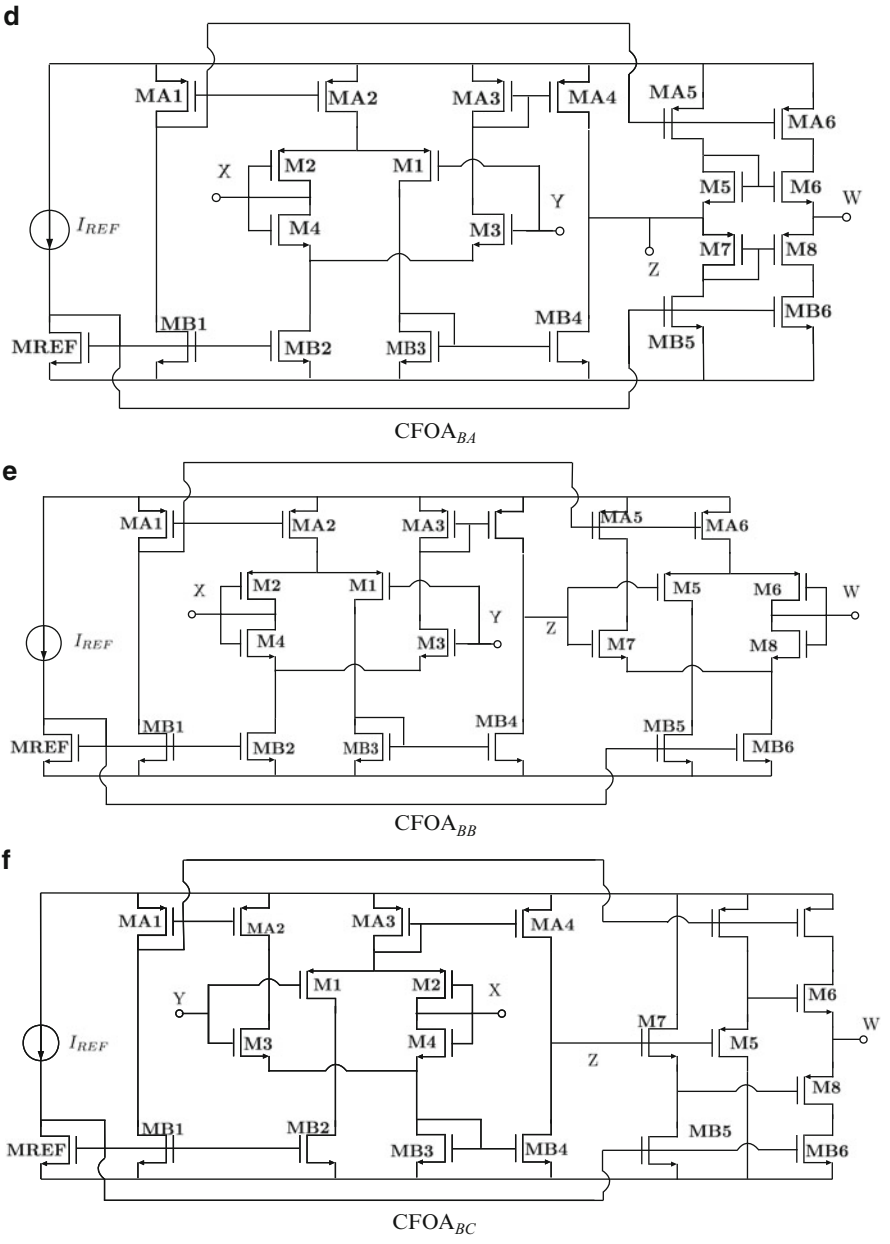


Fig. 1.21 (continued)

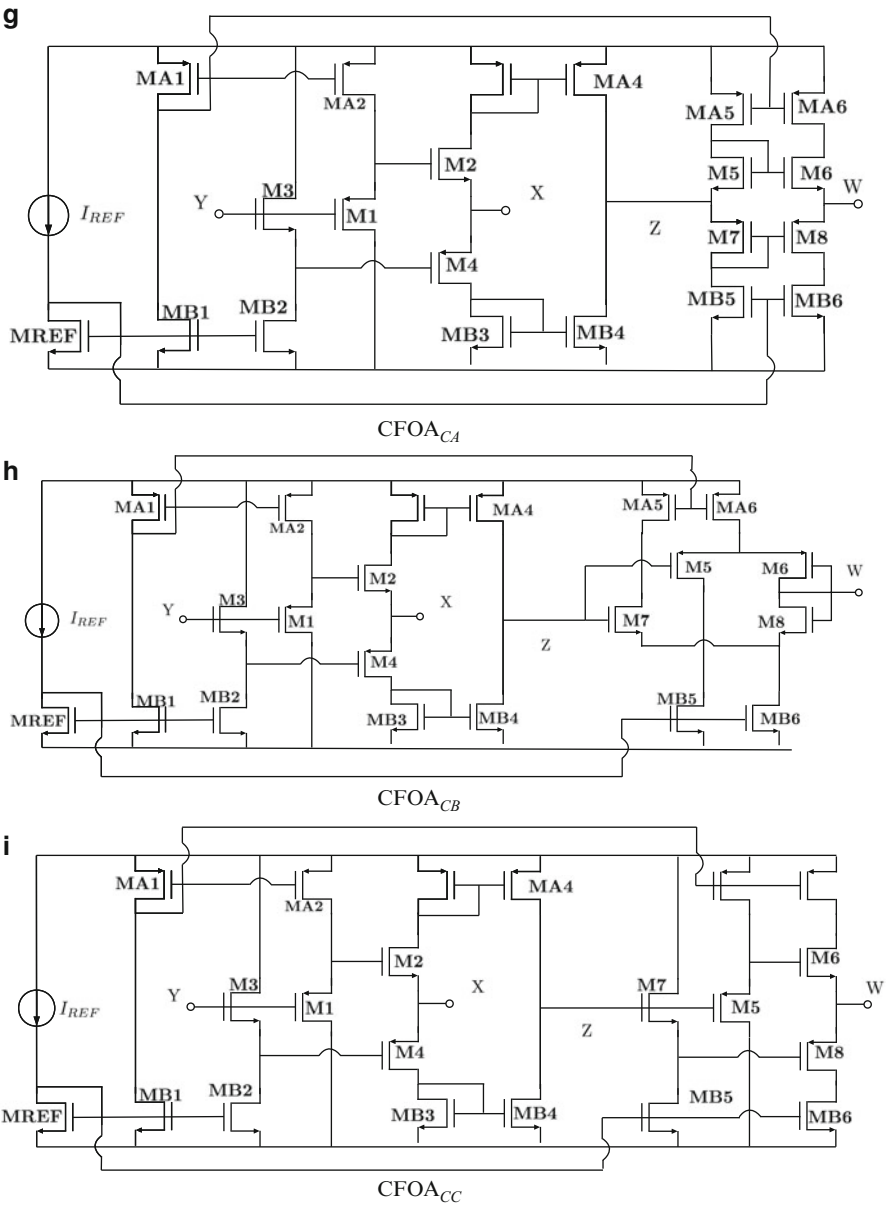


Fig. 1.21 (continued)

Algorithm 1 NSGA-II Algorithm

1: $P_0 =$ random, $Q_0 =$ random
2: $t = 0$
3: $P_{t+1} = \emptyset$ and $i = 1$
4: **repeat**
5: $R_t = P_t \cup Q_t$
6: $F =$ fast-non-dominated-sort(R_t)
7: crowding-distance-assignment(F_i)
8: **repeat**
9: $P_{t+1} = P_{t+1} \cup F_i$
10: $i = i + 1$
11: **until** $|P_{t+1}| + |F_i| \leq N$
12: Sort($F_i, \prec_n$)
13: $P_{t+1} = P_{t+1} \cup F_i[1 : (N - |P_{t+1}|)]$
14: $Q_{t+1} =$ make-new-pop(P_{t+1})
15: **until** stop criteria

1.4.1 Non-Dominated Sorting Genetic Algorithm II (NSGAII)

This is an improved version of the (NSGA) by including elitism and was named as NSGA-II [35]. The NSGA-II procedure is summarized in Algorithm 1, and it approximates the Pareto Front of a MOP by sorting and ranking all solutions in order to choose the better solutions to make a new offspring. This means, by ranking all the population in different Pareto subfronts that it will be possible to know which solutions show better performance. In this algorithm is contemplated a way to choose the best solution between two solutions in the same subfront preserving diversity, in this form it is possible to select the best part of a population without losing diversity.

NSGA-II is based on two main procedures: *Fast Nondominated Sort* and *Crowding Distance Assignment*. These two procedures ensure elitism and it is possible to add constraints to ensure that the solutions are feasible [34, 35].

At the begining it is necessary to randomly initialize the parameters and start by generating two populations (P_o and Q_o) each one of size N, from random values into a feasible region. The NSGA-II procedure in each generation consists of rebuilding the current population (R_t) from the two original populations (P_t and Q_t) then the new size of current population will be $2N$. Now, through a nondominated sorting all solutions in R_t are ranked, and classified in a family of subfronts, as shows Fig. 1.22. In the next step is necessary to create from the current population R_t (previously ranked and ordered by subfront number) a new offspring (P_{t+1}), the objective will be to choose from a population of size $2N$, the N solutions which belong to the first subfronts. In this manner, the last subfront could be greater than is necessary, then it is used a measure (i_{distance}) that allows to identify the better solutions and preserving elitism by selecting the solutions that are far the rest, this is possible simply by modifying a little bit the concept of Pareto dominance by including constraints in the dominance concept.

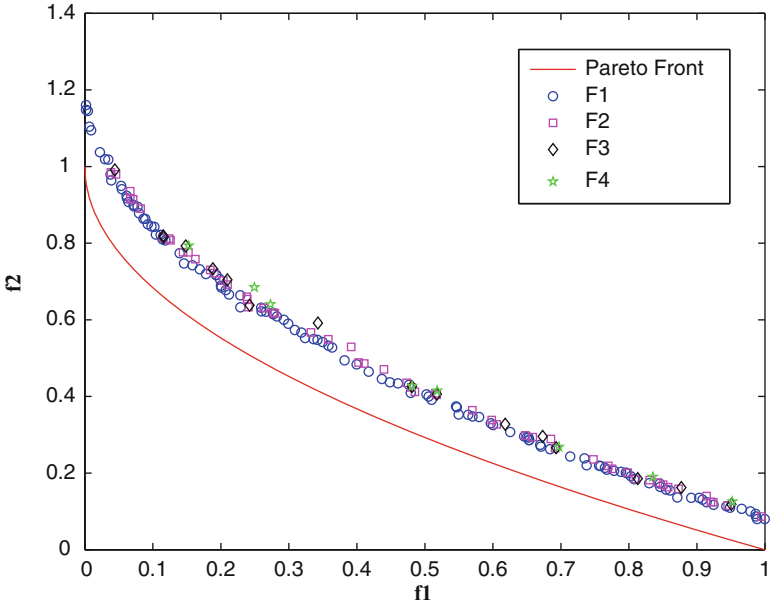


Fig. 1.22 Fast Non-dominated sorting

1.4.2 Multi-Objective Evolutionary Algorithm Based on Decomposition

The basic idea of MOEA/D is the decomposition of a multiobjective problem in scalar optimization subproblems by a *weights vector* [36]. This vector associates a weight (λ) for each subproblem which is considered as a single individual in the population which is going to try to improve by itself and to its nearby (*neighbors*).

After the initialization of the parameters the first step in MOEA/D is related to define the N spread weights vector over the objectives space (to each individual corresponds one λ_i). One way can be by using a parameter H in a sequence as described by (1.8):

$$\left\{\frac{0}{H}, \frac{1}{H}, \ldots, \frac{H}{H}\right\}. \tag{1.8}$$

Therefore, for $m = 2$, $N = H + 1$, with $m > 2$ the number of such vectors is defined by the combination in (1.9):

$$N = C_{H+m-1}^{m-1} \tag{1.9}$$

In Algorithms 2 and 3 are the pseudocode to generate these vectors, for three and m objectives, respectively. It is necessary to chose a value for H, so that the population size depends on this number.

Algorithm 2 Build spread of N weight vectors ($m = 3$)

```
1: i = 1, set H
2: for μ1 = 0 to 1, step 1/H do
3:     for μ2 = 0 to 1, step 1/H do
4:         if 1 − (μ1 + μ2) ≥ 0 then
5:             λi = {μ1  μ2 ... (1 − (μ1 + μ2))}
6:             i = i + 1
7:         end if
8:     end for
9: end for
```

Algorithm 3 Build spread of N weight vectors for m objectives

```
1: i = 1, set H
2: for μ1 = 0 to 1, step 1/H do
3:     for μ2 = 0 to 1, step 1/H do
4:         ...
5:         for μm−1 = 0 to 1, step 1/H do
6:             if 1 − (μ1 + μ2 + ... μm−1) ≥ 0 then
7:                 λi = {μ1  μ2 ... (1 − (μ1 + μ2 + ... μm−1))}
8:                 i = i + 1
9:             end if
10:        end for
11:        ...
12:    end for
13: end for
```

Algorithm 4 MOEA/D Algorithm

```
1: build an uniform spread of N weight vectors (λ)
2: B(i) = {i1, i2, ..., iT}
3: t = 1 , POP=random() , set E = ∅ , T
4: repeat
5:     for i = 1, 2, ..., N do
6:         randomly select parents from B(i)
7:         generate new individual y
8:         for each ℓ ∈ B(i) do
9:             if g(y | λℓ, Z*) ≤ g(xℓ | λℓ, Z*) then
10:                xℓ = y
11:                Fℓ = F(y)
12:            end if
13:        end for
14:    end for
15:    remove from EP all vectors dominated by F(y)
16: until stop criteria
```

A number (T) of neighborhoods is defined for each $\lambda_\mathbf{i}$. The Euclidean distance between each $\lambda_\mathbf{i}$ is calculated. Finally, for each $\lambda_\mathbf{i}$ there are (T) neighborhoods nearby, saved in B. Algorithm 4 shows the steps performed by MOEA/D [36].

In each generation there is a population of N points $\mathbf{x}_1, \mathbf{x}_2, \ldots, \mathbf{x}_N \in X$ where $\mathbf{x}_i = (x_i^1, x_i^2 \ldots x_i^n)$ is the current solution to the i_{th} subproblem and there are $F_1, F_2, \ldots, F_N$, where $F_i = F(\mathbf{x}_i) : \mathbb{R}^n \rightarrow \mathbb{R}$.

Algorithm 5 Pseudocode for MO-PSO

```
Initialize NoLoops, bound limits, population (N) and velocities
Evaluate population
Update Pbest
Select non-dominated particles
Select Gbest randomly among non-dominated particles
for i= 1 to NoLoops do
    for j=1 to N do
        Update particle velocity
        Update particle position
        Ensuring new position is into bound limits
    end for
    Evaluate population
    Update Pbest
    Select non-dominated particles and save them in REP
    Select Gbest randomly among non-dominated particles
end for
```

In the procedure, a new individual $\mathbf{y}$ is generated and compared with all its neighborhood by applying a decomposition approach ($g[\mathbf{x}_i \mid \lambda_i, \mathbf{Z}^*]$), e.g. the *Tchebycheff Approach*, and each neighbor worse than this new individual will be replaced by it in an external population (EP), which is used to store non-dominated solutions.

In the Tchebycheff Approach, the scalar optimization problem is described by (1.10), where $\mathbf{Z}^* = \{z_1^*, z_2^*, \ldots, z_m^*\}^T$ are the best current objective functions found.

$$g(\mathbf{x}_i \mid \lambda_i, \mathbf{Z}^*) = \max\{\lambda_i | f_j(\mathbf{x}_i) - z_j^*|\}_{\substack{1 \le i \le N \\ 1 \le j \le m}}. \tag{1.10}$$

1.4.3 Multi-Objective Particle Swarm Optimization

In the Multi-Objective Particle Swarm Optimization Algorithm (MO-PSO) [32], there are N particles denoted by $\mathbf{x}_i$, where $i = 1, 2, \ldots, N$, and are represented by their positions in the search space. Each particle $\mathbf{x}_i = (x_i^1, x_i^2 \ldots x_i^n)$ represents a position in the space and depends on its previous local best position (P_{best}) and global best position (G_{best}). Equation (1.11) is used to compute the speed of each particle, where V_i is the current velocity of the particle ith, k_w is the inertia weight which takes typical values lower than 1; P_{besti} is the best position of particle ith, P_i is the position of the current particle and G_{best} is a global best selected among the global best solutions. The new position of each particle is computed by (1.12).

$$V_i = k_w V_i + R_1(P_{\text{besti}} - P_i) + R_2(G_{\text{best}} - P_i). \tag{1.11}$$

$$P_i = P_i + V_i. \tag{1.12}$$

In Algorithm 5 our proposed MO-PSO is described. It takes care of the new position to avoid going beyond the bound limits. Step 1 is the initialization

procedure to set the bound limits, and the particles are initialized randomly within those bound limits. The velocities are initialized with zero values. In step 2, the population is evaluated to update the best position (P_{best}) at step 3, for each particle. Afterwards, the non-dominated particles are gathered to select randomly a global best (G_{best}) into that repository (steps 4 and 5). Then, the velocity and position of each particle is updated, and avoiding going beyond the bound limits (steps 7–11). Once all the particles are updated, an evaluation process updates the best position for each particle, the non-dominated particles are selected and saved in a repository (REP). Among the solutions contained in REP, one of them is selected randomly to be the global best for the next loop (steps 12–15). This process continues until a determined number of loops.

1.4.4 Optimization of Active Devices by Evolutionary Algorithms

This section shows the application of NSGA-II, MOEA/D and MO-PSO, in the optimization of the nine CFOAs shown in Fig. 1.21. Those algorithms were programmed with a PERL script, and the circuit simulations are made with HSPICE. The goal is to find the optimal width (W_i) and length (L) of each MOSFET. The simulation results are collected by using the HSPICE .MEASURE instruction, that is capable to save electronic measurements in the output listing. The CFOAs are biased with VDD = 1.5 V and VSS = −1.5 V. The electrical measurements were executed with a load capacitor of 1 pF and the HSPICE simulations were performed with a LEVEL 49 standard CMOS Technology of 0.18 µm.

As already shown in [32–34], the optimization problem is expressed as:

$$\begin{aligned} &\text{minimize } \mathbf{f}(\mathbf{x}) = [f_1(\mathbf{x}), f_2(\mathbf{x}), \ldots, f_{11}(\mathbf{x})]^{\mathrm{T}} \\ &\text{subject to } \; h_k(\mathbf{x}) \geq 0 \; , \;\; k = 1 \ldots p, \\ &\text{where } \; \mathbf{x} \in X. \end{aligned} \tag{1.13}$$

$\mathbf{f}(\mathbf{x})$ is the vector formed by eleven objectives:

- $f_1(\mathbf{x}) =$ Power consumption
- $f_2(\mathbf{x}) =$ |1 - Voltage gain from Y port to X port| (GAIN_X)
- $f_3(\mathbf{x}) = -1*$ Voltage band width from Y port to X port (BW_X)
- $f_4(\mathbf{x}) = -1*$ Input resistance on Y port (Z_Y)
- $f_5(\mathbf{x}) =$ Output resistance on X port (Z_X)
- $f_6(\mathbf{x}) =$ | 1 - Current gain from X port to Z port| (GAIN_Z)
- $f_7(\mathbf{x}) = -1*$ Current band width from X port to Z port (BW_Z)
- $f_8(\mathbf{x}) = -1*$ Output resistance on Z port (Z_Z)
- $f_9(\mathbf{x}) =$ |1 - Voltage gain from Z port to W port| (GAIN_W)
- $f_{10}(\mathbf{x}) = -1$ * Voltage band width from Z port to W port (BW_W)
- $f_{11}(\mathbf{x}) =$ Output resistance on W port (Z_W)

Table 1.2 CFOA_{AA} ENCODING

gene	Design variable	Encoding	Decision space
x_1	L	All transistors	$0.18\mu\text{m} \leq L \leq 0.9\mu\text{m}$
x_2	W_1	MREF, MB1-MB4, M1, M2	$0.18\mu\text{m} \leq W_1 \leq 200\mu\text{m}$
x_3	W_2	MA1-MA4, M3, M4	$0.18\mu\text{m} \leq W_2 \leq 200\mu\text{m}$
x_4	W_3	MB5, MB6, M5, M6	$0.18\mu\text{m} \leq W_3 \leq 200\mu\text{m}$
x_5	W_4	MA5, MA6, M7 , M8	$0.18\mu\text{m} \leq W_4 \leq 200\mu\text{m}$
x_6	I	I_{BIAS}	$10\mu\text{A} \leq I \leq 400\mu\text{A}$

Table 1.3 CFOA_{BC} ENCODING

gene	Design variable	Encoding	Decision space
x_1	L_1	MREF, MA1-MA4, MB1-MB4, M1-M4	$0.18\mu\text{m} \leq L_1 \leq 0.9\mu\text{m}$
x_2	L_2	MA5, MA6, MB5, MB6, M6-M8	$0.18\mu\text{m} \leq L_2 \leq 0.9\mu m$
x_3	W_1	MREF, MB1, MB2, M3, M4	$0.18\mu\text{m} \leq W_1 \leq 200\mu\text{m}$
x_4	W_2	MA1, MA2, M1, M2	$0.18\mu\text{m} \leq W_2 \leq 200\mu\text{m}$
x_5	W_3	MB3, MB4	$0.18\mu\text{m} \leq W_3 \leq 200\mu\text{m}$
x_6	W_4	MA3, MA4	$0.18\mu\text{m} \leq W_4 \leq 200\mu\text{m}$
x_7	W_5	MB5, MB6	$0.18\mu\text{m} \leq W_5 \leq 200\mu\text{m}$
x_8	W_6	MA5, MA6	$0.18\mu\text{m} \leq W_6 \leq 200\mu\text{m}$
x_9	W_7	M5	$0.18\mu\text{m} \leq W_7 \leq 200\mu\text{m}$
x_{10}	W_8	M6	$0.18\mu\text{m} \leq W_8 \leq 200\mu\text{m}$
x_{11}	W_9	M7	$0.18\mu\text{m} \leq W_9 \leq 200\mu\text{m}$
x_{12}	W_{10}	M8	$0.18\mu\text{m} \leq W_{10} \leq 200\mu\text{m}$
x_{13}	I	I_{BIAS}	$10\mu\text{A} \leq I \leq 400\mu\text{A}$

Table 1.4 CFOA_{CC} encoding

gene	Design variable	Encoding	Decision space
x_1	L_1	MREF, MA1-MA4, MB1-MB4, M1-M4	$0.18\mu\text{m} \leq L_1 \leq 0.9\mu\text{m}$
x_2	L_2	MA5, MA6, MB5, MB6, M6-M8	$0.18\mu\text{m} \leq L_2 \leq 0.9\mu\text{m}$
x_3	W_1	MREF, MB1-MB4	$0.18\mu\text{m} \leq W_1 \leq 200\mu\text{m}$
x_4	W_2	MA1-MA4	$0.18\mu\text{m} \leq W_2 \leq 200\mu\text{m}$
x_5	W_3	M3	$0.18\mu\text{m} \leq W_3 \leq 200\mu\text{m}$
x_6	W_4	M1	$0.18\mu\text{m} \leq W_4 \leq 200\mu\text{m}$
x_7	W_5	M2	$0.18\mu\text{m} \leq W_5 \leq 200\mu\text{m}$
x_8	W_6	M4	$0.18\mu\text{m} \leq W_6 \leq 200\mu\text{m}$
x_9	W_7	MB5, MB6	$0.18\mu\text{m} \leq W_7 \leq 200\mu\text{m}$
x_{10}	W_8	MA5, MA6	$0.18\mu\text{m} \leq W_8 \leq 200\mu\text{m}$
x_{11}	W_9	M6	$0.18\mu\text{m} \leq W_9 \leq 200\mu\text{m}$
x_{12}	W_{10}	M5	$0.18\mu\text{m} \leq W_{10} \leq 200\mu\text{m}$
x_{13}	W_{11}	M7	$0.18\mu\text{m} \leq W_{11} \leq 200\mu\text{m}$
x_{14}	W_{12}	M8	$0.18\mu\text{m} \leq W_{12} \leq 200\mu\text{m}$
x_{15}	I	I_{BIAS}	$10\mu\text{A} \leq I \leq 400\mu\text{A}$

Table 1.5 Optimized performances for the CFOAs shown in Fig. 1.21

Objective	POWER	$GAIN_X$	BW_X	Z_Y	Z_X	$GAIN_Z$	BW_Z	Z_Z	$GAIN_W$	BW_W	Z_W
Units	Watts	$\lvert\frac{V_X}{V_Y}\rvert$	Hz	Ω	Ω	$\lvert\frac{V_Z}{V_X}\rvert$	Hz	Ω	$\lvert\frac{V_X}{V_Y}\rvert$	Hz	Ω
$CFOA_{AA}$											
NSGA-II	1.61E-4	0.9883	5.54E7	20612	1737	0.9825	5.26E7	391360	0.9849	1.82E6	83091
MOEA/D	1.58E-4	0.9881	6.48E7	32139	1976	0.9711	9.29E7	442150	0.9811	1.30E6	120800
MOPSO	3.77E-4	0.9883	8.79E7	7227	902.6	0.9864	6.28E7	11138	0.9881	4.77E7	2853
$CFOA_{AB}$											
NSGA-II	3.32E-4	0.9851	1.34E8	16870	904.8	0.9943	1.93E8	173730	0.9779	1.42E6	100800
MOEA/D	1.59E-4	0.9881	6.30E7	33626	1921	0.9706	8.42E7	466010	0.9783	7.85E5	185980
MOPSO	3.91E-4	0.9869	1.02E8	10257	922.3	0.9823	9.42E7	15928	0.9749	2.53E7	6699
$CFOA_{AC}$											
NSGA-II	2.70E-4	0.9871	6.54E7	7357	2042	0.9942	6.84E7	134620	0.9778	4.39E7	3968
MOEA/D	3.13E-4	0.9882	6.26E7	95688	1835	0.9801	6.92E7	132850	0.9754	4.39E7	2456
MOPSO	1.13E-3	0.9835	1.40E8	45082	738.7	0.9752	6.98E7	2344	0.9878	1.25E8	645.2
$CFOA_{BA}$											
NSGA-II	3.35E-4	0.987	2.69E7	106960	4071	0.9907	5.68E7	5700	0.9848	7.60E7	2173
MOEA/D	4.73E-4	0.9873	2.70E7	142350	4350	0.9829	6.01E7	4444	0.9871	1.17E8	643.2
MOPSO	1.50E-3	0.9865	7.01E7	20337	1259	0.9912	8.25E7	975	0.9856	1.94E8	275.9
$CFOA_{BB}$											
NSGA-II	6.84E-3	0.9734	7.51E7	269280	1994	0.9735	2.27E8	1007	0.9457	7.89E8	176.6
MOEA/D	4.85E-4	0.9851	2.46E7	756260	6110	0.9829	5.73E7	60735	0.974	1.98E7	9002
MOPSO	6.75E-3	0.9821	1.53E8	27306	821.4	0.9912	1.29E8	709.3	0.9403	3.65E8	337.5
$CFOA_{BC}$											
NSGA-II	8.76E-4	0.986	1.70E7	382410	7816	0.9948	4.08E7	2470	0.9807	1.95E8	313.9
MOEA/D	1.43E-3	0.9857	9.01E7	55392	1471	0.975	7.24E7	100230	0.9839	3.32E7	3423
MOPSO	6.89E-3	0.9828	1.13E8	51479	1054	0.9801	1.32E8	1431	0.9786	4.62E8	148.6

$CFOA_{CA}$											
NSGA-II	3.34E-4	0.9823	6.59E7	172600	1953	0.9898	6.35E7	298510	0.9859	9.25E5	162920
MOEA/D	2.84E-4	0.9825	2.72E7	1012100	5376	0.9924	2.97E7	558540	0.9833	3.52E6	42719
MOPSO	1.13E-3	0.9835	1.40E8	45082	738.7	0.9752	6.98E7	2344	0.9878	1.25E8	645.2
$CFOA_{CB}$											
NSGA-II	6.93E-4	0.9838	1.25E8	92861	736.9	0.9789	8.85E7	141830	0.9747	4.87E6	32926
MOEA/D	4.53E-4	0.9847	5.55E7	277830	2480	0.9801	7.00E7	422190	0.9774	2.08E6	68170
MOPSO	1.77E-3	0.9829	1.85E8	35788	545.5	0.9837	1.10E8	2723	0.9769	7.75E7	1360
$CFOA_{CC}$											
NSGA-II	7.45E-4	0.9835	1.20E8	119030	844.4	0.9885	1.08E8	129250	0.9844	2.34E7	6985
MOEA/D	7.26E-4	0.9858	7.88E7	81182	1552	0.9911	6.97E7	305020	0.9773	3.72E7	5151
MOPSO	2.00E-3	0.9843	1.54E8	21114	698.3	0.9822	7.14E7	28261	0.9763	1.12E8	1463

where $X : \mathbb{R}^n \mid 0.18\,\mu\text{m} \leq L_i \leq 0.9\,\mu\text{m},\ 0.18\,\mu\text{m} \leq W_j \leq 200\,\mu\text{m},\ 10\,\mu\text{m} \leq I_{\text{BIAS}} \leq 400\,\mu A$, is the decision space for the n variables. Finally, $h_k(\mathbf{x}),\ k = 1 \ldots p$ are performance constraints, in our experiments we include the saturation condition in all transistors as constraints.

All CFOAs are encoded with L_i and W_i, where i represents a specific transistor or transistors sharing the same L or W. All L and W values are rounded to multiples of the minimum allowed by the technology process. The variables encoding for some CFOAs from Fig. 1.21 are listed in Tables 1.2–1.4. Table 1.5 shows the optimization results of the nine CFOAs. The three evolutionary algorithms are listed along with the best feasible solutions for the 11 objective functions. From this table, one can select the desired topology accomplishing target specifications [37].

1.5 Conclusions

This chapter summarized recent developments on the analysis and design of active devices by using the nullor concept and pathological elements. Those active devices find applications in the area of analog signal processing, as shown in the following chapters. The optimization of active devices was discussed by presenting the application of three evolutionary algorithms, which provide similar results, but their computational capabilities still being for future research.

Acknowledgment This work is supported by CONACyT/MEXICO under project 131839-Y.

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Chapter 2
Nullors, Their Bipolar and CMOS Implementations and Applications in Analog Circuit Synthesis and Design

Raj Senani, A.K. Singh, Pragati Kumar, and R.K. Sharma

2.1 Introduction

Analog circuits using the traditional voltage mode (VM) op-amps suffer from the well-known drawbacks resulting from the limited slew rate, gain-bandwidth conflict and requirements of passive component-matching in the realization of several functions (such as controlled current sources, non-inverting integrators/differentiators and variable gain differential/instrumentation amplifiers, to name a few). The requirement of component-matching quite often leads to increased sensitivities and may even cause instability in several cases.

During the past four decades, a number of research groups around the world have toiled with the idea of searching for a universal analog building block overcoming the aforementioned limitations. Of various building blocks proposed so far, nullors have been regarded to be universal building blocks since the four controlled sources and all existing analog circuit building blocks can be represented using only nullors

R. Senani (✉)
Division of Electronics and Communication Engineering, Netaji Subhas Institute of Technology, New Delhi, India
e-mail: senani@nsit.ac.in

A.K. Singh
Department of Electronics and Communication Engineering, ITS Engineering College, Greater Noida, India
e-mail: abdheshks@yahoo.com

P. Kumar
Department of Electrical Engineering, Delhi Technological University, New Delhi, India
e-mail: pragati_1964@yahoo.co.in

R.K. Sharma
Department of Electronics and Communication Engineering, Ambedakar Institute of Technology, New Delhi, India
e-mail: 21ravindra@gmail.com

E. Tlelo-Cuautle (ed.), *Integrated Circuits for Analog Signal Processing*,
DOI 10.1007/978-1-4614-1383-7_2,

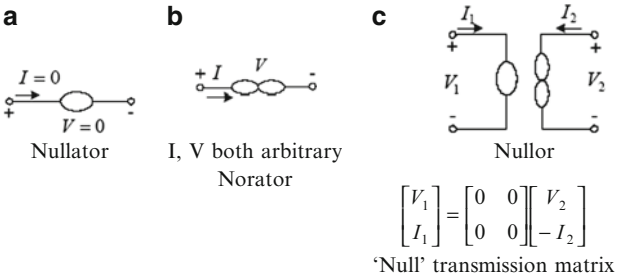


Fig. 2.1 Symbols and definitions of nullator, norator and nullor

and resistors. The floating nullor is a special form of nullor in which ground is external to the four terminals forming the two-port (with nullator comprising the input port and norator comprising the output port).

Although the origin of the concept of nullor itself was advanced as early as 1961–1964, by Carlin and Youla [1, 2] till about 1984 or so, theses elements were largely regarded as theoretical concepts useful only in generating equivalent networks of BJT and Op-Amp based circuits such as gyrators and impedance converters/inverters. However, over the years, nullors have attracted a lot of attention in literature and there have been a large number of publications dealing with applications and implementations of nullors, for instance, see [3] and the references cited therein. It was shown by a number of researchers (such as Nordholt [4], Stevenson [5], Huijsing [6] and Senani [7] (who coined the term "four-terminal floating-nullor" (FTFN) to represent a fully floating nullor) that fully floating versions of Op-Amps [termed as operational floating amplifier (OFA)] and FTFNs are more versatile and flexible building blocks than the traditional op-amps in several applications. Thus, the "OFA" and "FTFN" got going and soon attracted the attention of circuit designers as attractive building blocks for a number of voltage-mode and current-mode signal processing applications. In most of the investigations, the FTFNs have been realized by a composite connection of two CCIIs as suggested by Senani in [7]. The current feedback op-amp AD844 from Analog Devices, which embodies a CCII+ followed by an on-chip buffer, became a preferred choice for implementing FTFNs using the quoted formulation (shown explicitly in Fig. 2.7d in this chapter). However, it is the CMOS implementability of the concept of FTFN which has brought it to the forefront of analog design in more recent years. A number of CMOS implementations of the FTFNs are now known, for instance, see [8–11] and references cited therein.

In this chapter, we deal with the nullors, particularly the floating ones namely, the FTFNs or OFAs, their hardware implementations and applications in circuit synthesis and design.

The symbolic notation and characterizing equations for nullator, norator and nullor have been depicted in Fig. 2.1.

2.2 Nullor Representation of Various Analog Circuit Building Blocks

Since the evolution of nullors, the utility of nullor representation of ideal transistors (both BJT, FET) and the ideal Op-Amps was soon understood [12]. Subsequently, nullors have also been used to model other active building blocks which came into existence later on. Thus, it is well known that an ideal BJT as well as an ideal FET/MOSFET is a three-terminal nullor (see Fig. 2.2a); an ideal op-amp is also a three-terminal nullor with its input terminals representing a nullator and the output terminal with respect to the ground representing the norator; see Fig. 2.2b. A CCII− is equivalent to a three-terminal nullor (Fig. 2.3). This equivalence and the basic properties of nullators and norators and different ways of combining these have been used by Senani [13] and Higashimura and Fukui [14, 15] to synthesize a number of interesting CCII−based inductance simulation circuits.

In principle, since all the four controlled sources (namely, the voltage-controlled/current-controlled voltage/current sources) can be represented by nullators, norators and resistors, a CCII+ can also be represented by nullors but requires two resistors in addition (see Fig. 2.4).

A nullor representation of an operational transconductance amplifier (OTA), voltage follower (VF) and current follower (CF) are shown in Fig. 2.5.

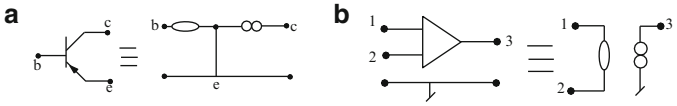


Fig. 2.2 Nullor models of active devices: (**a**) Ideal transistor (BJT). (**b**) Ideal op-amp

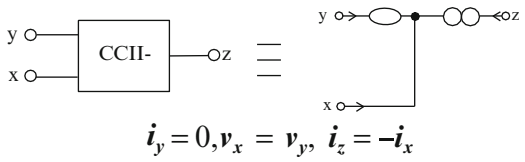


Fig. 2.3 Nullor model of CCII−

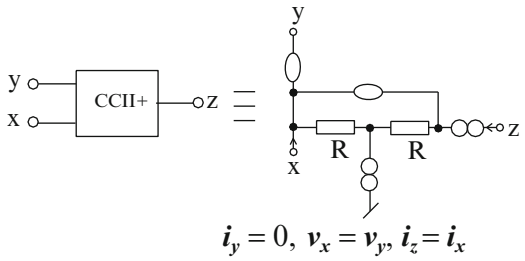


Fig. 2.4 Nullor model of CCII+

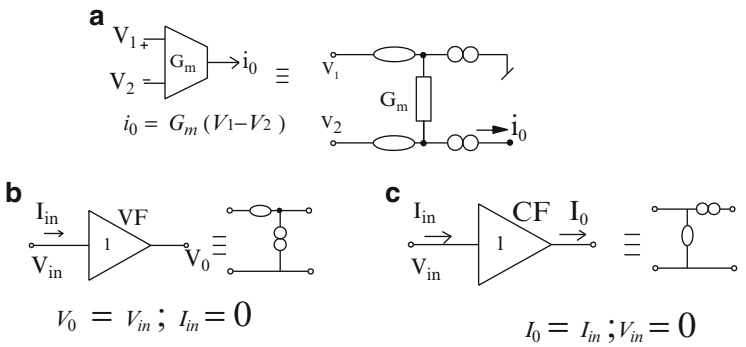


Fig. 2.5 Nullor model of other active building blocks. (**a**) Nullor model of an OTA. (**b**) Nullor model of a VF. (**c**) Nullor model of a CF

Since nullors can be used to represent a variety of active elements, they provide a unified framework not only for analysis, synthesis and design of active networks but also for inter-relating the realizations using different active elements. This fact will be unfolded in subsequent sections of this chapter. However, before proceeding further, we briefly look into the advent of OFAs and FTFNs.

2.3 The Advent of OFA and FTFN

Nordholt in 1982 [4], presented a method of extending op-amp capabilities using current source power supplies. This "extended op-amp" represented a four-port active element which was loosely equivalent to a floating nullor.

Another op-amp-based floating nullor was employed by Stevenson in 1984 in realizing two-way circuits with inverse transmission properties in [5]. This floating nullor circuit was derived from a three-terminal nullor realized with two op-amps, proposed earlier by Cox, Su and Woodland in 1971 [16].

Huijsing in [6, 17], introduced the concept of an OFA which is same as a floating nullor (Fig. 2.6). It was demonstrated that an OFA is particularly useful in realizing current amplifiers, gyrators and instrumentation amplifier with a minimum possible number of external passive components in contrast to conventional op-amp-based circuits for the same functions and hence, an OFA can be regarded to be a versatile building block.[1]

[1]For a differential difference version of an OFA, see [18].

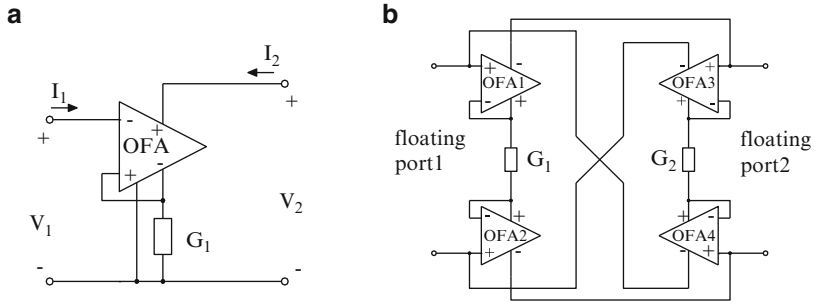


Fig. 2.6 OFA-based circuits (adapted from [17] © 1993 Springer). (**a**) V to I converter $I_1 = G_1 V_1$. (**b**) Floating gyrator ($I_1 = G_2 V_2$, $I_2 = -G_1 V_1$)

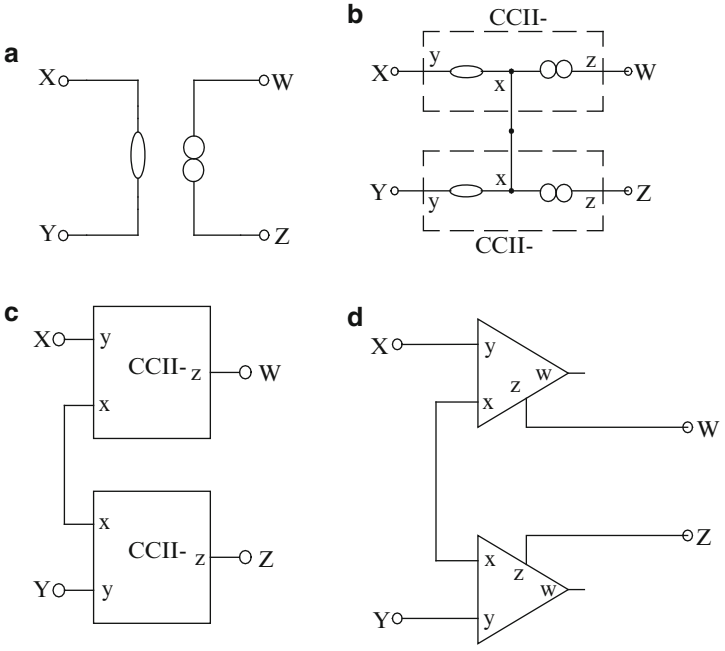


Fig. 2.7 A FTFN implementation using CCIIΘ. (**a**) FTFN. (**b**) A FTFN using two three-terminal nullors. (**c**) FTFN using two CCIIΘ. (**d**) FTFN using two CFOAs

It was shown by Senani in [7, 13] that FTFNs provide a novel solution to the problem of RC active synthesis of floating impedances. A discrete implementation of the FTFN using only an op-amp, OTA and a resistance was proposed in [7]. It was also suggested in [7] that a composite connection of two CCII− can be used to realize an FTFN (see Fig. 2.7a–c of this chapter). This follows from the fact that the representation of FTFN of Fig. 2.7a is equivalent to the combination of two 3-terminal nullors as shown in Fig. 2.7b where each 3-terminal nullor is equivalent to a

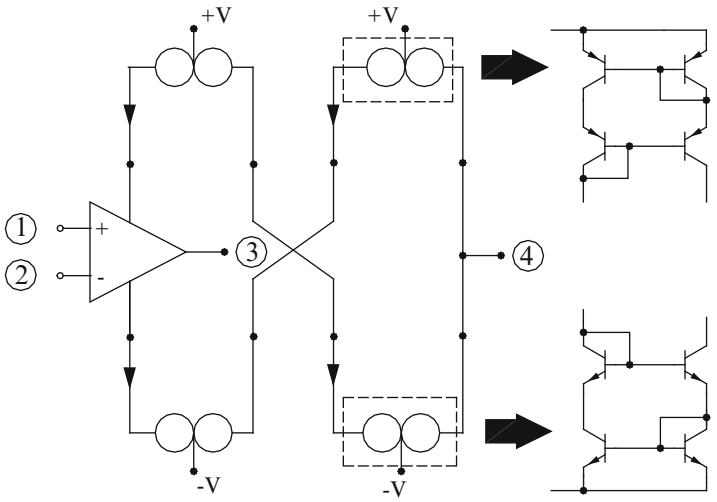


Fig. 2.8 An OMAΘ-based FTFN realization (adapted from [22] © 1994 IEEE)

CCII−, thus, finally, leading to the implementation of Fig. 2.7c. In fact, two CCII+ or two current feedback op-amps (CFOA) such as AD844, which contains a CCII+ and a VF, can also be used to realize an FTFN using the same configuration. In the recent years, the CFOA-based implementation of Fig. 2.7d has been quite frequently used by various circuit designers to implement an FTFN.[2]

Another implementation, which has also been employed in several instances, is the one based upon the concept of an operational mirrored amplifier (OMA) [20, 21], and is shown here in Fig. 2.8 which employs an OFA configuration particularly referred as OMAΘ. The outputs (3) and (4) are, however, dissimilar, the former being a voltage output (with ideally zero output impedance) and the later being a current output having ideally infinite output impedance).

2.4 CMOS and Bipolar Implementations of FTFN

Though a bipolar three-terminal nullor in integratable form was presented as early as in 1977 by Huijsing and Dekorte in [23], the renewed interest in the applications of nullors grew after workable discrete implementations of the floating nullor (FTFN) using the off-the-shelf components as detailed in the previous section started becoming available. Subsequently, during the late nineties, a number of researchers

[2]It was suggested in [19] that the OTA Max 435 could also be used as an FTFN although to the best knowledge of the authors the same does not appear to have been employed as an FTFN experimentally anywhere in the open literature so far.

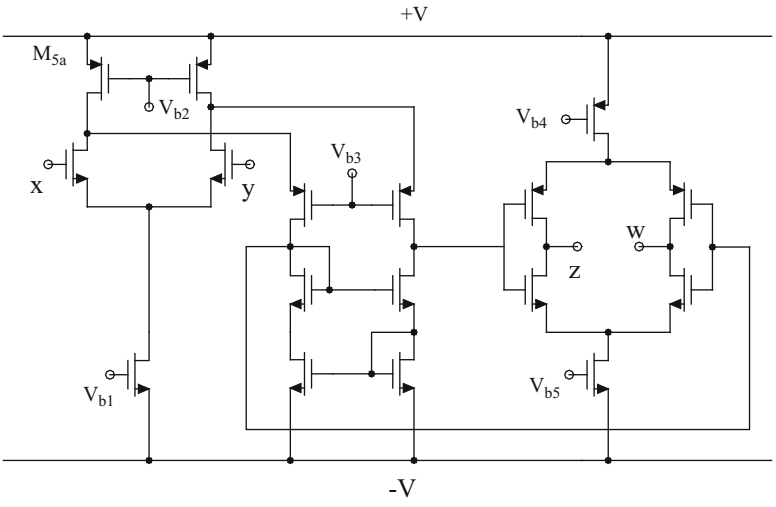


Fig. 2.9 CMOS FTFN proposed by Cam and Kuntman (adapted from [10] © 2000, Taylor and Francis)

worked out a number of CMOS implementations of the FTFN. Because of space limitations, it is difficult to describe all bipolar/CMOS OFAs/FTFNs reported so far, the discussion would be limited to a few representative implementations only.

In 1999, Cam and Kuntman presented a CMOS implementation of two circuits that realize FTFNs [8]. Both these implementations were based on CMOS CCII− architecture. In yet another proposition in 2000, Cam, Toker and Kuntman [9] presented a CMOS implementation of FTFN based on translinear cells. Though not mentioned there explicitly, this implementation is in fact, an interconnection of two translinear CCII+- conforming to the scheme of Fig. 2.7b.

Cam and Kuntman in [10] proposed another CMOS realization of the FTFN which combines the advantages of a cascade of common-source and common-gate amplifiers and a floating current source. This circuit was shown to exhibit wideband operation (unity gain bandwidth in excess of 250 MHz) with a wide dynamic range. Fig. 2.9 shows the circuit proposed in [10].

Tansritat, Unhavanich, Dumawipata and Surakompontorn [24] presented a bipolar implementation of an FTFN with variable current gain which they termed as a tunable FTFN. This implementation is a modification of the basic supply current sensing method for the realization of FTFN. Jiraseri-amornkun, Chipipop and Surakompontorn [25] presented another bipolar implementation of an FTFN with multiple complementary outputs. This implementation is based on a transconductor and an improved translinear cell wherein a number of CMs have been used to replicate the output currents (see Fig. 2.10).

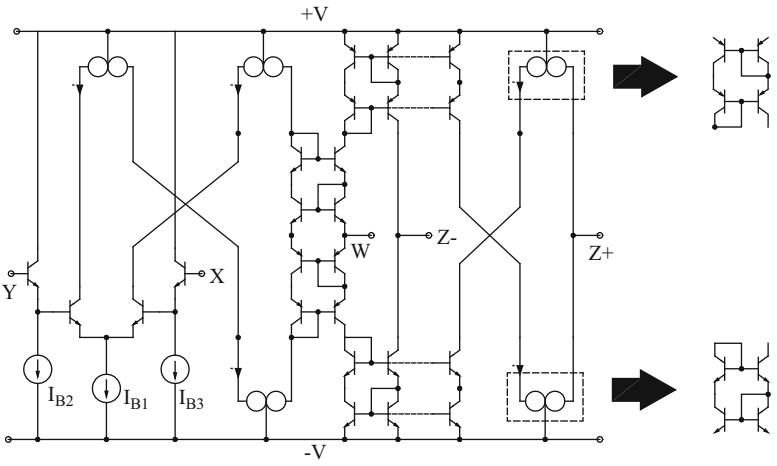


Fig. 2.10 Bipolar implementation of the multiple output floating nullor (adapted from [25] © 2001, IEEE)

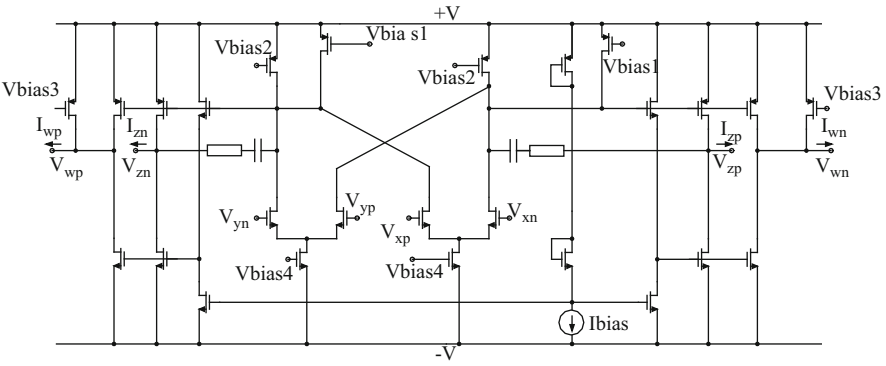


Fig. 2.11 CMOS fully-balanced FTFN (adapted from [11] © 2002, IEEE)

In 2002, Al-Zaher and Ismail in [11] presented the notion of a fully-balanced[3] FTFN and its CMOS implementation. They modified the design of the Op-Amp used in supply current sensing mode, by providing two input differential stages. Provision of two balanced outputs was made instead of a single output from the op-amp. These outputs are finally mirrored to the output port of the FTFN. This circuit is shown in Fig. 2.11 and is characterized by the following equations: $I_{xp} = I_{xn} = I_{yp} = I_{yn} = 0$; $V_{dx} = V_{xp} - V_{xn} = V_{dy} = V_{yp} - V_{yn}$; $I_{dz} = I_{zp} - I_{zn} = -I_{dw} = -(I_{wp} - I_{wn})$.

[3]For another extension of FTFN or OFA termed as "Differential difference operational floating amplifier", the reader is referred to [18].

From survey of literature and the exemplary implementations outlined here, the opinion of the authors is that any "perfect" bipolar/CMOS implementation of the FTFN has yet not been achieved.

In the subsequent sections, we will show important applications of nullors/FTFNs in the areas of floating impedance simulation, generation of equivalent oscillators and universal biquad filter realization which may serve as a motivation for developing a fully integrable bipolar/CMOS FTFN as an off-the-shelf IC.

2.5 Novel Applications of FTFN in Impedance Synthesis

Simulated inductors have important applications in the design of both filters and oscillators. The Antoniou's generalized impedance converter (GIC) [26] based grounded lossless inductance simulation circuit has been the most well-recognized and widely-acceptable solution in many applications. Before the advent of FTFN, the problem of synthesizing floating inductors/impedances (FI) was regarded to be relatively more difficult than that of realizing grounded inductors/impedances. All available circuits/techniques called for either the use of two identical op-amp RC sub-circuits thereby leading to the requirement of double the number of op-amps and RC elements as in [7, 13, 27] or required a large number of resistors with matching constraints and/or cancellation conditions when only two op-amps were employed (as in the circuits of The-Yanagisawa [28]).

A potential application of FTFNs has been in the area of floating impedance simulation where the resulting circuits offer significant advantages as compared to the previously known op-amp RC based FI circuits.

In the following, we highlight a number of techniques of realizing floating impedances of various kinds using the concept of nullors/FTFNs known so far.

2.5.1 Realizing Floating Generalized Impedance Converters/Inverters

The method to be presented here is based upon the following theorem presented in [7] and similar ideas contained in [13]:

Theorem 2.1. *Suppose that a 1-port active network N, containing grounded and floating, two terminal passive elements, nullators and norators realizes a grounded driving point impedance (GDPI)* $Y_{11}(s) = y(s)$. *If a 2-port network N* be formulated from N by disconnecting from ground all grounded passive elements and terminals (of grounded nullators and norators) and joining them together to form port 2, then N* will have short circuit admittance matrix* $[Y]_{N*} = [Y]$ (with $i_1 = -i_2 = y(s)[v_1 - v_2]$).

For a formal proof of the above theorem, the reader is referred to [7].

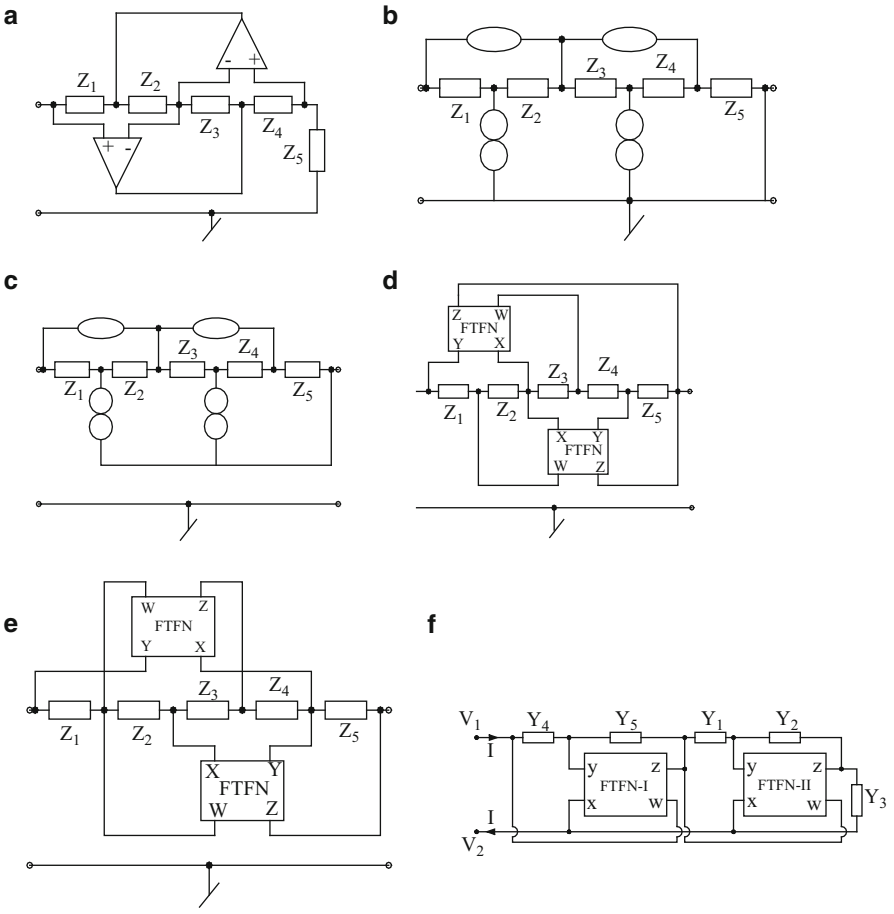


Fig. 2.12 Conversion of GIC-based grounded impedance into FTFN-based floating impedance (**a**) Antoniou's GIC-based grounded impedance (adapted from [26] © 1969 IEE). (**b**) The nullor model of the circuit of (**a**). (**c**) A floating version of the GIC resulting from the application of Theorem 2.1 [7]. (**d**) An FTFN-based floating generalized impedance as per the method first introduced in 1987 in [7, 13]. (**e**) An alternative generalized floating impedance using FTFNs (adapted from [30] © 1997 © 2000 Springer). (**f**) Another FTFN based generalized floating impedance simulation (adapted from [31] © 2001 Springer)

Consider now the Antoniou's GIC shown in Fig. 2.12a. Figure 2.12b shows the nullor model for the same. In Fig. 2.12c, the two-port obtained by ungrounding both the norators as well as the impedance Z_5 have been shown. Thus, from Theorem 2.1 it follows that the circuit of Fig. 2.12c would realize the same impedance in floating form as the grounded impedance realized by the GIC-based circuit of Fig. 2.12a, i.e.

$$Z(s) = \frac{Z_1 Z_3 Z_5}{Z_2 Z_4}$$

An FTFN implementation of the circuit of Fig. 2.12a is shown in Fig. 2.12d. It is, thus, seen that not only one does not require four op-amps and double the number of passive elements (including two capacitors) as required in the known methods of obtaining GIC-based floating impedance (for instance, see [29]) but one does not require any component matching conditions either which are required in the two-GIC-based (hence, four op-amp- based) approach. Note that for inductance simulation, Z_2 or Z_4 is chosen as a capacitor with all other impedances being resistors.

An alternative floating structure of GIC-based generalized floating impedance proposed by Cabeza and Carlosena 1997, [30] is shown here in Fig. 2.12e which also realizes a floating impedance of the same value. Yet another circuit having the same characterization was proposed by Cam, Ozoguz and Kuntman in 2001 [31] as shown here in Fig. 2.12f.

2.5.2 *Generation of CCIIΘ-based Floating Generalized Impedance Converters/Inverters*

Consider now the nullor model for generalized impedance converter/inverter shown in Fig. 2.13a taken from one of the models of reference [32]. By a routine analysis, the admittance looking into terminals 1 and 2 is found to be

$$y_0 = \frac{y_1 y_3 y_5}{y_2 y_4}$$

It is immediately clear from this nullor circuit, by appropriately defining the second port, a number of two port immittance inverter/converter circuits can be generated. Since none of the terminals or impedances is connected to ground, Theorem 2.1 applies. Since each pair of nullator, norator has common terminal, both the nullors are realizable with a CCII−. It may appear that a total number of six different floating generalized impedance converter/inverter should be derivable from the model of Fig. 2.13a however, after discarding the redundant cases; it is found that only three distinctly different configurations [27] are possible which are shown here in Fig. 2.13b.

It may be pointed out that all the three configurations of Fig. 2.12d–f as well as those of Fig. 2.13b can be used to realize a number of useful floating impedances. In this context, it may be noted that the three most common elements, from the point of view of various active network applications, are the synthetic floating L, floating FDNR $(Z(s) = 1/Ds^2)$ and floating FDNC $(Z(s) = Ms^2)$ elements. With the proposed GPIC/GPII configurations, these are realizable more efficiently than the CC- based simulations previously known.

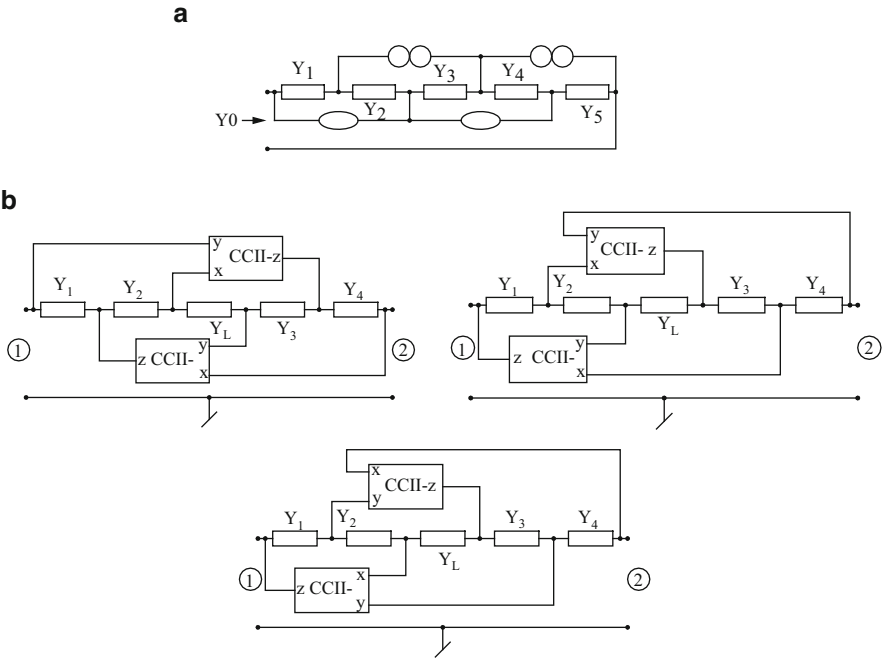


Fig. 2.13 (**a**) A nullor model of generalized impedance converter/inverter (adapted from [32] © 1970 IEEE). (**b**) Three CCIIΘ-based floating generalized impedance converter/inverter derived from nullor model of (**a**) (adapted from [27] ©1986 IEEE)

(a) Synthetic floating inductance (FI)-choosing Z_3 as a capacitor and remaining impedances as resistors, the simulated L is given by

$$L_{1-2} = \frac{C_3 R_1 R_4 R_L}{R_2} \tag{2.1}$$

(b) Floating FDNR- choosing Z_1 and Z_L as capacitors, the circuit simulates a floating FDNR having value

$$D_{1-2} = \frac{C_1 C_L R_2 R_3}{R_4} \tag{2.2}$$

(c) Floating FDNC– choosing Z_2 and Z_3 as capacitors, the circuit simulates a floating FDNC having value

$$\mathrm{M}_{1-2} = \mathrm{R}_1 \mathrm{R}_4 \mathrm{R}_\mathrm{L} \mathrm{C}_2 \mathrm{C}_3 \tag{2.3}$$

It is worthwhile to point out that the previously published CC-networks simulating floating ideal L or D elements [33–38] use three to four CCs. Also, the ideal floating L (and also the corresponding D element), outlined by Paul and Patranabis [39] as an application example of their proposed floating NIC too employs four CCs. In comparison, the use of the proposed networks of Fig. 2.13b makes it possible to realize these elements with only two FTFNs or two CCs, while providing the merits of lack of any component-matching requirement, low sensitivities to element value changes and single-resistance-tunability of the realized immittances. For the CC-based realization of lossy FIs using nullors see [40].

2.5.3 *Generation of Lossless Floating Inductance Circuits Using a Single FTFN*

To the best knowledge of the authors, only four single op-amp lossless grounded inductance circuits appear to have been known in the earlier literature till date which were proposed by Orchard-Willson 1974, [41], Schmitt-Lee 1975, [42], Ramsey 1978, [43] and Horn-Moschytz 1979, [44]. Here, we demonstrate how all these four circuits can be transformed as per the techniques of [7, 13] into as many as *sixteen*[4] lossless FI circuits using Theorem 2.1 in conjunction with Theorem 2.2 (to be outlined subsequently). Consider the grounded inductance simulation circuit of Horn-Moschytz [44] which realizes an inductance value

$$L = CR_3R_6\left(1+\frac{R_2}{R_1}\right)\left(1+\frac{R_5}{R_4}\right)^{-1} \text{ provided } \frac{R_2}{R_4} = \frac{R_1+R_6}{R_5} + \frac{R_1}{R_3}\left(1+\frac{R_6}{R_5}\right) \tag{2.4}$$

The process of deriving an FTFN/OFA based FI circuit corresponding to this circuit is shown in Fig. 2.14a to c is self-explanatory.

It is, however, interesting to note that from the FI circuit of Fig. 2.14c, three additional FI circuits can be derived as follows:

(1) An equivalent of the circuit of Fig. 2.14c can be generated invoking the following theorem:

Theorem 2.2. *If a 2-port active-RC network* N_1 *containing floating two terminal passive elements, floating nullators and floating norators has short circuit admittance matrix*

$$[Y_1] = y(s)\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \tag{2.5}$$

[4]In [13] 32 equivalent FI realizations were stipulated using a two-op-amp FTFN available then.

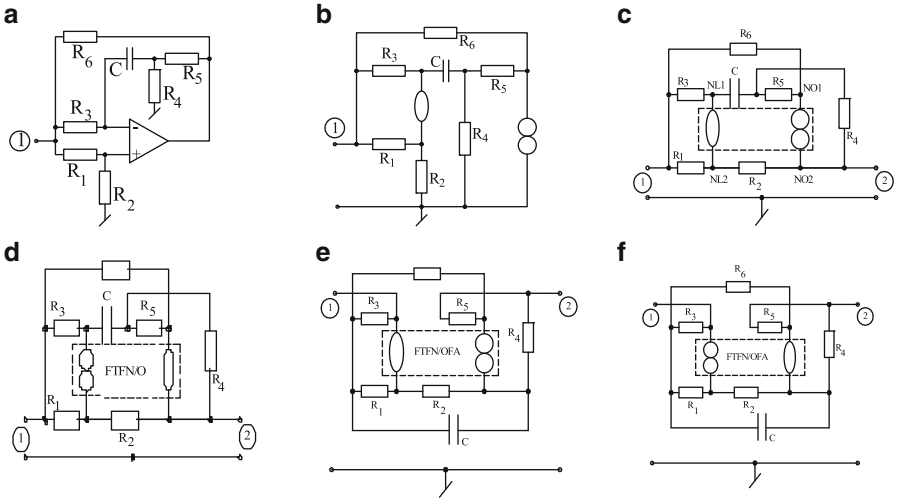


Fig. 2.14 (**a–c**) Method of transformation of a lossless grounded inductor into a FI using an FTFN or OFA [7, 13]. (**d–f**) Three other equivalent FIs having same value of realized inductance under the same condition of realization

then if it is transformed into another network N_2 *by interchanging all nullators and norators, the transformed network has the same Y-matrix.*

By applying Theorem 2.2 to the FI circuits of Fig. 2.14c, the resulting second equivalent FI turns out to be as shown in Fig. 2.14d.

(2) Owing to simulating a lossless inductance employing a single floating capacitor, the two port network of Fig. 2.14c can be looked upon as a floating gyrator with terminals 1 and 2 constituting the input port and terminals 3 and 4 (between which the capacitor is connected) constituting the output port. Thus, gyrator action is available even if the input and the output ports are transposed i.e. the capacitor is connected between terminals 1 and 2 and the floating impedance is looked between 3 and 4. This results in the third equivalent FI shown in Fig. 2.14e.

(3) Finally, the fourth and the last additional equivalent FI is obtained by swapping the nullator and norator in the circuit of Fig. 2.14f in accordance with Theorem 2.2.

Lastly, it must be pointed out that twelve additional lossless FI circuits, each employing only a single FTFN, are similarly realizable starting from the lossless grounded inductance circuits of Orchard-Wilson [41], Schmidt-Lee [42] and Ramsey [43] by following the above outlined procedure.

It may be mentioned that the basic ideas outlined above had been elaborated by Senani in [7] and [13].

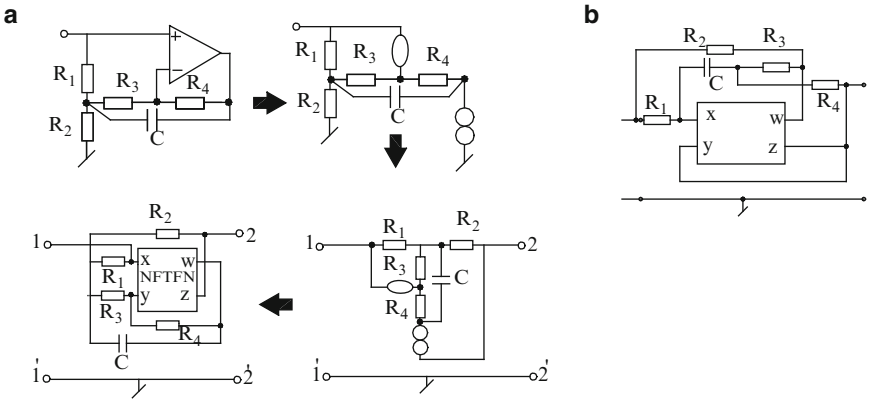


Fig. 2.15 Conversion of an op-amp based single resistance controllable GI into FTFN-based FI of the same form: (**a**) Floating series RL, (**b**) floating parallel RL

2.5.4 Single-Resistance-Tunable Lossy Floating Inductance Simulation Using Only a Single FTFN

The technique explained in Sect. 2.5.1 above opens the way for evolving a large number of floating impedance circuits starting from various known grounded GDPI circuits. Figure 2.15 shows the conversion of a simulated single resistance tunable grounded lossy inductance into a FI of the same value. Starting from the grounded inductance circuit of [45], its nullor model is drawn, a two port is created by ungrounding all grounded elements/terminals where from finally, a circuit simulating the same kind of impedance in floating form using FTFN is derivable (see Fig. 2.15).

Thus, GDPI using an op-amp as well as the derived FI using an FTFN both simulate series RL impedance with inductance value given by

$$R_s = R_1 + R_2 + \frac{R_1 R_2}{R_3} \cdot L_s = CR_1R_2\left(1 + \frac{R_4}{R_3}\right) \tag{2.6}$$

where from it is seen that L_S is independently adjustable by R_4 which does not appear in the expression for R_s.

A single FTFN-based floating parallel RL impedance possessing single- resistance controllability of inductance value is similarly derivable from the tunable grounded parallel RL impedance circuits of [45] is shown in Fig. 2.15b for which equivalent resistance R_p and inductance L_p are given by

$$\frac{1}{R_p} = \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{R_3}{R_1R_2}\right) \cdot L_p = (CR_1R_2)\left(1 + \frac{R_3}{R_4}\right)^{-1} \tag{2.7}$$

2.6 Use of Nullors in Deriving Equivalent Circuits of Single-Resistance-Controlled Oscillators (SRCO)

Although there have been several efforts in synthesizing oscillators using FTFNs as active elements, for instance, see [46–48] and the references cited therein, the potential of FTFNs has been particularly appealing in generating oscillator-equivalences which quite often have resulted in alternative oscillator topologies possessing properties not available in the parent circuits. In this section, we will, therefore, focus only on this particular application of FTFNs in the domain of oscillator design.

A general theory of deriving equivalent forms of op-amp RC sinusoidal oscillators using the formalism of nullors was presented earlier in [22]. This theory is based upon the following theorems:

Theorem 2.3. *Suppose there is a sinusoidal oscillator N which employs m nullators, m norators and an arbitrary number of passive resistors and capacitors. If N is transformed into another circuit* N^* *by interchanging all nullators and norators then* N^* *has the same characteristic equation (CE) as that of N.*

Theorem 2.4. *Corresponding to any RC-nullor oscillator having n nodes (excluding the ground node which is taken "external" to the circuit) and consisting of m nullors along with an arbitrary number of passive resistor and capacitors, there are 2n grounded nullor-RC equivalent oscillator circuits having the same CE since in an oscillator, because there is no external input, the ground node can be chosen arbitrarily without affecting the CE.*

In [22] it was shown that the classical Wein bridge oscillator has ten equivalent forms.[5] This number was further increased in [51] to sixteen by considering the junction of the series RC branch as another node.

It was shown in [22] that some of such additional realizations are likely to have some interesting properties not available in the original circuit.

In the following, we show how applying the above theorems on an existing SRCO we can derive a number of equivalents having same characterization and that some of the derived equivalents indeed have new and interesting properties not available in the original circuit.

Let us now consider the single op-amp RC SRCO of [52] reproduced here in Fig. 2.16.

This oscillator is characterized by the following condition of oscillation (CO) and frequency of oscillation (FO):

$$\frac{R_4}{R_3} = \frac{2R_5}{R_2} \text{ (with } C_1 = C_2 = C) \text{ and } f_0 = \frac{1}{2\pi C}\sqrt{\frac{1+\left(\frac{R_3+R_4}{R_1}\right)}{R_2R_3}} \tag{2.8}$$

[5] It is worthwhile to point out that the theory of [22] was usefully extended to derive a class of two FTFN-based SRCOs employing a minimum possible number of resistors in [49]. Yet another two FTFN-based GC SRCO was presented in [50].

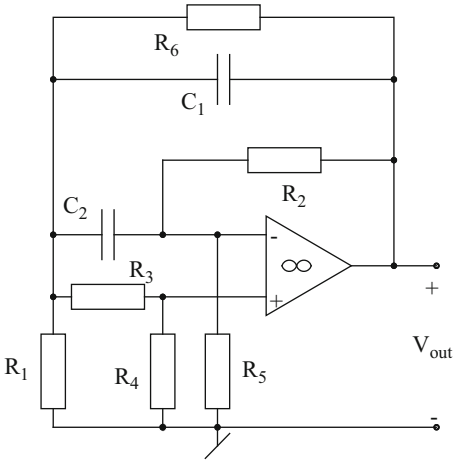


Fig. 2.16 Senani's SRCO (adapted from [52] © 1979 IEEE)

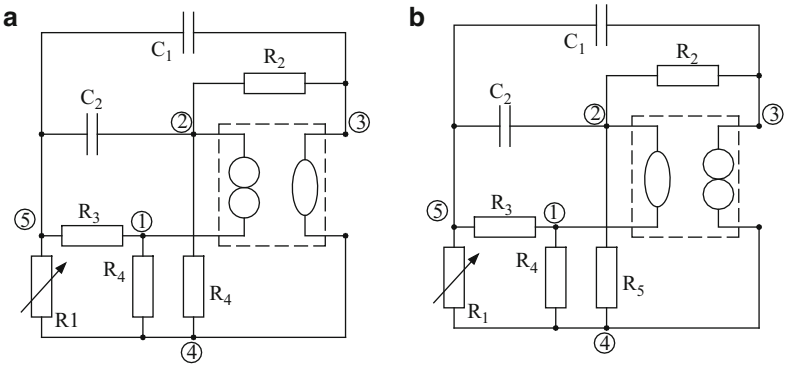


Fig. 2.17 (**a**) A nullor model of the SRCO of Fig. 2.16. (**b**) An alternative nullor model of the same circuit

From the above it is seen that CO is controllable independently by R_5 where as FO is independently controllable by R_1.

A nullor model of this SRCO, with ground node excluded, is shown in Fig. 2.17a. Figure 2.17b shows an alternative nullor model having the same CE obtained by applying Theorem 2.3. Since each model contains five nodes it follows from Theorem 2.4 that for each model, ground node can be selected in five different ways thereby leading to a total of ten equivalent SRCOs having the same CE. It may be noted that only four of these would be realizable with a normal op-amp while the remaining six require an FTFN (Fig. 2.18).

Two of the new SRCOs generated by this methodology (resulting from treating node 1 as ground) employ grounded capacitors as preferred for IC implementation and are particularly note worthy since this feature was not present in the original circuit of Fig. 2.16. Also, four of the quoted ten circuits can provide explicit current outputs-again a feature which was not there in the original circuit.

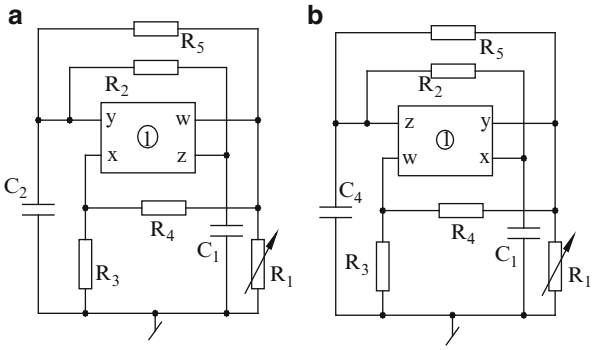


Fig. 2.18 (**a**) FTFN-based grounded capacitor version of the SRCO of Fig. 2.16. (**b**) An alternative FTFN-based grounded capacitor version of the SRCO of Fig. 2.16

Thus, the examples in [22, 51] and the one shown here prove the potential of FTFNs in generating new oscillator configurations possessing interesting properties, beyond their normal use as active elements in oscillator realization as demonstrated in [46–48].

2.7 Use of FTFN in Realization of Universal Biquad, Fully Differential and Inverse Filters

In the area of active filter design, the FTFNs have been shown to be very useful building blocks in realizing universal biquad filters, inverse filters and fully differential biquad filters. A brief account of some important works in this direction is provided in the following.

2.7.1 Universal Current-mode Biquad

Although a number of attempts have been made by various researchers in evolving universal biquads in current mode (CM), trans-admittance mode or so the called mixed-mode using a variety of building blocks, a particularly simple CM biquad with a minimum possible number of passive elements (namely only four) along with a minimum possible number of FTFNs to provide three explicit current outputs was proposed by Cicekoglu [53] and is reproduced here in Fig. 2.19.

Selecting $Y_1 = 1/R_1$, $Y_2 = sC_2$, $Y_3 = 1/R_3$, and $Y_4 = sC_4$, the circuit realizes a high pass (HP) response at i_{01} and a band pass (BP) response at i_{02} with relevant parameter given by

$$\omega_0 = \sqrt{\frac{1}{R_1 R_3 C_2 C_4}}, \text{ and } Q_0 = \sqrt{\frac{R_3 C_4}{R_1 C_2}} \tag{2.9}$$

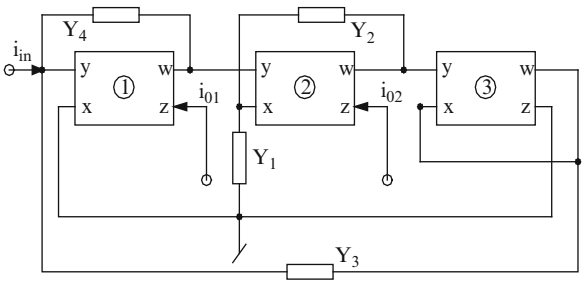


Fig. 2.19 Current-mode biquad using FTFN (adapted from [53] © 2001 IEEE)

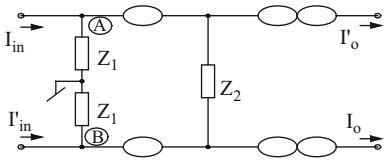


Fig. 2.20 Fully-differential CM building block (adopted from [54])

On the other hand, by selecting $Y_1 = sC_1$, $Y_2 = 1/R_2$, $Y_3 = sC_3$, $Y_4 = 1/R_4$, the same circuit realizes a low pass (LP) response at i_{01} and a BP response i_{02} with relevant parameters being given by

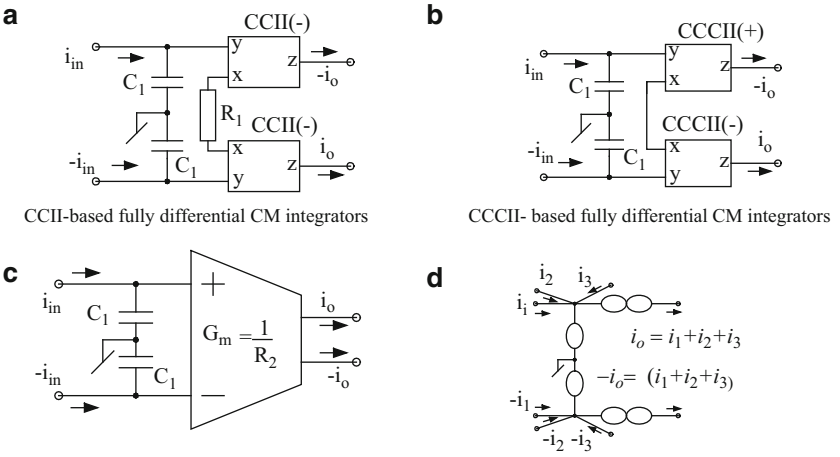
$$\omega_0 = \sqrt{\frac{1}{R_2 R_4 C_1 C_3}} \text{ and } Q_0 = \sqrt{\frac{C_1 R_2}{C_3 R_4}} \tag{2.10}$$

The advantageous features of this circuit are the availability of ideally zero input resistance, ideally infinite output resistances (both expected from an ideal CM filter) together with the use of a minimum possible number of passive elements.

2.7.2 Fully Differential CM Biquad

As another example of the potential of the nullors, we next demonstrate their use in the realization of a fully differential filter. There has been lot of interest in literature in realizing fully differential filters in both VM and CM because of their capability of eliminating common-mode noise. In the following, we discuss a nullor-based approach for constructing a fully differential CM building block which can be used to realize a fully differential CM universal filter in a configuration employing two fully differential integrators and a fully differential summer with complimentary CM outputs. A fully differential CM building block is shown in Fig. 2.20 and is characterized by $i_0 = -i_0' = Z_1/Z_2(i_{in} - i_{in}')$.

Thus, depending upon the choice (resistive/capacitive) of the impedances Z_1 and Z_2, this block can realize fully differential scalar, integrator or differentiator. With both impedances as resistors and summing nodes created at nodes "a" and



CCII-based fully differential CM integrators

CCCII- based fully differential CM integrators

DOTA based fully differential CM integrators

Summer with complementary CM outputs

Fig. 2.21 Various realizations of the fully differential CM integrators (adapted from [54])

"b" the configuration can realize fully differential CM summer. We now show that, as widely understood, nullors are indeed useful in realizing and unifying circuit structures using all such different kinds of active elements which can be modeled in terms of nullors. In the present case, the nullor-based configuration of Fig. 2.20 leads to a number of different practical implementations, three of which using CCII−, CCCII+ and differential output OTA (DOTA) are shown in Fig. 2.21.

It is worthwhile to mention that in all cases, the internal hardware of the employed building blocks can be easily modified to facilitate multiple and complementary outputs which should be useful in interconnecting two or more of such configurations as well as to provide feedback paths and summations as needed for either biquad realization or higher order filter designs. Alternatively, differential summer can also be realized by the nullor-based structure of Fig. 2.21d and an exemplary configuration of a fully differential CM universal filter obtained in this manner is shown in Fig. 2.22 which realizes LP, BP, HP outputs where from HP and LP outputs can be combined to realize a band stop filter while HP and BP (inverting) can be combined to realize an all pass filter without requiring any component-matching conditions other than the equality of capacitors (which is prevalent in almost all earlier fully differential filter structures as well). A notable property of the circuit of Fig. 2.22 is that bandwidth and pole frequency can be orthogonally tuned by R_1 and R_2 respectively: the gain is fixed at unity in all the cases. It has been shown elsewhere [54] that this approach can also be extended to the design of higher order filter.

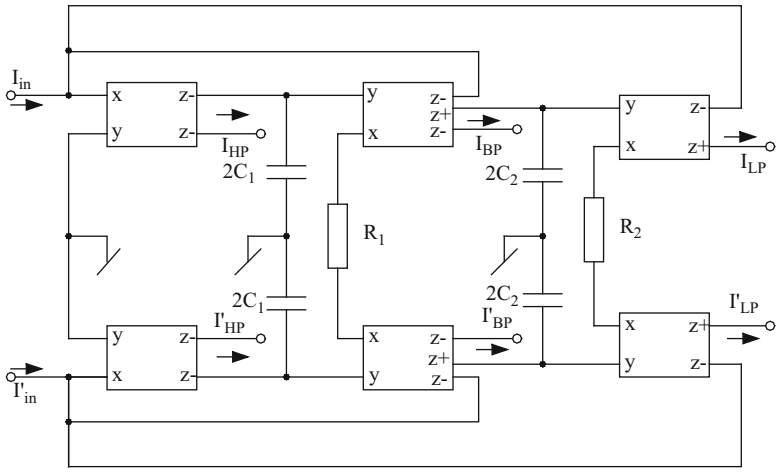


Fig. 2.22 A fully differential CM universal filter (adapted from [54])

The three transfer functions realized by the circuit of Fig. 2.22 are given by

$$\frac{I_{BP}}{I_{in}} = -\frac{s\left(\frac{1}{C_1R_1}\right)}{\Delta} : \frac{I_{LP}}{I_{in}} = \frac{\frac{1}{C_1C_2RR_2}}{\Delta}; \frac{I_{HP}}{I_{in}} = \frac{s^2}{\Delta} \quad where \quad \Delta = s^2 + \frac{s}{C_1R_1} + \frac{1}{C_1C_2RR_2} \tag{2.11}$$

2.7.3 Design of CM Inverse Filter

In the area of filter design another interesting application of FTFNs has been in the derivation of the so-called "inverse filters" [55]. Out of the various approaches of designing inverse filters published earlier, we present here a specific procedure of realizing a current mode FTFN-based inverse filter from a given op-amp RC-based filter based upon [55] which consists of the following steps:

(1) Obtain a nullor model of the given op-amp RC filter by replacing the op-amp by nullator-norator pair, (2) swap the driving source and the norator in the above model, (3) apply RC:CR dual transformation on the model of the previous step, (4) obtain the final inverse filter by replacing the nullors with FTFNs.

An exemplary inverse filter generated by using the above steps, is demonstrated in Fig. 2.23.

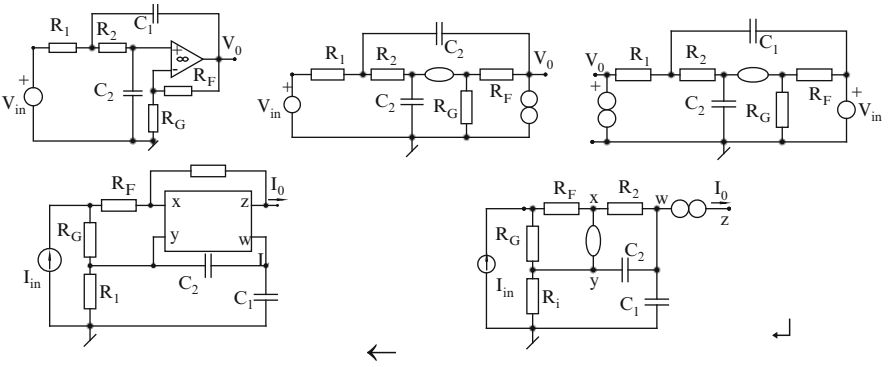


Fig. 2.23 Design of an inverse filter using FTFN (adapted from [55] © 1999 IEE)

The final CM inverse function realized by FTFN circuit of Fig. 2.23 is

$$\frac{I_0}{I_{in}} = \left[\frac{k/(R_1R_2C_1C_2)}{s^2 + s\left(\frac{1}{R_1C_1} + \frac{1}{R_2C_1} + \frac{1-k}{R_2C_2}\right) + \frac{1}{R_1R_2C_1C_2}} \right]^{-1} \tag{2.12}$$

where $k = 1 + (R_F/R_G)$.

2.8 Systematic Synthesis of Active RC Circuits Using Nullors

Haigh and co-workers [56] have carried out pioneering work on the systematic synthesis of active RC networks using nullors. While it is difficult to summarize the entire body of their work in a chapter of limited length, we outline here an exemplary synthesis of an immittance inverter circuit which evolves in a systematic way by expansion of the relevant port admittance matrices such that the circuit topology emerges naturally from the synthesis procedure.

We start from the common knowledge that an immittance inverter can be synthesized by a parallel back-to-back connection of a positive voltage controlled current source (VCCS) and a negative VCCS characterized by the two port admittance matrices: $\begin{bmatrix} 0 & 0 \\ G_1 & 0 \end{bmatrix}$ and $\begin{bmatrix} 0 & 0 \\ -G_2 & 0 \end{bmatrix}$ respectively.

Taking the first matrix, we move the element G_1 to the main diagonal so that it can describe a grounded resistor. This is accomplished by adding a blank row 3 and column 3, then moving G_1 term from column 1 to column 3 and from row 2 to row 3 and then adding a nullator between nodes 1 and 3 and a norator between nodes 2 and 3 in order to allow the G_1 term to move to the 3, 3 position, as shown in the following equation:

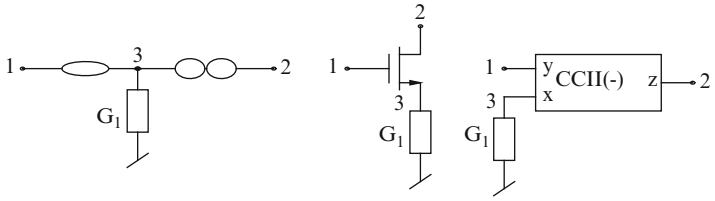


Fig. 2.24 The synthesis of noninverting VCCS and its FET and CCII− realizations (adapted from [56] © 2005 Springer)

$$\left[\begin{array}{cc|c} 0 & 0 & 0 \\ G_1 & 0 & 0 \\ \hline 0 & 0 & 0 \end{array}\right] = \overline{\left[\begin{array}{cc|c} 0 & 0 & 0 \\ G_1 & 0 & 0 \\ \hline 0 & 0 & 0 \end{array}\right]} = \overline{\left[\begin{array}{cc|c} 0 & 0 & 0 \\ 0 & 0 & 0 \\ \hline 0 & 0 & G_1 \end{array}\right]}$$

The circuit realizations corresponding to the last matrix of the above equation are shown in Fig. 2.24.

For the negative VCCS, we note that a negative conductance can be identified with one of the two off- diagonal negative elements describing a non-grounded conductance. The description of non-grounded conductance needs two rows or two columns. Thus, we introduce two blank rows and two blank columns, thereby introducing two new nodes 3 and 4 in the matrix.

$$\left[\begin{array}{cc} 0 & 0 \\ -G_2 & 0 \end{array}\right] \equiv \left[\begin{array}{cc|cc} 0 & 0 & 0 & 0 \\ -G_2 & 0 & 0 & 0 \\ \hline 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{array}\right] \equiv \overline{\left[\begin{array}{cc|cc} 0 & 0 & 0 & 0 \\ -G_2 & 0 & 0 & 0 \\ \hline 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{array}\right]} \equiv \overline{\left[\begin{array}{cc|cc} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \hline 0 & 0 & 0 & 0 \\ 0 & 0 & -G_2 & 0 \end{array}\right]}$$

Now connecting a nullator from node 3 to node 1 and a norator from node 4 to 2 will permit—G_2 to move to position 4, 3. Since an indefinite admittance matrix must have sum of each row and each column equal to zero hence, row 0 and column 0 should contain terms G_2, $-G_2$ and G_2, as shown.

$$\overline{\left[\begin{array}{cc|cc} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \hline 0 & 0 & 0 & 0 \\ 0 & 0 & -G_2 & 0 \end{array}\right]} \equiv \begin{matrix} \\ \\ \\ G_2 \end{matrix} \overline{\left[\begin{array}{cc|cc} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \hline 0 & 0 & G_2 & 0 \\ 0 & 0 & -G_2 & 0 \end{array}\right]} \begin{matrix} \\ \\ -G_2 \\ G_2 \end{matrix} \equiv \left[\begin{array}{cc|cc} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \hline 0 & 0 & G_2 & -G_2 \\ 0 & 0 & -G_2 & G_2 \end{array}\right]$$

Now connection of a norator between nodes 3 and 0 will allow the row 0 term to be brought to row 3. Similarly, connection of nullator between nodes 4 and 0 will allow column 0 term to be brought to column 4 as shown. The final admittance matrix in

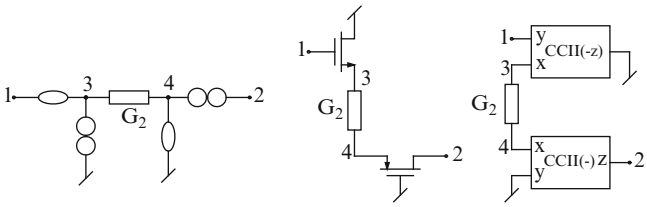


Fig. 2.25 Synthesis of inverting VCCS using nullor MOSFET and CCs (adapted partly from [56] © 2005 Springer)

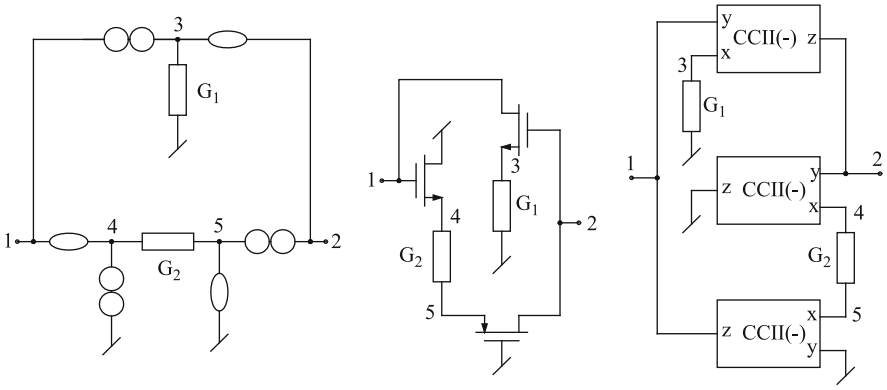


Fig. 2.26 Synthesis of an immittance inverter using nullors, MOSFET and CCIIs (In the CCIIs circuits, all three CCIIs could also be taken as CCII+ (adapted partly from [56] © 2005 Springer)

the above equation shows the connections of two nullors and a floating conductance representing the inverting VCCS, the final circuit for which is shown in Fig. 2.25 along with its FET and CCII− based realizations (not included in [56]).

Finally, the complete nullor representation of the immittance inverter and its FET- and CCII−based realizations are shown in Fig. 2.26.

2.9 Current Mirror and Voltage Mirror as Two New Pathological Elements

While a CCII− can be represented by a three terminal nullor without requiring any resistors, however, a CCII+ cannot be realized by nullators and norators only and does require at least two resistors see Fig. 2.4. This difficulty motivated Awad and Soliman [57, 58] to propose two new pathological elements namely the CM and VM which are basically used to represent active devices with current or voltage reversing properties. A CM is a two port network element for which V_1 and V_2

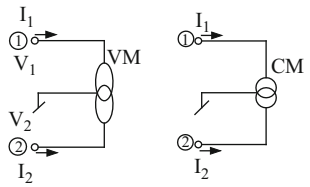


Fig. 2.27 The symbols of CM and VM (adapted from [58] © 2002 Springer)

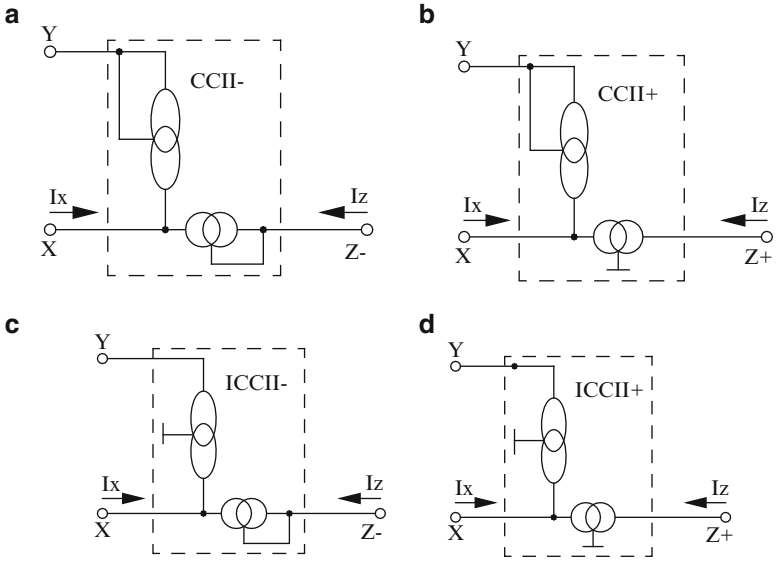


Fig. 2.28 Realization of various building blocks using VM–CM pair. (**a**) CCII−. (**b**) CCII+. (**c**) ICCII−. (**d**) ICCII+ (adapted from [59] © 2010 John Wiley & Sons)

are arbitrary and $I_1 = I_2$ and they are also arbitrary. The VM is a lossless two-port network element characterized by $V_1 = -V_2$ and $I_1 = I_2 = 0$. The symbolic notations of the CM and VM are shown in Fig. 2.27.

Saad and Soliman in 2010 [59] demonstrated that CM-VM pair constitutes an universal active element since it is capable of representing an op-amp as well as all the four types of current conveyors namely CCII−, CCII+, Inverting CCII− (ICCII−) and inverting CCII+ (ICCII+) without using any resistors (see Fig. 2.28).

Soliman and his co-worker have employed nullator–norator–CM–VM in the systematic synthesis of analog circuits, however, for a detailed discussion of these the reader is referred to [60] and the references cited therein.

2.10 Current Trends and Directions for Future Research

Although about a dozen different CMOS FTFN structures have been reported in literature, a perfect implementation of nullor which can be produced as an IC to take advantage of its universality[6] is still awaited.

It is also observed from a review of literature that applications of nullors have not been explored as exhaustively as these have been evolved using other devices like operational amplifiers, OTAs, current conveyors and current feedback amplifiers, etc. A good mixed mode universal filter realized with FTFNs providing most of the desirable properties is yet to be evolved and appears to be a worthwhile problem for future investigations.

The more recent works on the utilization of nullors include creation of general admittance matrix stamps for the operational trans-resistance amplifier (OTRA) current output amplifier (COA) [63]. Work is also being conducted by Tlelo-Cuautle and his co-workers [64] on the pathological element based active device modeling and their applications to symbolic analysis. The concept of nullors has also been employed in developing systematic synthesis procedure for realizing CFs and VMs [65].

Thus, continued work on nullors is currently dominantly motivated by the evolution of systematic synthesis procedures using nullator–norator–CM–VM elements for realizing impedance converter inverters, biquad filters and oscillators and it is expected that nullors (or FTFNs) in conjunction with CM-VM pair will continue to find more and more interesting applications in circuit synthesis and design, in days to come.

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[6]It is worth pointing out that it has been shown in [61] that there are nine distinctly different analog building blocks which can be said to be “universal” in a generic sense. Also, it may be noted that as pointed out in [40] and [62], the so called PFTFN or FTFN+-(based on norator +) are strictly speaking not floating nullors and hence, are not included in this chapter.

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Chapter 3
Current-Feedback Op-Amps, Their Applications, Bipolar/CMOS Implementations and Their Variants

R. Senani, D.R. Bhaskar, S.S. Gupta, and V.K. Singh

3.1 Introduction

The current-mode techniques have given way to a number of important analog signal processing/signal generating circuits as is evident from a vast amount of literature on current-mode circuits published over the past 35 years. Due to the advances made in integrated circuit (IC) technology circuit designers have quite often exploited the potential of current-mode analog techniques for evolving elegant and efficient solutions to several circuit design problems. As a consequence, the current-mode approach has often been claimed to provide one or more of the following advantages in analog circuit design: higher frequency range of operation, lower power consumption, higher slew rates, improved linearity, better accuracy as well as reduced component-count and elimination of passive component-matching requirements.

R. Senani (✉)
Division of Electronics and Communication Engineering, Netaji Subhas Institute of Technology, New Delhi, India
e-mail: dr_senani@yahoo.com

D.R. Bhaskar
Department of Electronics and Communication Engineering, Jamia Millia Islamia, New Delhi, India
e-mail: dbhaskar@jmi.ac.in

S.S. Gupta
Department of Industrial policy and promotion, Ministry of Commerce and Industry, New Delhi, Government of India
e-mail: ss.gupta@nic.in

V.K. Singh
Department of Electronics Engineering, Institute of Engineering & Technology, Lucknow, UP, India
e-mail: vksingh@ietlucknow.edu

E. Tlelo-Cuautle (ed.), *Integrated Circuits for Analog Signal Processing*,
DOI 10.1007/978-1-4614-1383-7_3,

3.2 The Evolution of Current Conveyors

The most popular current-mode building blocks have been, undoubtedly, the current conveyors (CC) introduced by Smith and Sedra. The first generation current conveyor (CCI) was introduced in 1968 [1] and was later refined to second generation current conveyor (CCII) by Sedra and Smith in 1970 [2]. Because of the extensive work done by researchers for more than four decades on the hardware implementation and applications of CCs, coupled with the commercial availability of a number of IC CCs (such as PA630A from Phototronics Corporation of Canada, CCII01 from LTP Electronics, AD844 from Analog Devices Inc. and more recently, MAX4198 from Maxim Integrated Products), the CCs have emerged as an important class of active building blocks with properties that enable them to rival the traditional voltage mode op-amp (VOA) in a wide range of applications.

3.3 The Current Feedback Op-amp

A closely related building block to CCs, which has received significant attention for over two decades now, has been the so-called "Trans-impedance op-amp", more popularly known as the "Current Feedback Op-Amp" (CFOA) [3–7]. CFOAs fabricated in bipolar technology exhibit an almost constant bandwidth irrespective of the closed loop gain in contrast to the VOAs. The slew rate attained is also very high, typically in excess of 2,000 V/μs as opposed to merely 0.5 V/μs in case of traditional μA741 type VOA. Although the theoretical basis of many of these current feedback designs had been known earlier, attention on these building blocks has been largely due to the recent developments in complementary bipolar technology. The translinear circuit principle, first introduced by Barrie Gilbert in 1975 [8], which exploits the logarithmic relationship between the base-emitter voltage and collector current in bipolar transistor to create a variety of novel analog circuits, has been used for the evolution of CFOAs and many other high performance analog circuits.

From the view point of internal architecture, a CFOA, such as the popular AD844, is essentially a translinear second generation current conveyor (CCII+) followed by a translinear voltage buffer (see Fig. 3.1 (a) for the block diagram of the internal circuit and (b) for a typical bipolar implementation). Thus, CFOA AD844 from Analog Devices is a 4-terminal building block characterized by the following terminal equations:

$$i_y = 0,\ v_x = v_y,\ i_z = i_x \quad \text{and} \quad v_w = v_z. \tag{3.1}$$

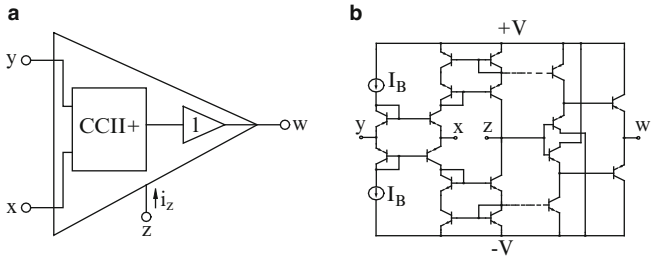


Fig. 3.1 Current feedback operational amplifier (**a**) the internal constituents, (**b**) bipolar implementation of AD844 type CFOA (adapted from [9])

3.4 CFOAs Overcome Several Limitations of VOAs

CFOA AD844 was introduced by Analog Devices around 1985, however, it caught the attention of circuit designers only after 1990 or so and subsequently, it was demonstrated [3–7] that it offers the following advantages in analog circuit design:

(1) Using CFOAs, various functional circuits can be realized with a minimum number of passive components without any component-matching (these advantages are particularly noticeable in case of realization of impedance converters/inverters, non-inverting/inverting differential integrators/differentiators, VCCS, instrumentation amplifiers, universal biquad filters and single resistor-controlled oscillators and many others). (2) CFOAs exhibit much higher slew rates (in excess of 2,000 V/μs) in contrast to VOAs (0.5 V/μs). (3) Gain and bandwidth can be set independently; amplifiers with variable gain but constant bandwidth become possible and (4) higher operational frequency range possible (as compared to conventional op-amps).

3.5 Why CFOA has a Higher Slew Rate?

In a typical internally-compensated op-amp architecture [6], the input stage is composed of a differential transconductance amplifier which exhibits a tanh-characteristic between the output current and the differential input voltage V_{id} since it is given by $I_{out} = I_B \tanh(V_{id}/2V_T)$ resulting in saturation of the current to a maximum value of I_B for larger values of V_{id}. Since the charging current to the compensating capacitor C_c is provided by the output current of the input transconductance stage, the slew rate which is decided by the maximum value of charging current is, therefore, limited to $\pm I_B$, the maximum slew rate is I_B/C_C. On the other hand, in case of a typical CFOA architecture, the input stage is a mixed translinear cell in which the characteristic between the differential input ($V_y - V_x$) turns out to be a Sinh-characteristic given by $I_{out} = 2I_B \sinh\{(V_y - V_x)/V_T\}$ thereby the output current goes on increasing indefinitely (theoretically up to infinity) when differential voltage input becomes large [6]. Since in the large differential input

case, the maximum charging current to the compensating capacitor is, in this case, theoretically infinite, this leads to a theoretically infinite slew rate. In practice, however, slew rates of the order of 2,000–4,000 V/μs are easily achievable.

Although CFOAs may not be very appropriate for applications which require low input offset voltage, good CMRR, low noise and high PSRR, nevertheless, they have been proved to be quite versatile for applications which require high slew rates, low distortion or the ability to set gain and bandwidth independently. Furthermore, there are numerous applications of CFOAs which can either not be performed with VOAs or which can be carried out more efficiently with CFOAs using lesser number of external passive components, with no component-matching required and with better tunability properties etc. The major focus of this chapter will, therefore, be on presenting only such applications of CFOAs, which exhibit one or more of the above-mentioned significant advantages.

3.6 Applications of the CFOAs

Numerous applications of CFOAs in the design of linear as well as nonlinear circuits have so far been evolved. Since well over one hundred publications have appeared on the applications and implementation of CFOAs during the past two decades, it is not feasible to even include references to all these works due to limitations of space. Due to this reason, we are constrained to include here only some representative application circuits and hardware implementations, which, in our opinion have some novelty and ingenuity in their architecture. Some key applications to illustrate the versatility of CFOAs now follow:

3.6.1 Design of Amplifiers With Variable-gain but Constant-bandwidth

A conventional op-amp-based instrumentation amplifier requires as many as three op-amps along with seven resistors and suffer from the drawback of gain-bandwidth conflict. By contrast, with CFOAs, only two CFOAs and a bare minimum of only two resistors are enough (see Fig. 3.2).

The instrumentation amplifier of Fig. 3.2 can be considered to be a CFOA-version of Wilson's CCII-based circuit [10].

Considering the finite input resistance looking into terminal X of the CFOA as r_x and taking parasitic output impedance looking into terminal Z as a resistance R_P in parallel with capacitance C_P, the maximum gain and 3-dB bandwidth of this circuit are found to be:

$$\frac{V_0}{(V_1 - V_2)} = \left(\frac{R_2}{R_1 + 2r_x}\right) \text{ and } BW = \frac{1}{C_p}\left(\frac{1}{R_2} + \frac{1}{R_p}\right) \tag{3.2}$$

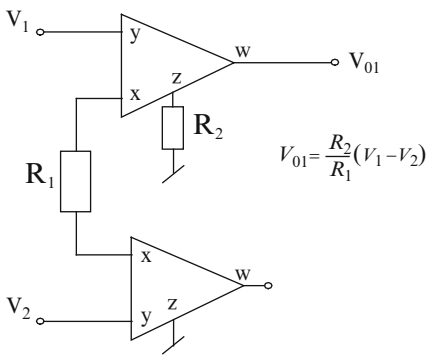


Fig. 3.2 An instrumentation amplifier using CFOAs (CFOA-version of Wilson's CCII-based circuit)

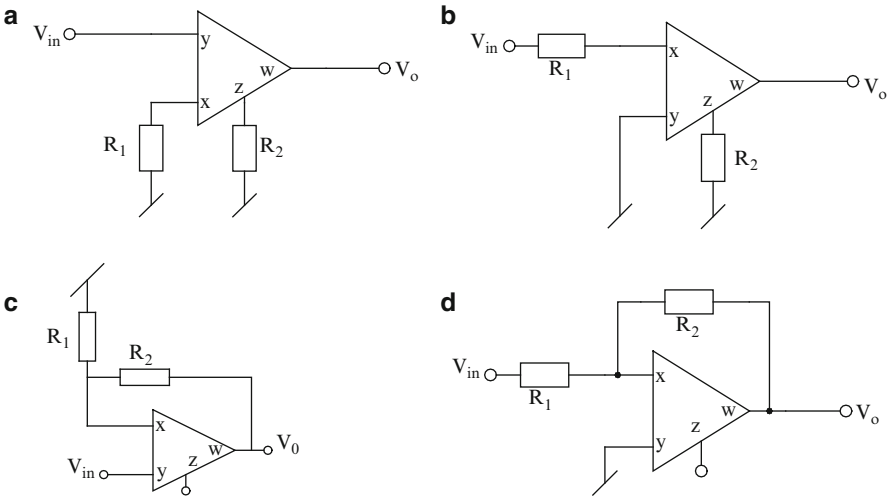


Fig. 3.3 Realization of non-inverting and inverting amplifiers using a CFOA

from where it is seen that the bandwidth of the amplifier can be fixed at a constant value by fixing R_2 while the gain can be made variable by changing R_1.

In Fig. 3.3, we show two different ways of realizing non-inverting amplifiers and inverting amplifiers using a single CFOA. For all the circuits, the expressions for maximum gain and 3-dB bandwidth are given by $|\text{Gain}| \cong (1+R_2/R_1)/(1+R_2/R_p)$ and $\text{BW} \cong (1+R_2/R_p)/C_pR_2$ for $R_1, R_2 \gg r_x$, from where it is seen that in all cases, the bandwidth can be fixed by R_2 whereas gain can be made variable through R_1.

Note that it is not possible to make either an instrumentation amplifier or inverting/noninverting amplifier using VOAs with the decoupling of gain and bandwidth, which is achievable by the CFOA circuits presented above.

3.6.2 Single Resistance Controlled Oscillators (SRCO)

Interest in realizing sinusoidal oscillators using CFOAs grew when it was demonstrated by Martinez, Celma and Sabadell [11] that using a CFOA, rather than a VOA, in the classical Wien bridge oscillator configuration results in an oscillator which offers important advantages such as: (1) more accurate adjustment of oscillation frequency, (2) much wider frequency span of frequency of operation, (3) higher frequency and larger amplitudes because of much higher slew rates than VOAs and (4) lower sensitivity of the frequency to the bandwidth variation of the active element thereby resulting in higher frequency stability. This stimulated considerable interest among the researchers to extend the realization of oscillators to the more popular and important class of single resistance controlled oscillators (SRCO) with the hope that such oscillators when realized with CFOAs will, therefore, offer significant advantages over their VOA-based counterparts as well as with the hope that the 4-terminal CFOA-based new SRCOs may possess additional interesting features not available in 3-terminal VOA-based SRCOs known earlier. Consequently, there has been a widespread interest on CFOA-based SRCOs and a large number of structures using one, two or three CFOAs are now known, however, here we present only three examples which prove the above mentioned contentions to be true.

Consider first a single CFOA-based SRCO proposed by Senani and Singh (from [12]; Fig. 3.7 therein) which is reproduced here in Fig. 3.4a. For the oscillator of Fig. 3.4a, the condition of oscillation (CO) and frequency of oscillation (FO) are given by

$$\frac{R_3}{R_4} = \frac{C_0}{C_1} + \frac{R_3}{R_0};\ \omega_0 = \sqrt{\left(\frac{1}{R_2} + \frac{1}{R_0}\right)\left(\frac{1}{R_3 C_0 C_1}\right)} \tag{3.3}$$

Thus, this circuit has the feature of providing independent control of FO by the resistor R_2 and independent control of CO by R_4 while using only a bare minimum of three resistors and two capacitors. This is significant, as any SRCO using a single VOA is not known to be realizable with only three resistors and two capacitors.

Second example is that of realizing SRCOs employing grounded capacitors as preferred for integrated circuit implementation. Many such SRCOs have been discovered including a number of systematic methods for realizing them for instance; see [16–18]. Here we present a specific circuit proposed by Gupta and Senani [14] which is shown here in Fig. 3.4b and for the oscillator of Fig. 3.4b, CO and FO are given by

$$R_1 = R_3 \ for\ C_1 = C_2\ (adjustable\ by\ R_1);\ \omega_0 = \sqrt{\frac{1}{C_1 C_2 R_2 R_3}}\ (adjustable\ by\ R_2) \tag{3.4}$$

To the best knowledge of the authors, this is the first two CFOA-GC SRCO, which provides explicit voltage mode output as well as explicit current mode output. It may be pointed out that no such SRCO with only VOAs is feasible.

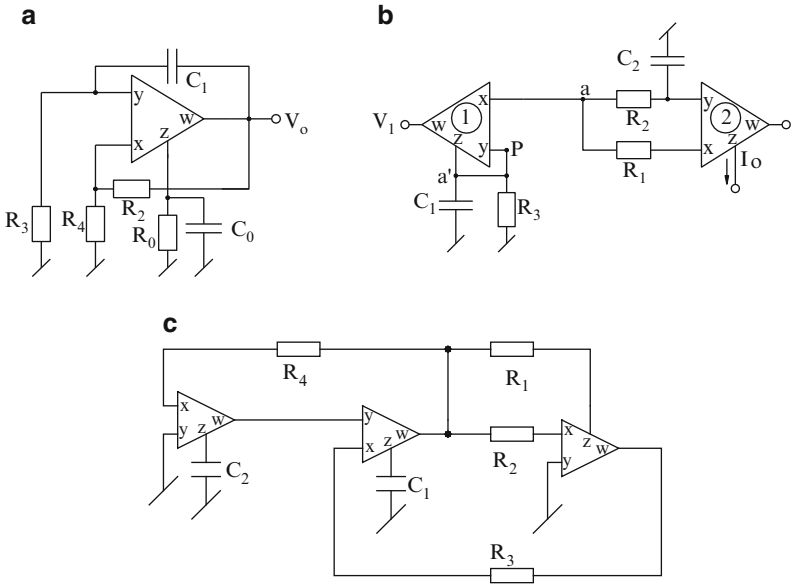


Fig. 3.4 SRCOs employing CFOAs (**a**) A single-CFOA-SRCO proposed by Senani and Singh (adapted from [12] © 1996 IET). (**b**) A dual-mode SRCO using both grounded capacitors proposed by Gupta and Senani (adapted from [14] © 1998 IET). (**c**) A fully uncoupled oscillator-cum-multifunction filter proposed by Bhaskar (adapted from [15] © 2003 Schiele and Schön)

As the last example, we present a three-CFOA oscillator which, apart from employing two grounded capacitors, provides fully uncoupled controls for CO and FO. (Note that CO and FO may be called fully uncoupled only when they are decided by two completely different sets of components, i.e. none of the components involved in CO are also involved in FO and vice versa.)

In the oscillator of Fig. 3.4c, CO and FO are given b $R_1 = R_2$; (adjustable by either or both of R_1, R_2)

$$\omega_0 = \sqrt{\frac{1}{C_1 C_2 R_3 R_4}} \text{ (adjustable by either or both of } R_3, R_4) \tag{3.5}$$

It is worth mentioning that no such fully-uncoupled-oscillator is known to be realizable using VOAs in the earlier literature. Furthermore, with feedback link broken at point "P", and considering the input to resistor R_2, the three filter responses namely V_{01}, V_{02} and V_{03} are BPF, LPF and BRF respectively (for details the reader is referred to [15]).

Thus, these three examples confirm the contention that using CFOAs such SRCO structures are possible the type of which cannot be realized by VOAs.

3.6.3 Floating Impedance Simulation Using CFOAs

It is well known that using VOAs it is impossible to simulate a floating inductance (FI) (lossless or lossy) without requiring any component matching conditions. Furthermore, for lossless FI simulation one normally requires two to four VOAs. By contrast, the first author of this chapter had demonstrated in 1979 onwards that using current conveyors it does become possible to simulate lossy floating inductance [19, 20] and as well as lossless [21] impedances respectively using no more than two current conveyors without requiring any component matching conditions.

Since a CFOA contains a CCII+ followed by a voltage follower it looks intuitively possible to be able to accomplish the same properties and features using CFOAs also. In this section, a few representative configurations which can realize lossless FIs and FDNRs as well as generalized positive/negative impedance convertors/invertors (GPIC/GPII) employing CFOAs along with a minimum possible number of passive components without requiring any component matching condition whatsoever are presented.

Fig. 3.5 shows two circuits [7] of which that of Fig. 3.5a can be regarded as a floating GPII/GPIC configuration whereas the circuits of Fig. 3.5b is generalized configuration for realizing positive/negative floating impedances. Both the circuits are characterized by the following equation:

$$i_1 = -i_2 = \frac{Z_3}{Z_1 Z_2}(v_1 - v_2) \tag{3.6}$$

From (3.6), it is obvious that a floating inductance or floating frequency-dependent-negative resistance (FDNR; an element having $Z(s) = 1/Ds^2$) by appropriate (resistive/capacitive) choice of impedance Z_1, Z_2 and Z_3 without requiring any component-matching and using least possible number of passive components.

In Fig. 3.6 we show a floating linear voltage-controlled-impedance (VCZ) configuration [22] which can simultaneously realize VCR, VCL and VC-FDNC (frequency-dependent-negative-conductance; an element having impedance of type $Z(s) = Ms^2$) elements from the same configuration.

From a straightforward analysis of the circuit of Fig. 3.6, the equivalent floating impedance realized by the circuit between terminals 1 and 2 is given by

$$Z_{1-2} = (R_1 R_3 / Z_2 Z_4) r_{DS}, \text{ where } r_{DS} = \frac{V_p^2}{2I_{DSS}(V_c - 2V_p)} \tag{3.7}$$

Linear floating positive, VCR, VCL and VC-FDNC elements can be realized from the circuit by the following choice (resistive/capacitive) of impedances Z_2 and Z_4: (1) VCR: $Z_2 = R_2$ and $Z_4 = R_4$; (2) VCL: either $Z_2 = 1/sC_2$ or $Z_4 = 1/sC_4$; (3) VC-FDNC: $Z_2 = 1/sC_2$ and $Z_4 = 1/sC_4$.

It is interesting to mention that the various negative-valued elements corresponding to the equivalent impedance given in (3.7) can be obtained by the simple artifice

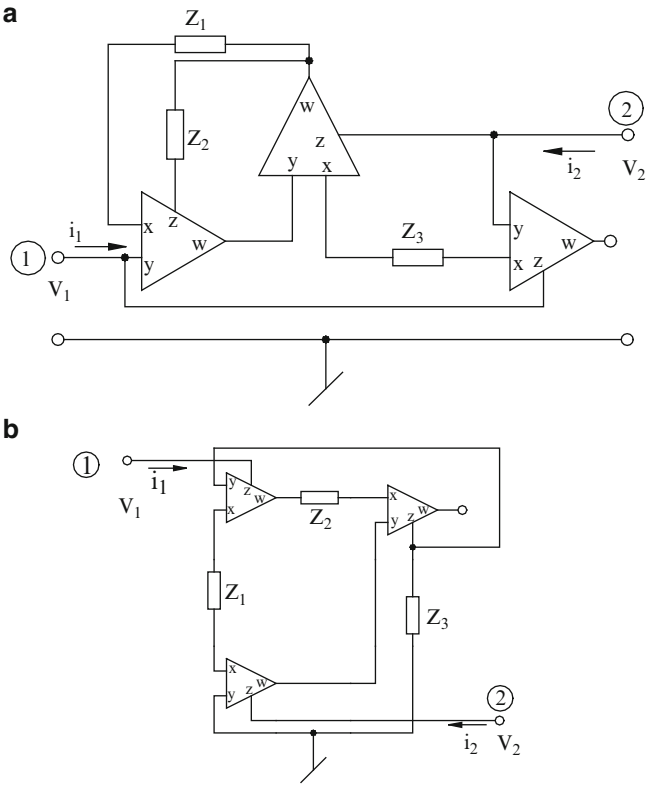


Fig. 3.5 Generalized floating impedance converters/inverters using CFOAs proposed by Senani (adapted from [7] © 1998 Schiele and Schön)

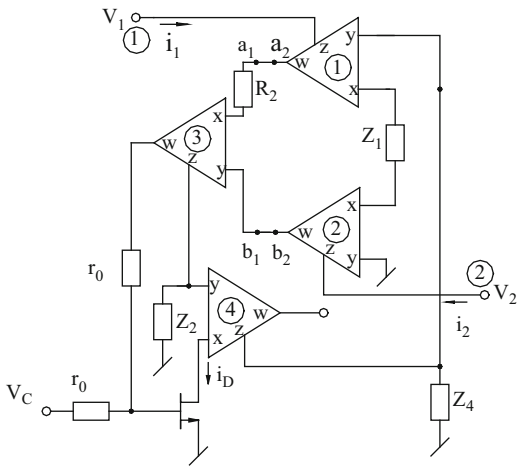


Fig. 3.6 Floating linear VCZ configuration proposed by Senani, Bhaskar, Gupta and Singh (adapted from [22] © 2009 John Wiley & Sons)

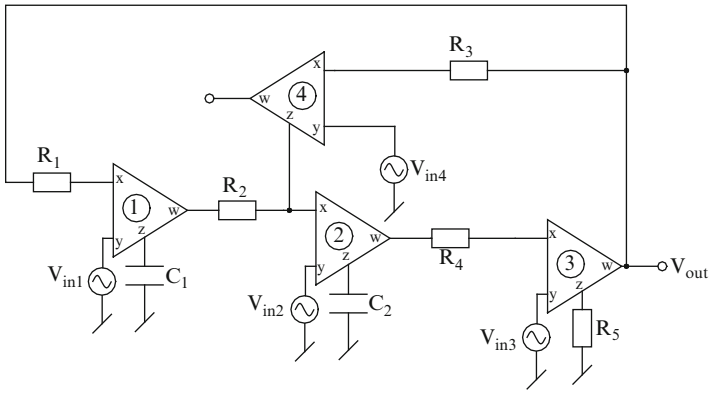


Fig. 3.7 A multiple-input single output type universal biquad proposed by Nikoloudis and Psychalinos (adapted from [13] © 2010 Springer)

of connecting $a_1 - b_2$ and $a_2 - b_1$ in the circuit of Fig. 3.6, thereby leading to floating negative impedance given by

$$Z_{1-2} = -(R_1 R_3 / Z_2 Z_4) r_{DS} \tag{3.8}$$

Furthermore, the grounded forms of all the above-mentioned floating impedances can be obtained by grounding either port-1 or port-2. However, in the circuit of Fig. 3.6, with port-2 grounded, CFOA2 becomes redundant (y-terminal of CFOA3 and R_1 can be connected to ground directly) and as a consequence, the circuit can be simplified to have only three CFOAs while still being capable of realizing a grounded impedance:

$$Z_{in} = \pm(R_1 R_3 / Z_2 Z_4) r_{DS} \tag{3.9}$$

3.6.4 Universal Biquad Filter Realizations

Although a large number of CFOA-based universal biquads have been presented in literature, to demonstrate the versatility of CFOAs in these applications, we present here two examples.

We first present a multiple-input single output (MISO) type universal biquad proposed by Nikoloudis and Psychalinos [13], using CFOAs, which is shown in Fig. 3.7.

The expression for the output voltage in terms of input voltages is given by

$$v_{out} = \frac{s^2 \frac{R_5}{R_4} v_{in3} - s \frac{R_5}{R_4} \left(\frac{1}{R_2 C_2} v_{in2} - \frac{1}{R_3 C_2} v_{in4} \right) + \frac{R_5}{R_1 R_2 R_4 C_1 C_2} v_{in1}}{s^2 + \frac{R_5}{R_3 R_4 C_2} s + \frac{R_5}{R_1 R_2 R_4 C_1 C_2}} \tag{3.10}$$

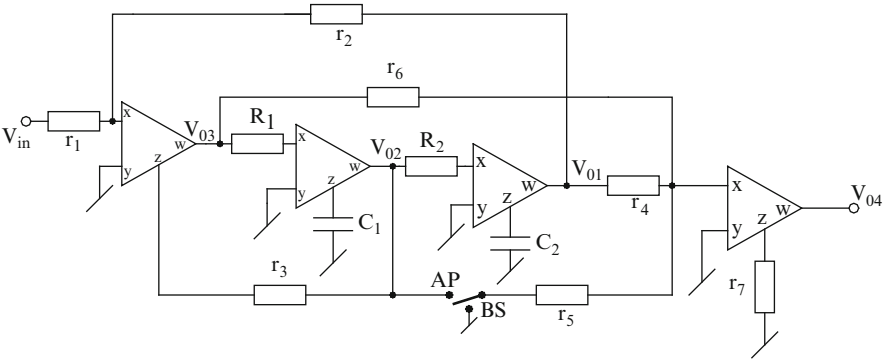


Fig. 3.8 A mixed-mode universal biquad proposed by Singh, Singh, Bhaskar and Senani (adapted from [23] © 2005 IEICE)

The various realizations of the five filter functions are obtained as follows:

Low pass filter: $v_{in2} = v_{in3} = v_{in4} = 0$ and $v_{in1} = v_{in}$, high pass filter: $v_{in1} = v_{in2} = v_{in4} = 0$ and $v_{in3} = v_{in}$, band pass filter: $v_{in1} = v_{in2} = v_{in3} = 0$ and $v_{in4} = v_{in}$ (non-inverting) or: $v_{in1} = v_{in3} = v_{in4} = 0$ and $v_{in2} = v_{in}$ (inverting), band stop filter: $v_{in1} = v_{in3} = v_{in}$, $v_{in2} = v_{in4} = 0$, all pass filter $v_{in1} = v_{in2} = v_{in3} = v_{in}$ and $v_{in4} = 0$. In addition, $R_2 = R_3$ and $R_4 = R_5$.

To the best knowledge of authors, no such op-amp RC structure is known which employs both grounded capacitor provides ideally infinite input impedance coupled with employing only four resistors and providing such versatility as exhibited by the circuit of Fig. 3.7.

As another example we now present a mixed-mode universal biquad proposed by Singh, Singh, Bhaskar and Senani [23] which is shown in Fig. 3.8.

A novel feature of this circuit is that universal biquad filters, in all the four possible modes, are realizable from this configuration. It may be noted that no such circuit using traditional VOAs is known to exist.

(a) Voltage-mode universal biquad filter: The various voltage-mode transfer functions realized by this circuit are given by

$$V_{01}/V_{in} = -\left(\frac{r_2}{r_1}\right)\left(\frac{r_3}{r_2R_1C_1R_2C_2}\right)/D(s),\ V_{02}/V_{in} = \left(\frac{r_3}{r_1}\right)\frac{s}{R_1C_1}/D(s) \tag{3.11}$$

$$V_{03}/V_{in} = -\left(\frac{r_3}{r_1}\right)s^2/D(s),\ V_{04}/V_{in} = \left(\frac{r_3}{r_1}\right)\left(s^2 + \frac{r_3}{r_2R_1C_1R_2C_2}\right)/D(s) \tag{3.12}$$

With the switch at BS position and choosing $r_2 = r_3$; $r_4 = r_6 = r_7$; one obtains:

$$V_{04}/V_{in} = \left(\frac{r_3}{r_1}\right)\left(s^2 - \frac{s}{R_1C_1} + \frac{r_3}{r_2R_1C_1R_2C_2}\right)/D(s) \tag{3.13}$$

where

$$D(s) = s^2 + \frac{s}{R_1C_1} + \frac{r_3}{r_2R_1C_1R_2C_2} \tag{3.14}$$

Thus, the circuit realizes a LP response at V_{01}, BP response at V_{02}, a HP response at V_{03}, and notch and all pass responses at V_{04} under appropriate conditions.

It is interesting to note that in all the five filters, all the three parameters of interest can be tuned through separate resistors as follows. After adjusting the bandwidth by R_1, desired ω_0 can be adjusted by R_2 and finally, the gain H_0 of the filters (in all the five responses) is tunable by r_1.

We now show how the same circuit, with simple modifications, can also realize universal biquad filters in the remaining three modes.

(b) Current-mode universal biquad filters: With r_1 and r_7 deleted, the circuit can be converted into a universal current-mode biquad with ideally zero input impedance and ideally infinite output impedance. With an input current I_{in} injected into input terminal "m" and output current I_{out} taken out from the node "n", the circuit can realize all the five filter functions in current mode. The general transfer function for this single-input-single-output universal current-mode filter is given by

$$\frac{I_{out}}{I_{in}} = \frac{r_3\left\{\frac{s^2}{r_6} - \left(\frac{1}{C_1R_1r_5}\right)s + \frac{1}{C_1C_2R_1R_2r_4}\right\}}{\left[s^2 + s\frac{1}{C_1R_1} + \frac{r_3}{C_1C_2R_1R_2r_2}\right]} \tag{3.15}$$

The circuit realizes a LPF with r_5 and r_6 open circuited; a band pass with r_6 and r_4 open circuited; a high pass with r_5 and r_4 open circuited; a notch with r_5 open circuited (along with $r_2 = r_4 = r_6 = r_0$ (say) thereby yielding $H_0 = r_3/r_0$) and finally, an all pass with $r_2 = r_3 = r_4 = r_5 = r_6$ yielding $H_0 = 1$. The gains for LP, BP and HP responses are r_3/r_4, r_3/r_5 and r_3/r_6 respectively.

In the CM biquads, LP and HP filters have only H_0 controllable (though r_4 and r_6 respectively); in notch and AP, H_0 is not tunable, however, BW and ω_0 can be independently adjusted (through R_1 and R_2) respectively and finally, in BP realization, BW, ω_0 and H_0, all are independently tunable (through R_1, R_2 and r_5 respectively).

(c) Trans-admittance universal biquad filters: In this case, we retain the input resistor r_1 but take the output I_{out} from z-terminal of the fourth CFOA. The various functions realized and their features are similar to those of case (b).

(d) Trans-impedance universal biquad filters: In this case, with r_1 deleted the input will be a current I_{in}, however, the output voltages will be V_{01}, V_{02}, V_{03} and V_{04}. The realisability conditions parameters of filters and their features are similar to those of case (a). Thus, the proposed circuit is a universal mixed-mode biquad.

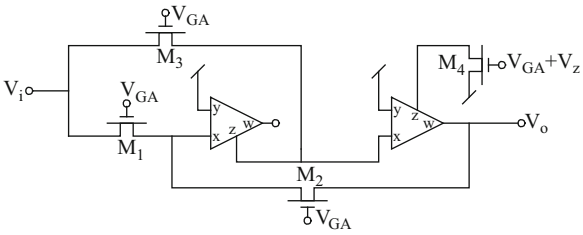


Fig. 3.9 An analog divider using CFOAs proposed by Liu and Chen (adapted from [24] © 1995 IET)

Lastly, it must be mentioned that no such mixed-mode universal biquad configuration is possible or known with traditional VOAs.

3.6.5 Analog Divider Using CFOAs and MOSFETs

Among various non-linear applications of CFOAs evolved so far, an interesting application is that of realizing an analog divider using MOSFETs operating in triode region. One such circuit is shown in Fig. 3.9 [24]. Assuming the input signals V_x and V_y to be small permitting all MOSFETs to be operating in triode region and having same transconductance parameter $K = \mu_S C_{ox}(W/L)$ where symbols have their usual meaning, a straight forward analysis of Fig. 3.9 gives the output voltage as

$$v_0 = (V_{GA} - V_{GB})\left(\frac{v_y}{v_x}\right) \tag{3.16}$$

From where it is seen that the circuit functions as an analog divider with input signals as v_x and v_y where the scale factor (V_{GA}-V_{GB}) is controllable through external voltages V_{GA} and V_{GB}.

3.6.6 MOSFET-C Biquad Using CFOAs

It is well known that MOSFET-C filters using VOAs suffer from effect of the finite gain bandwidth product of the op-amps. Due to the various advantages offered by CFOAs, MOSFET-C filters using CFOAs have been investigated by several authors. Thus, using MOSFET-C lossless/lossy integrators and MOSFET-C lossless/lossy summing integrators, a variety of MOSFET-C biquad filters are realizable. Here, we present a typical biquad filter proposed by Mahmoud and Soliman [25] shown in Fig. 3.10 which employs a MOSFET-CFOA lossless integrator comprised of the middle pair of CFOAs the two capacitors therein along with the MOSFET connected

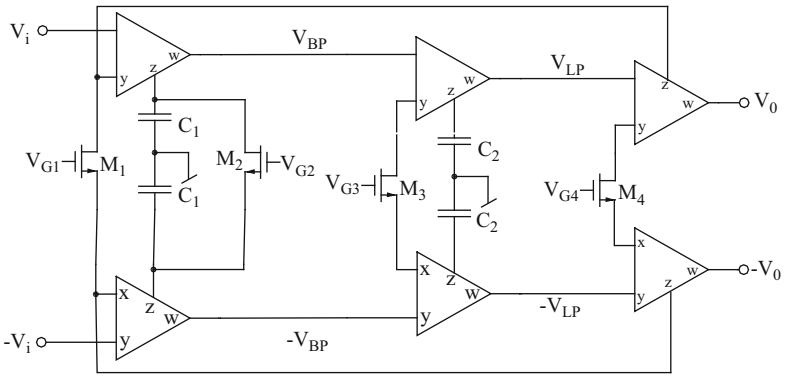


Fig. 3.10 An exemplary MOSFET-C LP/BP filter proposed by Mahmoud and Soliman (adapted from [25] © 1998 Taylor & Francis)

between X terminals of the two CFOAs, MOSFET-CFOA lossy integrator comprised of the first pair of CFOAs along with the two capacitors and two MOSFETs therein, and a voltage to current converter formed by the last pair of CFOAs along with MOSFET M_4 (acting as linear resistor). This biquad circuit realizes a low-pass response at V_{LP} and a band pass response at V_{BP}.

Assuming MOSFETs to be operating in triode region where i^{th} MOSFET has the transconductance parameter $k_i = \mu_s C_{ox}(W_i/L_i)$ where (W_i/L_i) is the aspect ratio of the i^{th} MOSFET, C_{ox} is the gate oxide capacitance/unit area, μ_s is the electron mobility and V_T is the threshold voltage (assumed same in case of identical devices), by a straight forward analysis of the circuit the two transfer functions realizable by this circuit are given by

$$\frac{V_{BP}}{V_i} = \frac{\frac{s}{R_1C_1}}{D(s)} \; and \; \frac{V_{LP}}{V_i} = \frac{\frac{1}{R_3R_4C_1C_2}}{D(s)} \tag{3.17}$$

where

$$D(s) = s^2 + \frac{1}{R_2C_1} + \frac{1}{R_3R_4C_1C_2} = s^2 + \frac{\omega_o}{Q_0}s + \omega_o^2 \tag{3.18}$$

$$\omega_0 = \frac{1}{(R_3R_4C_1C_2)^{1/2}}, \quad Q_0 = R_2\left(\frac{C_1}{R_3R_4C_2}\right)^{1/2} \tag{3.19}$$

and

$$R_i = 1/K_i(V_{Gi} - V_T) \text{ for } (i = 1,2,3,4) \tag{3.20}$$

From the above it is seen that for the realized filters, the parameter ω_0 can be controlled by V_{G3} and/or V_{G4} whereas Q_0 in case of LP and bandwidth ω_0/Q_0 in case of BP can be controlled by external voltage V_{G2}.

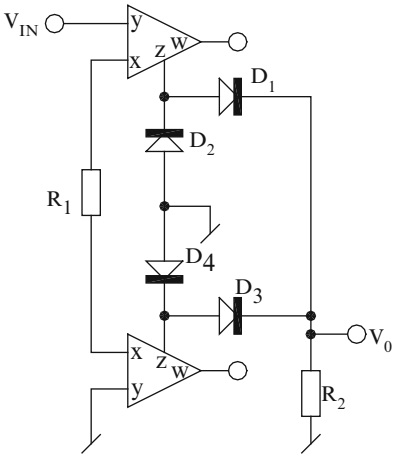


Fig. 3.11 An exemplary full wave rectifier proposed by Khan, Abou and Al-Turiagh using CFOAs (adapted from [26] © 1995 Taylor & Francis)

3.6.7 Design of Precision Rectifier Using CFOAs

There have been several attempts of making precision current mode full wave rectifiers using current conveyors quite often realized with AD844 type CFOA. Here we present a typical design of a simple full wave precision rectifier circuit proposed in [26] (Fig. 3.11) which avoids the use of closely matched resistors and provides a wide dynamic input voltage range. The circuit provides a high performance over a wide frequency range of operation. An inspection of the circuit reveals that the current flowing into the X terminal of AD844 at the bottom and the one flowing out of Z terminal of AD844 at the top are given by: $i_z = i_x = V_{in}/(R_1 + 2r_x)$.

The diode combinations D_1–D_2 and D_3–D_4 are connected in such a manner that the output current of the CFOA will flow either into the load resistance R_2 or will be bypassed to the ground depending upon the polarity of the input voltage V_{in}. In other words, when V_{in} is positive, i_x, i_{ZA} and i_{ZB} have the directions such that diodes D_1–D_2 allow i_Z to be flowing into load resistance R_2 whereas at the same time, diodes D_3–D_4 allow i_{ZB} to the ground. Similarly, when V_{in} is negative, i_x, i_{ZA} and i_{ZB} reverse their directions and as consequence, now i_{ZB} is taken to the load while i_{ZA} flows to the ground. It therefore follows that current through the load R_2 will be uni-directional thereby resulting in an output voltage given by

$$V_0 = i_{ZA}R_2 = i_{ZB}R_2 = (R_2/(R_1 + 2r_x))V_{in} \tag{3.21}$$

It is interesting to note that by reversing the connections of all the four diodes, one can obtain a full wave rectified signal with sign inversion (i.e. $-V_0$). Lastly, it must be mentioned that as compared to VOA-based precision rectifiers, which generally require four or more matched resistors, the circuit using CFOA described here uses a bare minimum of (only two) resistors.

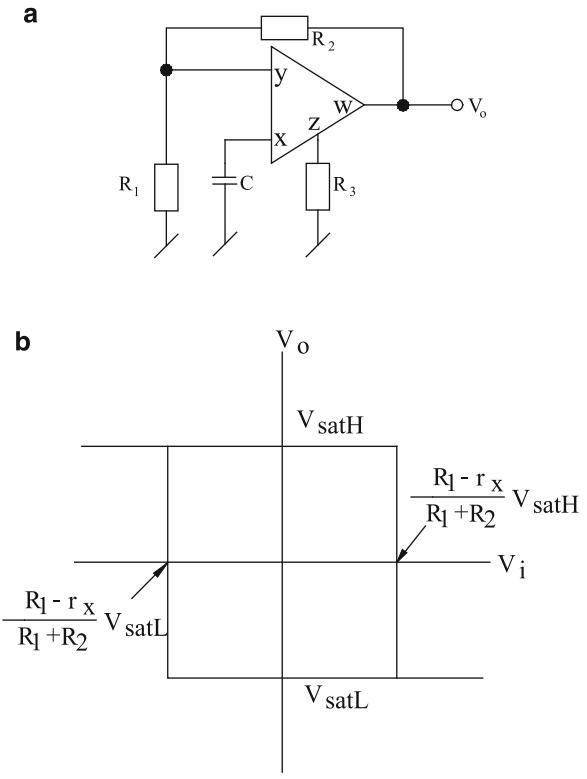


Fig. 3.12 Relaxation oscillator proposed by Abuelma'atti and Al-Shahrani (adapted from [27] © 1998 Taylor & Francis). (**a**) Triangular/square wave generator. (**b**) Transfer characteristic of the Schmitt Trigger composed of CFOA, R_2 and R_1

3.6.8 Realization of Relaxation Oscillator/Waveform Generator

A triangular/square wave generator can be made from a single CFOA as shown in Fig. 3.12 [27]. In this circuit, the CFOA behaves as a Schmitt trigger with the input–output characteristic shown in Fig. 3.12b where the threshold voltages are given by

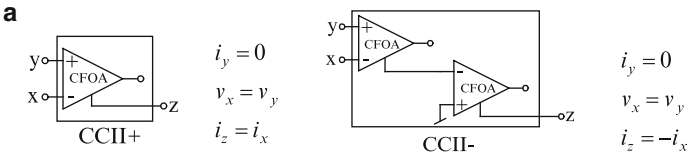
$$V_{TH} = \frac{R_1 - r_x}{R_1 - R_2} V_{satH} \text{ and } V_{TL} = \frac{R_1 - r_x}{R_1 - R_2} V_{satL} \tag{3.22}$$

where V_{satH} and V_{satL} are two stable states decided by the DC biasing power supply voltages of the CFOA and R_x is the input resistance of the CFOA looking into terminal X of the CFOA. The circuit can be analyzed by starting from any one of the two stable states of the output voltage V_0 (for details the reader is referred to [27]). The circuit generates a square wave signal at V_0 and a triangular wave signal at V_x the frequency of which is given by

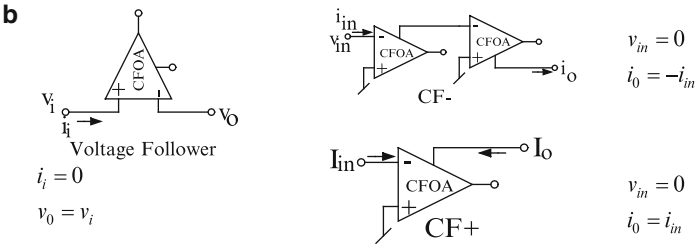
$$f = 1/\left(2CR_3\left(\frac{R_1 - r_x}{R_1 + R_2}\right)\right), \text{ or } f \cong \frac{1}{2CR_3}\left(1 + \frac{R_2}{R_1}\right) \text{ for } R_1 >> R_x. \tag{3.23}$$

3.7 Applications of CFOAs in Realizing Other Building Blocks

It is worthwhile to point out that, apart from being employed as four terminal building blocks in their own right, CFOAs have also been employed to realize other building blocks in the analog circuits literature, for instance see [28–31]. Some important realizations have been summarized here in Fig. 3.13a–h, where input marked as "+" represents y-input and the one marked as "−" represents x-input of the CFOA.

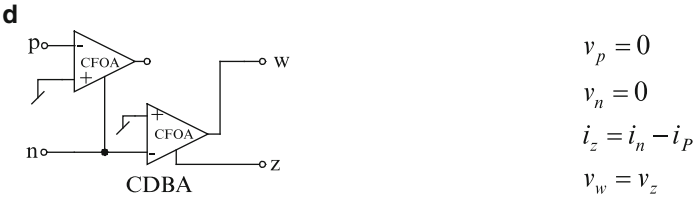


CCII+ and CCII -



Voltage and Current Follower

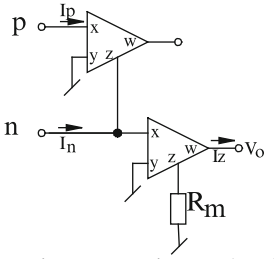
A Four Terminal Floating Nullor



Current Differencing Buffer Amplifier (CDBA) (adapted from [28] © 1999 Elsevier)

Fig. 3.13 Realization of various building blocks using CFOAs

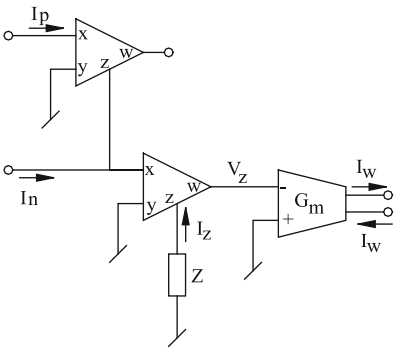
e



$$v_p = 0$$
$$v_n = 0$$
$$v_0 = R_m\left(i_p - i_n\right)$$

Operation Transresistance Amplifier (OTRA) (adapted from [29] © 1992 IET)

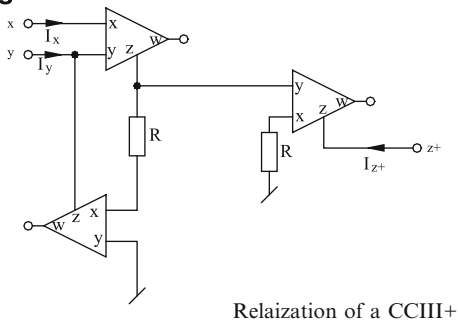
f



$$v_p = 0$$
$$v_n = 0$$
$$i_z = \left(i_p - i_n\right)$$
$$i_w = G_m v_z$$

Current Differencing Transconductance Amplifier (CDTA) [30]

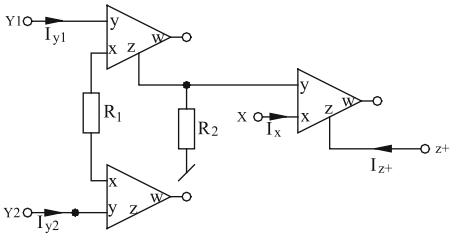
g



$$i_y = -i_x$$
$$v_x = v_y$$
$$i_z = i_x$$

Relaization of a CCIII+[31]

h



$$i_{y1} = 0$$
$$i_{y2} = 0$$
$$v_x = \left(v_{y1} - v_{y2}\right) \text{ for } R_1 = R_2$$
$$i_z = i_x$$

Relaization of a DVCC+[31]

Fig. 3.13 (continued)

3.8 Recent Developments in Bipolar and CMOS Implementation of CFOAs

Although there have been hundreds of publications on improving the design of current conveyors, surprisingly, in spite of the wide spread applications of CFOAs as exemplified here and in the references cited therein, there have been comparatively a very much smaller number of efforts [32–36] on improving the design of bipolar or CMOS CFOAs. In [32] Tammam, Hayatleh and Lidgey have presented a new CFOA architecture with significantly improved CMRR and gain accuracy. In [33] Hayatleh, Tammam, Hart and Lidgey have introduced a new CFOA architecture using forward and reverse bootstrapping (reproduced here in Fig. 3.14). This circuit is shown to offer increase of CMRR by about 46 dB with a reduction of input-referred-offset-voltage by a factor of two. References [34–36] have dealt with the design of improved CFOAs for CMOS technology. Out of these [35] deals with fully differential CFOA design reproduced here in Fig. 3.15. A typical CMOS CFOA architecture from [36] provides improved performance in terms of low output resistance, high current drive and high slew rate capability as compared to a number of earlier designs. The continued efforts on improving the design of bipolar and CMOS CFOAs include a systematic synthesis of CFOAs advanced by Torres-Papaqui and Tlelo-Cuautle through manipulation of voltage followers and current followers [37]. It is hoped that continued work in this direction may result in better CFOAs in both bipolar and CMOS technologies in near future to facilitate the realization of numerous applications of CFOAs more efficiently and fruitfully.

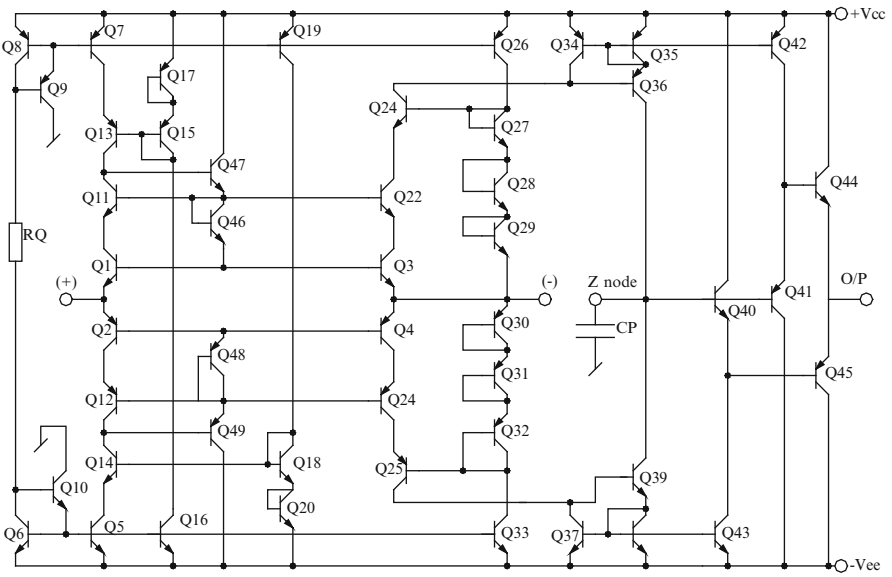


Fig. 3.14 CFOA using forward and reverse bootstrapping proposed by Hayatleh-Tammam, Hart and Lidge (adapted from [33] © 2007 Taylor & Francis)

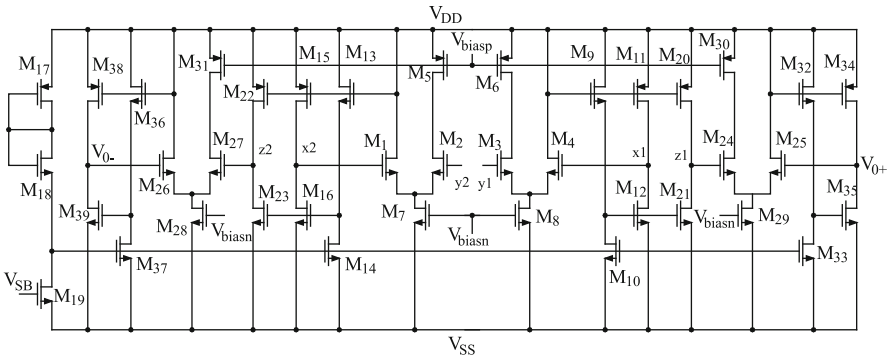


Fig. 3.15 Schematic of the fully differential current feedback operational amplifier proposed by Soliman and Awad (adapted from [35] © Springer 2005)

3.9 Different Types of Modified CFOAs Proposed in Literature

Due to popular appeal of CFOAs, a number of researchers have proposed, from time to time, a number of modified versions of CFOA such as specific current feedback operational amplifier (SCFOA) [38], differential voltage CFOA (DVCFOA) [39], differential difference complimentary CFOA (DDCCFA) [40] and modified CFOA (MCFOA) [41].

The SCFOA proposed by Erkan Yuce [38] is a seven port active building block which is unduly complex and except realizing a universal voltage mode/current mode filter using only a single SCFOA, along with three resistors and two capacitors as demonstrated by Yuce, does not appear to have attracted enough attention in the literature.

On the other hand, the MCFOA proposed by Yuce and Minaei [41] is nothing but a composite connection of two complementary second generation current conveyors (CCII+ and CCII−) which was already proposed long back by Smith and Sedra [42] which they chose to call a "Composite current conveyor" which is a four port having exactly the same characterizing equations, as given for MCFOA. In fact, the AD844 based construction of Fig. 19 of [41] as well as the CMOS structure of Fig. 2 of [41] both are nothing but a composite connection of a CCII+ and CCII− thus, confirming its equivalence with the "composite current conveyor" of [42].

Another modification, called the differential voltage current feedback amplifier (DVCFA) was proposed by Gunes and Toker in 2002 [39] which is characterized by: $i_{yk} = 0$; $k = 1 - 2$, $v_x = v_{y1} - v_{y2}$, $i_z = i_x$ and $v_w = v_z$.

DVCFAs have been shown to be particularly useful building blocks for synthesizing SRCOs employing grounded capacitors (GCs) [39]. In this context it may be noticed that while it has been amply demonstrated by a number of researchers that single resistance controlled oscillators (SRCO) can be realized using only a single CFOA however, none of the circuits known so far is able to employ both GCs as

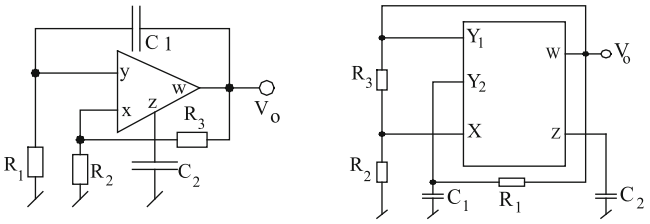


Fig. 3.16 Conversion of CFOA-based SRCO into DVCFA-based GC-SRCO as proposed by Gunnes and Toker (adapted from [39] © 2002 Elsevier)

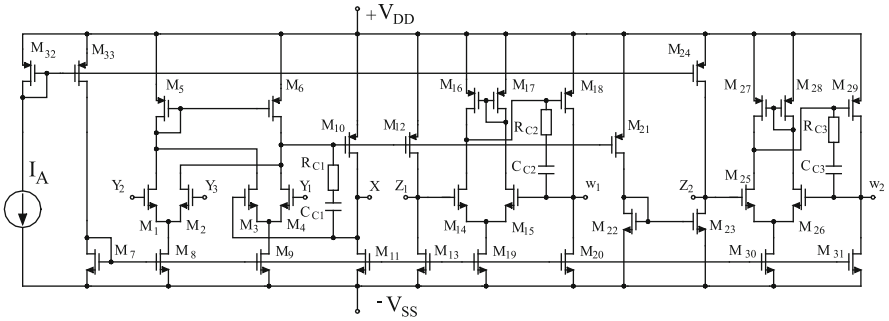


Fig. 3.17 CMOS implementation of the DDCCFA (adapted from [40] © 2005 IET)

desirable for integrated circuit implementation. A DVCFA is particularly useful in removing this difficulty and it makes GC-SRCOs realizable from a single DVCFA. A family of eight such GC-oscillators has been derived by Gunes and Toker in [39] and an exemplary realization there from is shown here in Fig. 3.16.

Both the circuits are characterized by exactly the same CO and FO which are given by

$$C_1R_1 = C_2R_2 \text{ (adjustable by } R_2\text{)};$$
$$\omega_0 = \sqrt{\frac{1}{C_1C_2R_1R_3}} \text{ (adjustable by } R_3\text{)}; \tag{3.24}$$

Differential difference complementary current-feedback-operational-amplifier (DDCCFA): This extension of the CFOA is an active eight-port building block defined by the following characterizing equations: $i_{yk} = 0$; $k = 1 - 3$, $v_x = v_{y1} - v_{y2} + v_{y3}$, $i_{z1} = i_x$, $i_{z2} = -i_x$, $v_{w1} = v_{z1}$ and $v_{w2=}v_{z2}$ and was formally introduced by Gupta and Senani in 2005 [40] (see Fig. 3.17).

It was shown in [40] that a single DDCCFA is sufficient to generate SRCO circuits possessing the following properties simultaneously: (a) use of a single active building block, (b) employment of two GCs along with a minimum number

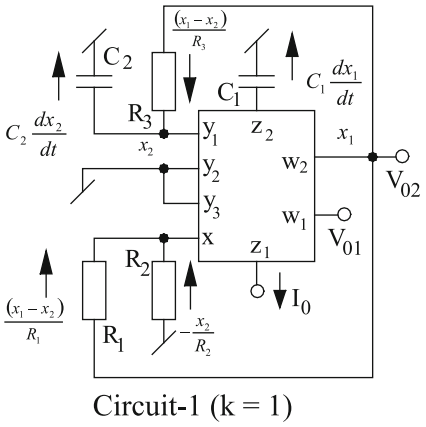


Fig. 3.18 An exemplary SRCO using a DDCCFA proposed by Gupta and Senani (adapted from [40] © 2005 IET)

(only three) of resistors, (c) non-interacting controls of CO and FO, (d) a simple condition of oscillation (i.e. not more than one condition) and (e) availability of current-mode and voltage-mode outputs both explicitly. An exemplary SRCO using a DDCCFA proposed by Gupta and Senani is shown in Fig. 3.18.

It has also been demonstrated in [40] that employing a single DDCCFAs, a large number of previously known building blocks can be derived as special cases while employing two DDCCFAs, still more number of other known building blocks can be realized. Thus, the present authors believe that DDCCFA can be considered to be one of the most universal building blocks known till date.

3.10 Further Research on CFOAs and Their Applications

The following appear to be worthwhile ideas to be taken up for further research and investigations on CFOAs and their applications:

(1) As of now, AD844 appears to be the only commercially available bipolar CFOA with an externally accessible Z-terminal. Although there are a variety of other CFOAs available from several manufacturers but they invariably do not provide an externally accessible Z-pin. In view of the versatility and flexibility provided by a 4-terminal CFOA, with an externally-accessible Z-terminal and their widespread and popular applications evolved so far, improved 4-terminal IC CFOAs having performance superior to AD844 are warranted and are expected to be widely welcome by the analog designers' community. (2) Search for better CFOA-based configurations for various analog signal processing/signal generation applications such as MOSFET-C universal biquads capable of realizing all five standard filters and analog multiplier as counterpart to the analog divider of Fig. 3.9 appear to be two interesting problems. Thus, it is seen that there is enough scope for further research in these areas. (3) Work on the evolution of CMOS

CFOAs, including their fully differential versions, is currently being carried out, for facilitating the implementation of CFOA-based circuits in CMOS analog VLSI. On another note, in view of their versatility evolution of fully integrated DVCFOA or DDCCFAs may be a welcome step. A preliminary design of the "DDCCFA" was proposed by Gupta and Senani, however, the problem of evolving fully Integratable, high performance DDCCFAs, as well as their newer applications, are open to investigation. Lastly, the evolution of topologies of CMOS CFOA suitable for Nanotechnological implementations is yet another worthwhile task which has not been attempted so far.

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Chapter 4
Generation of Grounded Capacitors Minimum Component Oscillators

Ahmed M. Soliman

4.1 Introduction

It is not possible to realize a sinusoidal oscillator using a single operational amplifier (Op Amp) and the minimum number of passive circuit elements namely two resistors and two capacitors. Several minimum passive circuit element oscillators are available in the literature [1–9] using a single voltage controlled voltage source (VCVS), a single voltage controlled current source (VCCS), a single current conveyor (CCII+) [10] and a single inverting current conveyor (ICCII−) [11].

The objective of this chapter is to apply nodal admittance matrix (NAM) expansion to generate three node, four node and five node oscillator circuits using members of the CCII and ICCII families.

Recently, a symbolic framework for systematic synthesis of linear active circuits based on NAM expansion was presented in [12]. The matrix expansion process begins by introducing blank rows and columns, representing new internal nodes, in the admittance matrix. Then, nullators and norators are used to move the resulting admittance matrix elements to their final locations, properly describing either floating or grounded passive elements. Thus, the final NAM is obtained including finite elements representing passive circuit components and unbounded elements, so called infinity-variables, representing nullators and norators. In this framework, nullators and norators ideally describe active elements in the circuit are used. The nullator and norator are pathological or singular elements that possess ideal characteristics and are specified according to the constraints they impose on their terminal voltages and currents. For the nullator shown in Fig. 4.1a $V = I = 0$, while the norator shown in Fig. 4.1b imposes no constraints on its voltage and current. The attractive feature of the two-nullor elements is their ability to model active

A.M. Soliman (✉)
Electronics and Communication Engineering Department, Faculty of Engineering,
Cairo University, Giza, 12613, Egypt
e-mail: asoliman@ieee.org

E. Tlelo-Cuautle (ed.), *Integrated Circuits for Analog Signal Processing*,
DOI 10.1007/978-1-4614-1383-7_4,

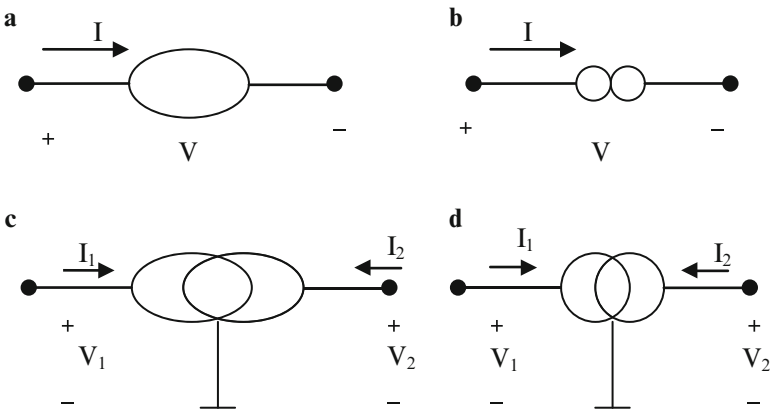

Fig. 4.1 (**a**) Nullator. (**b**) Norator. (**c**) Voltage mirror. (**d**) Current mirror

circuits [13]. Despite the ability of nullor elements to describe many active building blocks, they fail to represent devices like the CCII+. Other passive elements like resistors are combined with nullators and norators in order to obtain the nullor representation of the CCII+ [6]. In order to avoid the use of passive elements in the nullor representation of any building block, additional pathological elements called mirror elements describing the voltage and current reversing actions are introduced in [11]. The voltage mirror (VM) shown in Fig. 4.1c, is a lossless two-port network element used to represent an ideal voltage reversing action and it is described by:

$$V_1 = -V_2 \tag{4.1a}$$

$$I_1 = I_2 = 0 \tag{4.1b}$$

The current mirror (CM) shown in Fig. 4.1d, is a two-port network element used to represent an ideal current reversing action and it is described by:

$$V_1 \text{ and } V_2 \text{ are arbitrary} \tag{4.1c}$$

$$I_1 = I_2, \text{ and they are also arbitrary} \tag{4.1d}$$

Very recently the systematic synthesis method based on NAM expansion using nullor elements [12] has been extended to accommodate mirror elements. This results in a generalized framework encompassing all pathological elements for ideal description of active elements [14]. Accordingly, more alternative realizations are possible and a wide range of active devices can be used in the synthesis procedure.

In this chapter, the conventional systematic synthesis framework using NAM expansion presented in [15] to synthesize oscillator circuits is applied to the

minimum passive component oscillators. The oscillators are classified according to the number of nodes in the circuit and the nature of the two resistors whether being grounded or floating as shown in Fig. 4.2. Several new as well as well-known oscillator circuits are generated in this chapter; using CCII or ICCII or combination of both.

4.2 Formulation of the NAM Equation

The oscillators considered in this chapter are grounded capacitors second order oscillators using two resistors and two capacitors. The state matrix equation is described as follows:

$$\begin{bmatrix} sV_1 \\ sV_2 \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{4.2}$$

The condition of oscillation and the radian frequency of oscillation are given by:

$$a_{11}+a_{22} = 0, \omega o = \sqrt{a_{11}a_{22} - a_{12}a_{21}} \tag{4.3}$$

From the above equation it is seen that a_{11} and a_{22} must have opposite polarities, also a_{12} and a_{21} must have opposite polarities. If both a_{11} and a_{22} are zero there will be no control on the condition of oscillation.

The oscillator circuits considered in this chapter are canonic grounded capacitor oscillators represented by one of the four general configurations shown in Fig. 4.2.

Four different classes of oscillators are considered in this chapter. The class I oscillators has one grounded resistor and one floating resistor and each of the two resistors shares a node with one of the capacitors and it is a three node oscillator circuit as shown in Fig. 4.2a. On the other hand in the class II oscillators the grounded resistor does not share a node with one of the capacitors and it is a four-node oscillator circuit as shown in Fig. 4.2b. In the class III oscillators both resistors are grounded and do not share nodes with the two-grounded capacitors and it is a four-node oscillator circuit as shown in Fig. 4.2c. This class of oscillators has no condition of oscillation and will be discussed briefly in this chapter. The class IV oscillators has two floating resistors and one of them shares a node with one of the capacitors and it is a five node oscillator circuit as shown in Fig. 4.2d.

The class V oscillator has one grounded resistor and one floating resistor and both resistors do not share nodes with the two-grounded capacitors. It is also a five-node oscillator circuit with no control on condition of oscillation as in the class III and will not be discussed in this chapter.

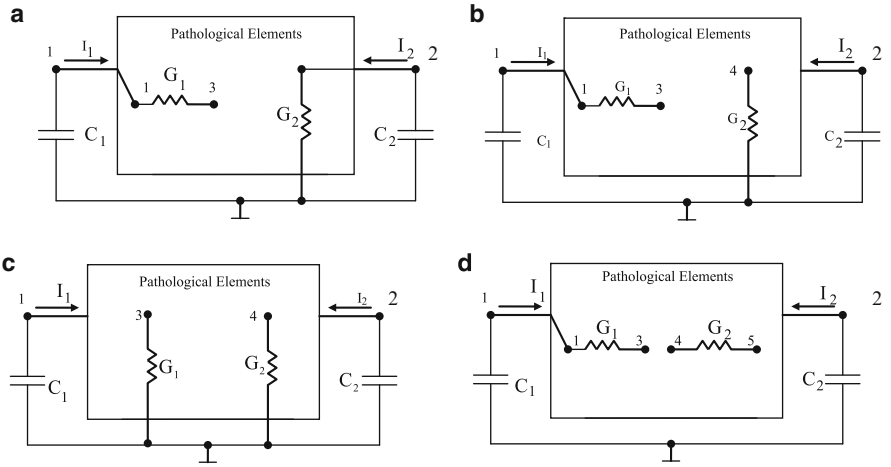

Fig. 4.2 (**a**) Class I three node generalized configuration. (**b**) Class II four-node configuration. (**c**) Class III four-node configuration. (**d**) Class IV five nodes generalized configuration

4.3 Class I Oscillators

The generalized class I oscillator configuration shown in Fig. 4.2a has two types and can be described by the state equations as given in Table 4.1. The admittance matrix Y of the two-port oscillator circuit taking the capacitors C_1 and C_2 as external elements at ports 1 and 2 is formulated from the state matrix by interchanging the signs of the admittance parameters.

4.3.1 Class I-Type A

The NAM in this case is given by:

$$Y = \begin{bmatrix} G_1 & -G_1 \\ G_1 & -G_1 + G_2 \end{bmatrix} \tag{4.4}$$

Adding a third blank row and column to the above equation and connecting a nullator between columns 2 and 3 to move $-G_1$ from 1, 2 position to the 1, 3 position and also to move $-G_1$ from 2, 2 position to the 2, 3 position, the following NAM is obtained:

Table 4.1 Summary of the state matrix equation of the four classes of oscillators

Class	State matrix equation	Oscillation condition	Number of nodes
I- A I- B	$\begin{bmatrix} sC1V1 \\ sC2V2 \end{bmatrix} = \begin{bmatrix} -G_1 & \pm G_1 \\ \mp G_1 & G_1 - G_2 \end{bmatrix} \begin{bmatrix} V1 \\ V2 \end{bmatrix}$	$\frac{C2}{C1} + \frac{G_2}{G_1} = 1$	3
II- A II- B	$\begin{bmatrix} sC1V1 \\ sC2V2 \end{bmatrix} = \begin{bmatrix} -G_1 & \pm G_1 \\ \mp G_1 \mp G_2 & G_1 \end{bmatrix} \begin{bmatrix} V1 \\ V2 \end{bmatrix}$	C2= C1	4
II- C II- D	$\begin{bmatrix} sC1V1 \\ sC2V2 \end{bmatrix} = \begin{bmatrix} -G_1 & \mp G_1 \mp G_2 \\ \pm G_1 & G_1 \end{bmatrix} \begin{bmatrix} V1 \\ V2 \end{bmatrix}$	C2= C1	4
III- A III-B	$\begin{bmatrix} sC1V1 \\ sC2V2 \end{bmatrix} = \begin{bmatrix} 0 & \mp G_1 \\ \pm G_2 & 0 \end{bmatrix} \begin{bmatrix} V1 \\ V2 \end{bmatrix}$	No condition	4
III- C III-D	$\begin{bmatrix} sC1V1 \\ sC2V2 \end{bmatrix} = \begin{bmatrix} 0 & \pm G_2 \\ \mp G_1 & 0 \end{bmatrix} \begin{bmatrix} V1 \\ V2 \end{bmatrix}$	No condition	4
IV- A IV-B	$\begin{bmatrix} sC1V1 \\ sC2V2 \end{bmatrix} = \begin{bmatrix} -G_1+G_2 & \mp G_2 \\ \pm G_1 & 0 \end{bmatrix} \begin{bmatrix} V1 \\ V2 \end{bmatrix}$	$G_2 = G_1$	5
IV- C IV-D	$\begin{bmatrix} sC1V1 \\ sC2V2 \end{bmatrix} = \begin{bmatrix} -G_1+G_2 & \pm G_1 \\ \mp G_2 & 0 \end{bmatrix} \begin{bmatrix} V1 \\ V2 \end{bmatrix}$	$G_2 = G_1$	5

$$Y = \begin{bmatrix} G_1 & \overbrace{0 & -G_1} \\ G_1 & G_2 & -G_1 \\ 0 & 0 & 0 \end{bmatrix} \tag{4.5}$$

Connecting a CM between rows 2 and 3 to move G_1 from 2, 1 position to become $-G_1$ at the 3, 1 position and also to move $-G_1$ from 2, 3 to become G_1 at the position to the position 3, 3, the following NAM is obtained:

$$Y = \left.\begin{bmatrix} G_1 & \overbrace{0 & -G_1} \\ 0 & G_2 & 0 \\ -G_1 & 0 & G_1 \end{bmatrix}\right\} \tag{4.6}$$

The pathological realization for the above equation after adding the two capacitors at nodes 1 and 2 is shown in Fig. 4.3a. The nullator and CM are realizable by a CCII+, which results in the well-known oscillator circuit reported in [1,4,6].

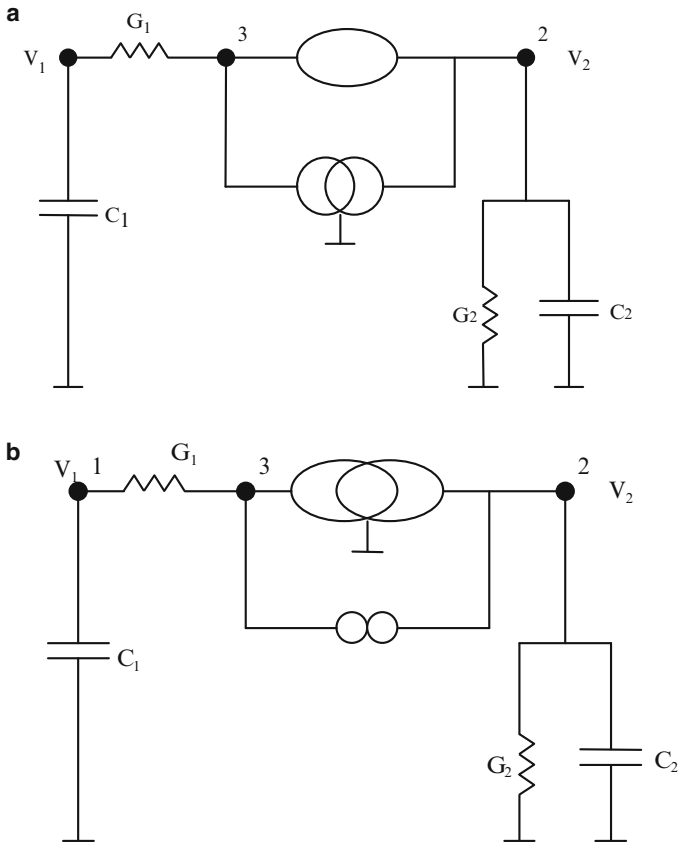

Fig. 4.3 (**a**) Pathological realization of class I-type A oscillator. (**b**) Pathological realization of class I-type B oscillator

4.3.2 Class I-Type B

The NAM in this case is given by:

$$Y = \begin{bmatrix} G_1 & G_1 \\ -G_1 & -G_1 + G_2 \end{bmatrix} \tag{4.7}$$

Adding a third blank row and column to the above equation and connecting a VM between columns 2 and 3 and a norator between rows 2 and 3 the following NAM is obtained:

$$Y = \left[\begin{array}{ccc} G_1 & \overbrace{0} & \overbrace{-G_1} \\ 0 & G_2 & 0 \\ -G_1 & 0 & G_1 \end{array}\right] \Bigg) \tag{4.8}$$

The pathological realization for the above equation after adding the two capacitors at nodes 1 and 2 is shown in Fig. 4.3b. The VM and norator are realizable by an ICCII−, which results in the well known oscillator circuit reported in [1, 2].

For each of the two circuits of the class I oscillators the condition of oscillation and the radian frequency of oscillation are given by:

$$\frac{C2}{C1} + \frac{G_2}{G_1} = 1, \ \omega o = \sqrt{\frac{G_1 G_2}{C1C2}} \tag{4.9}$$

Of course it is not possible to use equal G or equal C with this class of oscillators.

4.4 Class II Oscillators

The class II oscillator configuration is shown in Fig. 4.2b has four types and can be described by the state equations as given in Table 4.1. The condition of oscillation for this class is $C_1 = C_2$. This class of oscillators was generated in [1] from eight alternative grounded frequency dependent negative resistor (FDNR) circuits.

4.4.1 Class II-Type A

The NAM in this case is given by:

$$Y = \left[\begin{array}{cc} G_1 & -G_1 \\ G_1 + G_2 & -G_1 \end{array}\right] \tag{4.10}$$

Adding a third blank row and column to the above equation and connecting a nullator between columns 2 and 3 to move $-G_1$ from 1, 2 position to the 1, 3 position and also to move $-G_1$ from 2, 2 position to the 2, 3 position, the following NAM is obtained:

$$Y = \left[\begin{array}{ccc} G_1 & \overbrace{0} & \overbrace{-G_1} \\ G_1 + G_2 & 0 & -G_1 \\ 0 & 0 & 0 \end{array}\right] \tag{4.11}$$

Connecting a CM between rows 2 and 3 to move G_1 from 2, 1 position to become $-G_1$ at the 3, 1 position and also to move $-G_1$ from the position 2, 3 to become G_1 at the diagonal position 3, 3 thus the following NAM is obtained:

$$Y = \begin{bmatrix} G_1 & \overbrace{0 & -G_1} \\ G_2 & 0 & 0 \\ -G_1 & 0 & G_1 \end{bmatrix} \Big\} \tag{4.12}$$

Adding a fourth blank row and column to the above equation and then adding a nullator between columns 1, 4 and a norator between rows 2, 4 in order to move G_2 to the diagonal position 4, 4; the following NAM is obtained:

$$Y = \left(\begin{bmatrix} \overbrace{G_1 & \overbrace{0 & -G_1} & 0} \\ 0 & 0 & 0 & 0 \\ -G_1 & 0 & G_1 & 0 \\ 0 & 0 & 0 & G_2 \end{bmatrix} \Big\} \right) \tag{4.13}$$

The pathological realization for the above equation after adding the two capacitors at nodes 1 and 2 is shown in Fig. 4.4a. The corresponding CCII− and CCII+ oscillator circuit is shown in Fig. 4.4b [1, 16]. There is a second circuit that belongs to class II-type A having the same topology, which can be generated and it uses an ICCII+ and a CCII+ and was introduced in [1].

4.4.2 Class II-Type B

The NAM in this case is given by:

$$Y = \begin{bmatrix} G_1 & G_1 \\ -G_1 - G_2 & -G_1 \end{bmatrix} \tag{4.14}$$

Following similar steps as in the previous section two oscillator circuits having same circuit topology as the class II-type A can be generated. One of the two oscillators uses two ICCII− and the other uses a CCII+ and an ICCII−.

4.4.3 Class II-Type C

This is the adjoint to class II-type A [17], the NAM in this case is given by:

$$Y = \begin{bmatrix} G_1 & G_1 + G_2 \\ -G_1 & -G_1 \end{bmatrix} \tag{4.15}$$

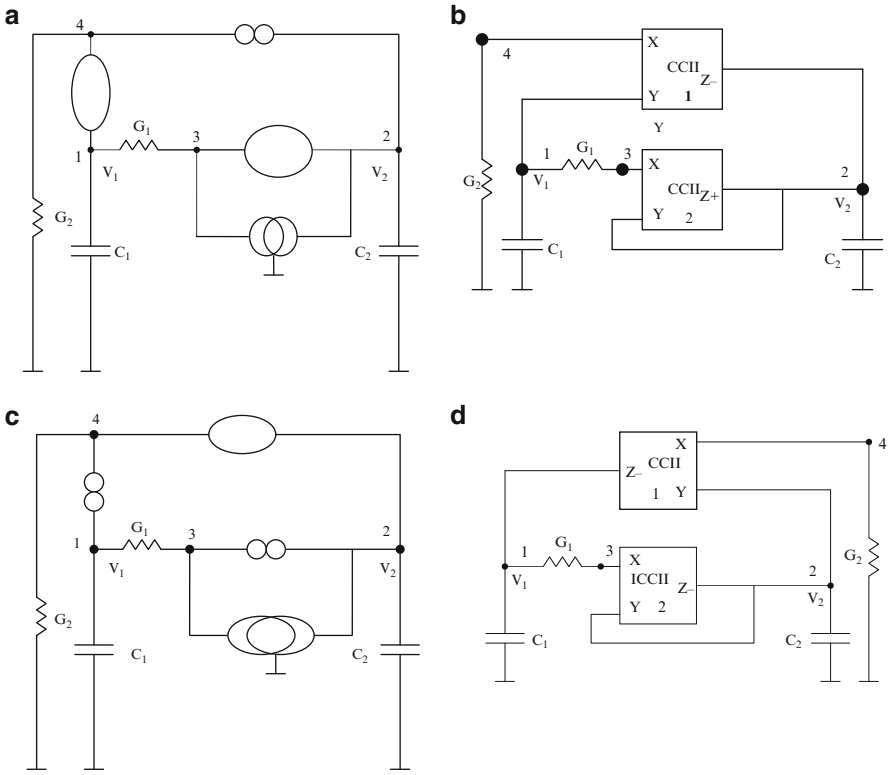

Fig. 4.4 (**a**) Pathological realization 1 of class II-type A oscillator. (**b**) CCII− and CCII+ oscillator circuit realizing Fig. 4.4a [1, 16]. (**c**) Pathological realization 1 of class II-type C oscillator. (**d**) CCII− and ICCII− oscillator circuit realizing Fig. 4.4c [1]

Following successive expansion steps the following NAM is obtained:

$$Y = \begin{bmatrix} G_1 & \overbrace{0 & -G_1}^{} & 0 \\ 0 & 0 & 0 & 0 \\ -G_1 & 0 & G_1 & 0 \\ 0 & 0 & 0 & G_2 \end{bmatrix} \Bigg) \Bigg) \tag{4.16}$$

The pathological realization for the above equation after adding the two capacitors at nodes 1 and 2 is shown in Fig. 4.4c. The corresponding CCII− and ICCII− oscillator circuit is shown in Fig. 4.4d [1]. There is a second circuit that belongs to class II-type C having the same topology that can be generated and it uses an ICCII+ and an ICCII− and was given in [1].

4.4.4 Class II-Type D

This is the adjoint to class-type B [17], the NAM in this case is given by:

$$Y = \begin{bmatrix} G_1 & -G_1 - G_2 \\ G_1 & -G_1 \end{bmatrix} \tag{4.17}$$

Following similar steps as in the previous section two oscillator circuits having same circuit topology as the class II-type C can be generated. One of the two oscillators uses two; CCII+ [1, 18] and the other use an ICCII− and a CCII+.

It should be noted that the class II oscillators were generated in [1] from eight-grounded frequency dependent negative resistance (FDNR) circuits by terminating input port by a grounded capacitor.

Two more circuits that belong to this class and have different topology can be generated from types type A and type C as follows.

Starting from (4.11) and adding a fourth blank row and column and connecting a nullator between columns 1, 4 to move G_2 to the position 2, 4 and a norator between rows 2 and 4 to move G_1 and $-G_1$ from row 2 to row 4, it follows that:

$$Y = \begin{bmatrix} G_1 & 0 & -G_1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ G_1 & 0 & -G_1 & G_2 \end{bmatrix} \tag{4.18}$$

Adding a CM between rows 4 and 3 to move G_1 and $-G_1$ from row 4 to row 3 to become $-G_1$ and G_1, it follows that:

$$Y = \begin{bmatrix} G_1 & 0 & -G_1 & 0 \\ 0 & 0 & 0 & 0 \\ -G_1 & 0 & G_1 & 0 \\ 0 & 0 & 0 & G_2 \end{bmatrix} \tag{4.19}$$

The oscillator circuit representing the above equation uses a CCII+ and a CCII− and is shown in Fig. 4.5a [1, 19]. This oscillator circuit can be obtained from the unity gain current mode band-pass filter given in [20] by feeding-back output current to the input port.

Similarly, expanding the NAM equation of the class II-type C can generate the circuit shown in Fig. 4.5b, this circuit was reported in [1, 21]. It should be noted that the stray resistance RX of conveyor 1 and the capacitance CZ of conveyor 2 affect the circuits of Fig. 4.5.

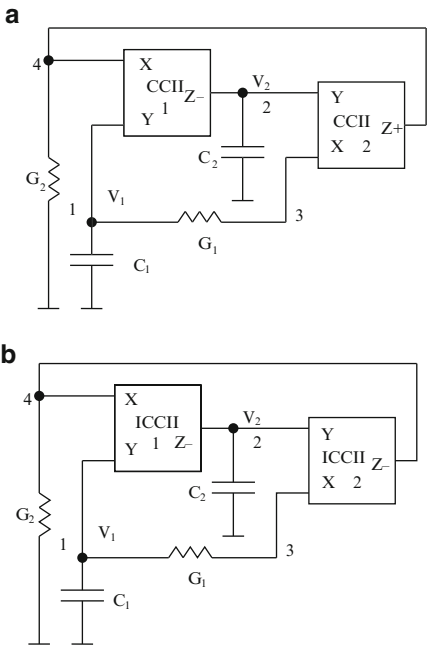

Fig. 4.5 (**a**) Alternative topology of a class II-type A oscillator [1, 19]. (**b**) Alternative topology of a class II-type B oscillator [1, 20]

4.5 Class III Oscillators

The class III oscillator configuration shown in Fig. 4.2c has four types and can be described by the state equations as given in Table 4.1. There is no condition of oscillation for this class. The eight oscillators belonging to this class can be obtained from the eight gyrators reported in [22] by terminating the two ports of the gyrators by the two capacitors.

4.5.1 Class III-Type A

The NAM in this case is given by:

$$Y = \begin{bmatrix} 0 & G_1 \\ -G_2 & 0 \end{bmatrix} \tag{4.20}$$

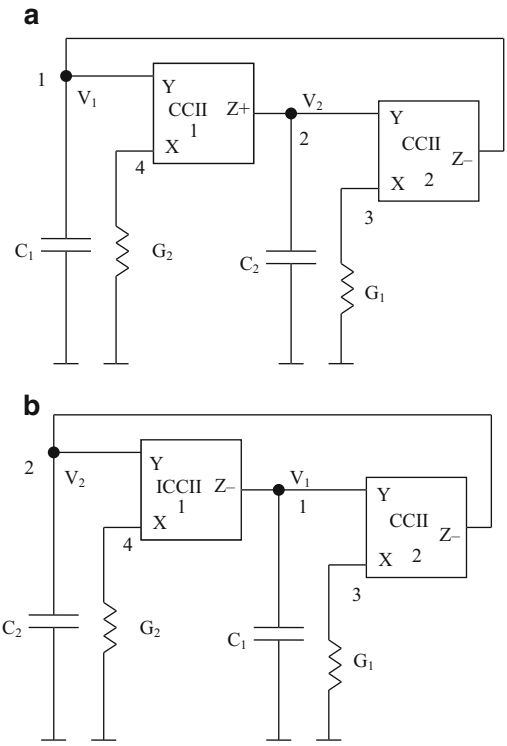

Fig. 4.6 (**a**) CCII+ and CCII− class III-type A oscillator circuit 1 [23]. (**b**) ICCII− and CCII− class III-type C oscillator adjoint to Fig. 4.6a

By successive expansions the following NAM is obtained:

$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & G_1 & 0 \\ 0 & 0 & 0 & G_2 \end{bmatrix} \tag{4.21}$$

The above equation results in the class III-type A realization 1 using a CCII+ and a CCII− as shown in Fig. 4.6a [23].

The class III-type-A oscillators include three more realizations and can be obtained in a similar way and are summarized as follows: realization 2; using a CCII+ and an ICCII+, realization 3; using an ICCII− and a CCII−, realization 4; using an ICCII− and an ICCII+.

4.5.2 Class III-Type B

The class III-type B oscillators include also four circuits and can be obtained in a similar way and are realizable using CCII−, CCII+ or ICCII+, CCII+ or CCII−, ICCII− or ICCII+, ICCII−.

4.5.3 Class III-Type C

This represents the adjoint oscillator circuits to class III-type A oscillator circuits. The four oscillator circuits realizing the type A realize also the type C oscillators after inter-changing ports 1 and 2. For example the oscillator circuit shown in Fig. 4.6b is the adjoint of that of Fig. 4.6a and is also obtainable from realization 3 of class III-type A after interchanging the two ports 1 and 2.

4.5.4 Class III-Type D

This represents the adjoint oscillator circuits to class III-type-B. The four oscillator circuits realizing the type-B realize also the type-D oscillators after inter-changing ports 1 and 2.

The oscillators of the class III can be designed with equal C and equal G.

4.6 Class IV Oscillators

The class IV oscillator configuration is shown in Fig. 4.2d has four types and can be described by the state equations as given in Table 4.1.

4.6.1 Class IV-Type A

The NAM in this case is given by:

$$Y = \begin{bmatrix} G_1 - G_2 & G_2 \\ -G_1 & 0 \end{bmatrix} \tag{4.22}$$

Adding a third blank row and column to the above equation and connecting a norator between columns 2 and 3 in order to move $-G_1$ from the 2, 1 position to the position 3, 1 the following NAM is obtained:

$$Y = \left.\begin{bmatrix} G_1 - G_2 & G_2 & 0 \\ 0 & 0 & 0 \\ -G_1 & 0 & 0 \end{bmatrix}\right) \tag{4.23}$$

Adding a fourth blank row and column to the above equation and then adding a nullator between columns 2, 4 in order to move G_2 to from the position 1, 2 to the position 1, 4 the following NAM is obtained:

$$Y = \left.\begin{bmatrix} G_1 - G_2 & \overbrace{0 \quad 0 \quad G_2} \\ 0 & 0 \quad 0 \quad 0 \\ -G_1 & 0 \quad 0 \quad 0 \\ 0 & 0 \quad 0 \quad 0 \end{bmatrix}\right) \tag{4.24}$$

Adding a norator between rows 1, 4 in order to move $-G2$ and G_2 to from the first row to the fourth row the following NAM is obtained:

$$Y = \left.\left.\begin{bmatrix} G_1 & \overbrace{0 \quad 0 \quad 0} \\ 0 & 0 \quad 0 \quad 0 \\ -G_1 & 0 \quad 0 \quad 0 \\ -G_2 & 0 \quad 0 \quad G_2 \end{bmatrix}\right)\right) \tag{4.25}$$

Adding a fifth blank row and column and connecting a nullator between columns 1 and 5 in order to move $-G_2$ from the position 4, 1 to the position 4, 5 therefore:

$$Y = \left.\left.\begin{bmatrix} \overbrace{G_1 & \overbrace{0 \quad 0 \quad 0} \quad 0} \\ 0 & 0 \quad 0 \quad 0 \quad 0 \\ -G_1 & 0 \quad 0 \quad 0 \quad 0 \\ 0 & 0 \quad 0 \quad G_2 \quad -G_2 \\ 0 & 0 \quad 0 \quad 0 \quad 0 \end{bmatrix}\right)\right) \tag{4.26}$$

The indefinite admittance matrix has the property that each row and each column sum to zero [24]. Connection of a norator between nodes 5 and zero will allow the row zero terms to be brought to row 5. Similarly, a connection of a nullator between nodes 3 and zero will allow the column zero to be brought to column 3 [24] as follows:

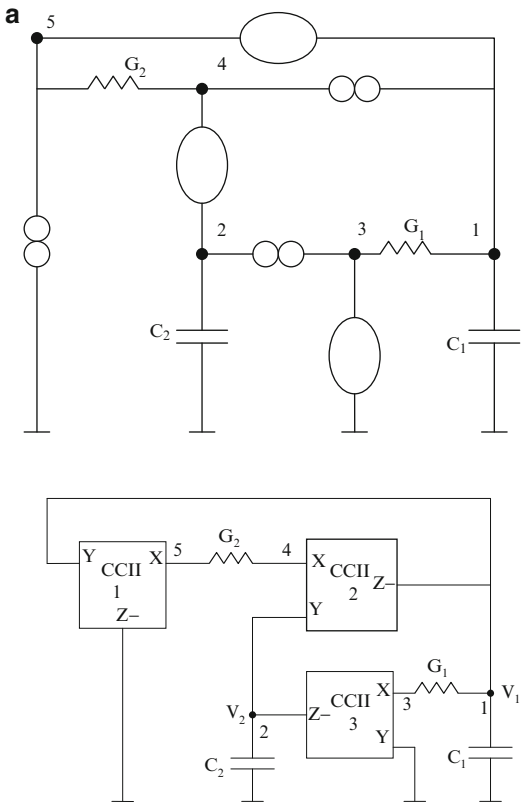

Fig. 4.7 (**a**) Pathological realization 1of class IV-type A oscillator. (**b**) Three CCII− realization 1of class IV-type A oscillator

$$Y = \begin{bmatrix} G_1 & 0 & -G_1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ -G_1 & 0 & G_1 & 0 & 0 \\ 0 & 0 & 0 & G_2 & -G_2 \\ 0 & 0 & 0 & -G_2 & G_2 \end{bmatrix} \tag{4.27}$$

The above equation results in the class IV-type A pathological realization 1 shown in Fig. 4.7a. The corresponding realization using three CCII− is shown in Fig. 4.7b. It should be noted that this new oscillator circuit can also be obtained from the unity gain band-pass filter introduced in [25] by connecting the band-pass output to the input port through a voltage follower to provide isolation to band-pass output port.

Following similar steps as in the previous section a second pathological realization is obtained and is shown in Fig. 4.8a and the corresponding current conveyor circuit realization is shown in Fig. 4.8b.

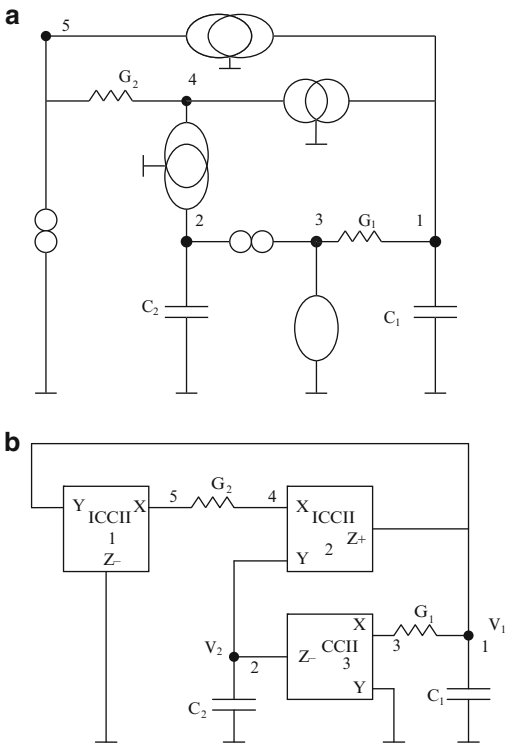

Fig. 4.8 (**a**) Pathological realization 2 of class IV-type A oscillator. (**b**) CCII and ICCII realization 2 of class IV-type A oscillator

4.6.2 Class IV-Type B

The NAM in this case is given by:

$$Y = \begin{bmatrix} G_1 - G_2 & -G_2 \\ G_1 & 0 \end{bmatrix} \tag{4.28}$$

Successive NAM expansion steps can expand the above Y matrix to the following form:

$$Y = \begin{bmatrix} G_1 & 0 & -G_1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ -G_1 & 0 & G_1 & 0 & 0 \\ 0 & 0 & 0 & G_2 & -G_2 \\ 0 & 0 & 0 & -G_2 & G_2 \end{bmatrix} \tag{4.29}$$

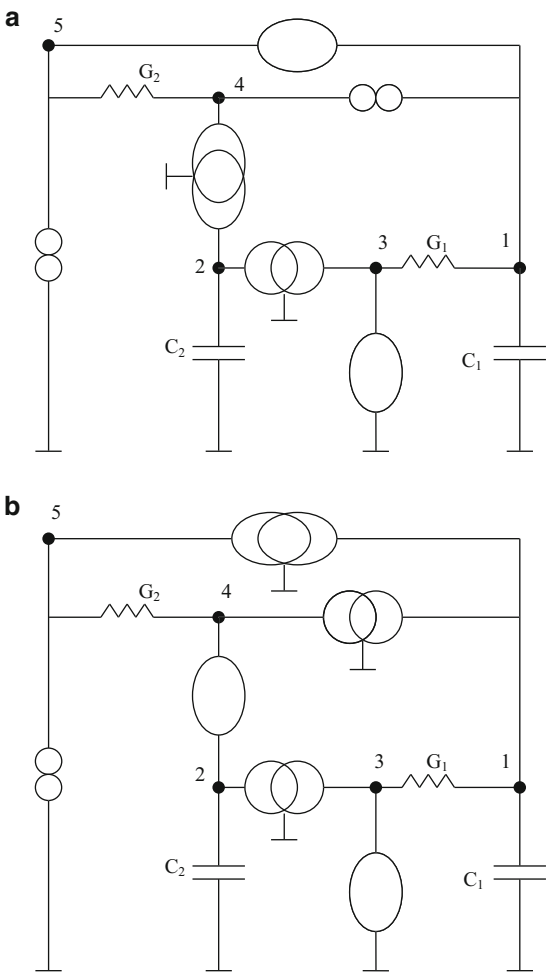

Fig. 4.9 (**a**) Pathological realization 1 of class IV-type B oscillator. (**b**) Pathological realization 2 of class IV-type B oscillator

The above equation results in the class IV-type B pathological realization 1 shown in Fig. 4.9a. The second pathological realization of the class IV- type B is shown in Fig. 4.9b.

The realizations of class IV-types C and D can be obtained following similar steps as before.

4.7 Alternative Topology Realizations of Class IV Oscillators

In this section a brief discussion on a second topology realization of class IV- types A and B is given.

4.7.1 Class IV-Topology II-Type A

Apply NAM expansion to (4.22) the following Y matrix is obtained:

$$Y = \begin{bmatrix} G_1 & 0 & -G_1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ -G_1 & 0 & G_1 & 0 & 0 \\ 0 & 0 & 0 & G_2 & -G_2 \\ 0 & 0 & 0 & -G_2 & G_2 \end{bmatrix} \tag{4.30}$$

The above equation results in the pathological realization 1 shown in Fig. 4.10a. The corresponding realization using a CCII+ and two CCII− is shown in Fig. 4.10b. A second pathological realization can be derived and results in the pathological realization shown in Fig. 4.11.

Similarly for the class IV-type B a second topology can be derived and results in the pathological realization 1 shown in Fig. 4.12a. The corresponding realization using two; CCII+ and one ICCII− is shown in Fig. 4.12b. A second pathological realization can be derived and results in the pathological realization shown in Fig. 4.12c.

4.8 Conclusions

Systematic generation method for realizing grounded capacitor oscillator circuits using NAM expansion was given. The oscillators considered in this chapter uses the minimum number of passive elements namely two capacitors and two resistors. All generated oscillator circuits except those of Fig. 4.5 have the advantage of their ability to absorb parasitic resistance and parasitic capacitance elements effects. Four classes of oscillators are generated in this chapter, the class I oscillator circuits include three nodes, the classes II and III oscillator circuits include four nodes and the class IV oscillator circuits include five nodes.

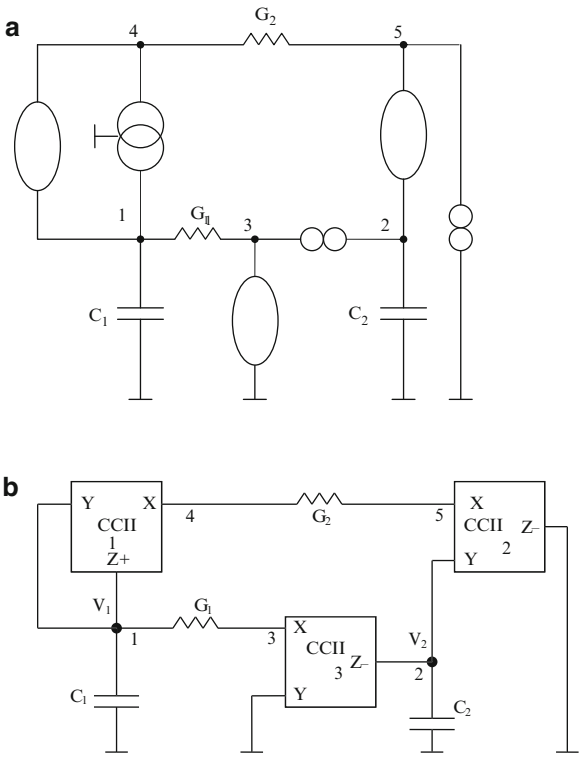

Fig. 4.10 (**a**) Class IV-type A topology II pathological realization 1. (**b**) Three CCII realization of Fig. 4.10a

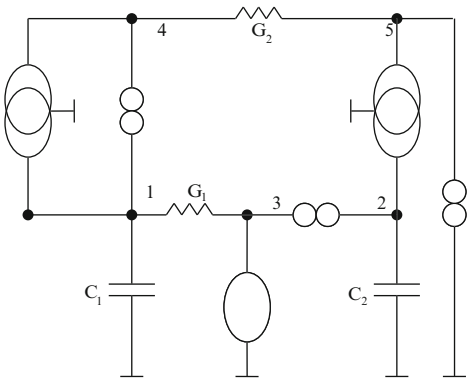

Fig. 4.11 Class IV-type A topology II pathological realization 2

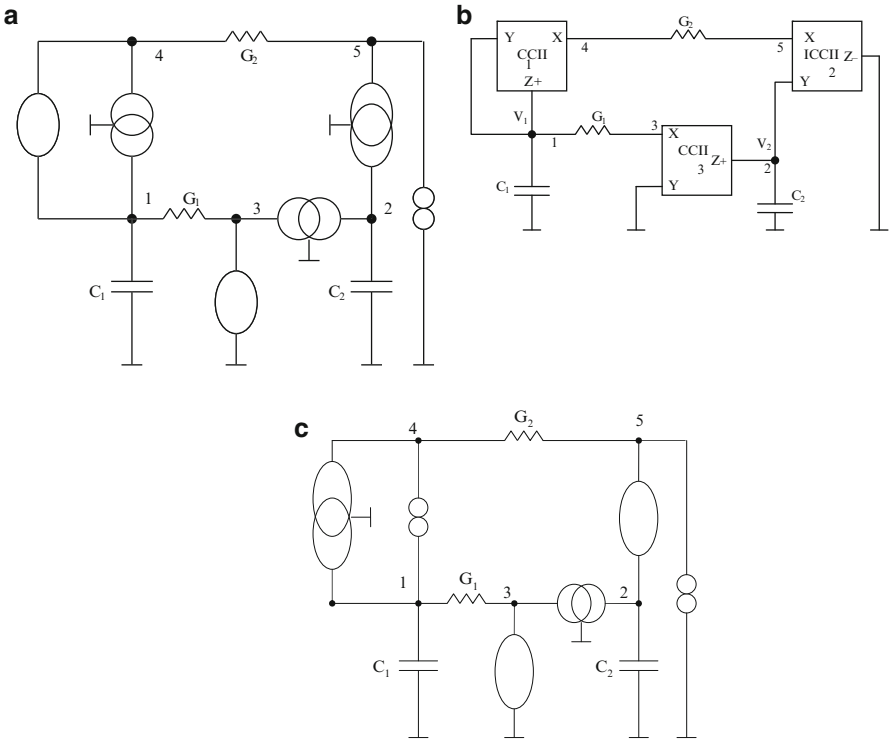

Fig. 4.12 (**a**) Class IV-type B topology II pathological realization. (**b**) Two CCII one ICCII realization of Fig. 4.12a. (**c**) Class IV-type B topology II pathological realization 2

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Chapter 5
Active Filter Design Using a Two-Graph Based Transformation Technique

Mourad Fakhfakh and Marian Pierzchała

5.1 Introduction

Active filter synthesis and design has been thoroughly investigated in the literature. The discovery of new active *RC*-circuits has been accomplished by using a variety of techniques. The modified nodal approach (MNA) has become the industry standard for both numerical and symbolic analysis [1, 2]. For the MNA, dimensions of the matrix and its representation are dependent on the type of elements encompassed in the circuit. This does not greatly obstruct the circuit's analysis where the circuit elements are known in advance and the matrix dimensions and basis can be set accordingly. However, this is a problem for circuit synthesis where the types of elements that are needed for the construction of the "new" active circuit are not known a priori. For a framework encompassing both circuit analysis and synthesis, it is necessary to respect the dimensionality, and that the chosen basis be independent of the type of elements. The admittance matrix satisfies these conditions, as the number of nodes in the circuit determines the dimensions of the matrix. However, the admittance matrix representation (NAM) suffers from the problem that key ideal circuits elements, including nullors and most dependent sources, require infinite matrix elements. The problem of the infinity elements in the NAM has been solved by using a form of a limit variable, called an infinity-variable, or ∞-variables [3]. The physical interpretation of such variables is not obvious and the synthesis method of active *RC*-circuits [4] with these elements is complicated.

In this chapter we propose a new method that overcomes the abovementioned difficulties. Our method uses the two-graph technique, which was first developed by Mielke in [5].

M. Fakhfakh (✉)
University of Sfax, Sfax, Tunisia
e-mail: mourad.fakhfakh@ieee.org

M. Pierzchała
Wroclaw University of Technology, Wroclaw, Poland
e-mail: marian.pierzchala@pwr.wroc.pl

E. Tlelo-Cuautle (ed.), *Integrated Circuits for Analog Signal Processing*,
DOI 10.1007/978-1-4614-1383-7_5,

Instead of using the incidence matrix to express KCL and KVL relationships, our method uses the fundamental and cutset matrices. For any given R, C, L, E, I, cs[1] network, we first form a closed system [6], and then construct the corresponding voltage graph G_V and current graph G_I. For the arbitrarily chosen common tree T, we construct the fundamental loop matrix B_T^V and the fundamental cutest matrix Q_C^I in both G_V and G_I. (We refer the reader to [5–7] for further details regarding the two-graph technique).

The classical two-graph method works only on R, L, C, E, I networks that may contain voltage controlled current sources (*VCCS*) (for network containing other elements, some preliminary network transformation might be required [6]). In this chapter we will also deal with the improved approach proposed in [8] which enables supporting the remaining controlled sources.

Actually, the design of new active *RC*-filters has been accomplished by using a variety of techniques. This includes proposing a general architecture, proposing a particular circuit topology, analyzing it and matching its coefficients, applying a transformation to a known circuit, dealing with some general approaches, such as the morphological approach and the computer generation of all possible topologies, and deriving an active *RC*-circuit from a symbolic transfer function by admittance matrix transformations [4].

In this chapter we deal with the transformation technique that is applied to a known circuit, because in many practical situations, engineers prefer to use the *LC*-filter prototype as a basis of the active *RC*-circuits synthesis.

The proposed work is mainly composed of two parts.

The first part (Sect. 5.2) briefly recalls the transformation technique and provides necessary details on the use of the two-graph technique for synthesizing lossless inductor based circuits.

The second part (Sect. 5.3) proposes a novel approach to generate lossy inductors. Adaptation and improvement of the transformation technique are detailed. Viability of the proposed technique is highlighted via the design of active filters using CMOS second generation current conveyors. SPICE simulations are given for this purpose.

5.2 Transformation of Lossless *LC*-Filters to Active *RC*-Circuits

5.2.1 The Two-Graph Technique

The two-graph technique [5–7] operates using two weighted graphs: a voltage graph (G_V) and a current graph (G_I). The classical approach works only on *RLC*-networks that may contain voltage controlled current sources (*VCCS*). The approach has been

[1] *R*,*C*,*L*,*E*,*I*,*cs* stand for resistors, capacitors inductors, independent voltage and current sources, and all types of controlled sources.

Table 5.1 $T_C^I = -(Q_C^I)^t$

	I_E	I_{CT}	I_{LT}	I_{RT}
I	$(-Q_{I,E})^t$	$(-Q_{I,C_T})^t$	$(-Q_{I,L_T})^t$	$(-Q_{I,R_T})^t$
$\mathbf{I_{CC}}$	$(-Q_{C_C,E})^t$	$(-Q_{C_C,C_T})^t$	$(-Q_{C_C,L_T})^t$	$(-Q_{C_C,R_T})^t$
$\mathbf{I_{LC}}$	$(-Q_{L_C,E})^t$	$(-Q_{L_C,C_T})^t$	$(-Q_{L_C,L_T})^t$	$(-Q_{L_C,R_T})^t$
$\mathbf{I_{GC}}$	$(-Q_{G_C,E})^t$	$(-Q_{G_C,C_T})^t$	$(-Q_{G_C,L_T})^t$	$(-Q_{G_C,R_T})^t$

Table 5.2 B_T^V

	E	V_{CT}	V_{LT}	V_{RT}
$\mathbf{V_I}$	$B_{I,E}$	B_{I,C_T}	B_{I,L_T}	B_{I,R_T}
$\mathbf{V_{CC}}$	$B_{C_C,E}$	B_{C_C,C_T}	B_{C_C,L_T}	B_{C_C,R_T}
$\mathbf{V_{LC}}$	$B_{L_C,E}$	B_{L_C,C_T}	B_{L_C,L_T}	B_{L_C,R_T}
$\mathbf{V_{GC}}$	$B_{G_C,E}$	B_{G_C,C_T}	B_{G_C,L_T}	B_{G_C,R_T}

improved and has been extended to support the remaining controlled sources [8] and two-graph stamps of the other linear controlled sources were proposed. In short, the two-graph technique consists of the following: the network is topologically represented by a linear graph that is composed of a voltage-graph and a current-graph, as stated above. Independent sources are replaced by dependent sources that are controlled by the desired output variable, thus forming a closed system [6]. The corresponding matrix equation system can be represented by expression (5.1).

$$H\,x = \begin{pmatrix} -I & 0 & Z_T & 0 \\ B_T^V & -I & 0 & 0 \\ 0 & 0 & -I & Q_C^I \\ 0 & Y_C & 0 & -I \end{pmatrix} \begin{pmatrix} V_T \\ V_C \\ I_T \\ I_C \end{pmatrix} = \begin{pmatrix} 0 \\ 0 \\ 0 \\ 0 \end{pmatrix} \tag{5.1}$$

Z_T and Y_C refer to matrices of the impedances of the tree elements and the admittances of the co-tree elements, respectively. I is the identity matrix and (B_T^V, Q_C^I) denote the fundamental loop matrix and the fundamental cut-set matrices (of orders (m,n) and (n,m), respectively).

Tables 5.1 and 5.2 give the general forms of the transposed cutest-matrix and the loop-matrix, where the first column and the first row of each table refer to the considered tree and cutset elements, respectively. Indexes C and T refer to the cotree and the tree position, respectively.

Further information and details regarding the two-graph technique can be found in [5–7].

5.2.2 *Application to the Synthesis of Active Filters*

This section details operations for replacing the loop and cutset matrices of the *LC*-filter $[(B_T^V)_{LC}, (T_C^I)_{LC}]$ by the matrices of the *RC*-circuit $[(B_T^V)_{RC}, (T_C^I)_{RC}]$.

Table 5.3 $(B_T^V)_{LC}$ and $(T_C^I)_{LC} = ((-Q_C^I)^t)_{LC}$ for LC-filters with independent current sources $T_C^I = -(Q_C^I)^t$ **(a)** $(B_T^V)_{LC}$ **(b)** $(T_C^I)_{LC} = ((-Q_C^I)^t)_{LC}$

(a)	V_{CT}
$\mathbf{V_I}$	B_{I,C_T}
$\mathbf{V_{LC}}$	B_{L_C,C_T}
(b)	I_{CT}
$\mathbf{I}$	$(-Q_{I,C_T})^t$
$\mathbf{I_{LC}}$	$(-Q_{L_C,C_T})^t$

Table 5.4 The $1/s^2 C_Y L_X$ submatrix. **(a)** Element of B_{L_C,C_T} for an LC-filter. **(b)** Element of T_{C_T,L_C} for an LC-filter

(a)	V_{Cy}
$\mathbf{V_{Lx}}$	1
(b)	I_{Cy}
$\mathbf{I_{Lx}}$	1

Table 5.5 The $1/s^2$ $R_{X1}R_{X2}C_{Y1}C_{Y2}$ submatrix. **(a)** Element of B_{C_T,R_C} for an RC-circuit. **(b)** Element of T_{C_T,R_C} for an RC-circuit

(a)	V_{Cy1}	V_{Cy2}
$\mathbf{V_{Rx1}}$	1	0
$\mathbf{V_{Rx2}}$	0	1
(b)	I_{Cy1}	I_{Cy2}
$\mathbf{I_{Rx1}}$	0	1
$\mathbf{I_{Rx2}}$	-1	0

The networks to be considered are connected, linear, time-invariant LC-filters. It is assumed that any independent voltage source has been replaced by a dependent voltage source controlled by the desired output variables, thus forming a closed system [6].

For instance, the fundamental circuit matrix $(B_T^V)_{LC}$ and the transpose of the cut-set matrix $(T_C^I)_{LC} = ((-Q_C^I)^t)_{LC}$ for LC-filters with independent current sources (the inductors in the cotree branches and the capacitors in the tree branches), can be presented as follows (see Table 5.3).

Each single element $1/s^2 C_x L_y$ of the submatrices B_{L_C,C_T}, T_{C_T,L_C} (see Table 5.4) may be replaced by two capacitors and two resistors $C_{x1}, C_{x2}, R_{y1}, R_{y2}$ in appropriate configuration (see Table 5.5). It has been shown in [9] that 16 combinations are possible to generate the equivalent submatrix. It is easy to notice that this configuration of capacitors and resistors has also dimension of $1/s^2$ (i.e. the term: $1/s^2 R_{y1}R_{y2}C_{x1}C_{x2}$) in the network function, similarly as the inductor L and the capacitor C (i.e. the term: $1/s^2 L_y C_x$)).

According to Table 5.5, it is obvious that the equivalent RC-circuit should have special kind of switches, i.e. switches that connect in the different ways the voltage and the current graphs. Indeed, and as an example, $(\mathrm{V}(R_{X1}) = \mathrm{V}(C_{Y1})$ and $\mathrm{V}(R_{X2}) = \mathrm{V}(C_{Y2}))$, however, $(\mathrm{I}(C_{Y1}) = \mathrm{I}(R_{X2})$ and $\mathrm{I}(C_{Y2}) = -\mathrm{I}(R_{X1}))$.

It has been shown in [10] that nullors can ensure such special switching functions.

In the following the switches are represented in the voltage position, i.e. the short-cut position fulfils the relations imposed by the voltage graph, whereas the open position is relative to the current graph.

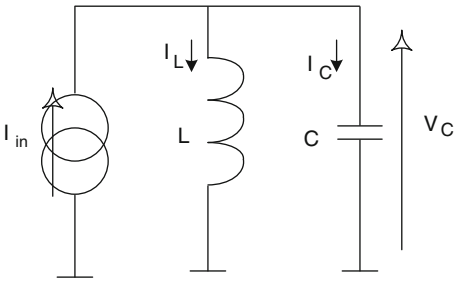

Fig. 5.1 A lossless parallel *LC*-filter (corresponding $(B_T^V)_{LC}$ and $(T_C^I)_{LC} = ((-Q_C^I)^t)_{LC}$ matrices are given in Table 5.6): Example #1

Table 5.6 $(B_T^V)_{LC}$ and $(T_C^I)_{LC} = ((-Q_C^I)^t)_{LC}$ for lossless parallel *LC*-filters with independent current. **(a)** $(B_T^V)_{LC}$ **(b)** $(T_C^I)_{LC} = ((-Q_C^I)^t)_{LC}$

(a)	V_C
$\mathbf{V_{Iin}}$	-1
$\mathbf{V_L}$	1
(b)	I_C
$\mathbf{I_{in}}$	-1
$\mathbf{I_L}$	1

Table 5.7 $(B_T^V)_{LC}$ and $(T_C^I)_{LC} = ((-Q_C^I)^t)_{LC}$ for lossless *RC*-filters with independent voltage source. **(a)** $(B_T^V)_{LC}$ **(b)** $(T_C^I)_{LC}$

(a)	V_{C1}	V_{C2}
$\mathbf{V_{Iin}}$	-1	0
$\mathbf{V_{R1}}$	0	1
$\mathbf{V_{R2}}$	1	0
(b)	I_{C1}	I_{C2}
$\mathbf{I_{in}}$	-1	0
$\mathbf{I_{R1}}$	1	0
$\mathbf{I_{R2}}$	0	-1

5.2.2.1 Application Example #1

As an application example, let's consider the lossless *LC*-filter presented in Fig. 5.1.

The basic idea consists of replacing the inductor L, from the cotree branch, by a capacitor C in the tree branch and adding elements to change directions of the transmissions (from the current to the voltage on the direction from the voltage to the current). This function can be realized using resistors, which will be placed, in the cotree branches of the graph. Accordingly, the B and T matrices, given in Table 5.6 will be modified as given in Table 5.7. It is simple to check that in this *RC*-configuration we have a similar network functions as in the *LC*-circuit. For example, in the *LC*-circuit the voltage on the capacitor C is given by expression (5.2) and for the *RC*-circuit, the output voltage is given by (5.3).

$$V_C = \frac{sL}{1+s^2LC} I_{in} \tag{5.2}$$

$$V_{out} = \frac{sR_1R_2C_2}{1+s^2R_1R_2C_2} I_{in} \tag{5.3}$$

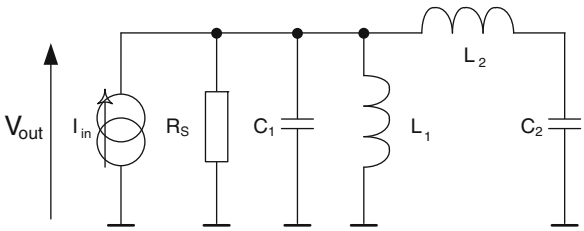

Fig. 5.2 A bi-band filter: Example #2

Table 5.8 *B* and *T* matrices of the bi-band circuit of Fig. 5.2. **(a)** The *B* matrix. **(b)** The *T* matrix

(a)	V_{L1}	V_{L2}
$\mathbf{V_{Iin}}$	−1	0
$\mathbf{V_{RS}}$	1	0
$\mathbf{V_{C1}}$	1	0
$\mathbf{V_{C2}}$	1	−1
(b)	I_{C1}	I_{C2}
$\mathbf{I_{in}}$	−1	0
$\mathbf{I_{RS}}$	1	0
$\mathbf{I_{C1}}$	1	0
$\mathbf{I_{C2}}$	1	−1

Table 5.9 *B* and *T* matrices of the *RC* equivalent circuit. **(a)** The *B* matrix. **(b)** The *T* matrix

(a)	V_{R1}	V_{R2}	V_{R3}	V_{R4}
$\mathbf{V_{Iin}}$	−1	0	0	0
$\mathbf{V_{RS}}$	1	0	0	0
$\mathbf{V_{C1}}$	1	0	0	0
$\mathbf{V_{C2}}$	0	1	0	0
$\mathbf{V_{C3}}$	1	0	1	0
$\mathbf{V_{C4}}$	0	0	0	1
(b)	I_{R1}	I_{R2}	I_{R3}	I_{R4}
$\mathbf{I_i}$	0	−1	0	0
$\mathbf{I_{RS}}$	0	1	0	0
$\mathbf{I_{C1}}$	0	1	0	0
$\mathbf{I_{C2}}$	−1	0	0	0
$\mathbf{I_{C3}}$	0	1	0	1
$\mathbf{I_{C4}}$	0	0	−1	0

5.2.2.2 Application Example #2

As a second application example, let us consider the bi-band circuit presented in Fig. 5.2, where two inductors are considered; a grounded inductor and a floating one.

Table 5.8 presents the corresponding *B* and *T* matrices.

By adopting the proposed method of transformation of the inductor using capacitors and resistor, the following matrices can be constructed.

Using the software proposed in [11], it is easy to compute both transfer functions using the *B* and *T* matrices corresponding to Tables 5.8 and 5.9, respectively.

a

```
 PB Coefficients:
a1=L1                          0
t1=L1/Rs                       0
T1=L1*C1                       0
T2=L1*C2                       T3=L2*C2
```

b

```
-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*
-*-*-*-*-*-*-*-*   NUMERATOR   *-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*
-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*
______________________________________________________________________

n1=(a1)
______________________________________________________________________

n3=(a1*T3)
```

c

```
-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*
-*-*-*-*-*-*-*-*   DENOMINATOR   *-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*
-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*
______________________________________________________________________

d0=1
______________________________________________________________________

d1=(t1)
______________________________________________________________________

d2=(T3)+(T2)+(T1)
______________________________________________________________________

d3=(t1*T3)
______________________________________________________________________

d4=(T1*T3)
----------------------------------------------------------------------
```

Fig. 5.3 Screenshot of the transfer function corresponding to Table 5.8 obtained using [11]. (**a**) The product matrix coefficients. (**b**) The numerator coefficients. (**c**) The denominator coefficients

Coefficients relative to the numerator and to the denominator of both transfer functions are given in Figs. 5.3 and 5.4, respectively.

Thus, by identifying results shown in Figs. 5.3 and 5.4, we have: $C_1 = C_2$, $C_2 = C_3$, $L_1 = R_2R_1C_1$ and $L_2 = R_4R_3C_4$.

Accordingly, the "switched" circuit can be constructed. Figure 5.5 presents the equivalent "switched" circuit that satisfies the relationships presented in Table 5.9.

a

```
 PB Coefficients:
0            a1=R2        0            0
0            b1=R2/Rs     0            0
0            t1=R2*C1     0            0
t2=R1*C2     0            0            0
0            t3=R2*C3     0            t4=R4*C3
0            0            t5=R3*C4     0
```

b

```
-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*
-*-*-*-*-*-*-*-*-*    NUMERATOR    *-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*
-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*
______________________________________________________________________

n1=(a1*t2)
______________________________________________________________________

n3=(a1*t2*t4*t5)
```

c

```
-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*
-*-*-*-*-*-*-*-*-*    DENOMINATOR    *-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*
-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*
______________________________________________________________________

d0=1
______________________________________________________________________

d1=(b1*t2)
______________________________________________________________________

d2=(t4*t5)+(t2*t3)+(t1*t2)
______________________________________________________________________

d3=(b1*t2*t4*t5)
______________________________________________________________________

d4=(t1*t2*t4*t5)
----------------------------------------------------------------------
```

Fig. 5.4 Screenshot of the transfer function corresponding to Table 5.9 obtained using [11]. (**a**) The product matrix coefficients. (**b**) The numerator coefficients. (**c**) The denominator coefficients

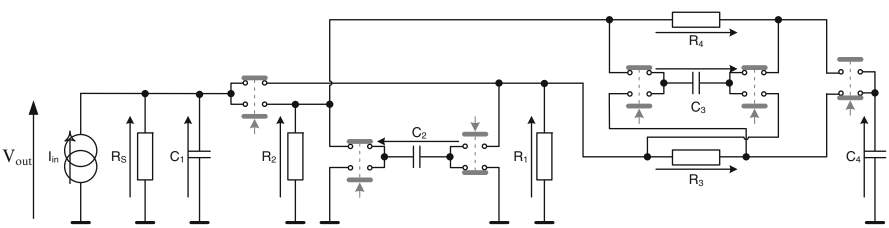

Fig. 5.5 The "switched" circuit obtained from Table 5.9

5.3 Designing Lossy Filters

In the following, we propose the application of the above-introduced technique to the synthesis of active lossy filters while minimizing the number of additional resistors.

Let's consider the lossy filter given in Fig. 5.6. The corresponding B and T matrices are given in Table 5.10.

Coefficients of the transfer function of the passive RLC circuit are given in Fig. 5.7.

Applying the technique introduced above, allows removing the two inductors and replacing each of them by two resistors and one capacitor.

Accordingly, the modified B and T matrices can be presented, as it is given in Table 5.11.

It is possible to further simplify the equivalent circuit that can be constructed from Table 5.11. Indeed, one can notice that the contribution of resistor R_2, i.e. the term s powered to 1 in the corresponding product matrix can be reproduced by substituting that resistor by another one from those already encompassed in the table, i.e. in the new RC-circuit. Four candidates exist, namely R_{d1}, R_{d2}, R_{d3} and R_{d4}. Using the symbolic analyzer proposed in [11], one can easily check that only R_{d3} and R_{d4} allow obtaining the expected transfer function that is equivalent to the ideal LC-circuit transfer function.

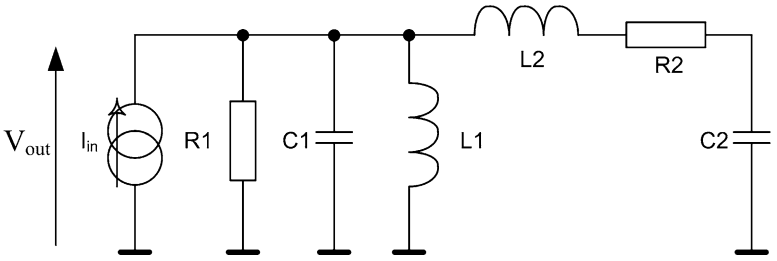

Fig. 5.6 An RLC biband filter: Example #3

Table 5.10 B and T matrices of the circuit shown in Fig. 5.6. **(a)** The B matrix. **(b)** The T matrix

(a)	V_{L1}	V_{R2}	V_{L2}
$\mathbf{V_{Iin}}$	−1	0	0
$\mathbf{V_{R1}}$	1	0	0
$\mathbf{V_{C1}}$	1	0	0
$\mathbf{V_{C2}}$	1	−1	−1
(b)	I_{L1}	I_{R2}	I_{L2}
$\mathbf{I_{in}}$	−1	0	0
$\mathbf{I_{R1}}$	1	0	0
$\mathbf{I_{C1}}$	1	0	0
$\mathbf{I_{C2}}$	1	−1	−1

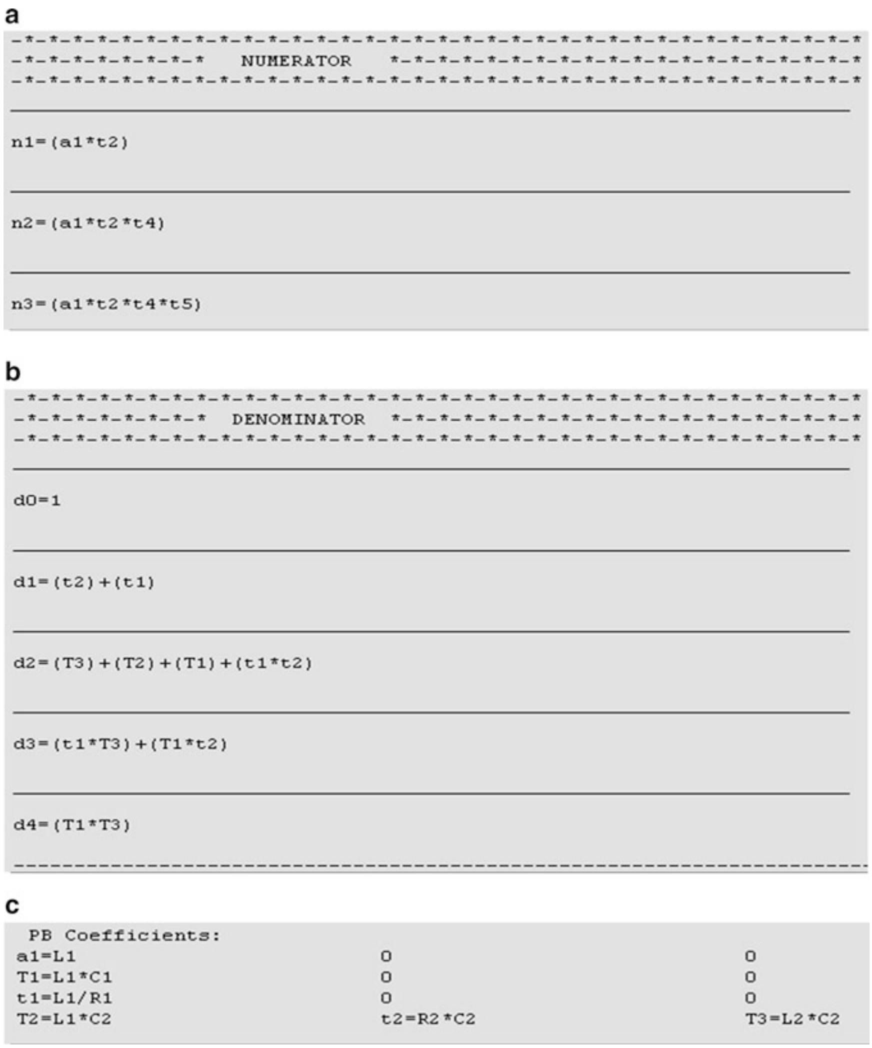

Fig. 5.7 Screenshot of the transfer function corresponding to Table 5.10 obtained using [11]. (**a**) The numerator coefficients. (**b**) The denominator coefficients. (**c**) The product matrix coefficients

For example, Table 5.12 gives B and Q tables corresponding to the substitution of R_2 by R_{d3}.

The corresponding transfer function can be obtained using [11]. Figure 5.8 gives coefficients of the transfer function (numerator and denominator) and the corresponding product matrix elements. Accordingly, we have $L_1 = R_{d1}R_{d2}C_{d1}$, and $L_2 = R_{d3}R_{d4}C_{d2}$.

Table 5.11 B and T matrices of the active circuit equivalent to the passive circuit shown in Fig. 5.6. **(a)** The B matrix. **(b)** The T matrix

(a)	V_{Rd1}	V_{Rd2}	V_{R2}	V_{Rd3}	V_{Rd4}
$\mathbf{V_I}$	0	−1	0	0	0
$\mathbf{V_{R1}}$	1	0	0	0	
$\mathbf{V_{C1}}$	0	1	0	0	0
$\mathbf{V_{Cd1}}$	1	0	0	0	0
$\mathbf{V_{C2}}$	0	1	−1		−1
$\mathbf{V_{Cd2}}$	0	0	0	1	0
(b)	I_{Rd1}	I_{Rd2}	I_{R2}	I_{Rd3}	I_{Rd4}
$\mathbf{I}$	−1	0	0	0	0
$\mathbf{I_{R1}}$	1	0	0	0	
$\mathbf{I_{C1}}$	1	0	0	0	0
$\mathbf{I_{Cd1}}$	0	−1	0	0	0
$\mathbf{I_{C2}}$	1	0	−1	−1	0
$\mathbf{I_{Cd2}}$	0	0	0	0	−1

Table 5.12 Substitution of R_2 by R_{d3}. **(a)** The modified B matrix. **(b)** The modified T matrix

(a)	V_{Rd1}	V_{Rd2}	V_{Rd3}	V_{Rd4}
$\mathbf{V_I}$		−1	0	0
$\mathbf{V_{R1}}$	1	0	0	
$\mathbf{V_{C1}}$		1	0	0
$\mathbf{V_{Cd1}}$	1	0	0	0
$\mathbf{V_{C2}}$	0	1	−1	−1
$\mathbf{V_{Cd2}}$	0	0	1	0
(b)	I_{Rd1}	I_{Rd2}	I_{Rd3}	I_{Rd4}
$\mathbf{I}$	−1	0	0	0
$\mathbf{I_{R1}}$	1	0	0	
$\mathbf{I_{C1}}$	1	0	0	0
$\mathbf{I_{Cd1}}$	0	−1	0	0
$\mathbf{I_{C2}}$	1	0	−1	0
$\mathbf{I_{Cd2}}$	0	0	0	−1

In order to design an equivalent circuit that reproduces the current and voltage relationships given by the B and T matrices given in Table 5.12, the use of the special switches is mandatory, as it was explained above. The equivalent circuit is shown in Fig. 5.9.

As introduced in [9], nullors can emulate such weird behavior of switches. Accordingly, a nullor based circuit can be constructed. The equivalent circuit is shown in Fig. 5.10. Knowing that a nullor can be considered as a universal element since it can reproduce the ideal behavior of many circuits, such as an Op-Amp, a current conveyor etc. The later was used to design the equivalent "switched" circuit. Figure 5.11 gives the current conveyor based RC-circuit.

The circuit presented in Fig. 5.11 was designed using the second generation current conveyor used in [9]. In Fig. 5.12 we present corresponding SPICE simulations, where we notice a good agreement between the ideal LC-filter

a

```
-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*
-*-*-*-*-*-*-*-*   NUMERATOR   *-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*
-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*
______________________________________________________________________

n1=(a1*t2)
______________________________________________________________________

n2=(a1*t2*t4)
______________________________________________________________________

n3=(a1*t2*t4*t5)
```

b

```
-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*
-*-*-*-*-*-*-*-*   DENOMINATOR   *-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*
-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*
______________________________________________________________________

d0=1
______________________________________________________________________

d1=(t4)+(b1*t2)
______________________________________________________________________

d2=(t4*t5)+(t2*t3)+(t1*t2)+(b1*t2*t4)
______________________________________________________________________

d3=(t1*t2*t4)+(b1*t2*t4*t5)
______________________________________________________________________

d4=(t1*t2*t4*t5)
----------------------------------------------------------------------
```

c

PB Coefficients:

a1=Rd1	0	0	0
t1=Rd1*C1	0	0	0
b1=Rd1/R1	0	0	0
0	t2=Rd2*Cd1	0	0
t3=Rd1*C2	0	t4=R2*C2	0
0	0	0	t5=Rd4*Cd2

Fig. 5.8 Screenshot of the transfer function corresponding to Table 5.12 obtained using [11]. (**a**) The numerator coefficients. (**b**) The denominator coefficients. (**c**) The product matrix coefficients

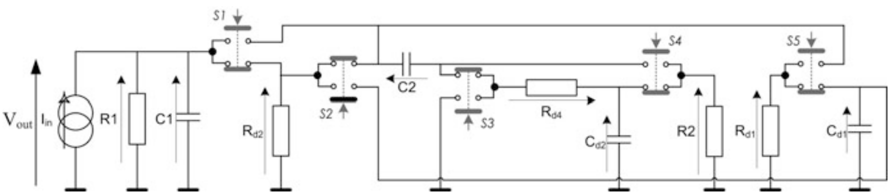

Fig. 5.9 The "switched" circuit (according to Table 5.12)

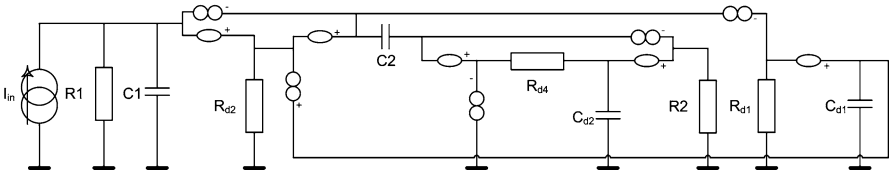

Fig. 5.10 The nullor based circuit that is equivalent to the "switched" circuit shown in Fig. 5.10

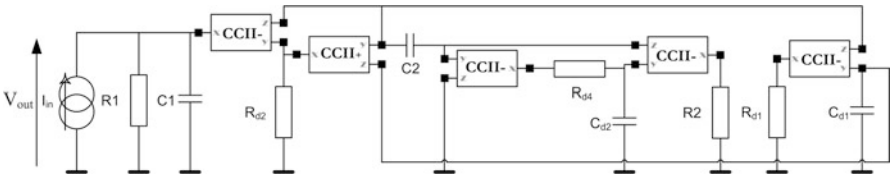

Fig. 5.11 The equivalent current conveyor based filter

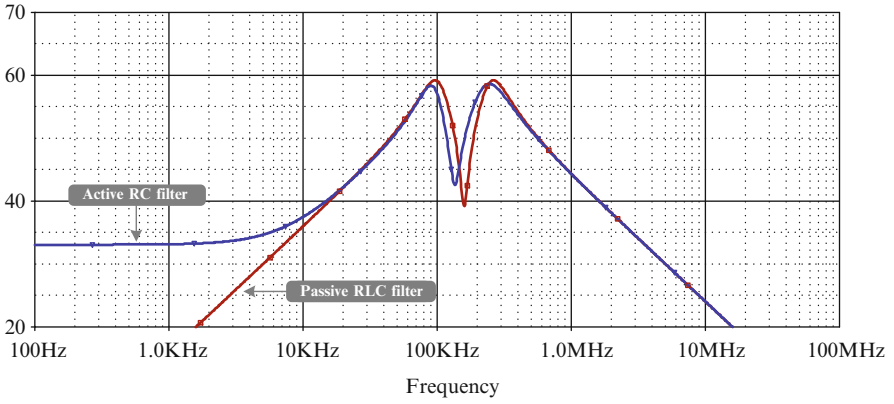

Fig. 5.12 $(V_{out}/I_{in})_{dB} = f(\text{frequency})$

response and the active *RC*-circuit. Component values are as follows: $R_1 = 1\,\text{k}\Omega$, $C_1 = 1\,\text{nF}$, $R_{d2} = 1\,\text{k}\Omega$, $C_2 = 1\,\text{nF}$, $R_{d1} = 1\,\text{k}\Omega$, $C_{d1} = 1\,\text{nF}$, $R_{d4} = 1\,\text{k}\Omega$, $C_{d2} = 10\,\text{nF}$, $R_2 = 100\,\Omega$.

5.4 Conclusions

The use of the two graph technique for the synthesis of active filters was detailed in this chapter. Firstly, designing lossless filters was presented. Then, adapting this technique to the design of active lossy circuits was proposed. Minimizing the use

of passive components, i.e. additional resistors, was also proposed. Designing such lossy active filter using "active" switches, and then using current conveyors, was highlighted. Application examples were given and SPICE simulation results were provided to show viability of the proposed technique.

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Chapter 6
Analog Baseband Filter Design Considerations for Wireless Receivers

Jose Silva-Martinez and Raghavendra Kulkarni

6.1 Introduction

Wireless systems have received significant attention in the recent years due to increased demand for high performance yet portable handheld receivers. This demand coupled with continued device scaling has led to design of multi-million transistor system-on-chip (SoC) solutions with rich digital signal processing (DSP) capabilities. A simple block level partitioning of the receiver is shown in Fig. 6.1. In addition to digital demodulation and signal processing, SoC solutions also require a high performance RF (radio-frequency) receiver in the signal chain. The RF front-end and analog-baseband can be termed as *radio*. The goal of radio is to deliver the desired signal to the demodulator with tolerable impairments (due to circuit non-idealities).

Wireless receivers must extract a weak desired signal buried within a crowded spectrum from plethora of standards supporting variety of analog and digital modulation formats. Successfully tolerating and rejecting undesired spectral content (termed as *blockers*) within the vicinity of the desired signal demands attentive planning of the analog signal processing chain that precedes the digital demodulator. In the absence of RF pre-filtering, analog baseband signal chain must efficiently handle the blocker power along with the desired signal prior to the analog-to-digital converter (ADC). As a result, the incoming blocker profile affects design of the baseband filter and requirements of a subsequent ADC in the signal chain.

Design of analog baseband for a direct-conversion UHF receiver serves as an example to underscore the impact of blockers in this chapter. Section 6.2 highlights the importance of out-of-band linearity specifications and also presents a systematic analysis to understand the interlaced filter specifications and ADC dynamic range (DR) requirements. Two popular filter approximations (Butterworth and Inverse

J. Silva-Martinez (✉) • R. Kulkarni
Texas A&M University, College Station, TX, USA
e-mail: jsilva@ece.tamu.edu; kulkarni.ee@gmail.com

E. Tlelo-Cuautle (ed.), *Integrated Circuits for Analog Signal Processing*,
DOI 10.1007/978-1-4614-1383-7_6,

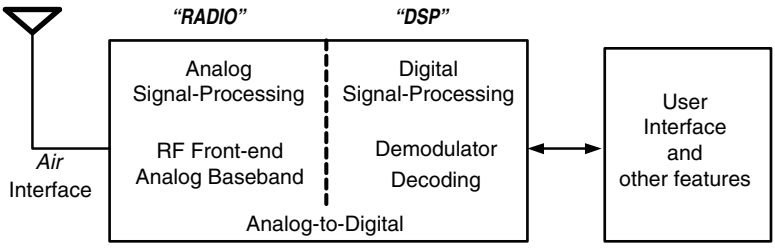


Fig. 6.1 Block level partitioning of a modern wireless device

Chebyshev) are evaluated for blocker filtering efficacy in the presence of analog and digital adjacent blockers since UHF spectrum (470–860 MHz) contains spectral content from both analog and digital modulation sources [1,2]. Section 6.3 provides implementation details of a filter for the UHF receiver example followed by experimental results of the filter and the receiver in Sect. 6.4.

6.2 Analog Baseband Dynamic Range Requirements

A wireless receiver using the direct conversion architecture is shown in Fig. 6.2. The input signal is down-converted (frequency translated from RF passband to lowpass baseband using I/Q demodulation), amplified, filtered by the analog baseband and after A/D conversion is presented to the demodulator. The RF and the baseband signal chain preceding the demodulator is often treated as an impairment block affecting the system performance. The quality of the delivered signal measured by the ratio of desired to undesired signal power (including phase noise, quantization noise, thermal noise and other impairments) depends on the modulation scheme and the bit-error-rate (*BER*) requirement of the system.

Blockers present at the RF input create several challenges since the entire input spectral content should be handled by the receiver front-end without degrading the signal quality for demodulation. For the UHF spectrum example, the undesired analog and digital adjacent blockers could be up to 40 dB higher than the desired signal power raising DR requirements of the receivers. LNAs in the RF signal chain provide broadband amplification and do not perform any channel-selection filtering. But an I/Q demodulator implemented using a passive current-mode mixer can be terminated using a transimpedance amplifier to implement a single-pole that provides first order filtering after signal down-conversion. This filter provides attenuation for blockers located *far* from the desired channel, but leave the spectral energy from immediate adjacent channels almost un-filtered. As a result majority of the *near* broadband spectral energy shows up un-filtered at the input of the analog baseband section. Typically, analog baseband signal chains utilize cascaded filtering

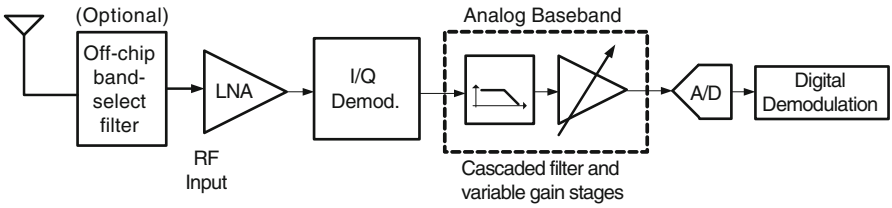


Fig. 6.2 A typical wireless radio using direct conversion architecture

and gain stages as shown in Fig. 6.2. While filtering stages reduce the blocker power successively, the gain stages increase the desired signal. In the following sections we will address how the presence of blockers affects the performance specifications of the analog baseband, and the resolution and cost of a subsequent ADC.

6.2.1 Spurious-Free-Dynamic-Range Requirements

As the signal is processed in the baseband chain, the signal gets corrupted due to additive noise from the active devices and nonlinear distortion components due to weakly-nonlinear behavior of these active devices. While the magnitude of the additive noise is independent of the input signal power, magnitude of the distortion generated depends on input signal to the active device. Higher the magnitude of the input power, larger the distortion. Although signal-to-noise ratio (SNR) increases by increasing the input power, the signal-to-distortion ratio (SDR) drops with increasing input power. This is indeed very critical for the design of first filtering blocks in the baseband signal chain when the blocker is relatively unattenuated. Hence we should expect an optimal input signal power at which the overall signal-to-noise-and-distortion ratio (SNDR) can be maximized. This SNDR value denotes the available Spurious-Free-Dynamic-Range (SFDR) of the system.

An example of the effect of distortion due to out-band blocker on signal dynamic range is shown in Fig. 6.3. The figure plots the desired signal power, blocker power, integrated noise power (input referred) and 3rd order intermodulation distortion (IM3) power (input referred) as the input signal increases on a log–log scale. The blocker is $UD_{\text{dB}} = 30\,\text{dB}$ higher than the desired signal power (UD denotes undesired-to-desired ratio). The distortion power is generated due to the intermodulation of two un-filtered out-band blockers such that the IM3 term falls in-band. In this example, the integrated noise power is independent of the input power and is indicated at $-76\,\text{dBm}$ (or 40 uVrms), while the linearity performance is specified at different third-order intercept points (IIP3) of $+20$ to $+35\,\text{dBm}$. As expected, IM3 power increases with a slope of $+3$ dB/dB with the input power while the desired (or the fundamental) increases with a slope of 1 dB/dB. As indicated in the figure, the distortion power rises out of the output noise floor at different

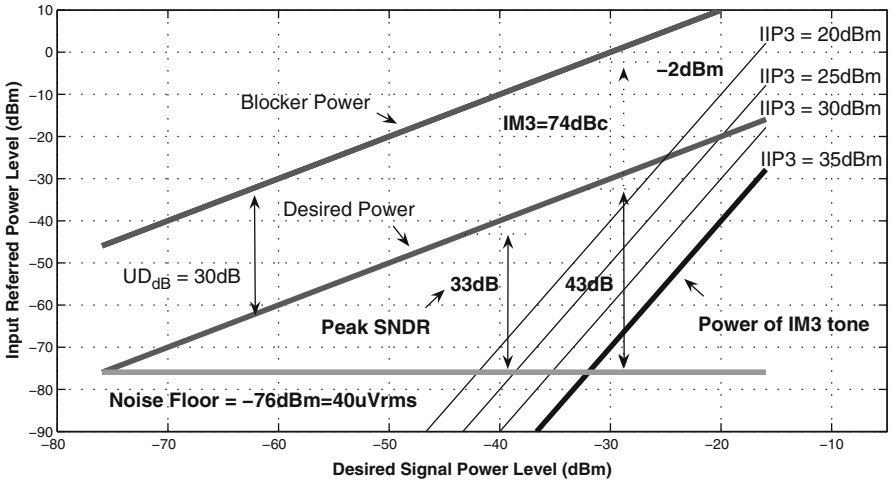


Fig. 6.3 Typical desired, blocker and intermodulation signal power for different out-band IIP3 values

input power levels depending on the linearity performance. Higher the out-band IIP3, higher is the blocker power (and hence the signal power for a given UD_{dB}) at which the distortion power rises above the noise floor. Any increase in the blocker power beyond this will result in SNDR of the desired channel being limited by the distortion power, while any reduction in the signal power leads to drop in the SNR.

As illustrated, compared to general filtering applications, analog baseband section of a wireless receiver signal chain exhibits an important difference. Intermodulation of out-of-filter-band blockers generates output terms that reside together with the desired signal affecting the signal quality. In summary, with regard to baseband SFDR requirements, we make the following observations relevant to design of filters for wireless receivers,

- For low input power levels of the desired channel, the input referred noise of the analog baseband must be minimized such that the in-band SNR does not limit the system performance.
- Since the input power levels of the desired channel are lower than the blocker power, distortion components generated due to in-band signals do not limit the SDR.
- Distortion due to large out-of-band blockers (UD_{dB} higher than desired) can limit the overall SNDR performance. Analog baseband must exhibit very good out-of-band linearity performance to keep the distortion components below noise floor. Hence blocker tolerance is very critical in the first filtering blocks in the signal chain after signal down-conversion.

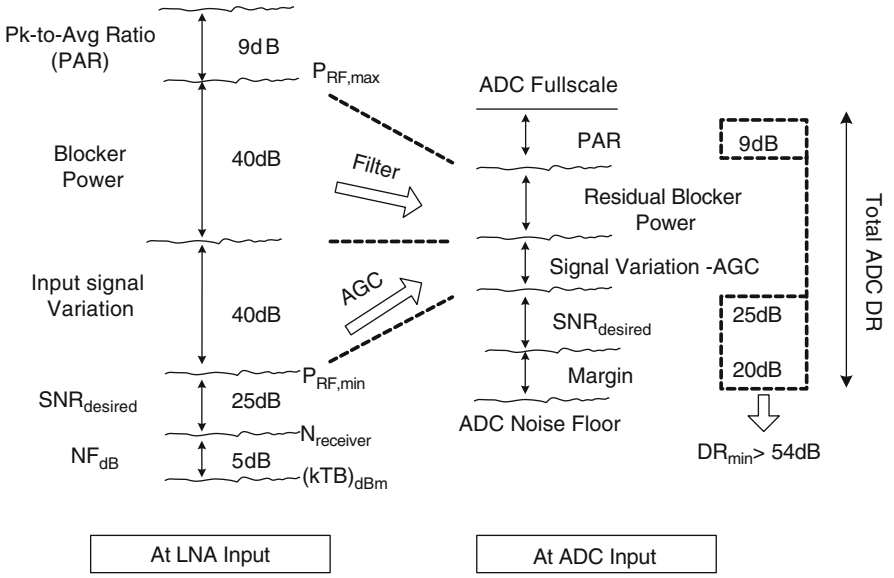


Fig. 6.4 Effect of filtering and AGC on dynamic range requirements from Antenna to ADC

6.2.2 *Interdependence of Baseband Filter and ADC Requirements*

In this section we further investigate the impact of blocker power in the receiver chain at the analog baseband and ADC interface. As illustrated in Fig. 6.2, the RF input signal is sensed first at the LNA input and is processed to extract the desired spectral content. The signal DR requirements from LNA input to the ADC input in the receiver are illustrated in Fig. 6.4. Typical numbers relevant to an UHF receiver example are also indicated in the figure.

As illustrated in the figure, the input noise floor of the receiver in dBm is

$$\text{Receiver noise floor} = N_{\text{receiver}} = (\text{kTB})_{\text{dBm}} + NF_{\text{dB}}. \tag{6.1}$$

where B is the *channel* bandwidth and NF_{dB} is the noise figure of the receiver.

Then, the sensitivity of the receiver defined as the minimum desired signal power to meet the SNR requirement for the modulation scheme is,

$$\text{Receiver sensitivity } = P_{\text{RF,min}} = N_{\text{receiver}} + SNR_{\text{desired}}. \tag{6.2}$$

As indicated in Fig. 6.4, the signal power of the desired channel received at the antenna can vary by up to 40 dB. In addition to this variation, undesired blocker 40 dB larger than the desired channel could appear at the LNA input (in the worst case) raising the dynamic range of the signal. Peak-to-average Ratio (PAR) indicated

in the figure is an attribute of the orthogonal-frequency-division-multiplexing (OFDM) based modulation schemes which results due to multiple carriers. Hence the radios built for OFDM systems must budget for PAR in the DR calculations to avoid severe distortion and clipping in the signal chain.

Analog baseband that resides in the signal chain after the I/Q demodulation but prior to an ADC processes the input signal after signal down-conversion and performs two important tasks: (1) filter undesired adjacent blocker power; and (2) deliver constant power to the ADC with the desired SNDR. Hence for a given input signal and blocker profile, choice of the baseband filter (order and approximation type) determines the DR of a subsequent ADC.

As indicated in Fig. 6.4, ADC DR should do the following:

1. Be greater than the minimum SNR requirement of the modulation scheme plus a design margin to minimize the SNR loss due to quantization noise of the ADC. In Fig. 6.4, a 20 dB margin (≈3 bits) is indicated [3–5].
2. Accommodate the peak-to-power-average ratio (PAR) of the received signal.
3. Include the input signal power variation that is not covered by automatic gain control (AGC). The residual desired signal power variation must also account for the resolution and the range of the AGC in the system.
4. Accommodate the residual unfiltered blocker power at the ADC input after the baseband filter.
5. Meet the outband linearity performance requirement based on the residual blocker power.

It should be noted from Fig. 6.4 that, for the UHF receiver example the $DR_{\min} >$ 54 dB (≈ 9 bits) even assuming a perfect AGC to compensate for the input signal power variation and also complete blocker filtering prior to the ADC. In addition, the minimum sampling frequency of the ADC should be chosen to keep the undesired aliased signal power below the desired signal power by at least $DR_{\min}$.

The effect of Butterworth filter order on sampling frequency and resolution of the ADC has been analyzed in [6]. We focus on item (4) in this chapter and quantify the component of the ADC DR required to accommodate the residual blocker power for Butterworth and Inverse Chebyshev analog filters with orders ranging from 3 to 8.[1] These two filters are chosen so that we can compare the impact of an all-pole approximation (Butterworth) and an approximation with poles and stop-band zeros (Inverse Chebyshev). The residual power evaluation is performed for both digital and analog adjacent channels as undesired blockers in the UHF receiver example can employ either modulation scheme. In analog channels, the bulk of the signal energy is concentrated near the carrier, resulting in strong peaks. In contrast, the energy in a multi-carrier modulated digital channel is spread smoothly across the

[1] A 1st order pole is added to an $(n-1)$th Inverse Chebyshev filter for comparison to nth order Butterworth filter. This addition improves the high frequency attenuation for even order Inverse Chebyshev filters.

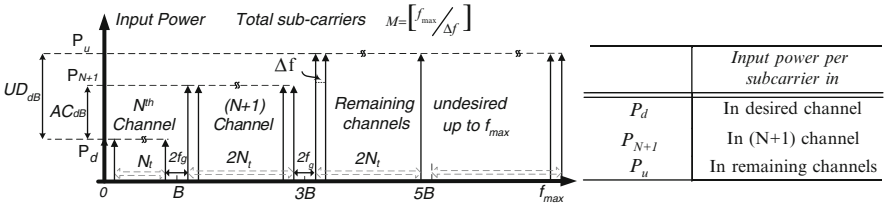


Fig. 6.5 Baseband input spectrum with digital adjacent channels

channel [7]. Understanding the impact of this difference is important as analog modulation techniques continue to be used along with digital broadcast [8]. The following analysis will show that the higher order Inverse Chebyshev filters perform better at reducing the undesired power in the presence of analog adjacent channels.

6.2.2.1 Residual Undesired Power from Digital Adjacent Channels

To evaluate the residual undesired power for digital channels, the baseband input spectrum is modeled as shown in Fig. 6.5. From this figure:

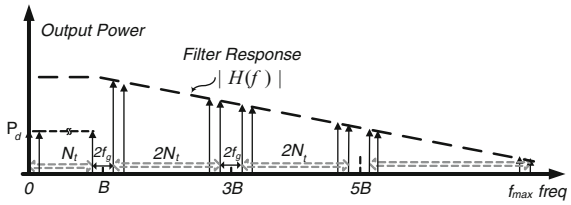
- The input power spectral density (PSD) $S_{\text{in}}(f)$ is defined for a broadband frequency range $(0, f_{\text{max}})$. Sub-carriers in the input spectrum are separated by $\triangle f$, resulting in $M = \lfloor f_{\text{max}}/\Delta f \rfloor$ total sub-carriers.
- The desired channel resides in a single-sided bandwidth of $(0, B)$ with N_t sub-carriers in $(0, B - f_{\text{g}})$ and a guard band f_{g} with zero power carriers. Each undesired channel has a two-sided bandwidth of $2B$ with $2N_t$ sub-carriers in $2(B - f_{\text{g}})$.
- The input sub-carrier power in the desired channel is set to P_{d}. The power of sub-carriers P_{N+1} in the first adjacent channel (referred as the $N + 1$ channel) is set AC_{dB} higher than P_{d}. For the remaining undesired channels ($> N + 1$), the power of sub-carriers P_u is UD_{dB} higher than the desired channel.

Total integrated input power P_{in} is

$$P_{\text{in}} = \int_0^{f_{\text{max}}} S_{\text{in}}(f)\,\mathrm{d}f. \tag{6.3}$$

This input spectrum is filtered using a transfer function $H(f)$. Hence, the integrated output power within the frequency range (f_1, f_2) is

$$P = \int_{f_1}^{f_2} S_{\text{in}}(f)\,|H(f)|^2\,\mathrm{d}f. \tag{6.4}$$



$$P_x = \int_{f_1}^{f_2} S_{in}(f)\ |H(f)|^2\, df$$

P_x	f_1	f_2
$P_{desired}$	0	B-f_g
$P_{res,N+1}$	B+f_g	$3B$-f_g
$P_{res,Total}$	B+f_g	f_{max}

Fig. 6.6 Output power density and definitions of integrated power in the desired channel, residual N+1 adjacent channel, and residual power in all undesired channels

Table 6.1 Parameters used for the analysis

Parameter	Values
B, f_g, f_{max}	4 MHz, 200 kHz, 396 MHz
AC_{dB}, UD_{dB}	38 dB, 45 dB
$2N_t$	3800 sub-carriers
P_{in}	+6 dBm

Using (4), integrated power in the desired channel (P_{desired}), the residual integrated power due to the $N+1$ channel ($P_{\text{res},N+1}$), and the residual integrated power due to all the undesired channels ($P_{\text{res,Total}}$) are evaluated as indicated in Fig. 6.6. To quantify the component of the ADC DR required to accommodate the $N+1$ channel residual power and total residual power, we evaluate

$$ResidualDR_{N+1} = 10\log_{10}\left(\frac{P_{\text{desired}}+P_{\text{res},N+1}}{P_{\text{desired}}}\right) = 10\log_{10}\left(1+\frac{P_{\text{res},N+1}}{P_{\text{desired}}}\right). \quad (6.5)$$

$$ResidualDR_{\text{total}} = 10\log_{10}\left(\frac{P_{\text{desired}}+P_{\text{res,Total}}}{P_{\text{desired}}}\right) = 10\log_{10}\left(1+\frac{P_{\text{res,Total}}}{P_{\text{desired}}}\right). \quad (6.6)$$

We find $ResidualDR_{\text{total}}$ and $ResidualDR_{N+1}$ for Butterworth and Inverse Chebyshev filters as the first adjacent channel power changes relative to the desired power (indicated by AC_{dB}). Corner frequency is set to 4 MHz for both the filters as applicable to UHF receiver example. Sub-carrier powers P_{d}, P_{N+1} and P_u are suitably adjusted to maintain fixed total input power ($P_{\text{in}} = +6$ dBm) with $UD_{\text{dB}} = 45$ dB. Values of the other parameters are indicated in Table 6.1. Figure 6.7 shows $ResidualDR_{\text{total}}$ and $ResidualDR_{N+1}$ for filters of order 3 to 8 as AC_{dB} is varied from +10 dB to +40 dB in 10 dB step size. As expected, Fig. 6.7 indicates that the residual DR requirement for the ADC ($ResidualDR_{\text{total}}$) reduces with increasing filter order.

The two important observations from Fig. 6.7 are:

1. If the undesired input power is dominated by high-frequency ($> (N+1)$) channels ($AC_{\text{dB}} = 10$ dB), then the first adjacent channel power is easily filtered

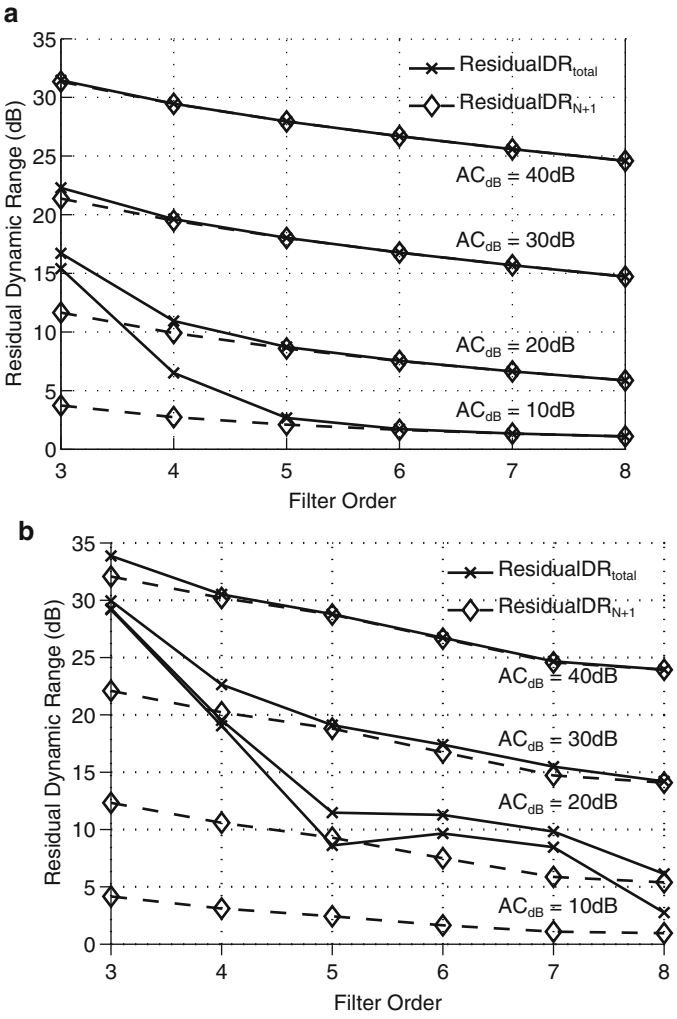


Fig. 6.7 Residual dynamic requirement for digital adjacent channels with (**a**) Butterworth filter (**b**) Inverse Chebyshev filter

by both Butterworth and Inverse Chebyshev filters. In this case, lower order Butterworth filters (3–5) are quite effective compared to Inverse Chebyshev filters.

2. If the undesired input power is dominated by the $(N+1)$ channel ($AC_{\mathrm{dB}} = 40$ dB), then $ResidualDR_{\mathrm{total}} \approx ResidualDR_{N+1}$. In this case, both Butterworth and Inverse Chebyshev filters have comparable $ResidualDR_{\mathrm{total}}$ requirement from the ADC.

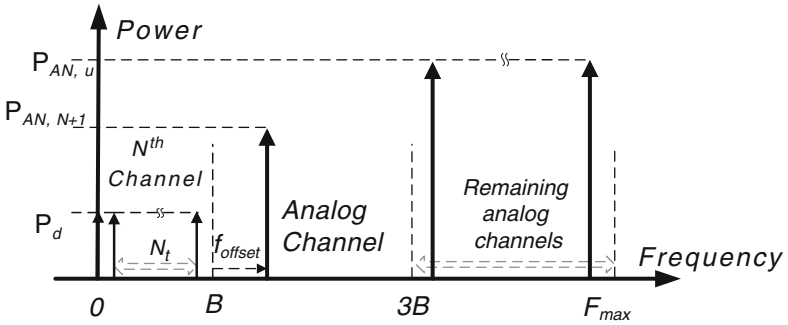


Fig. 6.8 Analog adjacent channels with single analog carrier per channel

6.2.2.2 Residual Undesired Power from Analog Adjacent Channels

Compared to digital channels, analog channels use two narrow band carriers (one for video and one for audio) located within the channel bandwidth. The video carrier is 13 dB higher than the audio carrier and is located closer to the pass band edge [2]. Hence, a single worst-case carrier at f_{offset} from the edge of the channel is modeled as shown in Fig. 6.8. For fair comparison, the input power of the single carrier is set equal to the integrated power from the undesired digital channel. As indicated in Fig. 6.8, the power of the analog carrier in the $(N+1)$ adjacent channel and remaining channels is

$$P_{AN,N+1} = P_{N+1}(2N_t) \tag{6.7}$$

$$P_{AN,u} = P_u(2N_t). \tag{6.8}$$

Similar to the previous analysis, AC_{dB} measures the difference in the desired and undesired first adjacent channel input power. As the $ResidualDR_{\text{total}}$ requirement for worst case high AC_{dB} values is dominated by $ResidualDR_{N+1}$, the difference in the performance of the two filters is highlighted with $ResidualDR_{N+1}$. For $f_{offset} = 1.25MHz$, $ResidualDR_{N+1}$ for Butterworth and Inverse Chebyshev filters are evaluated and the results are shown in Fig. 6.9. The key observations are:

1. For lower filter orders (3 to 5), both Butterworth and Inverse Chebyshev filters provide similar attenuation for the adjacent analog channel leading to comparable $ResidualDR_{total}$ requirement from the ADC.
2. For higher order Inverse Chebyshev filters (7 and 8), the $ResidualDR_{N+1}$ is 12dB lower than that for Butterworth filters. This improvement results from the sharp transition band and nulls in the transfer function due to stop-band $j\omega$-axis zeros in the Inverse Chebyshev approximation.

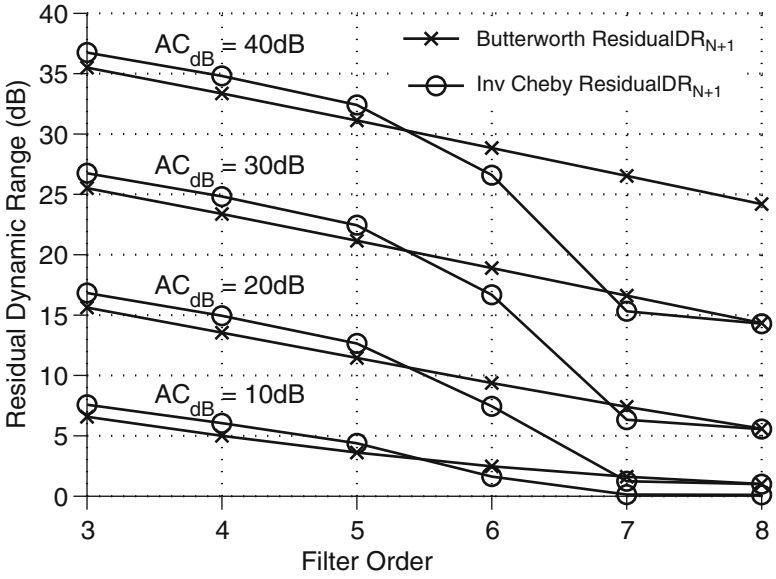


Fig. 6.9 Residual dynamic range for the analog adjacent channel

In summary: (1) Low order Butterworth filters are more efficient at reducing the undesired blocker power when it is dominated by far out blockers ($> N+1$) for both digital and analog modulation; (2) Butterworth and Inverse Chebyshev filters provide comparable performance when the residual power is dominated by the $(N+1)$ channel with digital modulation; and (3) Higher order Inverse Chebyshev filters (orders 7 to 8) are favorable than Butterworth filters when the residual power is dominated by the $(N+1)$ channel with analog modulation.

The drop in the required ADC DR due to filtering translates to reduction in ADC power consumption. ADC power consumption has a strong structural dependency [9]. According to [10], the power efficiency of the ADC for a given SNDR can be predicted using power per conversion bandwidth (P/f_{sig}) metric. Published ADC data indicates that P/f_{sig} increases approximately at $2X$ per additional bit but may approach $4X$ per additional bit for noise limited high DR ADCs [10, 11]. Based on the survey in [11], we estimate the power consumption of a 4 MHz signal bandwidth ADC as shown in Fig. 6.10. This estimation shows that drop in ADC power consumption due to filtering depends on the targeted SNDR and filtering can result in significant ADC power saving for high SNDR ranges. Low order Butterworth filters fare better than low-order Inverse Chebyshev filters if the undesired power is dominated by far out blockers. But in the presence of a strong $(N+1)$ blocker, high order Inverse Chebyshev filters have either similar(digital blocker) or better (analog blocker) performance than Butterworth approximation of the same order. As quantified by the previous analysis, Inverse Chebyshev filters offer up to $+12$ dB additional ADC DR reduction in the presence of strong analog adjacent blockers.

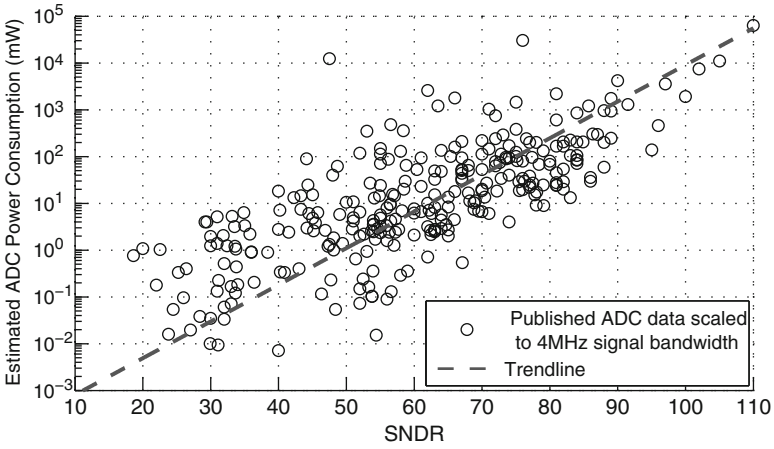


Fig. 6.10 Estimated ADC Power consumption (for 4 MHz signal bandwidth) based on the data in [11]

Hence for the UHF receiver example case, to tolerate the presence of strong $(N+1)$ adjacent channels (both analog and digital), Inverse Chebyshev approximation is selected for implementation as detailed in the following section.

6.3 Circuit Implementation

Building block specifications for the UHF receiver and the analog baseband can be obtained using the cascaded noise figure and IIP3 equations [12, 13]. For the analog baseband, the input referred noise should be $< 31nV/\sqrt{Hz}$ over a 4 MHz bandwidth, which translates to -73 dBm (using a 75Ω reference). The RF front-end includes a variable gain LNA and a passive mixer for I/Q demodulation with a $+18$dB gain. The RF take over point (i.e. when the LNA switches from gain to attenuation) is set to -20 dBm at the output of the LNA. This condition sets the blocker tolerance requirement and hence the out-band IIP3 of the analog baseband should be over 33 dBm to tolerate two input blockers at -2 dBm each.

Also, based on the analysis in the previous Section, an Inverse Chebyshev approximation is chosen for the 4 MHz bandwidth filter to provide >29 dB attenuation at 5.25 MHz for the implementation. This results in an 8^{th}-order approximation with pole-zero locations as indicated in Table 6.2.

Excellent linearity performance of active RC filters makes them suitable for broadband receivers [14–20]. However, the accuracy of pole-zero ratios limits roll-off sharpness, and process variations limit the absolute accuracy in active RC filters unless an automatic tuning scheme is employed. The complexity of the filter tuning scheme to mitigate this variation depends on the desired precision. In contrast,

Table 6.2 Pole-zero placement for baseband inverse chebyshev approximation

Complex pole pairs (MHz)	Complex zero pairs (MHz)	Realization
4.05/5.40, $Q = 0.71$	21.89/29.19	Active RC (Zero not realized)
4.66/6.21, $Q = 0.52$	7.69/10.25	Switched capacitor
3.49/4.66, $Q = 1.23$	5.14/6.85	Switched capacitor
3.21/4.29, $Q = 3.79$	4.35/5.81	Switched capacitor

8th order Low Pass Inverse Chebyshev Approximation (3/4 MHz bandwidth setting)

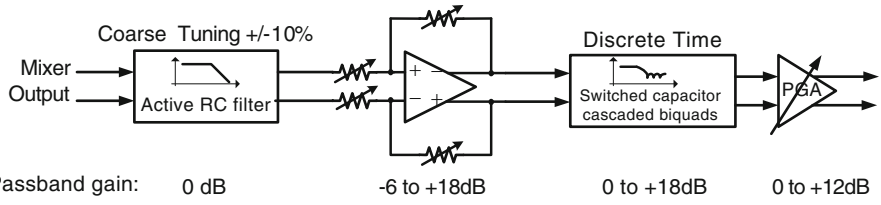


Fig. 6.11 Analog baseband architecture

switched capacitor (SC) filters can implement precise transfer functions without tuning but require anti-alias filtering. A 700 kHz SC filter for channel selection using an anti-alias filter with $>2X$ larger bandwidth (1.5 MHz) has been reported in [21]. A solution that implements an SC ladder filter with embedded anti-aliasing has been reported previously [22]. The required frequency and gain programmability of the baseband filter in this work precludes the use of such hybrid ladder architecture.

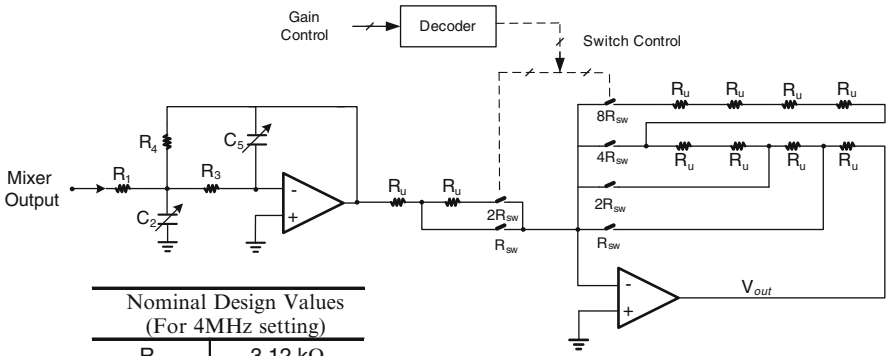
6.3.1 Cascaded Hybrid Baseband Architecture

The hybrid active RC and SC filter with built-in anti-aliasing shown in Fig. 6.11 is suitable for realizing cascaded transfer functions. The desired Inverse Chebyshev approximation is realized as a cascaded function of 4 biquad stages [23, 24]. Each biquad transfer function is given by

$$H_i(s) = K_i \frac{1 + \left(\frac{s}{\omega_{z,i}}\right)^2}{1 + \left(\frac{s}{\omega_{p,i}Q_{p,i}}\right) + \left(\frac{s}{\omega_{p,i}}\right)^2}, \tag{6.9}$$

where K_i is the DC gain, $\omega_{p,i}$ is the location of the complex pole-pair with quality factor Q_i, and $\omega_{z,i}$ is the location of the $j\omega$-axis zero pair. The required anti-aliasing transfer function is realized using a part of the Inverse Chebyshev approximation. Thus, the overall filter transfer function is

$$H(s) = H_1'(s)H_2(s)H_3(s)H_4(s), \tag{6.10}$$



Nominal Design Values (For 4MHz setting)	
R_1	3.12 kΩ
C_5,C_2	7.8pF, 35.1 pF
R_4, R_3	3125 , 781Ω
m= (R_3/R_1)	0.25
n = (C_2/C_5)	4.5

Nominal Design Values	
R_u	732Ω
R_{sw}	2.5V NMOS device 4(6.4μm/0.32μm)

Fig. 6.12 Active RC multi-feedback-filter and programmable gain amplifier (single-ended structure shown)

where $H_2(s)$, $H_3(s)$, and $H_4(s)$ are realized with SC filters while $H_1^{'}(s)$ is approximated from $H_1(s)$ by ignoring the highest zero pair from the Inverse Chebyshev approximation (29 MHz in Table 6.2) to provide anti-aliasing. The cascaded SC biquads implement precise stop-band zeros to provide accurate transition band positioning.

6.3.2 Active RC Implementation

Single-opamp multi-feedback (MFB) filter structure shown in Fig. 6.12 is used to implement $H_1^{'}(s)$. This structure has the advantages of low sensitivity (to Q and ω_o variations) as well as low power consumption. The transfer function of the filter is given by

$$H_1^{'}(s) = \frac{K_1}{1 + \left(\frac{s}{\omega_p Q_p}\right) + \left(\frac{s}{\omega_p}\right)^2} \tag{6.11}$$

where

$$K_1 = \frac{R_4}{R_1};\ \omega_p = \frac{1}{RC\sqrt{mn}};\ Q_p = \frac{\sqrt{n}}{\left(2\sqrt{m} + \sqrt{\frac{1}{m}}\right)} \tag{6.12}$$

with $K_1 = 1$, $R_1 = R_4 = R$, resistor ratio $m = \frac{R_3}{R_1}$ and a capacitor ratio $n = \frac{C_2}{C_5}$. For a given Q_p, m and n are interdependent and thus cannot be set independently. The output spot noise spectral density for the filter is

$$v_{\text{on}}^2 = 16\,\text{kTR}\left|\frac{1}{1+\left(\frac{s}{\omega_p Q_p}\right)+\left(\frac{s}{\omega_p}\right)^2}\right|^2 + 8\,\text{kTmR}\left|\frac{2\left(1+\left(\frac{s}{2\omega_p}\sqrt{\frac{n}{m}}\right)\right)}{1+\left(\frac{s}{\omega_p Q_p}\right)+\left(\frac{s}{\omega_p}\right)^2}\right|^2 + v_{\text{amp}}^2\left|\frac{2\left(1+\left(\frac{s}{\omega_z Q_z}\right)+\left(\frac{s}{\omega_z}\right)^2\right)}{1+\left(\frac{s}{\omega_p Q_p}\right)+\left(\frac{s}{\omega_p}\right)^2}\right|^2, \tag{6.13}$$

where v_{amp}^2 is the input referred noise density of the amplifier. The first term represents the noise contribution from R_1 and R_4; the second term represents the noise contribution from $R_3 = mR$; and the third term represents the noise contribution from the amplifier. Parameters ω_z and Q_z are

$$\omega_z = \omega_p\sqrt{2};\; Q_z = \frac{\sqrt{2mn}}{(2m+n+1)}. \tag{6.14}$$

For a fully differential filter, the total capacitance is $C_{\text{total}} = \frac{C_2}{2} + 2C_5 = (\frac{n}{2}+2)C$. For a given C_{total}, depending on the choice of m (and hence n as set by Q_p), the integrated noise is plotted in Fig. 6.13. The optimum range of resistor ratio m for reducing the noise for a given capacitance budget is in the range 0.2–0.4. Hence, we choose $m = 0.25$ (resulting in $n = 4.54$) and size the capacitors accordingly to meet the noise figure requirement. Programmable capacitors C_2 and C_5 (cf. Fig. 6.12) are adjusted using digital control bits to implement 3 and 4 MHz bandwidth settings in the filter.

The filter linearity requirement ($IIP3 > 33$ dBm) sets the minimum loop-gain in the filter passband to suppress distortion adequately. The minimum loop-gain and hence, the gain-bandwidth (GBW) of the amplifier is obtained using simulations and thus, we designed a two-stage Miller amplifier with 160 MHz GBW. The amplifier consumes 2.15 mA from a 1.8 V supply.

The input resistor R_1 (3.12 kΩ) is split into two 1.56 kΩ resistors with an additional shunt-capacitance (single-ended $10pF$) resulting in 3rd order filter to further enhance the anti-aliasing and rejection of far-out blockers. For a fully differential implementation (floating $5pF$), the additional capacitance simply provides a low impedance return path and recirculates the high frequency blocker power, improving the blocker tolerance and relaxing the out-band linearity requirements of the subsequent filter stages. The additional capacitance also limits the noise bandwidth and hence the integrated output noise contribution from the input resistor R_1.

A continuous time programmable gain amplifier (PGA) with a gain range of (-6 to $+18$ dB) follows the MFB filter. The PGA resistors are sized to minimize the

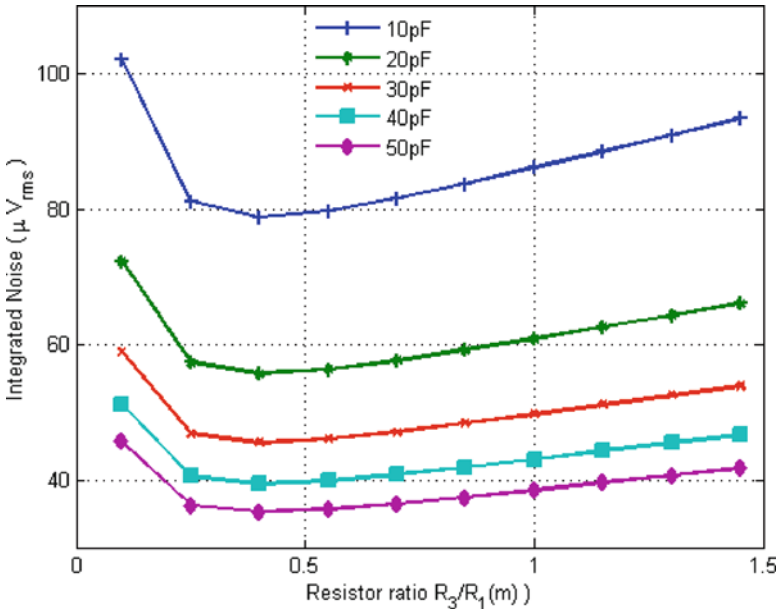


Fig. 6.13 Variation of integrated noise for a given total capacitance budget with varying resistor ratio

input-referred noise of the PGA in the maximum gain setting. The switches and resistor arrays are ratioed proportionately to keep the gain of the PGA independent of switch size to the first order. The PGA provides a low closed-loop output impedance to drive the subsequent SC filter.

6.3.2.1 SC Implementation

Three cascaded SC biquads implement the transfer functions $H_2(s)$, $H_3(s)$, and $H_4(s)$. Each biquad is a two integrator loop implemented using operational transconductor amplifiers (OTA) as shown in Fig. 6.14. The preceding PGA allows to relax the input-referred noise density of the SC section in the maximum gain setting. For a sampling frequency of 80 MHz ($T_s = \frac{1}{f_s} = 12.5$ ns), 1 ns is budgeted for slew rate effects, 1 ns for switch resistance delay, and 0.9 ns for the non-overlapping time, yielding a $T_{\text{linear}-\text{settling}}$ on the order of 3.35 ns [25].

The desired open-loop GBW ($f_{u,i}$ Hz) of each OTA is designed for 0.5% settling (6τ). Programmable capacitor arrays (C_1, C_3 and C_6 in Fig. 6.14) are used in the biquads to achieve accurate gain (0 or 6 dB) and frequency programming (3 or 4 MHz). Computation of the required capacitor ratios and OTA GBW account for dynamic range node scaling and noise estimation. The noise constraint ($k_B T/C$) determines the unit capacitor size, which in turn sets the power consumption of each

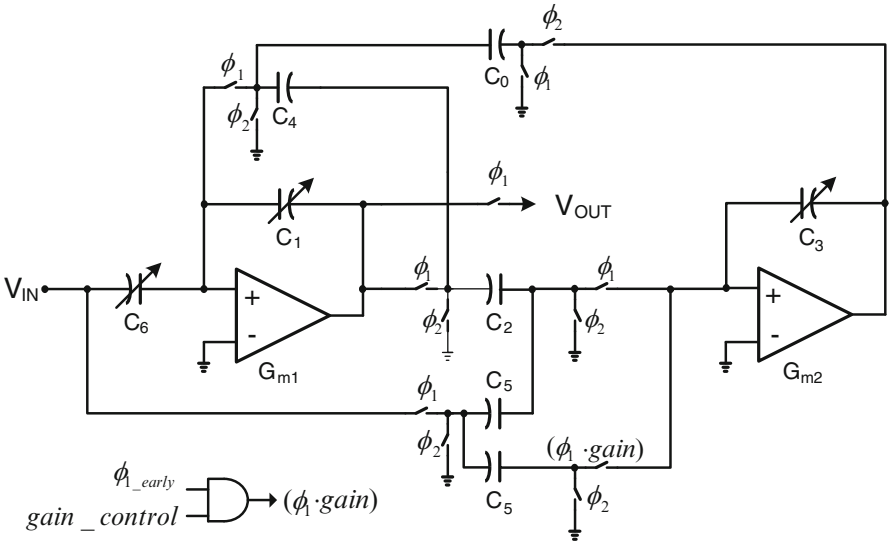


Fig. 6.14 Switched-capacitor biquad implementation (single-ended structure shown)

OTA for a desired f_u. We selected $C_{\text{unit}} = 113fF$ (minimum value imposed by the process), which results in a cascaded input referred noise density $<100nV/\sqrt{Hz}$ for the SC sections in the maximum gain setting. Fully differential, folded cascode transconductors (PMOS input) with switched capacitor common-mode feedback are used for the OTAs. Including the biasing circuits, the three biquads consume 6.3, 7.7, and 6.7 mA from a 1.8 V supply. The input referred noise density requirement for second and third biquads can be reduced allowing to relax the minimum C_{unit} and the total capacitance used in the biquads. Such a power optimization will allow to reduce the power consumption of later stages of filter. In this work, the process imposed constraint of minimum $C_{\text{unit}} = 113fF$, prevented such optimization. The switches are implemented with 2.5 V NMOS devices to provide headroom for the signal swing. Hence the digital clocking circuits to drive the switches are implemented using a 2.5 V digital supply.

The active RC section provides 24 dB variable gain and a 3rd order filter response with an attenuation of 4 dB at 5.25 MHz. With the additional SC filter (6th order), this attenuation increases to 29 dB (42 dB) at 5.25 MHz (5.75 MHz) with an additional 18dB variable gain. This improved attenuation and variable gain consumes 37.3 mW (limited by the high C_{unit} of the technology in this design). The passband group delay resulting from filter response adds to the total wireless channel delay which is time-variant and has to be compensated by the adaptive channel equalizer in the digital demodulator. Frequency dependent gain and phase mismatch between I/Q branches causes sub-carrier dependent errors within the bandwidth, but can be reduced at the system-level using digital compensation techniques [26].

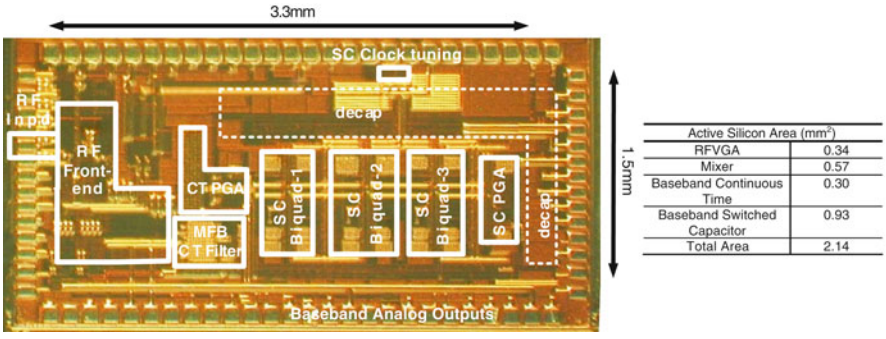
6.4 Experimental Results

The analog baseband was integrated and fabricated as part of a UHF receiver along with an RF front-end using the IBM 0.18 µm RFCMOS technology. Figure 6.15 shows the chip micrograph. Only one baseband signal path was realized (out of I and Q) in the prototype due to area constraints; however, analog performance verification only requires testing of one channel. The system occupies 2.14 mm^2 of active area and was characterized in a QFN80 package.

6.4.1 Baseband Response and Residual DR Measurements

The measured baseband transfer functions are shown in Fig. 6.16. Figure 6.16a shows the frequency (3 and 4 MHz) and gain programmability (−6 dB to +18 dB with 6 dB per step) of the continuous time section. Figure 6.16b shows frequency programmability of the composite hybrid filter (3 and 4 MHz options) along with the additional gain programmability of the SC section (0 to +18 dB range with 0 or 6 dB per biquad). For the 4 MHz setting, the measured frequency response indicates a stopband attenuation of >29 dB for frequencies >5.25 MHz, while the continuous time filter provides >2.8 dB attenuation at the same frequency.

To measure the *ResidualDR*, input power spread over two channels (generated using two signal generators and a power combiner) is injected into the filter. A digital channel is generated using 64-QAM modulation employing Root-Nyquist (RNYQ) pulse shape with appropriately scaled symbol rate to generate a flat PSD through-out the channel, while an analog channel is generated using a single carrier. The output power levels between the desired and the undesired channels is suitably adjusted to vary the AC_{dB} values to obtain a wide range of measurements. Filtered PSD is measured at both the continuous- and discrete-time outputs. Figure 6.17 shows the measured input and filtered outputs with digitally modulated desired



Active Silicon Area (mm^2)	
RFVGA	0.34
Mixer	0.57
Baseband Continuous Time	0.30
Baseband Switched Capacitor	0.93
Total Area	2.14

Fig. 6.15 Chip Micrograph of the UHF receiver

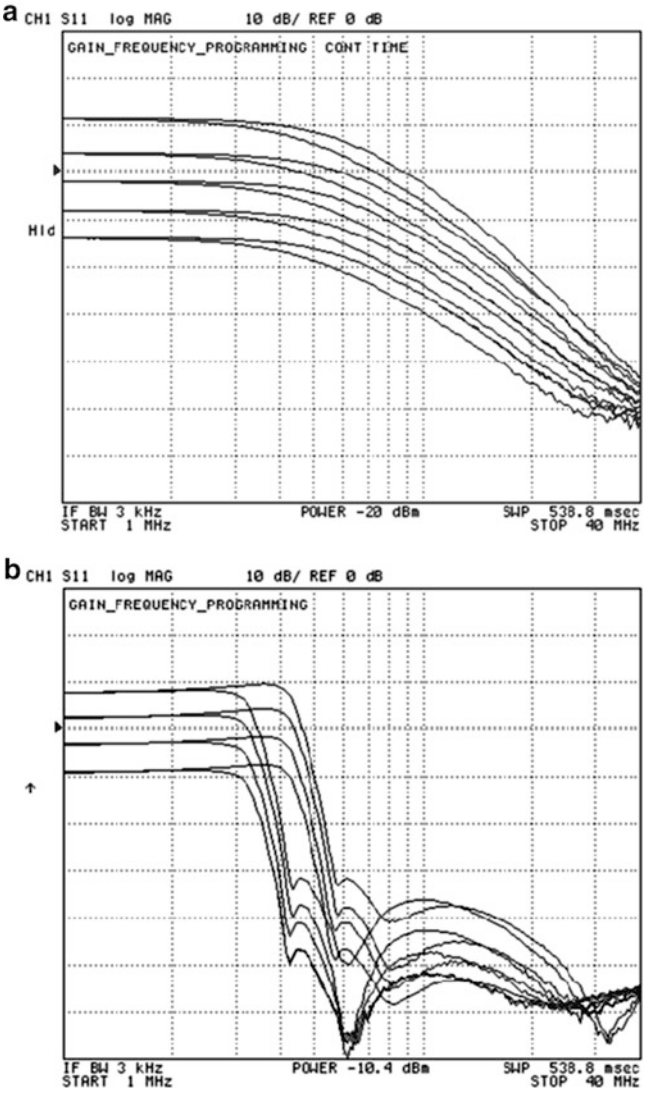


Fig. 6.16 Measured baseband transfer function (**a**) continuous-time section (**b**) continuous- and discrete-time sections together

and $N+1$ adjacent channel with $AC_{\mathrm{dB}} = 30\,\mathrm{dB}$. The PSD shows attenuation below 1 MHz due to the frequency limitation from the power combiner. Table 6.3 indicates the computed *ResidualDR* from measurements for near digital and analog blocker ($N+1$ channel) and far out digital blocker ($N+3$ channel) for varying AC_{dB} values. The filtered PSD at the hybrid filter output for the $N+3$ channel is below the output noise floor for AC_{dB} values of 10 and 20 dB. The hybrid filter reduces the

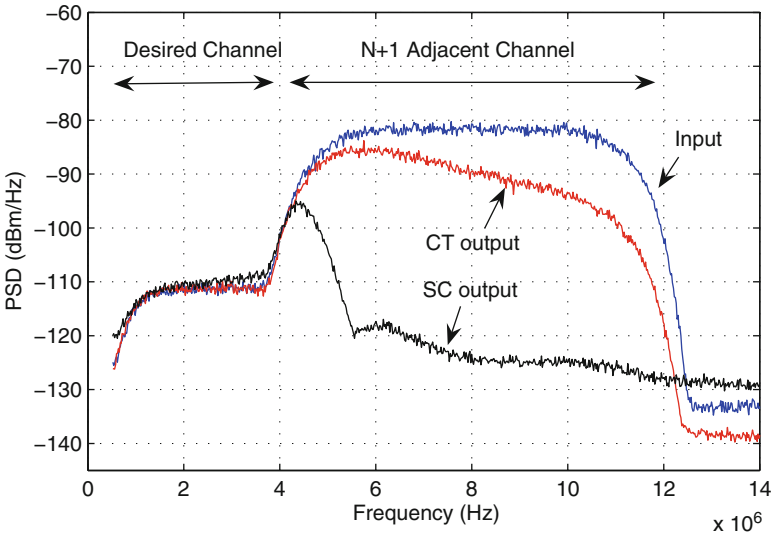


Fig. 6.17 Measured filtered output PSD with combined input of two 64-QAM digital modulated channels (desired and N+1 adjacent) with $AC_{\text{dB}} = 30\,\text{dB}$

Table 6.3 Measured *ResidualDR* with *near* $(N+1)$ and *far* $(N+3)$ blockers

	Continuous-time filter (dB)				Hybrid filter (dB)			
Blocker Profile with AC_{dB}[a] ⇒	10	20	30	**40**	10	20	30	**40**
Digital $(N+1)$ channel	7.5	16.5	26.4	**34.5**	1.3	2.9	8.8	**17.0**
Analog $(N+1)$ channel	10.6	20.2	30.2	**40.2**	0.15	1.3	6.3	**15.3**
Digital $(N+3)$ channel	0.53	0.84	3.12	**9.83**	–	–	0.45	**0.51**

[a]By definition, equivalent integrated power of the $(N+1)$ channel is $(AC+3)_{\text{dB}}$ higher than the integrated power of the desired channel due to $2X$ integrating bandwidth of $(N+1)$ channel

$ResidualDR_{N+1}$ by $+17.5\,\text{dB}$ ($\approx$3 bits using $N_{\text{bits}} = (\text{DR} - 1.76)/6.02$) for digital $N+1$ channel and $+24.9\,\text{dB}$ ($\approx$4 bits) for analog $N+1$ channel. Improvement in $ResidualDR_{N+1}$ is better in the presence of analog adjacent channel for the hybrid filter as predicted by the analysis in Sect. 6.2.2.

6.4.2 System Performance

Table 6.4 summarizes the experimental results of the UHF receiver and compares the entire receiver to published UHF receivers. The system linearity and noise measurement results reflect the performance of the receiver including the analog baseband. To obtain the out-band linearity performance, two out-of-channel RF tones located at $N+2$ (516 MHz) and $N+4$ (531 MHz) are injected at the LNA input, and the in-band distortion tone located at 1 MHz at the baseband filter output

Table 6.4 Experimental results with comparison to previous work

	This Work	[14]	[15]	[16]	[17]	[18]	[20]
Frequency range (MHz)	470–862	470–862	470–862 1670–1675	470–890 1400–1800	470–890 1670–1675	470–850	470–862 1670–1675
RFVGA gain range (dB)	29.2 (15.2 to −14)	40	35	>50	20	Not Available (N.A.)	40
Channel bandwidth (MHz)	6/8	8	7/8	6/7/8	4 to 10	5/6/7/8	2–5
Maximum gain (dB)	>80	75	85	94 to 100	86	95	95
Overall AGC range (dB)	>75	75	65	>98	80	95	103.5
NF at Max gain (dB)	7.9	8.5	3.6	3.1 to 4.6	3.5/4	4.5/5	3.7/4.3
IIP3 at Max gain (dBm)	−8	N.A.	N.A.	−13	N.A.	N.A.	−13
IIP3 (dBm)	+2 at 9 dB RF attn	+12 at 20 dB RF attn[a]	+4 at 20 dB RF attn	−6.8 at 8 dB RF attn	−9/−3/0.5 at 0/6/10 dB RF attn	−5/−6 at 64 dB system gain	+5 at 15 dB RF attn
Power consumption	120 mW (182 mW[b]) at 1.8 V analog and 2.5 V digital supply	240 mW at 2.78 V	340 mW at 2.7 V	184 mW at 2.8 V	295 mW at 2.8 V	184/207 mW at 2.8 V	114 mW at 1.2 V
Die Size (mm^2)	2.14[c]	11.5	12.25	16	9.7	7.8	7.2
Technology	CMOS 0.18 µm	SiGe 0.35µm	SiGe 0.35µm	SiGe 0.5µm	CMOS 0.18µm	CMOS 0.18µm	CMOS 0.13µm

[a] Measured with an external LNA of 10 dB gain
[b] Includes estimated additional power for Q-baseband channel
[c] Does not include the area for Frequency synthesizer and Q-baseband channel

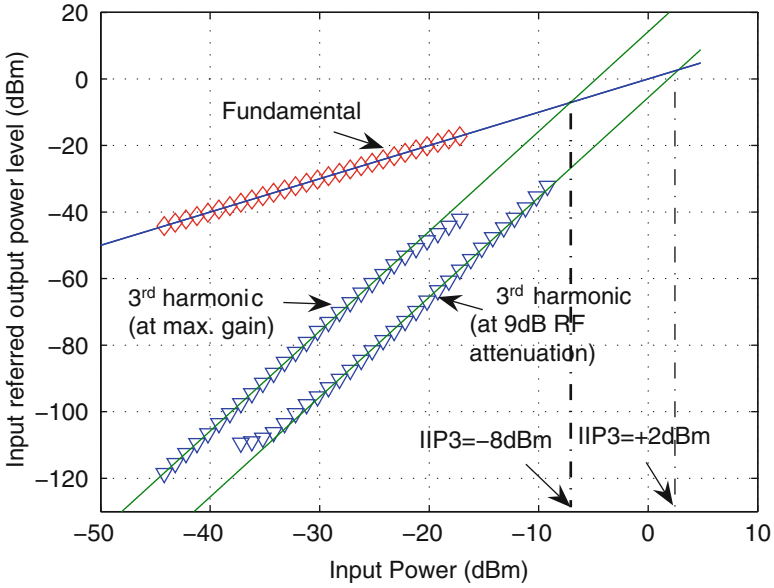


Fig. 6.18 Measured linearity performance using two-tone measurement results for the system

after down conversion was measured. The system IIP3 is −8 and +2 dBm for the highest gain and 9 dB RF attenuation cases, respectively as indicated in Fig. 6.18. Also, the 3rd order harmonic saturation is measured at −23 dBm for the highest gain setting but is not detected for 9 dB RF attenuation showing better linearity performance.

The power consumption and the area metrics indicated for this work in Table 6.4 do not include the frequency synthesizer, and quadrature generator. The RF front end and baseband blocks consume 58 and 52 mW from a 1.8 V supply respectively. The digital clock tree to drive the SC filter switches consumes 10 mW from a 2.5 V digital supply. Compared to the previously published UHF receiver solutions, this work implemented in CMOS process offers competitive performance.

6.5 Conclusion

Impact of blockers on analog baseband filter design in wireless receivers has been addressed in this chapter. Analog baseband design for an UHF receiver served as an example to illustrate the concepts. Analog baseband filters for wireless receivers must exhibit excellent out-of-band linearity performance and blocker tolerance. In addition, the analysis presented in Sect. 6.2 systematically evaluates the dynamic range requirements based on the blocker type (analog/digital), relative strength

(based on UD_{dB}), and spectral location (*near* or *far*). Analysis concludes that (1) for digital modulated channels, the majority of the undesired residual power after filtering resides in the first adjacent channel, and (2) In the presence of narrow band analog adjacent channel, high order Inverse Chebyshev filters are favorable for baseband filter implementations compared to Butterworth approximations. An implementation of the filter using a hybrid combination of continuous-time and switched-capacitor techniques is demonstrated.

Acknowledgements The authors would like to recognize that the UHF receiver was developed in collaboration with Dr. Jianhong Xiao, Jusung Kim, and Hyung-Joon Jeon. The authors would like to thank the MOSIS educational research program and IBM Corp. for chip fabrication.

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Chapter 7
Flexible Nanometer CMOS Low-Noise Amplifiers for the Next-Generation Software-Defined-Radio Mobile Systems

Edwin C. Becerra-Alvarez, F. Sandoval-Ibarra, and J.M. de la Rosa

7.1 Introduction

The increasing number of personal wireless applications demands for Radio Frequency (RF) front-ends capable to handle different standard specifications, signal conditions and battery status [1]. The trend is towards a maximum hardware reuse, by making as many transceiver building blocks as possible, digitally programmable, reconfigurable and compatible with mainstream nanometer CMOS technologies [2].

Among other RF circuits, the design of the LNA is specially critical, due to its early position at the very beginning of the receiver chain, that makes this block a determinant factor in the overall system performance. The LNA has to simultaneously match the antenna and to amplify weak input signals with reduced noise contribution, high linearity and isolation from the rest of the receiver chain. This problem is aggravated in the case of multi-standard applications, in which LNAs must operate over different frequency ranges, whereas keeping reduced number of passive circuit elements to increase integration [1].

The majority of multi-standard LNAs are based on the use of switchable passive networks to select the resonance frequency, thus preserving immunity to out-of-band interferers, although only one signal band is received at one time [3, 4]. Besides,

E.C. Becerra-Alvarez
IMSE-CNM, CSIC/University of Seville, Seville, Spain

CUCEI, University of Guadalajara, Guadalajara, Mexico
e-mail: edwin.becerra@cucei.udg.mx

F. Sandoval-Ibarra
Cinvestav-Unidad Guadalajara, Guadalajara, Mexico
e-mail: sandoval@gdl.cinvestav.mx

J.M. de la Rosa (✉)
IMSE-CNM, CSIC/University of Seville, Seville, Spain
e-mail: jrosa@imse-cnm.csic.es

E. Tlelo-Cuautle (ed.), *Integrated Circuits for Analog Signal Processing*,
DOI 10.1007/978-1-4614-1383-7_7,

the use of switches forces a discrete frequency selection and introduces parasitic switch-on resistances and capacitances, with the subsequent trade-off between linearity, noise and speed. This limitation can be partially solved by using concurrent multi-band LNAs [5, 6] which allows a simultaneous reception of multiple signal bands without using switches. However, the spurs in one band may corrupt signals in the other band due to the LNA non-linear operation.

A common issue in most reported multi-standard LNAs is the increase of the number of integrated passive elements (basically capacitors and inductors) as compared to their mono-standard counterparts, not offering a clear advantage with respect to using separate mono-standard LNAs [1,2]. Moreover, most circuit topologies are based on stacked amplifiers (usually simple cascode) in either common-source or common-gate configuration, which are not very suited for low-voltage operation. Recently, the used of folded-cascode topology has been applied to the design of LNAs, although very little has been done for multi-standard applications [7].

The work in this chapter contributes to this topic and presents the practical design and implementation of a continuously reconfigurable LNA integrated in a 90-nm CMOS technology. The circuit employs a topology which is based on MOS-varactor tuning networks to make the resonance frequency continuously programmable without needing any RF switches. The resulting circuit adapts its performance to the requirements of different wireless standards without increasing the number of inductors as compared to conventional mono-standard LNAs (considering that they are tested as stand-alone circuits). Layout-extracted simulations and experimental measurements are shown to validate the presented approach.

7.2 Background on Reconfigurable CMOS LNAs

The LNA is one of the most important building blocks in RF transceivers. Its design becomes specially critical due to its early position in the receiver chain—connected just after the antenna and the RF filter. Therefore, LNA circuits have to accomplish many requirements, namely: antenna's filter coupling for the input signal, enough gain for weak signals, low noise performance, high linearity as well as a proper isolation with respect to the rest of receiver building blocks [8]. All these requirements become more demanding in multi-standard applications, where LNAs must handle a number of different specifications within a widely programmable frequency range, while keeping an adaptive power consumption and reduced number of passive elements in order to minimize the effective area, and hence the final product cost [9].

7.2.1 Switchable Resonant Tank

As stated in the Introduction, a number of circuit techniques have been reported in the last few years to implement multi-standard CMOS LNAs [3–6, 10–16]. Some of

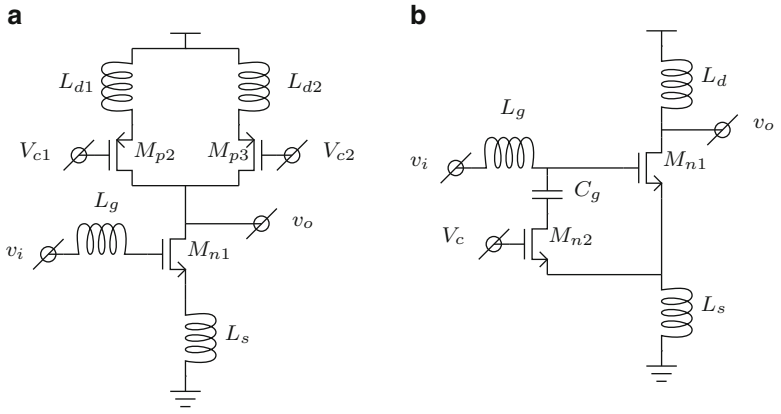

Fig. 7.1 Multi-standard LNA: (**a**) Based on switchable resonant tank [11] and (**b**) With an external switchable capacitor

them are based on the use of a switchable passive network, as shown in Fig. 7.1a, to select the resonance frequency, thus preserving immunity to out-of-band interferers, although only one signal band is received at one time [3, 4, 10, 11]. Besides, the use of switches forces a discrete frequency selection and introduces parasitic switch-on resistances and capacitances, with the subsequent trade-off between noise and speed. Thus, if a low switch-on resistance is used, the size of transistors implementing the switches—M_{p2} and M_{p3} in Fig. 7.1a—must be enlarged, thus increasing the associated parasitic capacitances, whereas small switches lead to high switch-on resistances, with the subsequent NF degradation.

Assuming that inductors L_g and L_s are ideal, the input impedance of the LNA in Fig. 7.1a is approximately given by:

$$Z_{in\mathrm{SI}} \approx \left(\frac{g_{mn1}}{C_{gsn1}}\right) L_s + \frac{1}{sC_{gsn1}} + sL_{gs} \tag{7.1}$$

where $L_{gs} = L_g + L_s$, g_{mn1} and C_{gsn1} are the small-signal transconductance and gate-source capacitance of M_{n1}. The real part of $Z_{in\mathrm{SI}}$, given by $g_{mn1}L_s/C_{gsn1}$, is usually chosen to be equal to the RF source resistance, R_{RF}, in the band of interest.

Note that the impedance derived from (7.1) is similar to the one obtained in the mono-standard case [17]. However, the LNA gain is degraded due to the effect of transistors M_{p2} and M_{p3}—connected to load inductors L_{d1} and L_{d2}, respectively. This can be mathematically expressed as:

$$A_{v\mathrm{SI}} \approx \frac{-g_{mn1}\left(1 + g_{mp2}sL_{dn}\right)}{\left(1 + g_{mn1}sL_s + s^2C_{gsn1}L_{gs}\right)\left(1 + s^2C_LL_{dn}g_{mp2}\right)} \tag{7.2}$$

where g_{mp2} is the small-signal transconductance of M_{p2}, L_{dn} is the selected load inductor during LNA operation—either L_{d1} or L_{d2}—and C_L is the load connected at the amplifier output.

In addition to the LNA gain degradation expressed in (7.2), the effective silicon area increases significantly with the number of targeted standards and/or operation modes because the number of load inductors in Fig. 7.1a increases as well, and these passive elements are typically the most area consuming in RF integrated circuits.

7.2.2 External Switching Capacitor

The problems associated to the area penalty in the LNA shown in Fig. 7.1a can be partially alleviated by switching capacitors instead of inductors. This technique—often referred to as external switching capacitor strategy [18]—is conceptually depicted in Fig. 7.1b. This LNA uses an external switchable capacitor, C_g, to change the overall gate-source capacitance of M_{n1} in order to operate at two different frequencies (in this example). The switch used to either connect or disconnect C_g is implemented by M_{n2} transistor.

Assuming that inductors L_d, L_g and L_s are ideal, the input impedance of the LNA in Fig. 7.1b is approximately given by:

$$Z_{i\text{EC}} \approx \left(\frac{L_s}{C_g + C_{gsn1}}\right) g_{mn1} + \frac{1}{s\left(C_g + C_{gsn1}\right)} + sL_{gs} \tag{7.3}$$

Expression (7.3) shows that capacitor C_g allows to change $Z_{i\text{EC}}$ depending on the operating state of M_{n2} transistor. As an illustration, Fig. 7.2a shows the variation of S_{11} with C_g—derived from (7.3). It can be noted how increasing C_g improves S_{11} performance at the price of reducing the resonant frequency. Therefore, there is a trade off between the resonant frequency and the input impedance matching.

On the other hand, assuming the same considerations used to calculate $Z_{i\text{EC}}$, it can be shown that the LNA gain, is approximately given by:

$$A_{v\text{EC}} \approx -\frac{g_{mn1} sL_d}{\left(1 + s^2 C_L L_d\right)\left(1 + g_{mn1} sL_s + s^2 C_g L_s + s^2 C_{gsn1} L_{gs}\right)} \tag{7.4}$$

is also degraded by C_g.

The external capacitor C_g also penalizes the noise factor, which can be approximated by the following expression:

$$F_{\text{EC}} \approx 1 + \left(\frac{\omega}{\omega_{ci}}\right)\left(\frac{1}{Q_i}\right)\left[\frac{\gamma}{\alpha} - 2|c|Q_i\sqrt{\frac{\gamma\delta}{5}} + \left(\frac{\alpha\delta}{5}\right)\left(1 + Q_i^2\right)\right] + \left(\frac{\omega^3}{\omega_{ci}}\right)\left(\frac{2C_g L_s}{Q_i}\right)\left(\frac{\gamma}{\alpha} + \frac{\alpha\delta}{5}\right) \tag{7.5}$$

where

$$\alpha = \frac{g_{mn1}}{g_{dsn1}}; \quad Q_i = \frac{1}{\omega R_{RF} C_{gsn1}}; \quad \omega_{ci} = \frac{g_{mn1}}{C_{gsn1}} \tag{7.6}$$

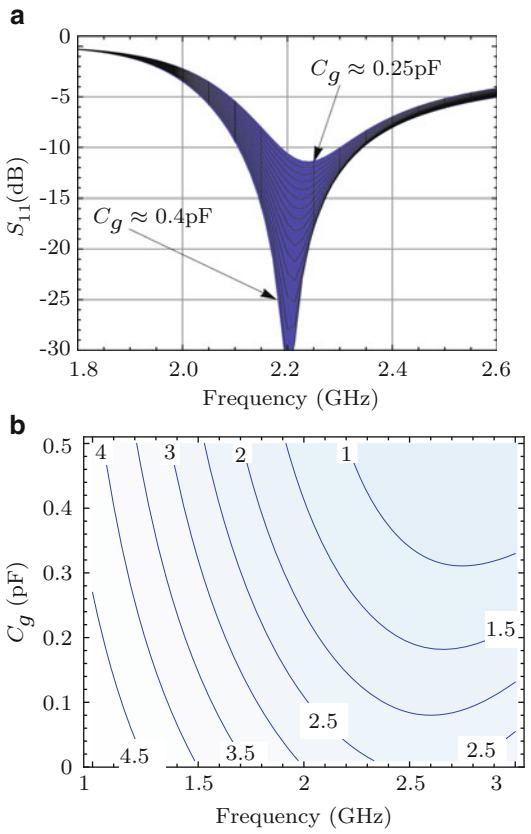

Fig. 7.2 C_g effect in a LNA with external switched capacitor for: (**a**) S_{11} and (**b**) NF

with g_{dsn1} being the small signal drain-source conductance of M_{n1}; c is the correlation factor, which has a value of $-0.395j$ and $-0.5j$ for long and short channel transistors respectively [17]; σ is a technology parameter used to model the gate noise; and γ is a technology parameter ranging from $2/3$ for long-channel transistors to 2–3 for short-channel transistors [19].

As an illustration, Fig. 7.2 shows the noise increment due to C_g, derived from (7.5). Note that there is a trade off between noise performance and the maximum frequency for a given value of C_g. For example, according to Fig. 7.2b, when noise requirement is NF $<$ 2 dB at 2 GHz, C_g must be at least 0.26 pF.

7.2.3 Multi-band LNA

The aforementioned limitations can be partially solved by using concurrent multi-band LNAs [5, 6], as illustrated in Fig. 7.3, which allows a simultaneous reception of multiple signal bands without using any switches. However, this approach has two main drawbacks. On the one hand, the spurs in one band may corrupt signals in

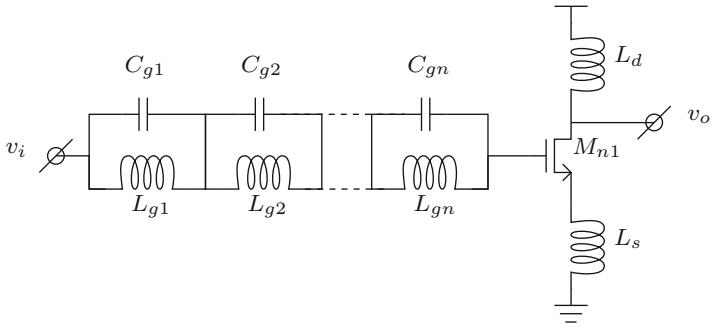

Fig. 7.3 Multi-standard LNA with multi-band matching network

other band due to the LNA non-linear operation [20]. On the other hand, the number of passive circuit elements—particularly inductors—increases significantly with the number of operation modes and wireless standards because each tuned band requires adding an additional LC network.

The LNA shown in Fig. 7.3 must match the antenna at each resonant frequency corresponding to the different operation modes. This requirement is fulfilled when a resonant frequency is generated by each LC network. Indeed, a multi-band LNA should have the same number of input signals and resonant frequencies. Assuming ideal inductors and capacitors for the LNA shown in Fig. 7.3, the input impedance for n LC networks is approximately given by:

$$Z_{in\mathrm{LC}} \approx \left(\frac{g_{mn1}}{C_{gsn1}}\right) L_s + \frac{1}{sC_{gsn1}} + sL_s + \frac{sL_{g1}}{1-\omega^2 C_{g1}L_{g1}} + \cdots + \frac{sL_{gn}}{1-\omega^2 C_{gn}L_{gn}} \tag{7.7}$$

In order to get the required resonant frequencies for the different input signals, the oscillation condition must be satisfied, yielding:

$$\frac{1}{sC_{gsn1}} + sL_s + \frac{sL_{g1}}{1-\omega^2 C_{g1}L_{g1}} + \frac{sL_{g2}}{1-\omega^2 C_{g2}L_{g2}} + \cdots + \frac{sL_{gn}}{1-\omega^2 C_{gn}L_{gn}} \approx 0 \tag{7.8}$$

Note that the complexity of (7.8) increases with the number of LC tanks, i.e. with the number of standards being processed. The simplest case is given for $n = 1$, which correspond to two resonant frequencies, with an oscillation condition given by:

$$\frac{1}{sC_{gsn1}} + sL_s + \frac{sL_{g1}}{1-\omega^2 C_{g1}L_{g1}} \approx 0 \tag{7.9}$$

Solving the above equations it can be shown that the values of C_{gs1} and L_{g1} in this case are given by:

$$C_{g1} \approx \frac{C_{gsn1}}{\left(-1+C_{gsn1}L_s\omega_1^2\right)\left(-1+C_{gsn1}L_s\omega_2^2\right)} \tag{7.10}$$

$$L_{g1} \approx \frac{\left(-1+C_{gsn1}L_s\omega_1^2\right)\left(-1+C_{gsn1}L_s\omega_2^2\right)}{C_{gsn1}^2 L_s\omega_1^2\omega_2^2} \tag{7.11}$$

where ω_1 and ω_2 stand for the resonant frequencies.

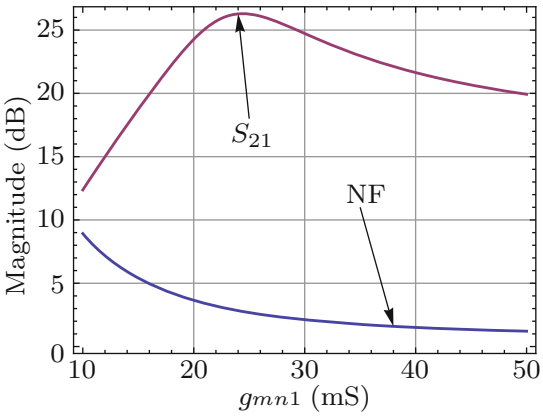

Fig. 7.4 S_{21} and NF variation due to g_{mn1} on a inductively source degenerated LNA

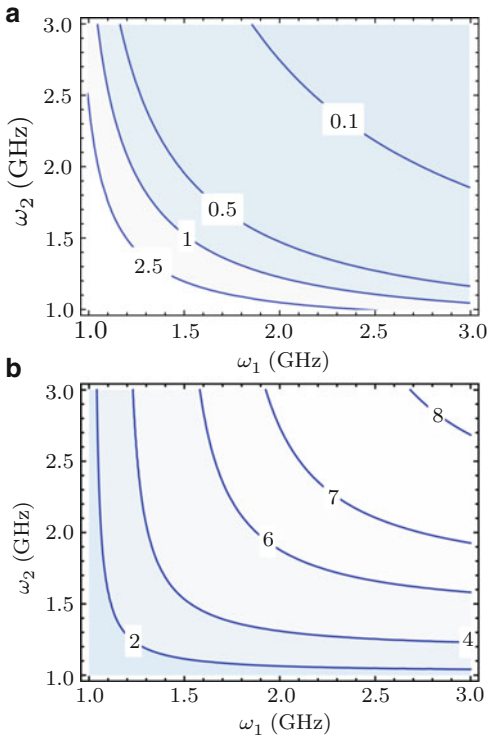

Fig. 7.5 Coupling input network sizing: (**a**) C_{g1} (pF) y (**b**) L_{g1} (nH)

The above design equations can be used to obtain the required performance in terms of NF and gain (S_{21}) for given values of the resonant frequencies. In order to illustrate the trade-off between gain and noise, Fig. 7.4 shows S_{21} and NF for different values of g_{mn1}.

The dependency of the resonant frequency with respect to C_{g1} and L_{g1} is illustrated in Fig. 7.5, where the required values of the input coupling network can

be obtained graphically. Note that there is an inverse relationship between C_{g1} and L_{g1}. For example, C_{g1} is increased when ω_1 and ω_2 becomes 1 GHz respectively—see Fig. 7.5a—and L_{g1} is reduced proportionally—see Fig. 7.5b.

7.3 Two-Stage Inductively Degenerated Common-Source LNA

This chapter presents an alternative strategy for the implementation of reconfigurable LNAs intended for multi-standard wireless applications. The principle of operation is based on using varactors to continuously tune the resonant frequency in the required bandwidth, without increasing the number of inductors as compared to the mono-standard case. An implementation of this idea will be discussed, considering the target requirements shown in Table 7.1, that covers four standards, namely: GSM, WCDMA, Bluetooth and WLAN. These requirements were obtained from experimental results reported by several ICs involving stand-alone LNAs and direct conversion receivers [12, 21–29]. Note from the data in Table 7.1 that Bluetooth has the least demanding NF requirement, which results in the lowest power consumption. On the other hand, GSM requires the minimum value of NF. In general, it should be noticed that the overall requirements for a multi-standard LNA could be more restrictive than the mono-standard case, since the same circuit can not be optimized (in terms of target specifications and power consumption) for all operation modes involved.

Figure 7.6 shows the schematic of the LNA proposed in this chapter. The circuit employs a two-stage topology to separately control the input impedance and the signal gain. A MOS-varactor tuning network is used in both stages in order to make the resonance frequency programmable without penalizing the LNA noise performance. The input stage—formed by transistors $M_{n\mathrm{NF}}$ and $M_{p\mathrm{NF1,2}}$—uses an inductively degenerated common-source structure to provide a specified real part for the input impedance and signal gain at a given frequency. The output stage is made up of transistors $M_{n\mathrm{G}}$ and $M_{p\mathrm{G1,2}}$, in order to provide higher gain without significantly degrading the noise performance. Strictly speaking, this proposal adds several properties of well-known topologies in a unique reconfigurable architecture in order to minimize power consumption, reduce integration area and low cost by making an extensive use digital signal processing.

Table 7.1 Design requirements for the inductively degenerated common-source two-stage LNA

Standard	Bandwidth (GHz)	NF (dB)	S_{21} (dB)	IIP3 (dBm)
GSM (PCS 1900)	1.85–1.99	4.2	11.5	−7.0
WCDMA (Band I)	1.92–2.17	3.2	14.0	−21.0
Bluetooth	2.40–2.48	4.7	12.5	−3.5
WLAN (b/g)	2.40–2.48	4.5	15.5	−5.4

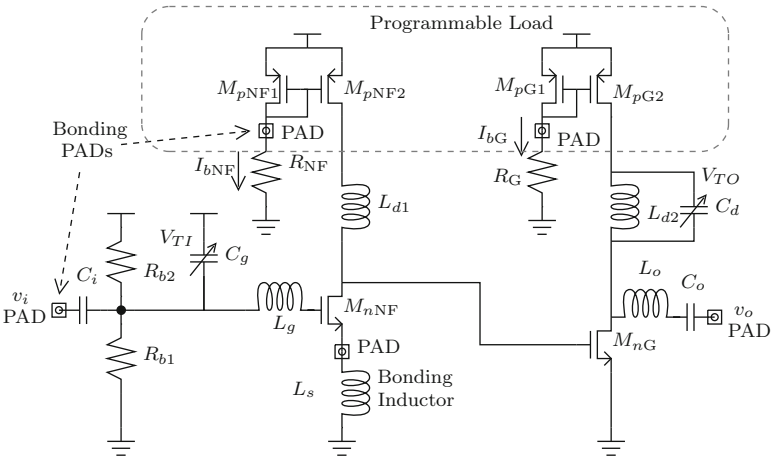

Fig. 7.6 Inductively degenerated common-source two-stage LNA

An active load formed by $M_{p\text{NF1,2}}$ and $M_{p\text{G1,2}}$ transistors is used to provide a way to control voltage gain on each stage. Although, it is very common on reported LNAs to have RLC loads [30–39].

Note that a cascode stage could be used to increase the voltage gain compared with the single stage with inductively source degeneration. However, cascode stages limit the resonant frequency tuning in terms of voltage gain. Such a trade-off is illustrated in Fig. 7.7, where an inductively source degeneration (ISD) and a cascode with an inductively source degeneration (CISD) LNAs are compared respectively, considering a variation of g_{mn1}. Note that a lower tuning range is obtained by the CISD topology. For that reason, a simple input stage was considered in this design.

7.3.1 Input Impedance

Assuming ideal inductors and all transistors in Fig. 7.6 operating in the saturation region, and neglecting the effect of $R_{b1,2}$,[1] it can be shown that input impedance of the LNA is approximately given by:

$$Z_{i\text{IDCSA}} \simeq \frac{C_{gi} + C_{gsn\text{NF}} + sC_{gi}g_{mn\text{NF}}L_s + s^2C_{gsn\text{NF}}C_{gi}L_{gs}}{sC_i\left(C_g + sC_g g_{mn\text{NF}}L_s + s^2C_g C_{gsn\text{NF}}L_{gs}\right)} \tag{7.12}$$

where $C_{gsn\text{NF}}$ and $g_{mn\text{NF}}$ are respectively the small-signal gate-source capacitance and transconductance of $M_{n\text{NF}}$ transistor and

$$C_{gi} = C_g + C_i; \quad L_{gs} = L_g + L_s \tag{7.13}$$

[1]This approximation is only valid if $R_{b1,2} \gg 50\Omega$, as it is the case in this design.

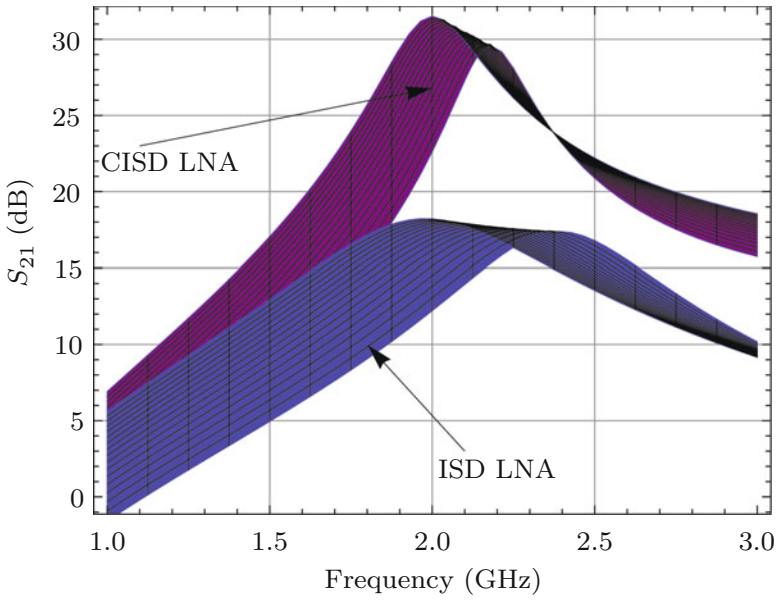

Fig. 7.7 Dependency of the voltage gain in CISD and ISD LNAs due to g_{mn1} variation

The real part of $Z_{i\text{IDCSA}}$, given by $(g_{mn\text{NF}}L_s/C_{gsn\text{NF}})$, must be set equal to the RF source resistance, R_{RF}, in the band of interest—1.85–2.48 GHz in this design. In this prototype, as the LNA is fully integrated as a stand-alone circuit, a termination of 50 Ω is needed not only at the input terminal but also at the output one, as will be shown in the next section.

The tuning mechanism of the LNA is achieved by varying the resonance frequencies of the passive input/output tuning network. This way, a variation in $Z_{i\text{IDCSA}}$ produces a change in S_{11}, because they are related by [40, 41]:

$$S_{11} = \frac{Z_{i\text{IDCSA}} - R_{\text{RF}}}{Z_{i\text{IDCSA}} + R_{\text{RF}}} \tag{7.14}$$

As an illustration Fig. 7.8 depicts S_{11} parameter for the LNA operating in the GSM standard, comparing theoretical predictions given by (7.14) with electrical simulations that take into account layout-extracted parasitics as well as chip-package parasitics. Both theory and simulations match well within the signal band, where the condition $S_{11} < -10$ dB is satisfied. Main differences between theory and simulation are obtained outside the signal band, and are mainly caused by the effect of the circuit element parasitics—not considered in the theoretical analysis described above.

Matching conditions can be obtained from the value of the LNA input impedance at the resonant frequency, where the imaginary part of Z_i becomes zero and its real part is approximately given by:

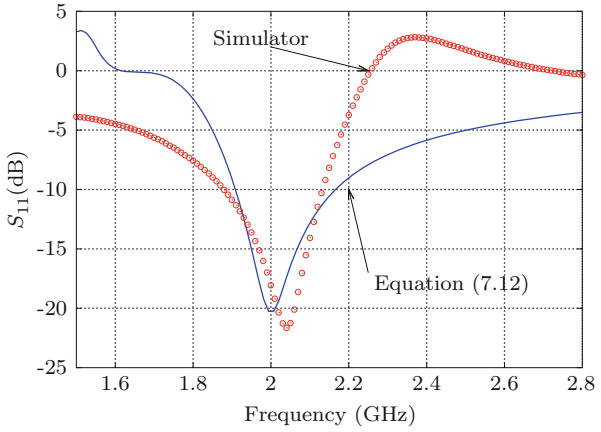

Fig. 7.8 S_{11} parameter on GSM standard

$$\mathrm{Re}|Z_i| \simeq \frac{C_{gsn\mathrm{NF}} g_{mn\mathrm{NF}} L_s}{C_g^2 g_{mn\mathrm{NF}}^2 L_s^2 \omega^2 + \left(C_g + C_{gsn\mathrm{NF}} - C_g C_{gsn\mathrm{NF}} L_{gs} \omega^2\right)^2} \tag{7.15}$$

where ω stands for the angular frequency, expressed in rad/s.

Therefore, the input impedance of the LNA must be equal to the antenna output impedance in order to obtain the required coupling. This condition can be written as:

$$R_{RF} \simeq \frac{C_{gsn\mathrm{NF}} g_{mn\mathrm{NF}} L_s}{C_g^2 g_{mn\mathrm{NF}}^2 L_s^2 \omega^2 + \left(C_g + C_{gsn\mathrm{NF}} - C_g C_{gsn\mathrm{NF}} L_{gs} \omega^2\right)^2} \tag{7.16}$$

On the other hand, making $Im|Z_i| = 0$, the resonant (angular) frequency can be calculated, giving:

$$\omega_{i\mathrm{IDCSA}} \simeq \sqrt{\frac{C_{gsn\mathrm{NF}} L_{gs} z_2 - z_1 - \sqrt{z_1^2 - 2C_{gsn\mathrm{NF}} L_{gs} z_1 z_2 + C_{gsn\mathrm{NF}}^4 C_i^2 L_{gs}^2}}{2C_g C_{gsn\mathrm{NF}}^2 C_{gi} L_{gs}^2}} \tag{7.17}$$

where

$$C_{gi2} = 2C_g + C_i; \quad z_1 = C_g C_{gi} g_{mn\mathrm{NF}}^2 L_s^2; \quad z_2 = 2C_g C_{gi} + C_{gsn\mathrm{NF}} C_{gi2} \tag{7.18}$$

Note that a variation of C_g allows us to properly set up the LNA operating bandwidth. This effect can be used for frequency tuning without needing any switches. As an illustration, Fig. 7.9a, represents the S_{11} variation with C_g for different operating frequencies. These curves can be used to optimize the LNA performance for a given set of specifications in a given frequency tuning range.

Note from Fig. 7.9a that there is not a linear relation between S_{11} parameter and C_g. As a consequence, depending on the absolute values of the operating frequencies, a different tuning range will be required for the value of C_g. For instance, the

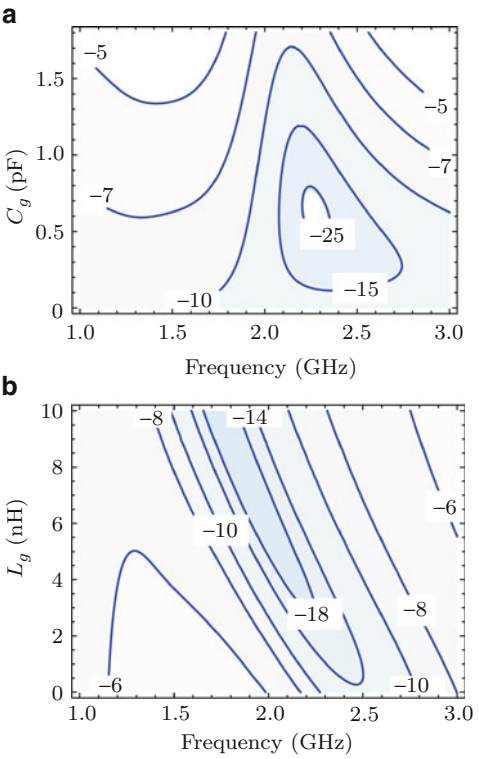

Fig. 7.9 Resonant frequency tunning for S_{11} using: (**a**) C_g varactor and (**b**) L_g inductor

frequency band ranging from 2.4 to 2.6 GHz requires a variation range for C_g smaller than in the case of 1.6–1.8 GHz band. This behavior translates into a maximum frequency tuning range that will depend on the maximum variation allowed by the physical implementation of C_g—based on the use of varactors in this case.

Inductor L_g can be combined with C_g varactor to set up the resonant frequency. This is illustrated in Fig. 7.9b for S_{11}, showing an inverse relation between the tuned frequency and L_g. This way, both the resonant frequency and the quality factor, Q, increases as L_g is reduced, at the price of increasing the sensitivity to circuit parasitics.

7.3.2 Voltage Gain

The proposed LNA shown in Fig. 7.6 has two amplification stages. In addition to increasing the overall gain, the second stage is used to improve the isolation.

Assuming that inductors are ideal, the voltage gain at each stage, denoted as $A_{v1\text{IDCSA}}$ and $A_{v2\text{IDCSA}}$, can be approximated expressed as:

$$A_{v1\text{IDCSA}} \simeq \frac{-C_i g_{mn\text{NF}}(1+g_{dsp\text{NF2}}sL_{d1})}{sC_{gi}C_{gsn\text{G}}(1+g_{mn\text{NF}}sL_s+s^2C_{gsn\text{NF}}L_{gs})} \tag{7.19}$$

$$A_{v2\text{IDCSA}} \simeq -g_{mn\text{G}}R_L(1+g_{dsp\text{G2}}sL_{d2}) \tag{7.20}$$

where $g_{dsp\text{NF2}}$ is the small-signal drain-source conductance of $M_{p\text{NF2}}$ transistor, $C_{gsn\text{G}}$ and $g_{mn\text{G}}$ are the small-signal gate-source capacitance and transconductance of $M_{n\text{G}}$ transistor, respectively, $g_{dsp\text{G2}}$ is the drain-source conductance of $M_{p\text{g2}}$ transistor and R_L is the load resistance connected at the output of the LNA.

The total voltage gain of the LNA can be calculated from (7.19) and (7.20), giving:

$$A_{v\text{IDCSA}} = A_{v1\text{IDCSA}}A_{v2\text{IDCSA}} \tag{7.21}$$

$$A_{v\text{IDCSA}} \simeq \frac{C_i g_{mn\text{NF}}g_{mn\text{G}}R_L(1+g_{dsp\text{NF2}}sL_{d1})(1+g_{dsp\text{G2}}sL_{d2})}{sC_{gi}C_{gsn\text{G}}(1+g_{mn\text{NF}}sL_s+s^2C_{gsn\text{NF}}L_{gs})} \tag{7.22}$$

Note that a resistive load, R_L, has been considered to compute (7.22) because the measurement equipment requires such a load impedance. However, if a capacitive load, C_L, is used, the voltage gain can be approximated written as:

$$A_{vCL\text{IDCSA}} \simeq \frac{C_i g_{mn\text{NF}}g_{mn\text{G}}(1+g_{dsp\text{NF2}}sL_{d1})(1+g_{dsp\text{G2}}sL_{d2})}{s^2C_{gi}C_{gsn\text{G}}C_L(1+g_{mn\text{NF}}sL_s+s^2C_{gsn\text{NF}}L_{gs})} \tag{7.23}$$

A performance metric typically used to characterize the voltage gain of LNAs is the S_{21} parameter, which can be calculated as [42]:

$$|S_{21}| = 2A_{v\text{IDCSA}}\sqrt{\frac{R_{\text{RF}}}{Z_L}} \tag{7.24}$$

As an illustration Fig. 7.10a represents S_{21} versus frequency, showing a good agreement between simulation results and theoretical predictions.

7.3.3 *Output Impedance*

As the LNA is tested as a stand-alone circuit, a varactor-based tuning network is also used at the output of the LNA. To this purpose, an accumulation-MOS varactor—labelled C_d in Fig. 7.6—was used.

Proceeding in a similar way as in previous sections and assuming that inductors L_{d2} and L_o are ideal, the output impedance of the LNA is approximately given by:

$$Z_{o\text{IDCSA}} \simeq \frac{1}{sC_o}+sLo+\frac{1+sL_{d2}\left(g_{dspG2}+sC_d\right)}{sg_{dsn\text{G}}g_{dsp\text{G2}}L_{d2}+z_3(1+s^2C_dL_{d2})} \tag{7.25}$$

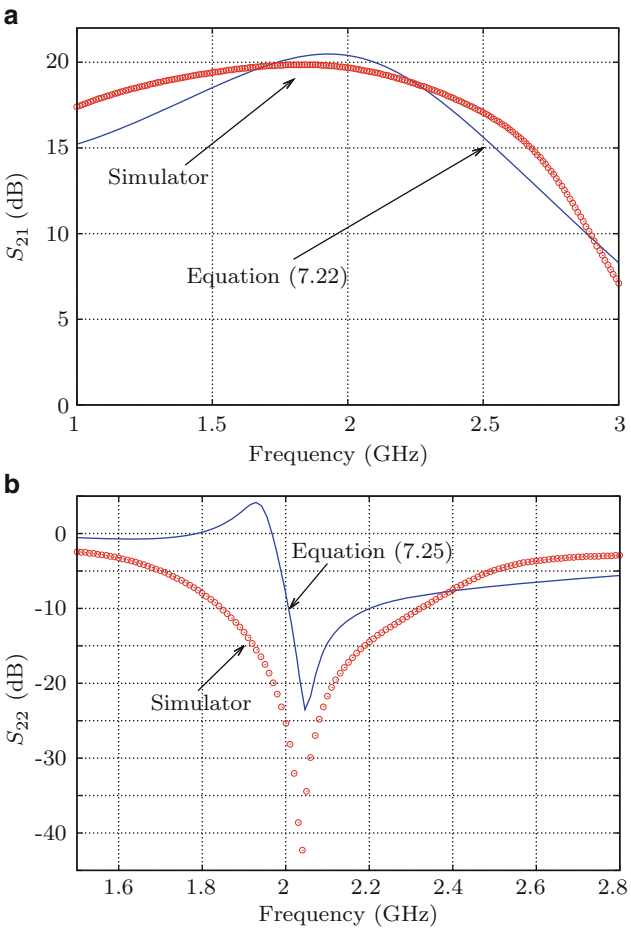

Fig. 7.10 Tunning S-parameters: (**a**) S_{21} for WLAN and (**b**) S_{22} in WCDMA

where

$$z_3 = g_{dsn\mathrm{G}} + g_{dsp\mathrm{G2}} \tag{7.26}$$

and $g_{dsn\mathrm{G}}$ is the small-signal drain-source conductance of $M_{n\mathrm{G}}$.

The output reflection parameter, S_{22}, can be calculated as [40, 41]:

$$S_{22} = \frac{Z_{o\mathrm{IDCSA}} - Z_L}{Z_{o\mathrm{IDCSA}} + Z_L} \tag{7.27}$$

As an illustration, Fig. 7.10b depicts S_{22}, comparing theoretical predictions with electrical simulations. The main differences between both curves are caused by circuit element parasitics, although a similar qualitative behavior is obtained. Note that in this example, the condition $S_{22} < -10\,\mathrm{dB}$ is satisfied in the band of interest.

A similar procedure to the one followed to establish the condition applied on input coupling network could be used for the output coupling network. In this case, coupling is achieved if the imaginary part of $Z_{o\text{IDCSA}}$ becomes zero when output network is operating at resonant frequency. Under these conditions, the real part of $Z_{o\text{IDCSA}}$ is approximately given by:

$$\text{Re}|Z_o| \simeq \frac{g_{dsn\text{G}} g_{dsp\text{G2}}^2 L_{d2}^2 \omega^2 + z_3 \left(-1 + C_d L_{d2} \omega^2\right)^2}{g_{dsn\text{G}}^2 g_{dsp\text{G2}}^2 L_{d2}^2 \omega^2 + z_3^2 \left(-1 + C_d L_{d2} \omega^2\right)^2} \tag{7.28}$$

Assuming that there is a load resistance, R_L, connected at the output of the LNA, the coupling condition can be written as:

$$R_L \simeq \frac{g_{dsn\text{G}} g_{dsp\text{G2}}^2 L_{d2}^2 \omega^2 + z_3 \left(-1 + C_d L_{d2} \omega^2\right)^2}{g_{dsn\text{G}}^2 g_{dsp\text{G2}}^2 L_{d2}^2 \omega^2 + z_3^2 \left(-1 + C_d L_{d2} \omega^2\right)^2} \tag{7.29}$$

On the other hand, assuming that $Im|Z_{o\text{IDCSA}}| = 0$, the output resonant frequency can be calculated as:

$$\omega_{o\text{IDCSA}} \simeq L_{d2} g_{dspG2} \sqrt{\frac{5.2 C_d g_{dsnG}^2 + 6 C_o g_{dspG2}}{3 g_{dsnG}^2 L_o}} \tag{7.30}$$

Note that L_o can be combined with C_d to operate at a given frequency while keeping the coupling condition. As an illustration, Fig. 7.11a shows how S_{22} parameter is tuned by varying C_d. Similarly, L_o can be adjusted to obtain the required value of S_{22}, as illustrated in Fig. 7.11b.

7.3.4 Noise Factor

Noise factor, F, is one of the most important performance metrics of LNAs. For the circuit under study, a noise analysis was carried out following the methodology described in [17], giving that the input referred equivalent noise sources of the LNA in Fig. 7.6 can be approximated by:

$$\overline{i_{ni}^2} \simeq \frac{-g_{mn\text{NF}} i_{ngn\text{NF}} + s C_g i_{ndn\text{NF}}}{g_{mn\text{NF}}} \tag{7.31}$$

$$\overline{v_{ni}^2} \simeq \frac{g_{mn\text{NF}} i_{ngn\text{NF}} + s C_{gi} i_{ndn\text{NF}}}{s C_i g_{mn\text{NF}}} \tag{7.32}$$

where $i_{ndn\text{NF}}$ and $i_{ngn\text{NF}}$ are respectively the internal noise sources associated to the gate and channel of $M_{n\text{NF}}$.

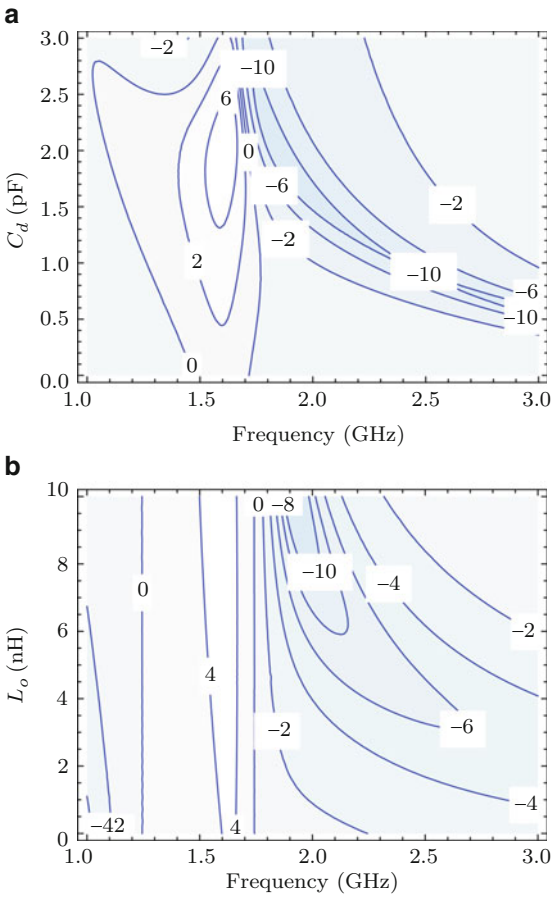

Fig. 7.11 Setting S_{22} parameter by using: (**a**) C_d varactor and (**b**) L_o inductor

Noise factor, F, can be easily obtained by replacing (7.31) and (7.32) in the following expression [43]:

$$F = 1 + \frac{\overline{v_{ni}^2} + R_{\mathrm{RF}}^2 \overline{i_{ni}^2}}{v_{n\mathrm{RF}}^2} \tag{7.33}$$

After some approximations, the noise factor for the proposed LNA shown in Fig. 7.6 can be approximated given by:

$$F_{\mathrm{IDCSA}} \simeq 1 + \frac{C_{gi}^2 \gamma}{C_i^2 g_{mn\mathrm{NF}} R_{\mathrm{RF}} \alpha} + \frac{C_g^2 R_{\mathrm{RF}} \gamma \omega^2}{g_{mn\mathrm{NF}} \alpha} + \frac{g_{mn\mathrm{NF}} \alpha}{C_i^2 R_{\mathrm{RF}} \omega_T^2} + \frac{g_{mn\mathrm{NF}} R_{\mathrm{RF}} \alpha \omega^2}{\omega_T^2} - \frac{2\sqrt{\gamma}\omega}{\omega_T} \tag{7.34}$$

where

$$\alpha = \frac{g_{mn\mathrm{NF}}}{g_{dsn\mathrm{NF}}}; \quad \omega_T = \frac{g_{mn\mathrm{NF}}}{C_{gsn\mathrm{NF}}} \tag{7.35}$$

As expected, the main contribution to the noise figure is due to the first stage, because the noise sources of the second stage are attenuated by the gain of the first stage within the signal bandwidth. Another interesting design issue is that the varactor capacitance, C_g, affects the noise performance—apart from its effect on the resonant frequency discussed in previous sections.

7.3.5 Design Procedure

The expressions described above have been used in a systematic design procedure, consisting of the following steps:

- Transistors $M_{n\mathrm{NF}}$ and $M_{p\mathrm{NF}1,2}$ are sized in order to obtain the minimum value required for NF in the signal bandwidth, see (7.34), while trying to achieve the maximum voltage gain possible with the least power dissipation, see (7.22). An important consideration is the fact that voltage gain is separated in two factors, because the proposed LNA topology has two amplification stages. This strategy allows to separately control the voltage gain and noise performance for a different set of specifications as will be shown later on. Thus, it contributes to achieve NF requirement with more freedom from voltage gain.
- Transistor $M_{n\mathrm{G}}$ and $M_{p\mathrm{G}1,2}$ are sized in order to achieve the maximum voltage gain through the proper adjustment of L_{d1} and L_{d2} inductors respectively, see (7.22).
- Passive elements of the input matching network (C_i, C_g, L_g and L_s) are derived in order to get the required impedance at resonant frequency, by using (7.12). This is a critical step, because LNA tuning depends on it. L_g inductor fixes frequency where operating mode will be adjusted by C_g varactor. L_s inductor allows to achieve real part of $Z_{i\mathrm{IDCSA}}$ at resonant frequency, and it must be equal to antenna impedance—see (7.16).
- The values of C_d, C_o and L_o are also calculated to get the output impedance matched at each required standard, using (7.25). However, L_o inductor is also used to establish frequency where it will be tunned by using C_d varactor, it is shown in Fig. 7.11b.
- Finally, technology parasitics are considered in an interactive electrical simulation process to re-fine the sizing and biasing obtained in the previous steps.

The outcome of the design procedure described above is the sizing and biasing of the LNA, summarized in Table 7.2, where C is capacitance, L and W are length and width for transistors respectively, I is the inductance and R is the resistance. $C_{da,b}$ and $C_{ga,b}$ are varactor arrays which allows to implement varactors with better performance.

Table 7.2 Programmable load LNA sizing

Element	Sizing
$C_{da,b}$	$C = 4.051\,\text{pF}$ $nfv = 19$ $L = 1\,\mu\text{m}$ $wv = 18\,\mu\text{m}$
$C_{ga,b}$	$C = 0.711\,\text{pF}$ $nfv = 6$ $L = 1\,\mu\text{m}$ $wv = 10\,\mu\text{m}$
C_i	$C = 1.5\,\text{pF}$
C_o	$C = 0.64\,\text{pF}$
L_{d1}	$dl = 140\,\mu\text{m}$ $I = 12.08\,\text{nH}$ $ntl = 6.5$ $wl = 10\,\mu\text{m}$
L_{d2}	$dl = 99.2\,\mu\text{m}$ $I = 4.733\,\text{nH}$ $ntl = 4.75$ $wl = 10\,\mu\text{m}$
L_g	$dl = 140\,\mu\text{m}$ $I = 5.87\,\text{nH}$ $ntl = 4.5$ $wl = 10\,\mu\text{m}$
L_o	$dl = 100\,\mu\text{m}$ $I = 7.049\,\text{nH}$ $ntl = 5.75$ $wl = 10\,\mu\text{m}$
L_s	$I = 0.7\,\text{nH}$
$M_{n\text{NF}}$	$L = 0.3\,\mu\text{m}$ $W = 220\,\mu\text{m}$
$M_{n\text{G}}$	$L = 0.3\,\mu\text{m}$ $W = 124\,\mu\text{m}$
$M_{p\text{G1}}$	$L = 0.1\,\mu\text{m}$ $W = 1\,\mu\text{m}$
$M_{p\text{G2}}$	$L = 0.1\,\mu\text{m}$ $W = 124\,\mu\text{m}$
$M_{p\text{NF1}}$	$L = 0.1\,\mu\text{m}$ $W = 1\,\mu\text{m}$
$M_{p\text{NF2}}$	$L = 0.1\,\mu\text{m}$ $W = 124\,\mu\text{m}$
R_{b1}	$R = 6\,\text{k}\Omega$
R_{b2}	$R = 4\,\text{k}\Omega$

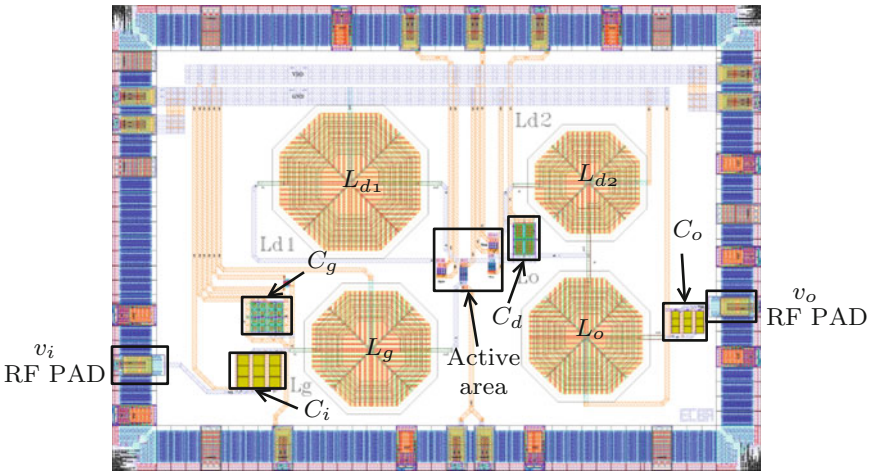

Fig. 7.12 LNA layout implemented in 90-nm CMOS technology

7.3.6 Layout, Packaging and Simulation Results

The LNA has been designed and implemented in a 90-nm CMOS technology with a single 1-V supply voltage. Figure 7.12 shows the layout of the chip highlighting their main parts. Integrated inductors have a patterned ground shield and octagonal shape—see Fig. 7.13a. Input/output capacitors are implemented by MOM structures, which are based on the combination of stacked and finger

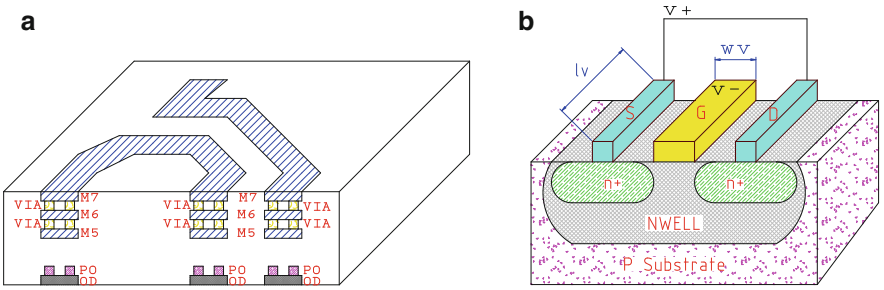

Fig. 7.13 Cross-section of the physical structure for: (**a**) Inductors and (**b**) Varactors

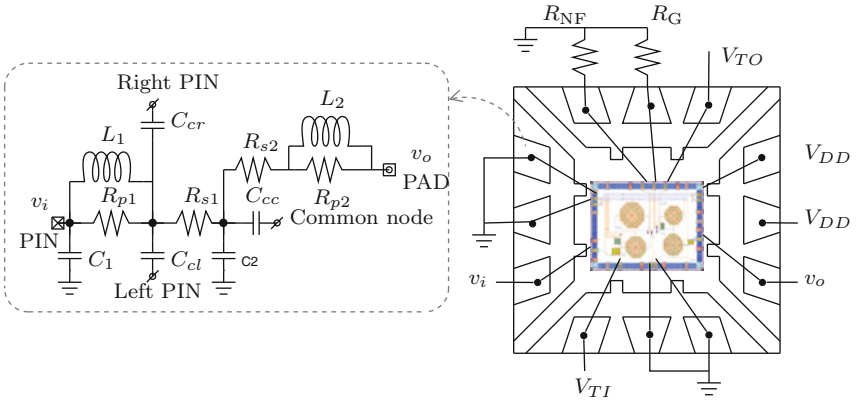

Fig. 7.14 Conceptual schematic of the PCB including the QFN package

metal-metal capacitors. MOS varactors shown in Fig. 7.13b are formed by source-drain connection in a MOS transistor. All PADs are Electrostatic Discharged (ESD) protected. The die area, including PADs, is 1.8 mm^2, with the core occupying 1.0 mm^2. As usual, a significant portion of this area corresponds to integrated inductors. However, in this circuit, and contrary to most reported multi-standard LNAs, the number of inductors is not increased as compared to the mono-standard case, with the subsequent area saving.

The circuit has been extensively verified using CADENCE SpectreRF©. Technology parasitics and package effects were considered in the simulations. For that purpose, the circuit in Fig. 7.14 was used. This circuit includes the package and the external components to be included in the PCB. A 4 mm × 4 mm 12-pin QFN plastic package has been used. This package has been modeled using CADENCE PKG© tool in order to take into account their associated parasitics during the design process.

Figure 7.15a represents NF vs input frequency for all the standards under study. The overall minimum value of NF is 1.9 dB, obtained at 2.4 GHz, which corresponds to the WLAN operation mode. Figure 7.15b–d show respectively the

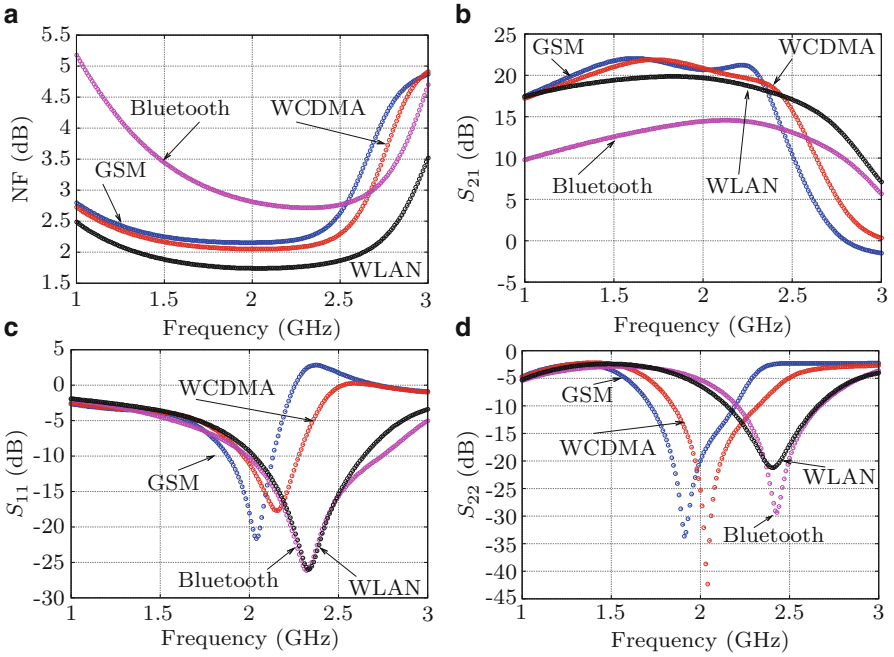

Fig. 7.15 Simulation of NF and S-parameters: (**a**) NF (**b**) S_{21} (**c**) S_{11} and (**d**) S_{22}

Table 7.3 Simulated LNA performance

Standard	IIP3 (dBm)	NF (dB)	S_{21} (dB)	S_{11} (dB)	S_{22} (dB)	P_{DC} (mW)
GSM	17.6	2.2	20.7	−9.0	−20.8	21.7
WCDMA	17.5	2.0	20.0	−8.6	−14.7	21.7
Bluetooth	10.9	2.7	13.3	−16.5	−21.8	17.4
WLAN b/g	19.0	1.9	17.2	−16.4	−18.2	21.7

input and output reflection coefficient (S_{11} and S_{22}) and forward-gain (S_{21}). The minimum value of S_{21} within the band of interest is above 13 dB—corresponding to Bluetooth—whereas S_{11} and S_{22} are below −8.6 dB for all standards.

On the other hand, the linearity of the LNA has been also taken into account in the design process. The minimum and maximum values achieved of the 3rd-order intermodulation intercept point, IIP3, are 10.9 dBm and 19 dBm, respectively for Bluetooth and WLAN. In addition to the nominal simulations describe above, Monte Carlo (100-run) and technology corners analysis were carried out.

Finally, Table 7.3 sums up the simulated performance of the LNA by showing the worst-case values of the different figures for each standard. Power consumption has a variation range of 4 mW, where the minimum power dissipation is for Bluetooth standard, but it has the minimum forward-gain and noise contribution is increased—worst case NF.

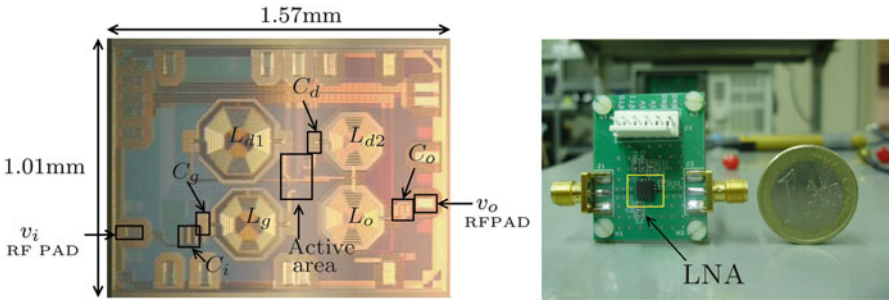

Fig. 7.16 (**a**) Chip microphotograph and (**b**) Test PCB

7.3.7 Experimental Results

Figure 7.16a shows a microphotograph of the chip highlighting their main parts, namely integrated inductors, capacitors, PMOS varactors and CMOS active area. The chip has been tested using the PCB shown in Fig. 7.16b, that includes the necessary filtering for biasing and power supplies as well as off-chip resistors and connectors for the instruments.

Figure 7.17a shows the measured NF vs input frequency, corresponding to different values of tuned frequencies, demonstrating the reconfigurability capability of the proposed LNA with a programmable NF within the band of interest. Reconfiguration of S_{21} parameter is illustrated in Fig. 7.17b, where value of S_{21} varies from 19.8 dB at 2.23 GHz to 23.4 dB at 1.9 GHz. This feature is a direct consequence of using MOS varactors in the resonance tuning networks, which provides approximately up to 700-MHz tuning range. Indeed, this is a peculiarity of the presented chip as compared to previously reported multi-standard LNAs—mostly based on using switchable LC tanks to select the resonant frequency in a discrete way and using varactors to fine tuning the selected band. The difference in the presented design is that it achieves a coarse continuous frequency tuning capability, just using varactors. This characteristic constitutes a first step towards achieving a tuning range in the order of GHz—required in future software defined radios.

7.4 State of Art on Reconfigurable LNAs

To conclude this chapter, Table 7.4 sums up the state of the art on reconfigurable LNAs reported so far. The performance of the chips in this table is compared by using the following Figures of Merit (FOM) [39]:

$$FOM_1 = \frac{S_{21}}{|\mathrm{NF}-1|\mathrm{P_{DC}}}; \quad FOM_2 = \frac{S_{21}\mathrm{IIP3}f_c}{|\mathrm{NF}-1|\mathrm{P_{DC}}} \tag{7.36}$$

where f_c is the resonant frequency of the LNA.

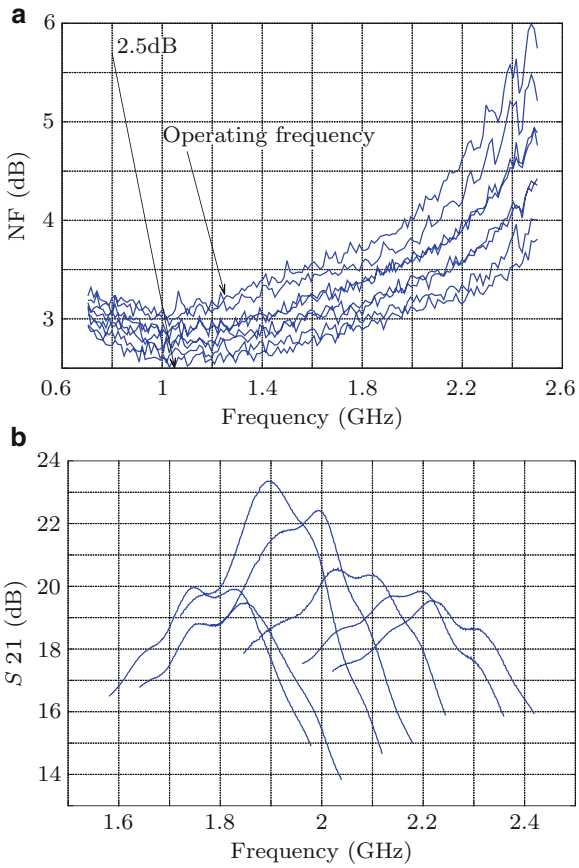

Fig. 7.17 Illustrating the LNA reconfiguration: (**a**) NF and (**b**) S_{21}

The LNA circuit presented in this chapter is included in the table for the sake of completeness. Note that the experimental results achieved by the proposed LNA compares favourably to previous LNAs while covering a larger number of standards.

7.5 Conclusions

Main circuit techniques for the design of reconfigurable LNAs intended for multi-standard wireless telecom systems have been overviewed. The use of varactors to continuously tune the operation frequency has been analyzed. This technique has been applied to the design and implementation of a two-stage LNA circuit which uses an inductively degenerated common-source configuration at the input stage. The use of MOS-varactor based tuning networks allows the circuit to adapt its performance to the specifications of different wireless standards in a continuously way, covering not only the target specifications at a given set of

Table 7.4 Comparison with the state-of-the-art reconfigurable CMOS LNAs

Ref.	Standard	IIP3 (dBm)	NF (dB)	P_{DC} (mW)	S_{21} (dB)	FOM_1	FOM_2
[6]	GSM 900	−12.8	4.6	32.4	18.0	0.1	0.0
	WLAN b/g	−15.3	4.43		24.0	0.3	0.0
	WLAN a	−14.7	4.42		23.0	0.2	0.0
[44]	2.4 GHz–5.4 GHz	−2.5	3.1	4.7	22.2	2.6	5.7
[45]	2.9 GHz–3.5 GHz	−10.0	3.6	18.0	9.0	0.1	0.0
[5]	WLAN b/g	0.0	2.3	4.0	14.0	1.8	4.3
	WLAN a	5.6	4.5		15.5	0.8	16.0
[18]	CDMA	−5.8	1.8	7.5	8.4	0.7	0.3
	WCDMA	−5.3	2.0		11.0	0.8	0.5
[12]	GSM	−7.5	5.2	24.0	28.5	0.5	0.2
	WCDMA	0.0	5.6		29.5	0.5	0.9
	WLAN b/g	−4.8	5.8		23.4	0.2	0.2
[46]	WLAN b/g	4.0	2.8	16.0	14.0	0.3	2.1
	WLAN a	−3.0	3.9	19.0	16.0	0.2	0.6
[47]	WLAN b/g	−21.4	3.1	1.1	10.0	2.8	0.0
	WLAN a	−6.7	3.8	1.0	10.1	2.3	2.6
[10]	ISM	−6.6	2.6	3.0	22.8	5.6	3.0
	UNII	−1.0	6.2	9.1	22.2	0.4	1.9
This work	1.78 GHz	−9.74	3.6		19.74	0.3	0.1
	1.84 GHz	−10.24	3.7		19.6	0.3	0.1
	1.92 GHz (GSM)	−10.11	3.6	23.0	22.82	0.3	0.1
	1.98 GHz	−10.22	3.7		22.31	0.5	0.1
	2.04 GHz (WCDMA)	−10.5	3.4		20.49	0.4	0.1
	2.1 GHz	−10.5	3.5		20.53	0.4	0.1

operation frequencies, as well as other operation modes in between. Experimental measurements of the prototype demonstrates a competitive behavior with the state of the art, showing that the proposed techniques are very suited for the implementation of continuously-tuned LNAs in future Software-Defined-Radio mobile systems.

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Chapter 8
Clocked Nanometer CMOS Comparators

Bernhard Goll and Horst Zimmermann

8.1 Introduction

A circuit block, which is mostly used in the link between the analog and the digital domain, e.g. in an analog-digital converter (ADC), is the clocked, regenerative comparator. This type of comparator is implemented mostly in ADCs with a fast conversion rate, e.g. in flash-ADCs [1–4] because of its capability of a fast decision. A comparator is a circuit, which typically compares two analog input voltages (VA_p, VA_n), currents or charges and delivers a logical level at the output, which indicates, what of the compared values was higher (see Fig. 8.1).

In other words the comparator gives as a result a logical value which indicates the polarity of the difference of the sizes of the input values. In common the circuit of a clocked, regenerative comparator is based on a cross-coupled inverter (latch) [5, 6] to force a fast decision with the help of positive feedback (see Fig. 8.2). With reset switches, which are not shown in Fig. 8.2, the latch is forced into a metastable point (see Fig. 8.2b), where both voltages u_1 and u_2 of the output nodes are equal. Therefore the regenerative comparator is clocked to reset the comparator during a part of the clock cycle, which means that for a following comparison phase an initial condition of a metastable point is forced. If comparison starts an initial voltage difference ΔU_0 is introduced to the latch after releasing the reset switches. Depending on the polarity of ΔU_0, u_2 is pulled to the stable point V_{DD} (e.g. the logical High) and u_1 is pulled to V_{SS} (e.g. the logical Low) or vice versa in case of inverse polarity (see Fig. 8.2b,d). Figure 8.2c shows the small-signal equivalent circuit of a latch. Index 1 marks the small-signal parameters (transconductance g_m, output resistance r) of inverter 1 (transistors N1 and P1) and index 2 is referred to inverter 2 (N2, P2). Voltage u_1 is the output voltage of inverter 1 (loaded with the capacitance C_1) and the input voltage of inverter 2. On the other hand u_2 is the output

B. Goll (✉) • H. Zimmermann
Vienna University of Technology, EMCE, Gußhausstraße 25/354 1040 Vienna, Austria
e-mail: bernhard.goll@tuwien.ac.at; horst.zimmermann@tuwien.ac.at

E. Tlelo-Cuautle (ed.), *Integrated Circuits for Analog Signal Processing*,
DOI 10.1007/978-1-4614-1383-7_8,

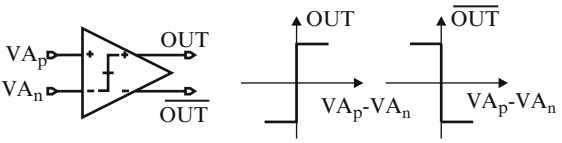

Fig. 8.1 Ideal comparator

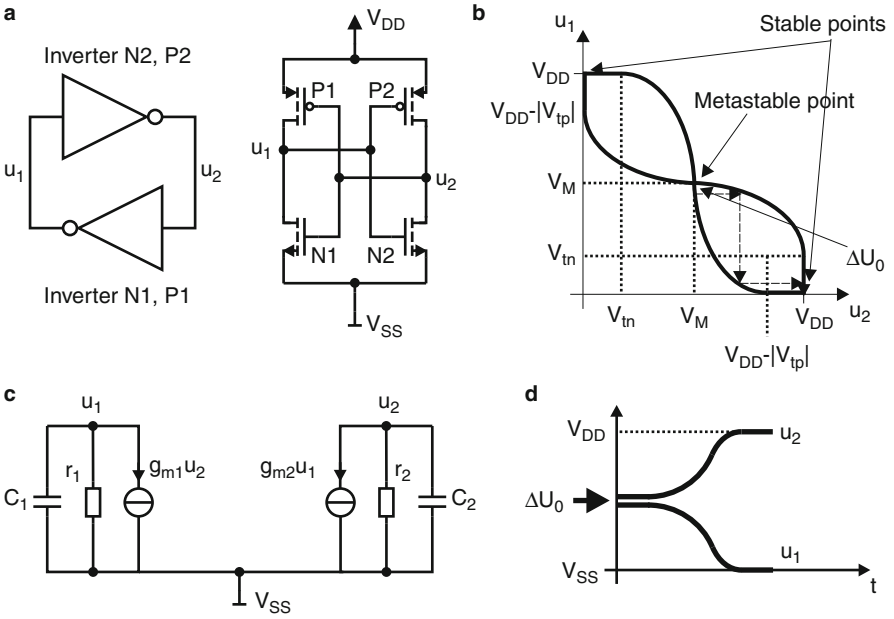

Fig. 8.2 The static latch: cross-coupled inverters (**a**), the characteristic (**b**), small-signal equivalent circuit (**c**), voltage-time dependence (**d**)

voltage of inverter 2 (loaded with capacitance C_2) and the input voltage of inverter 1. With the help of this small-signal representation a differential equation for the difference output-voltage $\Delta u(t) = u_2 - u_1$ with the initial condition $\Delta u(t=0) = U_0$ can be stated (see (8.1)), where the solution is shown in (8.2) [5].

$$\frac{d}{dt}\Delta u(t) = \Delta u(t)\frac{1}{C}\left(g_m - \frac{1}{r}\right) \tag{8.1}$$

$$\Delta u(t) = \Delta U_0 e^{\frac{g_m - \frac{1}{r}}{C}t} \quad \rightarrow \quad t_d = \frac{C}{g_m - \frac{1}{r}} ln\left(\frac{\Delta U_{end}}{\Delta U_0}\right), \quad g_m r > 1 \tag{8.2}$$

A delay time t_d can be also stated in (8.2) as the time duration till a distinct output voltage difference ΔU_{end} has been reached. It can be seen, that the delay time t_d lasts longer, if C is larger and g_m, r and ΔU_0 are smaller.

8.2 Characterization of Comparators

There are several characteristic values to describe a clocked regenerative comparator, which are treated in this chapter. The principle influence of an offset and a hysteresis to a clocked comparator, where additionally the decision is affected by noise, is depicted in Fig. 8.3. At the input nodes *INP* and *INN* the voltages to be compared are applied. In Fig. 8.3 at *INN* a reference voltage and at *INP* a triangle signal slowly varying compared to the clock period are applied. The influence of noise can be seen as an uncertainty in the decision near the crossover points of *INP* and *INN*, where the noise causes the comparator to perform random decisions [7]. The higher the input voltage difference $INP - INN$, the lower is the chance for a wrong decision. In most cases the noise is assumed to be a stationary random stochastic process, where the probability density function (pdf) of the amplitude of the noise is assumed to be mean free and Gaussian. There are different noise sources, which can be combined to an overall input referred noise source.

- *Noise of the sources of the signals*: The noise of the sources of the signals, which are applied to the input of the comparator disturb the decision. This might be uncertainty in amplitude or in time (jitter). Furthermore noise via the supply-voltage and ground-lines, which occur mostly due to switching of neighboring circuit components, may also cause a wrong decision of the comparator.

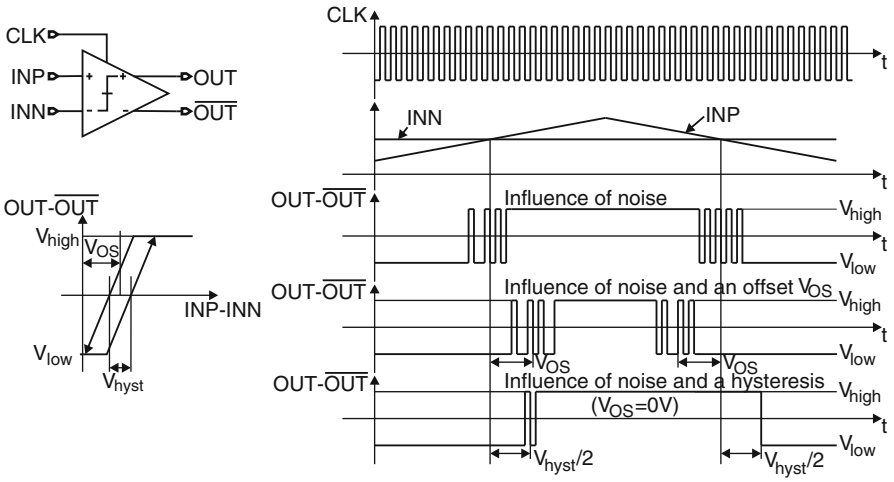

Fig. 8.3 Offset and hysteresis of a comparator, which is affected by noise

- *Noise caused by circuit elements*: In principle there are three sources of noise in CMOS devices [7]. *Shot noise* is the superimposed random variation of a current caused by fluctuation of charge carriers (electrons or holes) in pn-junctions. The mean square $\overline{i_{sn}^2}$ of this variation is given by $\overline{i_{sn}^2} = 2eI\Delta f$, where $e = 1.602 \times 10^{-19}C$ is the elementary charge, I is the average current and Δf is the bandwidth. *Thermal noise* is dominating in MOSFETS and exists due to random thermal motion of electrons in a real resistor at temperature ϑ. The mean square of the fluctuating voltage $\overline{v_{tn}^2}$ and of the equivalent current $\overline{i_{tn}^2}$ is given by $\overline{v_{tn}^2} = \overline{i_{tn}^2}R^2 = 4k\vartheta R\Delta f$. For a MOS transistor in saturation the approximation $R \approx \frac{3}{2g_m}$ can be used. *Flicker (1/f) noise* appears because of extra electron states at the boundary between Si and SiO_2, which trap and release electrons in a relatively slow time. Therefore most of the noise energy is located at lower frequency. An approximation of the mean square of the gate referred noise voltage of a MOS transistor is $\overline{v_{fn}^2} = \frac{K}{C_{ox}WL}\frac{\Delta f}{f}$, where K depends on the temperature and the fabrication process, C_{ox} is the gate capacitance per area and WL is the gate area.
- *Kickback noise*: Kickback noise [8] is caused by the comparator itself, when at the output nodes a fast transition due to positive feedback in the decision phase or due to pulling the output nodes to a defined voltage level in the reset phase occurs, which is coupled back via parasitic capacitances to the input nodes. Another source of disturbances coupled back is caused by the fast ramps of the clock. In most cases this noise can be neglected, because it results mostly in a common-mode disturbance at the inputs if also equal signal-source impedances are considered at each input. Also at the time, when the output nodes regenerate or reset, the output nodes cause a considerable voltage at the input nodes, the comparator has already done most of the decision and is therefore more immune against noise, if also a small enough source resistance is considered. The real problem of kickback noise occurs, if e.g. more comparators are placed in parallel in e.g. a flash ADC, where the reference and input voltages are affected by several comparators or e.g. the comparators decide at different times due to clock delays.
- *Static noise*: Static noise [9] is a DC disturbance, e.g. a disturbance of the working point, that is present in logic gates. This noise can be either series-voltage noise, parallel-current noise or voltage noise at the ground or power supply line. These noise sources might also appear in combination. In static random access memory (SRAM) cells, which consist in principal of static latched circuits to store a logical value, the *static noise margin (SNM)* is the minimal magnitude ΔV_{ser}, which has to be applied both at u_1 and in opposite sign at u_2 to change the logic state. Also for a comparator, which has already decided, it may be considered, that static noise may also affect the decision. But due to the fact, that a decision of the comparator in common only lasts for a half clock cycle and the clock period is small in the case of a fast comparator, the influence of DC disturbances can be neglected in most cases. A calculation of SNM can be found in [10]. The influence of device fluctuations of the process to SNM was analyzed in [11].

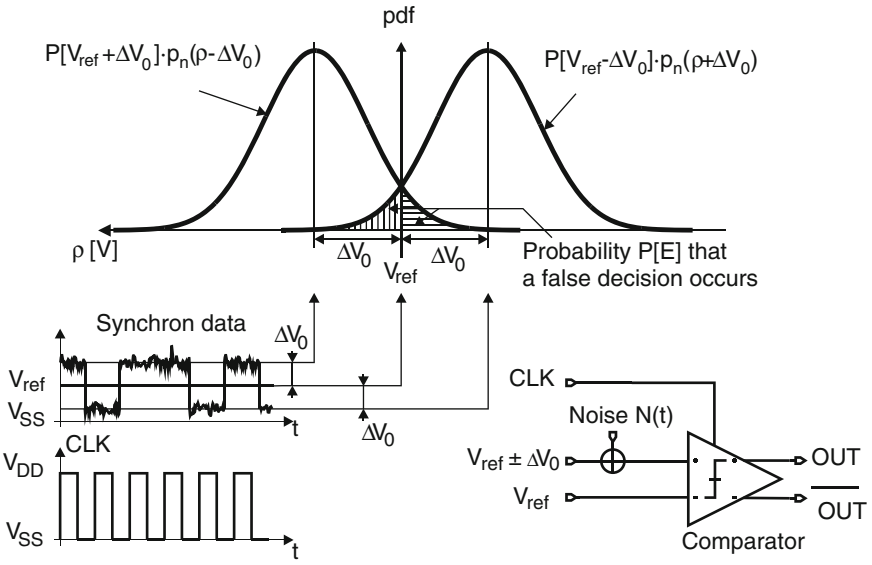

Fig. 8.4 Occurrence of bit errors due to the influence of noise [12]

The influence of noise to a decision of a clocked, regenerative comparator and hence the sensitivity of this comparator can be measured with the help of BER (bit-error-ratio) measurements. Figure 8.4 shows the principle model for calculating the BER. For calculation of the BER the whole input-referred combined noise $N(t)$ of the comparator is assumed to be a stationary stochastic process [12], where the probability density function (pdf) $p_{n0}(\zeta)$ is a Gaussian distribution (mean free μ_n, standard deviation σ_n) doesn't change at different time-points. The data stream is modelled by bits with logical voltage levels $V_{ref} \pm \Delta V_0$ (high and low), where V_{ref} is the decision threshold. If the probability of appearance of a logical high is equal to that of a logical low ($P[V_{ref} + \Delta V_0] = P[V_{ref} - \Delta V_0] = 0.5$), then the probability $P[E]$ that a bit error occurs can be calculated as shown in (8.3).

$$Q(\zeta) = \frac{1}{\sqrt{2\pi}} \int_{\zeta}^{\infty} e^{-\frac{\alpha^2}{2}} d\alpha$$

$$P[E] = 0.5Q\left(\frac{\Delta V_0}{\sigma_N}\right) + 0.5\left(1 - Q\left(\frac{-\Delta V_0}{\sigma_N}\right)\right) = Q\left(\frac{\Delta V_0}{\sigma_N}\right) \tag{8.3}$$

This BER can be measured with BER analyzer stations, where the data stream at the output of a comparator is compared with a reference data stream at the input (a pseudo-random bit-sequence) and where occurring bit errors are counted.

If the noise is considered to be removed in a comparator, a metastability error might occur if a too low input-voltage difference is applied. Such an error occurs, because the amplification of a comparator is dependent on the decision time as illustrated in (8.2). So at a higher clock frequency a lower decision time is available

and a higher input voltage difference is necessary to reach the final output voltage difference. For a distinct small input-voltage difference range the comparator cannot decide, the comparator stays during the available time for decision near the metastability point (see Fig. 8.2 and a metastability error occurs. With noise, the outputs of a clocked comparator would deliver a random decision per clock cycle if the condition of metastability is given (BER→0.5).

The *offset* V_{OS} of a comparator is defined as the input voltage difference, which has to be applied to obtain the crossing point between logic level low and high. In Fig. 8.3 it can be seen, that the switching point of the comparator is shifted away from the cross-point of *INP* and *INN* by the offset V_{OS}. In Fig. 8.3 the clock period of the comparator is small in comparison to the period of the triangle. The offset is caused by the following reasons:

- The mismatch of different electronic parts, e.g. resistors, capacitances [13] and transistors in the circuit results as a consequence of a deviation from an ideal symmetrical circuit structure. The mismatch between two transistors [14, 15], which is for MOS transistors mainly the mismatch of their threshold voltages V_t and their transconductance parameter β, can be described with (8.4). These laws for the standard deviations for the transconductance parameters and threshold voltages are based on a Gaussian probability distribution.

$$\sigma(\Delta V_t) = \frac{A_{\Delta Vt}}{\sqrt{W \cdot L}} \qquad \frac{\sigma_{\Delta\beta}}{\beta} = \frac{A_{\Delta\beta}}{\sqrt{W \cdot L}} \tag{8.4}$$

  The parameters $A_{\Delta Vt}$ and $A_{\Delta\beta}$ are proportionality factors being characteristic for the technology used. W is the width and L is the length of the gate of the MOS transistor. The influence of process tolerances causes in principle random offset, where the mean value is zero.
- Gradients of e.g. temperature or stress, which are introduced by neighboring circuit blocks have an influence to the symmetric functionality of the comparator and cause typically systematic offsets (the mean value is not zero). The offset caused by gradients can be minimized with an intelligent placement of components in the layout.
- Systematic offsets are also introduced by asymmetry due to the used circuit structure.
- The offset also may change in some cases between different clock frequencies (dynamic effects), e.g. if a mismatch in the reset switches or on coupling capacitors are present.

When a comparator has a *hysteresis* [7], the comparison threshold for input signals is different in the case that the output changes from low to high and in the case of a change from high to low. The distance between these comparison thresholds is characterized in Fig. 8.3 by the hysteresis voltage V_{hyst}. In case of an hysteresis, the comparator is more immune against noise, because noise has to overcome the voltage V_{hyst} to flip back the decision of the comparator. A typical source of creating a hysteresis in a clocked regenerative comparator is, if the

reset switches are dimensioned too small. So at the end of the reset phase a considerable voltage difference exists still between the output nodes, which has to be overcome by the input voltage in the following comparison phase and a hysteresis is established.

The *delay time* of a clocked regenerative comparator is the minimum time duration from beginning of the comparison phase (reset is released when the appropriate clock edge reaches typically 50% of V_{DD}) till a valid logical voltage level is available at the output. Another definition is the minimum time duration from beginning of the comparison phase (reset is released when the appropriate clock edge reaches typically 50% of V_{DD}) till one output node reaches the half supply voltage $V_{DD}/2$.

A further important parameter to characterize a clocked regenerative comparator is the power consumption. Typically it consists of a static and a dynamic part. The latter of depends on the clock frequency and the capacitances, which have to be charged and discharged.

8.3 CMOS Technology

The cross section of a typical CMOS process is shown in Fig. 8.5. It is a twin well process on a non-epi p-substrate, where for isolation a shallow trench isolation (STI) is used. The p^+ diffusion area of an n-MOS transistor is electrically connected

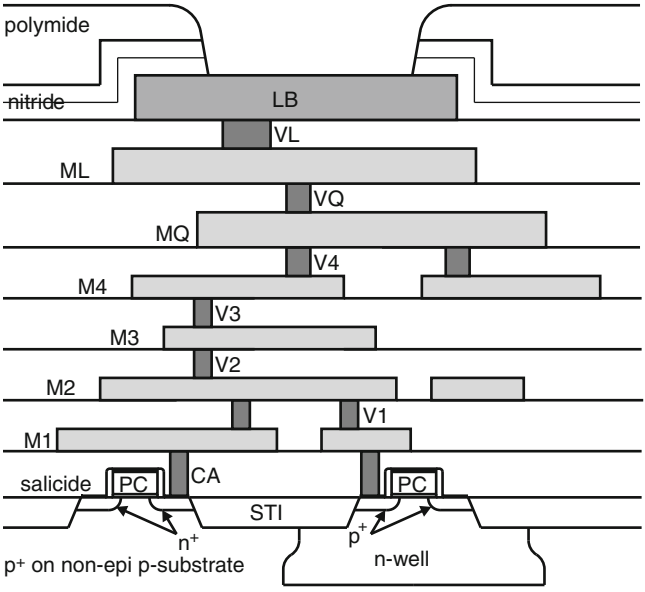

Fig. 8.5 Cross section of a typical deep-sub-micron (DSM) CMOS process

to the p-substrate. More advanced technologies implement a triple well process, where the p-well for an n-MOS transistor is placed inside a deep n-well, which electrically isolates the n-MOS transistor. In opposite to that, the p-MOS transistors are placed in a n-well, which separates this transistor from the p-substrate. To lower the resistance mostly a $CoSi_2$ salicided (self-aligned silicided) layer for n^+ and p^+ polysilicon and diffusion areas is added. A so called stud contact (tungsten plug) to connect the poly-silicon gate or diffusion region of transistors to metal level M1 is marked with CA and the wiring level contacts are named V1, V2, V3, VQ and VL. For the metal layers, copper is used. Layers M1 to M4 are thin and tighter-pitch copper levels and MQ and ML are thick copper levels with a relaxed pitch. The last metal level LB is also used for pads made of AlCu [16].

In ultra-deep-sub-micron (UDSM) CMOS technology, analog circuit design suffers from the low supply voltages, which are necessary to avoid too high electric fields in MOS transistors and to optimize power consumption of digital circuits. In common, having a small voltage headroom left, decreases the voltage gain at a given power consumption [20]. On the other hand the clock frequency of digital logic tends to become better in CMOS technologies due to lower parasitic capacitances. Also the bandwidth of analog circuits increases with shrinking transistors. However a problem is the increasing gate tunnel current, when the gate area is increased (optimal g_m/I_D ratio supposed) for e.g. reducing the input-referred offset. Lowering the influence of V_t and β mismatch by increasing gate area is limited by gate-leakage mismatch. It is now a challenge to develop new circuit structures, which either avoid a stack of too many transistors between the supply rails so that the technology-given better AC performance does not degrade, but otherwise keep the advantages of standard circuits, e.g. robustness against influence of noise and mismatch or lower power consumption.

8.4 Comparator Circuits

In the literature, many types of comparator circuits can be found. In Fig. 8.6 two comparator circuits are shown, which can be often found in integrated circuits. Figure 8.6a shows a comparator, where the input transistor pair N2, N3 is placed below the latch N0, P0, N1, P1 [17, 18]. The operation of the comparator is divided into two clock phases. When CLK is at voltage level V_{SS}, transistor N6 is cut off and transistors P2 and P3 pull both output nodes to supply-voltage level V_{Comp} to reset the comparator. If CLK changes to level V_{Comp} the initial condition is, that both output nodes are at level V_{Comp}, transistors P0, P1, P2 and P3 are off and transistors N0 and N1 are on. Transistors N2 and N3 start to discharge both output nodes with a current difference $\Delta I_{n6} = g_{mn2}\Delta U_{in} = \sqrt{2\beta_{n2}I_{n6}}$, where $\Delta U_{in} = INP - INN$ is the constant assumed input voltage difference, $g_{mn2} = g_{mn3}$ are the equally assumed transconductances of transistors N2 and N3, $\beta_{n2} = \beta_{n3}$ are their transconductance parameters and I_{n6} is the tail current through switch transistor N6. If one output

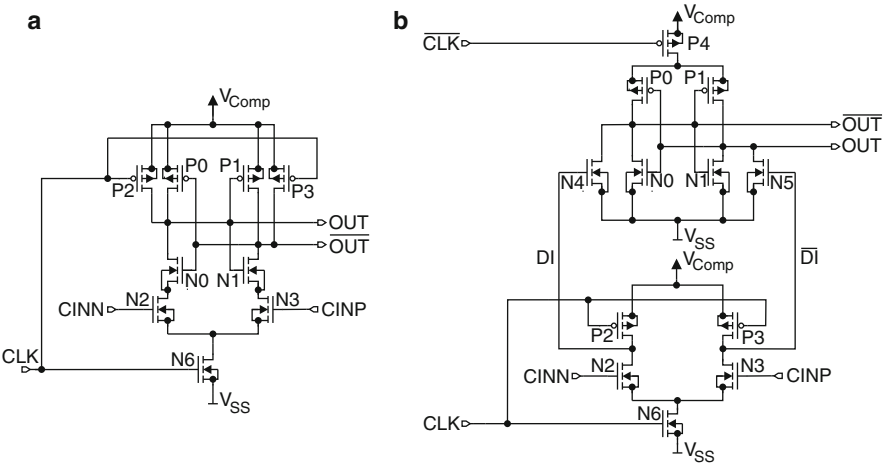

Fig. 8.6 Two comparators, which are often described in literature: latch-type voltage sense amplifier [17, 18] (**a**), double-tail latch-type voltage sense amplifier [19] (**b**)

node reaches the voltage $V_{Comp} - |V_{tP0}|$ after a time duration of $t_0 \approx (2C_L|V_{tP0}|)/I_{n6}$, where $V_{tP0} = V_{tP1}$ are the equally assumed threshold voltages of transistors $P0$ and $P1$, then positive feedback of cross-coupled inverters N0, P0 and N1, P1 begins and the latch regenerates to $OUT = V_{Comp}$ and $\overline{OUT} = V_{SS}$ in the case $INP > INN$ and vice versa. C_L is the overall load capacitance of an output node. The output voltage difference $\Delta u(t = t_0) = OUT(t = t_0) - \overline{OUT}(t = t_0) \approx 2|V_{tP0}|g_{mn2}\Delta U_{in}/I_{n4}$ at this time t_0 determines the initial voltage difference of the second phase, where positive feedback of the latch is turned on. With this initial voltage difference the latch regenerates similar as depicted in (8.2) (see (8.5), [18]).

$$\Delta u(t \geq t_0) = 2|V_{tP0}|\frac{g_{mn2}\Delta U_{in}}{I_{n4}} e^{\frac{g_m - \frac{1}{r}}{C_L} t} \tag{8.5}$$

In (8.5) g_m is the overall transconductance and r is the overall output resistance of the latch $P0$, $P1$, $N0$, $N1$. In principle the comparator structure of Fig. 8.6a has a rail-to-rail output voltage swing and consumes only dynamic power. The latch-type sense amplifier was produced in a 0.13 µm/1.5 V CMOS process and worked down to a supply voltage of 0.7 V [18]. The delay time was determined with electronic beam measurements and is e.g. 119ps for an input voltage difference of 100 mV. Disadvantageous is, that a sufficient supply voltage level is needed due to the stack of transistors (comparison time longer than 11 ns at 0.7 V). The comparator circuit in Fig. 8.6b is a further development of Fig. 8.6, which was first proposed in [19]. The amount of stacked transistors between the supply rails are reduced by adding an additional input amplifier (transistors N2, N3, N4, N5, P2, P3) instead of transistors N2 and N3 in Fig. 8.6a. In the reset phase ($CLK = V_{SS}$, $\overline{CLK} = V_{Comp}$) transistors N6 and P4 are switched on and transistors P2 and P3 are turned on. So nodes DI

and $\overline{DI}$ are pulled to supply voltage level V_{Comp} thus both output nodes OUT and $\overline{OUT}$ are pulled to V_{SS}. When CLK switches to V_{Comp} ($\overline{CLK} = V_{SS}$), transistors P2 and P3 are turned off, transistors N6 and P4 are switched on and the comparison phase starts. The internal nodes DI and $\overline{DI}$ are discharged by transistors N2 and N3 and corresponding to the input voltage difference $CINP - CINN$ an amplified voltage difference $DI - \overline{DI}$ occur. This voltage difference is amplified again by transistors N4 and N5, which drives the latch. The latch pulls OUT to V_{Comp} and $\overline{OUT}$ to V_{SS} in the case of $CINP > CINN$ and vice versa. Because the input voltage difference is amplified two times with transistors (N2, N4 and N3, N5 respectively) a comparably large voltage drives the latch. Therefore and due to the fact that less transistors are stacked between the supply rails, this type of comparator circuit is capable for low-voltage operation. In [19] the circuit of Fig. 8.6b was fabricated in a 90 nm/1.2 V CMOS technology. Simulation results have shown, that this sense amplifier needs e.g. a delay time of ≈90ps for an input voltage difference of 10 mV at a low supply voltage of 1 V. In principle this circuit is faster than the circuit shown in Fig. 8.6a. Measurement results have shown that this sense amplifier has an offset voltage of $\sigma_{OS} = 8$ mV. Furthermore a power consumption of 225 µW at a clock frequency of 2 GHz at 1.2 V supply voltage and 50 mV input voltage difference has been measured.

8.5 A Comparator in 0.12 µm CMOS Technology Requiring 0.5 V at 600 MHz

This section describes a comparator, which is capable to work down to a supply voltage of 0.5 V with a maximum clock frequency of 600 MHz [21]. Figure 8.7 shows the schematic of the comparator. Like in many comparator circuits, here a clock cycle is divided into a reset and a comparison phase. During reset phase the voltage level at CLK is V_{SS} thus turning off transisitors N0 and N1 and turning on transistors P0 and P1. In reset phase nodes CLK and $CLKR$ have the same level of V_{SS} because the gate-source voltage of N8 is larger than the threshold voltage V_{tN8} of this transistor. Both output nodes OUT and $\overline{OUT}$ are pulled to potential V_{Comp} thus creating an initial condition for the following comparison phase. Comparison of the input voltages $CINP$ with $CINN$ starts when CLK switches to voltage level V_{Comp} In opposite to a conventional comparator, transistors P0 and P1 are used to reset the comparator when CLK has the level of V_{SS} and when CLK changes to level V_{Comp} the same transistors are biased as active load. So additional reset switches, which contribute parasitic capacitances to the output nodes and reduce speed are avoided. Because transistor N8, which is biased with an adjustable bias voltage $TBIAS$ at its gate, has been added to the clock line, $CLKR$ rises to $TBIAS - V_{tN8}$, if sub-threshold and leakage currents are neglected for simplicity and an ideal quadratic MOS-transistor characteristic is assumed. So P0 and P1 are biased to become active loads. At the beginning of the comparison phase the output nodes

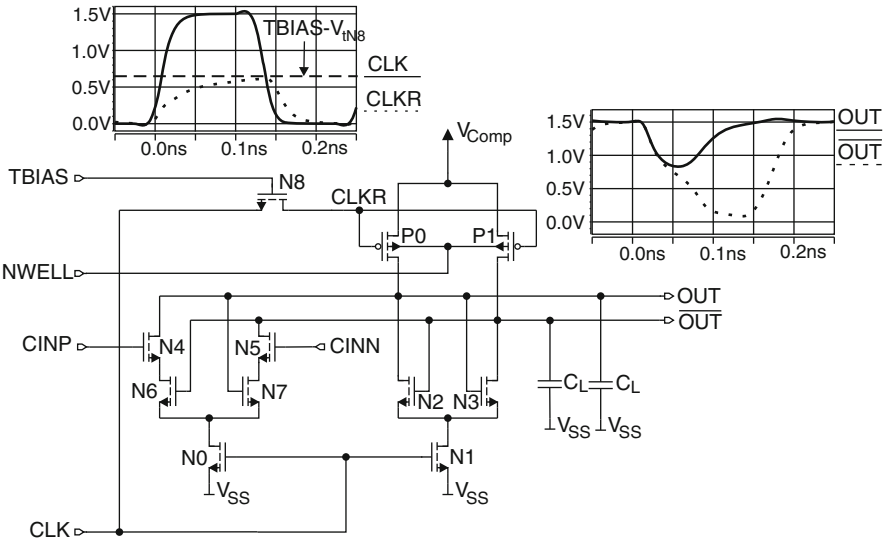

Fig. 8.7 Schematic of the comparator

have been pre-charged initially to V_{Comp} from previous reset. Transistors N6 and N7 are on and each of the transistors N2 and N3 (latch) has initially a gate voltage near V_{Comp}. Therefore the tendency to speed up transistors N2 and N3 is given. This and the fact that N2 to N8 are transistors with a low threshold voltage of about 0.29 V, provided by this CMOS process, it is possible to drive the comparator even down to a supply voltage of $V_{Comp} = 0.5$ V. Due to positive feedback of transistors N2 and N3 the latch regenerates depending on the input-voltage difference at transistors N4 and N5. Transistors N6 and N7 are added below the input transistors N4 and N5 to reduce static current flow after the decision of the comparator. This can be seen when the voltage level at e.g. OUT is below the threshold voltage of N7, the path via N5 and N0 to V_{SS} is cut off. Also the path between OUT and $\overline{OUT}$ via transistors N4, N5, N6 and N7 is cut off. At pin $NWELL$ the separated n-well of P0 and P1 can be biased with a DC voltage to somewhat utilize the backgate effect to have an additional possibility to adjust the currents through transistors P0 and P1. Transient simulations of the comparator can be seen in Fig. 8.8 for a supply voltage of $V_{Comp} = 0.5$ V.

A test chip for the comparator has been designed, which is shown in Fig. 8.9. The chip is divided into two parts, one with a supply voltage of $V_{DD} = 1.5$ V for optimal functionality of CMOS logic needed for measurement purposes, and a second part with supply voltage V_{Comp}, where the comparator is placed. The clock is applied to pin $CLKIN$ and processed by the clock driver to two complementary rectangular clock signals CLK and $\overline{CLK}$ with the logic levels V_{SS} for low and V_{Comp} for high. RC low-passes (R_1, C_1 and R_2, C_2) are added for adjusting the clock duty cycle to about 50% by varying the bias voltage at $CLKIN$. The mean voltage at pins $CLKAVP$ and

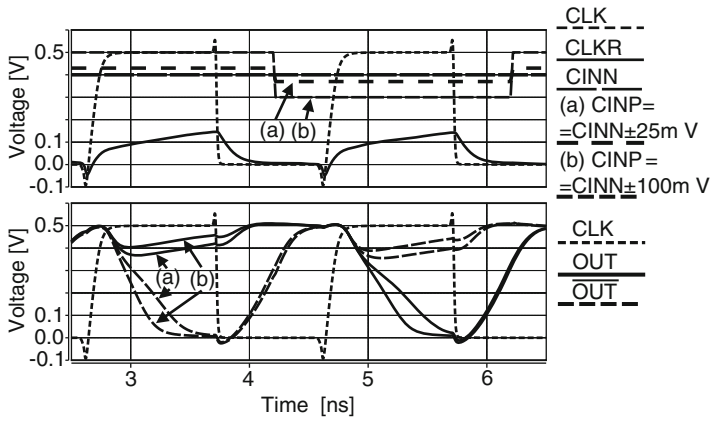

Fig. 8.8 Transient simulation of the comparator at a supply voltage of $V_{Comp} = 0.5\,\mathrm{V}$ and 500 MHz clock frequency: $TBIAS = 0.4\,\mathrm{V}$ (**a**) $CINP - CINN = \pm 25\,\mathrm{mV}$ (**b**) $CINP - CINN = \pm 100\,\mathrm{mV}$

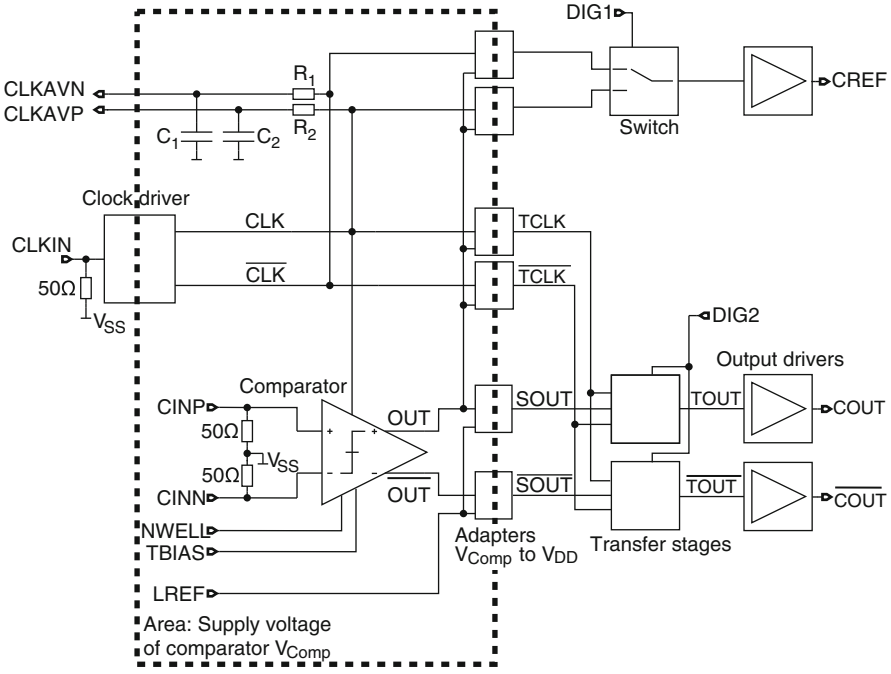

Fig. 8.9 Block diagram of the test chip containing the comparator to be measured

CLKAVN is a measure for the duty cycle. The adapters convert the logical levels V_{Comp} and V_{SS} to levels $V_{DD} = 1.5\,\mathrm{V}$ and $V_{SS} = 0\,\mathrm{V}$. During reset of the comparator the decision is held in the transfer stages. With a digital switch, controlled by pin *DIG*1, signals *CLK* or $\overline{CLK}$ can be checked at output CREF. The output drivers are in

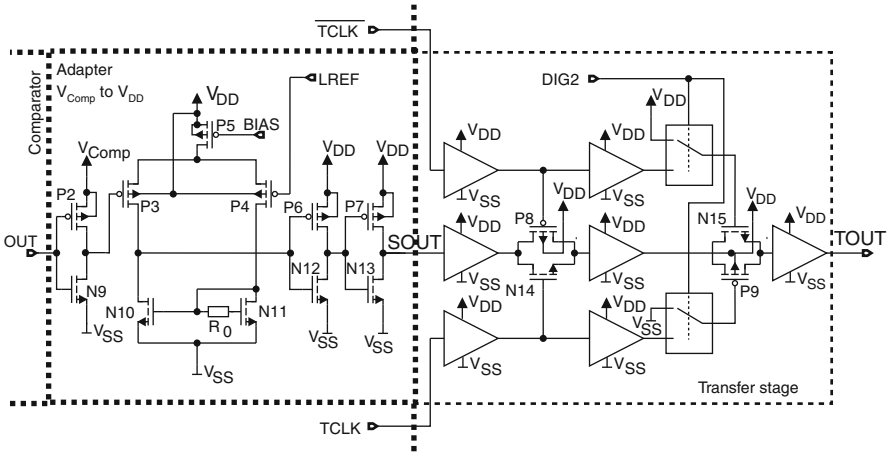

Fig. 8.10 Schematic of the adapter and block diagram of the transfer stage

principle a chain of inverters and are capable to drive a 50 Ω off-chip measurement system. The schematic of the adapter with the following block diagram of the transfer stage is depicted in Fig. 8.10. At the output of a buffer-inverter, which consists of transistors N9 and P2 and which is supplied by V_{Comp}, a differential amplifier (transistors P3, P4, P5, N10, N11 and resistor R_0) compares the logic signal with a voltage LREF. The difference is amplified so that the resulting output voltages are compatible to the logic levels of the following inverter, consisting of transistors N12 and P6 and which is supplied by V_{DD}. LREF is a DC bias voltage and is applied and adjusted from outside the chip. Resistor R_0 enhances somewhat the bandwidth of the differential amplifier. During reset phase of the comparator the decision of the previous comparison phase is held dynamically in the transfer stage at the output of the first transmission gate (transistors N14 and P8) at the gates of the following buffer. With the digital pin *DIG*2 it can be chosen, whether the second transmission gate (transistors N15 and P9) is always switched on or connected to the clock, where it is only switched on, when the first transmission gate (transistors N14 and P8) is off. With this second possibility a constant overall delay time in relation to the clock is achieved to avoid adjusting the optimal delay time in the BER analyzer station for every measurement, because the comparator's decision time depends on several parameters, e.g. the input voltage difference. In the last case, where both transmission gates are turned on and off inversely the output signal of the comparator is additionally delayed by half of the clock period in the transfer stage.

Monte Carlo simulations of the standard deviation of the offset of the comparator have the results of $\sigma_{OS} = 22.1$ mV for the case of $V_{Comp} = 1.5$ V, $TBIAS = 1$ V and 0.75 V input common-mode voltage and $\sigma_{OS} = 46$ mV for the case of $V_{Comp} = 0.5$ V, $TBIAS = 0.5$ V and 0.4 V input common-mode voltage.

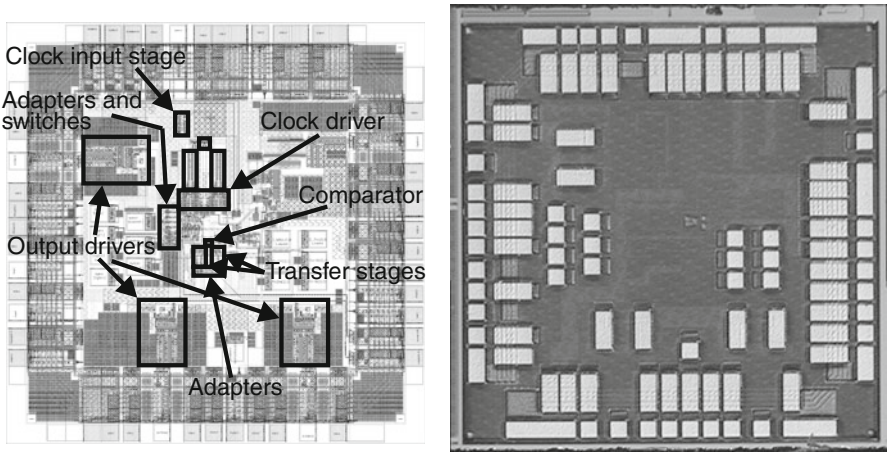

Fig. 8.11 Layout plot and microphotograph of the test chip ($1.38 \times 1.39\,\text{mm}^2$) with the comparator

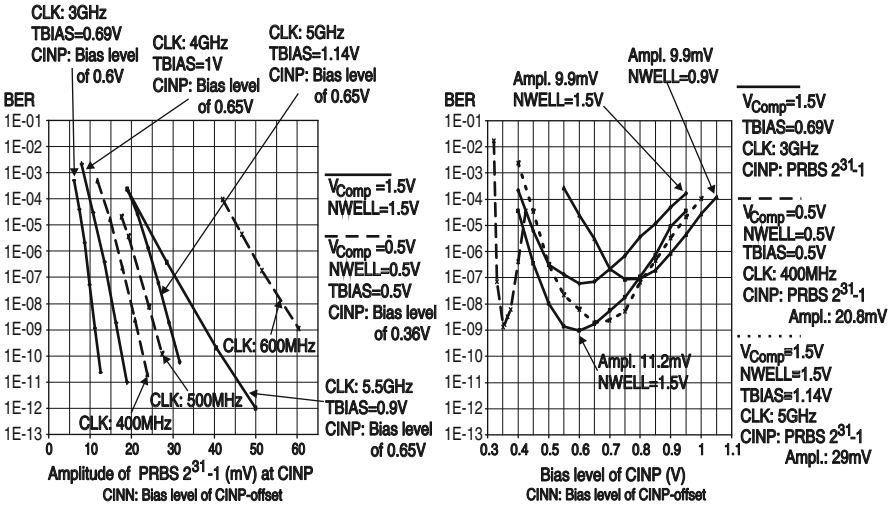

Fig. 8.12 BER measurements: On the *right side* the measured BER versus the bias level at *CINP* is shown and on the *left side* BER measurements versus the amplitude at the optimal operating point at different parameters are shown

The test chip has been fabricated in a 0.12 µm CMOS technology with 1.5 V nominal supply voltage. A layout plot and a microphotograph of the test chip can be seen in Fig. 8.11. The area of the whole test chip amounts to $1.38 \times 1.39\,\text{mm}^2$. Thereof $22 \times 21\,\mu\text{m}^2$ is dedicated to the comparator.

BER measurements were done by applying a bias voltage at *CINP*, which was superimposed by a 2^{31}-1 pseudo-random-bit-sequence (PRBS). In Fig. 8.12 on the right side the measured BER versus the bias level at *CINP*, which is similar to the input common-mode voltage, at different clock frequencies, supply voltages

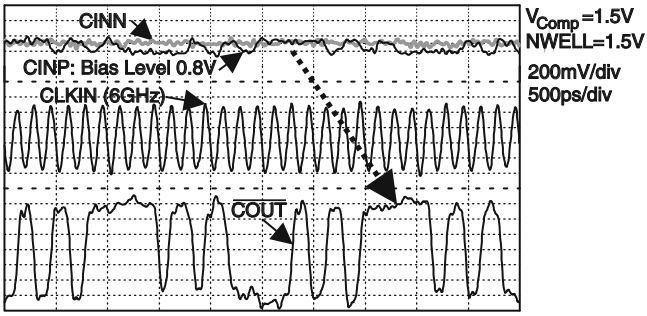

Fig. 8.13 Measured transient behavior at 6 GHz

and amplitudes of PRBS $2^{31}-1$ are shown. The amplitude is defined here with $CINP-(CINN+offset)$, because during measurements *CINN* and *CINP* were biased separately to compensate for the offset of the comparator. In Fig. 8.12 (right side) it can be seen, that every curve has a working point at a bias level of *CINP*, e.g. 0.6 V at 1.5 V supply and 3 GHz clock, where the BER is optimal. For fine-adjustment the bias voltage at NWELL can be lowered, which typically shifts this point to a higher input common mode level due to the back-gate effect. At the left side of Fig. 8.12 some BER measurements versus the amplitude of PRBS $2^{31}-1$ at the optimal working point for different parameters are shown. To achieve a better BER the input amplitude has to be raised, e.g. more than 21.2 mV are needed for a BER better than 10^{-9} at 0.5 V/400 MHz. The measured comparator worked down to a supply voltage of $V_{Comp}=0.5$ V with a maximal clock frequency of 600 MHz consuming 18 µW. For a BER better than 10^{-9} a minimal amplitude of 60.5 mV at 600 MHz, 25.8 mV at 500 MHz and 21.2 mV at 400 MHz has to be applied to the comparator. At a supply voltage of $V_{Comp}=1.5$ V these values are 38 mV at 5.5 GHz, 29.4 mV at 5 GHz, 16.5 mV at 4 GHz and 11.2 mV at 3 GHz. At 6 GHz a BER of 10^{-6} is achieved at an amplitude of 150 mV. The comparator has a power consumption of 2.65 mW at $V_{Comp}=1.5$ V with an operating clock of 6 GHz and 2.17 mW at $V_{Comp}=1.5$ V with an operating clock of 4 GHz, which was measured at a separate pad to supply the comparator of the test chip. A measured oscilloscope picture can be seen in Fig. 8.13 at a clock frequency of the comparator of 6 GHz.

8.6 Delay Time Reduction for a Comparator in 65 nm CMOS Technology for Supply Voltages Down to 0.65 V

The comparator circuit shown in Fig. 8.6a is a widely used standard circuit with rail-to-rail output swing, with high-impedance input and no static power consumption. Furthermore this circuit has the advantage of a good robustness against noise and mismatch, because among other reasons it can be also designed with large

input transistors N2, N3 e.g. to minimize the offset, where their larger parasitic capacitances do not directly affect switching speed, which depends primarily on the load capacitances at the output nodes OUT and $\overline{OUT}$. Disadvantageous is the fact that due to the many stacked transistors a sufficient high supply voltage is needed for a proper delay time [19]. In low-voltage UDSM-CMOS technologies this may cause problems, where even a stand-alone latch (e.g. used in [19]) as shown in Fig. 8.2 with its two cross-coupled inverters, suffers on a higher delay-time, if the supply voltage is reduced or if a low-power process with higher transistor threshold-voltages is used. For the standard comparator in Fig. 8.6a, after the reset phase the initial condition of the comparison phase is $OUT = \overline{OUT} = V_{DD}$. So at the beginning of decision only transistors N0 and N1 of the latch contribute somewhat to positive feedback until the voltage level of one output node has dropped enough to turn on transistor P0 or P1 to start complete regeneration.

To solve these problems a proposed comparator design with a modified latch is presented [22], where the latch of the conventional circuit in Fig. 8.6a has been replaced by a new latch for low supply-voltage operation, where the advantages of the resulting comparator circuit are again a high-impedance input, a rail-to-rail output swing, no static power consumption and non-direct influence of parasitic capacitances of the input transistors on the output nodes and therefore to switching speed have been kept. The circuit of a comparator with a modified new latch is shown in Fig. 8.14, where in opposite to the conventional latch used in Fig. 8.6a, where only N0 and N1 are initially on, the latch of the proposed comparator is expanded into two paths between the supply rails (transistors N0, N1, P0, P1, P4, P5). So at the beginning of the comparison phase, where both output nodes have the initial condition $OUT = \overline{OUT} = V_{Comp}$, transistors N0, N1 are turned on. But also transistors P0, P1 are turned on and build together with the input transistors N2 and N3 an amplifier with a distinct operating point. Finally the complete positive feedback is done with N0, N1, P0, P1, where P4 and P5 help with additional amplification. The advantages of a high-impedance input, a rail-to-rail output swing, no static power consumption and no direct influence of parasitic capacitances of N2, N3 to the output nodes are kept. A clock period is divided into a reset phase and a comparison phase, where the voltage at $CINP$ is compared with that at $CINN$. In the reset phase ($CLK = V_{SS}$) an initial condition $OUT = \overline{OUT} = V_{Comp}$ for the following comparison phase ($CLK = V_{Comp}$, V_{Coomp} is the positive supply voltage of the comparator) is established. During reset, transistor N6 is switched off and transistors P2, P3, N4 and N5 are on. Consequently the output nodes OUT and $\overline{OUT}$ are pulled towards V_{Comp} by reset transistors P2 and P3. This causes transistors P4 and P5 to be switched off. Reset transistors N4 and N5 are switched on and pull both internal nodes FB and $\overline{FB}$ to V_{SS}. As a consequence transistors P0 and P1 are turned on and help pulling OUT and $\overline{OUT}$ to the final voltage level V_{Comp}. Comparison of the input voltages $CINP$ with $CINN$ is started, when CLK switches to voltage level V_{Comp} (comparison phase) thus transistor N6 is turned on and P2, P3, N4 and N5 are turned off. At the very beginning, transistors P4, P5 are switched off, transistors P0 and P1 work in linear region and act as load for an amplifier

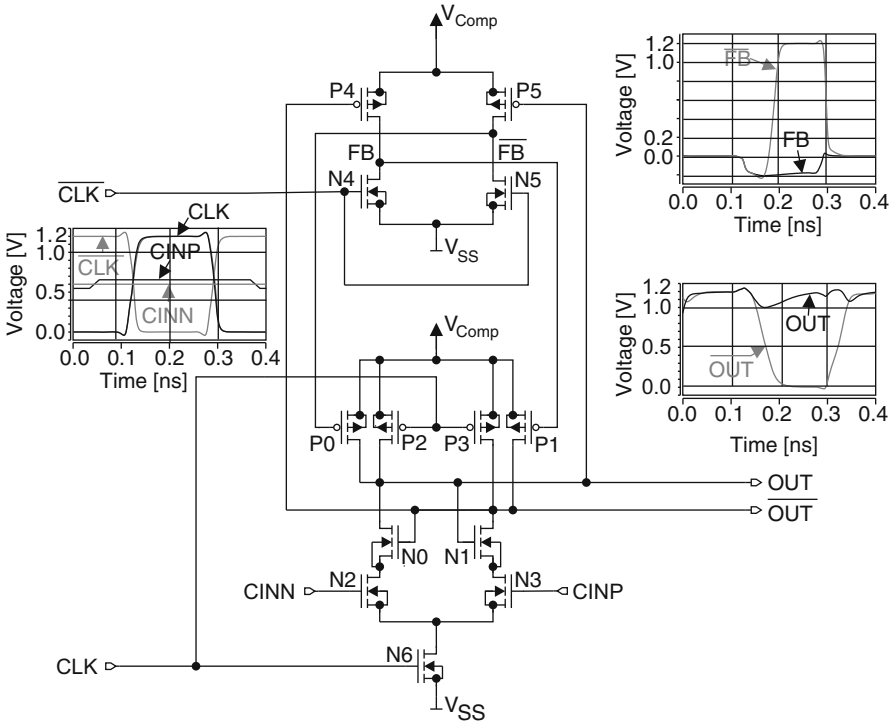

Fig. 8.14 Circuit of the comparator with the modified latch

with N2, N3. Transistors N0 and N1 are initially on (initially $OUT = \overline{OUT} = V_{Comp}$ and $FB = \overline{FB} = V_{SS}$). Assuming that the voltage at $CINP$ is larger than the voltage at $CINN$, then transistor N3 pulls the voltage level at output node $\overline{OUT}$ down faster than N2 does it at output node OUT. As a consequence transistor P4 begins to conduct when the potential at $\overline{OUT}$ becomes smaller than $V_{Comp} - |V_{tP4}|$, where V_{tP4} is the threshold voltage of P4. In this initial time period also a small amount of positive feedback is contributed by transistors N0 and N1. When P4 begins to conduct, node FB is charged towards V_{Comp} (N4, N5 are off) and finally complete positive feedback is started. Transistor P1 is turned off and P0 keeps conducting, because of node OUT is pulled to V_{Comp} thus P5 keeps off and remains near V_{SS} (The input voltage difference $CINP - CINN$ is assumed to be sufficient). When comparison has finished, transistors N1, P4 and P0 are switched on and N0, P1 and P5 are turned off. Output node OUT is at voltage level V_{Comp} and $\overline{OUT}$ at V_{SS}. No static current can flow after decision. When considering the other case of $CINP > CINN$, OUT is pulled to V_{SS} and $\overline{OUT}$ to V_{Comp} respectively.

For comparison of the decision times at different supply voltages of the proposed comparator containing the modified latch of Fig. 8.14 with the conventional comparator of Fig. 8.6a have been simulated and are shown in Fig. 8.15. Both comparators were designed in a similar way so that the decision time (50% clock

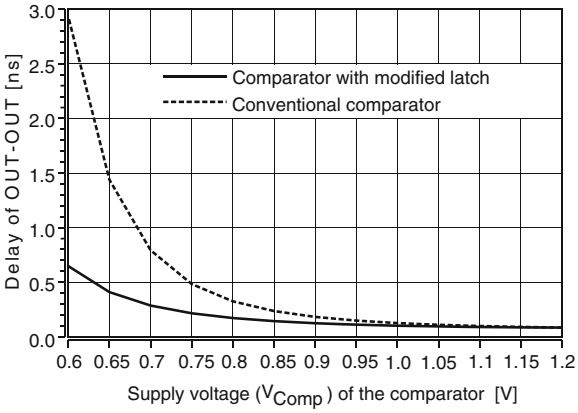

Fig. 8.15 Comparison of the decision time of the conventional comparator in Fig. 8.6a with the proposed comparator containing the modified latch in Fig. 8.14 versus their supply voltage. The decision time is defined here as the time duration between 50% of the rising clock edge and 50% of final output voltage difference $OUT - \overline{OUT} = V_{Comp}$

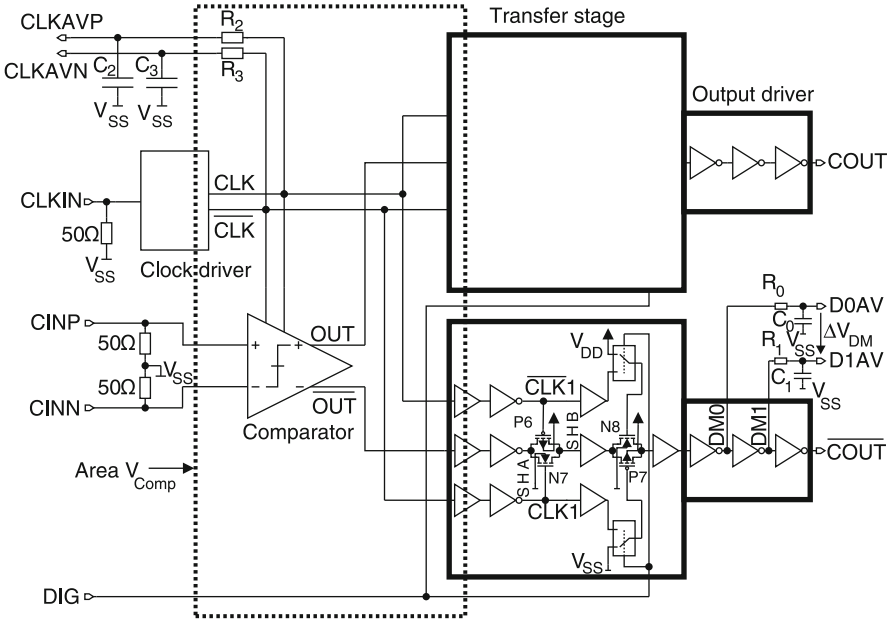

Fig. 8.16 Block diagram of the test chip including the comparator

edge to 50% of final output voltage difference $OUT - \overline{OUT} = V_{Comp}$) is equal for $V_{Comp} = 1.2\,\text{V}$ and same input conditions. For example at a supply voltage of $V_{Comp} = 0.6\,\text{V}$, the proposed comparator containing the modified latch needs only 650 ps instead of 2.95 ns of the conventional comparator. Therefore the comparator with the modified latch is capable of low-voltage operation.

The block diagram of a test chip with the proposed comparator, which is designed in a 65 nm low-power CMOS technology with a nominal supply voltage of $V_{DD} = 1.2\,\text{V}$ is shown in Fig. 8.16. The dotted rectangle marks an area, which

is supplied separately with a voltage V_{Comp} to be able to investigate the behavior of the comparator when V_{Comp} is lowered. Outside of this area a supply voltage of the nominal $V_{DD} = 1.2\,\text{V}$ is applied to have always functionality of additional measurement circuitry for characterization of the implemented comparator. With the help of the clock driver a non-inverted digital clock *CLK* and the appropriate inverted clock $\overline{CLK}$ is generated, where the voltage levels change between V_{Comp} for logic high and V_{SS} for a logic low. Generation of an on-chip clock signal is done by applying a sine-wave, where the frequency defines the on-chip clock frequency and the DC bias voltage level defines the duty cycle to pad *CLKIN*. For adjusting the duty cycle, the RC low-passes R_2, C_2 and R_3, C_3 are added to measure the mean voltage (corresponding to duty cycle) of the internal clock lines *CLK* and $\overline{CLK}$ at pads *CLKAVP* and *CLKAVN*, respectively. All high frequency inputs *CLKIN*, *CINP* and *CINN* are terminated with on-chip 50 Ω resistors to match the off-chip lines. The transfer stage is built in a similar way as described in Sect. 8.5, where *DIG* has the same function as *DIG*2 in Fig. 8.9. In the transfer stage adapter are added, which are a chain of two inverters, where each inverter is supplied separately for stepwise increasing the supply voltage from V_{Comp} to $V_{DD} = 1.2\,\text{V}$. The output drivers consist of a chain of inverters and are able to drive off-chip 50 Ω measurement equipment. Additionally RC low-passes R_0, C_0 and R_1, C_1 have been added at the output driver with which in addition with the transfer stage the delay time t_d of the comparator can be measured [22]. The delay time t_d is here defined as the time duration, which begins at the time point, when the voltage level has reached 50% of V_{Comp} at the rising edge of CLK to the time point, when $\overline{OUT}$ has fallen to the switching threshold of the following inverter (≈50% of V_{Comp}) in the case of $CINP > CINN$.

For test purposes a chip with an area of $930 \times 500\,\mu\text{m}^2$ was fabricated in a low-power 65 nm/1.2 V CMOS technology. Thereof $28.4 \times 49.1\,\mu\text{m}^2$ is dedicated to the comparator. Due to Monte-Carlo simulations a run of 50 samples revealed, that the standard deviations of the offset are 1.9 mV @ $CINN = 0.6\,\text{V}$ ($V_{Comp} = 1.2\,\text{V}$), 4 mV @ $CINN = 0.55\,\text{V}$ ($V_{Comp} = 0.75\,\text{V}$) and 6.1 mV @ $CINN = 0.5\,\text{V}$ ($V_{Comp} = 0.65\,\text{V}$). The influence of noise to the decision of the comparator and thus the sensitivity can be characterized with the help of statistical measurements by measuring the BER with an appropriate pattern generator and receiver. At *CINN* a reference voltage and at *CINP* a PRBS $2^{31} - 1$ were applied, which was superimposed to a bias voltage of $CINN + offset$ to compensate the offset of the comparator. The amplitude of a bit-sequence is defined here, that the bit-sequence switches at $CINP \pm amplitude$ around voltage level $CINN + offset$, while at CINN the reference voltage is applied. Measured BER results of a typical test chip are shown in Fig. 8.17. To achieve a $\text{BER} = 10^{-9}$ at 1.2 V supply, an amplitude of 7.8 mV at 3 GHz, 16.5 mV at 4 GHz and 145 mV at 5 GHz had to be applied. If V_{Comp} is lowered, 7 mV at 1 GHz/0.75 V, 6.9 mV at 0.5 GHz/0.65 V and 12.1 mV at 0.6 GHz/0.65 V have been measured. The results of the mean delay time of the comparator, which has been determined by a measurement of ten chip samples, where an on-chip implementation for measuring of the delay time has been used [22], are shown in Fig. 8.18. For an amplitude of e.g. 15 mV at the input of the comparator the mean delay times ($\sigma \approx 7\,\text{ps}$) were 93 ps at $CINN = 0.65\,\text{V}$,

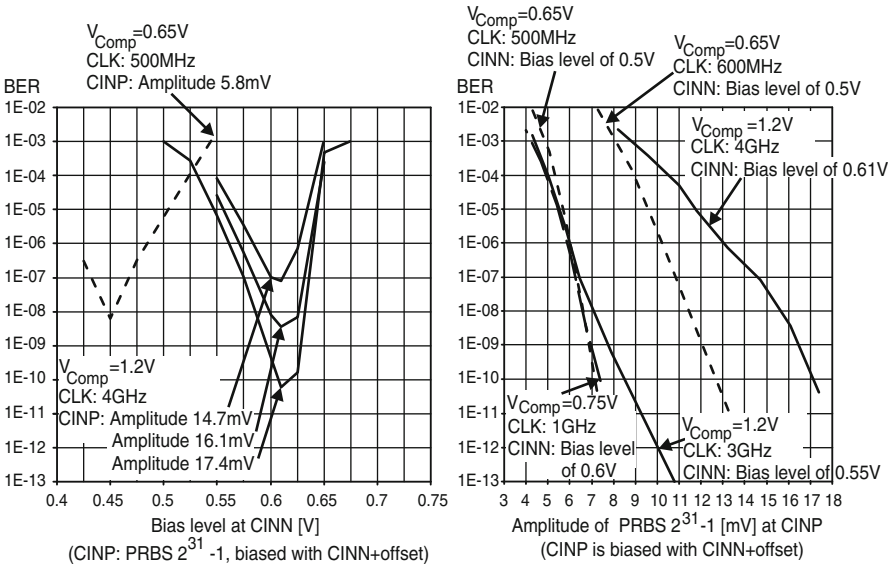

Fig. 8.17 BER measurements: On the *left side* the measured BER versus the bias level at *CINP* is shown and on the *right side* BER measurements versus the amplitude nearby the optimal operating point at different parameters are shown

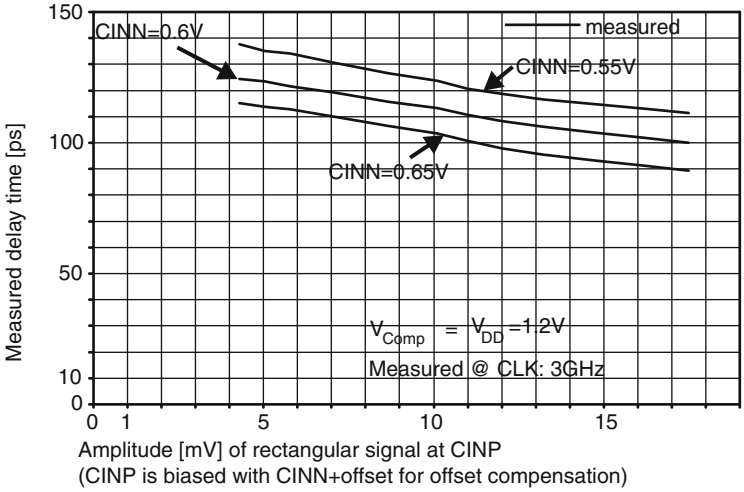

Fig. 8.18 Delay time measurements

104 ps at $CINN = 0.6\,\mathrm{V}$ and 115 ps at $CINN = 0.55\,\mathrm{V}$ at $V_{Comp} = 1.2\,\mathrm{V}$. The measured power consumption of the comparator is 2.88 mW at 5 GHz (1.2 V supply voltage), 295 µW at 1 GHz (0.75 V supply voltage), 128 µW at 0.6 GHz (0.65 V supply voltage).

8.7 Conclusion

An important element in ADCs, but also in other applications, like e.g. in sense amplifiers in SRAMs or for data regeneration, is the comparator. It compares an input signal with a reference voltage and has as a result a logical stage, which indicates whether the potential is lower or higher than a reference potential. In fast ADCs, e.g. in a flash ADC or a folding converter system, mostly many parallel comparators of the clocked and regenerative type are implemented, which work in parallel. Modern UDSM CMOS processes are optimized for implementing as many logic gates as possible per area with a minimum of power consumption thus the structure sizes are small. Therefore the design of analog circuits has to deal with this circumstances, e.g. a low supply voltage, gate tunnel currents and nonideal transistor characteristics. Especially for e.g. mobile devices, circuits are demanded, which work even at a low supply voltage. In this chapter comparators for UDSM CMOS technologies have been described, e.g. a comparator in a 0.12 µm/1.5 V-low-V_t CMOS technology, which works down to a supply voltage of 0.5 V with 600 MHz clock frequency with 18 µW power consumption or a comparator in a 65 nm/1.2 V low-power CMOS-process, which is capable of operating down to 0.65 V at 600 MHz clock thus consuming 128 µW power.

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Chapter 9
Low-Power Electronics for Biomedical Sensors

Syed Kamrul Islam, Fahmida Shaheen Tulip, Kai Zhu, and Melika Roknsharifi

9.1 Introduction

Long-term reliable detection of various biological signals in biomedical applications requires excellent signal sensitivity and adequate power savings. Integration of sensors and modern integrated circuit (IC) technology offers rapid and reliable identification and analysis of the biological signals. However, due to tremendous diversity of the biological samples and the complexity associated with the analysis of these samples, implementation of a biomedical sensor system requires a highly challenging task of integration of sensor technology with sophisticated data analysis techniques. Accurate detection and classification of microanalytes or microorganisms using classical laboratory-based techniques is time consuming and cumbersome. Early detection and characterization of microanalytes not only help minimizing potential biohazards but also prevent spreading of life-threatening contagious diseases. Reliable identification and characterization of the biological samples thus require robust, low cost, rapid sensing, and high throughput capability of the sensor system along with portability of the devices for field applications.

The evolution of sophisticated micro- and nano-fabrication processes have led to the development of various miniature, light-weight, cost-effective and energy-efficient sensors for biomedical applications such as monitoring of glucose [1–3], lactate [4], pH [5], carbon dioxide (CO_2) [6], oxygen (O_2), etc. The integration of the sensor technologies with low-power signal processing electronics resulted in the development of implantable sensors for various biomedical applications such as visual prosthesis for the blind [7], cochlear implant for the deaf [8], neuromuscular stimulator for the brain [9], capsule endoscopy [10], gastrointestinal microsystems [11] etc. Electronic circuits mimicking biological systems have also been reported [12]. Bio-inspired electronic systems such as bionic ear or RF cochlea which

S.K. Islam (✉) • F.S. Tulip • K. Zhu • M. Roknsharifi
The University of Tennessee, Knoxville, TN
e-mail: ftulip@utk.edu; kzhu3@utk.edu; mroknsha@utk.edu

E. Tlelo-Cuautle (ed.), *Integrated Circuits for Analog Signal Processing*,
DOI 10.1007/978-1-4614-1383-7_9,

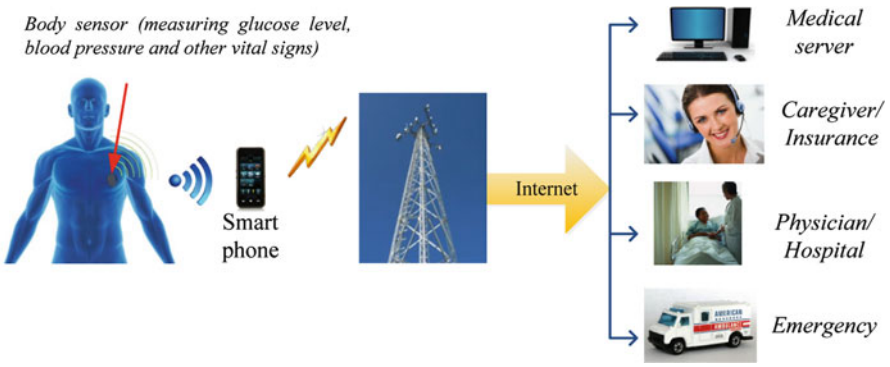

Fig. 9.1 An overview of wireless body area network (WBAN) based patient monitoring system

have computation capabilities equivalent of 1 GFLOPS of spectral-analysis and gain-control computations with 14 μW of power on a 150 mV battery have been reported [13]. Wee et al. reported a 275 μW silicon vocal tract designed to be used with auditory processors [14]. An energy efficient (0.12 pJ per quantization level) analog-to-digital converter (ADC) inspired by the performance of spiking neurons in pattern recognition with time rather than with voltage or current have been reported by Yang et al. [15]. In addition, micro electro mechanical systems (MEMS) have also been used for biological applications such as delivery of potent drugs or hormones in the area of nervous and endocrine system actuation and detection of anthrax simulants [16, 17]. Neural network based adaptive information processing has also been proposed [18]. Low power electronic devices are gaining increasing importance in biomedical applications. These devices are used for diagnostic as well as therapeutic applications. Due to recent development in data acquisition systems and novel sensing materials, use of smart sensors for point of care application has become a reality.

Emerging sensor technologies combined with the tremendous development in IC process technologies and wireless networks have resulted in a low-power sensor platform known as wireless body area network (WBAN) [19]. This wireless based patient monitoring system for a comprehensive healthcare alternative provides early detection of abnormal conditions and prevention of serious consequences. This system employs a number of different sensors to monitor various physiological phenomena and the sensor data is wirelessly transmitted to a server computer which communicates with the central database via internet. The data is monitored and stored in the central database and based on the sensor data proactive measures could be initiated by healthcare providers. An overview of this system is illustrated in Fig. 9.1.

9.2 Classification of Biosensors

Generally, all biosensors can be classified as either physical or chemical. Physical biosensors measure parameters such as muscle displacement, blood pressure, core body temperature, blood flow, cerebrospinal fluid pressure etc. Chemical biosensors are employed to identify and measure the quantity of specific chemical compounds, detect the concentrations of various chemical species and monitor chemical activities in the body. Examples of different types of chemical sensors include gas, electrochemical, photometric and bioanalytic sensors. However, the bioanalytic sensors are often classified as a separate sensor category due to their importance and diversity. Bioanalytic sensors incorporate biorecognition reactions such as enzyme-substrate, antigen-antibody or ligand-receptor to identify complex biochemical molecules [20].

Depending on sensor-substrate interface, biosensors can be classified as follows:

1. Non-contacting (Non-invasive)—Sensor that does not contact the subject being measured.
2. Skin-surface (Contacting)—Sensor which comes in contact with the skin surface temporarily.
3. Indwelling (Minimally invasive)—Sensor which is permanently secured with the subject but not implanted.
4. Implantable (Invasive)—Sensor which is implanted in the body cavity or underneath the skin.

Biosensors are employed in biomedical systems for patient care in hospitals, home, and even in some workplaces. A brief description of applications for healthcare applications is provided below:

1. *Wireless Hospital Network*: Inside the hospital, biosensors are used to monitor inpatients such as bedside monitoring, triage etc. These types of sensors collect data 24/7 and are usually designed to notify the healthcare workers when certain set alarm levels are reached.
2. *Home Care Monitoring*: Besides monitoring critical patients inside the hospitals, biosensors are also used to measure various physiological parameters during personal exercise at home to ensure the best self-management and motivation.
3. *Rehabilitation*: Biosensors can go a long way to help patients with chronic health conditions such as heart disease, Alzheimer's disease and diabetes to maintain active lifestyles. These patients need constant monitoring of their vital signs and immediate help in case of emergency.
4. *High-Risk Workers*: For high risk workers such as firemen, astronauts, or people working in any high risk environment such as extreme cold or hot climates, mine etc. The monitoring of vital signs is of utmost importance and could possibly be the difference between life and death.

Top ten targets for wireless health, as was identified in TEDMED 2009, are listed in Table 9.1 [21].

Table 9.1 Top ten targets for wireless medicine

Disease	Affected US population (millions)	Wireless solutions
Alzheimer's	5	Vital signs, location, activity, balance
Asthma	23	RR, FEV1, air quality, oximetry, pollen count
Breast cancer	3	Ultrasound examination
COPD	10	RR, FEV1, air quality, oximetry
Depression	21	Med. compliance, activity, communication
Diabetes	24	Glucose, Hemoglobin A1C, activity
Heart failure	5	Cardiac pressures, weight, BP, fluid status
Hypertension	74	Continuous BP, Med. compliance
Obesity	80	Smart scales, glucose, calorie in/out, activity
Sleep disorder	40	Sleep phases/quality, vital signs

9.3 Applications of Biomedical Sensors

9.3.1 BioChem Lab-On-A-Chip: Smart Sensor

Combining sensing devices with integrated signal-processing and telemetry circuits develops smart sensors. In most cases, multiple sensors are placed on a single chip to monitor various physiological parameters which are controlled by employing control signal from the integrated sensor select circuits; thereby making possible the realization of a lab-on-a-chip scheme. These sensors take advantage of the existing sensor technology, microfluidics and inexpensive CMOS integrated circuits and thus allow large-scale deployment. Figure 9.2 shows a lab-on-a-chip prototype for detection of bacteria [22]. The chip incorporates various functionalities including in situ analysis, DNA isolation and polymerase chain reaction (PCR).

9.3.2 Artificial Retina

A prosthetic retina prototype has been developed under the smart sensors and integrated microsystems (SSIM) project at Wayne State University and the Kresge Eye Institute to provide people without vision or with limited vision with sufficient visual functionality to allow them to "see" at an accepted level.

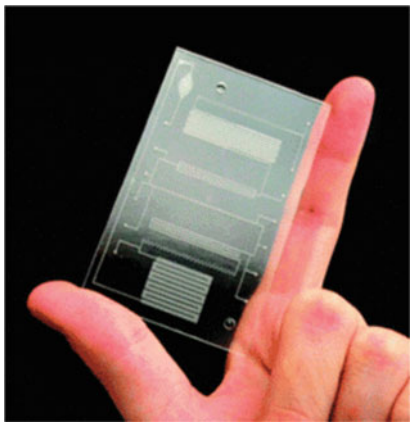

Fig. 9.2 A lab-on-a- chip for integrated detection of bacteria including analysis, DNA isolation and PCR [22]

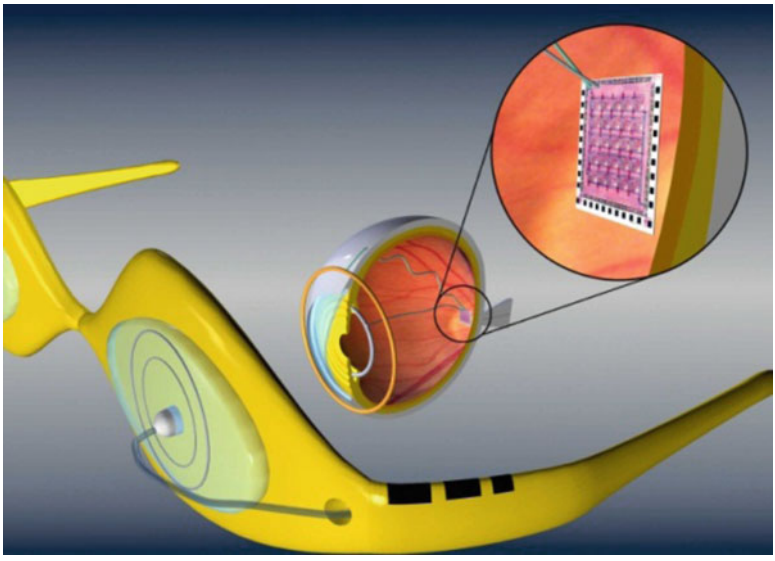

Fig. 9.3 Location of smart sensor within the eye [24]

This therapeutic sensor has two components, an IC and an array of sensors which are placed upon the retina. The electrical signals generated by the sensors are converted into chemical signals mimicking the normal operating behavior of the retina from light stimulation.

As shown by Fig. 9.3, the front side of the retina is in contact with a microsensor array. The backside of the retina is stimulated electrically via artificial retina prosthesis. The electrical signal is then converted to chemical signals by the underlying tissue structure and carried to the brain via optic nerve, thus providing signal transmission into the eye. Signal transmission from the eye works in a similar

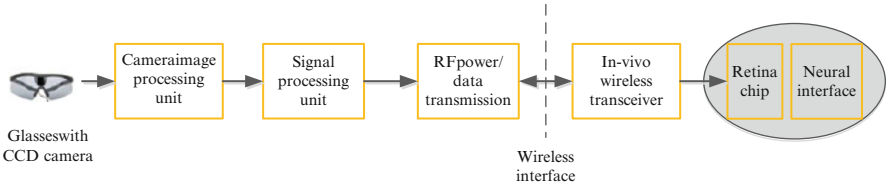

Fig. 9.4 Processing steps for retina prosthesis project [25]

manner, but only in the reverse direction, providing a feedback system within the eye. Figure 9.4 depicts the processing steps from external image reception to transmission to artificial retina prosthesis. A camera mounted on an eyeglass frame feeds its output to a DSP unit for data reduction and processing. The camera is combined with a laser pointer for automatic focusing. The DSP unit transmits the processed data via wireless transceiver system to the implanted chip in the eye for subsequent decoding. Figure 9.4 shows a wireless transceiver setup inside the human body, but not within retina.

9.3.3 Glucose Level Monitor

According to US National Institute of Health (NIH), 8.3% of total US population is affected by diabetes in 2010 [26]. The percentage was 5.9% in 1999 [25]. Diabetes is also responsible for complications such as heart disease, stroke, high blood pressure, blindness, kidney disease, and amputations. Current monitoring of blood glucose level requires pricking the finger with a lancet to collect a drop of blood that is analyzed either manually or electronically. The constant pricking of the same area over a period of years can damage the underlying tissue and the blood vessels. A wireless sensor implanted underneath the skin of the patient can constantly monitor blood glucose level without the need to frequent finger pricking as mentioned above. These implantable sensors represent minimally invasive methods of detection of glucose and other metabolites in the human body. A non-invasive wearable device known as "GlucoWatch" based on the coupling of reverse iontophoretic collection of glucose and biosensor functions has been developed by Cyngus Inc. [23] as shown in Fig. 9.5. The device provides up to three glucose readings per hour for up to 12 hours. The system has demonstrated the capability of measuring the electro osmotically extracted glucose with a clinically acceptable level of accuracy.

9.3.4 Organ Monitor

In 2011, more than 112,000 people were waiting for an organ donation in the US [27]. In 2001, this number was over 75,000 [25]. Unfortunately, a large number of

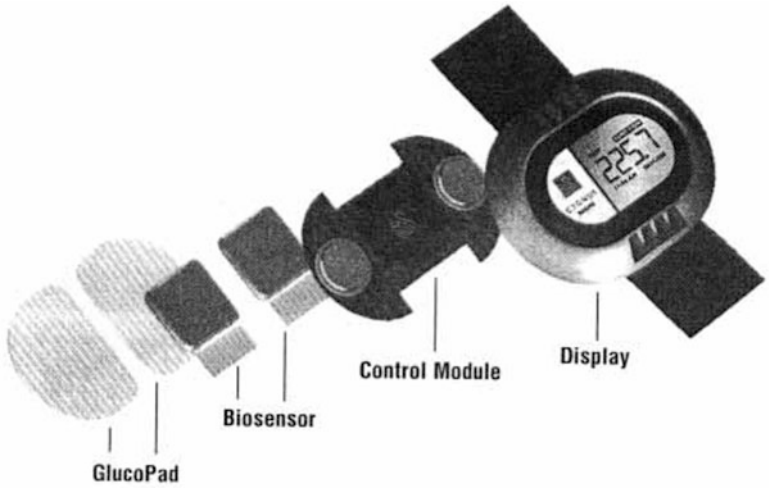

Fig. 9.5 Components of a watchlike glucose monitor being developed by Cygnus Inc [23]

the donated organs go unused as there is a very short window of time in which to transplant the organ before it becomes no longer viable. A better understanding of the condition of the organ could lengthen this window. Moreover, organ rejection after transplant is also a serious issue. Continuous monitoring of the patient after the transplant for symptoms of rejection is crucial. Biosensors can be employed for the monitoring of the condition of the donated organs as well as the symptoms of the rejection of the transplanted organs.

9.3.5 Cancer Detector

In 2011, 571,960 people are expected to die of cancer in the US, with 1,596,670 new cases diagnosed [28]. In 1999, the number of new diagnosed cases was 1,221,800 [25]. As of yet, there is no conclusive findings on the prevention of this disease. As such, early detection is the key to survival. Several unique cellular morphology and molecular signature events change during cancer development and progression processes. By discerning these changes accurately with the help of biomarkers early and accurate detection and diagnosis of the disease is possible.

9.3.6 General Health Monitor

In general, biosensors can be employed to monitor health conditions of patients as well as healthy persons. NASA has been working on several different biotechnology

and bioinstrumentation sensor systems to support life sciences research during space flight and ground based studies [25].These smart sensors can provide vital information about digestive or cardiac system of the astronauts.

9.4 Challenges Associated with Biosensors

Intelligent systems are required for the analysis of multi-parametric data. In addition, the multi-parametric data must be correlated with established biomedical knowledge to derive clinically relevant indicators. The challenges associated with biosensor applications are summarized below:

1. The sensors must provide accurate alerting and signaling of the risk to support healthcare professionals in their decision making.
2. New indicators should be identified for predicting or diagnosing of the worsening conditions at early stages and for prompting early intervention.
3. Absence of wires restricts the power requirements of wireless sensors. One way to supply the constant source of power is to use an integrated battery. But even with conservationist techniques, replacing battery as often as required might not be a suitable solution. Another way is to use passive power sources, such as solar and vibration, which provide insufficient power for constant operation. This leads to an external, wireless power source to be the only solution.
4. As the power becomes limited, the computation is also limited. The amount of computation possible with a low power biomedical sensor is significantly less than that of a generic sensor. One way to work around this problem is to transmit the data to an external data processing device.
5. Sensors implanted in the body will have shape, size and material constraints. Human immune system is designed to reject foreign substances. Therefore, the sensor must be encased in biocompatible materials which act as the barrier between the body fluids and the sensor components. The biocompatible material must not hinder the operation of the sensor. Moreover, if the body rejects the implant, the functionality of the sensor can be adversely affected, which must be taken into consideration.
6. Implantable sensors are expected to last a long time, usually in the range of decades. As such, the sensor must be extremely robust and fault tolerant. In particular, the failure of one node should not cause the entire circuit to cease operation. The best method to ensure this is to have a distributed network.
7. In order to ensure functionality with low-power and confined area constraints, several small sensors may need to be placed in close proximity and are required to work in conjunction with each other. With multiple sensors communicating among themselves and with the external device, efficient use of the wireless spectrum is required.
8. Although it is important that the physician and the patient have accesses to the data received from the sensors, the information must remain secured to ensure patient confidentiality. Strict security mechanisms must be put in place to prevent outside interference.

9. There must be some proof that these devices will not harm but potentially help the test subjects. The prototypes must maintain strict standards for human safety before any human testing is done. Their testing and use must be regulated by the Food and Drug Administration (FDA).

9.5 Low-Power Circuit Design

Low-voltage (LV), low-power (LP) circuit design techniques require careful consideration of the device behavior and the circuit topologies in order to meet the associated design challenges. Wouter A. Serdijn et al. [29] have identified the following design aspects with significant influences on the overall transfer quality for low-power system design:

1. System requirements,
2. Signal processing,
3. Indirect feedback,
4. Choice of information-carrying signal, and
5. Parasitics.

For the input and the output of the system, the best representative signal such as the voltage or the current or the flux of the external physical quantity must be chosen so that there is almost a linear relationship between the electrical signal and the physical quantities [30]. In general, current becomes more favorable than voltage as the information-carrying quantity in a low-voltage low-power environment [29]. However, as the voltage signals can be easily distributed among different blocks by simply connecting the input terminals of all the blocks in parallel, it is a better option if a signal needs to be transmitted to different circuit blocks within the system. Whenever the system handles the information coming from several sensors or transducers, the current is a better choice as the information-carrying quantity compared to the voltage. This is due to the fact that the information coming from various transducers in the form of current signals can be easily added by connecting the output terminals of all the transducers in parallel. In addition, for the design of a feedback system for low-voltage operation, indirect feedback is typically more suitable compared to the direct feedback approach. In low-power IC design, parasitic admittances (node capacitances) are often more influential on the signal behavior than the parasitic impedances. As a result by terminating the signal path with low-impedance circuit results in better minimization of the parasitic components of the circuit. “Current-mode”, “switched-current” and “switched transconductance” techniques [31–33] support this argument with their inherent capability to exhibit good high-frequency properties.

The major challenge associated with the low-voltage analog designer is that the threshold voltage and the drain-source saturation voltage do not scale down at the same rate as the supply voltage. In a typical 5 V CMOS process, cascode and regulated cascode structures are used in analog circuit design because of their high

output impedance and hence high voltage gain [34]. However, due to their limited voltage headroom, the cascode structures are not suitable for CMOS processes involving supply voltage below 2 V. Therefore the general trend in low-power designs entails the development of the circuits in horizontal i.e., cascade fashion instead of vertical stacking of the transistors.

However, the cascade structures do not completely resolve the design challenges of low-voltage and low-power circuit design. Each stage can be considered as a parallel block and there is a potential chance of increasing the power consumption even with the low supply voltage. Most importantly, each stage contributes one pole and there is a potential chance of system instability if frequency compensation techniques are not used [35–37].

In can be pointed out that the threshold voltage V_{th} of a MOSFET does not scale down at the same rate as scaling of power supply voltage because of the sub-threshold current consideration in mixed signal environment [38] and the wide spread of V_{th} value for sub-micron technologies [39]. In order to overcome this relatively high threshold voltage and to reduce the overall power consumption, the following low-power circuit design techniques have been reported [40, 41]:

(1) Sub-threshold design
(2) Supply voltage reduction
(3) Bulk-driven MOSFETs
(4) Self-cascode MOSFET
(5) Floating gate MOSFETs

9.5.1 Sub-Threshold Design

MOSFET operating in sub-threshold region offers extremely low-power operation. In sub-threshold region, the drain current (I_{D}) variation with the gate bias voltage of the MOSFET shows exponential behavior and offers higher transconductance efficiency (g_m/I_{D}), which allows the circuit to achieve desired performance in low-power operation. If the applied gate-source voltage is hundreds of millivolts higher than the threshold voltage so that the transistor channel is completely inverted, the transistor is considered to be biased in strong inversion (S.I.). If the gate-source voltage biasing decreases approaching the threshold voltage (V_{th}), then the transistor region of operation is called moderate inversion (M.I.), and if it goes below the threshold voltage then this transistor is considered to be biased in weak inversion (W.I.). Typically when a MOSFET is operating in weak inversion or in sub-threshold region its unity current gain cut-off frequency (f_{T}) deteriorates, thus making the device unsuitable for high frequency applications. However, modern deep submicron CMOS devices have achieved f_{T} values greater than 100 GHz by technology scaling which has made them suitable for analog/RF circuit design even in sub-threshold region.

C.C. Enz et al. [42] introduced the following equation for the drain current of a MOSFET that is valid in all levels of the transistor inversion:

$$I_{\mathrm{D}} = I_{\mathrm{S}}\left[\left(\ln\left(1+\mathrm{e}^{\frac{V_{\mathrm{p}}-V_{\mathrm{s}}}{2U_T}}\right)\right)^2 - \left(\ln\left(1+e^{\frac{V_{\mathrm{p}}-V_{\mathrm{d}}}{2U_T}}\right)\right)^2\right] \tag{9.1}$$

where,

$$I_{\mathrm{S}} = 2n\beta U_T^2 \tag{9.2}$$

and V_{s} is the source voltage of the transistor, V_{d} is the drain voltage of the transistor and V_{p} is the pinch off voltage of the transistor which can be estimated to be:

$$V_{\mathrm{p}} \cong \frac{V_{\mathrm{G}} - V_{\mathrm{T0}}}{n} \tag{9.3}$$

where, n is a function of gate voltage and can be estimated to be 1. The transistor current in (9.1) is defined to be the subtraction of the forward current and the reverse current. Forward current is generated based on the difference between the gate and the source voltages, while the reverse current is generated based on the difference between the gate and the drain voltages.

If the drain-source voltage of the transistor is large enough $[V_{\mathrm{DS}} > (V_{\mathrm{GS}} - V_{\mathrm{th}})]$ then the transistor enters the saturation mode. In S.I. region of operation, saturation occurs when $V_{\mathrm{s}} \leq V_{\mathrm{p}}$ and $V_{\mathrm{d}} > V_{\mathrm{p}}$. In this case the (9.1) can be simplified as shown below:

$$\begin{aligned} I_{\mathrm{D}} &\cong I_{\mathrm{S}}\left[\left(\ln\left(\mathrm{e}^{\frac{V_{\mathrm{p}}-V_{\mathrm{s}}}{2U_T}}\right)\right)^2 - (\ln(1))^2\right] \\ &= 2n\beta U_T^2\left[\left(\frac{V_{\mathrm{p}}-V_{\mathrm{s}}}{2U_T}\right)^2\right] = \frac{n\beta}{2}(V_{\mathrm{p}}-V_{\mathrm{s}})^2 = \frac{n\beta}{2}(V_{\mathrm{GS}}-V_{\mathrm{Th0}})^2 \end{aligned} \tag{9.4}$$

For W.I. region of operation saturation occurs when $V_{\mathrm{s}} > V_{\mathrm{p}}$, $V_{\mathrm{d}} > V_{\mathrm{p}}$ and $(V_{\mathrm{d}} - V_{\mathrm{s}}) \gg V_{\mathrm{p}}$. In this case the (9.1) reduces in to:

$$I_{\mathrm{D}} \cong 2n\beta U_T^2 \mathrm{e}^{\frac{V_{\mathrm{p}}-V_{\mathrm{s}}}{2U_T}} = 2n\beta U_T^2 \mathrm{e}^{\frac{V_{\mathrm{GS}}-V_{\mathrm{Th0}}}{2U_T}} \mathrm{e}^{\frac{V_{\mathrm{p}}-V_{\mathrm{s}}}{2U_T}} \tag{9.5}$$

The other parameter that can be used as a reference for defining the transistor level of inversion is known as inversion coefficient which can be calculated from $(I_{\mathrm{D}}/I_{\mathrm{S}})$ ratio. According to [43], if the inversion coefficient be greater than 10 the transistor is biased in S.I. and if it be less than 0.1 the transistor is biased in W.I.

Using (9.1) and (9.5) one can compare the difference between the behavior of the transistors biased in S.I. and the one that is biased in W.I. Based on (9.5) in W.I. region, the current is a strong function of the temperature. In addition, because

of the exponential relationship between the drain current and the threshold voltage, any small variation in the threshold voltage can cause a large variation in the drain current. Therefore providing a good matching is extremely hard in W.I. reign. In circuits containing current mirrors biasing the transistors in S.I. helps decrease the sensitivity to the threshold voltage mismatch. However, the exponential relationship between the drain current and the gate voltage in W.I. can help achieve higher transconductance efficiency at this level of inversion. Thus the voltage matching can be achieved more precisely by using the transistors biased in W.I. In this mode of operation a small change in V_{GS} can cause a large change in the drain current and therefore for the same drain current, the V_{GS} values of the transistors cannot differ by much.

As discussed above, the transistors biased in W.I. can achieve the maximum transconductance efficiency (g_m/I_D). The EKV model provides an equation for the transconductance of the transistor that is valid in all levels of inversion [42]. Equation (9.6) below represents this equation for the transconductance as a function of the inversion coefficient,

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \cong \frac{\frac{I_D}{I_S}(2n\beta U_T)}{\sqrt{\frac{I_D}{I_S} + \frac{1}{2}\cdot\sqrt{\frac{I_D}{I_S}} + 1}} \tag{9.6}$$

Based on (9.6), g_m for the conditions of S.I. and W.I. can be simplified as shown below:

$$g_m = \begin{cases} \sqrt{2n\beta I_D} & \frac{I_D}{I_S} > 10(\text{S.I.}) \\ \frac{I_D}{nU_T} & \frac{I_D}{I_S} < 0.1(\text{W.I.}) \end{cases} \tag{9.7}$$

From (9.7) in S.I. g_m is proportional to square root of I_D, while in W.I. it is proportional to I_D. Binkley et al. [43] provides the plot shown in Fig. 9.6 that demonstrates the change of g_m/I_D based on the transistor level of inversion. From this figure g_m/I_D is maximized in W.I. that can help reduce the power consumption of the circuit. Therefore for the same current, the transistor biased in W.I. can achieve higher g_m than the transistor biased in S.I. In this case the transistor which is biased in W.I. needs to be much wider than the other that is biased in S.I. This is because the gate-source bias applied in W.I. is much smaller than the one biased in S.I. Therefore biasing the transistors in W.I. usually asks for wider transistors. In addition, as discussed above, the biasing of the transistors in W.I. make them very sensitive to V_{th} variation and therefore can also be affected more by drain induced barrier lowering (DIBL). To decrease the sensitivity of the current to the drain voltage through DIBL, it is required to increase the length of the transistors. Therefore biasing the transistors in W.I. asks for a large sizing which generates a high parasitic input capacitance. However, it is not recommended in cases where the high parasitic capacitance cannot be tolerated. Therefore the best condition for biasing the transistors in week inversion is the first stage input pair transistors of the amplifier, where the maximum g_m is required and the parasitic capacitance cannot

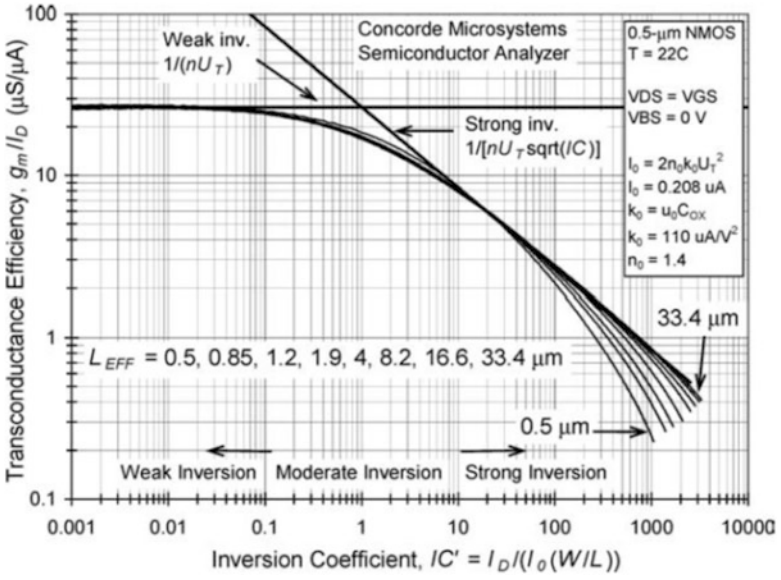

Fig. 9.6 Relationship between g_m and the drain current in different regions of operation [43]

affect the internal components of the circuit. Another advantage of biasing the input pair transistors in W.I. is the reduction of the total noise of the system. In low frequency circuit design flicker-noise has a huge impact on circuit quality. In these circuits the flicker noise can be derived from the equation below [44]:

$$\overline{v_i^2} = \left(\frac{K_f}{WLC_{\mathrm{ox}}f}\right)\Delta f \tag{9.8}$$

Based on this equation the flicker noise can be reduced by increasing the size of the transistors. The use of the large transistors in the input pair of the first stage can be very helpful in reducing the flicker noise. The thermal noise of the differential amplifier can be calculated to be the ratio of the g_m of the current mirrors to that of the first stage input pair. For a conventional amplifier shown in Fig. 9.7, the thermal noise density can be calculated to be [45]:

$$\overline{v_{\mathrm{in,thermal}}^2} = \left[\frac{16kT}{3g_{m1}}\left(1+2\frac{g_{m3}}{g_{m1}}+\frac{g_{m7}}{g_{m1}}\right)\right]\Delta f \tag{9.9}$$

where, Δf is the system frequency bandwidth and $g_{m3} = g_{m5} = g_{m4} = g_{m6}$, $g_{m7} = g_{m8}$ and $g_{m1} = g_{m2}$. Having the first stage transistors biased in W.I. and the current mirror transistors in S.I. can help decrease the ratios of g_{m3}/g_{m1} and g_{m7}/g_{m1} which leads to lower thermal noise. While having the current mirror transistors biased in S.I. can also help improve the current matching.

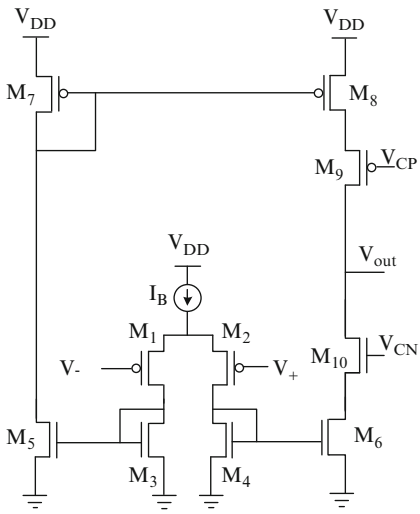

Fig. 9.7 Schematic of a conventional amplifier [45]

9.5.2 Supply Voltage Reduction

In analog/RF circuit the power consumption is proportional to the supply voltage and thus reducing the power supply can reduce the power consumption of the circuit. Lower supply voltage also reduces the electric field and improves the long term device reliability. However, lower supply voltage limits the dynamic range in analog circuit and offers reduced voltage headroom for the cascode structures. Therefore it is necessary to develop new techniques to obtain the same performance while using a nominal power supply voltage.

9.5.3 Bulk-Driven Technique

The bulk-driven MOS transistor concept was introduced by A. Guzinski et al. in 1987 [46], where the bulk terminals of the MOSFETs were used in the design of the differential input stage of an operational transconductance amplifier (OTA). The technique allows a designer to remove the voltage overhead associated with V_{th} from the signal path [47, 48]. The main idea to achieve the low supply voltage therefore is the reduction of the threshold voltages of MOSFETs. For a typical NMOS, the threshold voltage can be expressed as:

$$V_t = V_{t0} + \gamma(\sqrt{2\varphi_F - V_{\mathrm{BS}}} - \sqrt{2\varphi_F}) \tag{9.10}$$

where, the parameters in (9.10) are identical to the standard SPICE parameters for MOSFETs. The second term in (9.10) will be negative if V_{BS} is positive; thereby

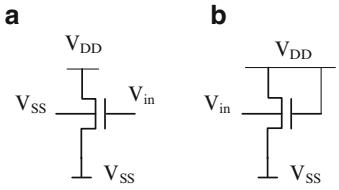

Fig. 9.8 (**a**) a conventional gate-driven NMOS transistor, (**b**) a bulk-driven NMOS transistor

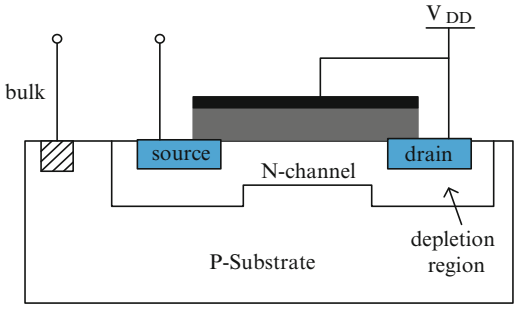

Fig. 9.9 Cross section of an N-channel MOSFET

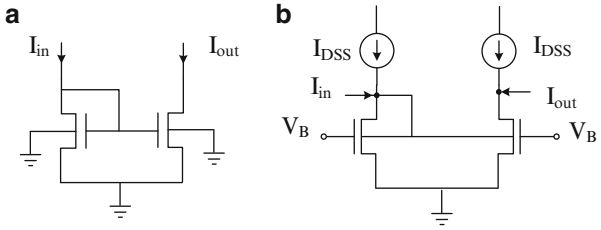

Fig. 9.10 Typical configurations of a current mirror with (**a**) gate-driven NMOS and (**b**) bulk-driven NMOS

reducing the V_{th} below V_{t0}. Figure 9.8 shows a basic configuration of a conventional gate-driven NMOS transistor (a) and bulk-driven NMOStransistor (b).The cross section of an N-channel MOSFET (P-substrate technology) is shown in Fig. 9.9. Unlike the conventional gate-driven MOSFETs, the bulk-driven ones operate very similar to JFETs [47]. Besides, the channel width is constant as long as the gate bias does not change. Therefore, the bulk-driven MOSFETs can operate as a depletion-mode device

Figure 9.10 shows the schematics of typical analog units such as current mirror and differential pairs with bulk-driven inputs; while the Fig. 9.11 shows the comparison between the differential pairs with gate-driven and bulk-driven NMOS transistors.

The most prominent advantage of the bulk driven technique is the reduced voltage supply. Besides, the depletion characteristic allows zero, negative and even small positive values of bias voltage to achieve the desired DC currents [47], which provides a large input common mode range for the input signal. In addition, since

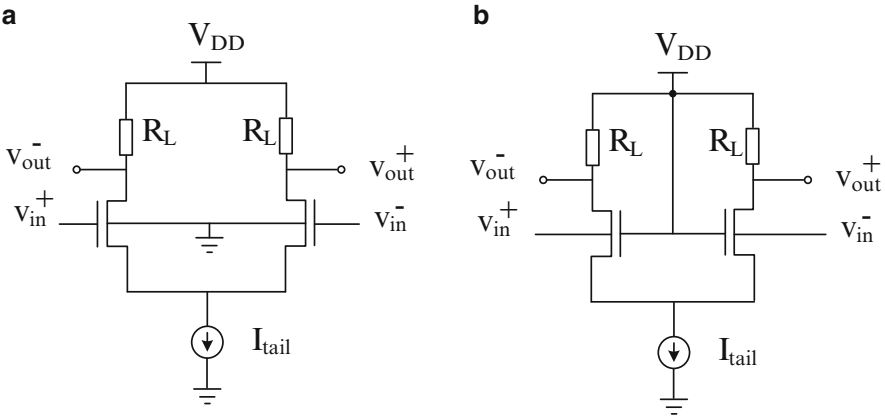

Fig. 9.11 Typical configurations of a differential pair with (**a**) gate-driven NMOS and (**b**) bulk-driven NMOS

the poly-Si gate can totally turn the channel off, the turn-on/off ratio of the bulk-driven MOSFET is very large, which makes it good candidate for application in modulation circuits.

There are also several limitations of the bulk-driven MOSFET which limit its wide acceptance. The first one is the lack of the availability of the isolated bulk terminals. For example, in P-substrate process, only PMOS (which is planted in N-well) can be used as bulk-driven MOSFET, since the bulk terminal of the NMOS is usually fixed to the most negative supply and cannot be fed with different voltages. Therefore, unless a deep N-well or a triple well process is available, the bulk-driven MOSFETs cannot be used in CMOS structures where both N and P type MOSFETs are required.

According to [47], the transconductance of a bulk-driven MOSFET can be expressed as,

$$g_{mb} = \frac{\mathrm{d}i_D}{\mathrm{d}v_{BS}} = \frac{\gamma g_m}{2\sqrt{2\varphi_F - V_{BS}}} \tag{9.11}$$

which can be designed to be either larger or smaller than the transconductance of a gate-driven MOSFET. However, the input capacitance can largely limit the speed of operation of these devices. The unity gain cut-off frequency of a bulk-driven MOSFET can be expressed as:

$$f_{T,bulk-driven} \approx \frac{g_{mb}}{2\pi(C_{bs} + C_{bsub})} = \frac{\eta g_m}{2\pi(C_{bs} + C_{bsub})} \tag{9.12}$$

Where η is the ratio of g_{mb} to g_m with typical value of 0.2 to 0.4.The other parameters in (9.12) are identical to the standard SPICE parameters for MOSFETs.

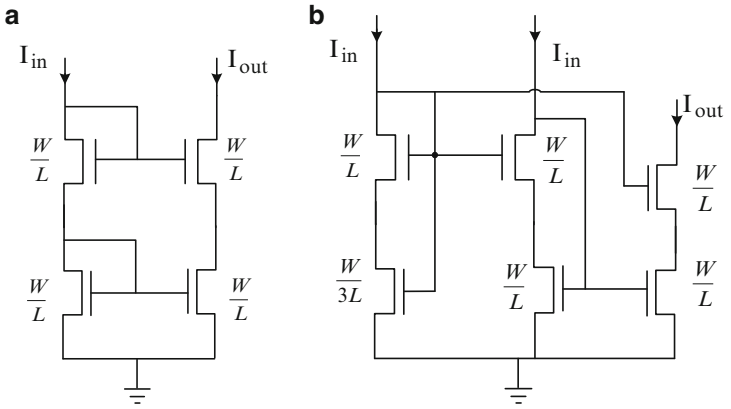

Fig. 9.12 (**a**) Conventional NMOS cascode structure, (**b**) improved NMOS cascode with high output voltage swing indicating the aspect ratios of the MOSFETs. An additional current branch is needed in (**b**) to properly set the bias

Thus the unity gain cut-off frequencies of the gate- and the bulk-driven MOSFETs can be related by the following expression,

$$f_{T,bulk-driven} \approx \frac{\eta}{3.8} f_{T,\text{gate-driven}} \tag{9.13}$$

Equation (9.13) indicates that the maximum operating frequency of the bulk-driven MOSFET is about one decade less than that of gate-driven MOSFET. Another disadvantage of the bulk-driven MOSFETs is larger mismatch of these devices. In addition, their noise performance is also inferior to their gate-driven counterparts, primarily due to the following reasons: (a) the channel noise current to the input of the bulk-driven device has a larger gain factor compared to the gate-driven one and (b) the bulk sheet resistance of the bulk-driven MOSFET can generate additional thermal noise.

9.5.4 Self-Cascode Technique

To some extent, the self-cascode technique can be considered another low voltage supply technique, similar to the bulk-driven technique. As the feature size shrinks, the output impedance of the MOSFET is also becoming smaller because of channel length modulation [49]. Cascode structure is usually employed to enhance the output impedance to achieve higher gain. However, the conventional cascode structure is not suitable for low voltage/power application due to either the reduced output swing or the need for additional biasing current. Figure 9.12 shows two commonly used cascode structures.

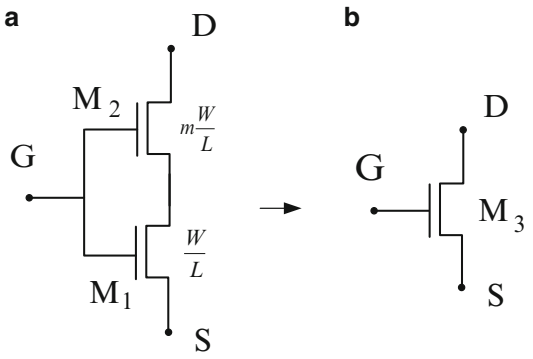

Fig. 9.13 (**a**) Self cascode structure and (**b**) its equivalent composite transistor

Self-cascode technique shown in Fig. 9.13a is developed to maintain a good output swing without requiring any additional biasing there by making this scheme a potentially good candidate for low voltage design. In this configuration, usually M2 has an aspect ratio of m times of that of M1 i.e., $(\mathrm{W/L})_2 = \mathrm{m}\ (\mathrm{W/L})_1$ (usually for optimal operation, m is set much larger than 1). Under this scenario, these two transistors can be considered as a composite transistor M3 as shown in Fig. 9.13b. This new transistor has much larger effective channel length while having a much lower effective output conductance (which results in much higher output resistance) [50].

Then, the effective transconductance of M3 can be expressed as:

$$g_{m3,\mathrm{effective}} = \frac{1}{m} g_{m2} = g_{m1} \tag{9.14}$$

The current flowing through M1, M2 or M3 can be expressed as,

$$I_{\mathrm{DM1,M2,M3}} = \beta_{\mathrm{M3}} (V_{\mathrm{in}} - V_{\mathrm{th}})^2 / 2 \tag{9.15}$$

where, $\beta_{\mathrm{M3}} = \beta_{\mathrm{M1}} \beta_{\mathrm{M2}} / (\beta_{\mathrm{M1}} + \beta_{\mathrm{M2}})$ and β is the transconductance parameter of a MOSFET.

Besides the high output resistance, another good characteristic of the self-cascode structure is that there is very little V_{DSsat} change of M3 compared with typical transistors due to the small V_{DS} of M1. In other words, the output swing is as high as that with a single NMOS transistor. Therefore, the self-cascode structure has potential for use in low-voltage design.

Besides the applications in current mirrors and amplifiers, the self-cascode technique can also be used in high frequency circuits. A low voltage self-cascode voltage controlled oscillator (VCO) as shown in Fig. 9.14 has been reported by Haider et al. [51]. Note that bulk terminals of the P-MOSFETs M1 and M2 are connected to another voltage bias V_{sub} to reduce the threshold voltages.

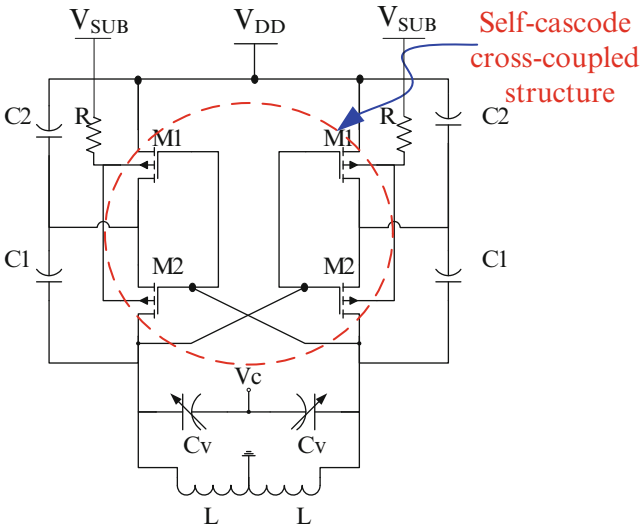

Fig. 9.14 A self-cascode differential VCO for high frequency application [51]

9.5.5 Floating Gate Technique

Floating gate MOSFETs have been typically used for digital memory circuits such as EPROM or EEPROM for several years. This technique has been widely used in a number of low-power analog circuit applications such as CMOS analog trimming circuit [52], multipliers in neural network [53], digital-to-analog converters [54] and amplifiers [55–57]. Unlike conventional MOSFETs, the floating gate voltage V_{FG} in a floating gate MOSFET is controlled by the control gates through capacitive coupling. Figure 9.15 shows a simple layout and circuit symbol of a multi-input floating gate MOSFET.

The gate of the device (Poly I) is normally floating with an electrical charge residing on it. The discharging rate of the gate is very slow due to the good insulation properties of SiO_2. Usually the charge can stay for several years with less than 2% variation at room temperature [58]. From (c), the floating-gate voltage can be expressed as:

$$V_{FG} = (Q_{FG} + C_{FG,D}V_D + C_{FG,S}V_S + C_{FG,B}V_B + \sum_{i=1}^{n} C_{Gi}V_{Gi})/C_{\Sigma} \tag{9.16}$$

where, Q_{FG} is the static charge on the floating-gate, and $C_{\Sigma} = (C_{FG,D} + C_{FG,S} + C_{FG,B} + \sum_{i=1}^{n} C_{Gi})$ is the total capacitance seen at the floating gate. $C_{FG,D}, C_{FG,S}$ and $C_{FG,B}$ are the capacitances between drain, source and bulk, respectively; while C_{Gi} is the capacitance between floating gate and control gates.

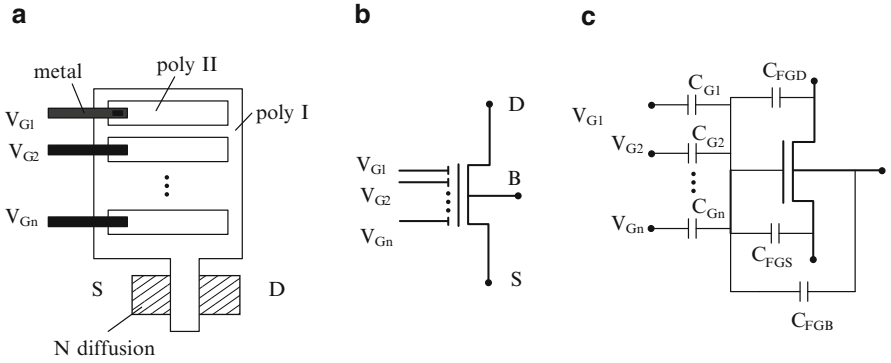

Fig. 9.15 A typical floating gate N-MOSFET (**a**) layout, (**b**) schematic symbol, and (**c**) equivalent circuit with parasitic capacitance noted [58]

For a two-input gate-floating MOSFET, when the signal voltage V_s is applied to gate #1, another bias voltage V_B is applied to gate #2. Usually V_B is higher than V_s, therefore, the threshold of the floating gate MOSFET will adjust to a new threshold voltage V_{th} as follows:

$$V_{th} = (V_{thi} - V_B k_2)/k_1 \tag{9.17}$$

where $k_1 = C_{G1}/C_\Sigma$,$k_2 = C_{G2}/C_\Sigma$ and V_{thi} is the initial value of the threshold voltage.

Therefore, one can achieve lower value of V_{th} than V_{thi} by appropriate selection of V_B, k_1, and k_2 values. Lower threshold voltage makes the circuit feasible for operating with lower supply voltage. However, the technique has several disadvantages. If the transconductance seen from the floating gate is $g_{m,FG}$, then the equivalent transconductance of this 2-gate MOSFET will be $g_{m,equivalent} = k_1 g_{m,FG}$, which is degraded by a factor of k_1. Besides, the floating gate voltage V_{FG} is dependent on the drain voltage due to the parasicitic C_{GD} and as a result the output impedance is also less than that of a normal MOSFET operating under the same biasing condition. The small-signal output resistance can be expressed by:

$$r_{o,FG} = r_o // \frac{C_\Sigma}{C_{GD} g_m} \tag{9.18}$$

where, r_o, C_{GD} and g_m are the small-signal output resistance, gate-drain capacitance and transconductance of the MOSFET. Figure 9.16 shows the typical configurations for current mirror and differential pair with floating-gate devices.

One of the excellent properties of floating gate MOSFET is that the electric charge in the floating gate terminal can stay for several years with a variation of less than 2% at room temperature. As a result this type of device has been widely used for EPROM applications. The static charge in the floating gate terminal can be changed by: (a) illumination under ultra-violet light, (b) hot electron injection, or (b) Fowler-Nordheim (FN) tunneling.

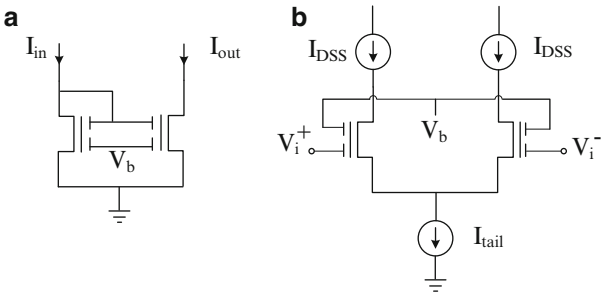

Fig. 9.16 Typical configurations of (**a**) current mirror, (**b**) differential pair with two-input gate-floating N-MOSFETs

9.6 Signal Processing

The signal generated from sensors needs to be processed and the information generated from the measured quantities must be transformed to the format that can be easily read or transmitted out wirelessly. The sensors output signal can be in the format of current or voltage. In the former case an array of sensors can help generate higher current. In the latter case when the voltage amplitude of the generated signal is low then it is required to have a low noise amplifier in the first stage of amplifier to amplify the signal and then convert it to other formats. In this section a nerve signal amplifier is introduced as an example of low level voltage signal processing. An example of current signal processing using a three electrode potentiostat is also introduced.

9.6.1 Neural Systems Signal Processing

Development of new methods to understand human brain has been of great interest for a long time. Neuroscientists and IC designers are collaborating to understand human brains using brain-computer interface (BCI). These studies have led to the development of low-power, light-weight implantable wireless sensors which can transfer information to the external devices. This technology can help people with severe motor disability (e.g., due to cerebral palsy) by using their brain data and sending them to the relevant muscle.

Designing neural interfaces is a very challenging task. The first gain amplifier has to provide low-noise amplification for the very small nerve signals (up to 500 μV [59]) while keeping the power consumption as low as possible. The system also needs to process the data fast enough for real time analysis and monitoring [60].

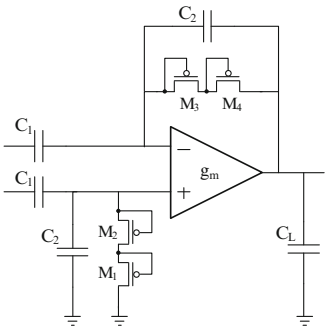

Fig. 9.17 Schematic of a neural amplifier

R.R. Harrison et al. proposed a neural amplifier [59] as shown in Fig. 9.17. The OTA used in this structure is the same as the one shown in Fig. 9.7. The midband gain (A_m) of this system is set by $C1/C2$ and for OTA transconductance of g_m the bandwidth is $g_m/A_m C_\mathrm{L}$.

In order to achieve the lowest input noise while providing the minimum of power for the OTA, this circuit is using the sub-threshold technique described earlier. As discussed before in (9.9), the thermal noise of this amplifier can be minimized by choosing the g_m of M_3, M_5 and M_7 much lower than the g_m of M_1 and M_2, which means: $(W/L)_3$, $(W/L)_5$, $(W/L)_7 \ll (W/L)_1$ and $(W/L)_2$.

The transistors M_1 and M_2 are biased in sub-threshold regime, while M_3, M_5 and M_7 are biased in strong inversion. Based on (9.8) the large sizing of the transistors M_1 and M_2which are biased in W.I. also helps decreasing the flicker noise. The total input noise of the structure shown in Fig. 9.17 is defined to be [59]:

$$\overline{v_{ni,\mathrm{amp}}^2} = \left(\frac{C_1 + C_2 + C_\mathrm{in}}{C_1}\right)^2 \overline{v_{ni}^2} \tag{9.19}$$

In this structure the noised efficiency factor (NEF) is calculated to be [59]:

$$\mathrm{NEF} = V_{ni,\mathrm{rms}} \sqrt{\frac{2I_\mathrm{tot}}{\pi . U_T . 4kT . BW}} \tag{9.20}$$

That can be reduced to [59]:

$$\mathrm{NEF} = \sqrt{\frac{4}{\kappa U_T}\left(\frac{I_\mathrm{D1}}{g_{m1}}\right)} \tag{9.21}$$

By biasing the transistors in sub-threshold regime, the NEF can be derived to be [59]:

$$\mathrm{NEF} = \sqrt{\frac{4}{\kappa^2}} \cong 2.9 \tag{9.22}$$

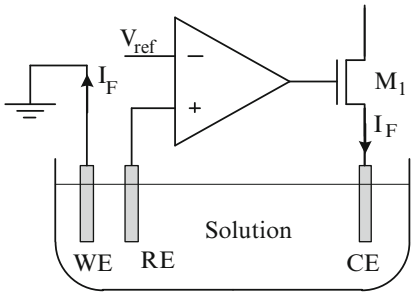

Fig. 9.18 A conceptual drawing of a three-electrode potentiostat

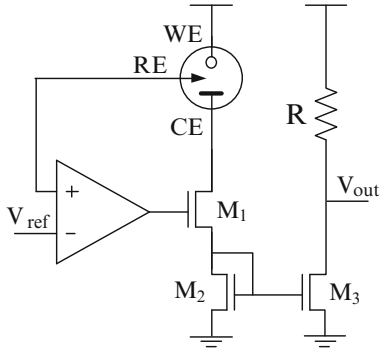

Fig. 9.19 A potentiostat with a current mirror to convert the current in to the voltage

9.6.2 Current Signal Processing in Potentiostats

An example of current signal processing using a three-electrode potentiostat is shown in Fig. 9.18 [61]. This potentiostat consists of three electrodes: working electrode (WE), counter electrode (CE) and reference electrode (RE). To measure the physical parameters such as glucose, lactate, CO_2 and pH, a constant difference potential should be provided across RE and WE. Based on the concentration of the analyte solution, the applied voltage across these electrodes can initiate chemical reaction which generates electrons that can be collected in CE. The collected current from this electrode needs to be processed using a signal processing unit.

A current mirror is used to generate a copy of the current collected by CE. The mirrored current generates a voltage across the resistor R which is proportional to the generated current [60]. This is shown schematically in Fig. 9.19.

Another type of signal processing unit implemented using a capacitor for the mirrored current as shown in Fig. 9.20 [62, 63]. In this case the generated voltage across the capacitor is the integral of the current that passes through this capacitor. In this structure a switch is used in parallel with the capacitor to discharge the capacitor when the capacitor voltage reaches the reference voltage of the comparator. A comparator is employed to compare the capacitor voltage with the reference voltage and if it exceeds the reference voltage the comparator output generates a signal that can turn this switch on and discharge the capacitor. Higher values of current

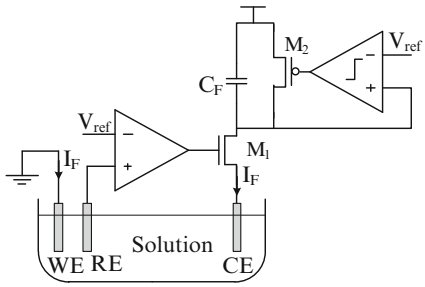

Fig. 9.20 Using capacitor in the pass of sensor current for generating pulses with frequency proportional to the sensor current

can charge the capacitor faster resulting is higher frequencies of pulse signal generated at the output of the comparator. Similarly, for lower level of current this frequency decreases. Therefore the frequency of comparator output signal contains the information on the magnitude of the sensor current.

9.7 Power-Conditioning Modules in Sensor Electronics

Battery is usually used in portable electronics for power supply. But it is not very convenient to replace it frequently, particularly for applications in health monitoring involving implanted sensors. Therefore, some other alternative power supplies are studies and developed recently [64, 65]. For example, photovoltaic cells are frequently used for applications with access to the light source. Typical photovoltaic cell can provide up to several to tens of milli-watts (mW) of power. The embedded electronics in RFID tags use the electromagnetic fields as its energy source, which can provide on the order of mW of power. Other sources include piezoelectric, thermal or other forms of harvested energy [66].

These sources usually cannot be directly used for electronic circuits. For example, the electromagnetic waves usually represent low-amplitude time-varying signals which may not be sufficient to power the electronic circuits. Even the battery voltage which is usually a relatively stable DC signal degrades with long term use. Therefore, an additional power-conditioning module is usually needed between these power sources and the electronic circuits. Figure 9.21 shows a typical power-conditioning module for integrated system with power source consisting of an inductive link [64]. Rectifier is used to convert the time-varying signal to a stabile DC signal. For some applications, additional blocks such as the voltage multiplier may be needed as well. To regulate this DC signal furthermore and provide desired DC voltage level, a voltage regulator is also needed.

A low drop-out (LDO) voltage regulator is usually employed more frequently than the other regulator structures in integrated circuits as it usually requires a much lower minimum drop-out voltage than the others. The voltage difference, so called drop-out voltage, defines the efficiency of the voltage regulator. Figure 9.22 shows the typical schematic of a LDO regulator.

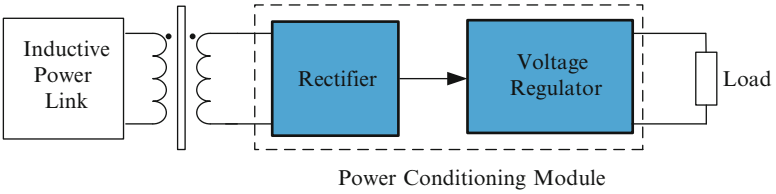

Fig. 9.21 Typical power-conditioning module for systems with inductive link power

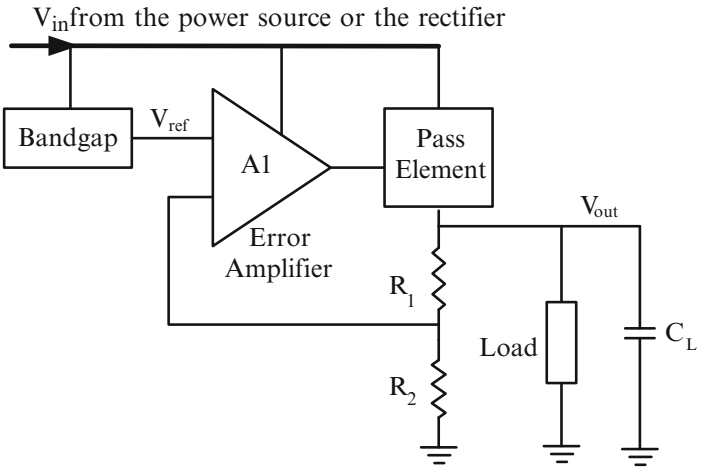

Fig. 9.22 Schematic of a LDO regulator

The circuit consists of: (1) a bandgap voltage reference, (2) an error amplifier, (3) a pass element, and (4) a voltage divider. The bandgap outputs a very stable DC voltage, V_{ref}, which is immune to supply and temperature variation, but it cannot directly drive the load. The error amplifier A1 is used to monitor the changes in the output voltage and to generate a drive voltage for the pass element to adjust the current with a negative feedback scheme to stabilize the output voltage. A conventional operational amplifier can be employed as the error amplifier. The pass element typically employs a MOSFET or a composite structure to provide the output stage for the load. Usually the transistor size is large to handle the required output current. Besides, it is also very important in terms of frequency compensation for the entire negative feedback loop. A voltage divider can be designed to obtain the desired output voltage. From the schematic, one can easily derive the output voltage expression:

$$V_{\text{out}} = V_{\text{ref}}\left(1 + \frac{R_1}{R_2}\right) \tag{9.23}$$

9.8 Summary

The advancements in IC processing and sensing techniques in the last few decades have made the widespread use of sensor techniques possible in modern biomedical applications. The high degree of miniaturization now possible for the classical measurement techniques has led to the realization of complex analytical systems, including sensors that are known as "BioChem Lab-on-a-Chip". The latest developments in micro/nano-technology have contributed to a wider range of medical applications. This chapter has been particularly focused on biomedical applications that can be benefited from the use of sensor techniques. Low-power circuit design, low-power signal-processing schemes and power-conditioning circuits for implementation of implantable biosensors have also been presented in this chapter. It is expected that this chapter will give the reader at least a fundamental understanding of the challenge associated with the design of biomedical sensors and of low-voltage low-power sensor electronics in this deep sub-micron CMOS era.

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Chapter 10
Sensor Conditioning Circuits*

Julia Hsin-Lin Lu and Byunghoo Jung

10.1 Introduction

Analog sensors produces a variation in an electrical property to show a change in the environment. The analog variation in electrical property needs a conditioning circuit to indicate the change before conversion into digital signal. The electrical properties most commonly detected by analog sensors are voltage, current, capacitance, resistance, and charge. Real-time capacitive and resistive sensors are used in a wide range of physical measurement systems. Detection of a small capacitance or resistance change is widely demanded in industrial process control systems and medical instrumentations [2]. Currently, there is an increasing demand for a compact mobile system that can be equipped with various types of sensors. As shown in Fig. 10.1, a cellular handset that is compatible with different types of health monitoring or environment sensors, combining with the wireless connectivity of the cellular system, the real-time collected data through the sensors can be maximally exploited. Since every sensor has its own requirements for readout and every user has their own applications that require different types of sensors, a reconfigurable low-power universal sensor interface is crucial for successful implementation. The compatibility with various disposable health monitoring sensors is particularly important since the cost of the disposable unit can be reduced by simplifying interconnect requirements between the readout and sensors. In most of these

*Portions of this manuscript and material referred in this manuscript have appeared in [1].

J.H.-L. Lu (✉)
Purdue University, West Lafayette, IN 47907, USA
e-mail: hlu@purdue.edu

B. Jung
Purdue University, West Lafayette, IN 47907, USA
e-mail: jungb@purdue.edu

E. Tlelo-Cuautle (ed.), *Integrated Circuits for Analog Signal Processing*,
DOI 10.1007/978-1-4614-1383-7_10,

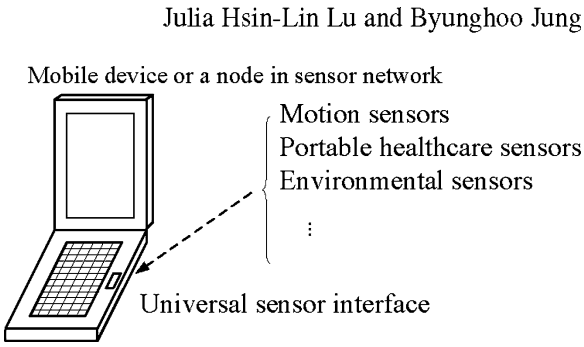

Fig. 10.1 Application example of universal sensor interface

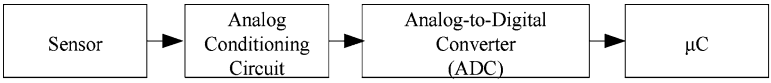

Fig. 10.2 Traditional method to obtain digital output

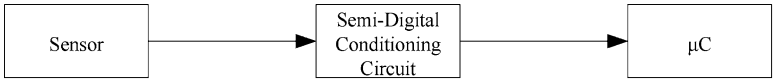

Fig. 10.3 Alternative method to obtain digital output

applications, a physical quantity is converted into a capacitance or resistance change, and a readout circuit converts various capacitance or resistance changes into digital or analog electrical signals.

10.2 Analog and Semi-digital Sensor Conditioning Circuits

The available types of sensor readouts can be broadly classified into analog and semi-digital. Traditionally, the digitized outputs were obtained by employing analog sensor readout signals followed by analog-to-digital converters (ADC), as shown in Fig. 10.2. This topology, which uses an ADC, not only increases the complexity and power consumption but also introduces extra noise. In order to address these issues, semi-digital solutions such as pulse-frequency modulation (PFM) [3] or pulse-width modulation (PWM) [4] have been investigated. These kind of readouts represent analog quantities using only digitized signal levels. This is achieved by encoding the information in the time or frequency domain, rather than the analog voltage or current domain as in analog readouts. This topology is shown in Fig. 10.3. Its rail-to-rail voltage swing also provide the advantage of robustness against environment noise. This alternative method eliminates the traditional ADC and reduces the power consumption significantly. In addition, the dynamic range in semi-digital readouts

is not limited by the supply voltage or current. This is in sharp contrast to the analog readout. Furthermore, the semi-digital output provides robustness against environmental noise due to its digital two-level nature.

10.3 Capacitive Sensor Conditioning Circuits

Detecting physical variation through capacitance sensing is one of the most common approach in a wide variety of physical measurement systems, such as liquid-level gauges, pressure meters, rotor displacement in integrated accelerometers, and MEMS-based sensors, etc. MEMS has favored the development of capacitive sensors for their compatibility to be integrated on silicon substrates, using slightly modified standard microelectronic processes [5]. In these systems a physical quantity is converted into a capacitance change. Next, the capacitance change is converted into a digital signal using a sensor interface. To minimize the parasitic capacitance of packaging, the readout conditioning circuits have to be integrated with the sensors, either on the same integrated circuit chip or inside the same package. Some integrated capacitance sensors produce analog output for implementing simple functions such as producing an alarming signal when the sensing capacitance is higher than a threshold or be included in part of an all-analog systems. Capacitance-to-voltage conversion can be performed using impedance metering circuits or switched capacitor charge amplifiers [4]. A capacitive Wheatstone-bridge can also be used to convert its impedance, at a specific frequency, to a voltage for conditioning a capacitive sensor.

A digital output is desirable when the sensors have to be connected to a low-cost microcontroller with only digital inputs or when the sensor is placed in a remote position in the harsh environment with high electromagnetic noise. The digital output is generally obtained by first producing an analog output and then converting it to digital. Existing semi-digital readouts can be classified into several categories. For a capacitive sensor readout, the first is the capacitance-to-frequency (PFM) [6–8] or capacitance-to-phase [9]. Oscillator-based circuits can be used to produce a variation in oscillating frequency as a function of capacitance. The second type of semi-digital readout, called capacitance-to-time or pulse-width modulation (PWM), provides smaller measurement time compared to PFM. In addition, in contrast to PFM, PWM designs have higher bandwidth and can facilitate the reading procedure by purposely adopting synchronization to the microcontroller [10]. PWM signals can be easily digitized using a digital decimating filter. A current-mode, dual-slope, capacitance-to-pulse duration converter that shows low sensitivity to parasitic capacitance and temperature has been proposed [4]. RC decay could be utilized for conditioning a capacitive sensor. The charging or discharging time it takes for the voltage to reach a threshold is a measure of the capacitance. Single or dual slope integrating detector can also be implemented to integrate a current and measure the elapsed time to reach a voltage threshold.

10.4 Resistive Sensor Conditioning Circuits

Resistive gas sensors and metal-oxide (MOX) sensors show a high baseline resistance on the order of giga-Ohms and a wide dynamic range. Electronic noses often use different gas sensors, and a conditioning readout circuit working for a very wide range is compatible to guarantee enough resolution [11]. Resistance-to-voltage conversion strategy can be used for conditioning the resistive sensor. With a simple voltage divider or a resistive Wheatstone bridge, the change in resistance can be converted to a change in voltage.

For a resistive sensor readout, there are also two popular semi-digital conditioning methods which are resistance-to-frequency [12] and resistance-to-time conversions. Oscillating circuits that perform resistance-to-time conversion are considered to be one of the best solutions since high resistive changes can be measured without using picoammeters or scaling factors [11]. Resistive-to-frequency conditioning readout with frequency output offers several advantages compared to resistive-to-voltage or resistive-to-current with voltage or current output conditioners such as robustness against environment noise and ease of multiplexing and signal processing. RC decay could be utilized for conditioning a resistive sensor. The charging or discharging time it takes for the voltage to reach a threshold measures the resistance change. The design in [4] uses analog amplifiers including integrators and OTA to integrate a current. This wide-range timing measurements such as in frequency, period, duty cycles are compatible to several low-cost microcontroller which support a timing processing unit for input capture.

10.5 Design of an Universal Sensor Readout Circuit

In this chapter, a low-power, low complexity, and wide-dynamic-range universal sensor readout circuit that converts the sensing capacitance or resistance changes to digital duty cycles based on pulse-width modulation (PWM) is introduced [1]. The functionality of the full circuit, including circuit analysis, and noise analysis are discussed.

10.5.1 Principle of Operation

The block diagram of the basic sensor readout circuit and two sensor configuration examples are shown in Fig. 10.4. In this universal design, a capacitive sensor uses a resistive reference, and a resistive sensor uses a capacitive reference.

The circuit operates as follows. First, most of the electronic contains an oscillator, for example a crystal oscillator, providing a clock signal of frequency f_{crys}.

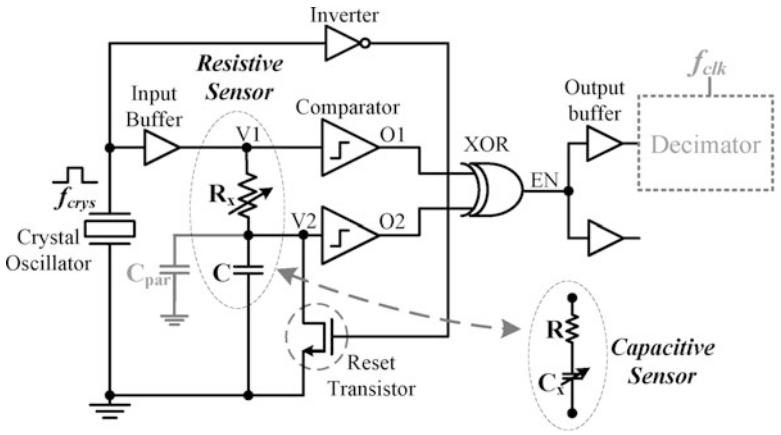

Fig. 10.4 The block diagram of resistive and capacitive sensor readout configurations

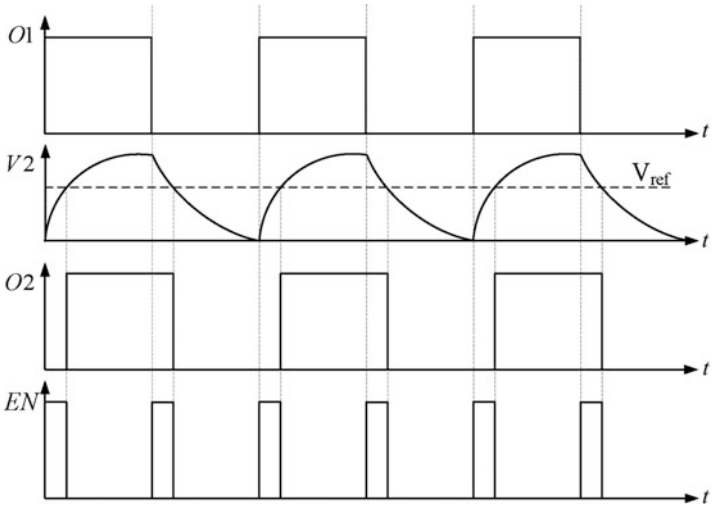

Fig. 10.5 Ideal response of the basic sensor readout

Assuming the input impedance of the comparators is large and the input clock transits quickly, a simple capacitance charging and discharging model can be utilized to analyze the behavior of the circuit during the low and high portion of the input clock. The ideal response of the circuit without a reset block is shown in Fig. 10.5. Neglecting the delay of the comparators, which does not impact the circuit response assuming both comparators have identical delay, we observe that the waveform on $O1$ is equal to $V1$ and depending on the excitation signal transition, node $V2$ either charges or discharges with an RC time constant. In this design, the switching threshold of the comparator is set to $0.5V_{DD}$. The outputs of the

comparators are fed into an XOR gate, which operates as a phase detector. The output pulse width is linearly proportional to the charging time constant at node $V2$. A digital decimation filter can be used to finally measure the pulse width of the output signal from the phase detector.

To understand the ideal sensing range of the basic readout design, we first illustrate the exponential charging and discharging behavior of the capacitor. Defining $\tau = \mathrm{RC}$, V_i the initial voltage and V_f the final voltage, we can express the voltage of the capacitor at any time t as:

$$V_{charge} = V_f \cdot (1 - e^{-t/\tau}) \tag{10.1}$$

$$V_{discharge} = V_i \cdot e^{-t/\tau}. \tag{10.2}$$

If we set the comparator threshold voltage V_{comp} to a percentage of the supply voltage, say αV_{DD} where α is a constant smaller than 1, substituting $V_{charge} = \alpha V_{DD}$ and $V_f = V_{DD}$ into (10.1) and solving for t, we obtain the pulse width T_{pw}:

$$T_{pw} = t = RC \cdot ln\left(\frac{1}{1-\alpha}\right). \tag{10.3}$$

Equation (10.3) shows that the output pulse width is linearly proportional to the sensing capacitance or resistance value. Contrary to other designs that use analog integrators to achieve the linearity between input and output [4], we use a purely CMOS circuit.

The maximum detectable capacitance and resistance, C_{max} and R_{max}, correspond to the maximum producible pulse width. To fully utilize the excitation signal period, we can employ an uneven duty cycle, D. Taking into account the pulse produced by the "on" duration of the excitation signal, we can obtain

$$C_{max} = \frac{D \cdot T_{crys}}{R \cdot ln\left(\frac{1}{1-\alpha}\right)} \tag{10.4}$$

$$R_{max} = \frac{D \cdot T_{crys}}{C \cdot ln\left(\frac{1}{1-\alpha}\right)} \tag{10.5}$$

where T_{crys} is the period of the excitation signal.

The sensing range linearly increases with duty cycle, D, as shown in (10.4) and (10.5). Note that the illustration in Fig. 10.5 assumes that the duty cycle is 50% which allows an equal amount of time to charge and discharge the capacitor. If, for example, we were to increase D to 95%, one can observe that a DC offset is introduced due to the inadequate discharging time. In order to resolve this issue we connect a fast reset switch at node $V2$, as illustrated in Fig. 10.4. As shown in Fig. 10.4, the reset block consists of an inverter and a pull-down NMOS transistor. When the reset transistor is triggered by a low excitation signal, it quickly discharges node $V2$. Depending on how much time is required to reset the circuit, one can optimize the duty cycle of the excitation signal to achieve the maximum sensing

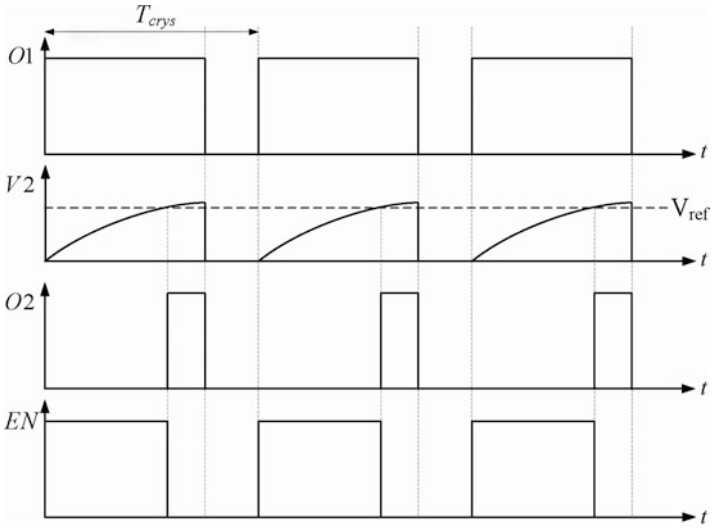

Fig. 10.6 Ideal response of readout circuit with reset block

range. An additional buffer is used to match the delay time of the reset signal. This allows the charging to begin as soon as the reset operation is complete. The response of the readout circuit with the reset block is demonstrated in Fig. 10.6.

10.5.2 Circuit Analysis and Optimization

In this section we explore the limitations in sensing range and the performance of the proposed readout circuit. This proposed readout circuit converts the capacitance or resistance into a pulse duration, herein we refer to it as pulse-width modulator (PWM). In the following analysis, we use only the capacitive-sensing configuration for simplicity. The analysis for resistive sensor readout is dual.

10.5.2.1 Maximum Sensing Capacitance

According to the operation described in Sect. 10.5.1, we can divide the sensing range limitations into two conditions: one imposed by the "on" duration of the crystal oscillator, which is the charging time, $f_1(D)$; the other imposed by the "off" duration, which is the reset time, $f_2(D)$. Both operations require an adequate amount of time. The first criteria, which is the maximum detectable capacitance limited by the "on" duration of the clock is given by (10.4). On the other hand, the reset criteria is given by

$$T_{dis} < (1 - D) \cdot T_{crys}, \tag{10.6}$$

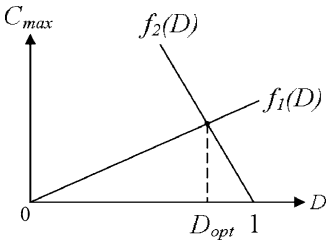

Fig. 10.7 Conceptual behavior of C_{max} when we sweep D

where T_{dis} is the time required to discharge node $V2$ to ground. As described in Sect. 10.5.1, during the reset operation the discharging time constant at node $V2$ can be expressed as

$$\tau_{dis} = (r_{on} \parallel R) \cdot C, \tag{10.7}$$

where r_{on} is the on-resistance of the reset transistor. A reasonable assumption for the time for $V2$ to discharge to GND is $5\tau_{dis}$. This translates to the following equations:

$$5(r_{on} \parallel R) \cdot C < (1 - D) \cdot T_{crys} \tag{10.8}$$

$$C_{max} = \frac{(1 - D) \cdot T_{crys}}{5 \cdot (r_{on} \parallel R)}. \tag{10.9}$$

Equation (10.9) shows the limit on the maximum detectable capacitance imposed by the reset operation. Together with (10.4), we can summarize the maximum detectable capacitance as

$$\begin{aligned} C_{max} &= min \left\{ \frac{D \cdot T_{crys}}{R \cdot ln2}, \frac{(1 - D) \cdot T_{crys}}{5 \cdot (r_{on} \parallel R)} \right\} \\ &= min\{f_1(D), f_2(D)\}. \end{aligned} \tag{10.10}$$

This behavior is conceptually illustrated in Fig. 10.7. Intuitively, the available charging time, $f_1(D)$, increases as D increases, while the available reset time, $f_2(D)$, decreases and vice versa. D_{opt} can be determined from the intersection of the two functions and represents an optimal duty cycle for C_{max}.

10.5.2.2 Effect of Parasitic Capacitance

The effective sensing capacitance, C_{eff}, is dependent on the parasitic capacitance seen by the sensing node $V2$. As shown in Sect. 10.5.1, the comparators are implemented with digital inverter circuits. Assuming the channel resistances of $M1$ and $M2$ in the comparators, which are biased in deep triode region, are small, we can express C_{eff} as follows:

$$C_{eff} \approx (C_{PCB} + C_{MOS}) + C_x \tag{10.11}$$

$$= C_{par} + C_x. \tag{10.12}$$

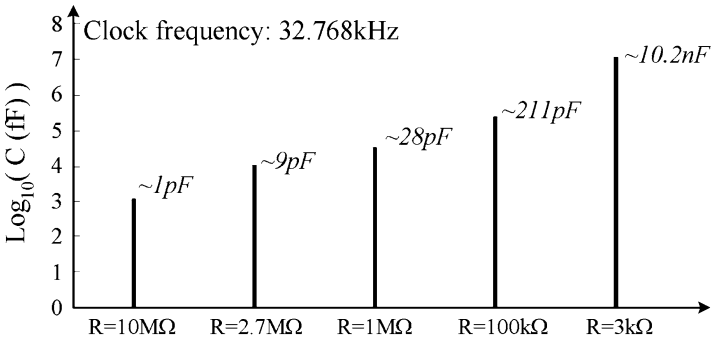

Fig. 10.8 Capacitance dynamic range with different reference resistors

where C_{MOS} is the capacitance from MOS devices (CMOS), C_x is the sensing capacitance, and C_{PCB} is the off-chip PCB parasitic capacitance seen by the sensing node $V2$. The linearity between the pulse width and sensing capacitance is not affected by the parasitic capacitance. It only introduces a fixed offset proportional to the C_{par} in the pulse width which can be easily calibrated.

10.5.2.3 Reconfigurable Readout Dynamic Range and Sensitivity

As a reconfigurable system, for variable capacitance or resistance readout, the sensor interface can perform different dynamic ranges. The factors that limit the minimum sensing values are (a) the comparator slew rate and (b) the dead zone of the phase detector (XOR gate). The comparators implemented by digital inverters have relatively high slew rate, so we focus on (b). The phase detector enters the dead zone when the rising edge of the output pulse is not allowed sufficient time to charge to V_{DD}. If we denote the resistance and capacitance at the XOR output as R_{XOR} and C_{XOR}, respectively, the minimum detectable pulse width $T_{pw,min}$ is approximately $5R_{XOR}C_{XOR}$. Thus the minimum sensing resistance and capacitance can be obtained as

$$R_{min} \cong \frac{5R_{XOR}C_{XOR}}{C \cdot ln\left(\frac{1}{1-\alpha}\right)}, \tag{10.13}$$

$$C_{min} \cong \frac{5R_{XOR}C_{XOR}}{R \cdot ln\left(\frac{1}{1-\alpha}\right)}. \tag{10.14}$$

For the maximum sensing resistance and capacitance, as derived in (10.4) and (10.5), the R_{max} and C_{max} are inversely proportional to the reference capacitance and resistance. Hence, the readout dynamic ranges defined as R_{max}-R_{min} and C_{max}-C_{min} are inversely proportional to the reference values. Figures 10.8 and 10.9 shows the simulated sensing ranges in the face of different reference values. As discussed,

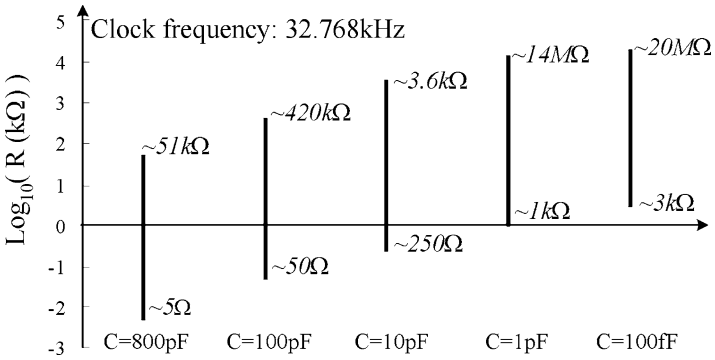

Fig. 10.9 Resistance dynamic range with different reference resistors

the sensing range increases with decreasing reference value. The C_{min} value does not change because the relatively large parasitic capacitance at the sensing node $V2$ generates a detectable pulse even with zero sensor capacitance ($C_x = 0$).

We define the readout sensitivity as the rate of change of the pulse width versus sensing value. Using (10.3), for $\alpha = 0.5$, we can obtain the sensitivities as

$$Sens(R) = \frac{\partial T_{pw}}{\partial R_x} = Cln2 \tag{10.15}$$

$$Sens(C) = \frac{\partial T_{pw}}{\partial C_x} = Rln2, \tag{10.16}$$

The sensitivities are linearly proportional to the reference values. The analysis clearly shows the trade-off between the sensing range and the sensitivity.

10.5.2.4 Circuit Noise and Readout Resolution

Noises injected into or generated by the readout circuit limits the sensing resolution. One of the most critical noise sources is flicker noise because most sensor signals occupy frequency bands below the flicker noise corner frequency (f_{knee}), which is typically 500-kHz–1-MHz for sub-micron transistors [13]. To mitigate the effect of flicker noise, the proposed readout circuit up-converts the sensor signal to a high sampling frequency, f_{crys}, using AC excitation in the very beginning before entering the main circuit blocks as shown in Fig. 10.10. The flicker noise issue can be mitigated by properly choosing the excitation frequency (f_{crys}), and we ignore it in the following analysis.

The noise generated by the PWM circuit stems from the thermal noises of the resistors and transistors, flicker noise, crystal oscillator jitter and supply noise. Noise introduces jitters in the pulse trailing edge and needs to be modeled in terms of its probability density function. However, we first consider an additive noise voltage,

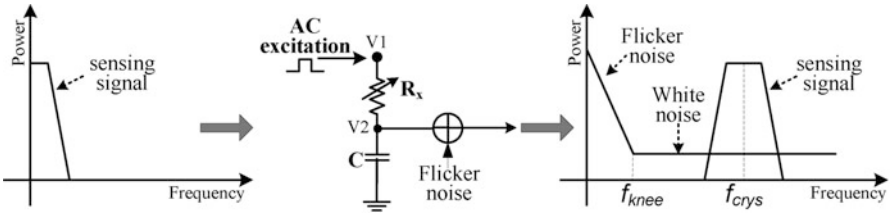

Fig. 10.10 Conceptual diagram of signal up-conversion operation

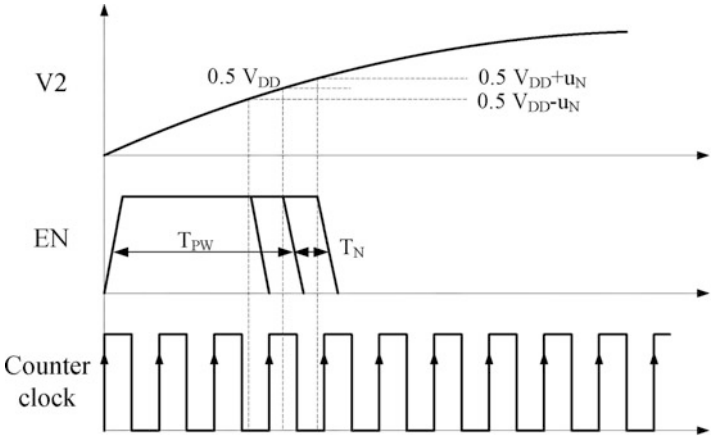

Fig. 10.11 Conceptual diagram of the additive noise voltage

u_N, superimposed on the charging curve. Figure 10.11 shows the effect of the noise voltage converted to a pulse width, then converted to a digital number by counting the number of counter clock cycles. As can be seen from Fig. 10.11, the noise can be either constructive ($+u_N$) or destructive ($-u_N$) for simplification. In a noiseless circuit, we can express the time it takes to charge node $V2$ to $0.5V_{DD}$ by visiting the familiar formula:

$$T_{pw} = RC \cdot ln2. \tag{10.17}$$

Now suppose we have a destructive noise $-u_N$ superimposed on the charging curve. In such a noisy environment, this translates to the original capacitor having to charge to $0.5V_{DD} + u_N$. We can obtain

$$0.5V_{DD} + u_N = V_{DD}\left(1 - e^{-t/RC}\right). \tag{10.18}$$

Solving for t we can obtain the time it takes to charge to $T_{pw} + \delta T_N$:

$$T_{pw} + \delta T_N = RC \cdot ln\left(\frac{V_{DD}}{0.5V_{DD} - u_N}\right). \tag{10.19}$$

The step capacitance ΔC that corresponds to the step pulse width from noise, δT_N, is equal to the maximum sensitivity of the circuit to noise with single shot measurement. We therefore determine the ΔC by using the following formulas:

$$T_{pw} + \delta T_N = R(C + \Delta C) ln2. \tag{10.20}$$

Equations (10.17) and (10.19) allow us to find δT_N as follows:

$$\delta T_N = RC \cdot ln\left(\frac{0.5V_{DD}}{0.5V_{DD} - u_N}\right). \tag{10.21}$$

Using (10.20) and (10.21) and solving for ΔC we can obtain:

$$\Delta C = C \cdot log_2\left(\frac{V_{DD}}{V_{DD} - 2u_N}\right). \tag{10.22}$$

Similarly, a constructive noise would correspond to the noiseless capacitor charging to $V - u_N$.

Note that the maximum sensitivity to an injected noise is dependent on the base sensing capacitance. Larger sensing capacitance has degraded readout resolution because of the high sensitivity to the noise.

In the following noise analysis, we assume that the additive noise is a stationary white Gaussian random variable with standard deviation σ_V. If we denote the noise as u_n, then it can be expressed as $u_n \sim N(0, \sigma_V^2)$. Thus, the output pulse width T_{pw} can be expressed as discrete time random processes that depend on noise u_n. By using (10.17) and (10.19), assuming $y = ln(0.5V_{DD} - u_N)$, the variance of jitter, σ_T^2, can be derived according to the variance of noise voltage, σ_V^2, as:

$$\begin{aligned}
\sigma_T^2 &= Var\{\delta T_N\} \\
&= R^2C^2 \cdot Var\{ln(0.5V_{DD} - u_N)\} \\
&= R^2C^2 \cdot \left\{ \int_{-\infty}^{\infty} y^2 \cdot \frac{1}{\sqrt{2\pi\sigma_V^2}} \cdot e^y \cdot e^{\frac{-(0.5V_{DD} - e^y)^2}{2\sigma_V^2}} dy \right. \\
&\quad \left. - \left[\int_{-\infty}^{\infty} y \cdot \frac{1}{\sqrt{2\pi\sigma_V^2}} \cdot e^y \cdot e^{\frac{-(0.5 - e^y)^2}{2\sigma_V^2}} dy \right]^2 \right\}.
\end{aligned} \tag{10.23}$$

A less accurate, but more intuitive equation for the variance of jitter can be derived using the equation derived in [14, 15],

$$\sigma_T = \frac{\sigma_V}{S}, \tag{10.24}$$

where S is the slew rate of the signal. Since the charging curve is not linear, the slope is not constant along the curve. Using (10.1), we can derive the slope at the moment when node $V2$ reaches αV_{DD} as:

$$\begin{aligned}\frac{dV2}{dt}|_{V2@\alpha V_{DD}} &= \frac{V_{DD}}{RC}e^{-\frac{t}{RC}}|_{t=RCln\left(\frac{1}{1-\alpha}\right)} \\ &= \frac{V_{DD}}{RC}e^{-\frac{RCln\left(\frac{1}{1-\alpha}\right)}{RC}} \\ &= \frac{V_{DD}}{RC}(1-\alpha),\end{aligned} \tag{10.25}$$

so the relationship between the σ_T and σ_V can be obtained as

$$\sigma_T \approx \left(\frac{RC}{V_{DD}(1-\alpha)}\right)\cdot\sigma_V, \tag{10.26}$$

which shows the same trend as the result derived in (10.23). The standard deviation of jitter is linearly proportional to the sensing capacitance and resistance values. Assuming Gaussian distribution, the root mean square (RMS) jitter, $Jitter_{rms}$, can be obtained directly by

$$Jitter_{rms} = \sigma_T. \tag{10.27}$$

In this design, we choose $V_{comp} = 0.5V_{DD}$ ($\alpha = 0.5$) for the comparator. Since the pulse width is determined by the time when RC charging curve reaches $V_{charge} = \alpha V_{DD}$, we can find out the relationship between the jitter and α from (10.26). Since the slope of the RC charging curve decreases with increasing α, smaller α provides better sensing resolution at the cost of sensing range. Assuming there is no jitter from the external crystal oscillator clock source, then the rising edge is only affected by the noise from the comparator and XOR circuit. Since the comparator and XOR are implemented using CMOS logic, which has high slew-rate digital signal, the jitter at the rising edge of output pulse signal is less significant. The falling edge becomes jittery due to the noise from the power supply, the noise from the external resistor, and the noise from the comparator and XOR.

Assuming jitter generation refers to the jitter produced by the sensor readout circuit itself when the input clock signal contains no jitter, as shown in Fig. 10.12, the main sources of jitter are as follows: (a) Jitter due to additive noise on the amplitude of the power supply V_{DD}, $u_{N-VDD} \sim N(0, \sigma^2_{N-VDD})$. (b) Jitter due to additive noise on the amplitude at the RC charging node from the thermal noise of the external resistor, $u_{N-Rx} \sim N(0, \sigma^2_{N-Rx})$. (c) Jitter from the electronic noises of its constituent devices in the circuit, $u_{N1} \sim N(0, \sigma^2_{N1})$, $u_{N2} \sim N(0, \sigma^2_{N2})$, and $u_{N3} \sim N(0, \sigma^2_{N3})$.

As shown in Fig. 10.13, each noise source generates σ_T which contributes to the jitter at the output pulse width. Using (10.26), the jitter, σ_{T-1st}, on the output

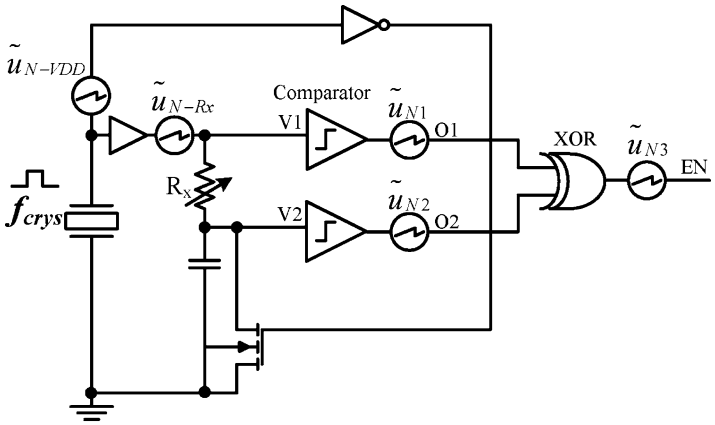

Fig. 10.12 Conceptual diagram of the noise sources in readout system

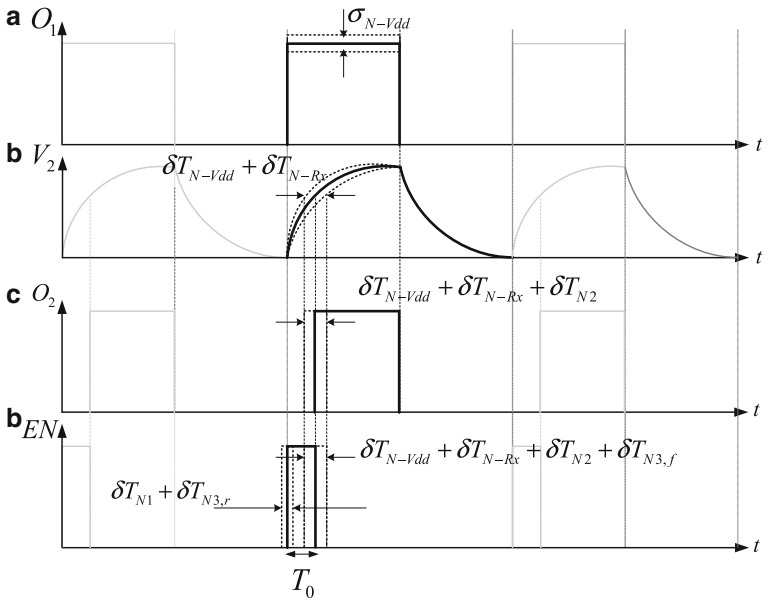

Fig. 10.13 Effect of jitter at different stages. (**a**) Clock signal after the comparator. (**b**) Signal at the RC charging node. (**c**) Signal after the comparator. (**d**) Output signal of the phase detector (XOR)

pulse width generated by the additive noise voltages u_{N-VDD} and u_{N-Rx} can be obtained as:

$$\begin{aligned}\sigma_{T-1st} &= \frac{RC}{V_{DD}(1-\alpha)} \cdot \sqrt{\sigma_{N-VDD}^2 + \sigma_{N-Rx}^2} \\ &= (\delta T_{N-VDD} + \delta T_{N-Rx})_{rms}. \end{aligned} \tag{10.28}$$

Because of the slowly changing RC charging curves, the σ_{T-1st} becomes the dominant jitter which is proportional to the sensing values. For noise sources u_{N1}, u_{N2}, and u_{N3}, we include the transistor channel thermal noise, but neglect the transistor induced gate noise since it is a blue noise and the sensor readout circuit operates at a comparably low frequency band. The jitter added by the comparator and the XOR are

$$(\delta T_{N1})_{rms} = (\delta T_{N2})_{rms} = \frac{u_{N1}}{S_{comp}}, \tag{10.29}$$

where S_{comp} is the slew rate at the output of the comparator.

$$(\delta T_{N3,r})_{rms} = \frac{u_{N3,r}}{S_{XOR}}; (\delta T_{N3,f})_{rms} = \frac{u_{N3,f}}{S_{XOR}}, \tag{10.30}$$

where S_{XOR} is the slew rate at the output of the XOR.

Equations (10.29) and (10.30) show the importance of a high bandwidth comparator and XOR designs for high resolution because S_{comp} and S_{XOR} are linearly proportional to the circuit bandwidth and u_{N1}, u_{N2}, and u_{N3} are proportional to $\sqrt{\Delta f}$. It is also important to note that the falling edge jitter is bigger than the rising edge jitter by $\delta T_{N-VDD} + \delta T_{N-Rx}$, and the falling edge jitter is linearly proportional to the sensing and reference values as described by (10.28).

Obtaining the jitter, $\sigma_{T,total}$, generated from the noises, we can estimate the resolution of capacitance and resistance measurements, C_{res} and R_{res}, using (10.17) and (10.20) as

$$C_{res} = \frac{\sigma_{T,total}}{Rln2} \tag{10.31}$$

$$R_{res} = \frac{\sigma_{T,total}}{Cln2}. \tag{10.32}$$

As described in (10.17) and Sect. 10.5.2.3, the detection range of the universal sensor interface can be reconfigured by changing the reference resistor or capacitor. The PWM output pulse width can be digitized using a digital decimator, such as a counter, to support a fine resolution yet accommodate a wide detection range at the same time.

10.5.2.5 Oversampling

The proposed readout is in effect a oversampling system with the crystal oscillator frequency f_{crys} being the sampling frequency and f_{sens} being the sampled signal frequency. Since the RC charging node is properly reset every clock cycle and the rising edge is defined by the external clock signal from a stable crystal oscillator, there is no cycle-to-cycle jitter propagation problem which is in sharp contrast to the dual-slope integrator based PWM structure[15]. Because of the independent sampling, the measurement accuracy can be improved by taking the sampled

mean of a set of consecutive measurement data. Averaging K samples while their uncorrelated random noises are folded to each sample reduces the noise variance by a factor of K, and hence the signal-to-noise-ratio (SNR) can be improved by a factor of K. This can be described through the following relationship:

$$\widehat{\sigma}_X^2 = \frac{\sigma_X^2}{K}, \tag{10.33}$$

where K is the number of averaged samples and $\widehat{\sigma}_X^2$ is the new variation after averaging. In this case, every time we increase the number of samples by a factor of 4, the resolution increases by two times. The maximum number of consecutive data to be averaged is determined by the following relationship

$$f_{crys} = K_{max} \cdot (2f_{sens}), \tag{10.34}$$

where $2f_{sens}$ indicates the Nyquist bandwidth of sensing signal. Hence, high f_{crys} can provide better resolution through averaging a large amount of samples at the cost of increased computational complexity and reduced readout dynamic range as described in (10.4) and (10.5).

10.5.3 Implementation and Measurement Results for the Universal Sensor Readout Circuit

The measurement results for the circuit implemented in a 0.13-μm CMOS technology show a capacitance readout range of 13-aF–10.7-nF and a resistance readout range of 5-Ω–11.5-MΩ with high sensitivity and resolution while drawing only 60-μA from 1-V supply. To check the sensing signal up-conversion operation described in Fig. 10.10, the power spectrum density and phase noise of the output signal is measured with test condition, $R = 3.3\text{-k}\Omega$, $C = 1\text{-pF}$, $f_{crys} = 1.5\text{-MHz}$, and $D = 80\%$. Figure 10.14 shows the up-converted sensing signal and flicker noise corner frequency around 600-kHz. Figure 10.15 shows the measured jitter on the rising and falling edges of the output pulse signal in the presence of different sensing capacitance values when $R_{ref} = 2.7\text{-M}\Omega$, $f_{crys} = 32.768\text{-kHz}$, and $D = 50\%$. As described by (10.28), (10.29), and (10.30), the falling edge jitter is bigger than the rising edge jitter and the falling edge jitter is linearly proportional to the sensing capacitance while the rising edge jitter remains constant. Table 10.1 shows performance summary and comparison with previous works. The readout circuit utilizes a RC-controlled pulse generator and produces pulse signals whose duration width is proportional to the charging time. The circuit is comprised of complementary CMOS circuit that enables the proposed design to consume significantly less power, high linearity, and low complexity compared to analog integrator based designs. This significantly low-power design is attractive for

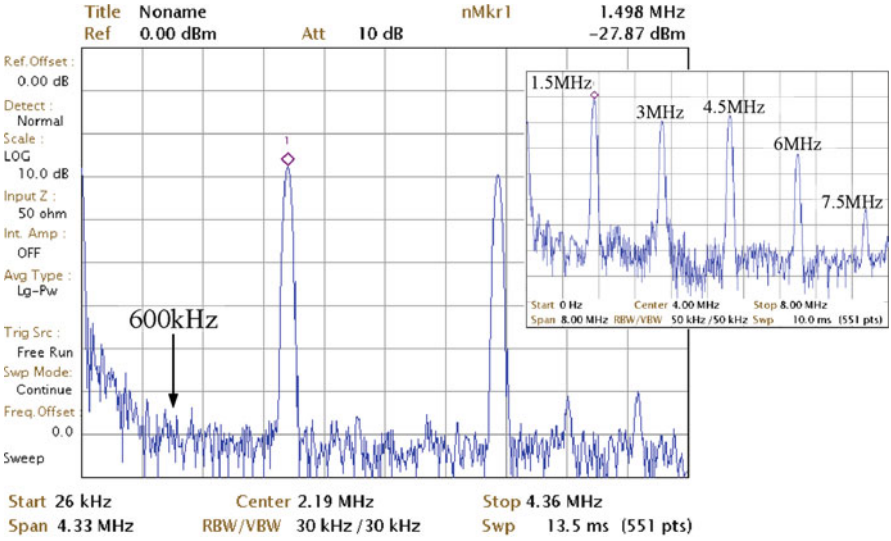

Fig. 10.14 Frequency spectrum measurement

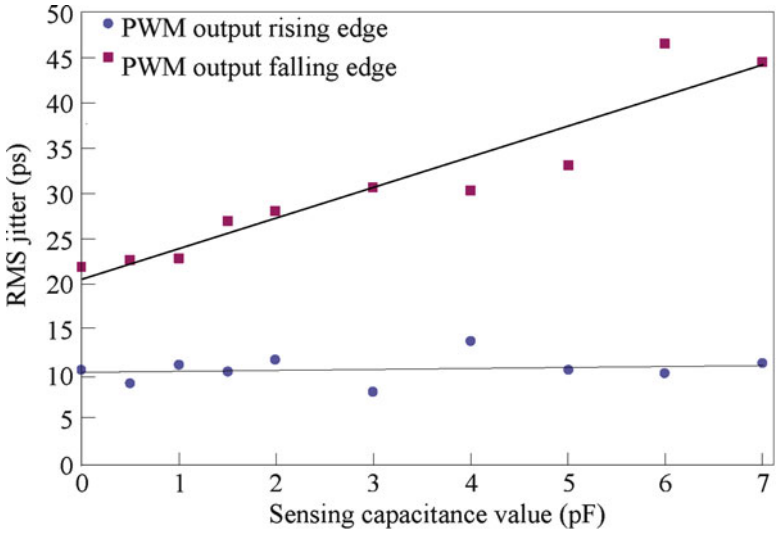

Fig. 10.15 RMS jitter on rising and falling edges of the PWM output signal versus sensing capacitance

implantable and mobile applications [19–21]. A low-complexity up-conversion process is utilized in order to address flicker noise. Sensor signal is up-converted utilizing AC excitation before it is contaminated by flicker noise. In addition, the example makes an effective use of the pulse period to provide an improvement to

Table 10.1 Performance comparison

Reference	[4]	[16]	[17]	[11]	[18]	This work[1]
Application type	C_{ap}	C_{ap}	C_{ap}	R_{es},C_{ap}	C_{ap},R_{es}	C_{ap},R_{es}
Power & V_{DD}	16.5 mW, 3.3V	1.1 mW, 5V	7 mW, 5V	3.5 mW, ±1V	21 mW, 5V	0.06 mW, 1.0V
Sensitivity	15 µs/pF @ $f_{ck} = 50$ kHz	1.25 mV/fF	N/A	N/A	N/A	7 µs/ pF(R:10 MΩ) 0.5 ns/Ω(C:800 pF)
C dynamic range	0.8 pF-1.2 pF	16 fF-40 pF	1 pF-300 pF	N/A-47 pF	N/A-300 pF	13 aF–10.7 nF[b]
R dynamic range	–	–	–	10 Ω-100 GΩ	25 Ω-10 KΩ[a]	5 Ω-11.5$M\Omega$[b]
Topology	PWM	Analog	PWM	R-to-T	PWM	PWM
Area (mm^2)	0.2	20	2.66	0.845	N/A	0.011 (0.08 with MIMcap)
Technology	0.35 µmCMOS	1 µmBiCMOS	0.7 µmCMOS	0.35 µmCMOS	N/A	0.13 µmCMOS

[a] Commercial universal transducer interface for resistive bridges 25-Ω–10-kΩ with maximum imbalance ±4% or ±0.25%

[b] The maximum resistance and capacitance are calculated using (10.3) and the measured output pulse widths, likewise the minimum resistance and capacitance are calculated using (10.3) and the measured jitters

the dynamic range of the sensor readout which makes it applicable to a wide range of resistive and capacitive sensors. It also allows the user to optimize the interface for either wide sensing range or high resolution.

10.5.4 Conclusion

In this chapter, the basic concept of analog and semi-digital sensor conditioning circuits, including capacitive and resistive sensor readout, has been introduced. Sensor conditioning circuits has been widely used to condition the output of common analog sensors. Several principles can be exploited to measure the sensor capacitance, depending on requirements of resolution, type of output signal, dynamic range, power and area budget. Since every sensor has its own requirements for readout and every user has their own applications that require different types of sensors and readouts, a reconfigurable low-power universal sensor interface is crucial for successful implementation. The exploratory of an integrated universal sensor readout circuit in this chapter satisfies the requirements of the demanding compact low-power system with a power consumption of about 60-μW. It offers compatibility with a wide range of resistive and capacitive sensors while still maintaining reconfigurable functionality.

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Chapter 11
Steady State Simulation of Mixed Analog/Digital Circuits

Federico Bizzarri, Angelo Brambilla, Giambattista Gruosso, and Giancarlo Storti Gajani

11.1 Introduction

Signal processing applications often deal with periodic or almost periodic phenomena. Efficient methods to find steady state solutions in circuits implementing these applications are thus very useful and allow the computation of relevant derived quantities such as noise. Unfortunately, steady state methods are available only for "analog" circuits and not for mixed "analog/digital" ones. For these cases, a precise definition of the concept of "analog" vs. "digital" and refined numerical methods are needed.

Defining a circuit as being *digital* or *analog*, often implying antithetic meanings to the two terms, has become in most cases useless if not even misleading. In most current system on chip (SOC) implementations, circuits are composed of cooperating subsystems that are implemented using the same silicon technology but are modelled using different approaches and different "abstraction" and detail levels. Each subsystem is responsible of a specific task and their joint operation implements the desired system function.

In this context, the terms "digital" and "analog" are standard ways to identify subsystems that are naturally modeled and designed using, respectively, discrete or continuous variable representations. During the design phase it is also quite common to initially model single parts through a very simple and high level behavioural representation that is progressively refined and detailed in a low level model as the design evolves [1]. Behavioural models can be written quickly and allow short simulation times at the cost of an often imprecise description of the real circuit.

F. Bizzarri • A. Brambilla • G. Gruosso (✉) • G. Storti Gajani
Politecnico di Milano, Dipartimento di Elettronica e Informazione,
pza. Leonardo da Vinci, 32, I20122, Milano, Italy
e-mail: bizzarri@elet.polimi.it; brambill@elet.polimi.it; gruosso@elet.polimi.it; storti@elet.polimi.it

E. Tlelo-Cuautle (ed.), *Integrated Circuits for Analog Signal Processing*,
DOI 10.1007/978-1-4614-1383-7_11,

As an example, if we consider a phase locked loop (PLL), its voltage controlled oscillator (VCO) and phase-frequency detector can be initially modelled as behavioural blocks. When a first assessment of the PLL performance is complete, the behavioural VCO model can be substituted by a more detailed transistor level description, and the phase-frequency detector by a gate level model. The digital parts of the circuit are almost always automatically synthesised starting from a high level formal description, given, for example, using the VERILOG or VHDL languages. The same approach can be applied to the design of digital to analog converters (D2As), analog to digital converters (A2Ds), switched capacitor filters, sigma delta modulators, CLASS-D amplifiers, etc. [2–4].

In a SOC each subsystem can be analyzed using the simulation tool that is most appropriate for the chosen description detail level. Digital subsystems could in principle be simulated using conventional analog tools such as SPICE-like simulators, but this is very inefficient, since the digital parts of a SOC are often composed of a huge number of components. It is much more efficient to use analog simulators to characterize and collect timing properties of simple digital cells, each composed by few tens of components, and check the functionality of the digital subsystems, that are composed by a very large number of these cells, using event-driven simulators [5–7].

After the initial design phases, where the digital and analog blocks of the circuit are simulated using different approaches and numerical algorithms, a general system simulation strategy is needed. A common approach is to perform an analog mixed signal (AMS) simulation where the digital and the analog simulators cooperate and synchronise the progress of system simulation time. In this case, pseudo-a2d (PA2D) and pseudo-d2a (PD2A) converters are inserted in the circuit netlist to adapt signal representation between the digital and the analog parts of the circuit. We defined these converters as "pseudo" since they are not part of the circuit in practice.

To the authors' knowledge, AMS simulators implement the direct current (DC) analysis, which determines at least one equilibrium point of the circuit, and the time domain (TRAN) analysis that, starting from a well defined initial condition, possibly determined by DC, computes the dynamic behaviour of the circuit [8]. Several analyses implemented in commonly used analog simulators are not available in AMS environments. Among these, those that allow to determine a periodic steady state solution, such as shooting (SH) and harmonic balance (HB); and derived ones, such as periodic small signal (PAC) and periodic noise (PNOISE), that allow to efficiently determine the small signal behaviour due to a small signal perturbation or noise that is superimposed to the circuit limit cycle in the phase space [9–12].

These analyses are largely used and useful for the design of periodic circuits such as, for example, those used for RF applications, PLLs, switched capacitor filters, etc. The unavailability of these analyses can be a serious problem, whose only solution is to find an approach that adds mixed analog/digital circuits to the class to which SH, PAC and PNOISE can be applied. This is possible if the concept of *variational model* is extended to dynamic systems that are not Lipschitz continuous.

In the sequel, a general presentation of AMS simulation methods is given, the extension of these methods to allow periodic steady state simulations is then

presented. The approach here shown has been developed starting from previous works in the field of mechanics based on the use of "saltation" matrices. Some pioneering work in the circuit analysis field and based on a similar approach can be found in [13]. A recent application of saltation matrices to the specific case of power conversion circuits can be found in [14, 15]. In these pages a unified and general framework for the use of saltation matrices in circuit simulation is presented, so to finally extend to mixed analog/digital circuits (i.e. circuits that are not Lipschitz continuous) variational model based analysis methods.

A general presentation of saltation matrices from a systems theory point of view can be found in [16].

11.2 The AMS Simulation Framework

The definition of a unified modeling framework [17] allowing the computation of the variational model of an AMS circuit, which is the core of the steady state analyses mentioned in the Introduction, can be given following a step-by-step approach. Smooth non-autonomous analog circuits are first considered, then switching non-autonomous analog circuits and, finally, AMS circuits.

11.2.1 Smooth Non-autonomous Analog Circuits

When one aims to formulate a compact and reliable model able to describe the dynamics of a well-posed smooth non-autonomous analog circuit, he can resort to the following semi-explicit index-1 differential algebraic equation (DAE)

$$\begin{cases} \dot{x} = f(x,y,t) \\ g(x,y,t) = 0 \\ x(t_0) = x_0 \\ g(x_0,y_0,t_0) = 0 \end{cases}, \tag{11.1}$$

where the *differential* state variables and *algebraic* variables of the circuit are $x(t) \in U \subset \mathbb{R}^{N_a}$ and $y(t) \in V \subset \mathbb{R}^{M_a}$, respectively, $f : \mathbb{R}^{N_a+M_a+1} \to \mathbb{R}^{N_a}$, and $g : \mathbb{R}^{N_a+M_a+1} \to \mathbb{R}^{M_a}$. In the case of smooth circuits, f and g are assumed to be continuously differentiable in their definition domain and their partial derivatives matrices are referred to as f_x, f_y, f_t, g_x, g_y, and g_t. As an example, $f_{x_{jk}} = \partial f_j / \partial x_k$, for $j,k = 1,\ldots,N_a$. In (11.1), x_0 is the initial condition of the circuit state variables at time $t = t_0$, whereas the initial condition y_0 of the algebraic variables must be chosen in order to satisfy the constraint $g(x_0,y_0,t_0) = 0$. Under the aforementioned differentiability hypotheses for g, y_0 can be evaluated through the implicit function theorem provided that $g_y(x_0,y_0,t_0)$ is not singular and a unique and smooth function

$\gamma: \mathbb{R}^{N_a+1} \to \mathbb{R}^{M_a}$ exists so that $y_0 = \gamma(x_0, t_0)$. In general, this is possible for any (x^*, y^*, t^*) such that $g_y(x^*, y^*, t^*)$ is invertible, thus allowing to obtain the sensitivity of y with respect to a parameter p from the sensitivity of x with respect to the same parameter. In fact, assuming that $(x_s(t), y_s(t))$ is the solution of (11.1) for $t \in [t_0, t_1]$, the sensitivity of this solution with respect to a system parameter $p \in \mathbb{R}$ can be computed from (11.1) as

$$\begin{cases} \dfrac{d}{dp}\dot{x}|_{x=x_s} = f_x|_{x=x_s}\dfrac{dx}{dp} + f_y\big|_{y=y_s}\dfrac{dy}{dp} \\ g_x|_{x=x_s}\dfrac{dx}{dp} + g_y\big|_{y=y_s}\dfrac{dy}{dp} = 0 \\ \dfrac{dx_0}{dp} = u_0 \end{cases} . \tag{11.2}$$

Setting $u \equiv {}^{dx}/_{dp}$ and $w \equiv {}^{dy}/_{dp}$ and interchanging the order of derivatives, we obtain

$$\begin{cases} \dot{u} = f_x|_{x=x_s} u + f_y\big|_{y=y_s} w \\ g_x|_{x=x_s} u + g_y\big|_{y=y_s} w = 0 \\ u(t_0) = u_0 \end{cases} . \tag{11.3}$$

Equation (11.3) represents a "new" *linear* and *time varying* DAE and, since we have assumed that g_y is non singular, we have

$$w = -\, g_y^{-1} g_x u \tag{11.4}$$

that, backsubstituted in (11.3), yields

$$\begin{cases} \dot{u} = \left(f_x|_{x=x_s} - f_y\big|_{x=x_s}\, g_y^{-1}\big|_{x=x_s}\, g_x|_{x=x_s} \right) u \\ u(t_0) = u_0 \end{cases} . \tag{11.5}$$

The $u(t)$ solution of the linear time-varying differential equation (11.5) leads to the sensitivity of $x_s(t)$ with respect to parameter p; the $w(t)$ sensitivity of $y_s(t)$ can be subsequently derived from (11.4).

If one is interested in evaluating the sensitivity of the solution with respects to the initial conditions, it is sufficient to introduce matrices $\Phi(t, t_0) \in \mathbb{R}^{N_a \times N_a}$ and $\Psi(t, t_0) \in \mathbb{R}^{M_a \times N_a}$ and solve

$$\begin{cases} \dot{\Phi}(t, t_0) = \left(f_x|_{x=x_s} - f_y\big|_{x=x_s}\, g_y^{-1}\big|_{x=x_s}\, g_x|_{x=x_s} \right) \Phi(t, t_0) \\ \Phi(t_0, t_0) = I_{Na} \end{cases} , \tag{11.6}$$

where I_{N_a} is the $N_a \times N_a$ identity matrix, and then evaluate $\Psi(t,t_0) = -g_y^{-1}\big|_{x=x_s} g_x\big|_{x=x_s} \Phi(t,t_0)$. From a numerical point of view, since the partial derivatives matrices in (11.6) are to be evaluated along the solution of (11.1), those differential equations are solved in parallel. The sensitivity matrix of y with respect to x_0 is then given by

$$\Psi(t,t_0) = -g_y^{-1} g_x \Phi(t,t_0). \tag{11.7}$$

If $(x_s(t), y_s(t))$ is a stable T-periodic solution of (11.1), the $\Phi(t_0+T,t_0)$ *monodromy* matrix, solution of (11.6) at $t = t_0+T$, exhibits N_a eigenvalues laying on and within the unit circle in the complex plane. If the circuit is autonomous, i.e. (11.1) does not depend explicitly on time, at least one of these eigenvalues is fixed to 1. It is worth noting that the sensitivity of y with respect to y_0 is always zero, since the algebraic variables of the circuit must satisfy, at each time instant, the constraint $g(x,y,t) = 0$ given the specific dynamics of the circuit state variables. Correspondingly, if (11.1) is written as the equivalent ordinary differential equation (ODE)

$$\begin{pmatrix} \dot{x} \\ \dot{y} \end{pmatrix} = \begin{pmatrix} f(x,y,t) \\ G(x,y,t) \end{pmatrix}, \tag{11.8}$$

where $G(x,y,t) = -g_y^{-1}(g_x f + g_t)$. If it admits a T-periodic solution, its sensitivity matrix evaluated over one period is characterized by $N_a + M_a$ eigenvalues; N_a (exactly the same of $\Phi(t_0+T,t_0)$) laying on and within the unit circle in the complex plane, and M_a identically null.

11.2.2 Saltation Matrices in Brief

Before dealing with modelling of switching non-autonomous analog circuits, we first recall here the *saltation matrix* formulation, one of the basic mathematical tools that is extensively exploited in the sequel. The reader can find for instance in [16] all the details concerning the analytical derivation of this formulation. In Sect. 11.4.2 an approach analogous to the one in [16] is used to obtain the saltation matrix expression in a specific application case. Without lack of generality we focus our attention on a basic hybrid system described by the set of ODEs

$$\begin{cases} \dot{x}(t) = f(x(t)) = \begin{cases} f_1(x(t)), & x(t) \in R_1(t) \\ f_2(x(t)), & x(t) \in R_2(t), \end{cases} \\ x(t_0) = x_0 \end{cases} \tag{11.9}$$

where $x \in \mathbb{R}^{N_a}$, f_1 and f_2 are assumed to be smooth in $\mathbb{R}^{N_a}$, and subregions R_1 and R_2 are not fixed but can vary at different time instants since they are separated by a surface $\Sigma(t)$ so that, for every $t \geq t_0$, $\mathbb{R}^{N_a} = R_1(t) \cup \Sigma(t) \cup R_2(t)$. An event manifold

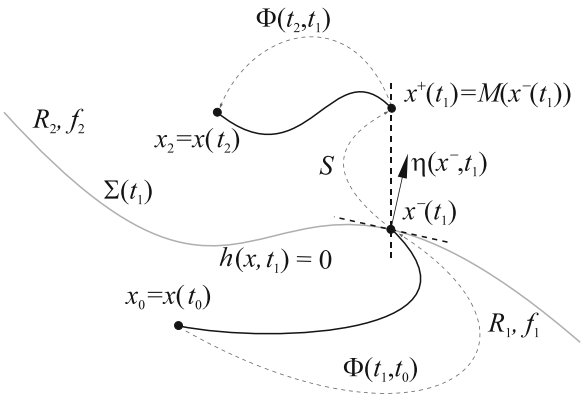

Fig. 11.1 An example of impact/switch phenomenon in $\mathbb{R}^2 = R_1 \cup \Sigma \cup R_2$

$h(x,t)$ is adopted to verify whether or not a generic point $x(t)$ belongs to either Σ, R_1 or R_2. More specifically

$$\begin{aligned} R_1(t) &= \left\{x \in R^{N_a} | h(x,t) < 0\right\} \\ \Sigma(t) &= \left\{x \in R^{N_a} | h(x,t) = 0\right\}. \\ R_2(t) &= \left\{x \in R^{N_a} | h(x,t) > 0\right\} \end{aligned} \tag{11.10}$$

The manifold $h(x,t)$ is assumed to admit $\eta = [\nabla_x^{\mathrm{T}} h(x,t), \frac{\partial}{\partial t} h(x,t)]^{\mathrm{T}}$ as normal vector for all $x(t) \in \Sigma(t)$, moreover, for all $t \geq t_0$,

$$\left[\eta^{\mathrm{T}}(x,t) f^-(x(t))\right] \cdot \left[\eta^{\mathrm{T}}(x,t) f^+(x(t))\right] > 0, \tag{11.11}$$

which means that every trajectory reaches the surface Σ transversally so that sliding motion [16] is not allowed.

As a further hypothesis, a mapping function $M(x) : \mathbb{R}^{N_a} \to \mathbb{R}^{N_a}$ is considered such that, whenever a trajectory crosses the surface Σ, for instance from R_1 to R_2 at $x(t_1) = x^-(t_1)$, the variable x is *instantaneously* mapped into $x^+(t_1) = M(x^-(t_1))$ in R_2. The dynamics of the system undergoes an *impact* at t_1 (i.e. $x^+(t_1) \neq x^-(t_1)$) and a *switch* (since $x^+(t_1) \in R_2$ implies $f = f_2$ for $t > t_1$). The Jacobian matrix of $M(x)$ will be referred to as $M_x(x)$. With reference to Fig. 11.1, assuming that $x_0 \in R_1$, $\Phi(t_1,t_0)$ can be obtained using the composition property of the sensitivity matrix, in this case as $\Phi(t_2,t_1) S \Phi(t_1,t_0)$, being

$$S = M_x(x^-(t_1)) + \frac{f_2(M(x^-(t_1))) - M_x(x^-(t_1)) f_1(x^-(t_1))}{\nabla^{\mathrm{T}} h\big|_{(x^-(t_1),t_1)} f_1(x^-(t_1)) + \frac{\partial h}{\partial t}\big|_{(x^-(t_1),t_1)}} \nabla^{\mathrm{T}} h\big|_{(x^-(t_1),t_1)}. \tag{11.12}$$

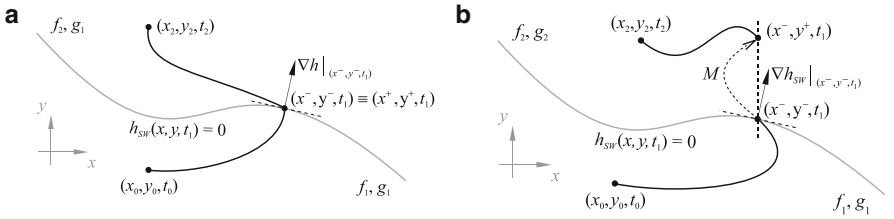

Fig. 11.2 Two different examples of two-dimensional "jumping" trajectories. In Fig. 11.2a both the differential variables x and the algebraic ones y are continuous since g undergoes no switch in correspondence with $h_{SW}(x,y,t_1)$. On the contrary, in Fig. 11.2b, $y^- \neq y^+$ since the algebraic constraint changes across $h_{SW}(x,y,t_1)$

If $M(x) = x$ (i.e. no impact occurs), (11.12) reduces to

$$S = I_{Na} + \frac{f_2(x^-(t_1)) - f_1(x^-(t_1))}{\nabla^{\mathrm{T}} h\big|_{(x^-(t_1),t_1)}\, f_1(x^-(t_1)) + \frac{\partial h}{\partial t}\big|_{(x^-(t_1),t_1)}} \nabla^{\mathrm{T}} h\big|_{(x^-(t_1),t_1)}\,. \tag{11.13}$$

11.2.3 Switching Non-autonomous Analog Circuits

A switching non-autonomous analog circuit can be basically modeled by a piecewise smooth DAE, i.e. considering f and g in (11.1) as piecewise smooth functions and introducing properly defined K_{SW} manifolds partitioning the circuit state space in non-overlapping regions where f and g are continuously differentiable. These manifolds can be written as $h_{SW,k}(x,y,t) = 0$, for $k = 1,\ldots,K_{SW}$, and it must be assumed that, for each of these manifolds, the normal vector exists and is expressed as

$$\begin{bmatrix} \eta_{x_{SW,k}}(x,y,t) \\ \eta_{y_{SW,k}}(x,y,t) \\ \eta_{t_{SW,k}}(x,y,t) \end{bmatrix} = \begin{bmatrix} \nabla_x h_{SW,k}(x,y,t) \\ \nabla_y h_{SW,k}(x,y,t) \\ \frac{\partial}{\partial t} h_{SW,k}(x,y,t) \end{bmatrix}. \tag{11.14}$$

When a trajectory "hits" one of these manifolds, say for instance at $t = t_1$, either f or g, or both, undergo a switching event which is responsible of discontinuities in $\dot{x}$ and/or y. The differential variables x in (11.1) are the circuit state variables and thus exhibit no discontinuous change, whereas the algebraic variables y can, possibly, undergo an impact event as shown in Fig. 11.2. This happens since, if the algebraic constraint changes when a given manifold is reached by a trajectory, intrinsic continuity of the differential state variables implies a "jump" in the algebraic ones (see Fig. 11.2b). In other words, adopting the superscript $^-$ and $^+$ to identify variable values immediately before and after $t = t_1$ respectively, one always has $x^+ = x^-$ and either $y^+ \neq y^-$, if g switches, or $y^+ = y^-$ otherwise. In these cases, as introduced

in Sect. 11.2.2 in the ODE case, it is still possible to define the matrices $\Phi(t,t_0)$ and $\Psi(t,t_0)$ introduced in Sect. 11.2.1 by resorting to saltation matrices and the composition property of the sensitivity matrix. Saltation matrices can be viewed as "correction factors" to be introduced whenever a trajectory of the system hits one of the aforementioned manifolds.

Consider now the more general case shown in Fig. 11.2b, in which both f and g exhibit a switch in correspondence with a generic manifold $h_{SW}(x,y,t) = 0$. It can be assumed that, starting from the initial condition (x_0,y_0) at $t = t_0$, we have

$$\begin{cases} h_{SW}(x(t),y(t),t) < 0 & t \in [t_0,t_1) \\ h_{SW}(x(t),y(t),t) = 0 & t = t_1 \\ h_{SW}(x(t),y(t),t) > 0 & t \in (t_1,t_2] \end{cases} . \tag{11.15}$$

In the following, making reference to Fig. 11.2b, functions f and g will be referred to as f_1 and g_1, or f_2 and g_2, if $h_{SW}(x(t),y(t),t) < 0$ or if $h_{SW}(x(t),y(t),t) > 0$, respectively. A further non restrictive basic assumption (already introduced in Sect. 11.2.2), is that f_k and g_k (for $k = 1,2$) are continuous and differentiable in U and V (see (11.1)). Under these assumptions, being (11.1) a semi-explicit index-1 DAE, we write (for $k = 1,2$)

$$g_{kx}(x,y,t)\dot{x} + g_{ky}(x,y,t)\dot{y} + g_{kt}(x,y,t) = 0. \tag{11.16}$$

By defining $G_k(x,y,t) = -g_{ky}^{-1}(g_{kx}f_k + g_{kt})$ (for $k = 1,2$), as it has been done in (11.8) for the smooth case, the piecewise smooth DAE modeling the switching circuit can be reformulated with the equivalent ODE

$$\begin{pmatrix} \dot{x} \\ \dot{y} \end{pmatrix} = \begin{pmatrix} f_k(x,y,t) \\ G_k(x,y,t) \end{pmatrix}. \tag{11.17}$$

To keep notation terse, in the following all the expressions evaluated at $t = t_1$ in (x^-,y^-) will be underlined whereas those evaluated in (x^+,y^+) will be overlined. To obtain all the terms needed to evaluate the saltation matrix expression given in (11.12) for this extended ODE, the implicit function theorem is applied to g_2 to identify the mapping function M (see Fig. 11.2b) relating (x^-,y^-) to (x^+,y^+),

$$(x^+,y^+) = M(x^-,y^-) = (x^-,\gamma_2(x^+,t_1)) = (x^-,\gamma_2(x^-,t_1)) = \underline{M} \ . \tag{11.18}$$

As a further consequence of the implicit function theorem, the Jacobian matrix of M evaluated at (x^-,y^-) is

$$\underline{M}_{x,y} = \begin{bmatrix} I_{N_a} & 0_{N_a \times M_a} \\ -\underline{g}_{2y}^{-1}\underline{g}_{2x} & 0_{M_a \times M_a} \end{bmatrix}, \tag{11.19}$$

where $0_{N_a \times M_a}$ is a $N_a \times M_a$ matrix whose entries are zero. The saltation matrix expression is

$$S = \underline{M}_{x,y} + \frac{\begin{pmatrix} \overline{f}_2 \\ \overline{G}_2 \end{pmatrix} - \underline{M}_{x,y} \begin{pmatrix} \underline{f}_1 \\ \underline{G}_1 \end{pmatrix}}{\left(\underline{\eta}_{x_{SW}}^T, \underline{\eta}_{y_{SW}}^T\right) \begin{pmatrix} \underline{f}_1 \\ \underline{G}_1 \end{pmatrix} + \underline{\eta}_{t_{SW}}} \left(\underline{\eta}_{x_{SW}}^T, \underline{\eta}_{y_{SW}}^T\right). \tag{11.20}$$

Notice that the denominator of the second term in the r.h.s of (11.20) does not depend on the expression g_2 assumed by g after the switching event. This term is related only to the system characteristics for $t < t_1$.

The last and fundamental step is now to derive the saltation matrices S_{Φ} and S_{Ψ} to be used directly in the DAE (and not in the extended ODE of (11.17)) to properly evaluate, also in the piecewise smooth case, Φ and Ψ, respectively. The basic idea is to keep in mind the very definition of saltation matrix and thus describe how a perturbation $(\Delta^T x^-, \Delta^T y^-)^T$, applied immediately before the switching event at $t = t_1$, is propagated and mapped in the perturbation $(\Delta^T x^+, \Delta^T y^+)^T$ observed immediately after the switching. Since, owing to the algebraic constraints in (11.1), a Δx^- perturbation of x^- results in a corresponding perturbation $\Delta y^- = -g_{1y}^{-1} g_{1x} \Delta x^-$, by applying (11.20) one can write

$$\begin{pmatrix} \Delta x^+ \\ \Delta y^+ \end{pmatrix} = S \begin{pmatrix} \Delta x^- \\ \Delta y^- \end{pmatrix} = S \begin{pmatrix} \Delta x^- \\ -g_{1y}^{-1} g_{1x} \Delta x^- \end{pmatrix}. \tag{11.21}$$

By substituting the expression of S from (11.20) in (11.21) one can write

$$\Delta x^+ = S_{\Phi} \Delta x^- = \left(\underbrace{I_{N_a} + \frac{\left(\overline{f}_2 - \underline{f}_1\right)\left(\underline{\eta}_{x_{SW}}^T - \underline{\eta}_{y_{SW}}^T \underline{g}_{1y}^{-1} \underline{g}_{1x}\right)}{\underline{\eta}_{x_{SW}}^T \underline{f}_1 - \underline{\eta}_{y_{SW}}^T \underline{g}_{1y}^{-1} \left(\underline{g}_{1x} \underline{f}_1 + \underline{g}_{1t}\right) + \underline{\eta}_{t_{SW}}}}_{S_{\Phi}} \right) \Delta x^- \tag{11.22}$$

and

$$\begin{aligned} \Delta y^+ &= S_{\Psi} \Delta x^- \\ &= \left(\underbrace{-\underline{g}_{2y}^{-1} \underline{g}_{2x} + \frac{\left(\underline{g}_{2y}^{-1} \underline{g}_{2x} \underline{f}_1 - \overline{g}_{2y}^{-1} \left(\overline{g}_{2x} \overline{f}_2 + \overline{g}_{2t}\right)\right)\left(\underline{\eta}_{x_{SW}}^T - \underline{\eta}_{y_{SW}}^T \underline{g}_{1y}^{-1} \underline{g}_{1x}\right)}{\underline{\eta}_{x_{SW}}^T \underline{f}_1 - \underline{\eta}_{y_{SW}}^T \underline{g}_{1y}^{-1} \left(\underline{g}_{1x} \underline{f}_1 + \underline{g}_{1t}\right) + \underline{\eta}_{t_{SW}}}}_{S_{\Psi}} \right) \Delta x^-. \end{aligned} \tag{11.23}$$

If just f is involved in the switching event (i.e., $g_1 = g_2$ as in Fig. 11.2a) no impact is observed on y (i.e., $y^+ = y^-$). As a consequence, mapping M reduces to $(x^+, y^+) = (x^-, y^-)$ and $\underline{M}_{x,y} = I_{N_a+M_a}$, in this case it is easy to verify that $S_\Psi = S_\Phi$.

The last step is to apply the composition property of the sensitivity matrix as in Sect. 11.2.2. With reference to Fig. 11.2, consider a trajectory originated from the initial condition (x_0, y_0) at $t = t_0$ belonging to the state-space region in which $f_k = f_1$ and $G_k = G_1$ and reaching the manifold $h_{SW}(x, y, t)$ at $t = t_1$. Then, for $t = t_1$, the switching event described above takes place and for $t \in (t_1, t_2]$ $f_k = f_2$ and $G_k = G_2$. In this case, owing to the composition property, the sensitivity matrix $\Phi(t_2, t_0)$ is given by $\Phi(t_2, t_1) S_\Phi \Phi(t_1, t_0)$ where $\Phi(t_2, t_1)$ and $\Phi(t_1, t_0)$ are "conventional" sensitivity matrices. *Mutatis mutandis* according to (11.7), $\Psi(t_2, t_0) = \Psi(t_2, t_1) S_\Psi \Psi(t_1, t_0)$.

If a generic piecewise smooth dynamical system admits a T-period solution, by properly introducing saltation matrices the same considerations done in Sect. 11.2.1 concerning the eigenvalues of the system monodromy matrix hold.

11.2.4 AMS *Circuits*

As a first step one can think of an AMS circuit as the composition of an "analog" part and a "digital/behavioral" part (see Fig. 11.3). Actually, from a purely physical point of view, the analog vs. digital distinction is in many ways artificial. When simulations of these circuits are performed, the distinction is often ruled by practical limitations (in terms of simulation times) and detail level required by the designer. For large circuits, it is common practice to represent parts of the circuit with very detailed analog models, and other parts with simplified behavioral (digital) models. The same circuit can be thus modeled in many different ways, the main goal of the mixed mode simulation is to obtain sufficiently accurate results in a reasonable simulation time.

In the analog part of the circuit all variables and time will assume real values and dynamical behaviour is modeled by a DAE (as described in Sects. 11.2.1 and 11.2.3). At the digital side all variables, except, possibly, time, are assumed as being quantized; this second part of the circuit is described by a discrete map (function $s(\cdot)$ in Fig. 11.3, representing the sequential parts of the circuit) plus, if it is necessary, some additional algebraic equations, modeling eventual pure combinatorial parts (function $c(\cdot)$ in Fig. 11.3).

The counterparts at the digital side of the *differential* and *algebraic* variables of the analog part are, respectively, the *sequential* variables $w \in \mathbb{R}^{N_d}$ and the *combinatorial* ones $v \in \mathbb{R}^{M_d}$. Since the digital and the analog domains have, in general, a different scale of values, each of these variables is remapped in the digital and analog parts, thus obtaining x_d, y_d and w_a, v_a, respectively. To do this a set of mapping functions is needed

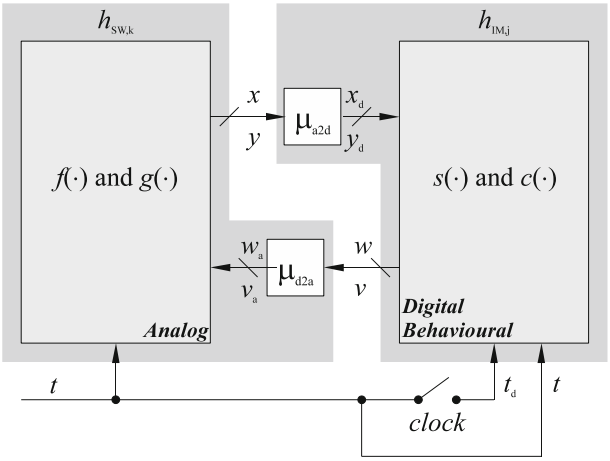

Fig. 11.3 The generic architecture of an AMS circuit. The time variable t is assumed, at least in principle, to be available at both sides of the circuit. In particular, in the digital part, both a clock signal t_d and the continuous variable t are available. Clock-time can trigger sequential events and the continuous variable can be used to store the value of t at specific events if one is interested, for instance, in producing delayed digital outputs

$$\begin{cases} x_d = \mu_{a2d}(x) \\ y_d = \mu_{a2d}(y) \\ w_a = \mu_{d2a}(w) \\ v_a = \mu_{d2a}(v) \end{cases} \tag{11.24}$$

that, in the simplest case, are PA2D and PD2A converters. Using this notation, as shown in Fig. 11.3, variables x_d and y_d have the role of "input" to the digital part, while variables w_a and v_a can be considered as input to the analog part. To take into account the influence of these new variables, (11.1) can be rewritten as

$$\begin{cases} \dot{x} = f(x,y,t;\mu_{d2a}(w),\mu_{d2a}(v)) \\ g(x,y,t;\mu_{d2a}(w),\mu_{d2a}(v)) = 0 \\ x(t_0;\mu_{d2a}(w_0),\mu_{d2a}(v_0)) = x_0 \\ g(x_0,y_0,t_0;\mu_{d2a}(w_0),\mu_{d2a}(v_0)) = 0 \end{cases} . \tag{11.25}$$

From the notation used in (11.25), it can be thought that the digital variables mapped in the analog domain act as parameters. It is crucial to highlight that these parameters are time-varying and their evolution is governed by

$$\begin{cases} w(t_{n+1}) = s(w(t_n),v(t_n),t_n;\mu_{a2d}(x(t_n)),\mu_{a2d}(y(t_n))) \\ c(w(t_{n+1}),v(t_{n+1}),t_{n+1};\mu_{a2d}(x(t_{n+1})),\mu_{a2d}(y(t_{n+1}))) = 0 \\ w(t_0;\mu_{a2d}(x_0),\mu_{a2d}(y_0)) = w_0 \\ c(w_0,v_0,t_0;\mu_{a2d}(x_0),\mu_{a2d}(y_0)) = 0 \end{cases} . \tag{11.26}$$

Evaluation of (11.26) is performed at time instant t_{n+1} in correspondence to the occurrence of external or internal events, e.g. transition of a clock signal, change of value of one or more input signal, etc. The values used in the r.h.s. of map s are evaluated at a previous time instant t_n. The time step $t_{n+1} - t_n$ can have a fixed value in clocked digital systems or any value (and even tend to zero) if the digital part is event driven.

Functions f and g in (11.25), as it has been done in Sect. 11.2.3 to deal with hybrid non autonomous analog circuits, are assumed to be continuously differentiable in a set of regions of the state space delimited by a proper set of switching manifolds. Note that switching phenomena are now ruled also by w and v. As matter of fact, even under the simplest assumption that both f and g are continuously differentiable in all their definition domain, a discontinuity in the digital variables can be interpreted as a switching event for those functions. To summarize, at the analog side one can observe the phenomena described in Sect. 11.2.3 owing to both the nature of functions f and g themselves, and the influence of variations of w and v. As a consequence the switching manifolds must be re-written as $h_{SW,k}(x,y,t;\mu_{d2a}(w),\mu_{d2a}(v)) = 0$, for $k = 1,\ldots,K_{SW}$.

At this point it is essential to focus on the dynamics of the digital part of the circuit and variables w will be first considered. These variables, if analyzed from the continuous time domain point of view, are characterized by an always null time derivative but in correspondence with those events that are responsible of their discontinuous variation, where their derivative is not defined. These (impact) events take place in correspondence to the occurrence of external or internal events and can thus be associated to impact manifolds. In the simplest case, w variables undergo impact events because the outputs of μ_{a2d} converters, that are stored in w-type variables, change. This kind of situation induces a subset of manifolds depending on x and y. A further cause of change of variables w is due to the evolution of map s. This may occur because of (1) a clock signal (in this case simple manifolds depending only on t are to be considered), (2) a variation of variables w depending on the μ_{a2d} converters outputs, or (3) a variation of variables v. In the last case, some of the variables v must change so that the (algebraic) combinatorial constraints c still hold when any of the variables w, storing the output x_d and y_d of μ_{a2d} converters, are changed. To summarize, discontinuous variations of w may occur when proper impact manifolds $h_{IM,j}(w,v,t;x,y) = 0$, for $j = 1,\ldots,J_{IM}$, are reached by the system trajectory.

The only difference between the manifolds $h_{SW,k}$ and $h_{IM,j}$ is that the former depend on the digital to analog conversion of w and v whereas the latter directly depend on x and y. This discrepancy is due to the fact that the μ_{a2d} converters are directly involved into the formulation of $h_{IM,j}$ and can be viewed as belonging to the digital side. For the sake of symmetry, the μ_{d2a} converters can be included in the analog part and, more specifically, in the very formulation of functions f, g, and $h_{SW,k}$. This is represented by the darker gray regions in Fig. 11.3.

As a last preliminary step, the reset functions ruling the variations of w and v must be analyzed. As far as w is concerned, the μ_{a2d} converters and the map s are directly responsible of assigning to w^+ proper values whenever an impact manifold

is reached at a given time instant $t = t_1$. The value v^+ of the algebraic variables is in turn computed by resorting to function c. In the most general situation both w^+ and v^+ are evaluated through a map M depending on x^-, y^-, w^-, and v^- as discussed in Sect. 11.2.3 in relation to y^+. Since (1) w and v can assume only discrete values and (2) the analytic expressions of s, c, and μ_{a2d} are not in general differentiable (for instance think of a combinatorial function c made up of logical operators), the reset functions acting on w^- and v^- will be treated as simple assignments $M(x^-, y^-, w^-, v^-) = \text{constant}$.

The above assumption is crucial and its effects must be highlighted. A direct consequence is that the Jacobian matrix $M_{w,v}$ of the reset function M is a diagonal matrix Λ whose entries $\Lambda_{q,q}$ (for $q = 1, \ldots, N_d + M_d$) are 1, if the corresponding digital variable w or v is unchanged by M, and 0 otherwise. Moreover, from a more conceptual point of view, a constant M means that no *direct* perturbations are allowed at the digital side; its time evolution can be only *indirectly* perturbed by the analog part of the circuit. The effect of this perturbation can be interpreted as *jitter* at the digital side, since it simply affects the time instant at which impact events may occur but does not modify the values assumed by w^+ and w^-.

Finally, by introducing a new differential variable $z = (x^T, w^T, v^T)^T$, the whole AMS circuit is described as follows

$$\begin{cases} \dot{z} = \begin{pmatrix} f(x,w,v,y,t) \\ 0 \\ 0 \end{pmatrix} = F(z,y,t) \\ g(z,y,t) = 0 \\ z(t_0) = (x_0^{\mathrm{T}}, w_0^{\mathrm{T}}, v_0^{\mathrm{T}})^{\mathrm{T}} \\ g(z_0,y_0,t_0) = 0 \\ c(z_0,y_0,t_0) = 0 \end{cases}, \tag{11.27}$$

together with the manifolds

$$\begin{cases} h_{SW,k}(z,y,t) = 0, & k = 1, \ldots, K_{SW} \\ h_{IM,j}(z,y,t) = 0, & j = 1, \ldots, J_{IM} \end{cases}, \tag{11.28}$$

and their normal vectors

$$\begin{bmatrix} \eta_{z_\Theta} \\ \eta_{y_\Theta} \\ \eta_{t_\Theta} \end{bmatrix} = \begin{bmatrix} \nabla_z h_\Theta \\ \nabla_y h_\Theta \\ \frac{\partial}{\partial t} h_\Theta \end{bmatrix}, \tag{11.29}$$

where Θ is either $\{SW, k\}$ or $\{IM, j\}$. For the sake of simplicity, in the following, whenever possible, symbol Θ will be omitted.

The sensitivity matrix of system (11.27) can be computed as introduced in Sect. 11.2.3 by assuming that (1) both functions F and g in (11.27) are piecewise

continuously differentiable and (2) the implicit function theorem can still be applied to g. Matrices Φ and Ψ are now $\mathbb{R}^{N_a+N_d+M_d} \times \mathbb{R}^{N_a+N_d+M_d}$ and $\mathbb{R}^{M_a} \times \mathbb{R}^{N_a+N_d+M_d}$, respectively.

Saltation matrix S_Φ can be evaluated as in Sect. 11.2.3, and DAE (11.27) can be written as an equivalent ODE as it has been done for (11.1) in (11.17). Then the analogous of (11.20) can be derived and matrix $M_{z,y}$ is obtained. In this case this matrix exhibits the following structure

$$M_{z,y} = \begin{bmatrix} \Gamma & 0_{(N_a+N_d+M_d)\times M_a} \\ -g_y^{-1} g_z & 0_{M_a \times M_a} \end{bmatrix}, \tag{11.30}$$

where

$$\Gamma = \begin{bmatrix} I_{N_a} & 0_{N_a \times (N_d+M_d)} \\ 0_{(N_d+M_d)\times N_a} & \Lambda \end{bmatrix}. \tag{11.31}$$

Saltation matrix S_Φ can then be written as

$$S_\Phi = \Gamma + \frac{\left(\overline{F}_2 - \Gamma \underline{F}_1\right)\left(\underline{\eta}_z^{\mathrm{T}} - \underline{\eta}_y^{\mathrm{T}} \underline{g}_{1y}^{-1} \underline{g}_{1z}\right)}{\underline{\eta}_x^{\mathrm{T}} \underline{f}_1 - \underline{\eta}_y^{\mathrm{T}} \underline{g}_{1y}^{-1}\left(\underline{g}_{1x}\underline{f}_1 + \underline{g}_{1t}\right) + \underline{\eta}_t}. \tag{11.32}$$

As in the analog case, if g is continuously differentiable in all its definition domain, (11.30) becomes

$$M_{z,y} = \begin{bmatrix} \Gamma & 0_{(N_a+N_d+M_d)\times M_a} \\ 0_{M_a \times (N_a+N_d+M_d)} & I_{M_a} \end{bmatrix}. \tag{11.33}$$

It is easy to show that, in both this last case and the previous one, the saltation matrix S_Ψ is exactly the same as in the analog case.

11.3 Time Domain Periodic Steady State Algorithms

The basic time domain periodic steady state simulation method is the well known SH which allows to efficiently obtain (if it exists) a limit cycle corresponding to a periodic steady-state solution of the circuit being analysed or designed. Once this limit cycle has been obtained, two other time domain periodic steady state simulation methods are typically adopted, PAC and PNOISE (see for instance [9–11, 18–20]), which are used to determine, with an acceptable computational effort, the small signal behaviour due to a small signal perturbation or noise, respectively, that is superimposed to the available limit cycle.

We limit here our discussion to SH since, once it is shown how it can be extended to the proposed AMS simulation framework, it will be worth extending also the

other two simulation methods. SH can be formulated in different ways, here a simple presentation of one of these is briefly given, a more thorough analysis can be found in [21, 22].

The first important assumption that must be made is that system (11.27) admits a limit cycle as a steady-state solution and that an initial condition x_0 sufficiently close to the cycle is known. In this case, if a smooth ODE is considered (i.e. there are no algebraic equations, no digital parts, and no vector field switchings) the solution is relatively simple and well known. Denote with $x_s(t) = x_s(t + T_s)$ the expected periodic solution of unknown period T_s and augment the original ODE with equation $dT/d\tau = 0$, where T is the unknown period of solution $x_s(t)$ and, having adopted the transformation $\tau = t/T$ is such that the period of the transformed problem is equal to 1.

The boundary conditions that must be specified for the transformed problem must force the trajectory that is found to be closed and, for autonomous systems, must specify a phase condition s that ensures that the boundary-value problem (BVP) has a unique solution

$$\begin{cases} x(1) - x(0) = 0 \\ s(x(0), T) = 0 \end{cases}, \tag{11.34}$$

The nonlinear equation solved by SH for this BVP is

$$\begin{cases} r(x(0), T) = \varphi(x(0), T) - x(0) = 0 \\ s(x(0), T) = 0 \end{cases}, \tag{11.35}$$

where $\varphi(x(0), T)$ is the solution of the initial-value problem at $t = T$, from initial condition $x(0)$.

Equation (11.35) can be solved using a Newton method, solving at each step a linear equation whose coefficients matrix is

$$\begin{bmatrix} \varphi_x - I_{N_a} & \varphi_T \\ s_x & s_T \end{bmatrix} \tag{11.36}$$

where, at the i-th iteration, the entries of (11.36) are evaluated at the current approximation $(x^{(i)}(0), T^{(i)})$.

When the Newton iterative method converges, an initial condition $x^*(0)$ on the limit cycle and the cycle period T^* are found, moreover,

$$\Phi = \varphi_x|_{(x^*(0), T^*)} \tag{11.37}$$

is the correct sensitivity matrix.

If switching events are present, SH can be easily generalized by introducing saltation matrices, in the following we will call this method including all related auxiliary algorithms *discontinuous shooting* (DSH). The Newton method yields at

each time step t_n the sensitivity matrix $\Phi(t_n,t_{n-1})$ and $\Phi(1,0)$ can be derived as the *left product* [23]

$$\Phi(1,0) = \prod_{n=1}^{N_s} \Phi(t_n,t_{n-1}). \tag{11.38}$$

If switching events are located at known time instants, it is sufficient to insert in the above left product a saltation matrix S_Φ at each event. If, as an example, there are two discontinuities in the vector field at time samples $n = N_1$ and $n = N_2$ $(N_1 < N_2)$, (11.38) becomes

$$\begin{aligned}\Phi(1,0) = &\left(\prod_{n=N_2+1}^{N_S} \Phi(t_n,t_{n-1})\right) S_{\Phi_{N_2}} \cdot \\ &\cdot \left(\prod_{n=N_1+1}^{N_2} \Phi(t_n,t_{n-1})\right) S_{\Phi_{N_1}} \cdot \left(\prod_{n=1}^{N_1} \Phi(t_n,t_{n-1})\right).\end{aligned} \tag{11.39}$$

Extension to the DAE case is rather straightforward and is detailed in [17].

In the general case, the AMS circuit is modelled by (11.27) and, since w and v can assume only discrete values, at each Newton iteration i providing the next $z^{(i+1)}(0)$, only $x^{(i+1)}(0)$ are to be directly considered as the initial condition for the next step of the time domain analysis, whereas $w^{(i+1)}(0)$ and $v^{(i+1)}(0)$ are to be evaluated according to the relations enforced by the digital part of the circuit.

11.4 Localization of the Switching and Impacting Manifolds

A main ingredient for the computation of the correct fundamental matrix for generic AMS circuits are the saltation matrices introduced in (11.20) and (11.32). These formulas require knowledge of the $h_{SW,IM}(z,y,t)$ manifolds and of their normal vector, and this can in some cases require some further analysis.

In the AMS circuit simulation context it is possible to distinguish between two different types of manifolds, the *extrinsic* ones and the *intrinsic* ones. Manifolds of the former type are known a priori and can be easily formalised, as, for example, the PA2D pseudo-converters: in this case the thresholds that define the corresponding digital code are known a priori. Manifolds of the latter type are not known a priori and must be determined run-time during the circuit simulation.

In the next two sections we present, respectively, an approach to automatically locate intrinsic manifolds and an algorithm to efficiently manage extrinsic ones.

11.4.1 Automatic Location of Intrinsic Manifolds

Consider the DAE described in (11.27) and perform one integration step of the time domain analysis, which is at the base of SH. Assume to know the $x(t_n)$ and $y(t_n)$ components of the solution at the t_n time instant and to compute the

same components at $t_{n+1} = t_n + h_n$, where h_n is the integration time step. The $\dot{x}(t_{n+1})$ and $\dot{y}(t_{n+1})$ derivatives are directly available from the evaluation of the $f(x(t_{n+1}), w(t_{n+1}), v(t_{n+1}), y(t_{n+1}), t_{n+1})$ vector field and $g(x(t_{n+1}), y(t_{n+1}), t_{n+1})$ in (11.27). The $\dot{r}(t_{n+1})$ and $\dot{s}(t_{n+1})$ estimates of $\dot{x}(t_{n+1})$ and $\dot{y}(t_{n+1})$, can be computed, respectively, through the sensitivity matrices $\Phi(t_{n+1}, t_n)$ and $\Psi(t_{n+1}, t_n)$ as

$$\begin{bmatrix} \dot{x}(t_{n+1}) \\ \dot{w}(t_{n+1}) \\ \dot{v}(t_{n+1}) \\ \dot{y}(t_{n+1}) \end{bmatrix} \simeq \begin{bmatrix} \dot{r}(t_{n+1}) \\ \cdots \\ \cdots \\ \dot{s}(t_{n+1}) \end{bmatrix}$$

$$= \begin{bmatrix} \Phi(t_{n+1}, t_n) & 0_{N_a+N_d+M_d \times M_a} \\ 0_{M_a \times N_a+N_d+M_d} & \Psi(t_{n+1}, t_n) \end{bmatrix} \begin{bmatrix} \dot{z}(t_n) \\ \dot{y}(t_n) \end{bmatrix} + \begin{bmatrix} F_t(z(t_n), y(t_n), t_n) \\ g_t(z(t_n), y(t_n), t_n) \end{bmatrix}, \quad (11.40)$$

where the known term is different from zero only in non-autonomous circuits. If f and g are smooth functions we have

$$\lim_{h_n \to 0} \left| \overbrace{\begin{pmatrix} \dot{r}(t_{n+1}) \\ \dot{s}(t_{n+1}) \end{pmatrix}}^{\widetilde{\chi}(t_{n+1})} - \overbrace{\begin{pmatrix} \dot{x}(t_{n+1}) \\ \dot{y}(t_{n+1}) \end{pmatrix}}^{\widehat{\chi}(t_{n+1})} \right| = \zeta_{n+1} = 0. \quad (11.41)$$

Consider now inequality

$$\zeta_{n+1,j} \leq \psi_{n+1,j} = \alpha_{\text{rel}} \min\left(\left| \widetilde{\chi}_j(t_{n+1}) \right|, \left| \widehat{\chi}_j(t_{n+1}) \right| \right) + \alpha_{\text{abs}} \quad (11.42)$$

where subscript $_j$ identifies the j-th component, $0 < \alpha_{\text{rel}} < 1$ represents a relative tolerance threshold and $\alpha_{\text{abs}} \in \mathbb{R}^+$ represents the absolute one. Along the time domain integration of (11.27), (11.42) is used as a monitor function to locate jumps in the vector field. Any time (11.42) is not satisfied the integration time step h_n is shortened and the integration procedure is repeated. If the value of h_n becomes smaller than the minimum allowed step $h_{\min}$ determined by the relative precision ε of the ALU and inequality (11.42) is still unsatisfied, then it is possible to conclude that f and/or g are not "sufficiently" smooth or, equivalently, that there is a "jump" and thus introduce a saltation matrix. This "cut and try" mechanism ensures that the manifold is located in time with an accuracy limited by ε, i.e. the best possible one. In case of a "false alarm", since f and g are smooth, the S_Φ and S_Ψ saltation matrices in (11.22) and (11.23) simply reduce to the identity matrix. False jumps can be due to modeling functions such as $a(t) = \tanh(kb(t))$ that are C^∞, but that can be seen as discontinuous during their *numerical* evaluation if the $|kb(t)|$ argument undergoes large variations. In this case the $h(z, y, t)$ equation of the manifold *does not exist*, but, during simulations, "numerical manifolds" have to be anyway located and saltation matrix exploited to accurately compute the fundamental matrix.

When a jump has been located in time, its normal vector must be computed. We assume that, locally, the manifold is modeled with sufficient accuracy by the linear equation

$$\begin{bmatrix} z^{\mathrm{T}} & y^{\mathrm{T}} & t \end{bmatrix} \begin{bmatrix} \eta_z \\ \eta_y \\ \eta_t \end{bmatrix} - b = 0 \tag{11.43}$$

where b can assume only the 0 and 1 values. The number of unknowns in (11.43) is $(N_a + M_a + N_d + M_d + 1)$, therefore, the same number of independent scalar equations is needed to determine the entries of the η_z, η_y and η_t unknown vectors. We "explore" F and g in a neighborhood of the manifold by starting from the $(z^- - \delta_z, t^- - \delta_t)$ solution (see Fig. 11.2), y is derived using g. Increments δ_z and δ_t are chosen so that we remain in the portion of the vector field laying before the manifold traversal point but sufficiently far to ensure an acceptable condition number of the matrix related to the linear problem in (11.43). We explore F and g by linearly varying one by one each of the analog state variable components of z_j $(j = 1, \ldots, N_a)$. Specifically, the value of $\left|\delta_{z,j}\right|$ is increased until the maximum allowed value $\delta_{z,j}^{\max}$ while checking if there is a sharp variation of a component of F and g. The value of $z + \delta_{z,j}$ and y at which there is the jump is substituted in scalar equation (11.43) and we set $b = 1$. This procedure is repeated for each component of z and for t. Note that each sweep exclusively requires evaluations of F and g and is thus very efficient.

If a sweep till $\delta_{z,j}^{\max}$ does not show any sharp variation of F or g, then the manifold does not depend on this specific z_j component; in this case we set $z_j = 1$, all the other entries of z and y equal to 0 and $b = 0$. The same mechanism is applied to time t. At the end of this process the set of scalar equations (11.43) forms a linear problem that can be solved for η_z, η_y and η_t.

11.4.2 An Algorithm to Efficiently Manage Extrinsic Manifolds

As a first assumption we will consider an AMS circuit modeled by (11.27)–(11.29) in the special case in which its analog part is described by an ODE (i.e., no algebraic variables y are present at the analog side) and the switching manifolds $h_{SW,k}(z)$ (for $k = 1, \ldots, K_{SW}$) depend on w and v only. The first assumption can subsequently be removed thus generalizing the method also to DAEs. The second assumption means that switching phenomena at the analog side of the circuit are driven just by digital events transferred to the analog side by PD2As. These events will be identified in the following by generic manifolds $h_{\mathrm{PD2A}}(z)$. The digital part of the circuit, in turn, is driven by the evolution of an external time signal triggering digital events and by the outputs of PA2Ds providing it with evolving values x_d to be processed. The latter events will be associated with the $h_{\mathrm{PA2D}}(z)$ manifolds.

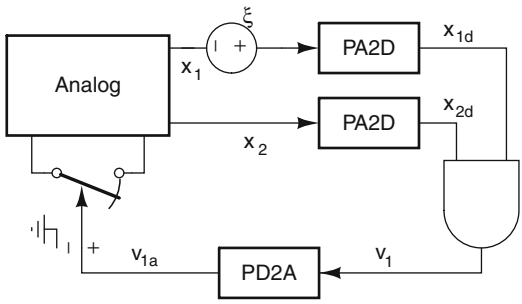

Fig. 11.4 A simple example of AMS circuit. The AND logic gate is assumed to be characterized by a delay Δt in its elaboration time. ξ is a noise voltage source

All the aforementioned manifolds are extrinsic since their analytical expressions are provided by PA2Ds and PD2As, whose "mapping functions" are assigned when the AMS circuit is designed.

One can now ask himself how a perturbation applied to the analog part of the circuit propagates its effect through the digital one and then how it comes back. This is interesting since, if we assume to have noise at the analog part of the circuit, it affects the analog variables x causing uncertainty at the input of PA2Ds and, consequently, affecting the time instants at which the x_d variables change. This, in turn, causes a variation in the time instant at which PD2As "communicate" at the analog side, through w_a and v_a, the output of the digital elaboration driven by the evolution of x_d and, consequently, its effect on the dynamics of x. If we stop at this level of analysis, one might be convinced that each event modeled by a $h_{\mathrm{PA2D}}(z)$ manifold *always* has repercussions on the effects, at the analog side, of a related $h_{\mathrm{PD2A}}(z)$-manifold modeled event. In fact this is not the case. A simple example is given in Fig. 11.4 where the digital (combinatorial) part of the circuit is simply made up of a logic AND gate characterized by a delay Δt in its elaboration time. The v_1 output of such a gate is passed to the analog part of the circuit to drive, for instance, an ideal switch. The inputs of the gate are two properly digitally converted analog variables x_1 and x_2, the former being perturbed by a noise source ξ. We can imagine to choose an initial condition for the circuit at $t = t_0$ so that $x_{1_d}(t_0) = x_{2_d}(t_0) = 0$ (in the following 0 and 1 stand for the logical values *false* and *true*, respectively). Assume now ξ to be null and the evolution of the analog part of the circuit to be such that $x_{1_d} = 1$ and $x_{2_d} = 1$ in t_1 and t_2, respectively, with $t_1 < t_2$. It is evident that $v_{1_a}(t_2 + \Delta t) = 1$. Assume now $\xi \neq 0$, in this case $x_{1_d} = 1$ at $t = t_1 + \Delta t_1$ but, if $t_1 + \Delta t_1 < t_2$, one will always observe $v_{1_a}(t_2 + \Delta t) = 1$. This means that the effect of perturbing x_1 is not propagated back from the digital part of the circuit to the analog one. Exactly the opposite behaviour would be obtained by perturbing x_2 instead of x_1.

Through this simple example it should be clear that, in general, when analyzing the dynamics of an AMS circuit, all the events at the digital side driven by PA2Ds should be tracked in order to identify which one is the last responsible of a subsequent PD2A event. Each event can be tagged at the analog/digital interface and these tags are propagated in the digital elaboration and finally used, if necessary, at

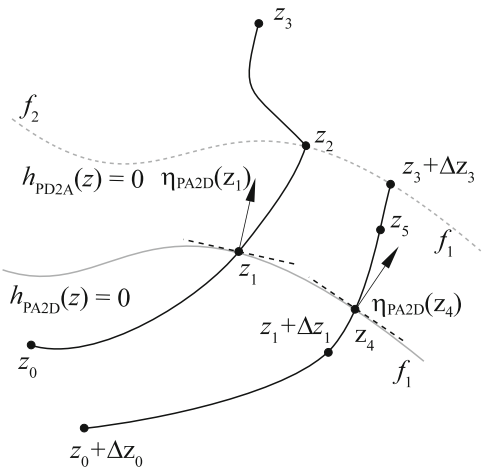

Fig. 11.5 Nominal (starting from initial condition z_0) and perturbed (from $z_0 + \Delta z_0$) trajectories. Manifolds $h_{PA2D}(z)$ and $h_{PD2A}(z)$ represent, respectively, switching of a PA2D and of a PD2A, only the latter represents a change of vector field and, hence, a switching condition. This sketch represents the projection of the system trajectory on the analog state variables subspace

the digital/analog interface. The algorithm we show in the following exploits exactly this idea properly "composing" saltation matrices during the analysis of the circuit dynamics.

Before proceeding, another important consideration must be done concerning the digital elaboration time. In general, it makes sense assuming that the effects of an event driven by a PA2D can be always observed at the analog side after an even brief time interval. This time interval can depend on either the intrinsic delays of the digital part, or the digital part elaboration time, or a fixed time chosen by the circuit designer as it happens, for instance, in pulsed energy restored oscillators [24]. In general, when a given h_{PA2D} is reached, the derivative of the continuous trajectory of the x-variables exhibits no discontinuity. Keeping this concept in mind, let's consider Fig. 11.5 in which previous assumptions have been graphically summarized. By referring to this figure, we imagine to compute the system sensitivity matrix along a trajectory starting from z_0 and evolving in the region where f_1 is the active vector field. At z_1 the $h_{PA2D}(z)$ boundary introduced by a PA2D is traversed and its digital output code changes; however, there is no jump in the vector field at the analog side. At z_2 there is a "jump" in the vector field caused by the switching of a PD2A; this is formalised by traversal of the $h_{PD2A}(z) = 0$ manifold. The trajectory then evolves from z_2 to z_3 showing a cusp in z_2. In this specific case we want to derive the expression of the $\widehat{S}$ saltation matrix finding out (at first order) how the Δz_0 perturbation of the state z_0 at t_0 affects the deviation of the trajectory from z_3 to $z_3 + \Delta z_3$ at $t = t_0 + t_{PA2D}(z_0 + \Delta z_0) + \widehat{\Delta t}$ being

- $t_{PA2D}(z(t_0))$ the time needed to reach the $h_{PA2D}(z)$ manifold (i.e. switching of a PA2D) from $z(t_0)$.
- $\widehat{\Delta t}$ the fixed time interval that must elapse after the switching of the PA2D before observing a switch in the vector field of the analog part of the circuit; this happens when the trajectory reaches the manifold $h_{PD2A}(z) = z - \varphi^{t_0 + t_{PA2D}(z(t_0)) + \widehat{\Delta t}}(z(t_0))$.

- $\varphi^t(z(t_0))$ the system trajectory evaluated at t and originated in $z(t_0)$.

Furthermore, without losing generality, it is assumed that $t_{\mathrm{PA2D}}(z_0 + \Delta z_0) = t_{\mathrm{PA2D}}(z_0) + \widetilde{\Delta t}$ with $\widetilde{\Delta t} > 0$. In particular, we are interested in deriving $\widehat{S}$ such that

$$\Delta z_3 = \widehat{S} \Delta z_1. \tag{11.44}$$

To obtain a simpler notation we define (see Fig. 11.5)

$$\begin{aligned}
z_1 &= \varphi^{t_0 + t_{\mathrm{PA2D}}(z_0)}(z_0) \\
z_1 + \Delta z_1 &= \varphi^{t_0 + t_{\mathrm{PA2D}}(z_0)}(z_0 + \Delta z_0) \\
z_2 &= \varphi^{t_0 + t_{\mathrm{PA2D}}(z_0) + \widehat{\Delta t}}(z_0) \\
z_3 &= \varphi^{t_0 + t_{\mathrm{PA2D}}(z_0 + \Delta z_0) + \widehat{\Delta t}}(z_0) \\
z_3 + \Delta z_3 &= \varphi^{t_0 + t_{\mathrm{PA2D}}(z_0 + \Delta z_0) + \widehat{\Delta t}}(z_0 + \Delta z_0) \\
z_4 &= \varphi^{t_0 + t_{\mathrm{PA2D}}(z_0 + \Delta z_0)}(z_0 + \Delta z_0) \\
z_5 &= \varphi^{t_0 + t_{\mathrm{PA2D}}(z_0) + \widehat{\Delta t}}(z_0 + \Delta z_0)
\end{aligned} \tag{11.45}$$

As a first step it is possible to write

$$\begin{aligned}
z_3 &\approx z_2 + f_2(z_2)\widetilde{\Delta t} \\
z_3 + \Delta z_3 &\approx z_5 + f_1(z_5)\widetilde{\Delta t} \approx z_5 + f_1(z_2)\widetilde{\Delta t}
\end{aligned}, \tag{11.46}$$

and then

$$\begin{aligned}
&0 = h_{\mathrm{PA2D}}(z_4) \approx \\
&\approx h_{\mathrm{PA2D}}(z_1 + \Delta z_1 + f_1(z_1 + \Delta z_1)\widetilde{\Delta t}) \approx \\
&\approx h_{\mathrm{PA2D}}(z_1 + \Delta z_1) + \eta^{\mathrm{T}}_{\mathrm{PA2D}}(z)\big|_{z_1 + \Delta z_1} f_1(z_1 + \Delta z_1)\widetilde{\Delta t} \approx \\
&\approx \eta^{\mathrm{T}}_{\mathrm{PA2D}}(z)\big|_{z_1} \Delta z_1 + \eta^{\mathrm{T}}_{\mathrm{PA2D}}(z)\big|_{z_1} f_1(z_1)\widetilde{\Delta t}.
\end{aligned} \tag{11.47}$$

From (11.47) and (11.46) we have

$$\widetilde{\Delta t} = -\frac{\eta^{\mathrm{T}}_{\mathrm{PA2D}}(z)\big|_{z_1} \Delta z_1}{\eta^{\mathrm{T}}_{\mathrm{PA2D}}(z)\big|_{z_1} f_1(z_1)},$$

and $\Delta z_3 = z_2 - z_5 + (f_2(z_2) - f_1(z_2))\,\widetilde{\Delta t}$, respectively. By defining Φ_{ik} the system sensitivity matrix evaluated on the trajectory originated from z_k and ending in z_i, since

$$z_2 - z_5 = \Phi_{21} \Delta z_1,$$

we finally obtain

$$\widehat{S} = \Phi_{21} + \frac{(f_2(z_2) - f_1(z_2))}{\eta^{\mathrm{T}}_{\mathrm{PA2D}}(z)\big|_{z_1} f_1(z_1)}\, \eta^{\mathrm{T}}_{\mathrm{PA2D}}(z)\big|_{z_1}, \tag{11.48}$$

and thus

$$\boldsymbol{\Phi}_{30} = \boldsymbol{\Phi}_{32} \underbrace{\left[\boldsymbol{\Phi}_{20} + (f_2(z_2) - f_1(z_2)) \underbrace{\frac{\eta^{\mathrm{T}}_{\mathrm{PA2D}}(z)\big|_{z_1} \boldsymbol{\Phi}_{10}}{\eta^{\mathrm{T}}_{\mathrm{PA2D}}(z)\big|_{z_1} f_1(z_1)}}_{\alpha} \right]}_{\beta}, \tag{11.49}$$

If switching of PA2D and PD2A is simultaneous, $\widehat{\Delta t} \to 0$ and, consequently, $\widehat{S}$ reduces to the standard saltation matrix formulation given in (11.13).

At this point it is possible to delineate an algorithm to deal with the extrinsic manifolds to be included in the DSH analysis (see Sect. 11.3).

- At each integration time step it is checked if at least one PA2D or PD2A has switched. In the following we consider first a commutation of a PA2D since PD2As switches are a consequence of PA2Ds commutations.
- If there is a switch of a PA2D, the corresponding $h_{\mathrm{PA2D}}(z) = 0$ manifold is known since it is defined by the voltage threshold at which there is a change in the digital coding at the PA2D output. The manifold equation is added as an extra equation to those of SH and the integration time step is added among the unknowns to have a well posed problem. The solution of this enlarged problem gives the "exact" time instant at which the manifold is hit. The term exact is quoted since we use the Newton method to solve this problem and the iterative method stops when the estimated accuracy of the found time step satisfies a given value.
- Vector α of (11.49) is computed. The $\eta^{\mathrm{T}}_{\mathrm{PA2D}}(z)\big|_{z_1}$ normal to the manifold is known together with both the $f_1(z_1)$ vector field and the $\boldsymbol{\Phi}_{10}$ transition matrix at the switching time instant. The vector is attached as a property of the digital network connected to the output of the switching PA2D.
- These α properties are handled and inherited consistently with the elaboration of the digital signals in the digital portion of the circuit. The elaboration depends on the implementation of the digital model of the circuit through, for example, the VERILOG or the VHDL languages. At the end of the digital elaboration (that can involve also delays) there can be a switching of a PD2A due to a change of the digital code at its input. In Fig. 11.5 this is formalised by manifold $h_{\mathrm{PD2A}}(z) = 0$. The specific α property attached to the digital net that is causing the commutation is assigned to the PD2A.
- When a PD2A commutes it can generate a jump in the vector field; product β in (11.49) is computed by exploiting the propagated α property.

This implementation is highly efficient since the memory required to compute the saltation matrices depends only on the number of PA2Ds, being the number of α variables equal to the number of PA2Ds, and not on the complexity of the analog and digital parts of the circuit.

11.5 Numerical Results

To show the effectiveness of the approach discussed in the previous sections, in the sequel we consider two circuits that implement signal processing functions and that can be modeled by DAEs characterised by a switching vector field. We simulate them with DSH in the version implemented in our simulator PAN[1] and discuss the obtained numerical results. Before proceeding, we underline that the emphasis in proposing these circuits is not on the circuits themselves but on the application of the DSH approach.

The first circuit here considered is shown in Fig. 11.6; it implements a simple sample & hold (S&H) that drives an analog to digital converter (ADC). The ADC is directly connected to a digital to analog converter (DAC) that drives a low pass RC filter. We intentionally omitted the digital circuit that eventually does the elaboration of the signal before its conversion by the DAC since it is irrelevant in this context. The circuit is driven by a "large" 1 V at 10 kHz sinusoidal input signal, we are interested in the small signal behaviour of this circuit, namely, the In to Out periodic small signal transfer function. It is assumed that the effects of the small signal perturbation can be considered as additive with respect to the large signal ones. This small signal is applied at the In terminal and it is S&H by commuting S_1 at 100 kHz. This switch is "ideal" but for its on and off resistance. The sampled version of the analog signal is amplified 10 times and applied to the ADC that codes the signal on the digital bus. The ADC is activated when the input signal has been sampled by the S&H. The digital signal is converted back by the DAC and then low pass filtered by R3 and C2.

From the standpoint of the fundamental-matrix numerical computation, this circuit has the peculiarity of being characterised by several kinds of switching manifolds. If we assume an ideal S&H driving signal that is not affected by any jitter, the manifold related to S_1 of S&H depends only on time (switching time instants)

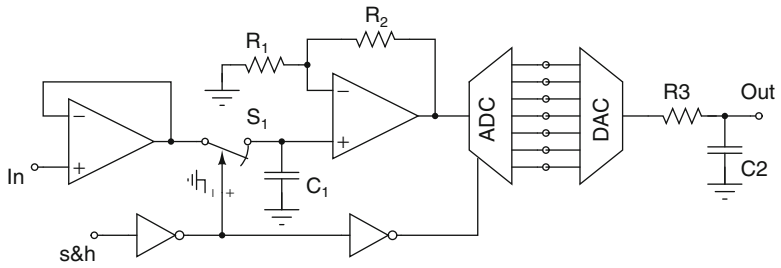

Fig. 11.6 The schematic of the analog to digital converter

[1]Simulator PAN is available at the URL: http://brambilla.ws.dei.polimi.it.

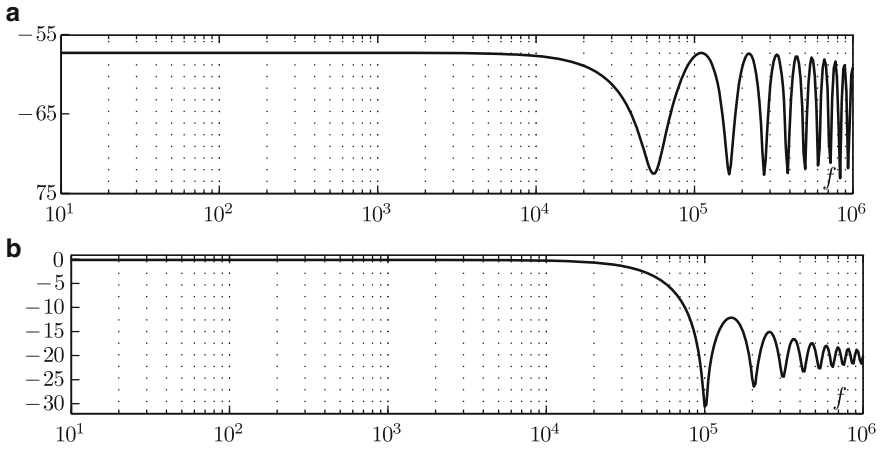

Fig. 11.7 The modulus of the spectra computed by the DSH based PAC analysis related to the analog conversion of one bit of the ADC (across the C_2 capacitor) in Fig. 11.7a and to S&H (across the C_1 capacitor) in Fig. 11.7b. x-axis: frequency of the small signal applied to In; y-axis: magnitude of the components of the spectra in dB

and *not* on the electrical circuit variables. In this case there is no need to insert a saltation matrix. If the S&H driving signal depends on the electrical variables in some way, saltation matrices are needed.

The second kind of manifold is related to the ADC, its digital output depends on the analog input, therefore saltation matrices must be introduced and contribution to the fundamental matrix must be handled in the digital portion of the circuit to allow the "reconstruction" of the small signal transfer function when the digitally elaborated signal is converted back as an analog signal. This is exactly what is done by the DAC; if conventional approaches are used, the incorrect variational model and fundamental matrix lead to the "isolation" of the small signal output at the Out node with respect to the driving small signal at In. Furthermore, the number of bits or levels used in the analog to digital conversion, as shown in the previous sections, determines the number of manifolds and how manifold traversal effects are handled by the digital portion of the circuit.

We have simulated this circuit with DSH; after a steady state solution has been determined we applied the extended version of PAC [11, 20]. In Fig. 11.7 we show the modulus of the spectrum of the small signal voltage across the C2 capacitor (upper panel) and across the C1 one (lower panel). Being the variational model of the circuit time varying the spectra computed by the PAC are composed of the beats among the frequency of the small signal perturbation and the fundamental and harmonics of periodic functions contributing the entries of the $\Phi(1,0)$ sensitivity matrix as shown in (11.38). The result shown in Fig. 11.7 refers to the beat between the DC components of $\Phi(1,0)$ and the frequency of the small signal perturbation.

The frequency of the small signal applied to In has been swept in the [10 Hz, 1 MHz] frequency interval. The S&H shapes the transfer function related to C1 that is largely influenced by the opening and closing of S1 at 100 kHz. The shape

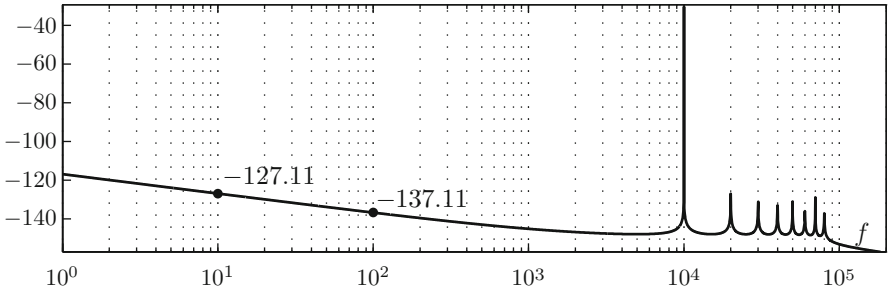

Fig. 11.8 The power spectral density of total noise at the `Out` node. The only considered sources of noise are the `R1` and `R2` resistors

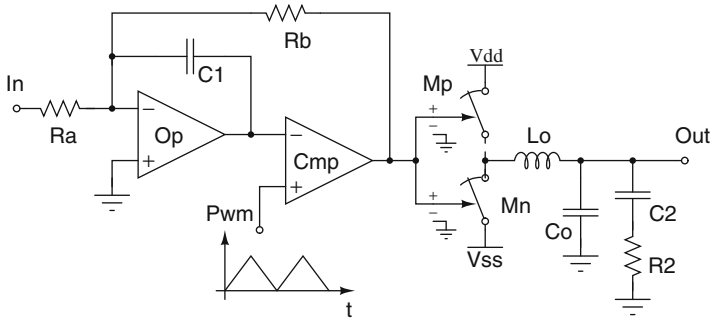

Fig. 11.9 The schematic of the CLASS-D audio amplifier

of the `Out` voltage spectrum is determined by the square pulses at the output of the `DAC`, whose time durations depend on α in (11.49), found in the solution of the variational model when the circuit is driven by the small signal. These pulses can have a very short duration with respect to the working period of the circuit.

A correct determination of the periodic small signal transfer functions is an important aspect in the periodic noise analysis [10, 18–20]. To this end, assume to be interested in how noise generated for example by the `R1` and `R2` resistors affects the signal at pin `Out`. In our analysis, these resistors generate thermal and flicker noise; all the other elements of the circuit are assumed noiseless. We performed a periodic noise analysis based on DSH, the total noise power spectral density obtained at `Out` is shown in Fig. 11.8; we can appreciate the almost constant slope of $-10\,\mathrm{dB/dec}$ due to flicker noise and the up conversion of noise near the fundamental and harmonics of the large signal input.

The second considered circuit is shown in Fig. 11.9; it implements a CLASS-D audio amplifier. The input signal at node `In` is conditioned by the feed-back loop constituted by the `Op` operational amplifier, the `Ra`, `Rb` resistors and the `C1` capacitor. The signal at the output of `Op` is compared by `Cmp` to the sawtooth waveform at the `Pwm` node. The model of the comparator is ideal, i.e. its output instantaneously switches between its upper and lower values. The output of `Cmp` drives the voltage

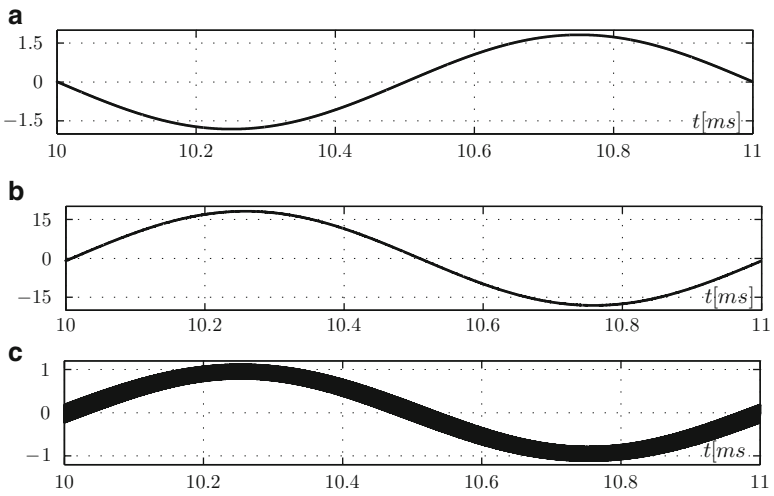

Fig. 11.10 The waveform at the `In` node (Panel 11.10a), at the `Out` node (Panel 11.10b) and at the output of the `Op` operational amplifier (Panel 11.10c)

controlled switches `Mp` and `Mn`. The models of these switches are such that `Mn` closes (its on resistance becomes equal to R_{on}) when the driving signal is larger than a given threshold while `Mp` closes when the driving signal is less than this threshold. The sawtooth waveform at node `Pwm` has a period of 1 μs. The pulsed width modulated large signal (and power) is filtered by the LC filter composed of `Lo` and `Co`. The values of these elements have been chosen considering the impedance of the load (loudspeaker). The value of `Rb` has been chosen equal to 10`Ra` in order to have an input/output gain of the CLASS-D amplifier equal to +20 dB.

The amplifier has been driven at the `In` node by the $\texttt{Vin} = 2\sin(2\pi 10^3 t)$ waveform (large signal). This circuit leads to a DAE model with a discontinuous vector field. In fact, by circuit inspection, we can see that the instantaneous switching of `Cmp` and of the driven `Mp` and `Mn` switches lead to a discontinuous voltage across `Lo` and to a discontinuous current through `C1`. Furthermore, the manifold characterising `Cmp` is voltage dependent, i.e. the time instant at which there is a commutation of `Cmp` depends on the instantaneous value assumed by the voltages at the output of `Op` and at the `Pwn` node.

The steady state working condition has been computed once more with the DSH method. In Fig. 11.10 we report the driving waveform at `In` (upper panel), the output waveform at `Out` (center panel) and that at the output of the `Op` operational amplifier (lower panel). The apparent thick waveform at the output of `Op` is a graphical artifact due to the fact that the feedback signal is taken at the output of the `Cmp` comparator.

As for the previous circuit we assume to be interested in the input/output small signal periodic transfer function of this CLASS-D amplifier when it is driven by a small signal that superimposes to the large signal. We thus performed once more an

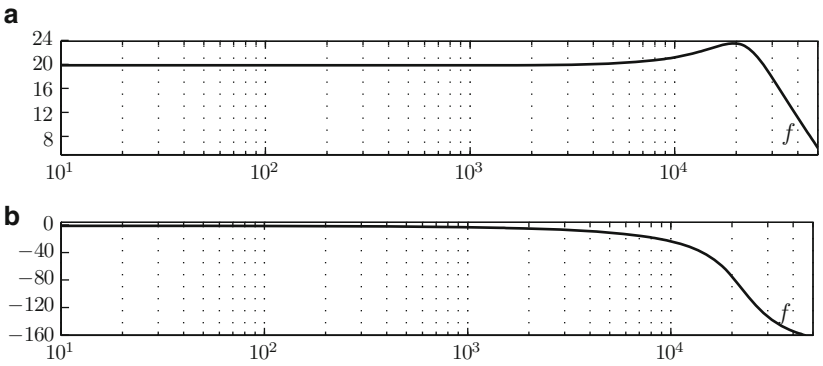

Fig. 11.11 CLASS-D amplifier: the modulus of the input/output transfer function in Fig. 11.11a and its phase in Fig. 11.11b

extended PAC analysis; Fig. 11.11 shows the obtained modulus (upper panel) and phase (lower panel) of the input/output periodic transfer function. As it can be seen from Fig. 11.11 the modulus is "almost flat" till about 10 kHz then it exhibits a peak determined by the resonance of `Lo` and `Co` with the loading resistor (not shown in Fig. 11.11) and finally drops with a slope of $-40\,\mathrm{dB/dec}$ due to the output filter. The values assumed by the phase is coherent with that of the modulus.

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Chapter 12
Variability-Aware Optimization of RF Integrated Inductors in Nanometer-Scale Technologies

Fernando Coito, Helena Fino, and Pedro Pereira

12.1 Introduction

Radio frequency and analog/mixed-signal (RF and AMS) are essential and critical technologies for the rapidly growing wireless communications market [1]. The progressive scaling of CMOS technology towards nanometer sizes has made the implementation of highly integrated systems for the wireless communication systems possible. However it is widely recognised that as technology continues to scale down, the variability in process parameters may cause significant deviations in the device behaviour [2–5]. Various techniques such as silicon strain and high-K gate dielectric, among others, have been proposed as a way of maintaining the transistors performance in spite of the ever-diminishing device sizes [6]. These techniques, however, envisage the minimization of the active devices parameter's variations. Further manufacturing variations should also be accounted for such as the dynamic variations and the interconnect variations. Dynamic variations are caused by fluctuations in the operation of the system, such as in the temperature caused by the existence of highly active blocks within the die. Finally interconnect variations relate fluctuations in metal width and spacing between conductor and the thickness of interlayer dielectrics [7, 8].

Among the RF realm, spiral inductor design and synthesis is still a major concern for analogue designers, since it involves the characterization of complex loss mechanisms in the metal and the substrate, and an ever demand for area reduction is needed [9]. The complexity of the design as well as the necessity for having an environment offering the possibility for exploring design trade-offs has led to the development of multi-objective optimization based design methodologies yielding the generation of Pareto-optimal surfaces [9, 10].

F. Coito (✉) • H. Fino • P. Pereira
DEE, Faculdade de Ciências e Tecnologia, UNL, Portugal
e-mail: fjvc@fct.unl.pt

E. Tlelo-Cuautle (ed.), *Integrated Circuits for Analog Signal Processing*,
DOI 10.1007/978-1-4614-1383-7_12,

For the efficient generation of the Pareto surfaces, lumped scalable models have been largely employed for the characterization of integrated inductors [8–11]. The accuracy of the results obtained is strongly determined by the availability of accurate closed-form expressions for all the lumped elements. Although physics-based analytical expressions have been proposed for the evaluation of the lumped elements, the variability of the process parameters is usually ignored due to the difficulty to formalize it into an optimization performance index. In this way, we may be selecting ideally optimal solutions in detriment of quasi-optimal solutions that may prove to be better, should their sensitivity to process parameter variation be accounted for. To overcome this misleading, both solutions on the Pareto-optimum surface as well as quasi-optimum solutions should be considered. Finally information on the sensitivity to process parameter variations must be used for electing the best design solutions.

In this chapter we propose a methodology for exploring the design space of integrated inductors based on the use of a Pareto extended surface. The evaluation of this extended set of sub-optimum solutions requires methods that are able to find, on the parameter space, the set of local optima, since solutions that are close to each other in the performance index space may be very distant in the design parameter space.

Particle swarm optimization (PSO) is an effective method to perform global optimization and it has been successfully used [12] in the evaluation of the Pareto surface for the design of spiral inductors. In order to extend the use of PSO into finding the set of suboptimum solutions it is necessary to consider niching methods [13, 14]. Using PSO niching algorithms may become significantly more complex than the standard algorithm and a number of additional problem dependent parameters must be accounted for. As a way to avoid the additional complexity, we use the approach based in ring topology PSO proposed by [15].

In Sect. 2 this chapter presents a brief description of the adopted inductor model and then the influence the variability of each technological parameter on the inductor performance is justified. In Sect. 3 the PSO algorithm developed or the generation of the Pareto surface is introduced. Section 4 is dedicated to the optimization of the inductor and the evaluation on the robustness of the design solutions, against parameter variability. Finally, Sect. 5 offers the conclusions.

12.2 Sources of Variability in the Performance of Integrated Inductors

As already pointed out the interconnect variations account for the fluctuations in the metal width, in the spacing between conductors and in the thickness of interlayer dielectrics. The influence of the fluctuations on the above mentioned parameter values, in both the inductor quality factor, Q, and inductance value, L, will be investigated. For a simple characterization of the inductor behavior the Pi-model, illustrated in Fig. 12.1, will be considered.

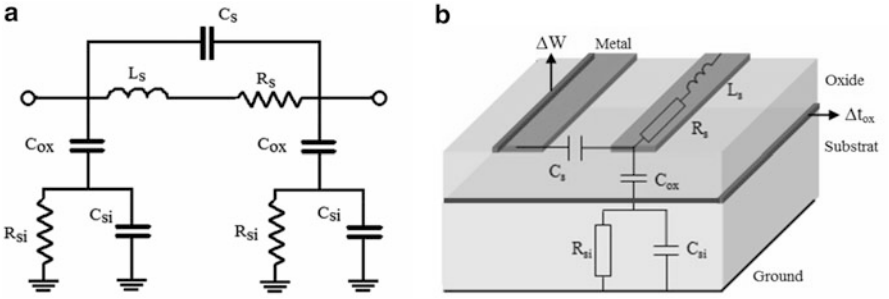

Fig. 12.1 Integrated spiral inductor: (**a**) Planar inductor pi-model, (**b**) Single metal layer inductor metal width variation Δw

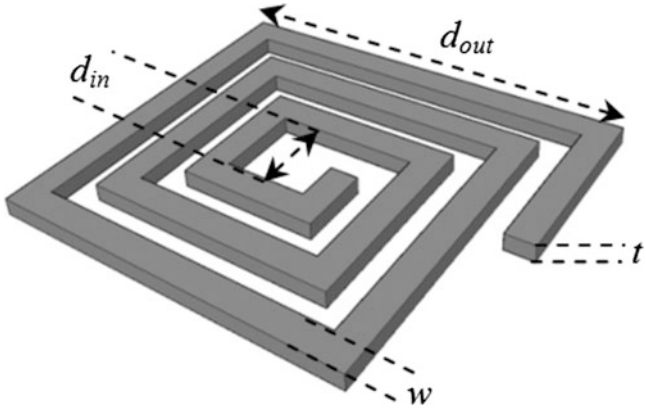

Fig. 12.2 Square inductor geometric parameters

For this model physics-based analytical expressions have been proposed for the evaluation of the lumped elements. For the evaluation of the inductance, L_s, the Modified Wheeler formula is used [11], where

$$L_s = \frac{k_1 \mu_0 n^2 d_{\text{avg}}}{(1 + k_2 \rho)}, \tag{12.1}$$

given that

$$\begin{aligned} \rho &= \frac{(d_{\text{out}} - d_{\text{in}})}{(d_{\text{out}} - d_{\text{in}})}, \\ d_{\text{avg}} &= 0.5(d_{\text{out}} + d_{\text{in}}), \\ d_{\text{out}} &= d_{\text{in}} + 2nw + 2(n-1)s. \end{aligned} \tag{12.2}$$

Where, n is the number of turns, s is the track-to-track distance, and w is the track width, as represented in Fig. 12.2. Finally, k_1 and k_2, are coefficients allowing the model to be adapted to several inductor shapes [11].

The evaluation of the spiral resistance, R_s, is obtained by

$$R_s = \sqrt{R_{\text{dc}}^2 + R_{\text{ac}}^2}. \tag{12.3}$$

Where,

$$R_{\text{dc}} = \frac{l}{(\sigma w t)}, \tag{12.4}$$

$$R_{\text{ac}} = \frac{kR_{\text{hf}} = kl}{(2\sigma\delta(w+t))}. \tag{12.5}$$

And k is a correction factor and takes the value 1.2, σ and t are the metal conductivity and thickness, respectively. The metal length, l, is obtained with [16]

$$l = N_{\text{side}}\, d_{\text{avg}}\, n \tan\left(\frac{\pi}{N_{\text{side}}}\right). \tag{12.6}$$

And the skin depth, δ, can be determined by [17]

$$\delta = \frac{1}{\sqrt{\sigma\mu\pi f}} \tag{12.7}$$

For the evaluation of the capacitance, C_s, all overlap capacitances are considered and given by [18]

$$C_s = \frac{n_c\, w^2\, \varepsilon_{\text{ox}}}{t_{\text{ox}M1-M2}}. \tag{12.8}$$

Where ε_{ox} is the oxide permittivity, n_c is the number of overlaps and $t_{\text{ox}M1-M2}$ is the oxide thickness between the spiral upper and lower metal. The parasitic capacitance, C_{ox}, between the spiral metal and the silicon substrate, is estimated with [18]

$$C_{\text{ox}} = \frac{0.5\, l\, w\, \varepsilon_{\text{ox}}}{t_{\text{ox}}}. \tag{12.9}$$

Where t_{ox} is the thickness of the SiO_2 between the inductor and the substrate and lw defines the area of the spiral. Finally the Substrate resistance, R_{si}, and capacitance C_{si}, are obtained with [18]

$$R_{\text{si}} = \frac{2\, h_{\text{si}}}{(l\, w\, \sigma_{\text{si}})}. \tag{12.10}$$

$$C_{\text{si}} = \frac{0.5\, l\, w\, \varepsilon_o\, \varepsilon_r}{h_{\text{si}}}. \tag{12.11}$$

The expression of the quality factor becomes [19]

$$Q = \left(\frac{w L_s}{R_s}\right)\left(\frac{R_p}{R_p + \left[\left(\frac{w L_s}{R_s}\right)^2 + 1\right] R_s}\right)\left(1 - \frac{C_p R_s^2}{L_s} - \omega^2 L_s C_p\right). \tag{12.12}$$

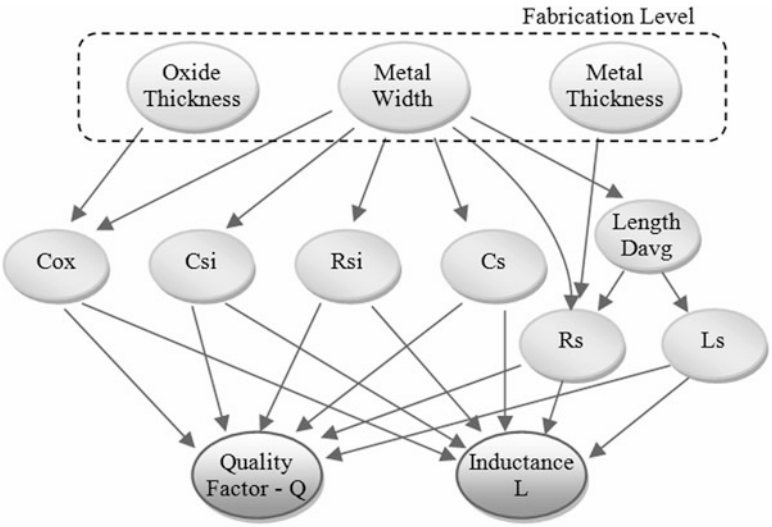

Fig. 12.3 Process variables impact on inductor quality factor and inductance

Where

$$R_p = \left(\frac{1}{\omega^2 C_{\text{ox}}^2 R_{\text{si}}}\right) + \frac{R_{\text{si}}(C_{\text{ox}} + C_{\text{si}})^2}{C_{\text{ox}}^2}. \tag{12.13}$$

$$C_p = C_{\text{ox}} \frac{1 + \omega^2 (C_{\text{ox}} + C_{\text{si}}) C_{\text{si}} R_{\text{si}}^2}{1 + \omega^2 (C_{\text{ox}} + C_{\text{si}})^2 R_{\text{si}}^2}. \tag{12.14}$$

From the above expressions the influence of the interconnect variations in the inductor behavior may be inferred. In Fig. 12.3, a graphical representation of the dependency of the inductors performance functions, i.e., L and Q, on fluctuations of technological parameters values is illustrated.

As we may conclude the variability of the oxide thickness, t_{ox}, will cause fluctuations on C_{ox}. Metal thickness, t, will be reflected in R_s only. Finally, the metal width, w, will influence all the elements of the Pi-model. For a quantitative evaluation of the influence of each technological parameter on the inductor behavior, sensitivity analysis must be performed. Yet, for the sake of simplicity, only the influence of metal width will be considered in this chapter.

12.3 Multi-Objective Particle Swarm Optimization

The general multi-objective optimization problem is posed as follows [20]:

$$\underset{\mathbf{x}}{\text{Minimize}}\ \mathbf{F}(\mathbf{x}) = [f_1(\mathbf{x}), f_2(\mathbf{x}), \cdots, f_n(\mathbf{x})]^T. \tag{12.15}$$

Subject to $g_j \leq 0 (j = 1, 2, \ldots, m)$, and $h_i = 0 (i = 1, 2, \ldots, q)$.

Where n is the number of objective functions, m is the number of inequality constraints, and q is the number of equality constraints. $\mathrm{x} = (x^1,\ x^2,\ \ldots,\ x^D)$ is a vector of D real valued independent design parameters (also called decision variables). F(x)is a vector of real valued performance indexes. The feasible design space is the set $\mathrm{X} = \{\mathrm{x} : g_j \leq 0,\ j = 1,2,\ \ldots,\ \mathrm{m};\ \text{and}\ h_i = 0, i = 1,2,\ldots,q\}$.

As opposed to what happens in single-objective optimization, in general there is no single solution to a multi-objective optimization problem. Usually, the optimization result is a set of points on the design space all of them fitting a certain definition of optimum known as *Pareto optimality*. Let us start by defining the concept of dominance between two vectors.

$$\mathbf{x}_1 \text{ weakly dominates } \mathbf{x}_2 : \mathbf{x}_1 \preceq \mathbf{x}_2 \ \text{ iff } \ \forall_i : f_i(\mathbf{x}_1) \leq f_i(\mathbf{x}_2). \tag{12.16}$$

$$\mathbf{x}_1 \text{ dominates } \mathbf{x}_2 : \ \mathbf{x}_1 \prec \mathbf{x}_2 \ \text{ iff } \ \forall_i : f_i(\mathbf{x}_1) \leq f_i(\mathbf{x}_2) \ \text{ and } \ \exists_i : f_i(\mathbf{x}_1) < f_i(\mathbf{x}_2) \tag{12.17}$$

This leads to the concept of *Pareto Optimal* solution: A point x^* is Pareto optimal if there is no $\mathrm{x} \in \mathrm{X}$ for which

$$\mathbf{x} \prec \mathbf{x}^* \tag{12.18}$$

The *Pareto optimal set* (P) is the set of all non-dominated solutions, and the *Pareto front* is: $\mathrm{PF} = \{\mathrm{u} = \mathrm{F}(\mathrm{x}) :\ \mathrm{x} \in \mathrm{P}\}$.

The Pareto front corresponds to the best possible trade-off between the n performance indexes. It is not possible to improve one of the performance indexes $f_i(\mathrm{x})$ without degrading some other. Therefore the goal for a global multi-objective optimization algorithm is to determine the Pareto set and the Pareto front associated to the problem under analysis.

Evolutionary strategies aim to improve on the performance of random searches for points of optimality. This is accomplished by the identification of regions containing good designs and assuming that searches in the region of good designs may uncover further improved designs. Different strategies are used to identify and explore regions with a high probability of improved candidate solutions. These strategies distinguish between different evolutionary computation algorithms.

Particle Swarm Optimization (PSO) is an efficient optimization method for constrained or unconstrained single objective optimization. More recently it has gained an increasing interest as a means of solving multi-objective optimization problems [12–14, 21, 22].

PSO is inspired by studies on the social behavior of insects and animals [23, 24]. A population of particles is made to evolve within the parameter search space. Each particle position x corresponds to a candidate solution for the optimization problem. As the population evolves the particles are guided towards the most promising region within the parameter search space.

12.3.1 The Canonical PSO Algorithm

In this section the canonical PSO algorithm is addressed. Therefore we will focus on the case where a single performance index is considered (F(x) is scalar).

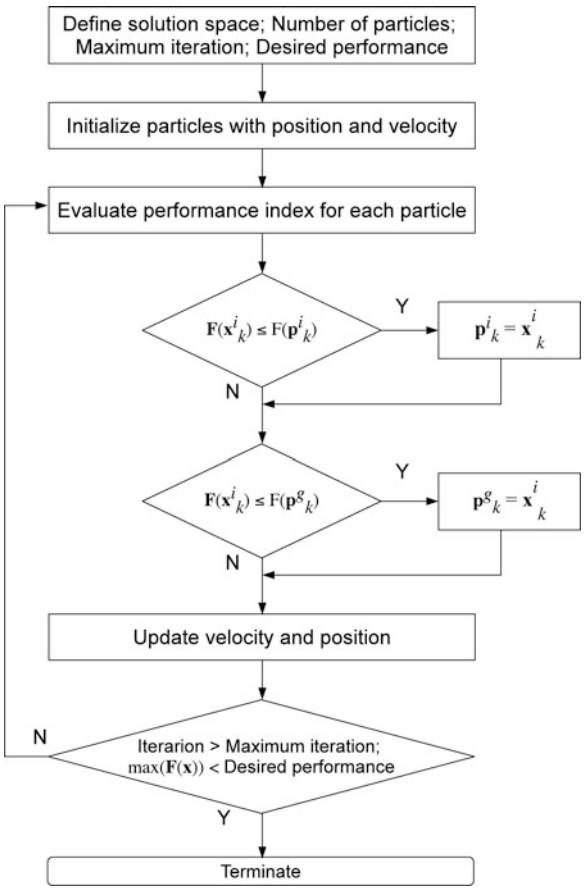

Fig. 12.4 PSO flowchart

Its velocity determines a particle progress within the search space. At each moment this velocity depends on the particle's current position, on the best position it has found so far, and on the best position found by all the other particles on the swarm [25], as given by

$$\mathbf{v}_{k+1}^{i} = \alpha \mathbf{v}_{k}^{i} + c_1 \, \text{rand}_1 \left(\mathbf{p}_{k}^{i} - \mathbf{x}_{k}^{i} \right) + c_2 \, \text{rand} (\mathbf{p}_{k}^{g} - \mathbf{x}_{k}^{i}). \tag{12.19}$$

$$\mathbf{x}_{k+1}^{i} = \mathbf{x}_{k}^{i} + \mathbf{v}_{k+1}^{i}. \tag{12.20}$$

Where $\mathbf{v}_k^i$ is the ith particle velocity vector at iteration k, $\mathbf{p}_k^i$ is the best position the particle has found up to that iteration and $\mathbf{p}_k^g$ is the best position found by the swarm (*global best*); rand_1 and rand_2 are D-dimensional column vectors whose elements are independent random numbers, uniformly distributed in the range [0,1]; α, c_1 and c_2 are coefficients (>0).

The basic flowchart for the canonical PSO algorithm is presented in Fig. 12.4. Each particle is initialized with a random position and velocity. At every iteration each particle position is assessed through the performance index. The particle keeps

track of the best position it has found so far ($\mathbf{p}_k^i$). The swarm keeps track of the best position ever found by any particle ($\mathbf{p}_k^g$). As the algorithm evolves the particles are attracted towards a single global solution.

12.3.2 PSO and Discrete Search Space

Like most nonlinear optimization methods, the canonical PSO algorithm assumes that the parameters defining the search space are continuous variables. However, technical constraints may restrict the values that can be used for the design parameters, confining them to discrete valued sets, therefore leading to a discrete search space.

The set of technical constraints used on the design of the Spiral Inductor is presented in Table 12.1. While the values for w and d_{in} are only incremented with steps of 0.25 µm, the number of spires of the inductor may only be increased by integer values. As for the inductor shape only three types are considered (square, hexagonal and octagonal).

Expressions (12.19) and (12.20) do not account for this discrete nature of the design parameters. The problem is illustrated in Fig. 12.5 for a one-dimensional search space. Minimizing the function on the continuous space yields $\hat{x}$ as the optimum. It's nearest discretized value is $\hat{x}_d$. However, the optimal feasible value corresponds to x_d^*.

To insure that the solution yielded by the algorithm is in fact optimal, it is necessary to force the particles to move only over this discrete search set. Therefore instead of (12.20) the new particle position is computed according to

$$\mathbf{x}_{k+1}^i = \text{round}\left(\mathbf{x}_k^i + \mathbf{v}_{k+1}^i\right). \tag{12.21}$$

Table 12.1 Spiral inductor design constraints

Parameter	Min	Step	Max
w(µm)	5.0	0.25	1.0
d_{in}(µm)	20.0	0.25	2.0
N	1.5	1.0	15.5
N_{side}	Square (4)/	Hexagonal (6)	/ Octagonal (8)

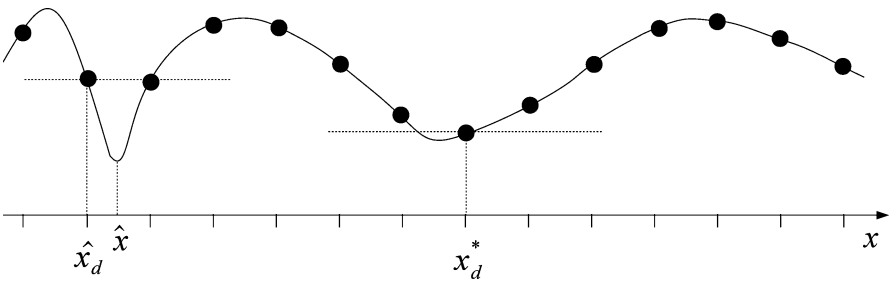

Fig. 12.5 Effect of discretizing a continuous search space

Where round(x) replaces the value x by the nearest discretized value. It is relevant to notice that the particle's performance must be evaluated only after its discretized position is computed. This guarantees that the optimal solution found by the PSO algorithm truly corresponds to a feasible solution.

12.3.3 Handling Multiple Objectives with PSO

The simplicity from the canonical PSO algorithm makes it a candidate method for multi-objective optimization. However, the algorithm is not truly fit for the task. Its focus is the determination of a single optimal solution, while there is no absolute global optimum in a multi-objective performance index. Usually it is not possible to define a single best position either for a particle ($\mathbf{p}_k^i$) or for the entire swarm ($\mathbf{p}_k^g$). Due to its point-centered features the algorithm is unable to locate the Pareto front.

Therefore, it is necessary to modify the basic algorithm. Examples of such modifications may be found in [13, 14, 21, 22, 26–28]. In the modified versions the search for a global best is replaced by the search for a set of non-dominated solutions, defining the Pareto front. The speed of each particle is updated using one of the non-dominated positions instead of the global best $\mathbf{p}_k^g$. Different algorithms take different approaches on how to select each non-dominated position. Algorithms also differ on how particle positions integrating the non-dominated set, are determined at each iteration.

12.3.3.1 The Dual-Objective PSO Algorithm for Inductor Design

The optimization scheme has two simultaneous objectives

- To maximize the inductors quality factor(Q).
- To minimize the designed inductance deviation $\left(\frac{|L_s - L_{\text{specified}}|}{L_{\text{specified}}}\right)$.

These objectives may not be simultaneously fulfilled as improving the inductors precision generally leads to a decrease on the quality factor. Therefore the goal is to find the points in the search space that reflect the optimum trade-off between the two goals.

The two objective functions define a two-dimensional value space. The Pareto front is a line in this space, corresponding to the boundary of the region where the feasible performance values lie. To minimize the inductance deviation while maximizing the quality factor, this boundary is located at the top left side of the feasible region (Fig. 12.6).

This figure sketches a simple method to determine the points from the Pareto front proposed by [13]. The method starts by fixing the value for one of the performance values, and then optimizing the other performance index with this additional constrain. The result of this optimization yields a point on the Pareto.

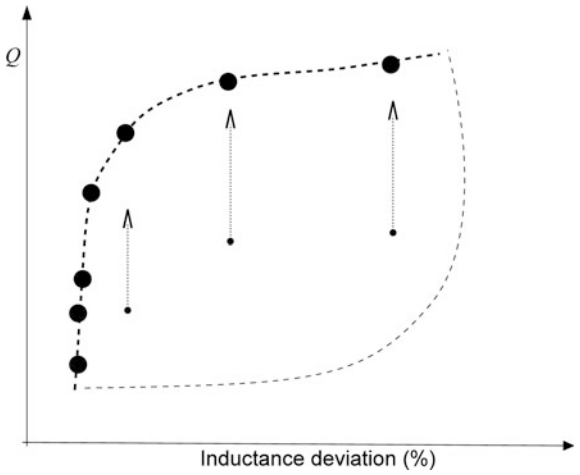

Fig. 12.6 Example of a two-dimensional performance value space

In Fig. 12.6 the inductance deviation values are fixed, and the optimization is performed over the quality factor.

When the parameter values are chosen from a discrete set, the Pareto front is not a continuous boundary. In the discrete case, the Pareto front is composed by a set of isolated points (marked as "O"), as represented in Fig. 12.6. As the optimization problem cannot be solved with an equality goal on one of the performance index, an inequality constrain ($\leq$) is used.

12.3.4 Design Results

A group of particle swarms is used to determine the set of parameter combinations that yields the best compromise between precision and quality factor. One of the swarms aims to minimize the inductance deviation, with no constrain on Q. The other swarms aim to maximize Q, constrained by a maximum deviation allowed ($dev_{\max}$). Three swarms are used with different values for $dev_{\max}$: 1%, 5% and 7%.

The four swarms run simultaneously, allowing crossing information among them. When a particle from one of the swarms reaches a position, the performance indexes for all the swarms are evaluated. If one of these indexes is better than it's corresponding global best, that global best position is updated.

Each swarm is composed of 25 particles and runs for 6 iterations. The algorithm parameters are $\alpha = 0.98$, $c_1 = 0.2$ and $c_2 = 0.1$. The algorithm is run twice and the Pareto front results are merged.

The best design results obtained by this procedure are illustrated in Fig. 12.7 and given in Table 12.2. Although the maximum deviation allowed for the inductance

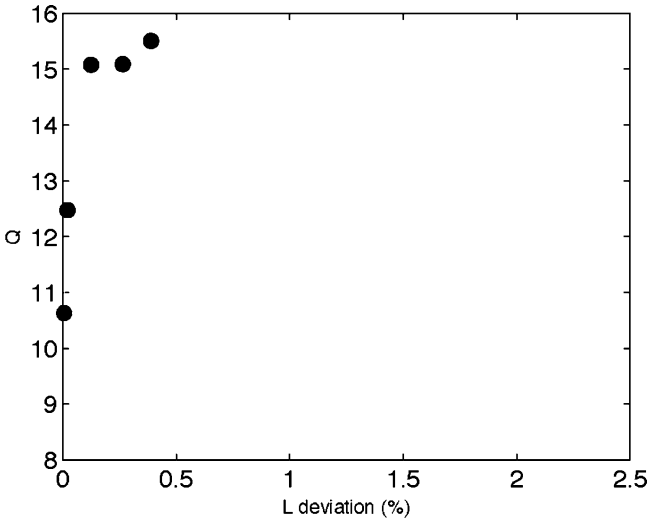

Fig. 12.7 Best design results obtained by the group of four swarms

Table 12.2 Best design results obtained by the group of 4 swarms

Q	Inductor Deviation (%)	w (μm)	d_{in} (μm)	n	N_{side}
15.51	0.39	11	55.25	5.5	4
15.09	0.27	10.75	55.5	5.5	4
15.08	0.13	10.75	55.75	5.5	4
12.48	0.02	9	60	5.5	4
10.63	0.6	6.75	78.75	5.5	8

design is 7%, the highest quality factor corresponds to an inductance deviation of only 0.4%. Higher values for Q are achieved only for a deviation larger than the 7% limit.

12.3.5 Features of the Canonical PSO Based Algorithm

Table 12.2 shows that the top four results correspond to different combinatins of the same inductor structure, i.e., a square inductor with 5.5 turns. This is caused by the fast convergence of the PSO canonical algorithm towards p^g. It also leads the algorithm to miss some Pareto front optimal solutions that associated to different inductor structures. Table 12.3 presents two solutions which are not captured by the algorithm.

This limitation is caused by an intrinsic property of the canonical PSO algorithm. When a particle position reaches the global best ($\mathrm{X}_k^i = \mathbf{p}_k^i = k$) the velocity update depends only on the inertia term $\alpha \mathbf{v}_k^i$. Therefore, when a particle approaches the

Table 12.3 Pareto front points missed by the PSO canonical algorithm

Q	Inductor Deviation (%)	w (μm)	d_{in}(μm)	n	N_{side}
13.80	0.017	9	46.75	6.5	8
12.40	0.5	8.75	76.75	5.5	6

global best solution its velocity approaches zero, and the particle will, eventually, stop moving. As a result, the particle will converge to the best position found so far, without granting that the true global optimum has been reached. In fact it may not even correspond to a local optimum.

We may therefore conclude that the canonical PSO based algorithm is able to find a set of good design solutions that allow establishing a compromise between the inductor's precision and quality factor. However it does not find all the solutions that lie in the Pareto front.

Furthermore, the performance indexes used for optimization may not fully represent all the features aimed by a designer. This stems from both the difficulty in formalizing some of the features as a performance index, and the computational burden that the analysis of some features may add to the algorithm.

In these conditions, to obtain relevant design information requires the optimization algorithm to be able to provide not only optimal trade-off solutions, but also solutions the lie in the vicinity of the Pareto front (quasi-optimal solutions). Next section presents an example of such an algorithm.

12.4 Niching PSO Using Ring Topology

12.4.1 The Niching PSO Algorithm

When multiple satisfactory solutions exist and it is difficult to define a performance index to do the selection, it is important to develop a method able to pick the set of satisfactory solutions, and not only finding global optimal ones. In this section satisfactory solutions are considered to be a sub-set of the optimization problem local optima. For sake of simplicity the method proposed uses a local best PSO algorithm based on a ring topology population map [15].

Let the swarm of particles be mapped on to a ring topology as presented in Fig. 12.8. Each particle's search movement is driven by it's own ($\mathbf{p}_k^i$) position, and by a group best position ($\mathrm{p}_k^{g,i}$), which takes the place of the global best used in expression (12.19).

The evaluation of each particle group best ($\mathrm{p}_k^{g,i}$) takes into account the personal best positions from its direct neighbours. For example, the personal best of particle 3 ($\mathrm{p}_k^{g,3}$) is determined from the set $\{\mathrm{p}_k^2, \mathrm{p}_k^3, \mathrm{p}_k^4\}$.

The fact that each particle interacts only with its two neighbours slows down the communication within the swarm. As shown in [15, 24] this leads the particles to associate in clusters around the local optima, instead of converging to a single point.

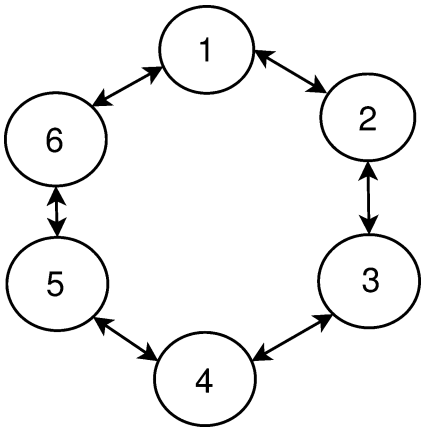

Fig. 12.8 PSO swarm ring topology with six particles

Slow communication is a desirable feature on algorithms that aim to locate multiple optima as it allows the particles to thoroughly search in its local neighbourhood. When the algorithm stops the set of group best positions $\{p_k^{g,i}: 1 = 1, \ldots, n\}$ corresponds to the set of local optimal solutions.

12.4.2 Design Results

To deal with the dual-objective problem two different swarms are used. One of them aims to minimize the inductance deviation. The goal of the second swarm is to maximize the quality factor, constrained to a 5% maximum inductance deviation. Each swarm is composed of two particles and runs for four iterations. The algorithm parameters are $\alpha = 0.75$ and $c_1 = c_2 = 0.3$.

The local optima found by the two swarms are merged in Fig. 12.9. Table 12.4 presents the extended-Pareto front containing the non-dominated set of solutions (shaded rows) as well as a set of quasi-optimal solutions. Only solutions corresponding to a precision under 2.5% are presented. Only five of the displayed solutions are non-dominated solutions (marked as O in the figure). For all the other solutions it is possible to increase the quality factor without losing precision (or vice-versa). From a Pareto-optimal approach these five solutions correspond to the set from which the designer ought to select.

12.4.3 Analysis of the Robustness to Parameter Variation

In this section the effect of parameter uncertainty is integrated on the optimization results analysis. It is assumed that the implemented values for the track width (w)

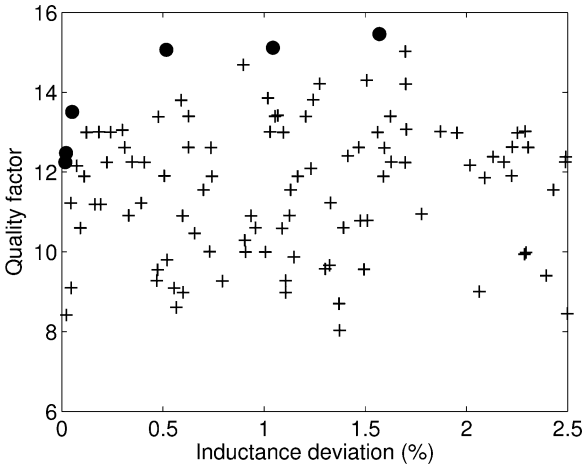

Fig. 12.9 Local optima obtained by the niching PSO algorithm

Table 12.4 Extended-pareto front

Q	Inductor deviation (%)	w (µm)	d_{in} (µm)	n	N_{side}
15.49	0.78	11.00	55.5	5.5	4
15.08	0.13	10.75	55.75	5.5	4
14.66	0.12	10.5	56.25	5.5	4
14.23	0.43	9.25	46.25	6.5	8
13.81	0.46	9.25	75.00	5.5	8
13.80	0.02	9.00	46.75	6.5	8
13.40	0.20	9.25	47.00	6.5	6
13.39	0.06	8.75	47.5	6.5	8
12.99	0.12	8.5	48.25	6.5	8
12.72	0.16	9.00	76.25	5.5	6
12.62	0.20	8.25	48.75	6.5	8
12.40	0.005	8.75	76.75	5.5	6
12.25	0.02	8.5	49.00	6.5	6
11.83	0.20	7.75	77.75	5.5	8
11.70	0.27	8.75	97.00	4.5	4
11.24	0.22	8.00	62.00	5.5	4
11.23	0.05	7.75	51.00	6.5	6
10.18	0.16	6.5	32.5	7.5	8
9.54	0.03	6.00	34.25	7.5	8
9.28	0.05	6.25	34.25	7.5	6

and the internal diameter (d_{in}) may differ from the design values. The maximum tolerance for each of these parameters is taken to be equal to half the value of the design parameter step from Table 12.1.

The values for Q and Inductance precision are re-evaluated taking into account the above-mentioned tolerances, for each local optima presented in Fig. 12.9. It is assumed that, in the vicinity of each local optimum, both Q and the inductance precision show a monotonic behaviour. Therefore, using a worst-case approach, the

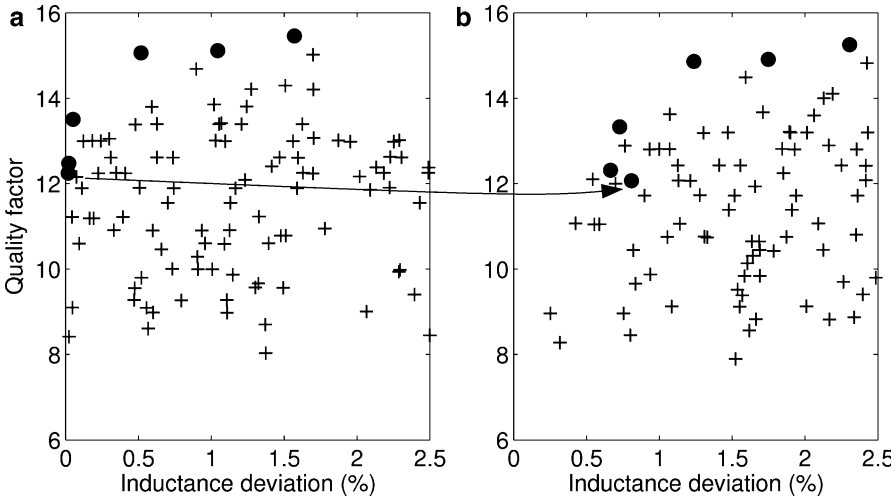

Fig. 12.10 (**a**) Local optima. (**b**) Worst-case robustness results for the local optima

largest deviation from the nominal performance will be found on the boundary of the region defined by $\{x: x \in p^{g,i} \pm [0.125, 0.125, 0, 0]\}$, where $p^{g,i}$ is a local optimum.

For each of the local optima, Q and inductance deviation are computed at the corners of the region. The worst performance values are used to characterize the inductor. The results from this procedure are presented in Fig. 12.10b. Not surprisingly, the worst-case inductance deviation values are larger than in the error free case. More relevant, however, is the fact that not all the solutions, which are non-dominated in the error free, case (Fig. 12.10a) also stay non-dominated in Fig. 12.10b. Therefore, an optimal design choice may lead to a less than optimal implementation.

Results from Fig. 12.11 show that, after implementation, some of the error free quasi-optimal solutions may correspond to a better trade-off than other taken from the nominal optima. Therefore, the set of solutions presented to the designer should be composed not only by the non-dominated optimal set, butinclude the quasi-optimal solutions as well.

It is, of course, possible to integrate the proposed procedure in the optimization algorithm. However the procedure will heavily increase the overall computational burden. Hence it is preferable to use it to post-process only the optimization solutions.

12.5 Conclusions

In this chapter a multi-objective optimization based methodology for the design of integrated inductors is described. The necessity for obtaining design solutions robust against the technological parameters variability has led to a new methodology

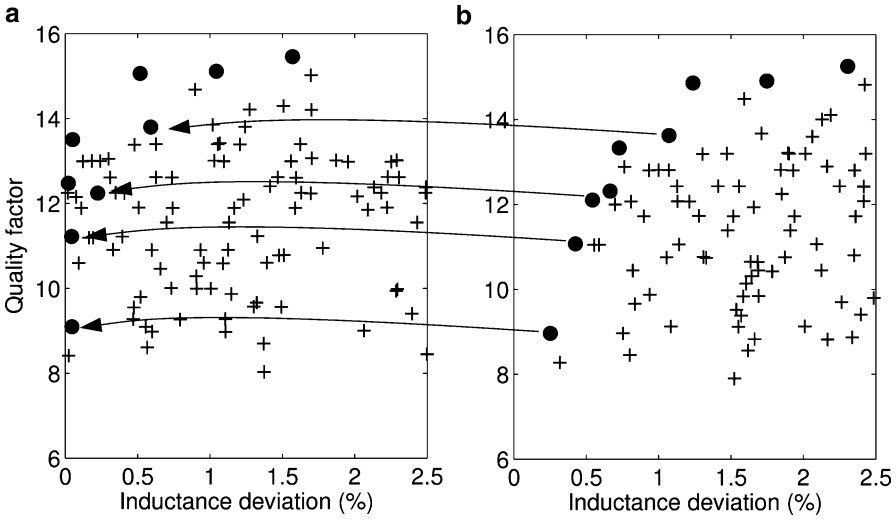

Fig. 12.11 Location on the local optima plane (**a**) of the worst-case non-dominated solutions (**b**)

where an extended-Pareto surface is generated. This extended-Pareto front contains both optima solutions and quasi-optimum solutions. Finally information on the robustness against process parameter variations is used for electing the best design solutions.

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Chapter 13
A Survey on the Static and Dynamic Translinear Paradigm

Rafael Vargas-Bernal and Carlos A. De La Cruz Blas

13.1 Introduction

Nowadays, electronic designers are facing up the analog design using low-supply-voltages and low power consumption to fulfill the requirements of technology and portable applications. The VLSI technology is leaded by the CMOS processes due to the suitability for digital design and their lower cost than other fabrication processes involving BJT transistors. In this scenario, the new trends are to reduce the transistor length to increase the integration density and speed. Moreover, these characteristics allow implementing more sophisticated systems in less chip area to be exploited, for instance, in portable equipment. The size of silicon devices has decreased at a fairly steady rate by factor of about 100, since the invention of the integrated circuit (IC). Such reduction is making that the fabrication processes are moving to constant-field scaling instead of constant–voltage scaling, to reduce power consumption and to obtain an adequate performance of the integrated devices. The goal is mainly to avoid the breakdown of the thin gate-oxide insulator of the submicron process. However, this approach also requires diminishing the supply voltage by the same scaling factor. Besides, the threshold voltage is not reduced by the same ratio that scaling factor to avoid high leakage currents in the digital implementations. Therefore, analog designers are investigating novel techniques or revisiting the known procedures to design high performance mixed signal designs according to these new trends, i.e., very low voltage operation.

R. Vargas-Bernal (✉)
Departamento de Ingeniería en Materiales, Instituto Tecnológico Superior de Irapuato, Carretera Irapuato-Silao Km. 12.5, Irapuato, Guanajuato, C.P. 36821, Mexico
e-mail: ravargas@itesi.edu.mx

C.A. De La Cruz Blas
Departamento de Ingeniería Eléctrica y Electrónica, Universidad Pública de Navarra, Campus Arrosadía, Pamplona, Navarra, España, C.P. 31006, Spain
e-mail: carlos.aristoteles@unavarra.es

E. Tlelo-Cuautle (ed.), *Integrated Circuits for Analog Signal Processing*,
DOI 10.1007/978-1-4614-1383-7_13,

Within these strategies, the main issues are operation of the MOS transistors with the minimum voltage available, rail-to-rail input and output voltages and that the internal voltage swings have to be as small as possible with maximum dynamic ranges and bandwidths. Obviously, a trade-off among these parameters exists, thus the optimal implementation will depend on the specifications of the design. For instance, current-mode processing exploits the signal-handling capability of currents, whereas voltages are nonlinearly related to circuit currents according to their inherent compression law, for MOS and bipolar junction transistors (BJTs). In this way, the signal dynamic range becomes less influenced by a reduction in supply voltage. Translinear (TL) loops fall into this category, and it is based on large-signal behavior, exploiting a wide set of regions of operation of MOS transistors, thus, making it an interesting alternative for nonlinear and linear current-mode signal processing in the current scenario of IC analog design.

TL loops are formed by a special transistor topology, where the devices can operate in different regions of operation providing different linear–nonlinear processing; besides with the addition of capacitors, it is possible to form dynamic systems which can operate linearly or nonlinearly. Thus, when BJT transistors or CMOS in weak inversion are used the circuits are known as log-domain circuits; when CMOS are operating in the quasi-quadratic law, they are called square-root domain circuits. The main contribution of translinear circuits is the fast and efficient realization of many analog nonlinear signal processing functions with small quantities of MOS transistors [1, 5, 7, 14–18, 21–23, 25–30, 32, 33, 35–40], BJTs [2, 4, 8, 12–14, 20, 24, 31, 32, 34, 35], BJT/HBTs [10], floating-gate MOS transistors [3, 6, 11, 19] or ISFETs [9, 52, 53, 66, 80]. Also, TL circuits have several advantages: high frequency operation, tuneability, low supply voltage, lower-power consumption, low noise, low third order intermodulation distortion, low total harmonic distortion, the immunity to body effects, extended dynamic range, compactness, design modularity, and low circuit complexity.

The content of this chapter is as follows: Section 13.1 describes the interest in reviewing the state-of-art of this paradigm used for designing analog signal processing applications based on low-voltage and low-power. The static translinear principle is analyzed in Sect. 13.2, where translinear circuits based on BJTs, MOS transistors, and FMOS transistors can be used under different operation regions (strong inversion, triode, weak inversion). In Sect. 13.3, the dynamic translinear paradigm is firstly described in a generic way, then particularized to log-domain applications and square-root domain circuits. In addition, the dynamic nonlinear building blocks are studied with the aim of presenting different strategies of design that have been used in dynamic translinear circuits. A lot of work can still be realized on TL circuits, nevertheless, the huge advances achieved until now, and this is addressed in Sect. 13.4. In Sect. 13.5, a set of applications in analog signal processing are enumerated and related with the corresponding papers that have been published until now. Finally, conclusions associated with this study are given in Sect. 13.6.

13.2 Static Translinear Paradigm

A translinear circuit (TC) is a current-mode circuit based on non-linear current–voltage characteristic of the input port, which carries out its function using the translinear principle. The term *translinear* was first introduced by Gilbert in 1975, underlining the fact that *trans*conductance g_m is *linear* with current, for the case of BJT and MOS transistors in weak inversion. However, when transconductance is linear and voltage are used, another class of TCs based on quasi-quadratic law are obtained. The translinear principle (TP) consists in that a closed loop including an even number of translinear elements are arranged of manner that an equal number of them are placed clockwise (*CW*) and the rest in counter-clockwise (*CCW*). For the case of BJT transistors, the translinear loop (TL) is formed by the series connexion of base-emitter junctions, while ports gate and source are used in MOS transistors. Therefore, the non-linear relationship of the currents circulating through the *CW* elements equals the non-linear relationship of the currents circulating through the *CCW* elements. The translinear elements can be implemented by means of BJTs, MOS transistors, and FGMOS transistors. For the case of BJT transistors, and MOS transistors in weak inversion such a non-linear relationships is a product. For the case of MOS transistors working in the saturation region; it is a sum of current square-root. Both operations plus MOS transistors working in triode will be explained in the following sections.

Three basic configurations for forming TL loops can be implemented: (1) alternating cell (elements with different type of transistor are interconnected one to one in the TL), (2) balanced cell or stacked cell (elements with similar type of transistor are interconnected first, after the rest of transistors of the other type are joined to the TL) or (3) electronically simulated o tunable cell (elements are operated by adjusting the gate voltages making possible to cancel the possible circuit nonlinearity caused by the input voltages). These topologies are shown in Fig. 13.1 for *n*-channel MOS transistors, using a TL of four transistors for the case of Fig. 13.1a, and Fig. 13.1b. For the case of Fig. 13.1c; a floating gate realization is shown, since with these devices the extra circuitry to force the gate voltages is notably reduced.

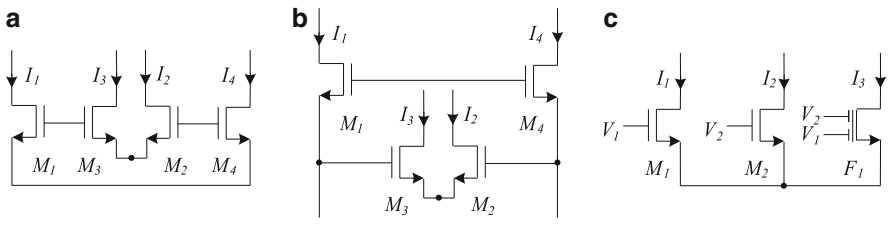

Fig. 13.1 Topologies of translinear circuits: (**a**) alternating, (**b**) balanced, and (**c**) electronically simulated

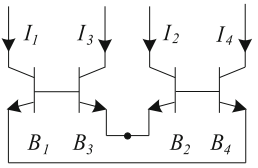

Fig. 13.2 Translinear circuits based on bipolar transistors

TCs are classified in two main groups: static translinear circuits (STCs) and dynamic translinear circuits (DTCs) [32]. STCs are used to implement linear and nonlinear transfer functions between the input and output of an analog circuit without the time as reference. Otherwise, DTCs can be used to obtain the same transfer functions but in these the frequency, phase or time dependence of the input signals is used as reference to manipulate the desired outputs. In the following subsections, the main nonlinear TL characteristics of MOS and BJT transistors will be introduced; but only from a mathematically and described point of view; since the pages number available for this chapter is limited, and there is not room to present the bias circuits required to force the input–output currents, thus, the readers are directed to References.

13.2.1 Translinear Circuits Based on Bipolar Junction Transistors

A bipolar junction transistor (BJT) is a three-terminal bidirectional electronic device used in the first generation of translinear circuits. Its terminals are called collector (C), base (B), and emitter (E) and has two junctions called: base–emitter (BE) and base–collector (BC). The collector–emitter (CE) current or output current is controlled by the BE current (current control), or by the BE voltage (voltage control).

The translinear principle exploits the exponential or logarithmic relationships between the base–emitter voltage (V_{BE}) and the collector current (I_C), which is holded for almost five decades of current, and it is expressed as:

$$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right) \quad \text{or} \quad V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right) \tag{13.1}$$

where I_S is the saturation current, and V_T is the thermal voltage of the device, respectively. A translinear circuit based on BJTs is illustrated in Fig. 13.2. Consider a general translinear circuit composed by i NPN transistors, and j PNP transistors in each direction, respectively. By applying the definition of the translinear principle given previously, then it can generically be established as:

$$\sum_{i\in\{CW\}} V_{BE_i} + \sum_{j\in\{CW\}} V_{EB_j} = \sum_{i\in\{CCW\}} V_{BE_i} + \sum_{j\in\{CCW\}} V_{EB_j} \tag{13.2}$$

or

$$\sum_{i\in\{CW\}} V_T \ln\left(\frac{I_{C_i}}{I_{S_n}}\right) + \sum_{j\in\{CW\}} V_T \ln\left(\frac{I_{C_j}}{I_{S_p}}\right) = \sum_{i\in\{CCW\}} V_T \ln\left(\frac{I_{C_i}}{I_{S_n}}\right) + \sum_{j\in\{CCW\}} V_T \ln\left(\frac{I_{C_j}}{I_{S_p}}\right) \tag{13.3}$$

where I_{C_i} and I_{C_j} are the collector currents associated with each transistor, and I_{s_n} and I_{s_p} are NPN and PNP saturation currents of the transistors, respectively. A simplification process to (13.3) is realized as follows: V_T can be omitted in all terms, and the sum of terms with natural logarithm can be replaced by products of currents. In addition, if all transistors are equal and $k = i + j$ is the number of junctions in each direction, then the translinear principle can be simplified as:

$$\prod_{(i,j)\in\{CW\}} \frac{I_{C_i} I_{C_j}}{I_{S_n} I_{S_p}} = \prod_{(i,j)\in\{CCW\}} \frac{I_{C_i} I_{C_j}}{I_{S_n} I_{S_p}} \quad \text{or} \quad \prod_{k\in\{CW\}} I_{C_k} = \prod_{k\in\{CCW\}} I_{C_k}. \tag{13.4}$$

Briefly, the biasing circuit of BJT TL circuits are easy, and a small number of transistors is needed for the implementations. Basically these circuits operate in Class-A, but replicating a forming proper input current the cell can operate in Class-AB.

13.2.2 Translinear Circuits Based on MOS Transistors

In the following, we consider that MOS transistors follows the quasiquadratic law; however in the new CMOS process this law can be seriously affected; nevertheless increasing the channel length this law can be valid, so there is a trade-off between area and quasi-quadratic law. Also, this law can only be valid for 2 decades of current. A metal-oxide-semiconductor field-effect transistor or MOS transistor is a four-terminal unidirectional electronic device. Its terminals are called gate (G), drain (D), source (S), and bulk (B). The latter commonly is tied to ground and/or bias voltage, and therefore, it is not considered in current and voltage relationships of the device as electrical variable. A threshold voltage (V_{th}) is the gate voltage necessary to form an inversion layer of carriers at the interface between the insulating layer (oxide) and the substrate (bulk) of the transistor, which have as aim to allow the flow of electrons or holes through the gate-source junction. MOSFETs have three operational modes:

- **Subthreshold or Weak-Inversion Mode $\mathbf{V_{GS} \approx V_{th}}$:** There is a weak-inversion current o subthreshold leakage due a insignificant flow of electrons at the source to enter the channel and flow to the drain, which is an exponential function of gate-source voltage. The weak-inversion current I_{DS} is expressed as:

$$I_{DS} \approx I_{D0} \exp\left(\frac{V_{GS} - V_{th}}{nV_T}\right) \tag{13.5}$$

where I_{D0} is the current at $V_{GS} = V_{th}$, i.e., $I_{D0} = I_s W/L$, V_T is the thermal voltage equal to kT/q, and the slope factor n is given by $n = 1 + C_D/C_{ox}$, where C_D is the capacitance of the depletion layer, and C_{ox} is the capacitance of the oxide layer per unit area. In this region of operating, the MOS transistors can be used in the same configuration of BJT TL loops. TL loops in weak inversion are used in artificial neural networks, log-domain filters [6, 7, 19, 28, 37, 38], multiplier/divider circuits [36], biochemical sensors [9], Lorenz oscillators [11], neural networks, and $\Sigma\Delta$ A/D converters [30]. This operation allows overall lower-power consumption for low-frequency applications [30], and the bulk terminal can be used to form an extra exponential relationship, which has not been fully exploited.

- **Triode, Ohmic or Linear Mode $\mathbf{V_{GS} > V_{th}}$ and $\mathbf{V_{DS} < (V_{GS} - V_{th})}$:** An electrical current between drain and source terminals occurs due to that a channel of electrical carriers is created. Such channel allows to the device to operate as a resistor controlled by the gate voltage relative to both the source and drain voltages. The drain-source current is expressed as:

$$I_{DS} = \mu C_{ox} \frac{W}{L} \left((V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right) \tag{13.6}$$

where μ is the charge–carrier effective mobility, W is the gate width, and L is the gate length.

- **Saturation, Active or Strong-inversion Mode $\mathbf{V_{GS} > V_{th}}$ and $\mathbf{V_{DS} > (V_{GS} - V_{th})}$:** A current flow between drain and source through a broader, two- or three-dimensional current distribution extending away form the interface and deeper in the substrate, due to the difference higher between drain voltage and gate voltage. The drain-source current is expressed as:

$$I_{DS} = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{th})^2 (1 + \lambda (V_{DS} - V_{DSsat})) \tag{13.7}$$

where λ is the channel-length modulation parameter. The maximum value of I_{DS} occurs when $V_{DS} = V_{DSsat}$, and therefore, I_{DS} is expressed as:

$$I_{DS} = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{th})^2. \tag{13.8}$$

A translinear circuit based on MOS transistors is illustrated in Fig. 13.1.

13.2.2.1 Translinear Principle for MOS Transistors in Strong Inversion

Consider a general translinear circuit composed by i p-channel MOS transistors, and j n-channel MOS transistors in each direction, respectively. For MOS transistors working in strong inversion, the translinear principle can be expressed as:

$$\sum_{i\in\{CW\}} V_{GS_i} + \sum_{j\in\{CW\}} V_{SG_j} = \sum_{i\in\{CCW\}} V_{GS_i} + \sum_{j\in\{CCW\}} V_{SG_j} \tag{13.9}$$

where

$$V_{GS} = V_{th} + \sqrt{\frac{2I_{DS}}{\mu C_{ox}\frac{W}{L}}} = V_{th} + \sqrt{\frac{I_{DS}}{K\frac{W}{L}}}. \tag{13.10}$$

If identical MOS transistors are used, then (13.9) is reduced to:

$$\sum_{(i,j)\in\{CW\}} \left(\sqrt{\frac{I_{DS_i}}{K_n\left(\frac{W}{L}\right)_i}} + \sqrt{\frac{I_{DS_j}}{K_p\left(\frac{W}{L}\right)_j}}\right) = \sum_{(i,j)\in\{CCW\}} \left(\sqrt{\frac{I_{DS_i}}{K_n\left(\frac{W}{L}\right)_i}} + \sqrt{\frac{I_{DS_j}}{K_p\left(\frac{W}{L}\right)_j}}\right) \tag{13.11}$$

Equation (13.11) involves K_n and K_p which are process dependent, but it can be simplified if only one type of MOS transistor is used as follows:

$$\sum_{j\in\{CW\}} \sqrt{\frac{I_{DS_j}}{\left(\frac{W}{L}\right)_j}} = \sum_{j\in\{CCW\}} \sqrt{\frac{I_{DS_j}}{\left(\frac{W}{L}\right)_j}} \quad \text{or} \quad \sum_{j\in\{CW\}} \sqrt{\frac{I_{DS_j}}{S_j}} = \sum_{j\in\{CCW\}} \sqrt{\frac{I_{DS_j}}{S_j}} \tag{13.12}$$

where j is the number of translinear elements, and $S = W/L$.
TL loops in strong inversion are used to form translinear loops or translinear circuits in RMS-DC converters [3, 17], chaotic analog noise generators [5], a differentiator circuit [14], a flipped voltage followers (geometric-mean circuits and squarer/divider circuits) [16], square-root domain filters [18, 21–23], log domain filters [24, 25, 27, 28, 32, 40], integrators [26], oscillators [29], square-root circuits [33], squarer/dividers [33], and multiplier/divider circuits [33, 39]. Most of above references uses four transistors single loops for the cell implementation operating in Class-A, however in [3] multicoupled cells are proposed operating in Class-AB. These last procedure has no be generalized, and can be a challenge for a new research.

13.2.2.2 Translinear Principle for MOS Transistors in Triode

To overcome the increased parametric mismatch and poor frequency response of translinear circuits operating in weak inversion, and the lack of differential outputs in translinear circuits working in strong inversion, in [58] it is proposed a novel scheme to develop translinear circuits in the triode region of MOS transistors. Consider a general translinear circuit composed by i p-channel MOS transistors working in triode, the translinear principle can be expressed as (13.9), where

$$V_{GS} = \frac{I_{DS}}{\mu C_{ox}\left(\frac{W}{L}\right)V_{DS}} + \frac{V_{DS}}{2} + V_{th} \tag{13.13}$$

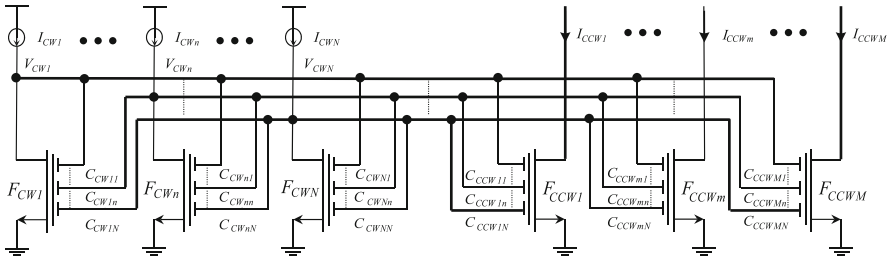

Fig. 13.3 Translinear circuits based on FGMOS transistors

If V_{th} is matched for all transistors, all transistor have the same dimensions, and V_{DS} it is considered very small or equals in a first approximation, then the translinear principle can be expressed as:

$$\sum_{j\in\{CW\}} \frac{I_{DS_j}}{V_{DS_j}} = \sum_{j\in\{CCW\}} \frac{I_{DS_j}}{V_{DS_j}} \tag{13.14}$$

There are a few research works on [58]; and there is an open door for further implementations. One line to follow can combine triode MOS transistors with FGMOS. The circuits proposed in [58] are used to demonstrate the principle and the bias circuits, thus an optimized design of the circuits or simplifications can be desirable.

13.2.3 Translinear Circuits Based on FGMOS Transistors

A floating gate MOSFET (FGMOS) was used in the third generation of translinear circuits, which is a field-effect transistor with a floating node in DC and a finite number of secondary gates or inputs which are electrically isolated of the floating gate (FG). Such inputs are only capacitively coupled to the FG, and therefore, this device is called a MITE (multiple-input translinear element) [102]. It has N inputs with an input voltage that can represented as a weighted summation, where V_n is the input voltage of the nth input and w_n is the constant gain or weighting coefficient of the corresponding input $w_n = (C_n/C_T)$, that is, partial capacitance between total capacitance, being C_n large to reduce nonlinear parasitic capacitances. The gate voltage for the case of MOS transistor can be expressed as:

$$V_{GS} = \sum_{n=1}^{N} w_n V_n \tag{13.15}$$

A general translinear circuit based on FGMOS transistors is illustrated in Fig. 13.3. It is composed by a set of N input transistors labeled as F_{CW1} to F_{CWN}, and a set of M ouput transistors labeled as F_{CCW1} to F_{CCWM}. N input currents (I_{CW1}, ... ,

I_{CWN}) bias to the N input transistors producing N drain voltages ($V_{CW1}, \ldots, V_{CWN}$) forming a $N \times N$ input connectivity matrix, $\mathbf{C_{CW}}$. C_{CWnk} is a capacitive coupling between the drain of F_{CWk} and the floating gate of F_{CWn}. The circuit generates M output currents ($I_{CCW1}, \ldots, I_{CCWM}$) by combining the N drain voltages in a $M \times N$ output connectivity matrix, $\mathbf{C}_{CCW}$. C_{CCWmn} is a capacitive coupling between the drain of F_{CWn} and the floating gate of F_{CCWm}. If all FGMOS transistors are identical and matrix $\mathbf{C_{CW}}$ has inverse, then, the translinear principle for weak inversion and strong inversion, respectively can be expressed as:

$$\prod \mathbf{I}_{CCW}^{\mathbf{C}_{CW}} = \prod \mathbf{I}_{CW}^{\mathbf{C}_{CCW}} \tag{13.16}$$

$$\mathbf{C}_{CW} \sqrt{\mathbf{I}_{CCW}} = \mathbf{C}_{CCW} \sqrt{\mathbf{I}_{CW}} \tag{13.17}$$

In strong inversion, I_{CCW} is dependent of capacitive coupling as a multiplicative factor, while, in weak inversion, the I_{CCW} is dependent of capacitive coupling as an exponent. FGMOS transistors provide versatility to TL principle leading simple bias circuitry, but the capacitors coupled to the gate lead to small bandwidth, and an increment in area.

13.3 Dynamic Translinear Paradigm

The dynamic translinear principle is formed adding capacitors to the inputs and/or outputs of basic translinear components [32, 69, 76, 100]. It is possible implement all kinds of frequency-dependent or time-dependent linear transfer functions. The DTCs allow us to realize linear filters, and linear- and nonlinear differential equations. These later has been used for realizing mixer-filter combinations, oscillators, phase-locked loops, syllabic companding filters, and chaos generators [84, 91, 95, 106].

In order to describe DTC, we will use an integrator as example, and the generalization of DTC can be found in References. Consider a translinear circuit represented by the block diagram shown in Fig. 13.4. The current inputs denoted as i_{in} and i' are supplied to a divider block, whose output current is denoted as $I_0(i_{in}/i')$, where I_0 is a normalizing constant. This current is integrated by means of the capacitor C, generating the voltage v. Next, the voltage v is introduced to the nonlinear block to produce two equal general output currents. One of such currents is supplied together with the voltage v to a derivative block, which generate the input current i' that can be expressed as $V_0(di_{out}/dv)$, where V_0 is a normalizing constant. Output currents can be expressed as $i_{out} = f(v)$.

Of the expression of i', it is possible to obtain an equation for the derivative of the output current:

$$\frac{di_{out}}{dv} = \frac{i'}{V_0} \tag{13.18}$$

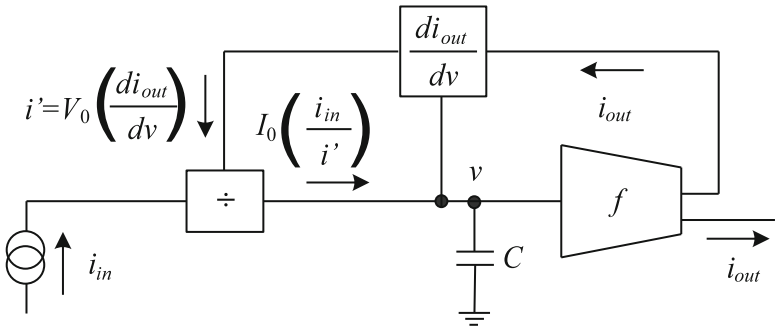

Fig. 13.4 Dynamic translinear principle

The capacitor current is equal to the current generated by the divider, then

$$I_{cap} = C\frac{dv}{dt} = I_0 \frac{i_{in}}{i'}, \tag{13.19}$$

which can also be expressed as:

$$\frac{dv}{dt} = \frac{I_0}{C}\frac{i_{in}}{i'}. \tag{13.20}$$

Equations (13.18) and (13.20) can be related by means of the chain rule as follows:

$$\frac{di_{out}}{dt} = \frac{di_{out}}{dv}\frac{dv}{dt}. \tag{13.21}$$

By substituting (13.18) and (13.20) in (13.21), it can be rewritten as:

$$\frac{di_{out}}{dt} = \frac{i'}{V_0}\frac{I_0}{C}\frac{i_{in}}{i'} = \frac{I_0}{V_0 C} i_{in} \tag{13.22}$$

The output current can be obtained by integrating (13.22) with respect to the time:

$$i_{out} = \frac{I_0}{V_0 C}\int i_{in} dt \tag{13.23}$$

Equations (13.18) to (13.23) are generals and can be used to implement different companding systems. If f in Fig. 13.4 is a exponential law the systems are called log-domain; and if f is the quasiquadratic law the systems are called square-root domain. Note that the divider can be implemented using static translinear circuits. For the case of log-domain usually only one loop of four elements is required, and for the square-root domain, at least 2 loops or 1 multi-coupled loop is necessary.

13.3.1 log-Domain Circuits

log-Domain filters are a subclass of dynamic translinear circuits that develop linear transfer functions using exponential functions f in Fig. 13.4 [4, 6–8, 19, 20, 22–25, 27–31, 34, 35, 38, 40, 42–47, 50–52, 54–56, 62, 65, 67, 70, 74, 75, 78, 81–98, 106]. The nonlinearity is directly exploited without depending on linearization. Thanks to overall linear behavior, they can be used in applications where are needed a large-signal linearity. These are also called as translinear filters, companding current-mode filters, or exponential state-space filters. Among the advantages that a log-domain filter offers are: (1) only transistors and capacitors are required for its implementation, and (2) for ultra low-power applications, the absence of resistors in the filters reduce the size of the VLSI design.The filters have been designed for four different approaches: Chebyshev [6, 19], Bessel [7], Elliptic [19, 24], and state-space synthesis [8, 18, 19, 21, 23, 24, 27, 28, 31, 32, 35, 37, 40]. Additionally, these filters have been implemented using topologies either ladder [6, 7, 19], multiple feedback [8, 14, 18, 19, 21, 23, 24, 27, 28, 31, 32, 35, 37, 40] or biquad [4, 22, 23, 34, 38].

13.3.2 Square-Root Domain Circuits

Among its advantages are: operation to low-voltage, operation to low-power, large dynamic range, high-frequency applications, and electronic tuneability. Until now, there are three different synthesis methods for square-root domain circuits: (1) state-space synthesis, (2) signal flow graph synthesis, and (3) the substitution of the LC ladder of the equivalent circuit by their square root domain equivalents.

Through square-root domain circuits, it is possible to design state variable filters by means of one or more integrators connected in some feedback configuration, where each integrator represents one state and each output voltage of them is considered one state variable [14, 18, 21, 23, 26, 49, 73, 103, 104, 107]. The main advantages of these filters is that: (1) the use of different states as outputs generates different kinds of filters, (2) the circuit can directly realize the state-space models proposed, and (3) larger signal swings. A clear example of this type of filters is the Kerwin–Huelsman–Newcomb (KHN) biquad filter.

13.3.3 Dynamic Nonlinear Building Blocks

Square-root circuits, squaring circuits, geometric-mean circuits, current conveyors, and/or squarer/divider circuits are the basic blocks for designing multiplier/divider circuits [1, 33, 36, 39]. Multipliers/dividers, squarers/dividers, geometric-mean circuits, square-root circuits, and/or squaring circuits are elemental to build a RMS-to-DC converter or a flipped voltage followers [2, 3, 16, 17]. The integrators,

geometric-mean circuits, multipliers/dividers, logarithmic circuits, exponential circuits, square-root circuits, squarer/divider circuits, squaring circuits, current conveyors, and/or multipliers are fundamental elements of analog filters [4, 6, 7, 18, 19, 21–25, 27, 28, 31, 32, 34, 37, 38]. A harmonic mixer, modulators and frequency doublers can include multiplier circuits [10, 33]. A differentiator can contain geometric-mean circuit and multipliers [14, 15, 20]. Low-voltage current controlled current conveyor can be used as basic blocks to design current mode filters. An integrator can be designed by means of geometric-mean and multiplier/divider blocks [26, 32]. Oscillators can be based on translinear current conveyors, which have frequency of oscillation and the condition of oscillation controlled electronically, and independently of the bias current [13]. Also, the oscillators can have as elemental blocks analog filters, square-root circuits, squarer/divider circuits, and geometric mean circuits [14, 22, 27, 29]. $\Sigma\Delta$ A/D converters can be implemented using analog filters, and integrators as basic blocks [30].

13.4 Open Research Lines

In spite of the design advantage that TL systems provides; there are still some open research fields that requires investigation. Among these we can find, the noise performance, to find a systematic method to synthesize the cells; since now most of the proposals are based on four loop transistors. To explore another operation regions completing the possibility design, for example MOS transistor working in triode. Moreover also another TL structures can be explore for example CCII and diodes.

Analog noise generators for applications such as cryptography systems (watermarking systems), and secure communications (spread spectrum) [5, 11] must be developed using controlled gain in the feedback loop and null intermittency effect, which only can be obtained by means of translinear circuits. In artificial neural networks, the use of translinear circuits is searching modularity, scalability, computational density, real time operation, and power efficiency. A lot of work related with these topics must be realized.

Methods with the aim of reducing the errors generated by the second order effects in translinear loops have been discussed [1, 2, 6, 11, 17, 21, 30, 33, 34, 36–38], which are based in the changes in V–I relationship associated with the reduction of MOS transistors, smaller chip size and much higher operation frequencies. Between the effects before mentioned that must still be completely studied are body effects, mobility reduction, weak inversion, channel length modulation, component mismatch, parasitic resistances and capacitances, input and/or output resistance, multiple operating points (MOPs), waveform asymmetry, cycle limit, chaos, thermal noise, and temperature dependence of these parameters.

The use of graph theory as a tool of design and analysis has been poorly exploited [60, 73, 108, 109]. In the future, these techniques will must be more used to verify and optimize the efficiency and performance of translinear circuits.

Although the companding technique permits the design of filters featuring small distortion levels, large signal-to-noise ratios, low supply voltages, and wide bandwidths, it may also give rise to externally-nonlinear behavior. The occurrence of unwanted limit-cycle behavior in log-domain filters is reported in [107] and investigated in [67]. The appearance of multiple operating points in such filters is discussed in [105]. So far, these nonlinear phenomena have been reported only in log-domain filters and more recently in instantaneously digital companding [55,78]. But the square root-domain filters may also suffer from external nonlinearity. In [104], a fully-differential class-AB second-order SRD filter is designed, and then modified according to a standard linear IC design technique, i.e. any pair of equal-value capacitors, each connected between a node and ground, is replaced with a single half-sized floating capacitor, placed between those nodes. This saves IC area, but may induce zero-input limit cycle behavior under particular conditions describe in [104].

13.5 Applications

This section is devoted to describe the applications that can be implemented by TL principle, but are not described in the previous sections: square-root circuits [1, 2, 14, 18, 21–23, 26, 27, 29, 33, 40, 49, 69, 73], squarer/divider circuits [1, 3, 17, 21, 22, 25, 33, 36, 39, 40, 57, 64, 72, 103], multiplier/divider circuits [1, 7, 19, 25, 26, 33, 36, 39, 57, 59, 72, 73], squaring circuits [2, 14, 16, 28, 29, 36, 69], geometric mean circuits [2, 3, 6, 7, 14, 17, 21, 22, 25, 26, 29, 36, 39, 40, 60, 70, 72, 73, 79, 83, 99], differentiators [6–8, 14, 20], integrators [4, 6, 15, 26, 31, 34, 45, 48, 51, 67, 70, 73, 83, 84, 86, 88, 90, 94, 96–98], filters low pass, high pass, band pass, all pass, notch, low pass notch, high pass notch, sinh, tanh, log-domain, square-root, wave, anti-aliasing, and adaptive filters) [4, 6–8, 14, 16, 18–25, 27, 28, 31, 32, 34, 35, 37, 38, 40, 43–45, 48–52, 55, 56, 64, 65, 67, 69–76, 78, 81–83, 85–90, 92, 94–98, 103, 104], oscillators [11, 14, 16, 22, 27, 29, 43, 46, 47, 80, 91], multipliers [4, 9, 14, 16, 20, 42, 58, 73], RMS-DC converters [2, 3, 16, 17, 69], modulators [33], harmonic mixers [10], phase shifters [41], sine/cosine synthesizers [13, 43, 63], fuzzy logic controllers [61, 77], artificial neural networks [61, 93], cryptography systems [5], chaotic analog noise generators [5, 11, 46, 47, 67, 91], programmable gain current amplifiers [12, 59, 62, 68, 77, 89, 101], current conveyors [13], $\Sigma\Delta$ A/D converters [30, 77], frequency multipliers [41, 60, 63], exponential function converters [42, 54], group-delay equalizers [44, 48], divider circuits [53, 69, 83, 89], sensors [53, 66], RMS detectors [64], 2-D vector-magnitude circuits [69], 2-D vector-normalization circuits [69], defuzzifiers [77], one-quadrant multiply-reciprocal circuits [79], etc. Some of these cells are used as building blocks of the above applications.

FGMOS retain a long time the injected charge in the gate and then weighted voltage addition at the input terminals is a direct consequence. Such qualities provide attractive characteristics as accuracy, high-speed, and compactness. MITEs have specific applications [3, 6, 19, 69, 71, 75, 77, 79, 88] such as weighted average circuits

for resistive networks, defuzzifiers, FIRs, common-mode feedback networks, sigma-delta modulators, log-domain filters, multipliers/dividers, integrators, square-root circuits, squaring circuits, one-quadrant divider circuits, 2-D vector-magnitude circuits, 2-D vector-normalization circuits, RMS-to-DC converters, geometric-mean circuits, and fast A/D and D/A converters.

13.6 Conclusions

Translinear circuits use the large signal characteristic of transistors to implement static-dynamic systems, processing the signals nonlinearly. These systems are versatile, and can provide a very well solution in the current scenario of low voltage, low power, and high efficiency circuits. The chapter is a survey of the techniques that have been proposed in the last years; such techniques have been reviewed as a tutorial for beginners in the field, but it can be used as reference for researches since the number of publications and results are so many, that all the information cannot be acceded from only one source, and this is one of the objectives of this survey. Finally, some uncover topics, and new research lines were discussed in order to show a general frame of translinear circuits.

Acknowledgements This work was supported by the Spanish Ministerio de Ciencia e Innovacion and the European Regional Development Fund (FEDER) under Grant TEC2010–21563-C02–01. The first author wish thank to their wife and son for your time to realize this study, and to PROMEP agreement 92434 for the support to this project.

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E. Tlelo-Cuautle (ed.), *Integrated Circuits for Analog Signal Processing*,
DOI 10.1007/978-1-4614-1383-7,

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