Integrand Software, Inc.

EMX ®

A Large-Scale Full-Wave Simulator for RF Designs

Integrand Software, Inc.

www.integrandsoftware.com

Integrand Software

- Integrand Software founded in 2003
- Founders from Bell Labs
- Formed company to target RF and RF IC design
- Focus on accuracy, speed and ease of use
- Successful company!
- Many of the world's major foundries and design houses now use the Integrand's products

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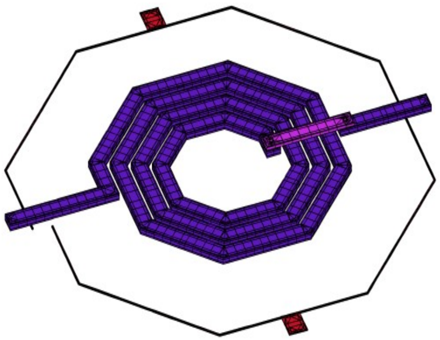
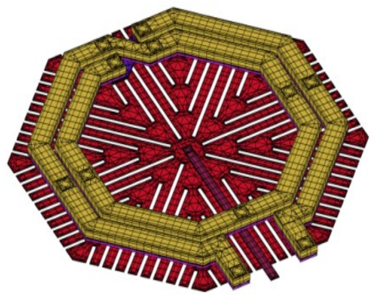
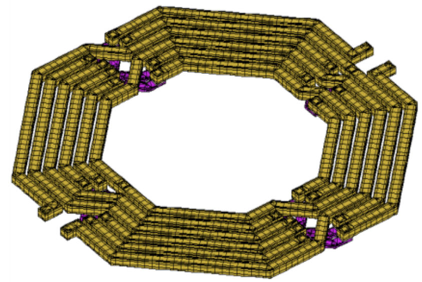
EMX modeling of passives



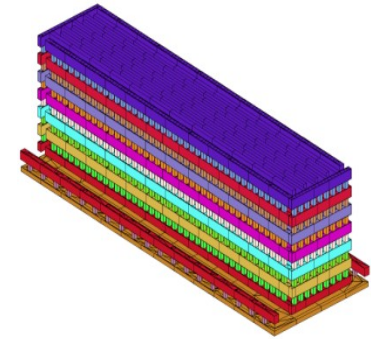
Inductor



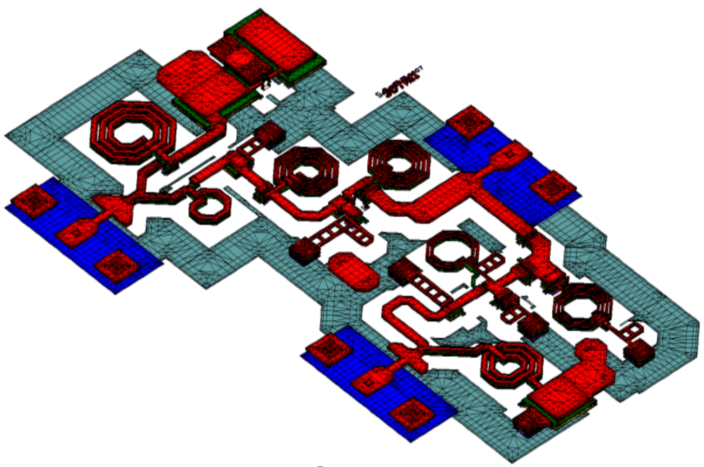
Shielding



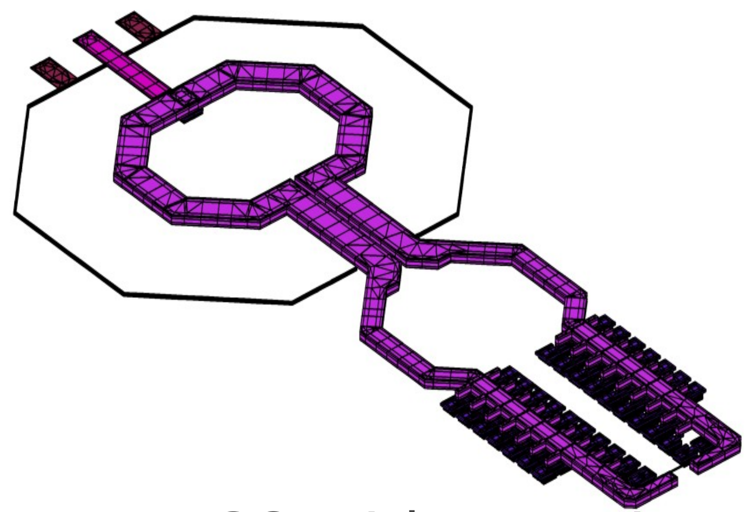
Transformer



MOM capacitor



Diplexer



VCO with capacitor bank

EMX (ElectroMagnetic EXtraction)

- Large scale full-wave, planar 3D electromagnetic simulator for verification and design of integrated circuits
- A powerful engine handles all electromagnetic effects in an unified manner
- Fast and very accurate
- Simulate full component ensembles with all couplings to avoid various sources of error
- Very easy to use
  - Mask Layout to S-parameters or spice models
  - Eliminates layers of intermediate steps and potential errors
  - Integrated into the Cadence Virtuoso® environment

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EMX Customers

tsmc, GLOBALFOUNDRIES, UMC, IBM, SMIC, ST, TPSCo

BROADCOM, SAMSUNG, MEDIATEK, QUALCOMM, MARVELL, AVAGO TECHNOLOGIES, ANALOG DEVICES

SKYWORKS, Rambus, HUAWEI, NVIDIA, XILINX, maxim integrated, SILICON LABS, TOSHIBA, FUJITSU

REALTEK, Microsemi, Alcatel·Lucent, MAXLINEAR, imec, LG, SPREADTRUM, MICROCHIP

CISCO, dialog SEMICONDUCTOR, ARM, freescale, Finisar, MegaChips, RFMD, ciena, ZTE中兴

STATSChipPAC, RDA, DENSO, GUC, PMC PMC-SIERRA, CERAGON, cadence, Lantiq

Quantenna Communications, PERASO, Atmel, VIA Telecom Mobile Communication Innovations, RAONTECH, Tensorcom Extreme Wireless, TELEDYNE LECROY Everywhereyoulook, THine

BlackBerry, invecas, Credo, D-CLUE Technologies, MoSys, PXI, SiliconMotion, LUXTERA, proteus DIGITAL HEALTH, AVNERA, CORTINA

Foundry Relationships

- The world's major foundries have chosen EMX for characterization and models for passives.
- We have a very close relationship with the foundries
- Foundry qualifies technology files with measurements provides customers with technology files
- High accuracy can be guaranteed for the customers using the EMX design flow.
  - **TSMC** (180nm, 130nm, 90nm, 65/55nm, 45/40nm, 32/28nm CMOS, 20nm, 16nm, 10nm)
  - **UMC** (130nm, 90nm, 65nm, 45nm, 28nm CMOS)
  - **IBM** (180nm SiGe, 5PAE, 7WL, 9RF, 45nm CMOS)
  - **Global Foundries** (130nm to 14nm)
  - **TowerJazz** CA 18HR, SBC18HX, SBC18PTH
  - **ST** B9MW, H9SOIFEM, 14FDSOI, 28FDSOI

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Difficulties with other EM tools

- Low Efficiency
  - Tradeoff between Accuracy and Computation Time/Expense. Traditional full-wave EM simulation is too long.
- Low Accuracy
  - Approximations are made to overcome inefficiency (2.5D methods), insufficient meshing or inaccurate matrix solution
  - Cannot handle true dielectric profiles with 10s of layers; often need to be approximated
- Not user-friendly
  - Cannot handle true mask GDSII layout with vias, slotting rules, dummy fill, etc.
  - Demand lots of human effort to “massage” layout, such as , merging vias, removing fill, simplifying the geometry so that the simulator can accept the input.
  - Simple user interface to Cadence Virtuoso®

EMX Design Flow

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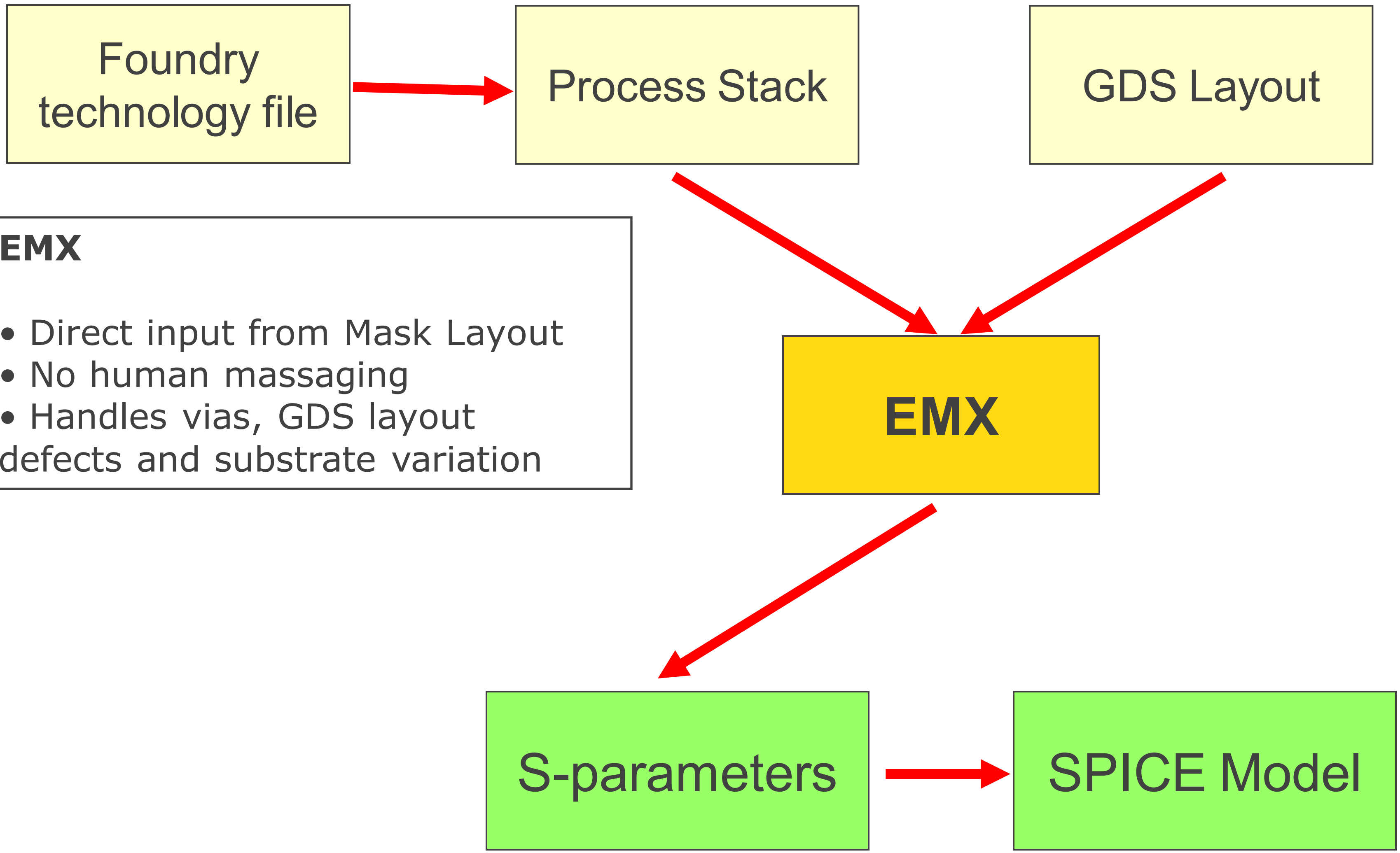
EMX

- Direct input from Mask Layout
- No human massaging
- Handles vias, GDS layout defects and substrate variation

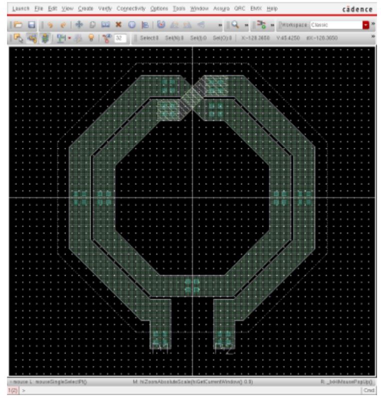


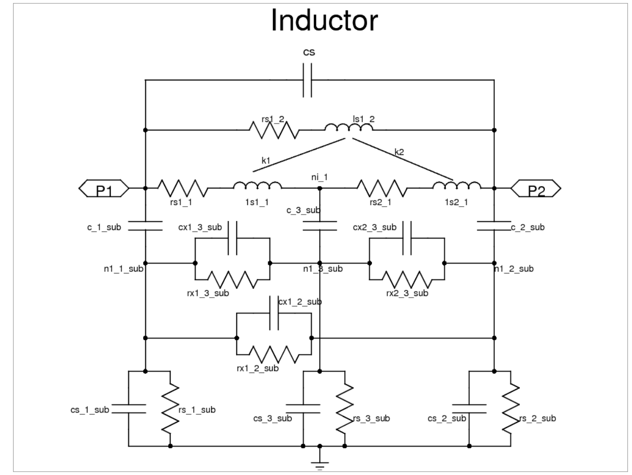
Models

- The results of EMX can be used in higher level Spice simulators like Spectre
- EMX can generate three kinds of models
  1. S-parameters
  2. RLCK models for basic passive s (inductors, baluns, caps)
     - Used by major foundry PDKS (TSMC, GF, UMC, IBM).
     - Physical topology
  3. RCLK + Control sources (pole zero models): VCOs, LNAs
     - Non-physical topology
- S-parameters are the most accurate result
- RLCK template models are used for transient analysis when S-parameters result in non-convergence in the time domain
- PZ models are used when the lumped models don't suffice (multiport circuits, e.g., 20 ports)

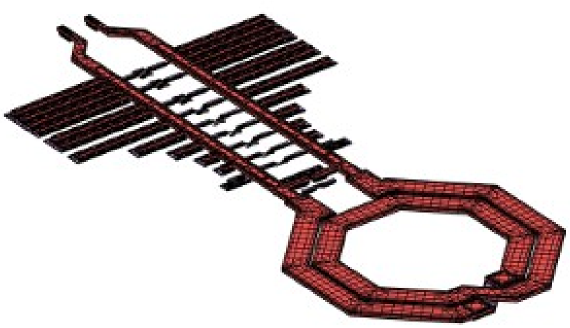
Spice Models

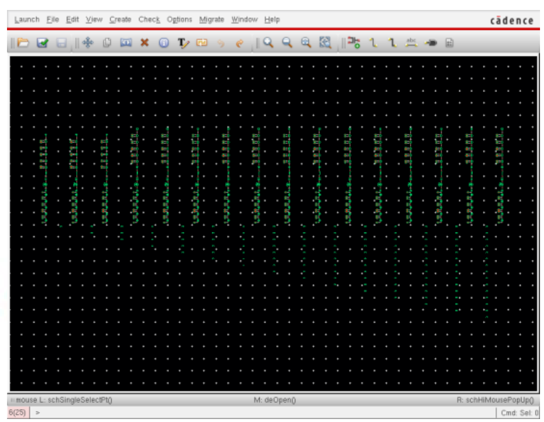
- Lumped models

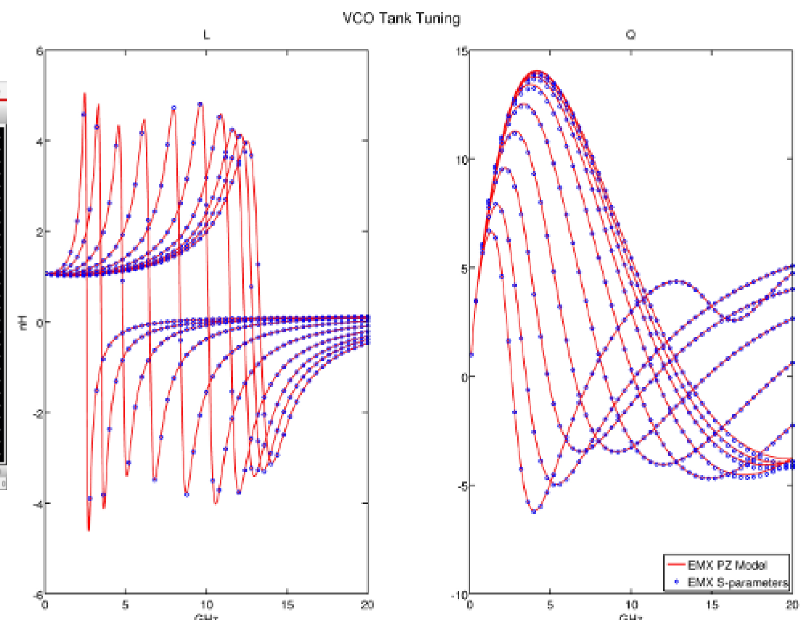




- Pole Zero models







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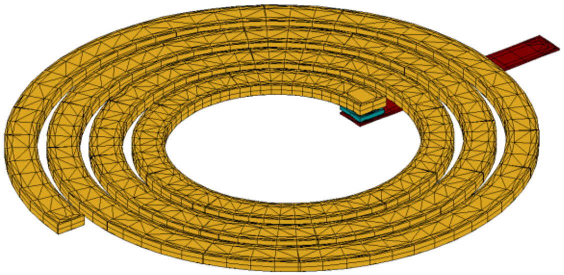
Distinguishing features of EMX

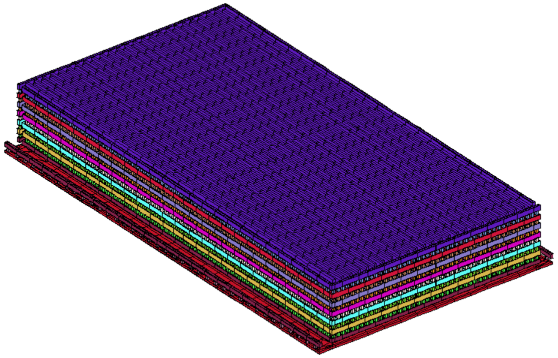
1. Accuracy
   - Uncompromised accuracy in solving Maxwell's equations
2. Speed
   - The fastest EM simulator, based on the Fast Multipole Method
3. Easy to use
   - Easy to use from within Cadence or from command line scripting

Accuracy (Electromagnetics)

- All physical effects included
  - R, L, C, substrate in a fully coupled manner
- Inductance
  - Distributed 3D volume currents
- Resistance
  - Skin effect and volume loss
- Capacitance
  - Accurate side-wall capacitance
  - MIM and thin-film capacitors
- Substrate
  - Multi layered lossy substrates
  - Substrate doping and bias
- Vias
  - Via inductance and capacitance

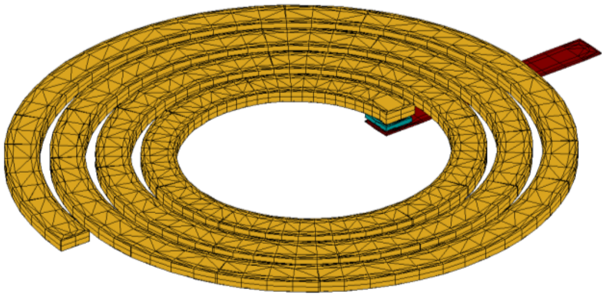
$$E_s(r) = \frac{1}{\sigma}J(r) + j\omega A(r) + \nabla\phi(r)$$





Speed (Numerics)

- Integral Equation-based
- 3D EM Field Solver
  - Preconditioned iterative methods
  - New "Full-Wave" FMM
  - Layout-regularity exploited
  - Adaptive Fast Frequency Sweep using Krylov subspace techniques
- Speed
  - 2 orders of magnitude faster than finite-element tools
  - 1 order faster than BEM
  - Even faster with multi-threading



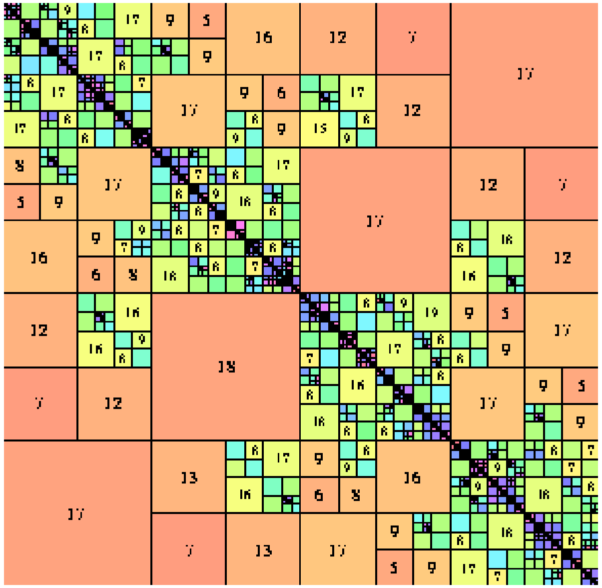
9244 basis functions
13692 vector potential elements
4877 scalar potential elements

Freq. Range	Simulation	Time	Memory
5 GHz	1	40 sec	7 MB
0.1 to 20 GHz	Sweep (201)	90 sec	22 MB

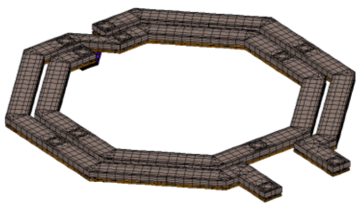
AMD Athlon XP 3200
2.2 GHz, 1GB RAM

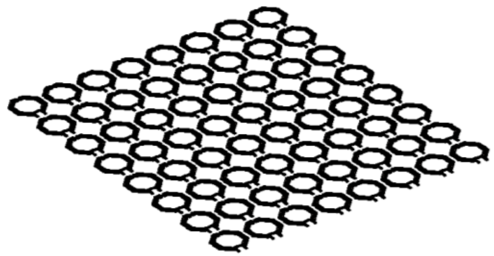
Foundation of EMX

- Uses the hierarchical Fast Multipole Method for rapid solution
  - Nearby regions are handled directly
  - Far regions are approximated to fixed precision
- Solution time is O(N) in time and memory, i.e. double the problem size, double the time
  - as opposed to N^2 or N^3
- Can solve very large problems with minimal computer resources



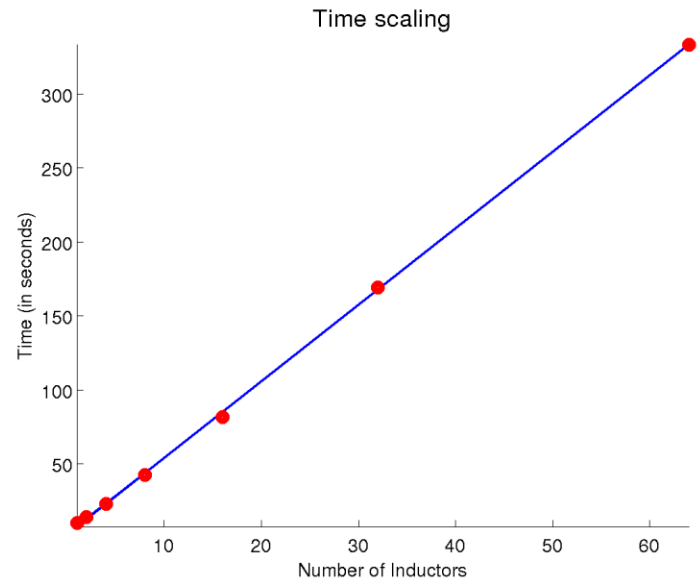
Time and Memory scaling

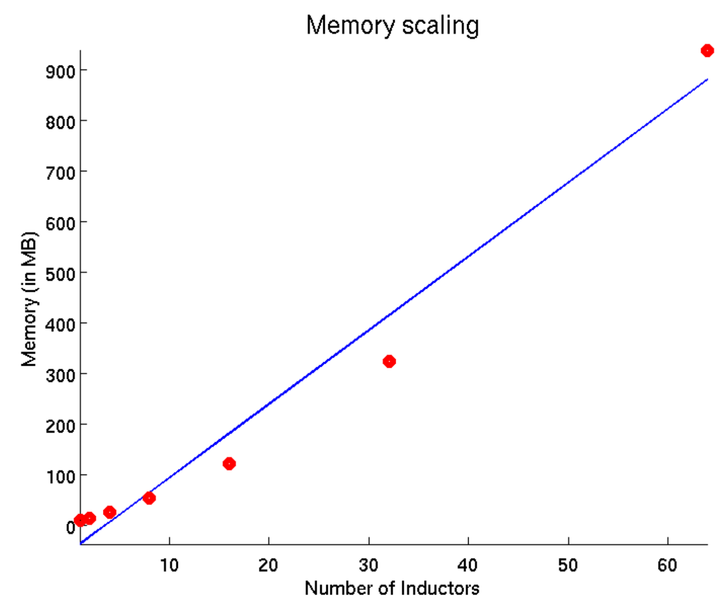




1 inductor 64 inductors

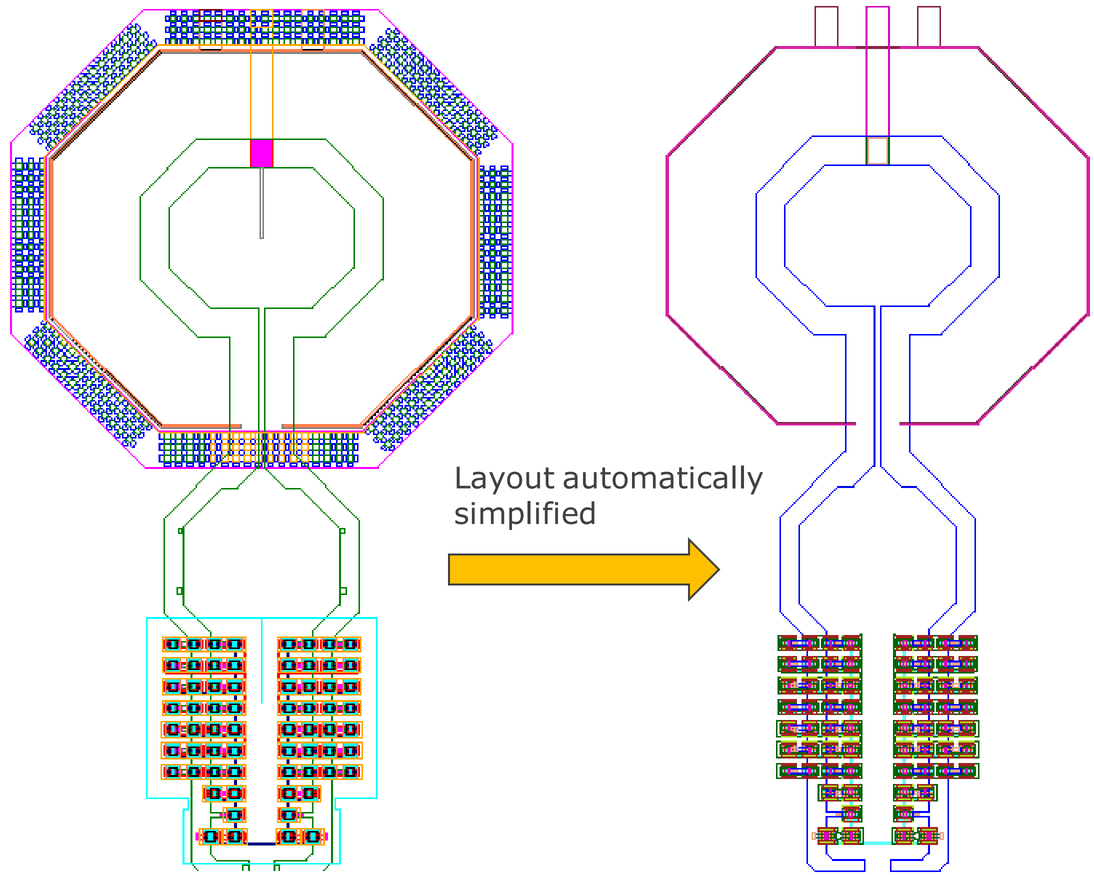
- Single frequency simulation (including iterative solve)
- Compare speed and memory for 1, 2, 4, 8, …, 64 inductors





Easy to Use

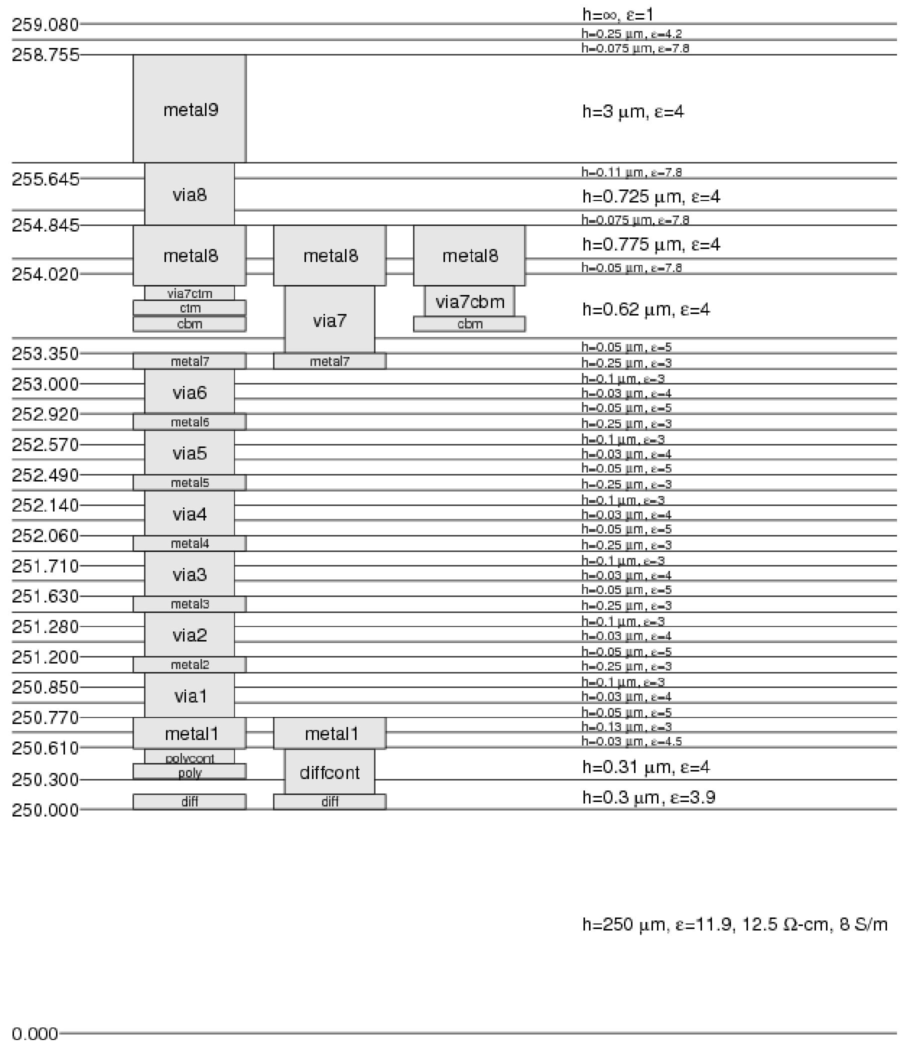
- EMX accepts true mask layout and will automatically simplify the layout for meshing and EM simulation
  - Via arrays, slotting rules, metal fill simplified
  - Boolean masking operations can be performed
  - Can apply grows and shrinks to the geometry including half-node scaling and metal bias
- **What goes to mask goes to simulator!**



Vias merged
Fill removed
Metal bias applied
MiM cap bank handled

Easy to Use

- Accepts true dielectric profile with no approximation to inter-layer dielectrics
  - Foundry provided tech file
  - 10s of dielectrics
  - Array and bar vias
  - Thin film MiM capacitors
  - Variable sheet resistance and metal width as a function of proximity
  - Context dependent vias (e.g. same via used for metal-poly or metal-diffusion)
  - True lossy layered substrates
  - Thru-silicon vias



metal9: h=3 µm, 6 mΩ/sq
metal8: h=1 µm, 20 mΩ/sq
ctm: h=0.1 µm, 20 Ω/sq
cbm: h=0.2 µm, 0.5 Ω/sq
metal7: h=0.25 µm, 0.18 Ω/sq, bias 10 nm
metal6: h=0.25 µm, 0.18 Ω/sq, bias 10 nm
metal5: h=0.25 µm, 0.18 Ω/sq, bias 10 nm
metal4: h=0.25 µm, 0.18 Ω/sq, bias 10 nm
metal3: h=0.25 µm, 0.18 Ω/sq, bias 10 nm
metal2: h=0.25 µm, 0.18 Ω/sq, bias 10 nm
metal1: h=0.18 µm, 0.2 Ω/sq, bias 5 nm
poly: h=0.1 µm, 14.9 Ω/sq, bias -0.5 nm
diff: h=0.086 µm, 16.9 Ω/sq

via7ctm: h=0.0273 µm, 0.5 Ω/via
via7cbm: h=0.145 µm, 0.5 Ω/via
via8: h=0.91 µm, 0.4 Ω/via
via7: h=0.495 µm, 0.2 Ω/via
via6: h=0.18 µm, 2 Ω/via
via5: h=0.18 µm, 2 Ω/via
via4: h=0.18 µm, 2 Ω/via
via3: h=0.18 µm, 2 Ω/via
via2: h=0.18 µm, 2 Ω/via
via1: h=0.18 µm, 2 Ω/via
polycont: h=0.17 µm, 20 Ω/via
diffcont: h=0.504 µm, 26 Ω/via

TSMC iRCX technology files

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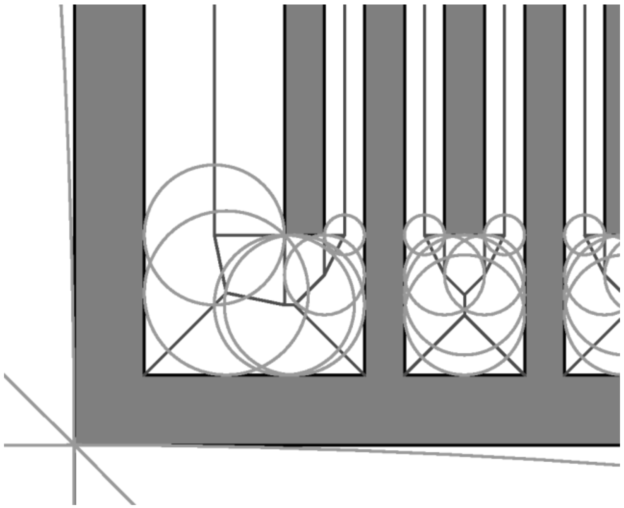
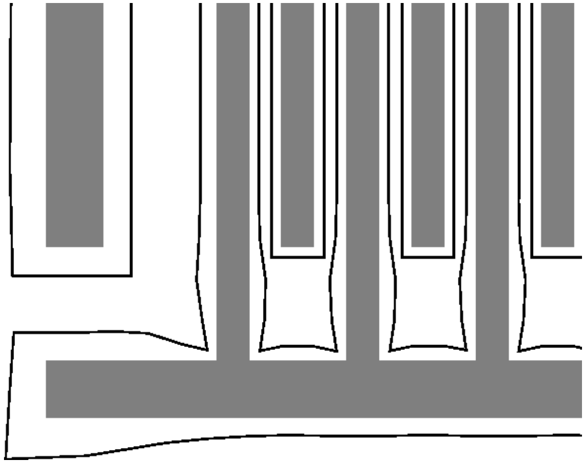
- Accurate process parameters are critical for EM simulation
- TSMC iRCX file provides a detailed process information
  - Metal, dielectric properties
  - Temperature dependence
  - Statistics and corner cases
  - Width-spacing dependent properties
  - Designer does not have to enter information from design manual
  - Removes sources of error
- Width and spacing properties (paper at RFIC 09 with TSMC)
  - Mimics fabrication process
  - shows that this <u>significantly improves simulation accuracy</u> for passive components like inductors and MOM capacitors.

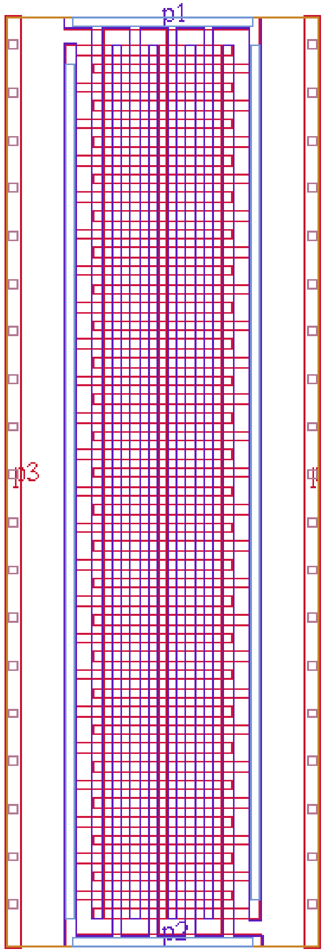
Mimicking the TSMC fabrication in EMX

- EMX uses Voronoi diagrams to capture the width-and-spacing dependent parameters in the iRCX files
- These Voronoi diagrams are used to alter the drawn layout to mimic the fabrication process
- The shaded region shows the “drawn” layout and the “line” shows the modified layout according to the iRCX rules

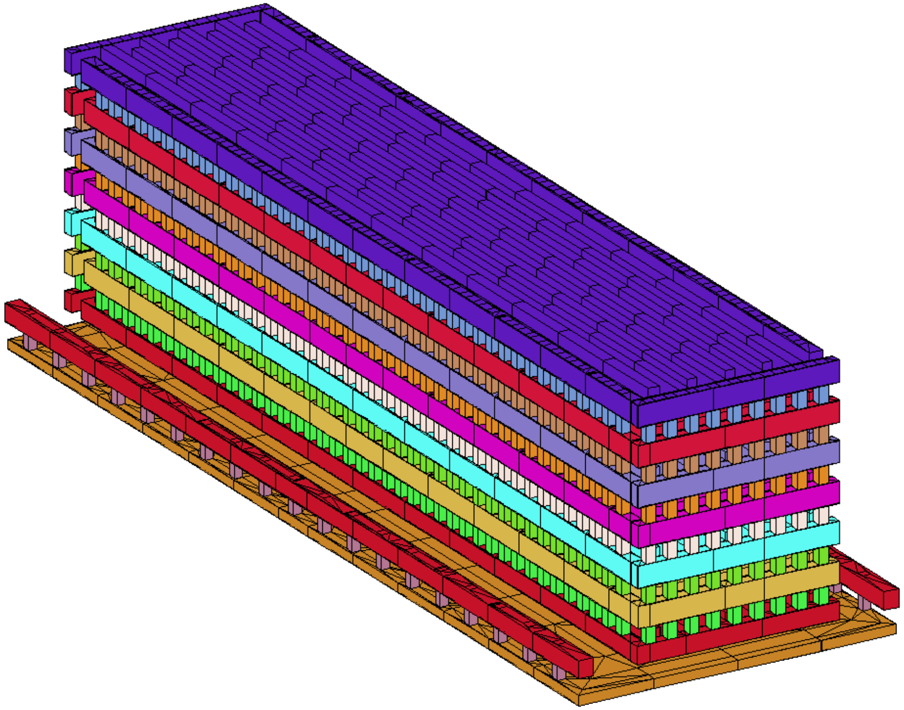




Typical TSMC MOM capacitor and EMX mesh

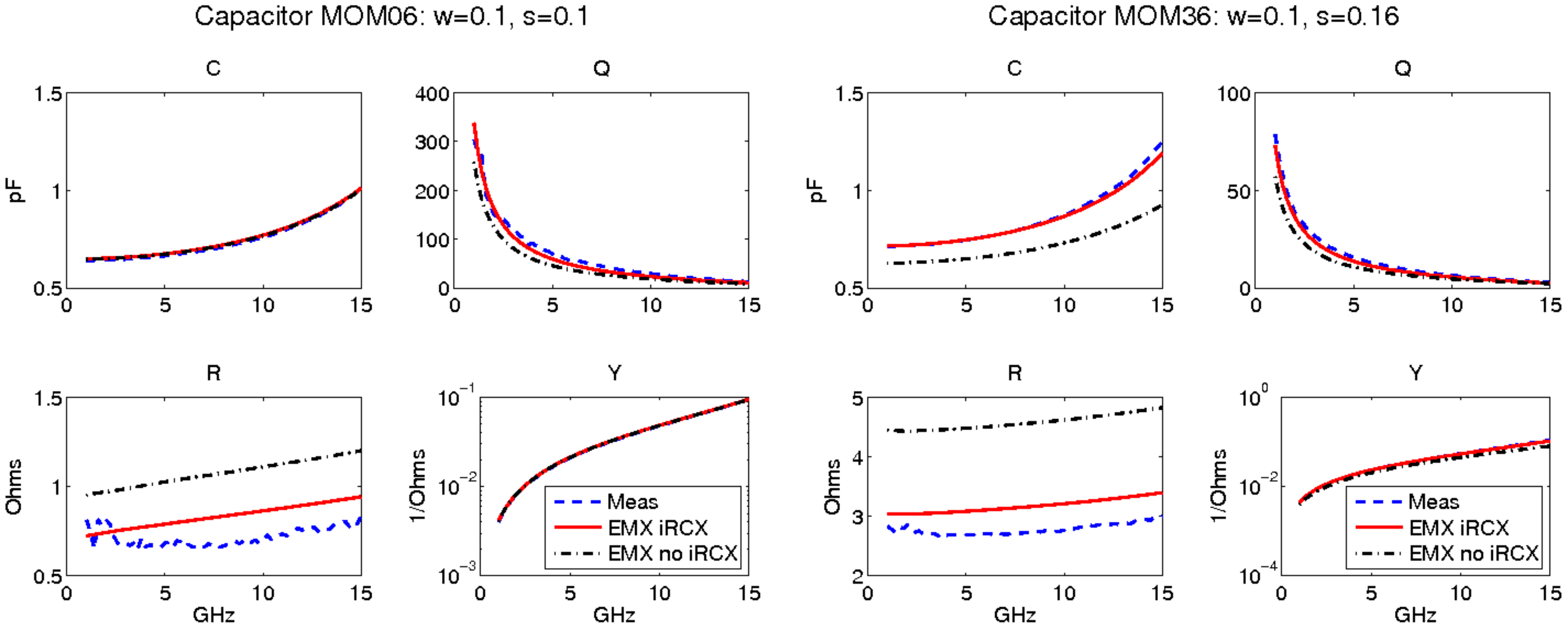


gdsview



EMX 3D Mesh

EMX simulation of MOM capacitors



The iRCX width-and-spacing dependence is more critical for structures that are not at minimum dimensions. The accuracy of EMX using iRCX is increased since the fabrication process is mimicked more closely.

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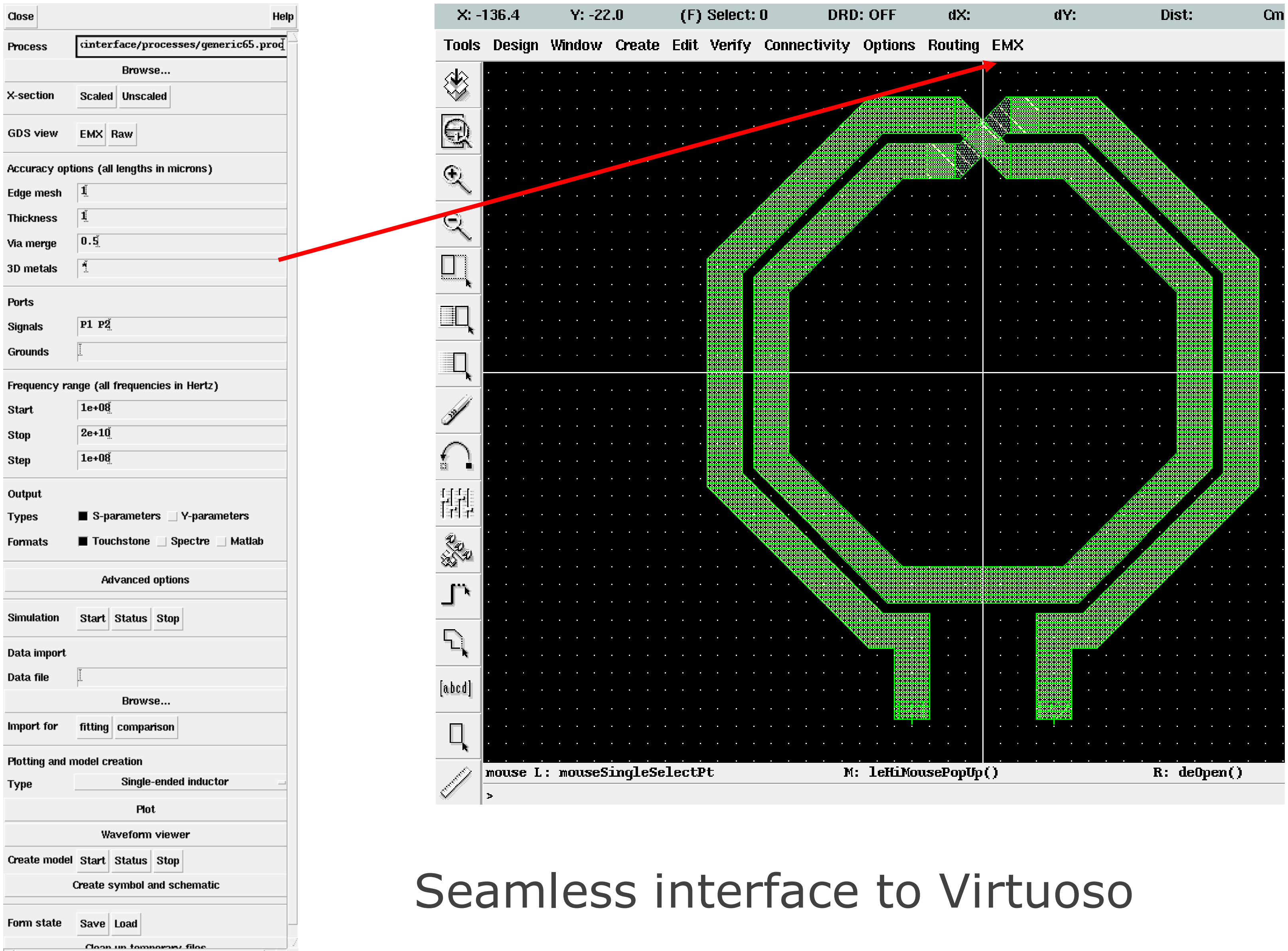
Easy to use: Virtuoso interface



Seamless interface to Virtuoso

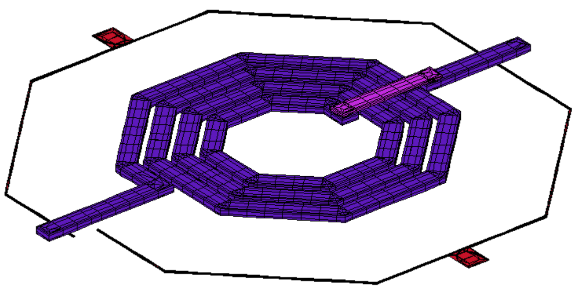
Easy to use: Running EMX using a script

- Some customers use EMX using simple shell scripts or the command line

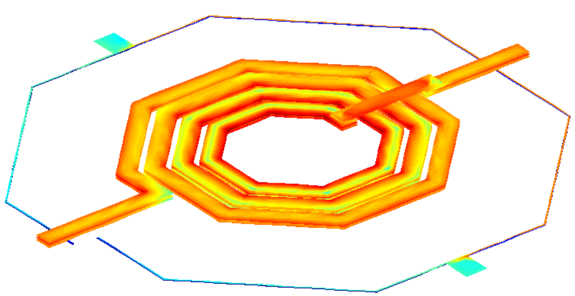
```
gdsfile=testind.gds
process=RC_IRCX_CRN65LP_1P8M+ALRDL_6X1U_typ.proc
freqs="--sweep 2e8 20e9 --sweep-stepsize 2e8"
opts="--verbose=3 -e 1 -t 1 --3d=* -v 0"
emx $gdsfile.gds testind $process.proc --touchstone -s $gdsfile.s2p $opts
```

- Jobs can be submitted in queues to do extensive analysis
- Fast and easy to use

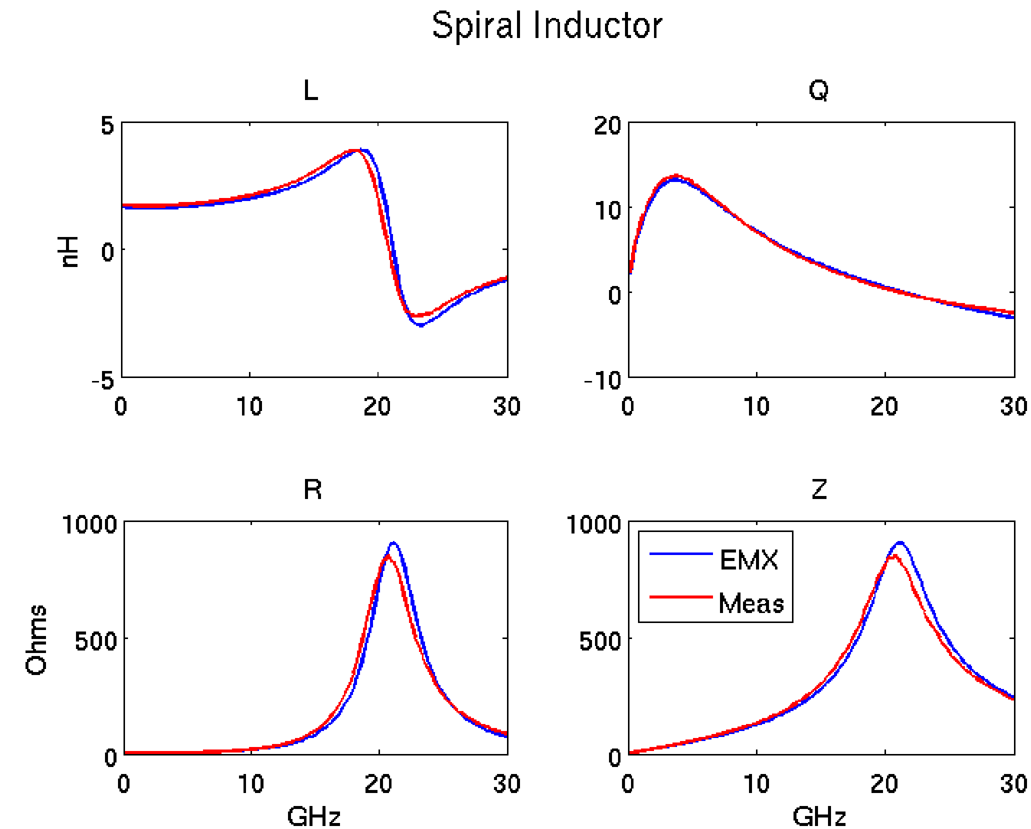
Benchmarks: Spiral Inductor



3D mesh



Current



Example	Ports	Freq Range	Size	1 CPU		8 CPUs	
				Mem.	Time	Mem.	Time
Planar Inductor	2	0.2GHz-30GHz	13,181	193MB	3m29s	**790MB**	**1m48s**

Courtesy: TSMC. 65nm RFCMOS, 9LM thick metal technology. Published at RFIC 2009

"Including Pattern-Dependent Effects in Electromagnetic Simulations of On-Chip Passive Components", Integrand and TSMC

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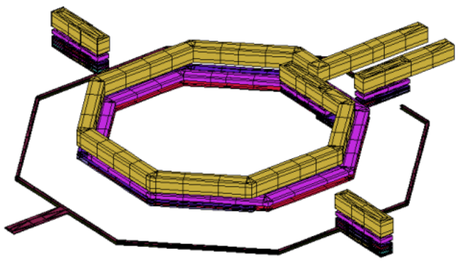
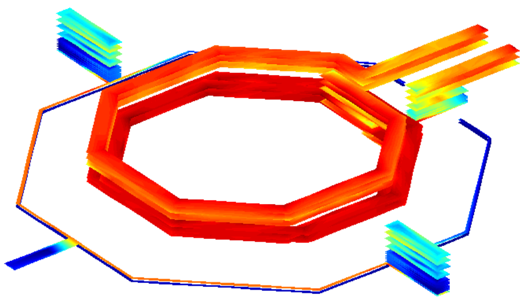
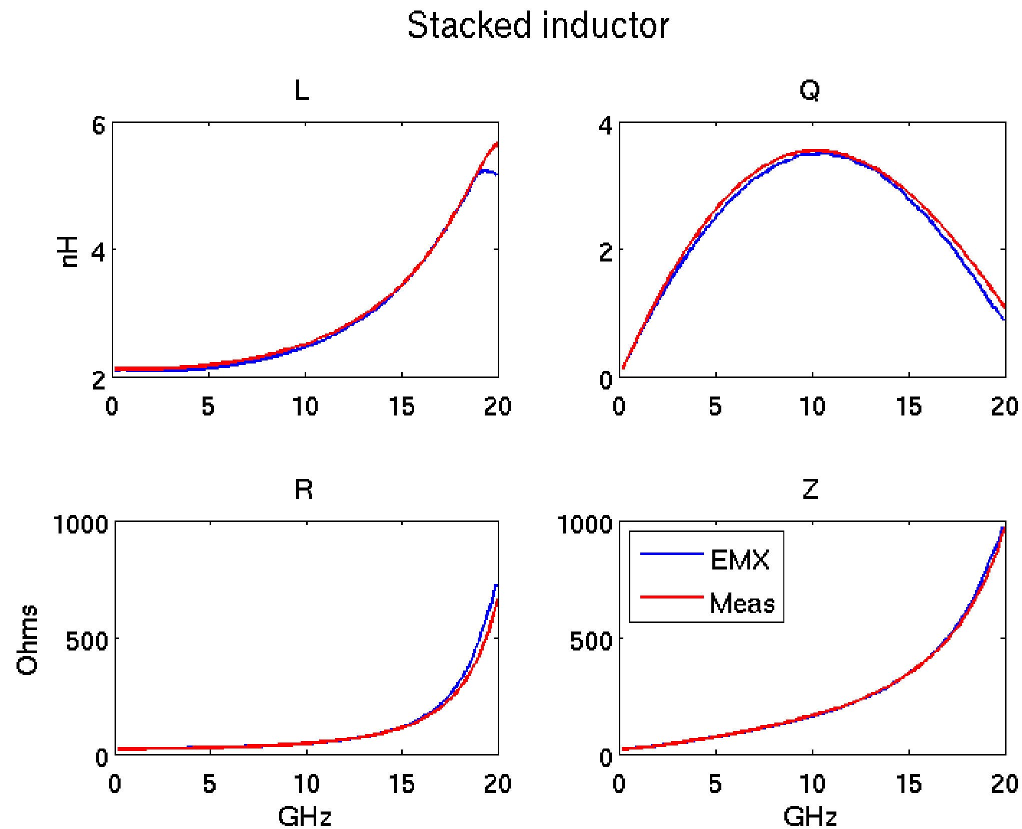
Stacked Inductor



3D mesh



Current



Example	Ports	Freq Range	Size	1 CPU		8 CPUs	
				Mem.	Time	Mem.	Time
Stacked Inductor	2	0.2GHz-20GHz	10,407	453MB	6m58s	**688MB**	**4m42s**

Courtesy: TSMC. 65nm RFCMOS, 9LM thick metal technology. Published at RFIC 2009
"Including Pattern-Dependent Effects in Electromagnetic Simulations of On-Chip Passive Components", Integrand and TSMC

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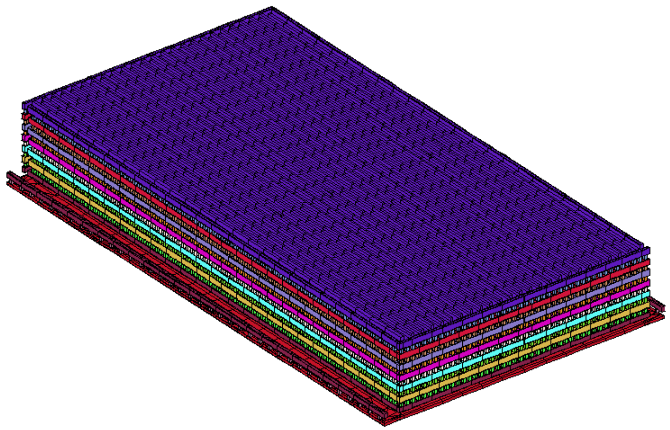
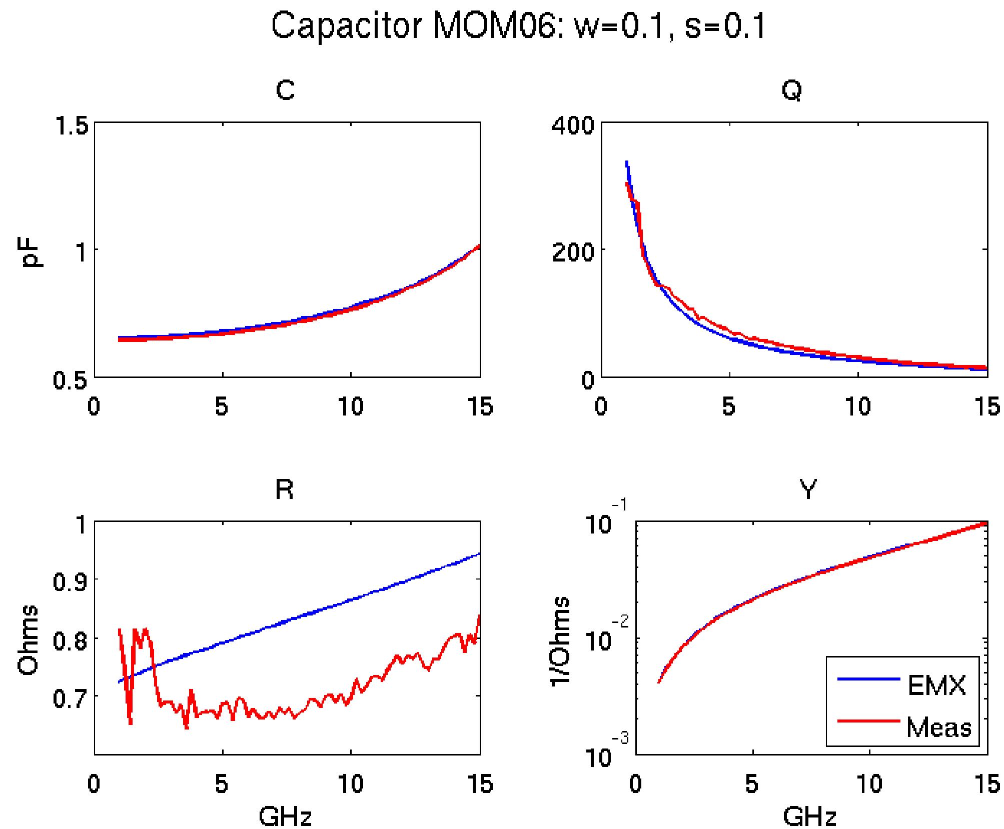
MOM (finger)Capacitor



3D mesh of 0.6pF Cap

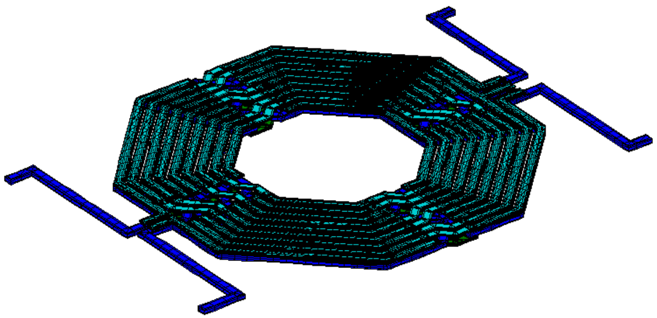


Example	Ports	Freq Range	Size	1 CPU		8 CPUs	
				Mem.	Time	Mem.	Time
MoM capacitor	2	0.2GHz-20GHz	48,997	1140MB	19m12s	**2591MB**	**5m59s**

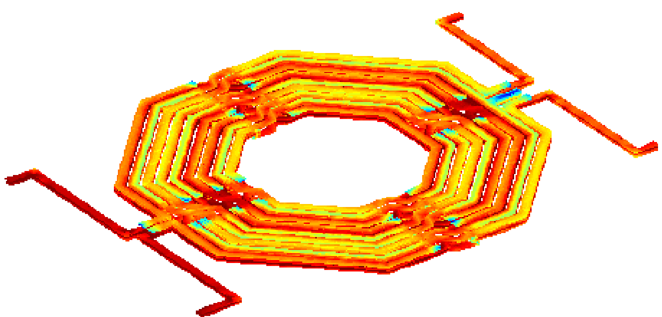
Courtesy: TSMC. 65nm RFCMOS, 9LM thick metal technology. Published at RFIC 2009

"Including Pattern-Dependent Effects in Electromagnetic Simulations of On-Chip Passive Components", Integrand and TSMC

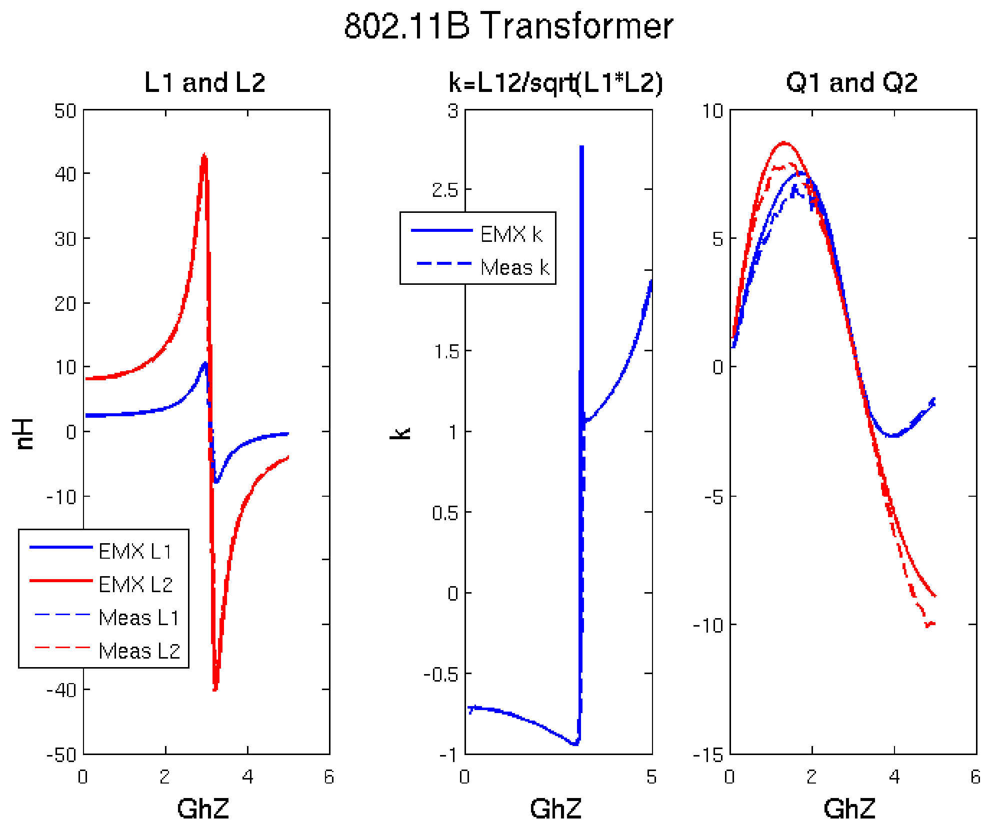
Transformer



3D mesh



Current

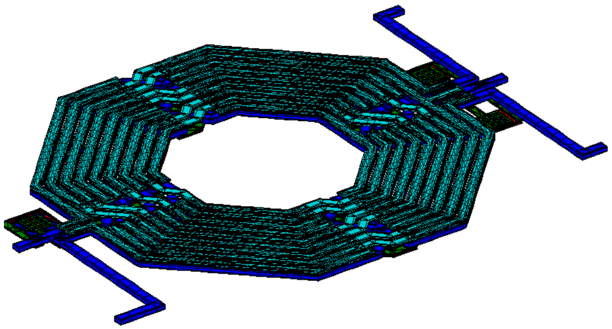


Example	Ports	Freq Range	Size	1 CPU		8 CPUs	
				Mem.	Time	Mem.	Time
Transformer	4	0.1GHz-10GHz	81,405	1234MB	28m48s	**2016MB**	**6m01s**

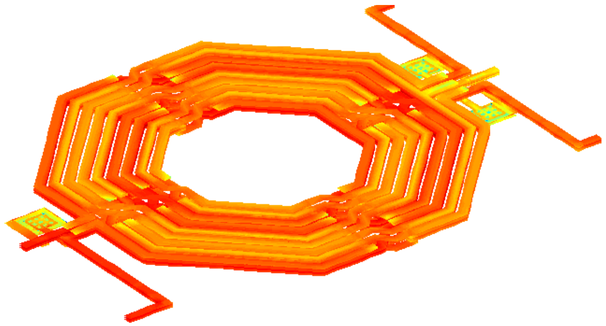
Courtesy: UMC. 90nm RFCMOS, 8LM thick metal technology. Published at CICC 2007

"Synthesis of Optimal On-Chip Baluns", Integrand and UMC

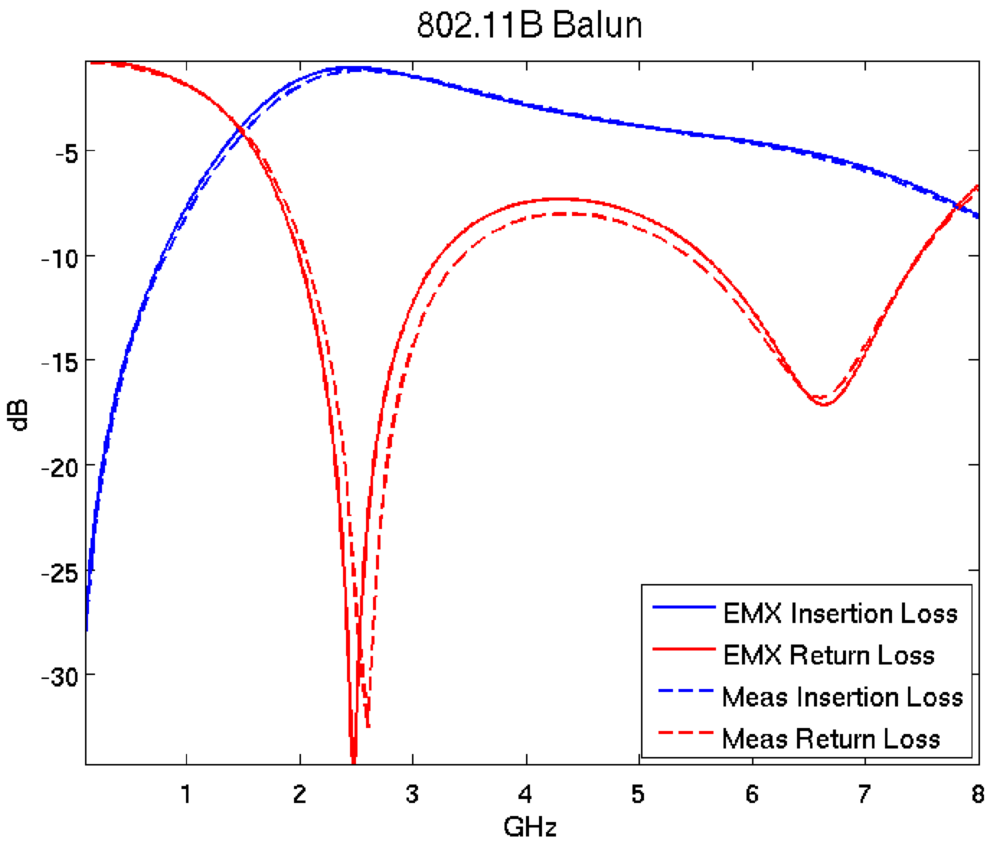
Balun (with MiM caps)



3D mesh



Current

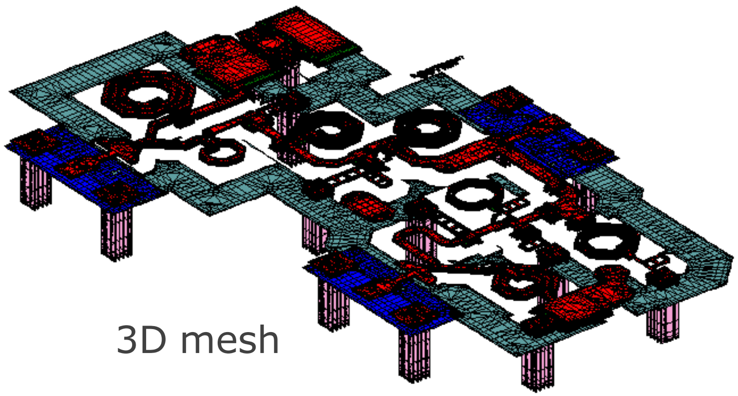


Example	Ports	Freq Range	Size	1 CPU		8 CPUs	
				Mem.	Time	Mem.	Time
Balun	5	0.1GHz-10GHz	89,174	1449MB	38m48s	**2584MB**	**8m43s**

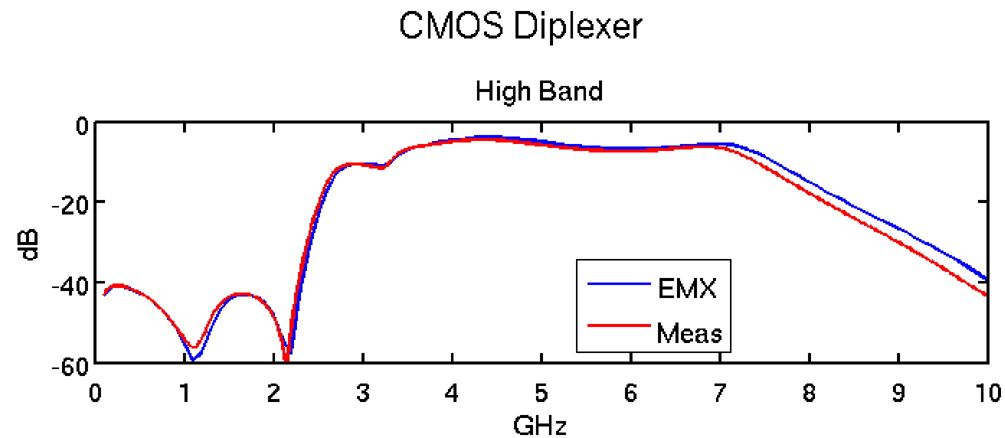
Courtesy: UMC. 90nm RFCMOS, 8LM thick metal technology. Published at CICC 2007
"Synthesis of Optimal On-Chip Baluns", Integrand and UMC

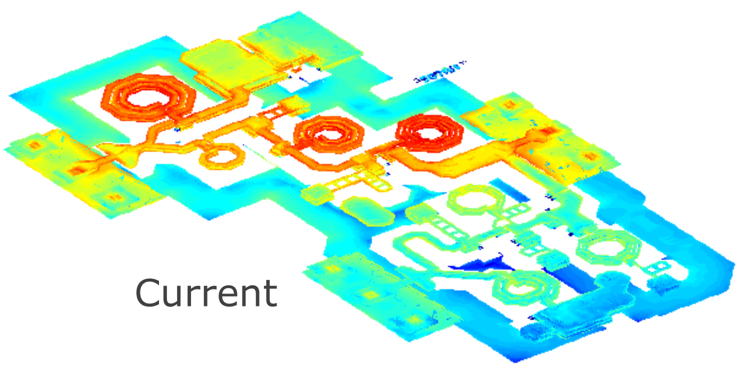
Integrand Software, Inc.

BiCMOS Diplexer (with Thru Silicon Vias)

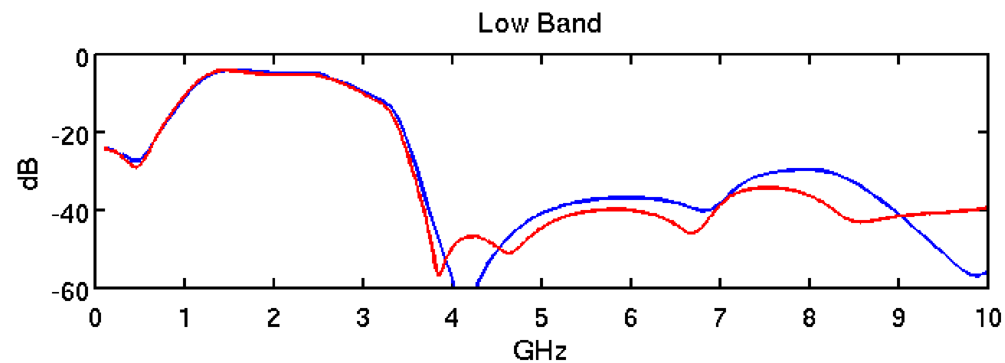


3D mesh





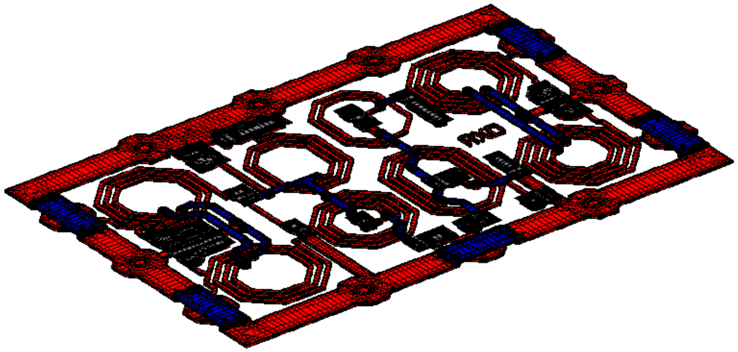
Current



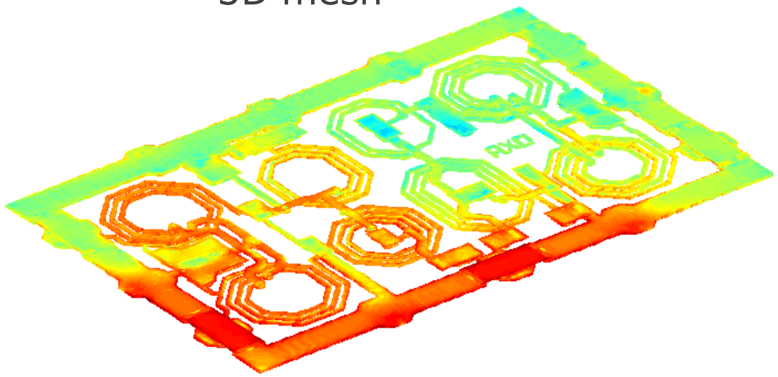
Example	Ports	Freq Range	Size	1 CPU		8 CPUs	
				Mem.	Time	Mem.	Time
CMOS Diplexer	3	0.1GHz-10GHz	195,009	4778MB	374m18s	**8062MB**	**65m41s**

Courtesy: Skyworks. IBM BiCMOS 5PAE.
Published at CICC 2010, 2010

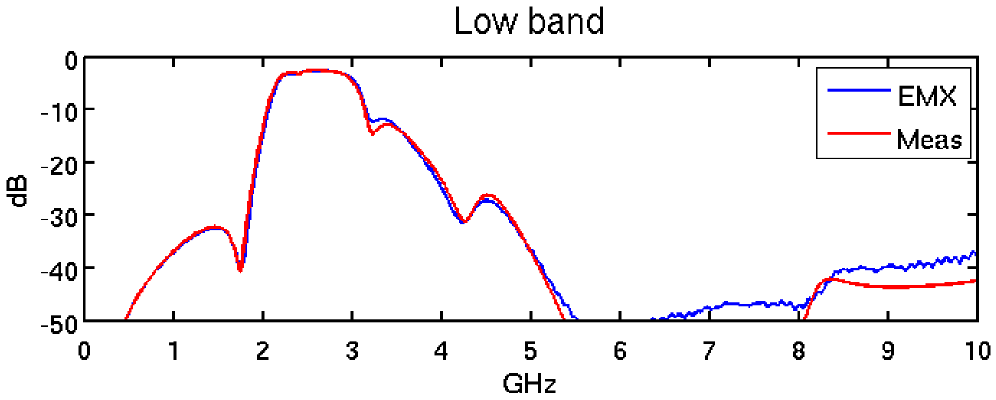
IPD Diplexer

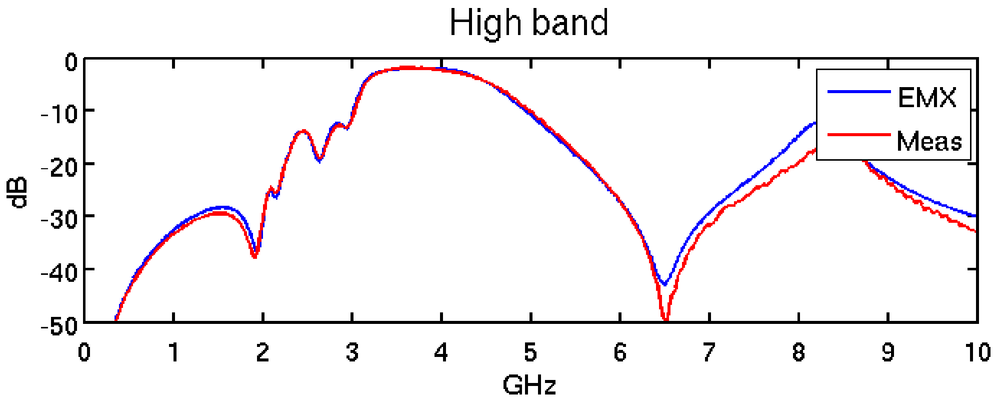


3D mesh



Current





Example	Ports	Freq Range	Size	1 CPU		8 CPUs	
				Mem.	Time	Mem.	Time
IPD Diplexer	12	0.1GHz-10GHz	238,849	1932MB	414m21s	**5449MB**	**89m18s**

Courtesy: STATSChipPAC, IPD technology (8um Cu on high resistivity Si substrate)

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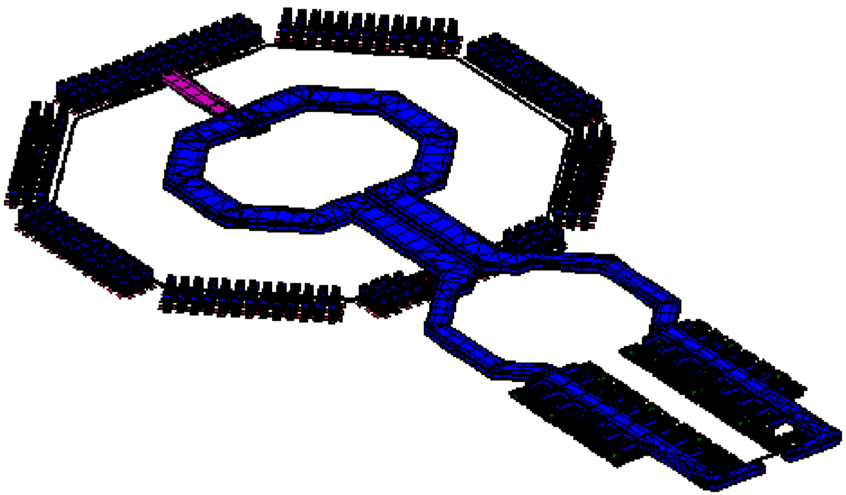
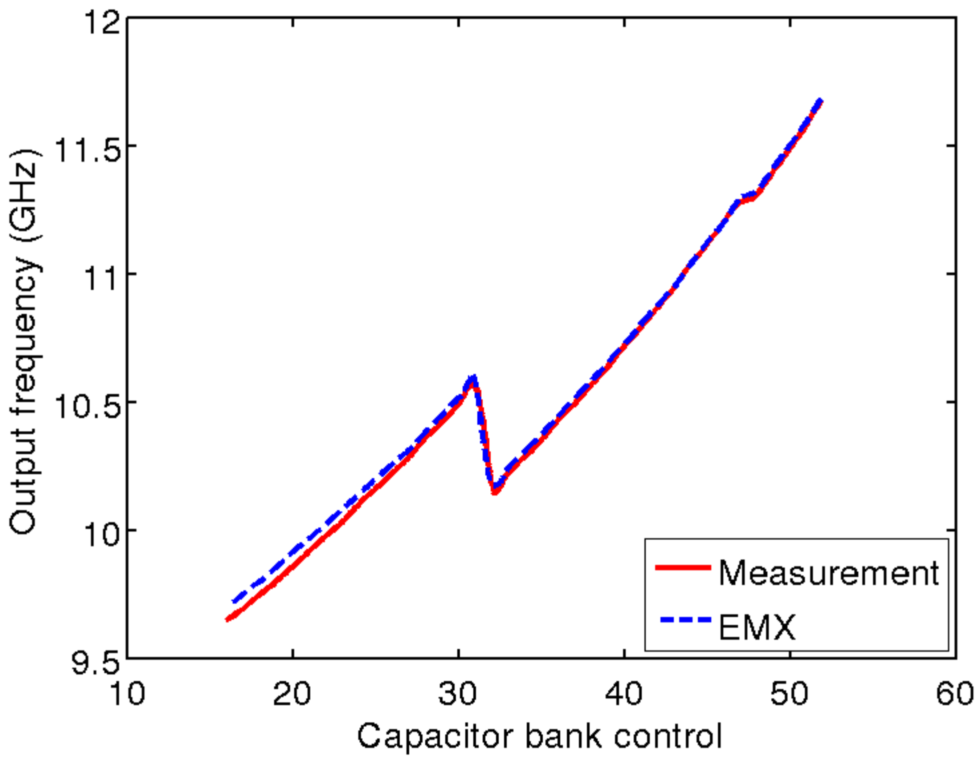
CMOS VCO



3D mesh (inductor+ capacitor bank)



Example	Ports	Freq Range	Size	1 CPU		8 CPUs	
				Mem.	Time	Mem.	Time
CMOS VCO	20	0.1GHz-20GHz	137,694	5216MB	399m41s	**18878MB**	**98m19s**

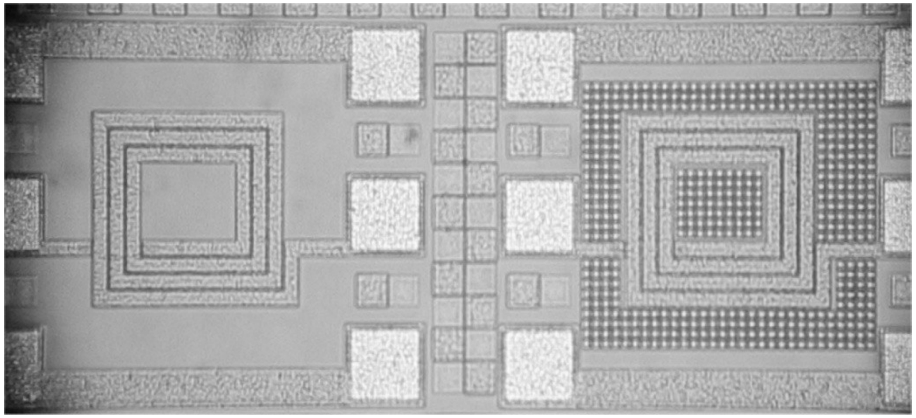
Courtesy: Wipro, TSMC90nm, 1P5M

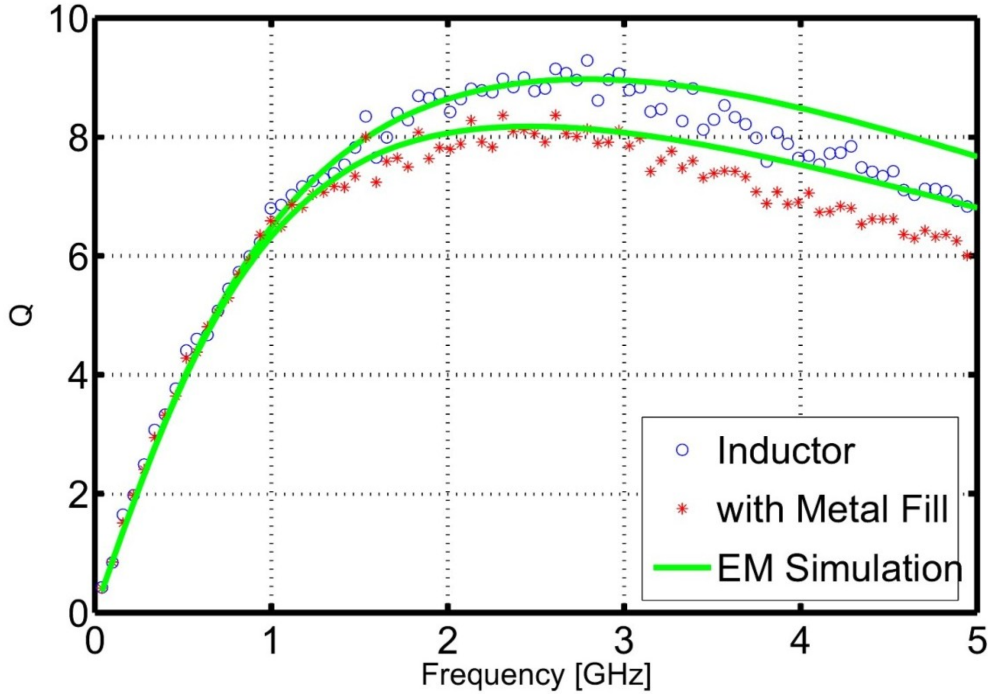
Benchmark Summary

Example	Ports	Freq Range	Size	1 CPU		8 CPUs	
				Mem.	Time	Mem.	Time
Planar Inductor	2	0.2GHz-30GHz	13,181	193MB	3m29s	**790MB**	**1m48s**
Stacked Inductor	2	0.2GHz-20GHz	10,407	453MB	6m58s	**688MB**	**4m42s**
MoM capacitor	2	0.2GHz-20GHz	48,997	1140MB	19m12s	**2591MB**	**5m59s**
Transformer	4	0.1GHz-10GHz	81,405	1234MB	28m48s	**2016MB**	**6m01s**
Balun	5	0.1GHz-10GHz	89,174	1449MB	38m48s	**2584MB**	**8m43s**
CMOS Diplexer	3	0.1GHz-10GHz	195,009	4778MB	374m18s	**8062MB**	**65m41s**
IPD Diplexer	12	0.1GHz-10GHz	238,849	1932MB	414m21s	**5449MB**	**89m18s**
CMOS VCO	20	0.1GHz-20GHz	137,694	5216MB	399m41s	**18878MB**	**98m19s**

- The new multi-threaded EMX is 2-3X faster for small examples and 5-6X faster for larger examples on an 8 CPU machine.
- The memory for the multi-threaded version goes up at a slower rate than the speedup.

Metal Fill

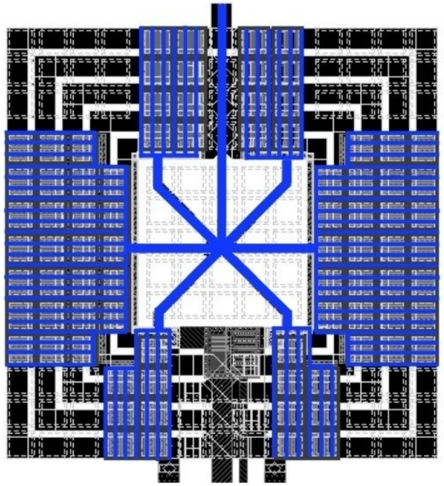




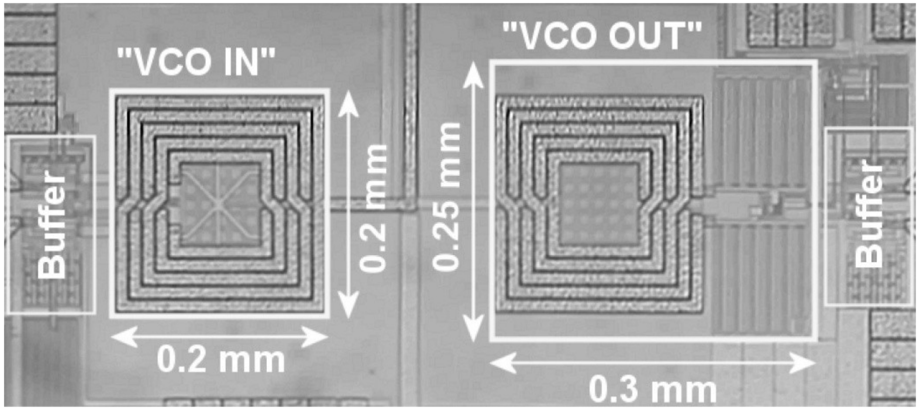
The effect of Metal Fill inside inductor was studied using EMX by Columbia University. (CICC 2005)

VCO in Coil

Inductor with Varactor/MOM Capacitor acting as a substrate shield

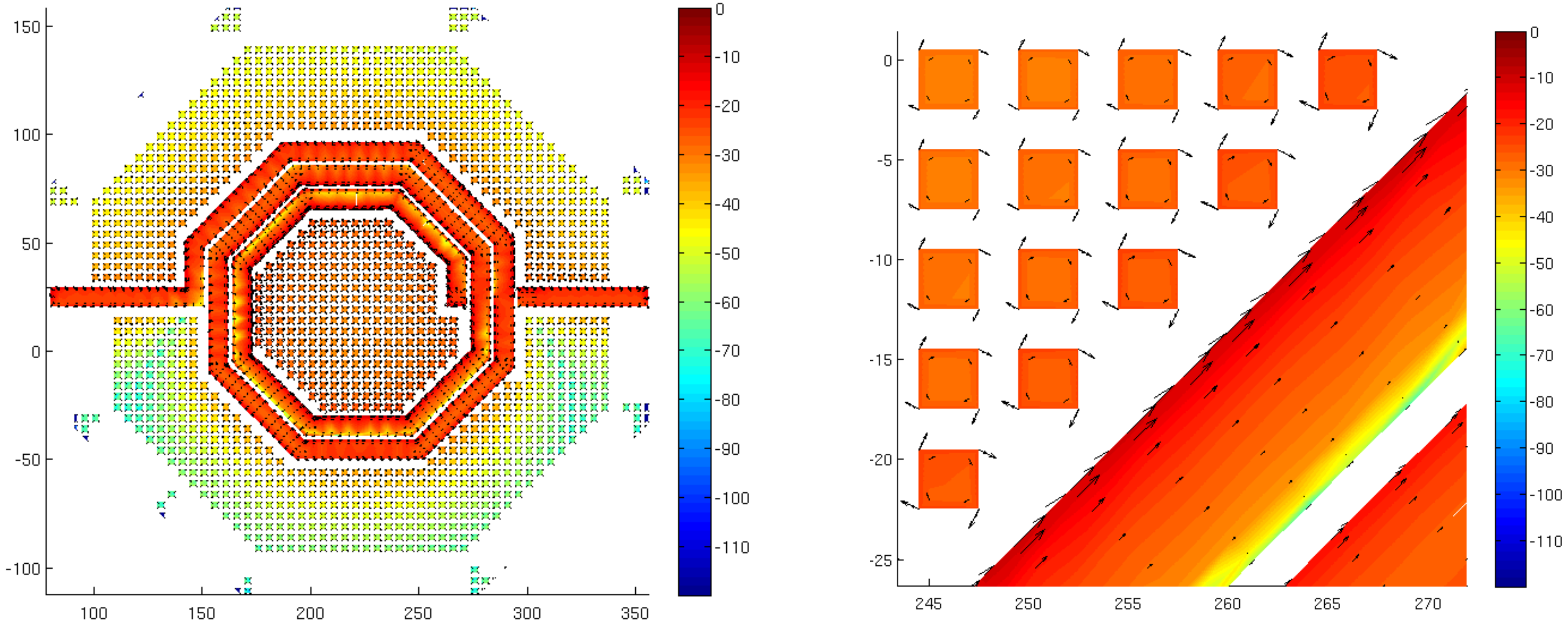


- Equal performance in phase noise and output power as compared to a traditional VCO while **reducing design area by 47%.**



(Columbia University, CICC 2005)

Dummy fill simulation

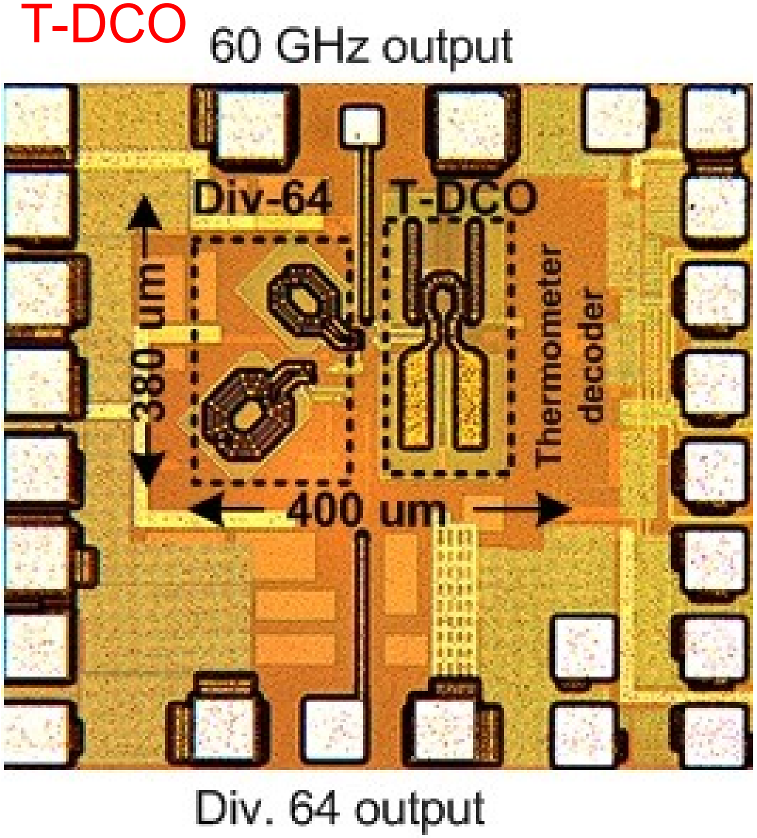


EMX used to model circulating currents in dummy fill

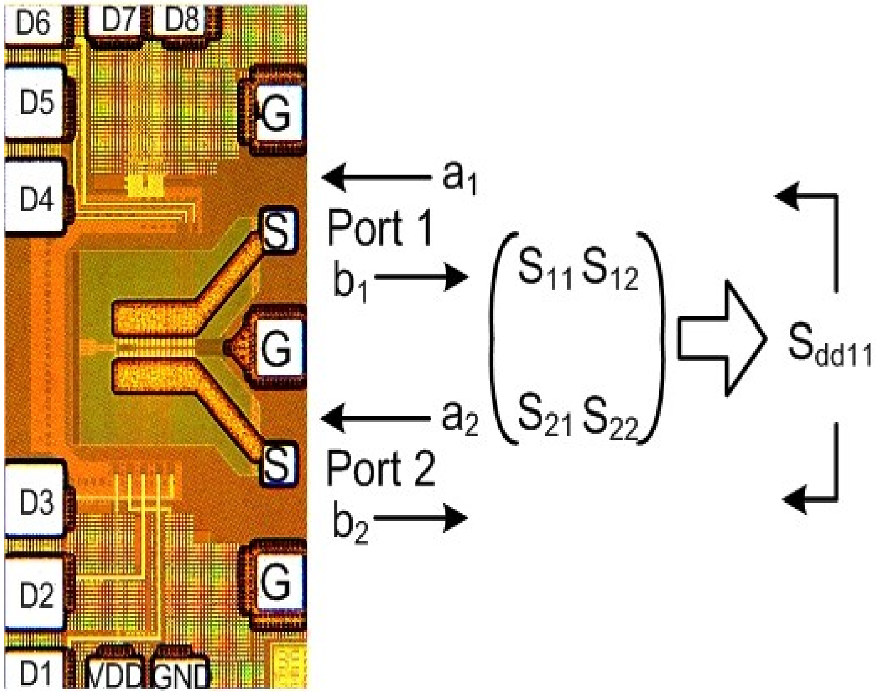
60-GHz DCO Test Chips

[published at RFIC 2012/ ISSCC 2013]: TU Delft, J.R. Long's group

T-DCO

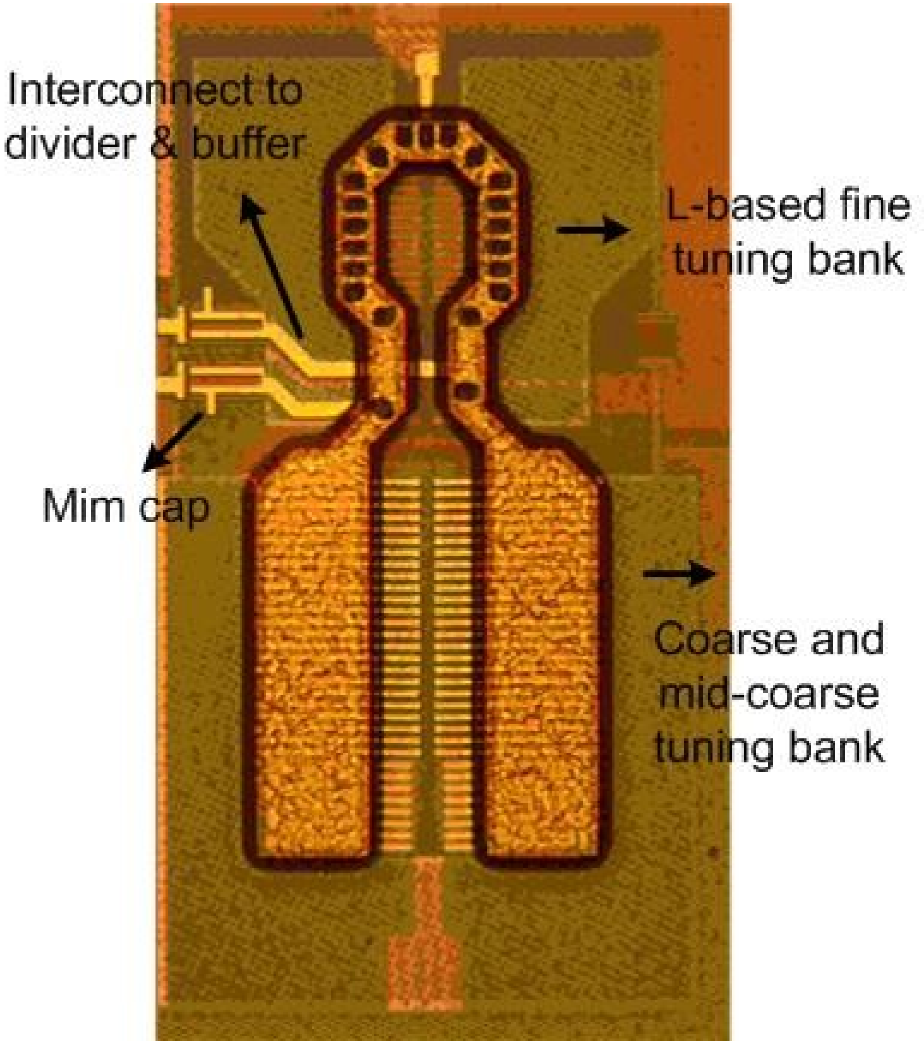


Transmission line testchip



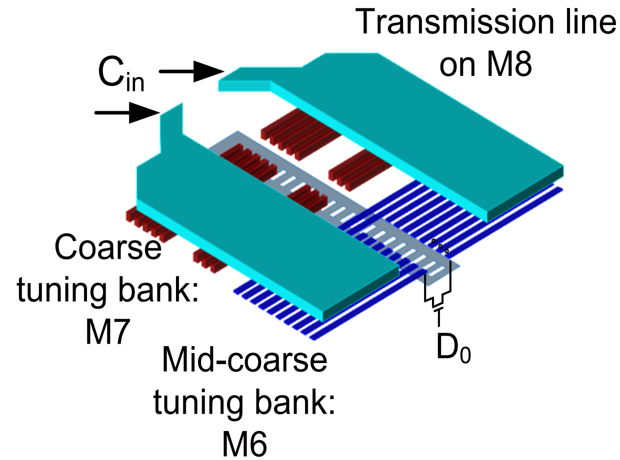
Complete L-DCO tank EM simulation

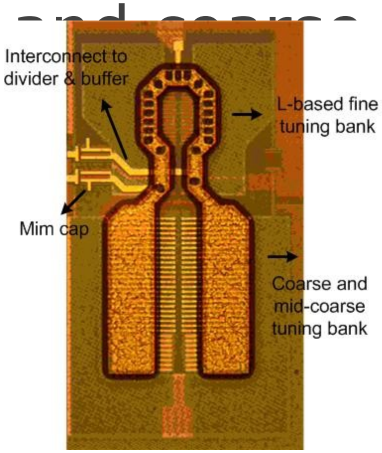
- Including:
  - Coarse, mid-coarse tuning bank
  - Fine tuning bank
  - Interconnection to divider and buffer
  - Mimcap for AC coupling
  - Ground ring
- 100+ port EMX simulation

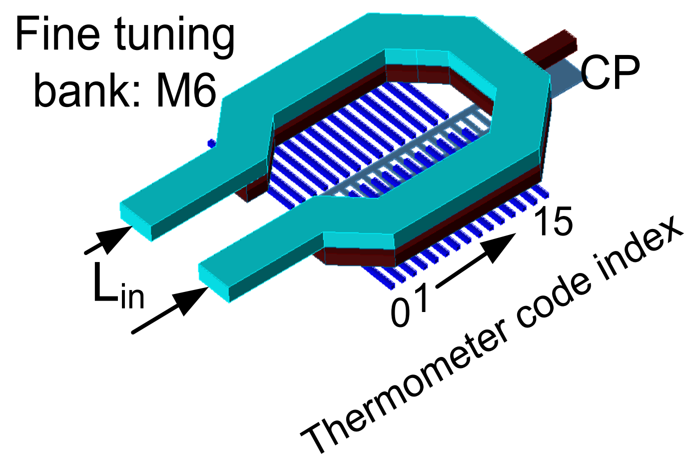


T-line and inductor tuning

- Passive structures with tuned by capacitive loading
  - Transmission line with fine … cap
  - … th … s

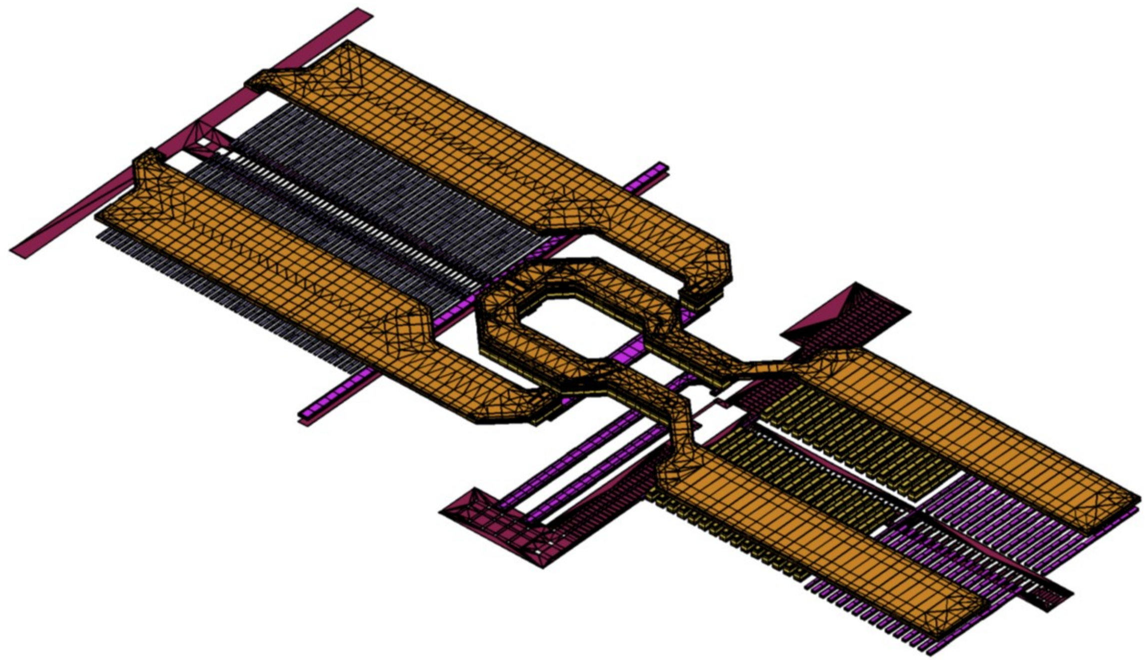






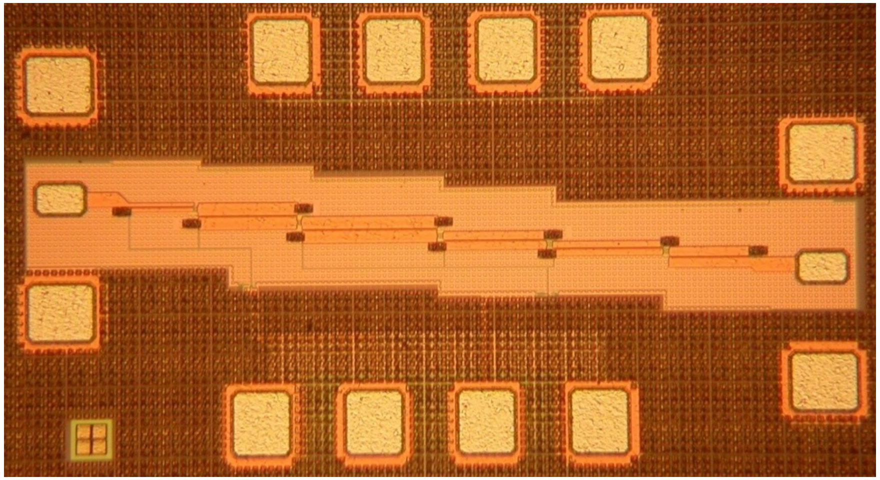
Full DCO tank simulation in EMX

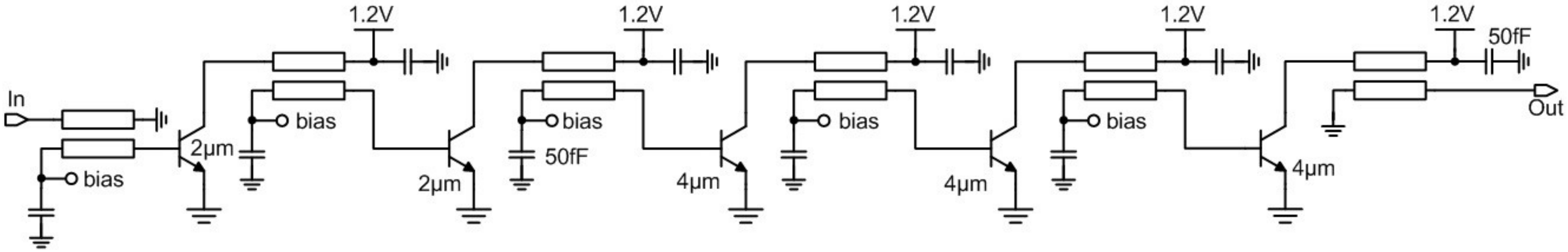
- EMX simulation of 60GHz DCO
  - TL-based coarse and mid-coarse tuning bank, transformer based interconnect, ground plane
  - Ports: 175
  - Layout size 400x200μm^2
  - Computational resources
    - 3GB memory
    - 8 CPU (2.2GHz)
    - 3 hours of sim time



180GHz Amplifier

- D-band amplifier
- 6dB coupler
- 180GHz H2O attenuation window
- Atmosphere monitoring



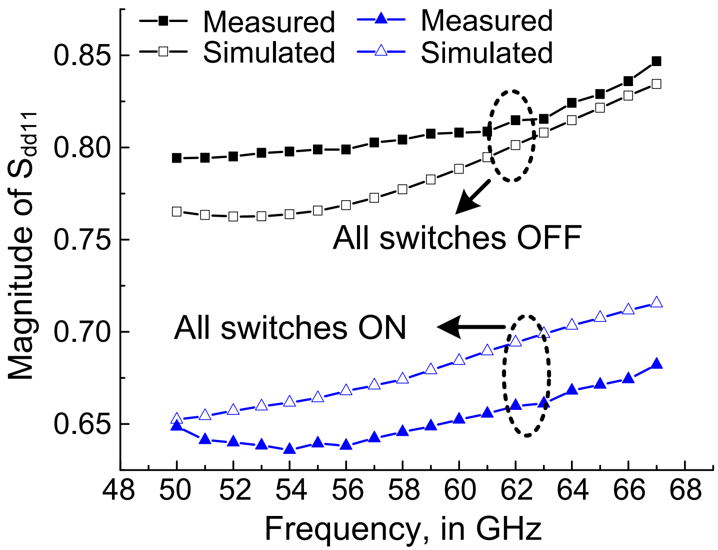


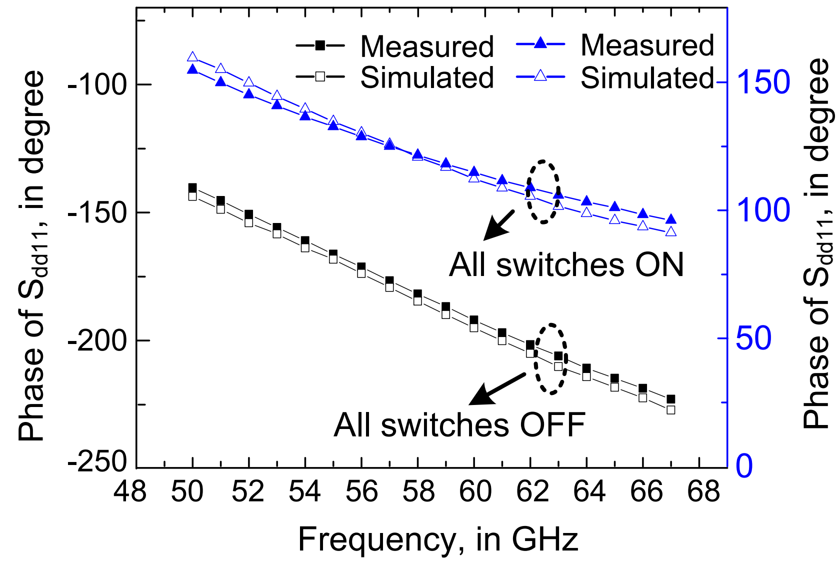
University of Toronto

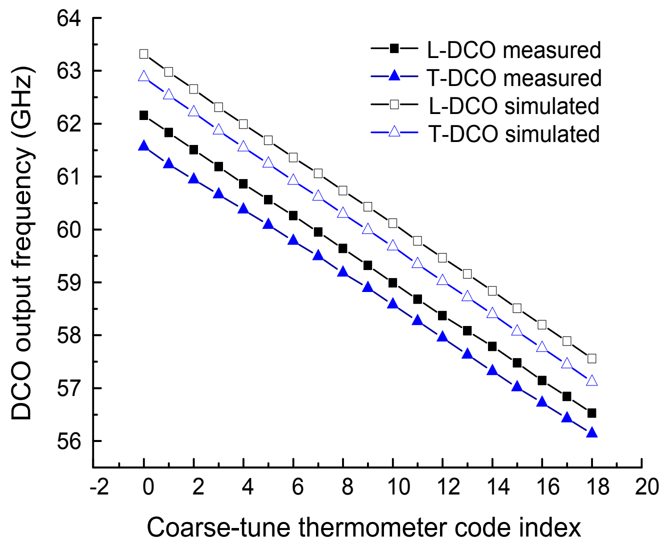
IMS 2012 (private communicati

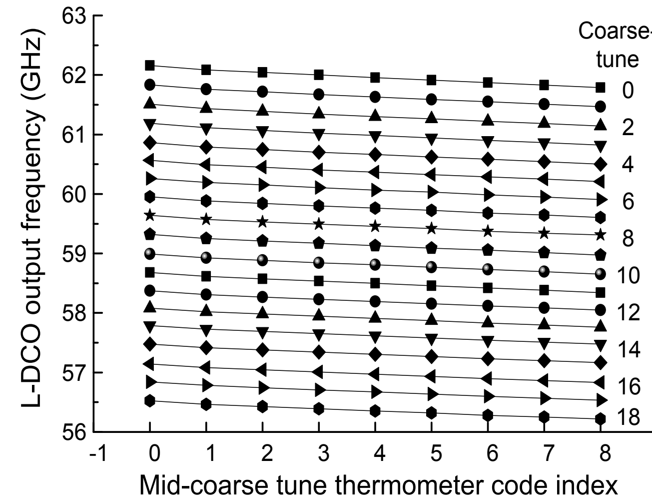
Ionnis Sarkas, Sorin Voinigescu

Measured results









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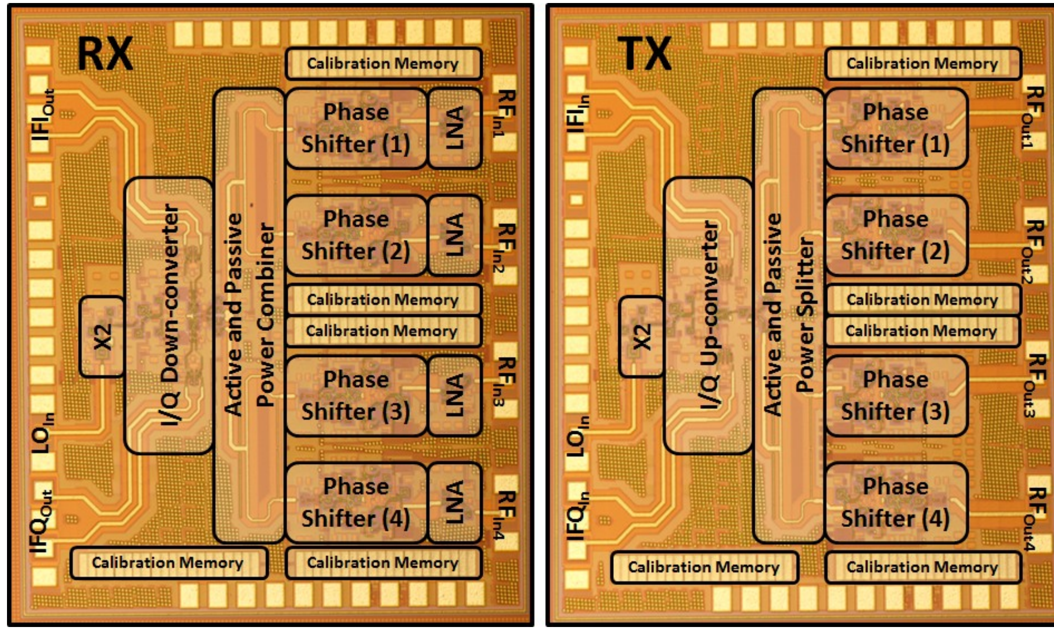
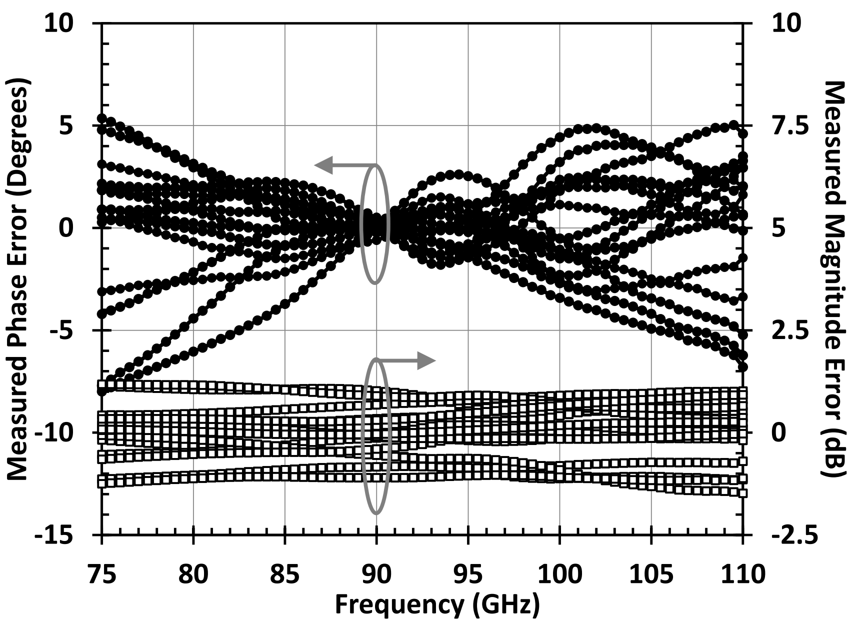
W-band chip

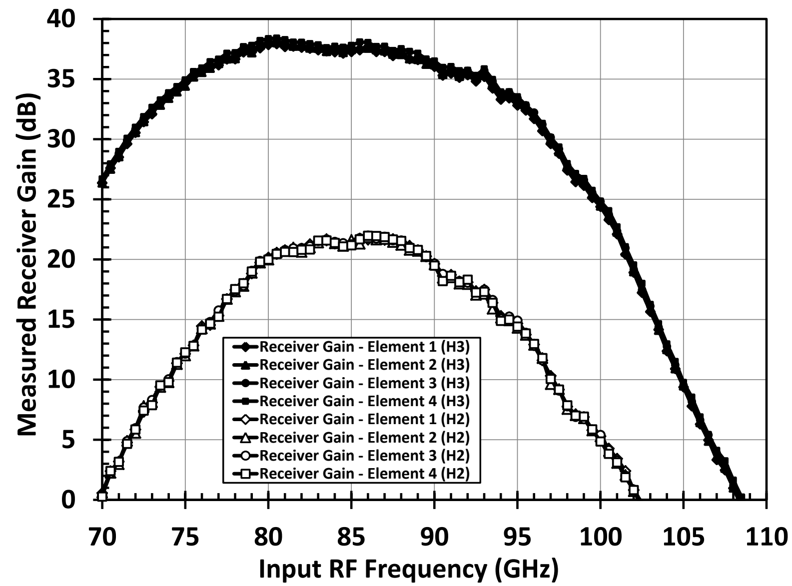
- All passive traces modeled with EMX
- Wilkinson Divider
- Transformer Hybrid architecture
- MM wave passive circuits. Not easy to construct a discrete component equivalent
- Need full S-parameter EM simulation
- All simulations in the 70GHz to 200GHz range

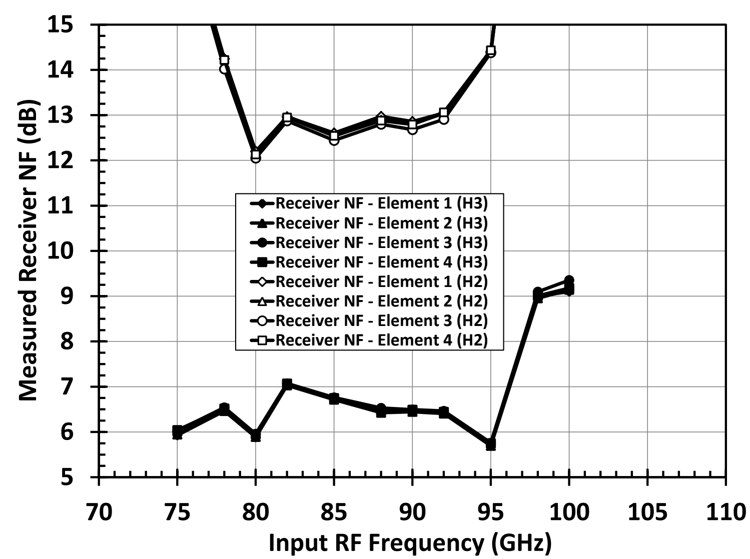


Measured results



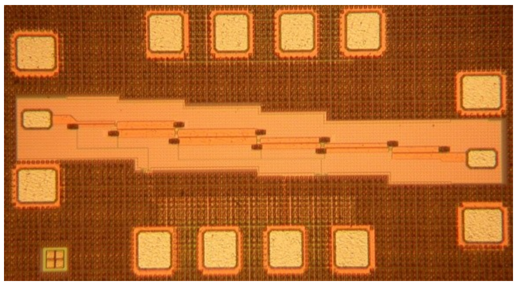
Single Slice Phase/Mag Accuracy

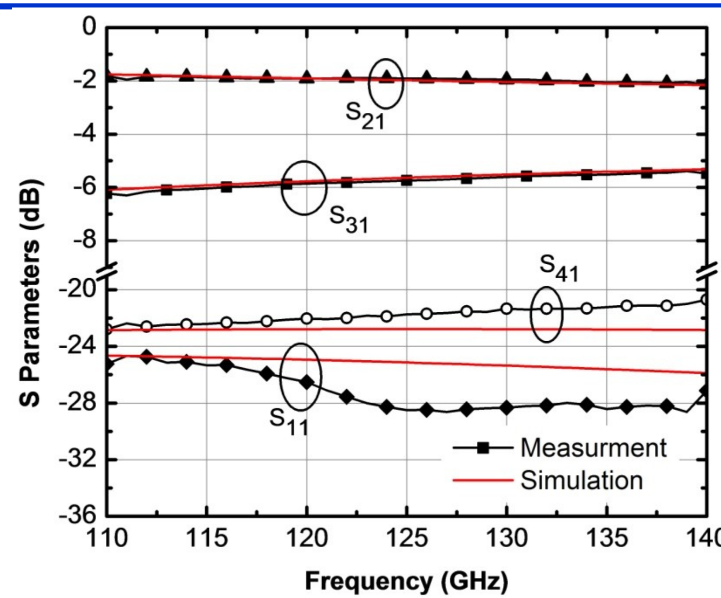


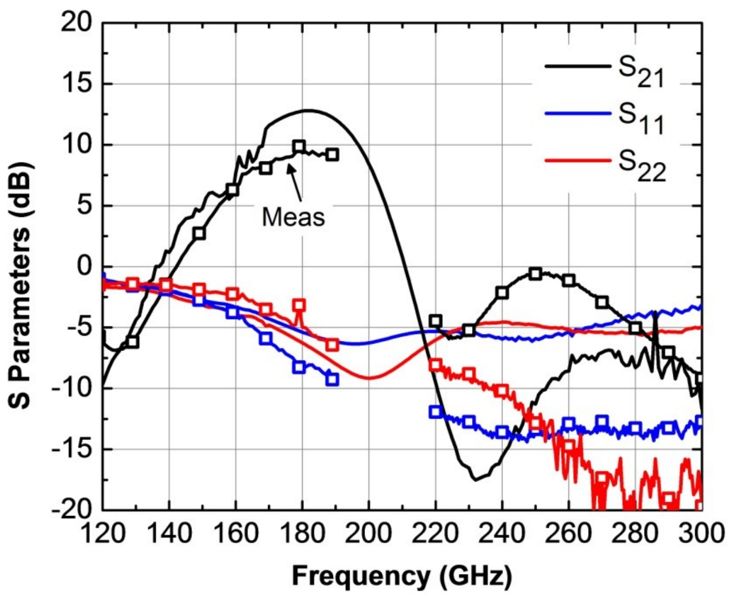


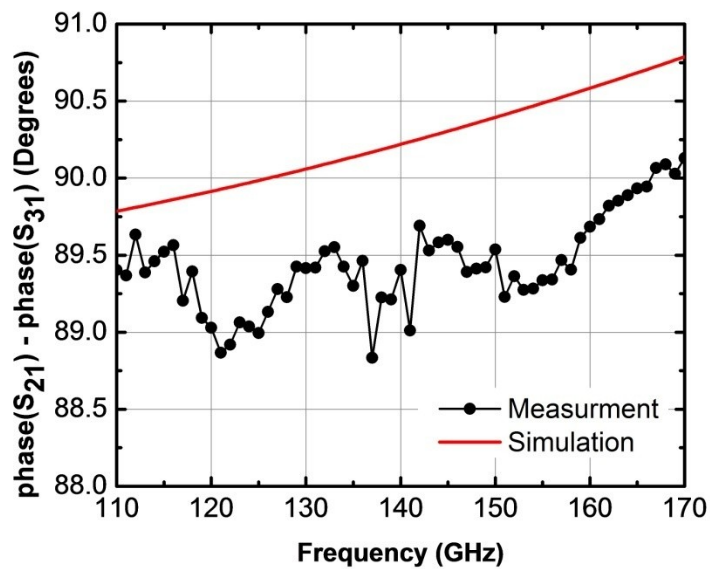
6dB coupler and amplifier

- S-parameter measurements of 6dB coupler up to 180GHz









EMX interface to Virtuoso

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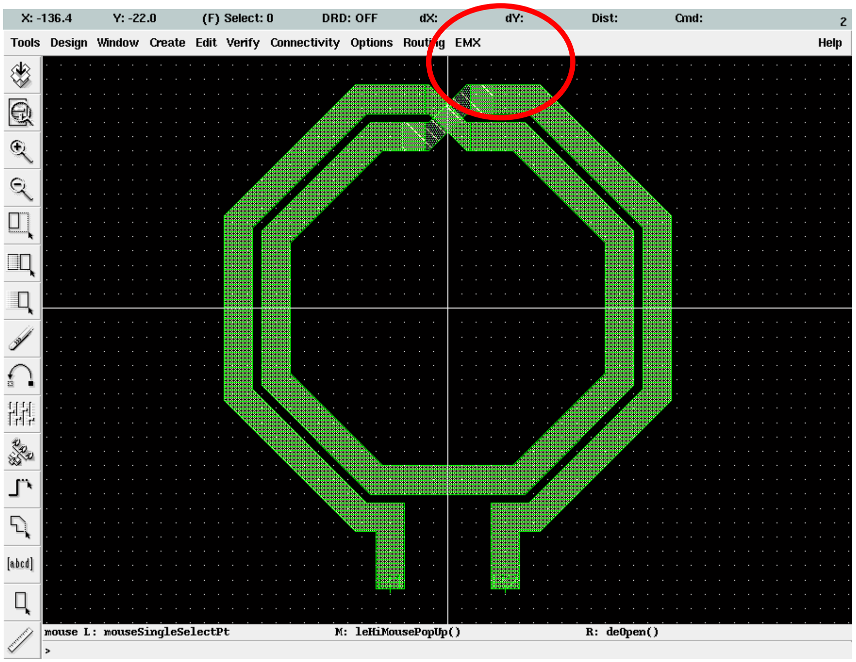
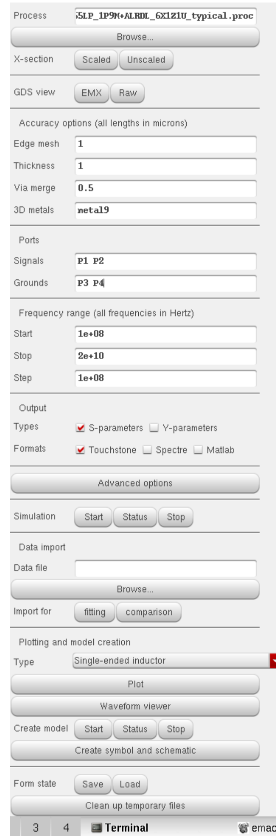
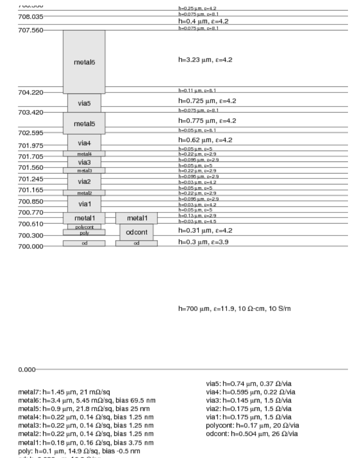
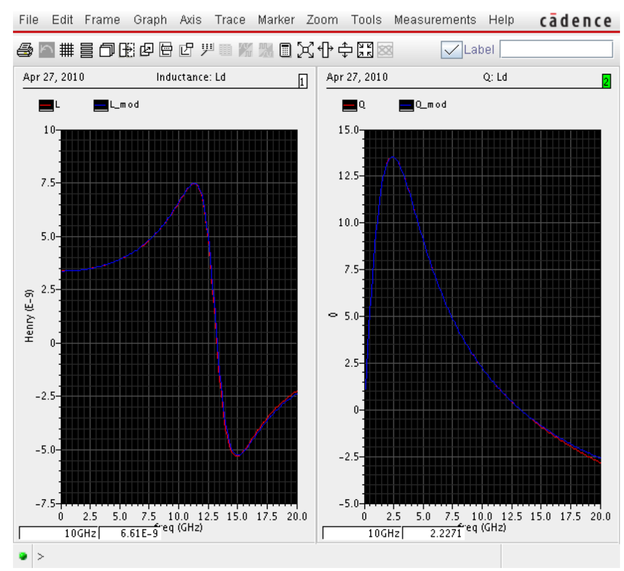




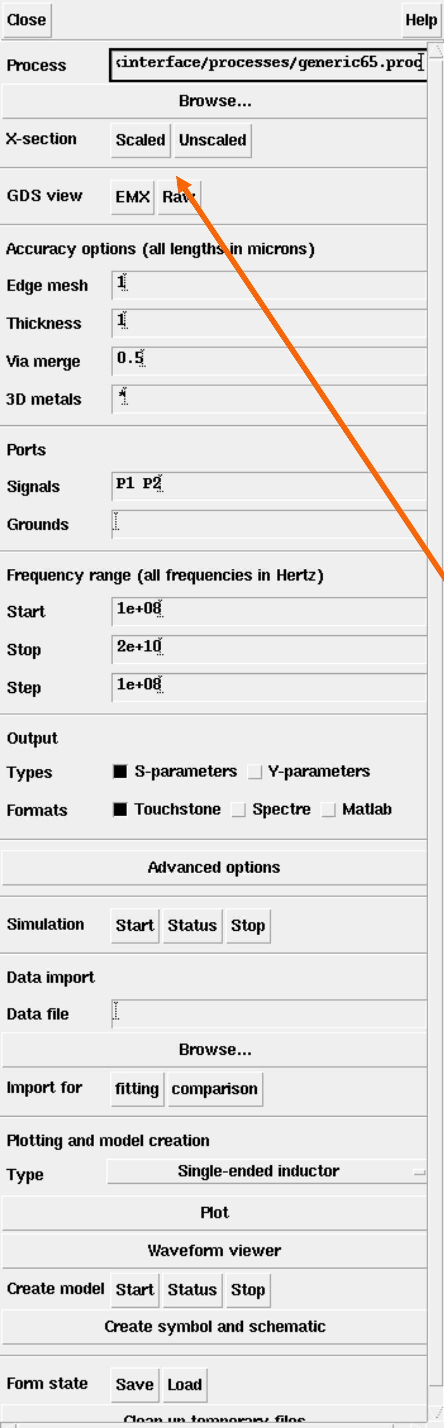


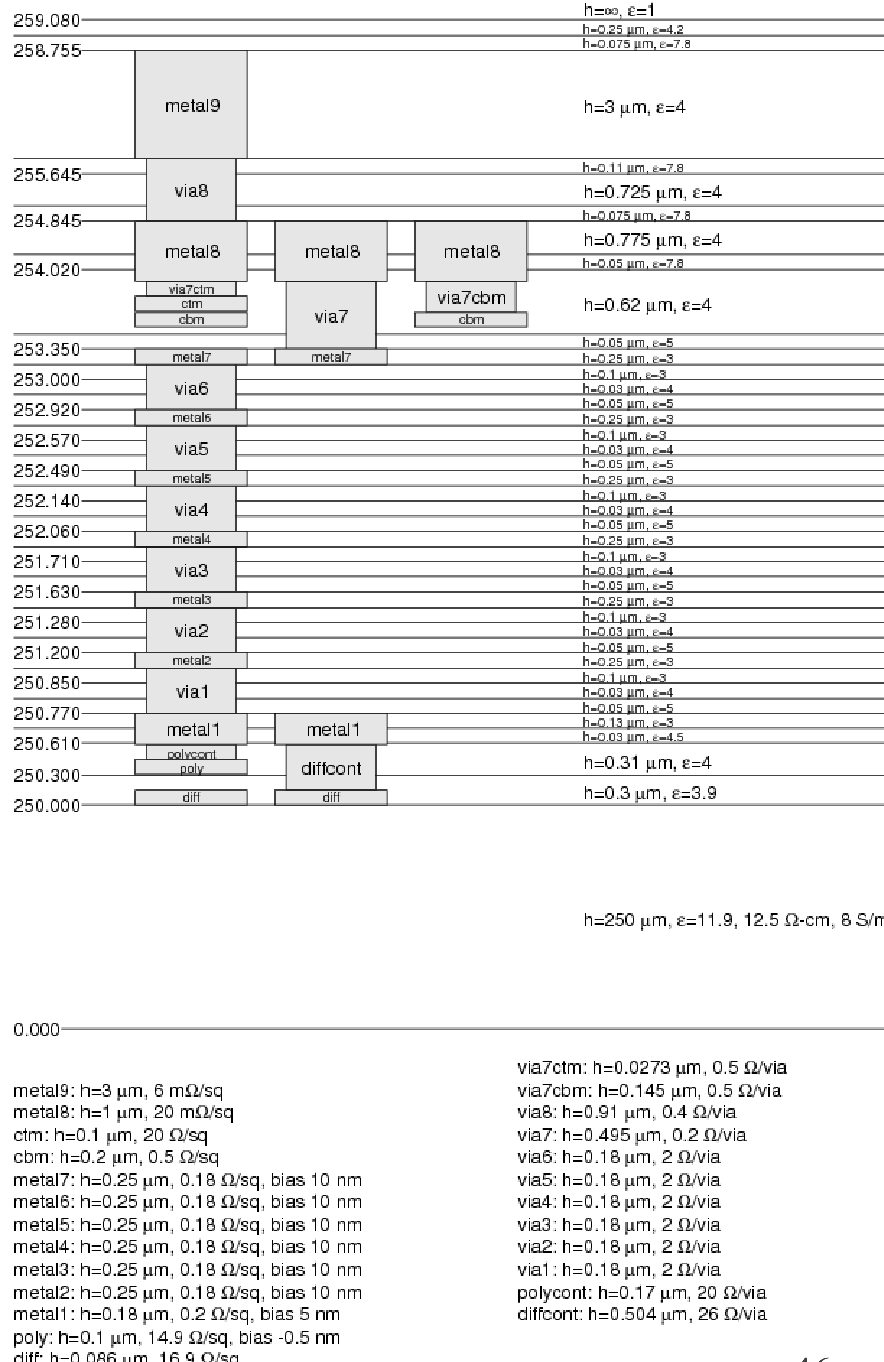
process file



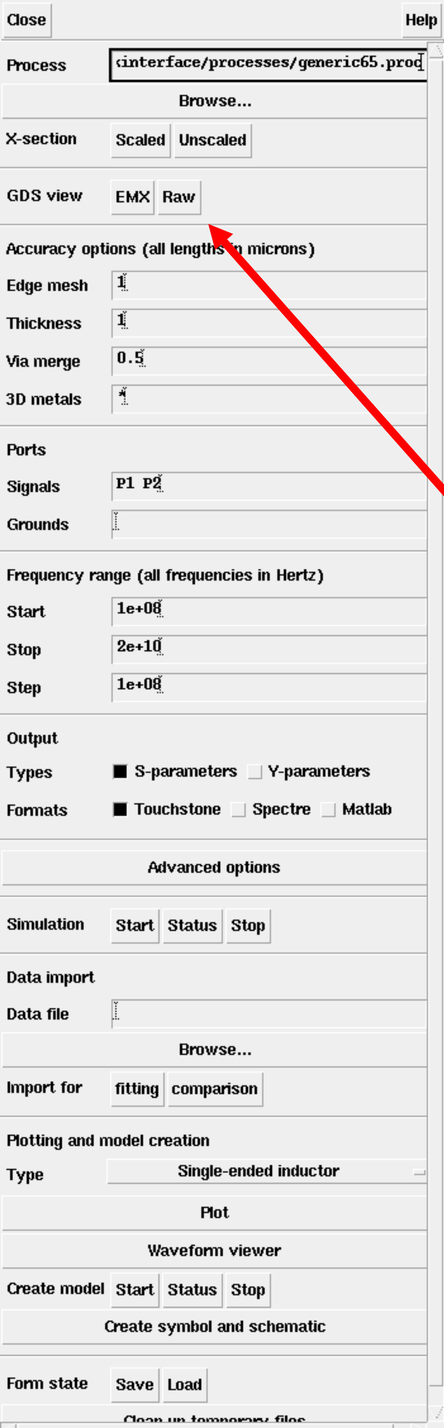
From layout to Spice model in seconds

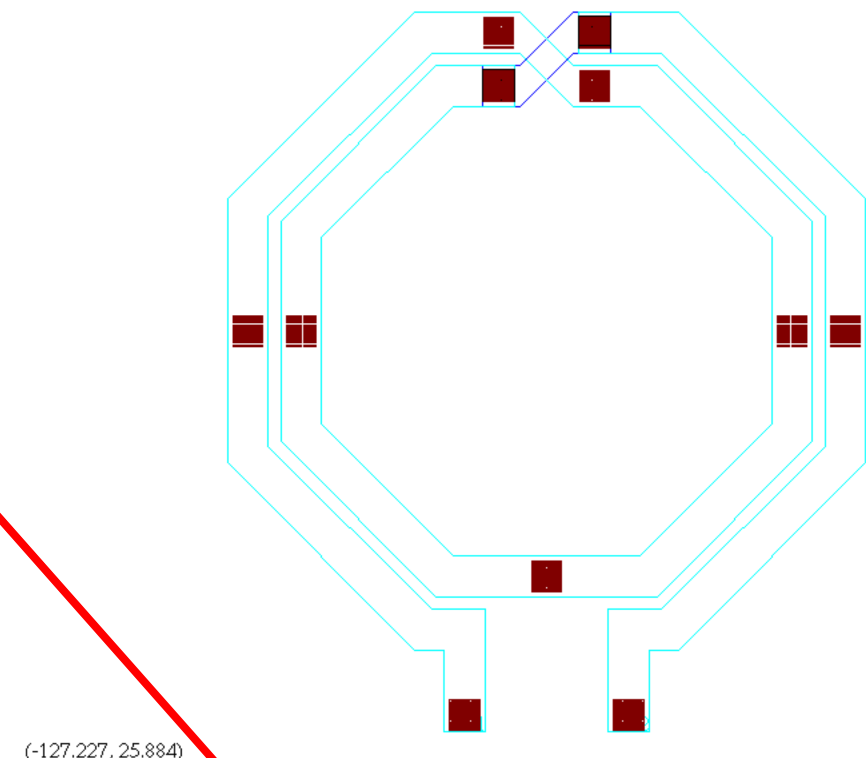
Simulation, modeling and plotting



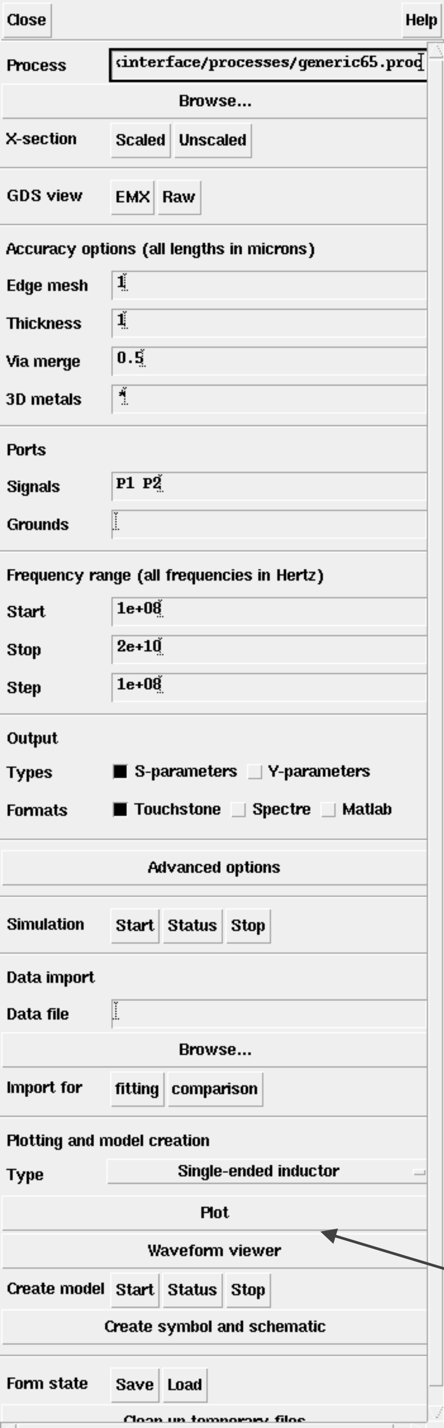


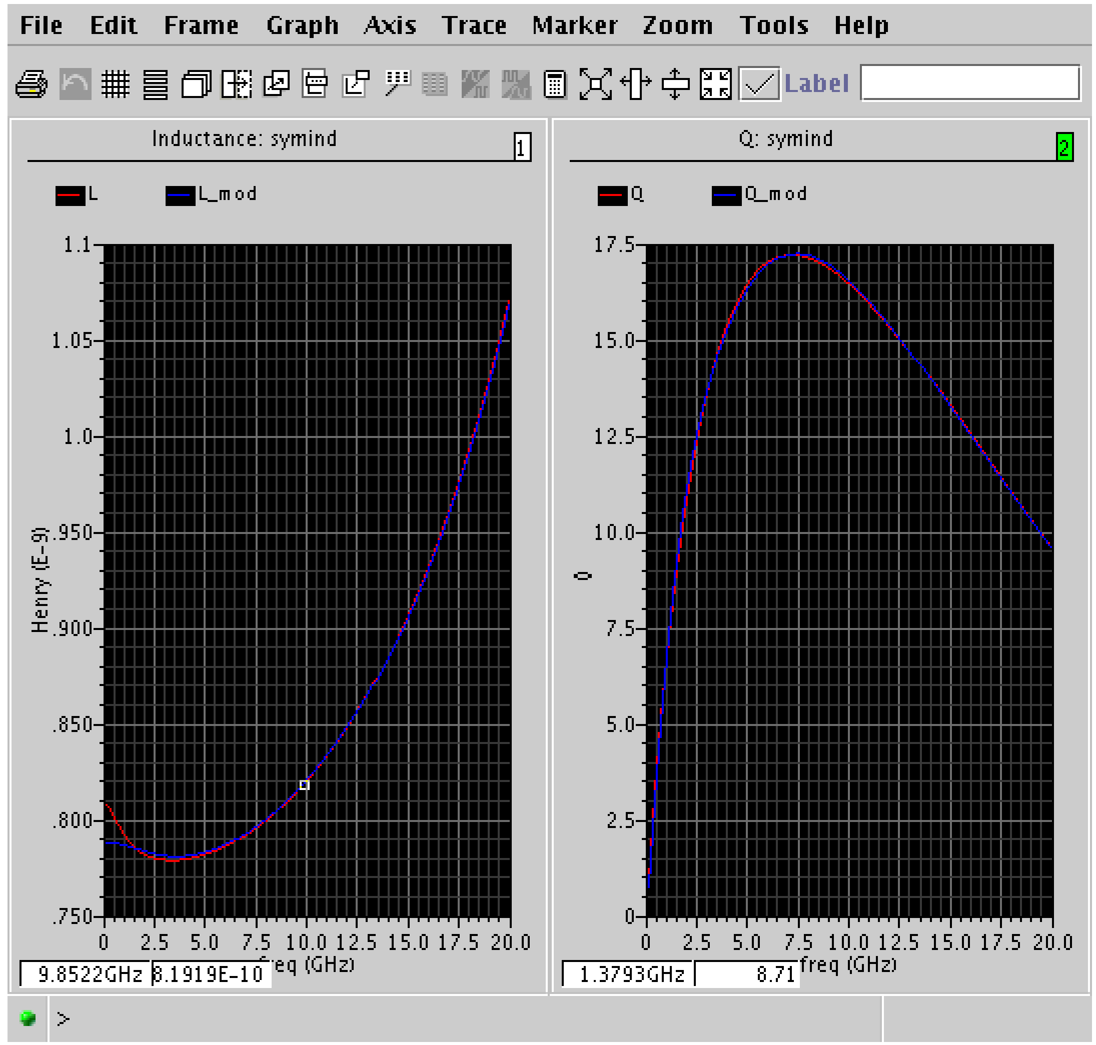
View the process file





View the raw .gds

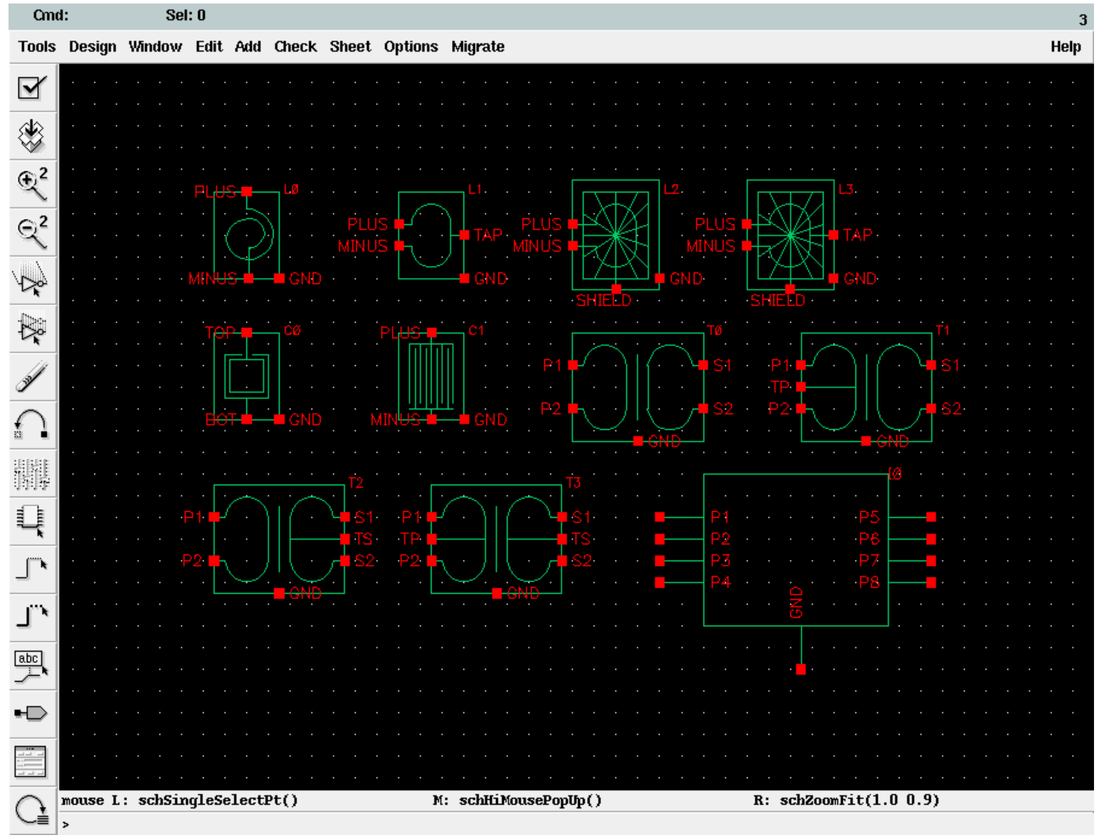




Generate/compare model vs EMX simulation

The devices

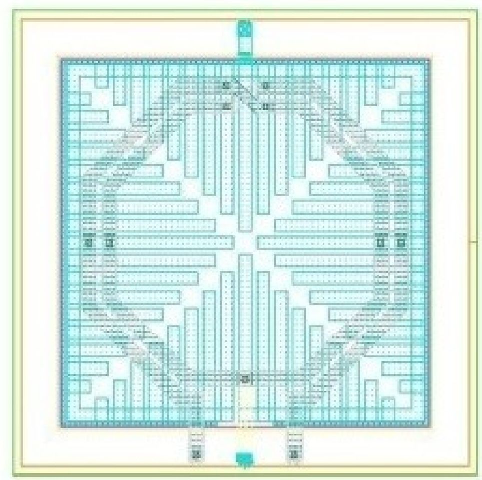
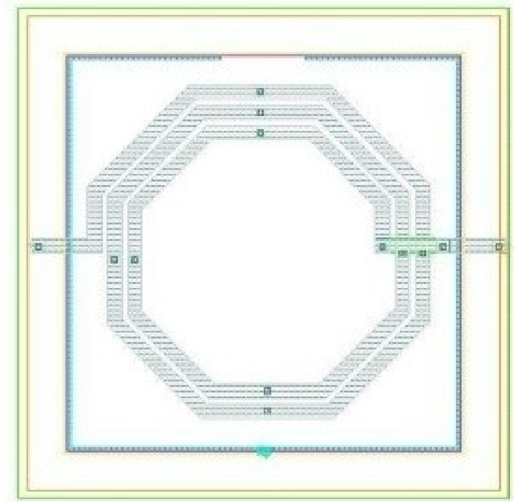
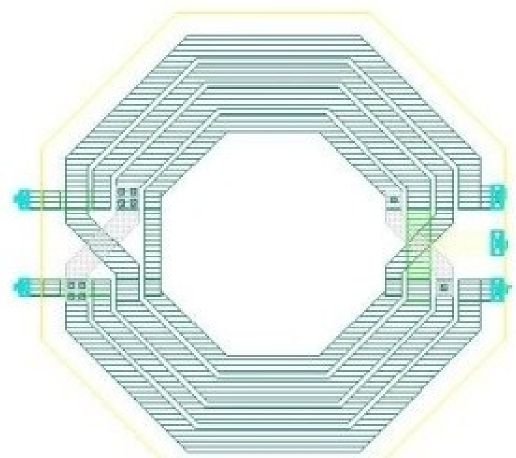
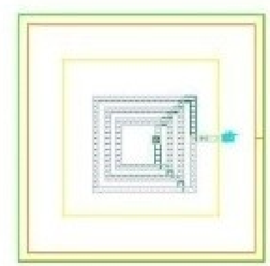
- Single-ended inductor
- Differential inductor
- Single-ended shield inductor
- Differential shield inductor
- Center-tapped inductor
- Center-tapped inductor (common mode)
- Center-tapped shield inductor
- Single-ended finger capacitor
- Differential finger capacitor
- MiM capacitor
- Transformer, no taps
- Transformer, tapped primary
- Transformer, tapped secondary
- Transformer, both tapped
- Tcoil
- N-port



This is the list of currently supported models that can be generated by EMX and Modelgen.

PCELLS

- PCELLS for various components
- Inductors
  - Spiral, Stacked, Symmetric, Peaked
- Transformers
  - 4,5,6 port
- MOM capacitors
- Shields
- DRC clean

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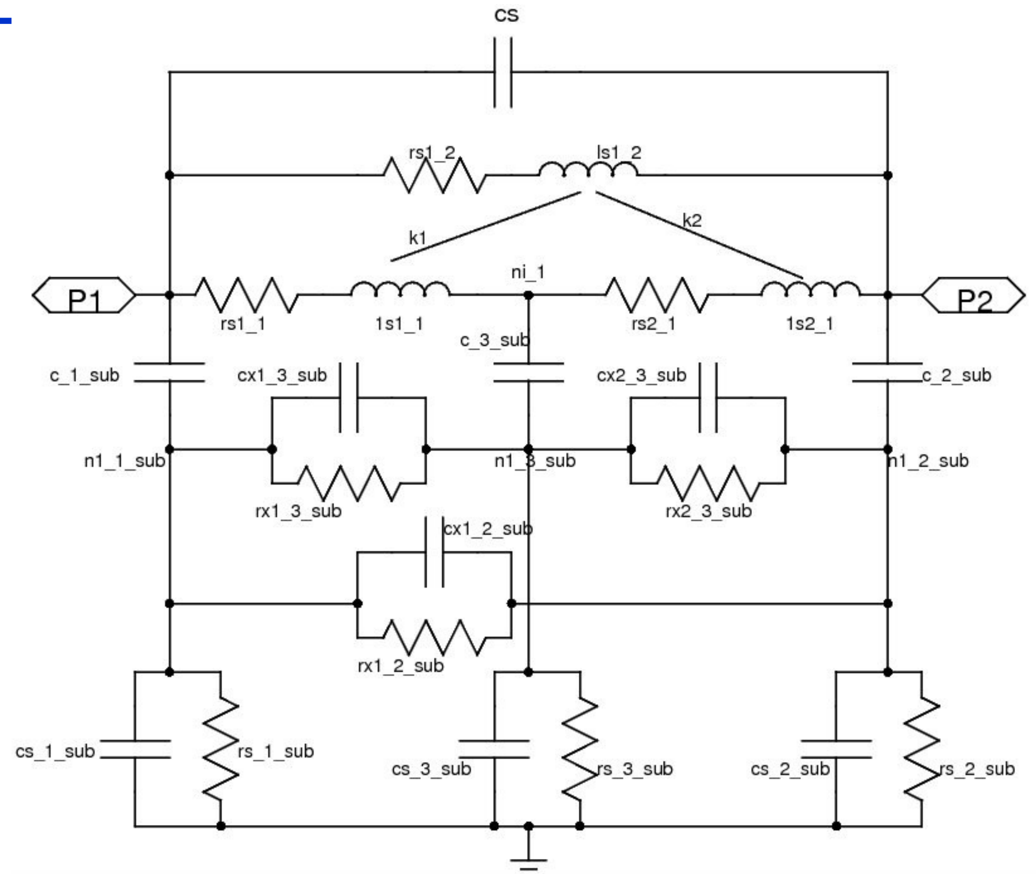
Scalable models

- EMX-Continuum used to generate scalable component models
- 100s of EMX simulations
- Single scalable model is constructed
- Model topology is physics based
- Within a few percent of the EMX simulation
- Models used by TSMC, UMC, GF and IBM

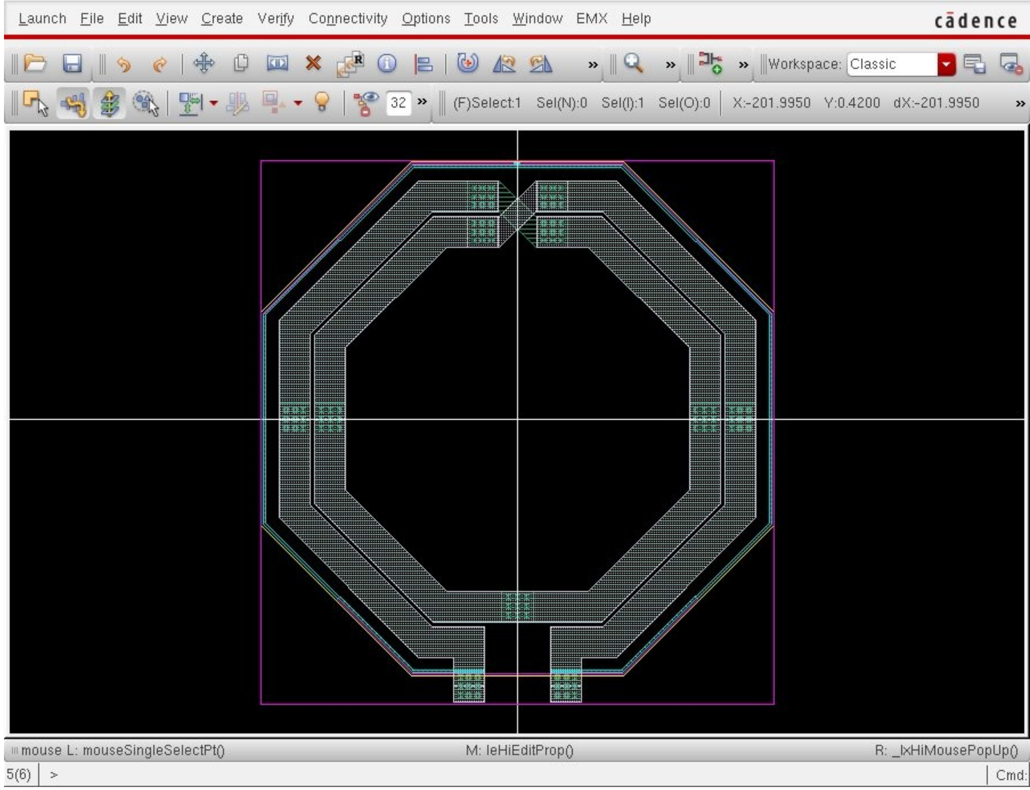


Scalable Model

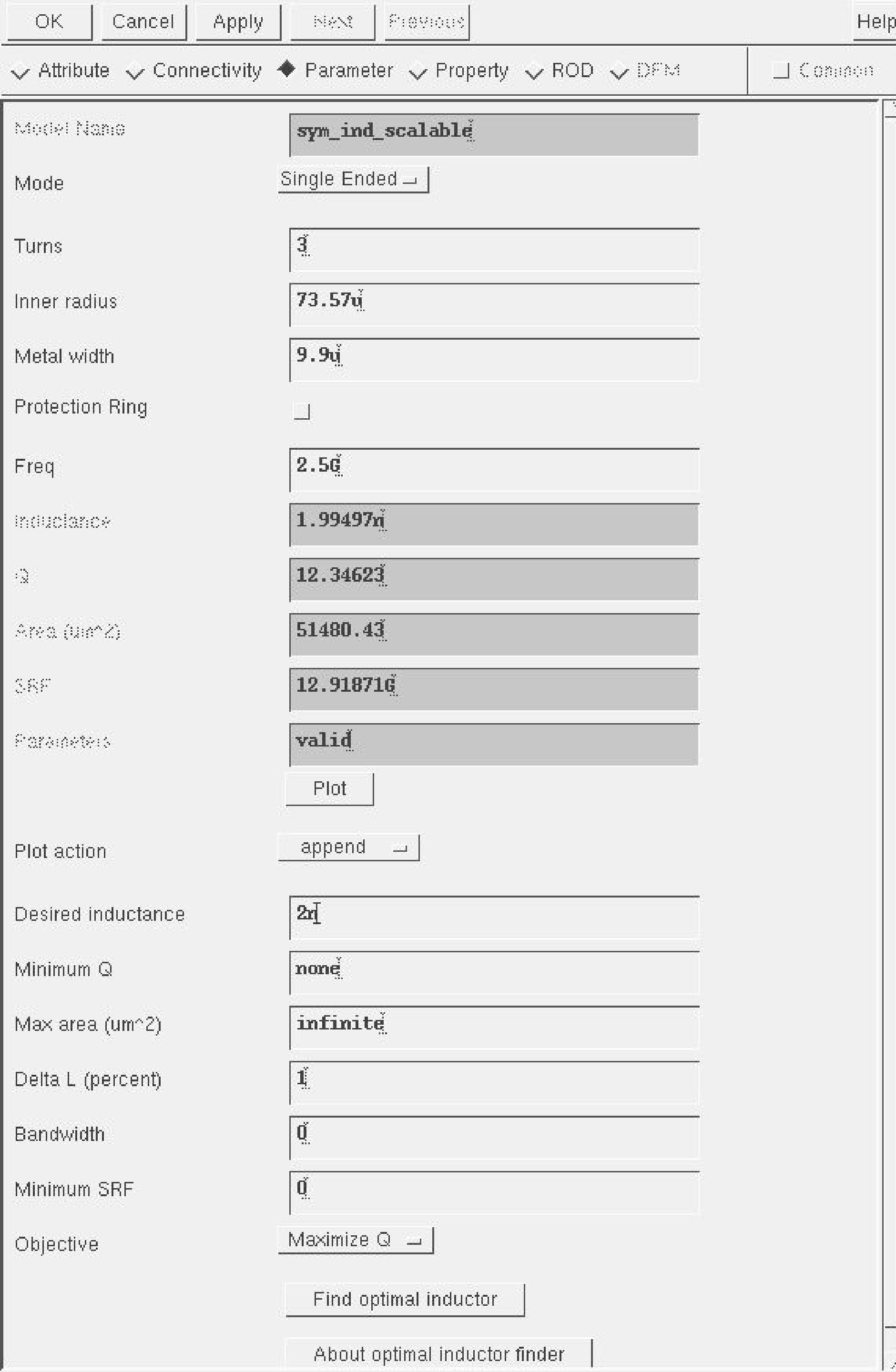
Integrand Software, Inc.

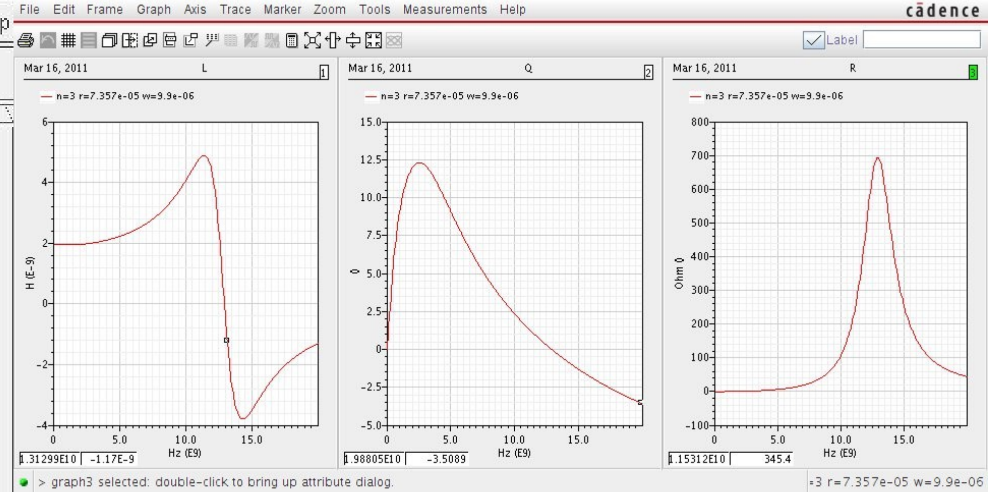
Optimum component synthesis

- With scalable models it is possible to do a gradient based optimization
- Exploration of design space
  - Maximize Q of inductors
  - Minimize insertion loss of Baluns
- Optimum component in seconds



Optimum inductor


OK Cancel Apply Next Previous Help
Attribute Connectivity Parameter Property ROD DFM Common
Model Name sym_ind_scalable
Mode Single Ended
Turns 3
Inner radius 73.57u
Metal width 9.9u
Protection Ring
Freq 2.5G
Inductance 1.99497n
Q 12.34623
Area (um^2) 51480.43
SRF 12.918716
Parameters valid
Plot
Plot action append
Desired inductance 2n
Minimum Q none
Max area (um^2) infinite
Delta L (percent) 1
Bandwidth 0
Minimum SRF 0
Objective Maximize Q
Find optimal inductor
About optimal inductor finder


File Edit Frame Graph Axis Trace Marker Zoom Tools Measurements Help
cadence
Mar 16, 2011 L
Mar 16, 2011 Q
Mar 16, 2011 R
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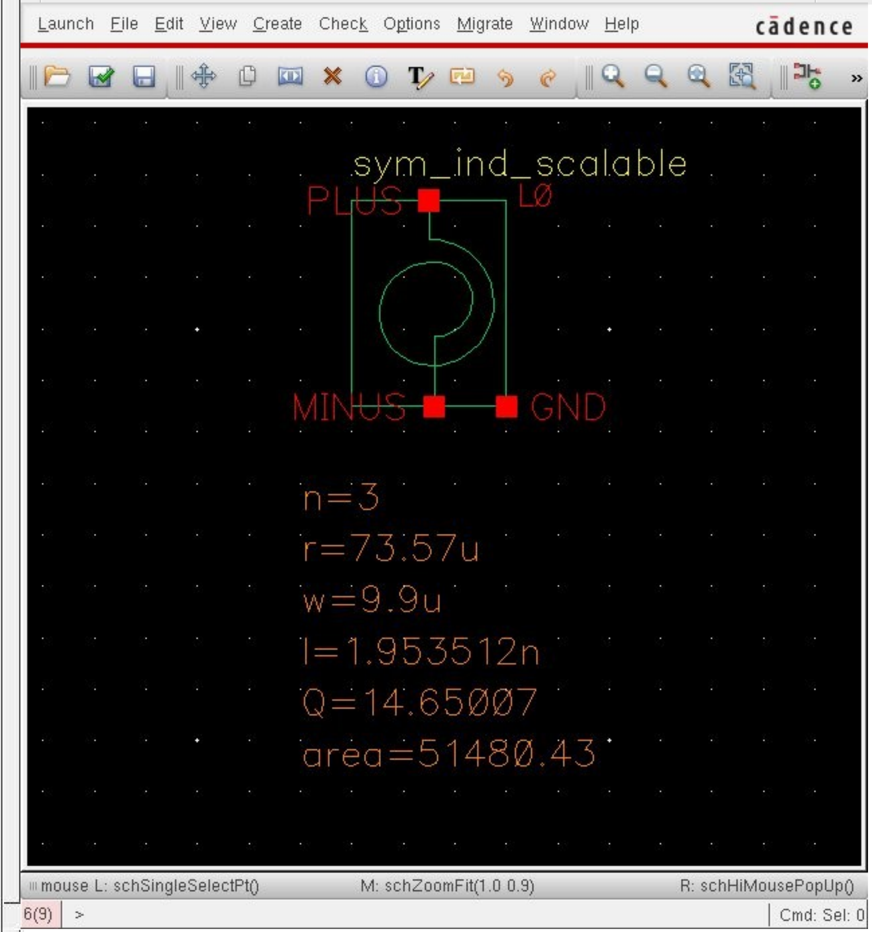
H (E-9)
Ohm
Hz (E9)
graph3 selected: double-click to bring up attribute dialog.


Launch File Edit View Create Check Options Migrate Window Help
cadence
sym_ind_scalable
PLUS
L0
MINUS
GND
n=3
r=73.57u
w=9.9u
l=1.953512n
Q=14.65007
area=51480.43
mouse L: schSingleSelectPt()
M: schZoomFit(1.0 0.9)
R: schHiMousePopUp()
Cmd: Sel: 0

Using EMX

- Operating Systems
  - 64-bit or 32-bit Linux OS
- Memory
  - 2GB RAM for 32-bit machines
  - As much as you can have for 64-bit machines

    8G, 16G, 32G are commonly used by our customers
- Multi-threading feature available
  - 2X-6X faster on an 8CPU machine
- Platform LSF support
  - Bsub for cloud based compute farms
- Auxillary programs in Matlab
  - Plotting and circuit extraction toolkit, EMX meshes, Current Plots, Charge Plots

Conclusions

- EMX
  - Full Wave, 3D simulation, accurate and very fast
  - What goes to mask goes to simulator (vias, slotting, fill)
  - Very easy to learn and use
  - Used for component-level to circuit level simulations
  - Can be used from command line or within Cadence Virtuoso
  - Dramatically reduces design cycle time and enhances productivity
  - Has been adopted by the world’s major foundries for all scalable model generation and modeling