Input Filter Design for Power Factor Correction Circuits

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Abstract— **The issues involved in the design of PFC circuit input filters are significantly different from those involved in the design of input filters for dc-dc converters. In many cases, the EMI and power factor requirements are impossible to meet using the existing filtering technology. This paper proposes the use of high-order elliptic filters to achieve the required EMI attenuation and power factor. The new input filter technology provides a significant filter size reduction over the standard filter designs, minimizes the filter-converter interaction, and maintains a good converter power factor. New active and passive filter damping methods that guarantee optimal filter pole damping, while virtually eliminating damping resistor power dissipation, are proposed. The filter design procedure that makes possible a simple and fast design of filters with an arbitrary number of stages is also presented.**

I. Introduction

THE design of input electromagnetic interference (EMI) filters for power factor correction (PFC) circuits is becoming increasingly important in the light of the new harmonic and EMI reduction standards. These standards impose very high switching noise attenuation requirements, often in excess of 100 dB. Such attenuation levels are all but impossible to meet using the existing input filter technology. They call for the use of three- or even four-stage input filters for which there are practically no design guidelines. The filters are typically designed on a trial-and-error basis, using circuit simulators. This type of design results in poor and bulky input filters, which may account for the larger part of the converter weight and volume.

Unlike the case of the EMI filter design for dc-dc converters [1], the design of input filters for PFC circuits has not yet been addressed. The issues in designing an EMI filter operating with ac power are different from and broader than those involved in the filter design for dc-dc converters; thus, the design guidelines provided in [1] are inadequate for the PFC circuit input filter design. The use of standard input filter design procedures developed for dc-dc converters generally results in poor power factor due to large reactive currents through input filter capacitors, excessive power dissipation in damping resistors, or converter instability due to filter-converter impedance interaction.

This paper addresses the PFC circuit EMI filter design and proposes the use of a new, high-order, input filter. The proposed technology provides great reduction in filter size and output impedance, while maintaining the power factor at the desired level. Attenuation levels in excess of 100 dB are easily attainable. Filter design procedure is provided that makes possible a simple and fast design of filters with arbitrary number of stages. The paper also proposes a new passive and active filter damping methods that guarantee optimal filter pole damping, while practically eliminating damping resistor power dissipation.

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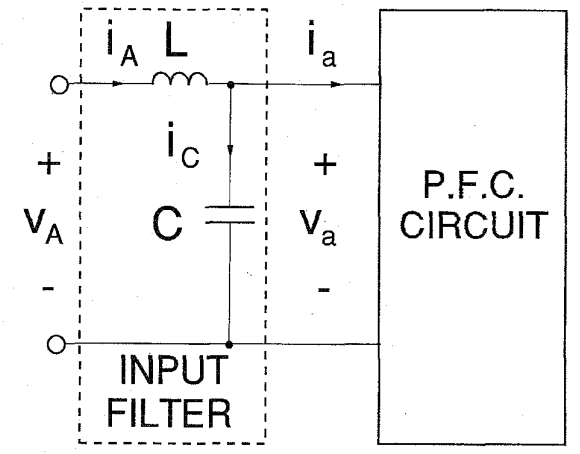
II. PFC Circuit EMI Filter Design Criteria

The three main requirements a PFC circuit input filter has to meet are the following:

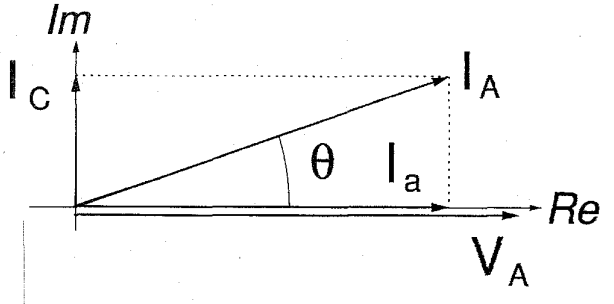
1) required switching noise attenuation,
2) low input displacement angle between filter input voltage and current, and
3) overall system stability.

The first requirement is dictated by the EMI control standards, e.g., VDE 0871, Mil. Std. 461D. All of the mentioned standards require very low EMI levels. The required switching frequency attenuation provided by the input filter, for a typical 1–10 kW converter switching in the 50 kHz range, is between 60 and 120 dB, depending on the converter power and topology.

The second requirement exists only in the PFC circuit input filter design. Fig. 1(a) shows a simplified diagram of a PFC converter with an input filter. Fig. 1(b) shows the phasor diagram of the line frequency components of the system currents and voltages. It is assumed here that all the filter components are placed on the ac side of the input rectifier, so that no low-frequency distortion of input current is introduced. A typical PFC circuit is operated in a way that produces converter average current, i_a, that is, in phase with the converter voltage, v_a. Since the voltage drop across the input filter inductor L is very small at line frequency, the voltage at the converter input is essentially equal to the line voltage v_a. The voltage v_a causes reactive current, i_c, to flow through the filter capacitor C. The total current drawn from the line, i_a, is therefore phase-shifted, relative to the input voltage, by the angle θ, resulting in reduced input power factor. If v_a



(a)



(b)

Fig. 1. Input voltage and current displacement due to input filer. (a) Simplified PFC converter and input filter diagram. (b) Current and voltage phasor diagram.

and i_a are given by

$$v_a \simeq v_A = V_m \cos \omega t$$
$$i_a = I_m \cos \omega t \tag{1}$$

where V_m and I_m are the voltage and current amplitudes, respectively, the input current, i_A, in Fig. 1 is

$$i_A = i_a + i_c = I_m \cos \omega t - \omega C V_m \sin \omega t. \tag{2}$$

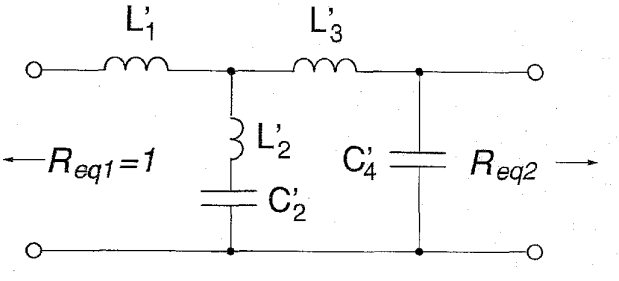
There, the current i_A leads the voltage v_A by a phase angle

$$\theta = \tan^{-1} \frac{\omega C V_m}{I_m}. \tag{3}$$

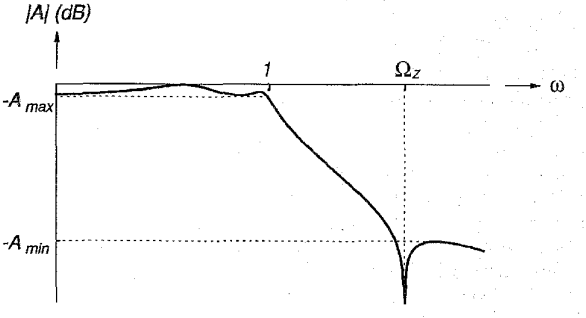
The phase shift is proportional to the filter capacitance value; so in order to maintain high input displacement factor (IDF), defined as $IDF \equiv \cos \theta$, the capacitor size has to be minimized. This typically translates into an upper limit for the filter capacitor value, which from (3) is

$$C_{\max} = \frac{I_m}{\omega V_m} \tan (\cos^{-1} IDF). \tag{4}$$

In the case of multistage filters, $C_{\max}$ represents the limit for the sum of all parallel capacitances in the filter [3].



(a)



(b)

Fig. 2. Cauer-Chebyshev filter. (a) Two-stage filter topology. (b) Typical attenuation characteristic.

The capacitor size limitation has several implications on the PFC circuit filter design. In order to meet the required attenuation specifications, the filter inductor size increases, which results in the overall filter size increase. Filter damping methods typically applied in the dc-dc converter filters cannot be used. The input filter output impedance, related to the total filter capacitance, is more difficult to control, potentially resulting in converter instability.

The third requirement amounts to controlling the impedance interaction between the input filter and the PFC converter. In general, the filter output impedance should be as low as possible when compared to the converter input impedance [1], [3], [6]. The filter output impedance can be reduced by increasing the filter capacitor size. The impedance interaction constraint will practically determine the lower bound on the filter capacitor value. Additionally, proper filter pole damping is extremely important for achieving low filter output impedance for all frequencies and, thus, overall system stability.

Finally, in order to keep the filter component values and size small, it is desirable to have the filter corner frequency as close as possible to the switching frequency, i.e., the filter should have a very steep pass-band-to-stop-band transfer characteristic. Therefore, only high-order filters can have a reasonable size and meet all the requirements in the PFC circuit.

One filter type that is known to provide these features is the Cauer-Chebyshev (CC) filter [2], also known as the elliptic-integral filter. A two-stage CC filter with normalized component values and a typical attenuation characteristic are shown in Fig. 2(a) and (b), respectively. The filter design procedure will be discussed later in the paper.

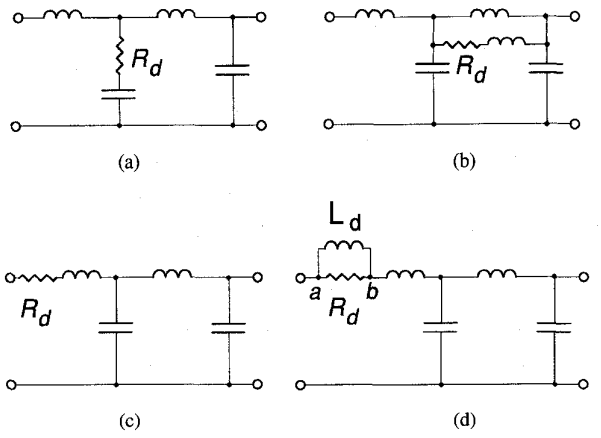


Fig. 3. Four passive filter pole damping methods.

The filter shown in Fig. 2(a) can be used either in a single-phase or in a three-phase PFC system. In a three-phase system, the filter of Fig. 2(a) would be a per-phase filter connected between the line and neutral points, which can then be transformed to equivalent line-to-line filter if desired.

III. Passive Damping of Filter Poles

Fig. 3 shows four possible filter pole damping methods. The damping method shown in Fig. 3(a) is typically used in dc-dc converters. This method is not applicable in ac power converters for the following reason. In order for the damping resistor to be effective, the capacitor in series with R_d has to be at least 10 times bigger than the other filter capacitor. This can cause excessive dissipation at line frequency because of the ac current flowing through the damping branch. Also, the required wide spread of capacitance values is usually not possible with CC filters.

The damping method in Fig. 3(b) uses a parallel R-L branch. This method eliminates the excessive resistor dissipation and is, therefore, widely used in ac power converter filters. The drawback of this method is that the parallel R-L branch provides an alternative path for high-frequency current, thus deteriorating the high-frequency attenuation capability of the filter. In order to meet the required attenuation, the filter has to be overdesigned by typically more than 50% when compared to filters shown in Fig. 3(c) and (d), which results in excessively large components.

The damping method shown in Fig. 3(c) provides an optimal filter attenuation characteristic and is standardly used in low-power electronic circuits. This method, however cannot be used in power electronics circuits because of excessive power dissipation in the damping resistor.

A new damping method presented in this paper is shown in Fig. 3(d). It solves the dissipation problem of the series resistor damping scheme by providing an alternative line frequency current path through the inductor L_d, without affecting the damping action of the resistor at high frequencies. The main drawback of the proposed damping method is that the corner frequency of the damping network given as $f_d = R_d/(2\pi L_d)$ has to be significantly lower than the lowest filter pole frequency. This requirement typically results in a large value of L_d.

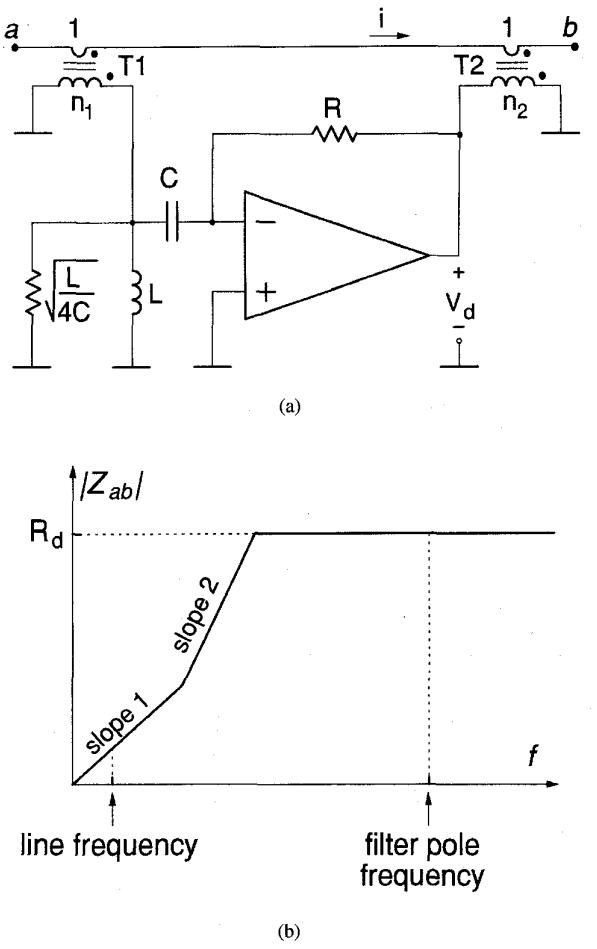


Fig. 4. Active damping scheme. (a) One circuit implementation. (b) Impedance characteristic.

IV. Active Damping of Filter Poles

The problem of the passive damping method shown in Fig. 3(d) can be resolved by implementing the damping circuit using an active impedance simulation scheme. A possible active damping scheme, which replaces the $R_d \| L_d$ connection in Fig. 3(d), is shown in Fig. 4(a). The transformer T1 is used to sense the line current. The low-frequency components of T1's secondary current are bypassed to ground through L. The high-frequency current components flow through C and R and create voltage at the output of the operational amplifier. The voltage v_d at high frequencies is proportional to the line current, i.e. $v_d \simeq R\, i/n_1$. This voltage is impressed across the secondary of the transformer T2 so that the effective resistance seen in the primary is

$$R_d \equiv \frac{v_{ab}}{i} \simeq \frac{R}{n_1 n_2} \tag{5}$$

at high frequencies. The corner frequency of L and C has to be much higher than the line frequency and much lower than the lowest input filter pole frequency. The resistor in parallel with

L provides critical damping for the resonant circuit formed by L and C. The impedance characteristic Z_{ab} seen in the circuit primary is shown in Fig. 4(b) and is given by

$$Z_{ab}(s) = \frac{R}{n_1 n_2} \frac{s\left(s + \frac{n_2}{n_1 RC}\right)}{s^2 + s\frac{2}{\sqrt{LC}} + \frac{1}{LC}}. \quad (6)$$

At low frequencies, Z_{ab} is the impedance of the inductor L reflected through T1. There is practically no current through C and R, so that the op-amp does not process any power. The placement of the zero

$$f_{zab} = \frac{-n_2}{2\pi n_1 RC} \quad (7)$$

is not very critical. The only requirement is that it should lie below the damping circuit pole frequency. Such a placement ensures that Z_{ab} is resistive above the pole frequency $f_{pab} = 1/(2\pi\sqrt{LC})$.

This active circuit provides significant savings in size compared to the passive damping circuit realization. The power processed by the circuit is typically less than 0.1% of the total converter power so it can be easily implemented with high-power op-amps.

V. Cauer-Chebyshev EMI Filter Design Procedure

The design procedure presented in this section uses the already existing knowledge of CC filter design systematized and condensed in filter design tables such as those in [2] or available in filter design computer programs [8]. This approach leads to a very simple and flexible design procedure that can efficiently be used for the design of input filters of any order.

The first step in the filter design is the determination of the required filter attenuation. The allowable EMI voltage, V_{EMI}, injected to the line by the converter at the switching frequency can be determined from the EMI specifications. V_{EMI} is typically specified as voltage drop on a 50-Ω resistor R_{lisn} (line impedance stabilization network [5]) caused by the converter switching current. The switching frequency current, I_{SW}, generated by the converter can either be determined analytically by Fourier analysis, by simulation [7], or by measurement. With the knowledge of V_{EMI} and I_{SW}, the required filter attenuation, $A_{\min}$ at the switching frequency is given by

$$A_{\min} = \frac{R_{lisn} I_{sw}}{V_{EMI}}. \quad (8)$$

Next, the total maximum filter capacitance has to be determined. For this, the input displacement factor constraint has to be chosen as a desired minimum IDF under certain line voltage, $V_{\lim}$, and current, $I_{\lim}$, conditions, typically high-line, partial load. The total maximum filter capacitance can be calculated using (4), with $I_m = I_{\lim}$, and $V_m = V_{\lim}$.

Next, the normalized filter parameters have to be determined. For this, the filter order, n, has to be chosen first. The choice may be made either using filter order nomographs, [2, p. 142], or by reading the filter tables. The assumptions that should be made in the filter order choice are that the passband ripple is reasonable (e.g., $A_{\max} \simeq 2dB$) and that the converter is running under no-load condition ($R_{eq2} = inf$). This will guarantee proper filter damping even under no-load conditions. There is some freedom in the filter order choice. Filters of higher order may end up being smaller than those of lower order, so some engineering judgment should be used in each application. Notice that with a filter structure as shown in Fig. 2(a) (series inductor at the filter input, parallel capacitor at the filter output), n is always an even number. With the knowledge of $A_{\min}$ and the filter order determined, the normalized filter parameters L'_1, L'_2, etc., C'_2, C'_4, etc., and Ω_z, all defined in Fig. 2, can be readily obtained from the filter tables.

The final design step is the filter denormalization. First, the reference frequency, ω_r, is calculated as

$$\omega_r = 0.85\frac{2\pi f_{sw}}{\Omega_z} \quad (9)$$

where f_{sw} is the converter switching frequency. With the reference frequency calculated in this way, the frequency of the filter transfer function first notch will be 15% below the switching frequency. It is important to place the switching frequency sufficiently far from the transition region so that any variation of filter component values does not influence its attenuation characteristic at switching frequency significantly. The 15% margin in (9) guarantees that if the filter is built using components with 10% tolerance, the switching frequency will remain in the filter stop-band region. If components with wider tolerance are used, this margin has to be increased.

In general, the filter denormalization is done by choosing the value of any one filter component and then calculating the values of the remaining filter components. This choice is based on different practical considerations, such as availability of a particular component, damping resistor power dissipation, total filter size, etc. In the filter design for PFC circuits, the filter should be denormalized so that its total capacitance equals $C_{\max}$. Such denormalization ensures that the IDF requirement is met. So, the damping resistor is calculated as

$$R_d = \frac{\sum_{i=1}^{i=n/2} C'_{2i}}{\omega_r C_{\max}}. \quad (10)$$

The remaining filter components are calculated using

$$L_i = \frac{L'_i R_d}{\omega_r}, \qquad i = 1, 2, \ldots, n-1$$
$$C_k = \frac{C'_k}{\omega_r R_d}, \qquad k = 2, 4, \ldots, n \quad (11)$$

with the filter design completed, only the active damping circuit remains to be designed. The first step in doing this is to choose the transformer turns ratios, n_1 and n_2, according to the maximum line current and the operational amplifier voltage and current capabilities. With n_1 and n_2 known, R can be calculated from (5) and (10). T1's magnetizing inductance can be used as L, and C can be calculated so that f_{pab} is much higher than the line frequency and much lower than the lowest filter pole frequency, f_{lp}, e.g.

$$C = \frac{1}{4\pi^2 L f_{\text{line}} f_{lp}}. \quad (12)$$

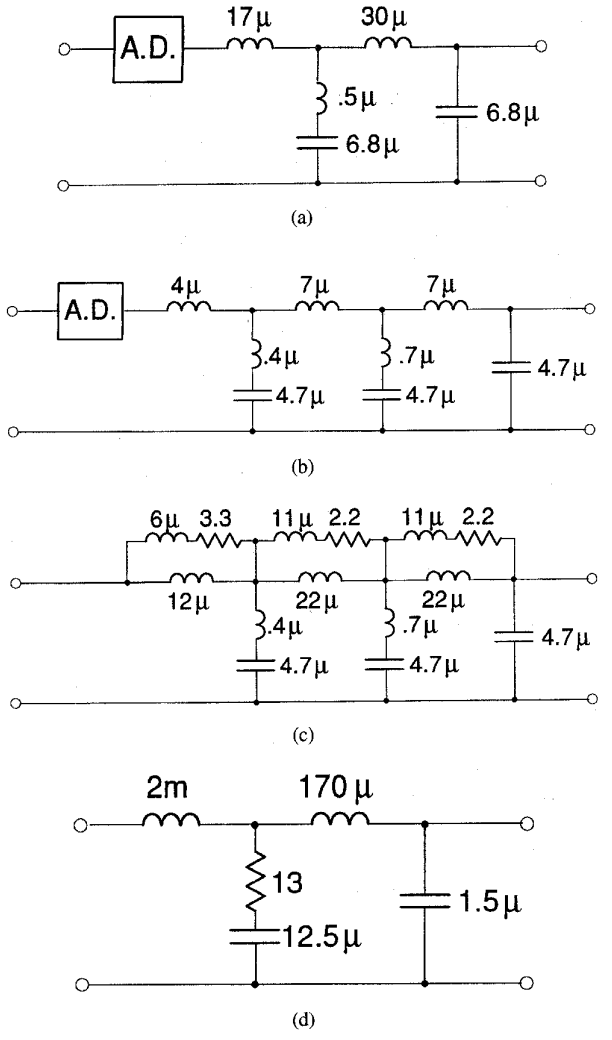


Fig. 5. Comparison of different filters designed for the same specifications. (a) Two-stage CC filter from the design example. (b) Three-stage CC filter with active damping. (c) CC filter with passive damping. (d) Standard LC filter.

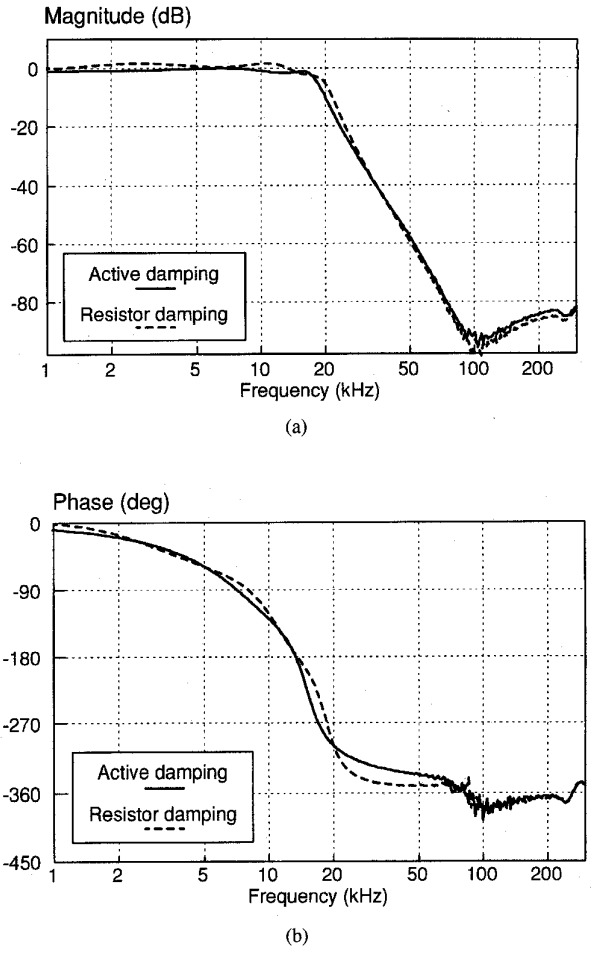


Fig. 6. Measured filter transfer functions.

Finally, it should be checked if f_{zab}, given by (7), is lower than f_{pab}. If not, n_1, n_2, R and I or C should be modified, and the damping circuit should be redesigned accordingly.

The use of the above design procedure is illustrated in the design of the two-stage filter shown in Fig. 5(a). Since the procedure is applicable to the design of filters of any order, a possible three-stage implementation of the input filter that also meets the same specifications is shown in Fig. 5(b). This illustrates the possibility of reducing the overall filter size by increasing the number of filter stages.

Figure 5(c) shows a three-stage filter designed to meet the specifications of the example, but using the more conventional parallel R-L damping method. The total inductance in this filter is around 60 μH as compared to only 18 μH in the actively damped filter. The reduction of the inductor size leads both to significant reduction of the filter size and also to the reduction of the filter output impedance, thus contributing to the overall system stability.

The advantage of using CC filters is illustrated when the above filters are compared with the standard LC filter designed for the same specification, which is shown in Fig. 5(d).

VI. Experimental Results

The filter in Fig. 5(a) has been implemented and tested. Fig. 6 compares measured transfer functions of the filter, which is damped passively using only the 1.7 Ω series resistor [as shown in Fig. 3(c)], with those of the filter using active damping. This demonstrates that the active damping scheme provides the required damping without affecting the ideal filter transfer function.

Fig. 7 shows the damping circuit performance under large-signal transient conditions. The filter is connected to a square-wave modulated active load drawing a 2.5-A sinusoidal current plus a 1-A square-wave current. The equivalent block diagram of the measurement setup is shown in Fig. 8. Fig. 7(a) shows the filter input current (i in Fig. 8) when the filter is not damped, i.e., with the active damping circuit turned off. The high-frequency oscillations originate from the undamped 6-kHz filter pole. Fig. 7(b) shows the same current when the damping circuit is operational. Fig. 7(c) shows the operational amplifier output voltage [v_d in Fig. 4(a)]. It is seen that even

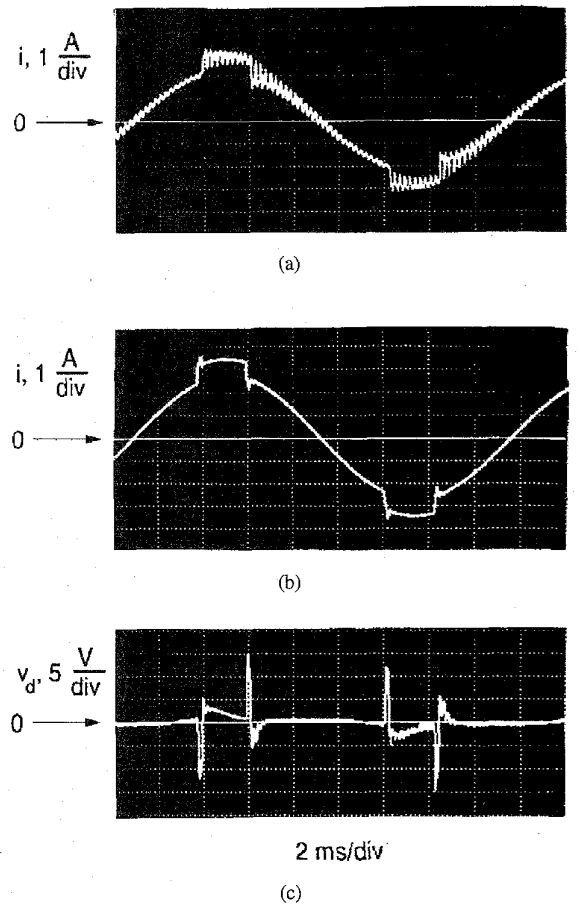


Fig. 7. Filter responses to current transients. (a) Filter input current without damping. (b) Filter input current with active damping. (c) Op-amp output voltage.

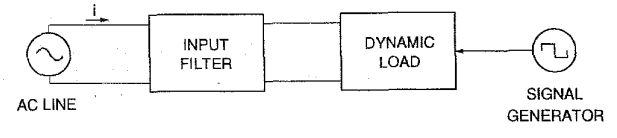


Fig. 8. Block diagram of the filter measurement setup used to obtain the waveforms of Fig. 7.

though there is a large 60-Hz current component in the filter current, the voltage v_d contains only a very small 60-Hz component.

VII. Conclusion

Power converter designers face several difficult issues when designing input filters for PFC circuits: very high attenuation requirement, low filter output impedance requirement, and maintenance of high converter power factor. Meeting all these requirements is in most cases impossible using the standard filter design technology. In fact, the existence of "standard input filter design technology for PFC circuits" is indeed questionable. There are no analytical or systematic numerical design tools, and the designs are performed on a trial-and-error basis, which results in large and heavy filters.

This paper presents a new approach to design of input filters for power electronic circuits. This approach is based on the application of a vast body of knowledge about passive L-C filters that has existed for many years but has not been used in power electronics. The main obstacle to applying this knowledge has been the inadequate filter pole damping technology.

The new passive and active filter pole damping schemes proposed in the paper provide damping without affecting the filter high-frequency attenuation characteristic. Applying these damping methods to high-order elliptic filters results in significant filter size reduction, compared to the standard filter designs.

The paper presents an input filter design procedure for PFC circuits. Relying on the existing, well organized, and readily available knowledge about passive L-C filters, the design procedure is simple and straightforward. The technology described in this paper is a step towards miniaturization and performance optimization of input filters.

Appendix
Filter Design Example

In this example, a per-phase filter for a 2 kW, three-phase PWM buck rectifier with 3 × 120 V input, switching at 100 kHz, [3], [4], is presented:

- The filter is designed according to the VDE0871 "Class A" specifications, which allow no more than $V_{EMI} = 74$ $dB_\mu V$ of switching noise at 100 kHz with $R_{lisn} = 50\Omega$.
- The converter is producing $I_{sw} = 1$ A.
- This yields a required filter switching frequency attenuation of $A_{\min} = 80$ dB.
- IDF is required to be $IDF \geq 0.94$ with $V_{\lim} = 170$ V and $I_{\lim} = 3.5$ A.
- This yields $C_{\max} = 14\ \mu F$.
- The filter order is chosen as $n = 4$ with $A_{\max} = 1.25$ dB.
- The normalized filter parameters are [2, pp. 200–201] $\Omega_z = 4.89$, $L_1' = 1.11$, $L_2' = 0.03$, $L_3' = 1.96$, $C_2' = 1.36$, and $C_4' = 1.25$.
- The reference frequency is $\omega_r = 109\,217$ rad/s.
- The damping resistor is $R_d = 1.7\ \Omega$.
- The denormalized filter parameters are $L_1 = 17\ \mu H$, $L_2 = 0.5\ \mu H$, $L_3 = 30\ \mu H$, and $C_2 = C_4 = 7\ \mu F \simeq 6.8\ \mu F$.
- The active damping is implemented with $n_1 = n_2 = 50$, which gives $R = .3\ k\Omega$. The magnetizing inductance of T1 is $L = 16$ mH. Since the lowest filter pole is at 5 kHz, the L-C corner frequency is chosen at 550 Hz, which gives $C = 5.2\ \mu F$. The damping scheme is implemented with the PA26 power operational amplifier [9].
- The damping circuit zero frequency is $f_{zab} = 7.1$ Hz.

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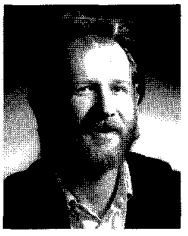

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