A High-Swing Complementary Class-C VCO

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***Abstract*—This paper presents a high-swing VCO combining the efficiency of the class-C oscillator with that of the complementary PMOS-NMOS topology. Moreover, removing the traditional tail current source, the VCO exhibits an even larger swing, maximizing the phase noise performance.**

Designed in a 90 nm CMOS process, the VCO operates between 3.3 GHz and 4.4 GHz, for a 28% tuning range. Drawing 1.8 mA from 1.2 V, the phase noise is -142 dBc/Hz at a 10 MHz offset from a 4.4 GHz carrier. The resulting phase-noise FoM is 191.5 dBc/Hz and varies 1.5 dB across the tuning range.

***Index Terms*—VCO, class-C, phase noise, start-up, feedback class-C, CMOS**

I. Introduction

The efficiency is becoming one of the most critical requirements in the design of voltage-controlled-oscillator (VCO), especially in mobile application where the definition of new bands and standards increases the number of VCOs and PLLs inside the transceiver. In this scenario, highly efficient topology like the class-C [1] and complementary class-B [2] architectures become very attractive. In particular, the latter exhibits a double efficiency compared to the traditional single-pair VCO, while the former saves as much as 36% of the bias current by enforcing the switching pair in the traditional class-B VCO to work in class-C, achieving the same phase noise performance.

Mazzanti *et al.* combines in [3] the two mentioned architectures to minimize the current consumption, but the oscillator exhibits the same trade-off of the traditional class-C VCO [1] between maximum oscillation amplitude and start-up robustness, which limits its use in a real-life application.

The hybrid architecture, proposed in [4] and based on a single pair configuration, improves this trade-off placing a class-B switching pair in parallel to the class-C core, ensuring a robust start-up even with a relatively low gate bias voltage $V_{bias,N}$ for the two class-C transistors. This approach, adopted in [5] for a cellular transmitter VCO, increases the VCO robustness to PVT variations, but implies a lower efficiency compared to a pure class-C topology. Since the $V_{bias,N}$ needed to ensure start-up is considerably higher than its steady-state value, a more efficient class-C solution is to adopt a negative feedback circuit that sets $V_{bias,N}$ adaptively. For instance, Deng *et al.* [6] and Chen *et al.* [7] use an amplitude detector in the negative feedback that adjusts $V_{bias,N}$ to keep constant the oscillation amplitude, but the amplitude detector loads the VCO tank, penalizing both tank quality factor (Q) and tuning range. A less affecting approach is to keep the current consumption at the desired value ensuring the current source works properly [8].

This paper presents a complementary class-C VCO that solves the start-up issue by means of negative feedback performed by a current mirror, as proposed in [9], which adjusts $V_{bias,N}$ to keep the current consumption at the desired value. Moreover, removing even the tail current source, the oscillator maximizes the oscillation amplitude without deteriorating the supply-pushing performance. The VCO has been realized in a 90 nm CMOS targeting the phase noise requirements of cellular GSM/WCDMA transmitters.

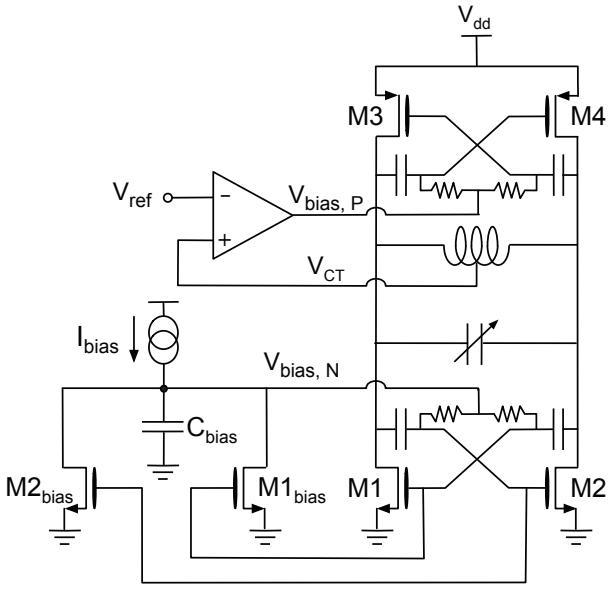

Fig. 1. Schematic view of the high-swing complementary class-C VCO.

II. High-Swing Complementary Class-C VCO

Fig. 1 shows the high swing complementary class-C VCO architecture. The two cross-coupled pairs $M1/M2$ and $M3/M4$ work in class-C, providing the negative resistance restoring the energy losses in the resonant load. The current mirror composed by $M1/M2$ and $M1_{bias}/M2_{bias}$ sets the current consumption I_{DC}, ensuring a robust start-up, while, in steady-state, the bias voltage $V_{bias,N}$ drops from its start-up value, maximizing the output swing [9]. The operational amplifier (op-amp) controls the bias voltage $V_{bias,P}$ at the gate of $M3/M4$ by means of a negative feedback that enforces the voltage V_{CT} at the central tap of the inductor equal to the reference voltage V_{ref}. Since the two cross-coupled pairs are designed to have the same overdrive voltage, V_{ref} is chosen equal to $V_{dd}/2$.

The steady-state error between V_{ref} and V_{CT} depends on the op-amp bandwidth and DC gain. A single-pole architecture with a DC gain of 25-30 dB is enough to ensure both the unconditional stability of the loop, and a V_{CT} with an accuracy of a few tens of mV, which is sufficient to guarantee the proper behaviour of the VCO. Since the loop only needs to set the DC values of V_{CM} and $V_{bias,P}$, with a minor impact on

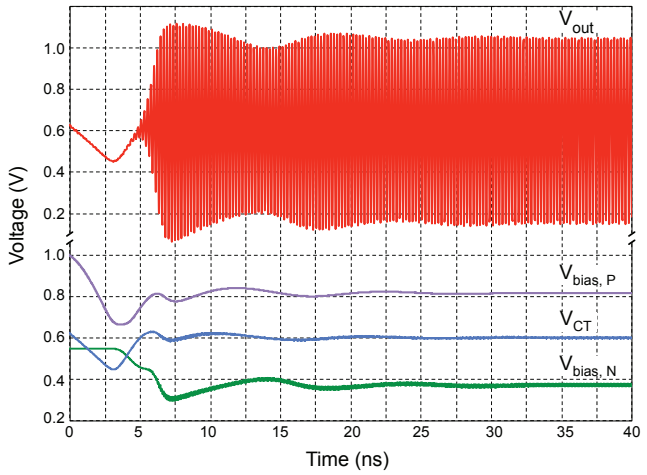

Fig. 2. Transient voltage waveforms in the high swing class-C VCO.

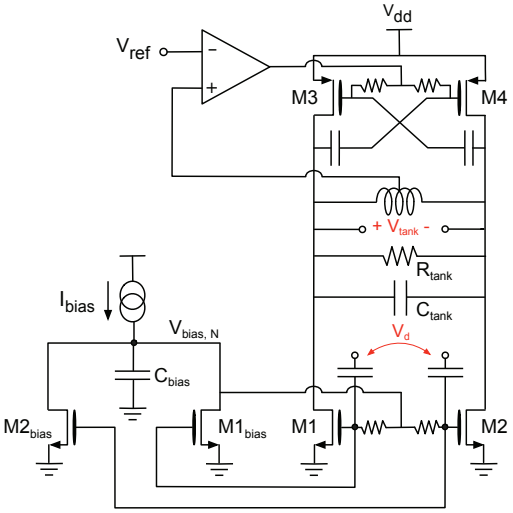

Fig. 3. VCO circuit for stability analysis of the oscillation amplitude.

the bias current, the op-amp bandwidth can be very narrow without causing a modulation of the oscillation amplitude. Moreover, the contribution of the op-amp noise to phase noise is negligible (in general, the op-amp noise contributes to phase noise via the AM-to-PM effect) and the op-amp current consumption can be set negligibly small, compared to the VCO current.

C_{bias} is instrumental for operating $M1/M2$ in class-C, integrating the difference between I_{bias} and the current (scaled by the mirror) drained by the VCO. Moreover, the capacitance filters the high-frequency noise contribution from $M1_{bias}/M2_{bias}$, improving the phase noise. However, the VCO exhibits a maximum C_{bias} value that cannot be greater than C_{tank}/N to ensure the stability of the oscillation amplitude as shown in the next subsection.

Fig. 2 plots the simulated waveforms of the most relevant voltages in the VCO at start-up. Initially, $M1_{bias}/M2_{bias}$ are diode connected (at DC) and I_{bias} is mirrored (multiplied by N) to the VCO core, enabling a safe and swift start-up. As the oscillator amplitude grows, the average current I_{DC} drained by $M1_{bias}/M2_{bias}$ increases. The excess current, integrated into C_{bias}, reduces $V_{bias,N}$, leading the switching pair $M1/M2$ to work in class-C. Meanwhile, the op-amp and the negative feedback counteracts the V_{CT} variation adjusting the $M3/M4$ gates DC-voltage to keep V_{CT} equal to the reference voltage ($V_{ref} = 600\,mV$). At the end of the transient, the two loops have generated the values of $V_{bias,N}$ and $V_{bias,P}$ needed in steady-state for class-C operation while enforcing $I_{DC} \approx I_{bias}$ and $V_{CT} \approx V_{ref}$. This maximizes the oscillator amplitude, as desired, obtaining a simulated voltage efficiency α_V (defined as the oscillation-amplitude to supply-voltage ratio) of approximately 0.38 (to be compared to the ideal $\alpha_V = 0.5$ in the complementary VCO topology). The simulated settling time is around 35 ns, low enough for any cellular communication standard.

A. Oscillation amplitude stability analysis

Since the feedback biasing $M3/M4$ gates has a negligible impact on the VCO current, which is set by the current mirror, the stability analysis focuses on the feedback loop created by the current mirror, deriving the maximum value of the capacitance C_{bias} that results in a stable amplitude of the oscillation. We use the same approach adopted in [1] and [8], where instability is assumed to result in an ideal amplitude modulation of the oscillation, and calculating the common-mode and differential-mode loop gains ($G_{loop,\,cm}$ and $G_{loop,\,d}$) for common-mode and differential-mode signals applied to the respective open-loop circuits (linearised around the large-signal operation point of the oscillator across one oscillation period).

In particular, the differential-mode stability is assessed applying a differential two-tone signal V_d with amplitude A_d and frequencies $\omega_0 + \Delta\omega$ and $\omega_0 - \Delta\omega$ (answering for the amplitude modulation of the large carrier) between the gates of $M1$ (and $M1_{bias}$) and $M2$ (and $M2_{bias}$) as in Fig. 3, while the output coincides with the differential output V_{tank} across the LC tank. The currents i_{M1} and i_{M2} delivered by $M1$ and $M2$ ($i_{M1_{bias}}$ and $i_{M2_{bias}}$ are equal to i_{M1} and i_{M2} scaled down by N) are therefore:

$$i_{M1}(t) = \left[\sum_p g_p \cos[p(\omega_0 t + \pi)]\right]\left(V_{bias,N}(t) - \frac{V_d}{2}(t)\right) \quad (1)$$

$$i_{M2}(t) = \left[\sum_p g_p \cos[p(\omega_0 t)]\right]\left(V_{bias,N}(t) + \frac{V_d}{2}(t)\right) \quad (2)$$

where the transconductances $g_m(\omega_0 t + \pi)$, $g_m(\omega_0 t)$ of $M1$, $M2$ are expressed with the respective Fourier series, and

$$V_{bias,N}(t) = A_{bias,N}\cos(\Delta\omega t) \quad (3)$$

$$V_d(t) = A_d\left\{\cos\left[(\omega_0 - \Delta\omega)t\right] + \cos\left[(\omega_0 + \Delta\omega)t\right]\right\} \quad (4)$$

yielding $G_{loop,\,d}$ at $\omega_0 + \Delta\omega$ (or at $\omega_0 - \Delta\omega$) as

$$G_{loop,\,d} = -\frac{R_{tank}}{2(1 + j2Q\Delta\omega/\omega_0)}\left(\frac{(g_2 + 2g_0)Nj\Delta\omega C_{bias}}{Nj\Delta\omega C_{bias} + g_0}\right) \quad (5)$$

The envelope frequency $\Delta\omega$ and the maximum C_{bias} ensuring stability are determined applying the Barkhausen stability criterion, which states that the loop is on the verge of instability if $G_{loop,cm} = 1$, obtaining:

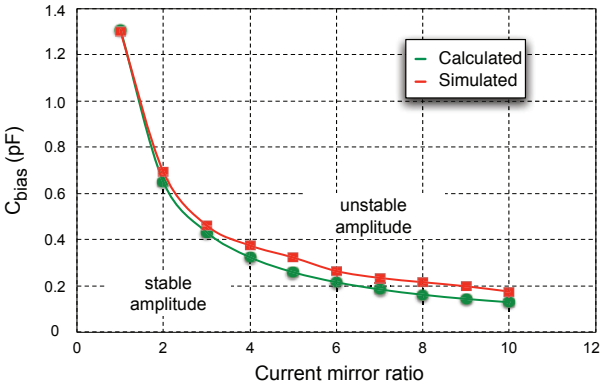

Fig. 4. Calculated and simulated upper bound for C_{bias} vs. N ensuring amplitude stability (f_{osc} = 4.4GHz)

$$\Delta\omega = \sqrt{\frac{g_0\omega_0}{2C_{bias}NQ}} \tag{6}$$

and

$$C_{bias} < \frac{2C_{tank}}{N}\frac{g_0R_{tank}}{R_{tank}(g_0+g_2/2)+1} \tag{7}$$

where expressions of g_0 and g_2 are given in [1]. In the limit case of the current pulses delivered by $M1$-$M2$ becoming Dirac deltas, (7) can be approximated as

$$C_{bias} < \frac{C_{tank}}{N} \tag{8}$$

Turning to the common-mode stability, $G_{loop,cm}$ is calculated applying a common-mode signal V_{cm} with amplitude A_{cm} and frequency $\Delta\omega$ at the gates of the switching pairs, and picking the output voltage $V_{bias,N}$ across C_{tail}. Adopting the same approach used to derive $G_{loop,d}$, it is easy to show that the common-mode feedback is always stable.

Equations (7) and (8) indicate a trade-off between N and C_{bias}. A higher N allows to reduce the bias current, but implies a smaller C_{bias}, affecting its filtering action and increasing $M1_{bias}/M2_{bias}$ contribution to phase noise (as the $M1_{bias}/M2_{bias}$ noise current is mirrored in the VCO core multiplied by N^2). Fig. 4 shows the agreement between the theoretical value of C_{bias} from (7), and SpectreRF simulations using a simplified MOS transistor model. The same simulations with the MOS model provided by the silicon foundry show that C_{bias} can be somewhat higher due to the lower gain of the real MOS transistors.

III. Prototype

Fig. 5 shows the die photo of the VCO, integrated in a 90 nm CMOS process, having a 3.2 μm thick top metal layer. The VCO occupies an area of 0.078 mm^2, comprising the MOS switching pairs, the resonant load and the op-amp. The LC tank has been designed with a 1 nH double-turn inductor having an estimated Q_L of 17 at 4 GHz. The frequency is tuned by a 5-bit coarse MOM capacitive bank, a 3-bit fine MOM capacitor bank, and an AMOS varactor for continuous tuning. The quality factor of the switched capacitance is approximately 55 at 4 GHz, resulting in an average tank-Q of 13. The switching pairs use standard 1.2 V devices with a length of 90 nm, since the oscillation amplitude cannot swing

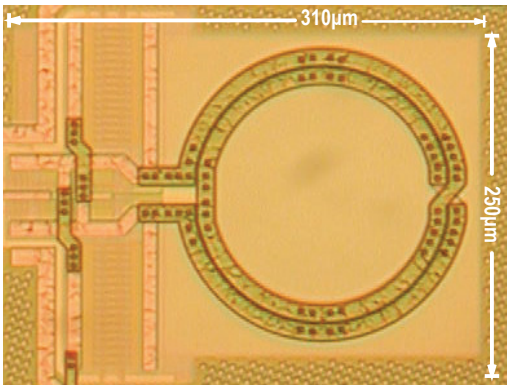

Fig. 5. Die photograph of the high-swing class-C VCO ($310\mu m \cdot 250\mu m$).

above the 1.2 V voltage supply. The PMOS width is twice the NMOS width, resulting in the same overdrive voltage. The reference current is provided off-chip for easy tunability, while the current mirror has a ratio of 1:8. The capacitance C_{tail} is 150 fF, a safe value to avoid instability of the oscillation amplitude. The op-amp is designed with a single differential stage, having a DC gain of 25-30 dB and a dominant pole at 25-50 MHz. Both DC gain and dominant pole can be changed acting on the op-amp bias current, which is controlled off-chip to allow an assessment of the VCO performance for different values of DC gain and bandwidth.

IV. Measurements

The VCO covers a tuning range of 1.1 GHz (28%) between 3.3 GHz and 4.4 GHz. The AMOS varactor has a continuous tuning range of 12 MHz, which covers 3 fine tuning steps for a robust frequency acquisition during PLL locking. Fig. 6 and Fig. 7 plot the phase noise measurements for a supply voltage of 1.2 V, using a V_{ref} of 600 mV and biasing the op-amp with 50 μA, which results in a DC-gain of 30 dB and a bandwidth slightly larger than 20 MHz according to simulations. The VCO yields the phase noise of -144 dBc/Hz (-142 dBc/Hz) at 10 MHz offset from 3.3 GHz (4.4 GHz), which extrapolates to -162 dBc/Hz at 20 MHz offset from 900 MHz, meeting the requirements of the GSM transmitter (albeit with no margin). The $1/f^3$ noise corner varies between 500 kHz and 800 kHz across the tuning range. The current consumption decreases from 2.5 mA to 1.8 mA with increasing oscillation frequency, for an estimated oscillation amplitude (peak, single-ended) of approximately 500 mV. The figure-of-merit (FoM, including

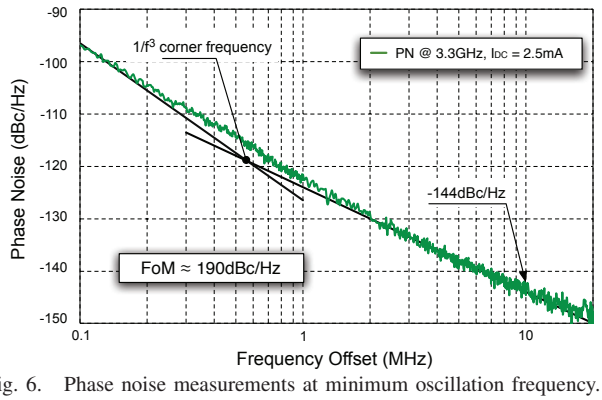

Fig. 6. Phase noise measurements at minimum oscillation frequency.

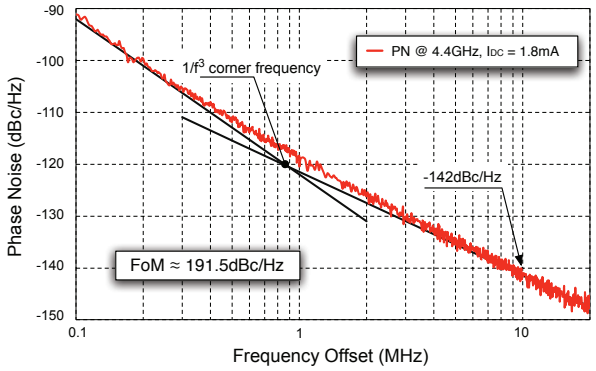

Fig. 7. Phase noise measurements at maximum oscillation frequency.

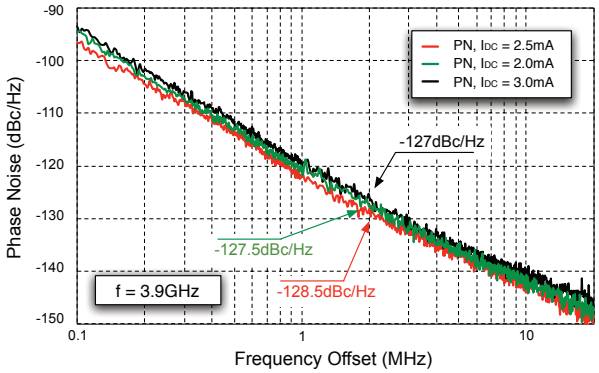

Fig. 8. Phase noise measurements at middle frequency vs current consumption.

the op-amp power consumption as well) is 190-191.5 dBc/Hz across the tuning range.

Fig. 8 displays the phase noise at the center frequency of 3.8 GHz vs. the current consumption. The VCO achieves its optimal phase noise performance for $I_{DC} = 2.5mA$. As long as $M1/M2$ work in class-C, the low-frequency noise from the op-amp and the MOS transistors has no impact on the phase noise, as expected; however, a larger I_{DC} pushes $M1/M2$ into the (deep) triode region, and the mentioned low-frequency noise contributions affect the phase noise via AM-to-PM conversion.

Fig. 9 shows the frequency pushing from the 1.2 V power supply. Pushing is very low at the lowest oscillation frequencies, and is always below 60 MHz/V across the tuning range.

Table I summarizes the VCO performance, comparing it to several published complementary class-B/C VCOs.

V. Conclusions

We have proposed a complementary class-C VCO that exhibits a high efficiency and a large oscillation amplitude together with a robust start-up. As a result, the fabricated 90 nm CMOS VCO displays a state-of-the-art phase-noise performance with a tuning range of 28%.

VI. Acknowledgements

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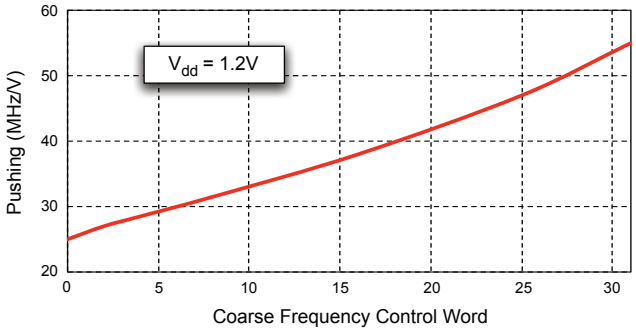

Fig. 9. Pushing from the voltage supply vs. coarse frequency tuning word.

TABLE I
Comparison with state-of-the-art complementary VCOs

	Technology	Frequency (GHz)	PN (dBc/Hz)	P_{DC} (mW)	FoM (dBc/Hz)
This work	90 nm	**3.3-4.4 (28%)**	**-130/-124 @2MHz**	**3.0-2.2**	**190-191.5**
[3]	180 nm	6.1-7.5 (20%)	-123/-120 @2MHz	2.2	189-191
[2]	350 nm	2.15-2.35 (9%)	-144 @3MHz	10	191.5
[10]	55 nm	6.5-9.0 (33%)	-135 @2MHz after div. by 2	36	185
[11]	65 nm	3.3-6 (58%)	-114/-109 @1MHz	0.7	187-180
[12]	45/32 nm	3.15-4.4 (33%)	-136/-133 @3MHz	23-16	186-183
[13]	90 nm	2.1-2.8 (28%)	-115@1MHz	1.2	183

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