Decision Feedback Equalizer (DFE) Behavioral Macro Model for Packaging System Eye Diagram Transient Simulations

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Abstract

Decision Feedback Equalizer (DFE) [1] is widely used in the high-speed packaging system as a part of receiver for recovering the signal from the distortion by the inter-symbol interference (ISI). Simulating the eye diagram at the receiver output after DFE is helpful to system designers especially in the case there is no longer an open eye diagram at the receiver input. Currently, particular simulation tools or particular algorithm implementations are required to support the modeling and simulation of the DFE function.

In this paper, a DFE behavioral macro model is proposed and tested. The proposed DFE behavioral macro model is an HSPICE circuit model and can be used directly in any existing conventional HSPICE compatible transient simulation tools.

We use a voltage controlled resistor and a capacitor to model the bit slicer (Symbol Detector) in DFE. The terminated ideal transmission lines with particular delays combined with voltage controlled voltage sources are used for modeling the Feedback Filter (FBF) part of DFE. The summer in DFE is modeled by Directional Junction [2]-[4].

The proposed DFE behavioral macro model can be easily combined directly with existing receiver behavioral macro models targeting other receiver behaviors such as the Mpilog receiver model [5] for accurate receiver input property modeling and the hyperbolic-tangent behavioral model[6] for accurate pre-amplifier/CTLE nonlinear modeling.

1. Introduction

As the signal bit rate of the electronic interconnect and packaging system increases, the inter-symbol interference (ISI) caused by the lossy channel makes the eye diagram at the receiver input node worse or even closed. Decision Feedback Equalization (DFE) is one of the effective techniques to recover the signal at the receiver side from the signal distortion by ISI. The eye diagram observed at the receiver input node is no longer enough for the packaging system performance evaluation. In some applications, we also have to simulate and observe the eye diagram after DFE (Fig.1).

Currently, the DFE function has been implemented as an algorithm in conjunction with the IBIS-AMI model [9] in some fast eye diagram simulation tools which are based on single-bit response convolution or statistic methods. These fast eye diagram simulation tools usually do not support general-purpose transient simulation. Most of them do not support accurate non-linear device models such as the time-variant impedance transmitter and the receiver with non-linear preamplifier.

In some applications with strong nonlinear I/O devices, we still need the transient simulation tools for packaging system eye diagram simulation. Since the IBIS-AMI is more like a protocol than a behavioral macro model, it can not be simply applied to a conventional transient simulation tool without corresponding algorithm implementation in the tool. To run a transient simulation on an electrical packing system with DFE, we may need to use the receiver transistor level model including the DFE part in a general-purpose transient simulation. However, the transistor-level receiver model including DFE is too complex and then too slow for direct application in the eye diagram transient simulations. Another issue is that usually the transistor level model including the DFE part is not available since it contains some IP information which the chip vendor may not want to release.

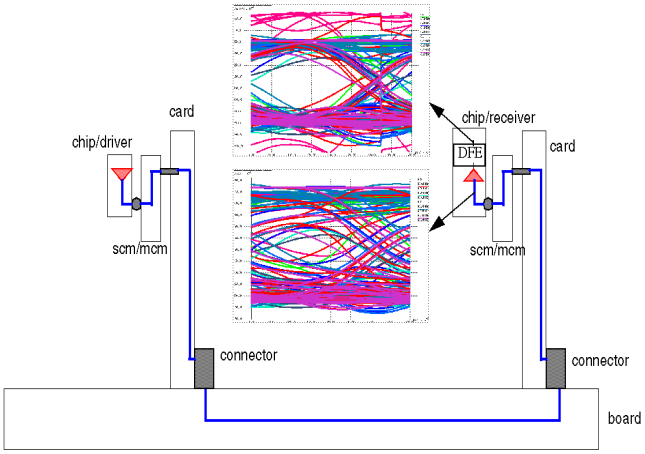

Fig.1 Observing the eye diagrams on electronic packaging signal transmission system before and after DFE.

Although it is possible to use a DFE post-processor to process the original waveform at receiver before DFE, it needs to store whole original waveform at receiver and perform a post-processing after the transient simulation. The post-processing approach is an un-convenient two-stage procedure. A real-time DFE embedded in the transient simulation without a post-processing tool is preferred and more convenient to most package system designers.

In this paper, we will discuss the principle and construction of a DFE behavioral macro model. The proposed model is an HSPICE circuit model and can be used directly in any conventional HSPICE compatible transient simulation tools, most of them are mature and with full range of model supporting and transient simulation capabilities. In the meantime, the behavioral macro model is much simpler and runs faster in transient simulation than the original transistor level model. The DFE function is processed in a real-time style through an HSPICE circuit model by the general-

purpose transient simulation tool without any requirement for implementing the DFE algorithms into the tool.

2. DFE Behavioral Macro Modeling

The block diagram of Decision Feedback Equalizer (DFE)[1] is shown in Fig.2. It includes a summer, a few slicers. The output of a slicer (Slicer i), except Slicer N, connects to the input of the next slicer (Slicer i+1), except the last one, and also feedbacks to the summer after multiplication by a coefficient h_i which can be optimally set according to the single bit response of the lossy channel. Node out1 is the output node at the summer and the location for observing the eye diagram after DFE. Node out2 is the node after the first slicer and a connecting node to the logic latch.

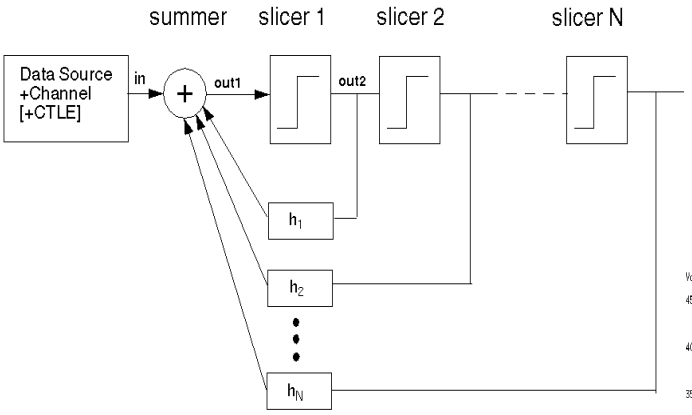

Fig. 2 Block diagram of DFE

In the following part, we will discuss how to make individual behavioral macro model for each component including the slicers and the summer with coefficient multipliers, and then combine them together to assemble the DFE behavioral macro model.

2.1 Slicer Behavioral Macro Model

Fig.3 is the schematic of the slicer behavioral macro model. The resistor R_{switch} is a voltage controlled resistor acting as a switch. A period independent voltage source V_{rc} controls the switch. When R_{switch} is turned to a small resistance value (the switch is turned on), the slicer samples the input signal V_{in}. The holding capacitor C_{hold} will be charged rapidly to V_{in}-V_{in}(DC) in about a time of $R_{low}C_{hold}<t_{sample}$ After a very short sampling time t_{sample}, R_{switch} turns to a very large resistance value (the switch is turned off) for a relatively long time $t_{hold}=t_{bit}$ - t_{sample} - t_{rise} - t_{fall}. The holding capacitor C_{hold} will hold the sampled voltage since the large time constant at the hold state ($t_{hold}<<R_{high}C_{hold}$) . The input-output behavior of the model is just like a real slicer by the function definition or by the transistor level model.

In all test cases of this paper, we use R_{high}=10000Ω, R_{low}=0.001Ω, C_{hold}=1nF, t_{bit}=0.4ns, t_{rise}=t_{fall}=2ps, t_{sample}=0.05t_{bit}=20ps>$R_{low}C_{hold}$., $R_{high}C_{hold}$=10μs>>t_{hold}=376ps. The above R,C, and t parameters can be fine tuned for optimal performance balance among the simulation result accuracy, simulation speed, and simulation stability. Please note t_{bit} of the switch controlling signal should be equal to the bit time of the system signal travelling in the packaging system signal channels. However, t_{rise} and t_{fall} are the rise and fall times of the switch controlling signal, they are usually different from the rise and fall times of the system transmission signal.

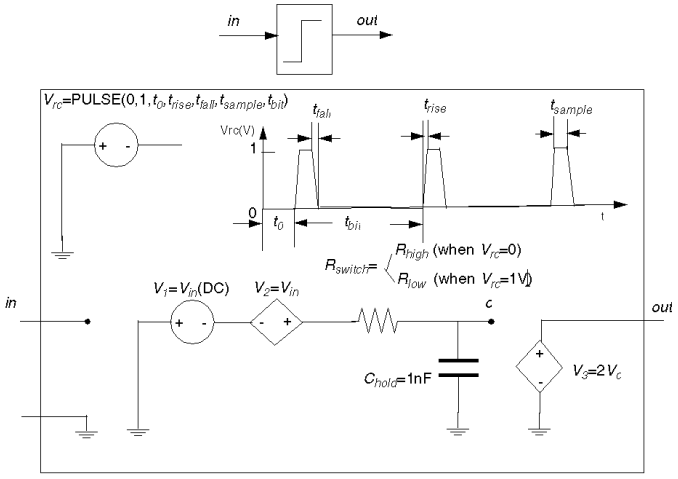

Fig.3 Slicer behavioral macro model

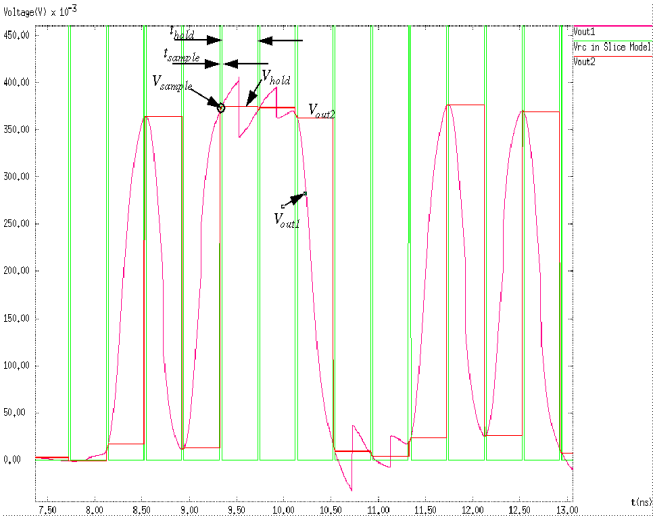

Fig.4 Sample and hold of a signal by a slicer macro model.

In this paper, the slicer behavioral macro model as shown in Fig.3 is used for representing the first slicer only. The other slicers are modeled by the ideal transmission lines, each with a delay time of (1-a)T_{bit}, (2-a)T_{bit}, etc. as shown in Fig.5, where a is parameter to adjust the sampling time point of the first slicer. In the test cases of paper, we use a=0.5. Since the waveform at the output node of each slicer is very close to a rectangular shape with one bit time delay to the previous slicer, using the ideal transmission line will be much simpler and more stable in the transient simulation.

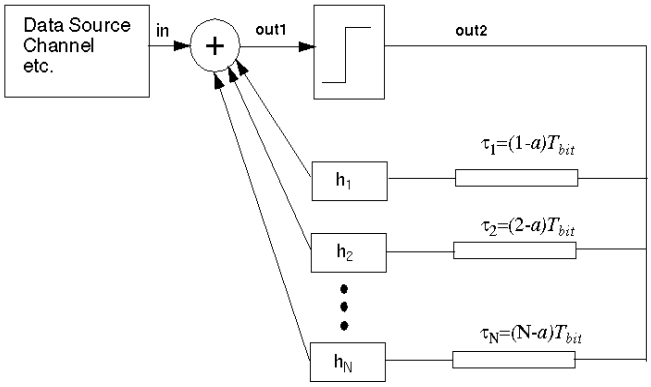

Fig.5 Ideal transmission lines in the DFE behavioral macro model to represent slicers other than the first one.

2.2 Summer Behavioral Macro Model

The (N+1):1 Directional Junction model is used to represent the summer as shown in Fig.6. The directional junction model was originally proposed and used in model combination [2] and crosstalk superposition [3]. The concept of directional junction is based on controlling forward and backward travelling waves, $V_{forward}$ and $V_{backward}$ with a reference impedance Z_0. Fig.6 shows the original block diagram and the corresponding behavioral macro model of the summer including the tap coefficient multipliers. To match the reference impedance of the directional junction, we put a resistor R_{bi} (i=1,2,…,N) at each voltage-controlled voltage source and double the voltage amplitude which already includes the coefficient h_i (the ith tap value, i=1,2,…,N). Fig.7 shows the 9:1 Directional Junction model in HSPICE format which is a part of the behavioral macro model in Fig.6.

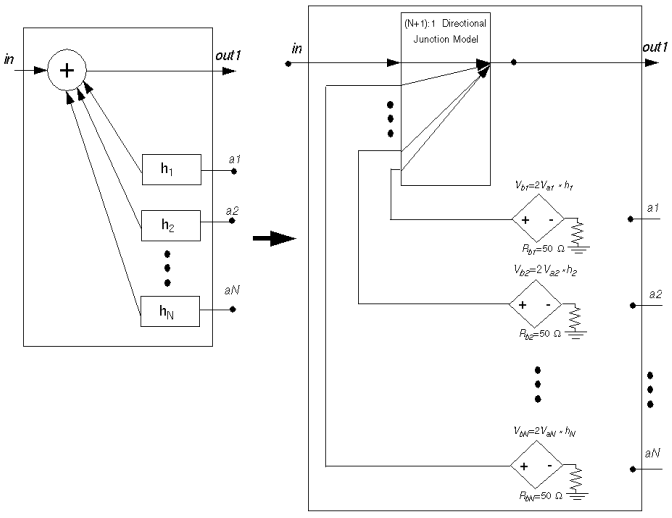

Fig.6 Block diagram and behavioral macro model of the summer with tap coefficient multipliers

```
.subckt djct9to1 out in1 in2 in3 in4 in5 in6 in7 in8 in9 ref
+ pz0=50.0
rout n0a ref pz0
rin1 n1a ref pz0
rin2 n2a ref pz0
rin3 n3a ref pz0
rin4 n4a ref pz0
rin5 n5a ref pz0
rin6 n6a ref pz0
rin7 n7a ref pz0
rin8 n8a ref pz0
rin9 n9a ref pz0
h01 n0a   n0a02 v1 pz0
h02 n0a02 n0a03 v2 pz0
h03 n0a03 n0a04 v3 pz0
h04 n0a04 n0a05 v4 pz0
h05 n0a05 n0a06 v5 pz0
h06 n0a06 n0a07 v6 pz0
h07 n0a07 n0a08 v7 pz0
h08 n0a08 n0a09 v8 pz0
h09 n0a09 n0b   v9 pz0
e01 n0b   n0b02 ref in1 1.0
e02 n0b02 n0b03 ref in2 1.0
e03 n0b03 n0b04 ref in3 1.0
e04 n0b04 n0b05 ref in4 1.0
e05 n0b05 n0b06 ref in5 1.0
e06 n0b06 n0b07 ref in6 1.0
e07 n0b07 n0b08 ref in7 1.0
e08 n0b08 n0b09 ref in8 1.0
e09 n0b09 n0c   ref in9 1.0
v0 n0c out 0.0
v1 n1a n1b 0.0
v2 n2a in2 0.0
v3 n3a in3 0.0
v4 n4a in4 0.0
v5 n5a in5 0.0
v6 n6a in6 0.0
v7 n7a in7 0.0
v8 n8a in8 0.0
v9 n9a in9 0.0
e11 n1b n1c ref out 1.0
h12 n1c in1 v0 pz0
.ends djct9to1
```

Fig.7 The 9:1 Directional Junction model in HSPICE format

2.3 Full-Rate DFE Behavioral Macro Model

The behavioral macro model for the whole DFE can be assembled by above mentioned macro models which are already in HSPICE or other SPICE-like formats.

The schematic of the assembled model for the full-rate DFE is shown in Fig.8. The corresponding circuit model in HSPICE format for supporting the applications up to 8 taps is shown in Fig.9. The HSPICE model can be easily extended to support more taps. The optimum tap coefficients h_1, h_2, …,, h_N can be obtained based on single bit response of the channel(Fig.10), or just taken from the original transistor level model if available. In the HSPICE model, the tap coefficients (ptap1(h_1),..,ptap8(h_8)) and other parameters like slicer switch on- and off-resistances, prl(R_{low}) and prh(R_{high}), slicer holding capacitance pcap(C_{hold}), signal bit time pWidth(t_{bit}), switch signal rise time to bit time ratio psamp1 (t_{rise} = t_{fall} = psamp1*pWidth), switch initial time psamp2(t_0) which should be adjusted according to the cursor time of the single bit response in the application t_0=T_c-mT_{bit}, m is an integer, so that $0<t_0<T_{bit}$, receiver input DC voltage pvdc(V_{in}(DC)) which should be adjusted according to the DC level at the eye diagram observing location in the application, and the slicer sampling delay parameter pa(a) can be over-written from a model call in the HSPICE main deck. Small modifications on the math equation format in the HSPICE model may be required for porting to any SPICE-like transient simulation tool other than HSPICE.

Fig 10 shows the single bit response before and after the optimal DFE by the transient simulation using the DFE behavioral macro model. We can see the Inter-Symbol Interference (ISI) is reduced significantly after DFE as we see much smaller overall tail values. Fig.11 shows the waveforms of a signal bit of "0101110001010…" before and after DFE. The recovered signal after DFE looks much better than the signal before DFE.

The proposed DFE behavioral macro model is based on the DFE algorithm, and realized by an HSPICE compatible circuit model. It can be generated before the transistor level model is available. This is a major difference from other

behavioral macro models like the Mpilog receiver macro model which is based on the original transistor level model.

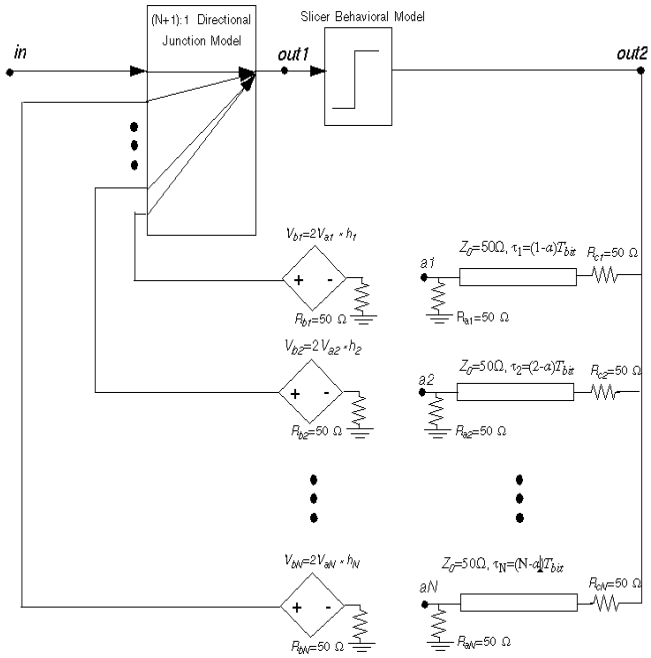

Fig. 8 Full-rate DFE behavioral macro model

```
.subckt dfe_macro_model_01 in out1 out2 ref
.param  psamp2=0.1207e-9
.param  psamp1=0.050
.param  pWidth=0.400e-9
.param  pvdc=0.2771736
.param  ptap1=0.2310
.param  ptap2=0.0923
.param  ptap3=0.0277
.param  ptap4=0.0286
.param  ptap5=0.0000
.param  ptap6=0.0000
.param  ptap7=0.0000
.param  ptap8=0.0000
.param  ptrb=0.002e-9
.param  pth=10000.0
.param  prl=0.001
.param  pcap=1000.0e-12
.param  pWidth1='pWidth*psamp1'
.param  pa=0.5
vrs rs ref PULSE(0.0 1.0 psamp2 ptrb ptrb pWidth1 pWidth)
ec1 con1 ref vol='v(in,ref)-pvdc'
gsw1 out1 con2 vcr pwl(1) rs ref 0.0v, 10000 1.0v, 0.001
cc1 con2 ref pcap
ec2 out2 ref vol='v(con2,ref)*2.0'
rcin1 out2 delayin1 50.0
rcin2 out2 delayin2 50.0
rcin3 out2 delayin3 50.0
rcin4 out2 delayin4 50.0
rcin5 out2 delayin5 50.0
rcin6 out2 delayin6 50.0
rcin7 out2 delayin7 50.0
rcin8 out2 delayin8 50.0

tl1 delayin1 ref delay1 ref z0=50.0 td='pWidth*(1.0-pa)'
tl2 delayin2 ref delay2 ref z0=50.0 td='pWidth*(2.0-pa)'
tl3 delayin3 ref delay3 ref z0=50.0 td='pWidth*(3.0-pa)'
tl4 delayin4 ref delay4 ref z0=50.0 td='pWidth*(4.0-pa)'
tl5 delayin5 ref delay5 ref z0=50.0 td='pWidth*(5.0-pa)'
tl6 delayin6 ref delay6 ref z0=50.0 td='pWidth*(6.0-pa)'
tl7 delayin7 ref delay7 ref z0=50.0 td='pWidth*(7.0-pa)'
tl8 delayin8 ref delay8 ref z0=50.0 td='pWidth*(8.0-pa)'
rdelay1 delay1 ref 50.0
rdelay2 delay2 ref 50.0
rdelay3 delay3 ref 50.0
rdelay4 delay4 ref 50.0
rdelay5 delay5 ref 50.0
rdelay6 delay6 ref 50.0
rdelay7 delay7 ref 50.0
rdelay8 delay8 ref 50.0
ed1 delay1a ref vol='-v(delay1,ref)*ptap1*2.0'
ed2 delay2a ref vol='-v(delay2,ref)*ptap2*2.0'
ed3 delay3a ref vol='-v(delay3,ref)*ptap3*2.0'
ed4 delay4a ref vol='-v(delay4,ref)*ptap4*2.0'
ed5 delay5a ref vol='-v(delay5,ref)*ptap5*2.0'
ed6 delay6a ref vol='-v(delay6,ref)*ptap6*2.0'
ed7 delay7a ref vol='-v(delay7,ref)*ptap7*2.0'
ed8 delay8a ref vol='-v(delay8,ref)*ptap8*2.0'
rd1 delay1a delay1b 50.0
rd2 delay2a delay2b 50.0
rd3 delay3a delay3b 50.0
rd4 delay4a delay4b 50.0
rd5 delay5a delay5b 50.0
rd6 delay6a delay6b 50.0
rd7 delay7a delay7b 50.0
rd8 delay8a delay8b 50.0
xdj1 out1 con1 delay1b delay2b delay3b delay4b
+      delay5b delay6b delay7b delay8b ref djct9to1
.ends   dfe_macro_model_01
```

Fig.9 Eight-tap full-rate DFE behavioral macro model in HSPICE format

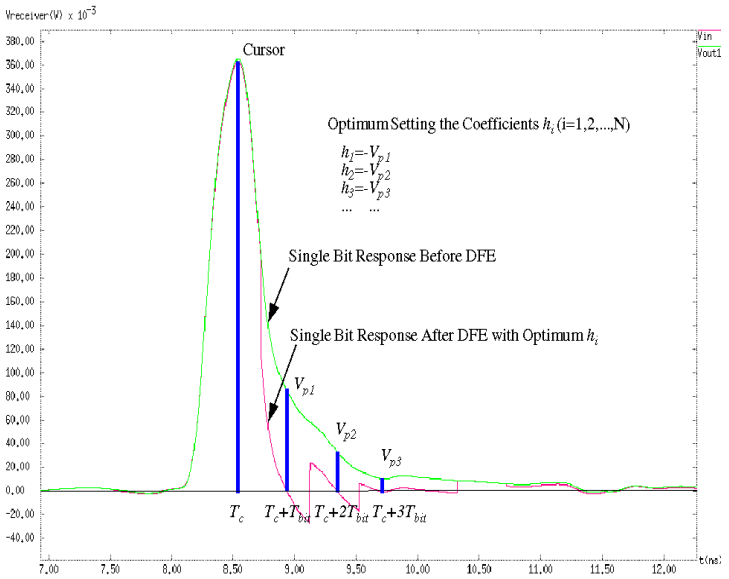

Fig.10. Single bit response before and after DFE

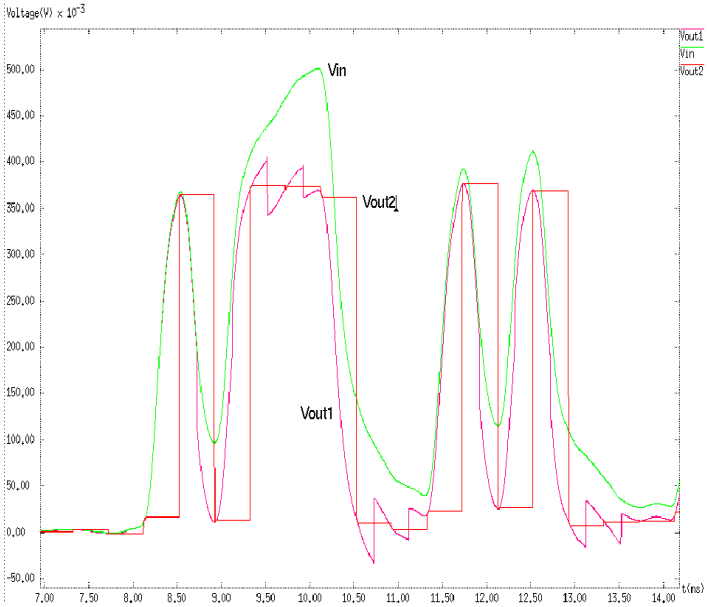

Fig.11 Signal Waveforms before and after DFE in a test case

2.4 Half-Rate DFE Behavioral Macro Model

The DFE behavioral macro model can be used not only for the full-rate DFE but also for the half-rate DFE[7] which allows larger slicer device delay in real hardware. In the half-rate DFE, the input signal bits are split into two output bit groups, the odd bits and the even bits. Just apply the same method to a different block diagram for the half-rate DFE, we can make the half-rate DFE behavioral macro model as shown in Fig.12. This model can be used in transient simulation to observe both even- and odd-bit eye diagrams separately after the half-rate DFE.

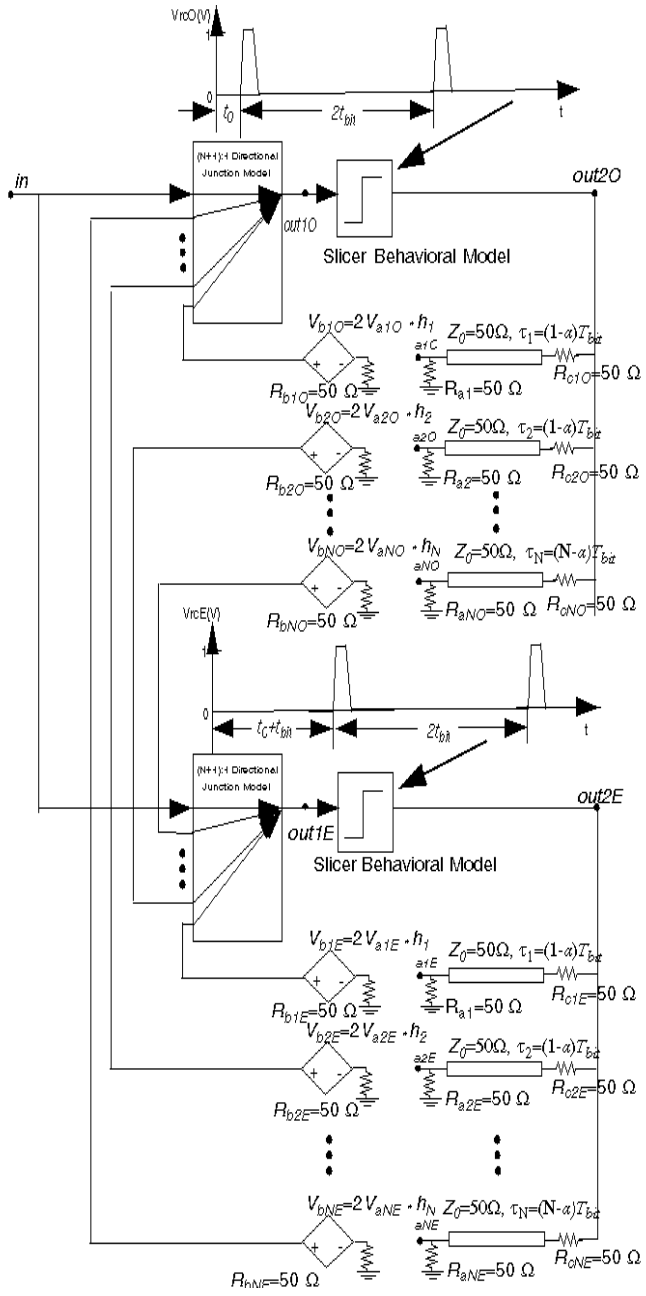

Fig.12 Half-rate DFE behavioral macro model

Fig.14 shows single bit responses at the receiver input and the CTLE/pre-amplifier output with nonlinear effects. The one with nonlinear effects has little ISI. It looks like the benefit from DFE will be very small if the DFE is placed after a non-linear pre-amplifier.

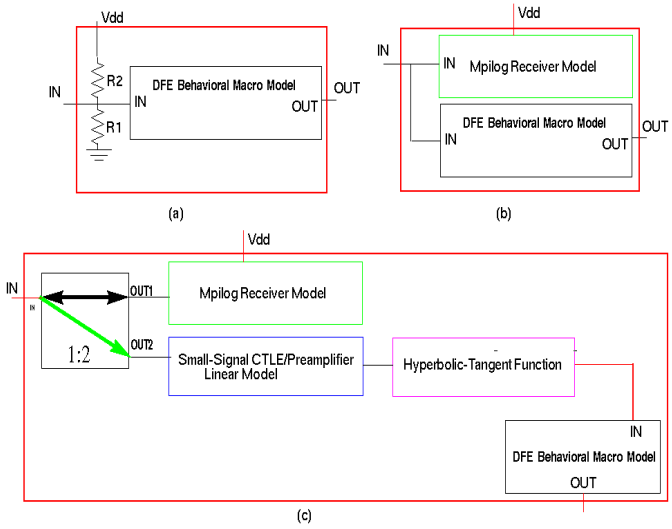

Fig.13 Receiver behavioral macro models by combining other receiver macro models and the DFE macro model

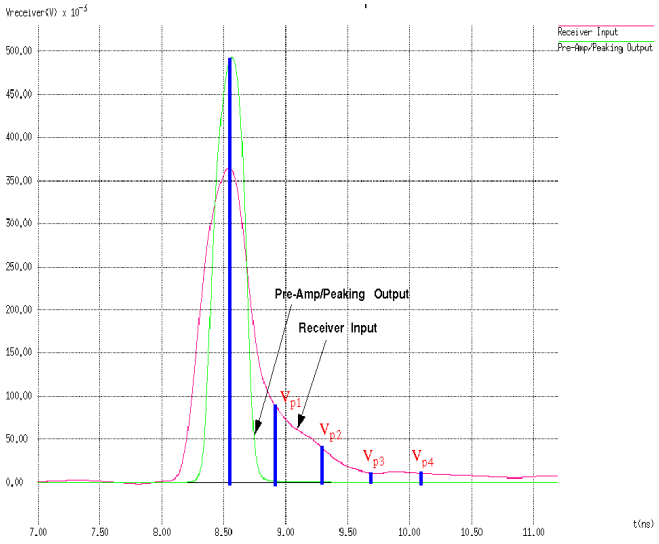

Fig.14 Single bit responses at the receiver input and the CTLE/ pre-amplifier output with nonlinear effects

2.5 Receiver Behavioral Macro Model

The input impedance of this DFE behavioral macro model is infinity. It can be attached directly to any existing receiver models to assemble a full receiver behavioral macro model including DFE, without any interference problem. The existing receiver model (without DFE) can be the lumped RC loading(Fig.13(a)), the Mpilog model(Fig.13(b)), the small signal S-parameter model or lumped model for the passive Continuous Time Linear Equalizer (CTLE), and the non-linear preamplifier macro model(Fig.13(c)) by the Hyperbolic-Tangent Function [6], or any combination of them according to the real configuration of the receiver and the application accuracy requirement.

3. Applications

The DFE behavioral macro model can be applied directly in the practical packaging system transient simulations as the DFE part of the full receiver behavioral macro model as described in 2.5.

We tested the proposed DFE behavioral macro model in a signal bus of an IBM eServer packaging system. The signal starting from the driver travels through a ceramic package, a module-to-card connector, a card with low-loss material, a card-to-card connector, another card with low-loss material,

another module-to-card connector, and another ceramic module to the receiver. The signal bit time is 0.4ns.

An ideal driver model with 40 Ω internal impedance and 1.1V voltage is used in the testing with a rise and fall time of 50ps. The Mpilog receiver model is used to represent the real receiver input properties.

The card wire models are made by CZ2D[11], an IBM quasi-static 2D electromagnetic simulation tool, using the frequency dependent ε_r and tanδ and taking into account the skin effect of the conductor. All other packaging component models are provided by the IBM eServer modeling team by using the full-wave 3D electromagnetic simulation tools[11][12].

The S-parameters of the channel from the driver C4 location to the receiver C4 location are obtained by cascading all individual packaging component S-parameter models. IdEM Plus[10] is used to make the channel SPICE model from the channel S-parameter model.

We tested the proposed DFE behavioral macro model on a signal channel under two different crosstalk scenarios, one without crosstalk, the other with eight crosstalk aggressors in the transient simulations by PowerSPICE, an IBM internal circuit transient simulation tool, and HSPICE[13], a popular commercial circuit simulation tool, for eye diagram at the receiver. In the DFE behavioral macro model, we used four taps for all examples shown in this paper by setting the last four taps in the eight-tap HSPICE behavioral macro model to zero.

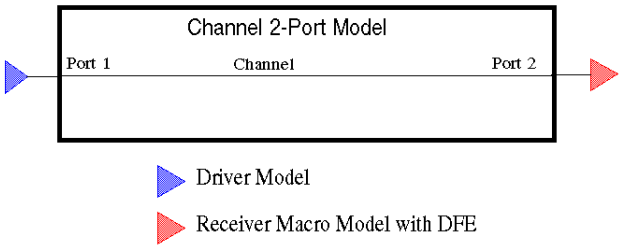

Fig.15 A Signal channel model without crosstalk from the nearby channels

Firstly, we tested a signal channel in the above mentioned IBM e-Server packaging system without crosstalk from the nearby channels (Fig.15). We used a conventional random signal with about 140 bits. The comparison of the eye diagrams before and after optimal full-rate DFE is shown in Fig. 16. The eye diagram after the CTLE/pre-amplifier without DFE is also shown for comparison. We can see that DFE results in better eye opening on both vertical and horizontal criterions.

The CPU time of the PowerSPICE simulation on an AIX workstation is 237s with the eight-tap DFE behavioral macro model, and 139s if not using the DFE behavioral macro model. It is possible to reduce the CPU time by fine tuning the R,L, and t parameters in the slicer behavioral macro model.

The simulated even- and odd-bit eye diagrams after a half-rate DFE are shown in Fig.17 by using the proposed half-rate DFE behavioral macro model. The odd-bit eye diagram opens widely than even-bit at the second eye position (the odd-bit eye position), while the even-bit eye diagram opens widely than the odd-bit at the first eye position (the even-bit eye position).

Secondly, we tested the same channel but taking into account the crosstalk from eight nearby aggressor channels (Fig.18) by the worst-case eye diagram algorithm[8] using a 12-bit worst-case signal pattern search on the victim net, and a 10-bit worst-case crosstalk signal pattern search on all 8 aggressors. For the worst-case eye diagram transient simulation, we use the same worst-case eye search method as in [8] by using the receiver input node waveform to search the worst-case eye diagram (Fig.19). After obtaining the worst-case victim and aggressor signal patterns based on a 25% crosstalk sampling window width, we use the worst-case signals after the alignment [8] to simulate the worst-case eye diagrams. At this final stage of the worst-case eye diagram simulation precedure, we apply the proposed DFE behavioral macro model for observing the corresponding eye diagram after DFE (Fig.20).

Fig.16 Eye diagrams before (upper eye diagram) and after (middle eye diagram) the full-rate optimal DFE, and another one after the CTLE/pre-amplifier without DFE.

The applications show that the proposed DFE behavioral macro model is easy to use with good convergence property in the transient simulation, and reflects the DFE effect correctly.

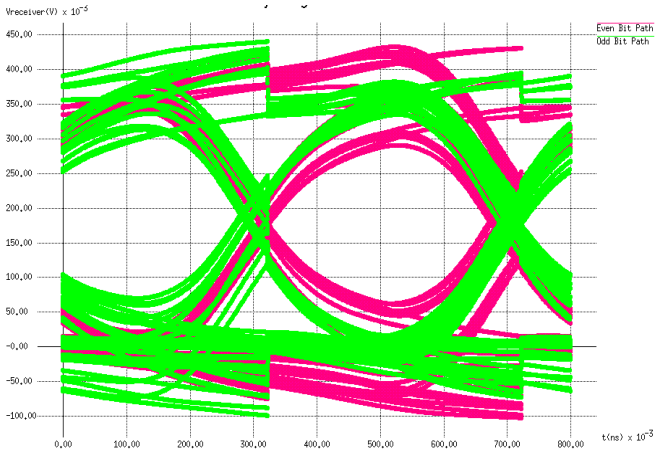

Fig.17 Even- and odd-bit eye diagrams after a half-rate DFE

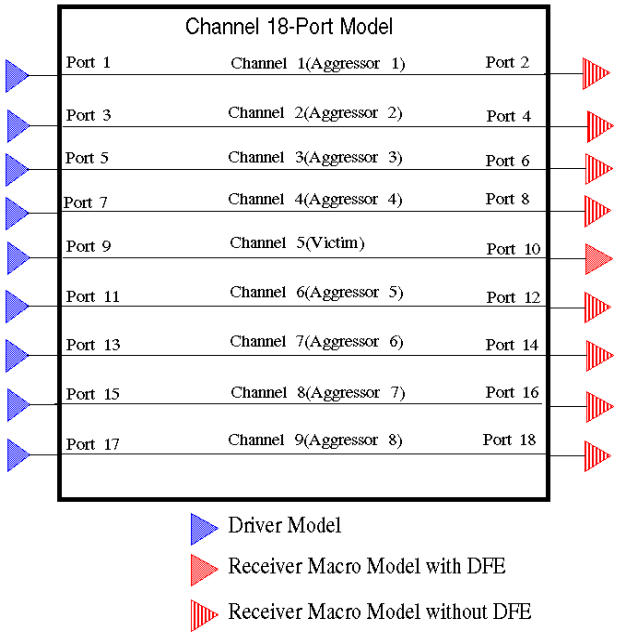

Fig.18 A signal channel with 8 nearby crosstalk aggressors

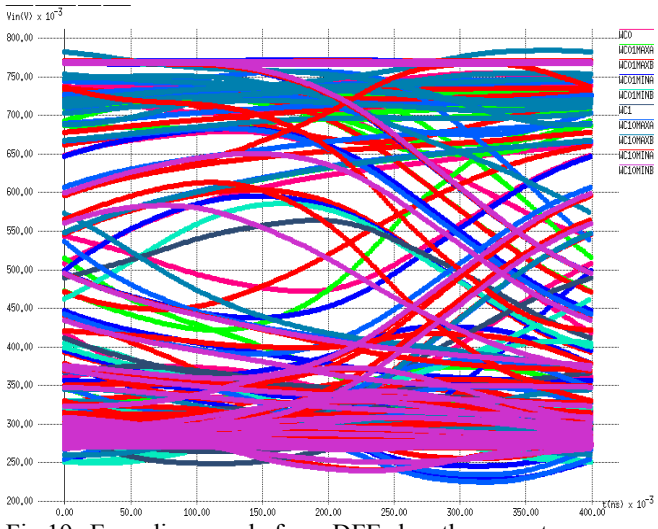

Fig.19 Eye diagram before DFE by the worst-case eye diagram algorithm applied at the receiver input node

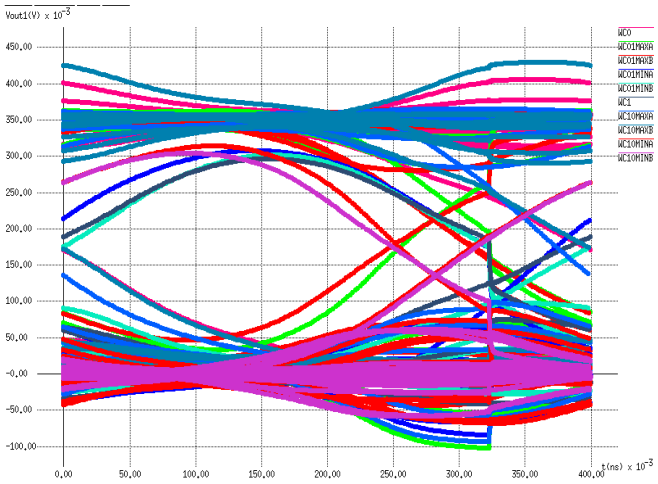

Fig.20. Corresponding eye diagram of the Fig.19 case after DFE by the proposed DFE behavioral macro model

Conclusions

A DFE behavioral macro model has been proposed and tested. The proposed DFE behavioral macro model is an HSPICE circuit model and can be used directly in any existing conventional HSPICE compatible transient simulation tools for the real-time display of the receiver signal after DFE.

The proposed DFE behavioral macro model is based on the DFE algorithm and can be easily combined directly with existing receiver behavioral macro models targeting other receiver behaviors such as the Mpilog receiver model, the small signal peaking filter with the Hyperbolic-Tangent nonlinear pre-amplifier model, etc.

The applications of the proposed behavioral DFE macro model in the conventional random pattern eye diagram transient simulation and the worst-case eye diagram transient simulation have been tested and shown on an IBM eServer electronic packaging system.

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