Chapter 2 Layout Design Rules

- Layout Design Rules
- Definition of Layout Rules
- Stick Diagram
- Euler Path
- CMOS Inverter Layout

Layout Design Rules

- a prescription for preparing the photomasks that are used in the fabrication of integrated circuits.
- a set of specification for the mask patterns used in the layout and provide geometry information such as the minimum width and spacing for each layer.
- provide a necessary communication link between circuit designer and process engineer during the manufacturing phase.
- obtain the circuit with option yield in an small a geometry as possible without compromising reliability of the circuit

Layout Design Rules

- Compromise between performance and yield

  - the more conservative the rules are, the most likely it is that the circuit will function.
  - the more aggressive the rules are, the greater the probability of improvements in circuit performance, this improvement may be at the expense of yield.

The design rules primarily address two issues :

1. The geometrical reproduction of features that can be reproduced by the mask masking and lithography process.
2. The interaction between different layers.

Physical Basic of Design Rules

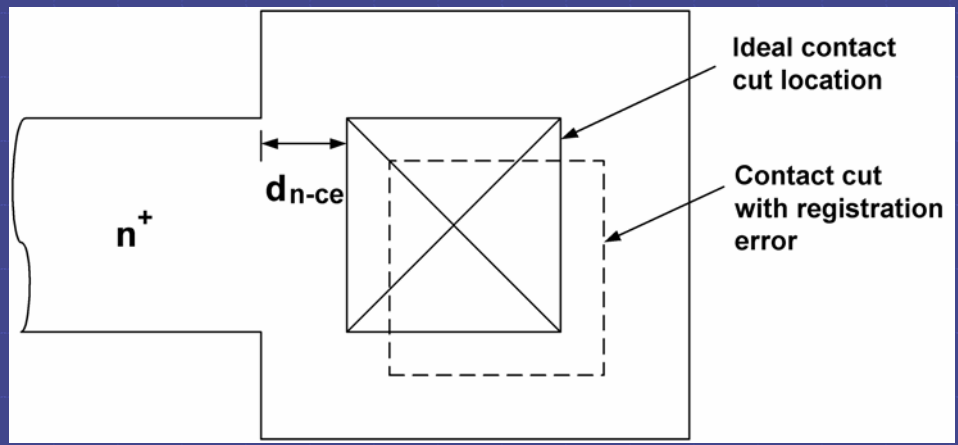
- limitation of lithography
- physics of the process flow
- electrical characteristics of the final structure

Minimum line width

- limitation on the lithographic resolving power.
- if the line width are made too small, it is possible for the to be discontinuous.

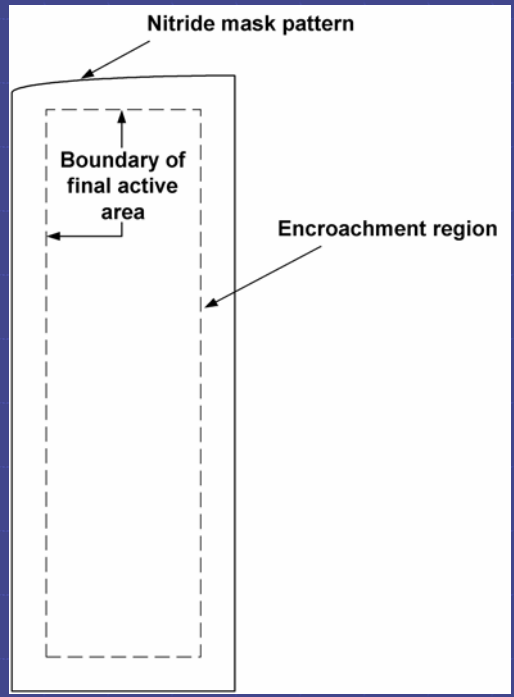
Minimum Spacing

- lines on a given layer also tend to originate form the lithography
- if the wire are placed two close, it is possible for them to merge together.
- lines on different layers : restriction arises because the layers must be stacked to form devices
- spacing between lines of different layers are chosen to compensate for misalignment or registration errors in the layering process, thus a registration tolerance must be allowed.



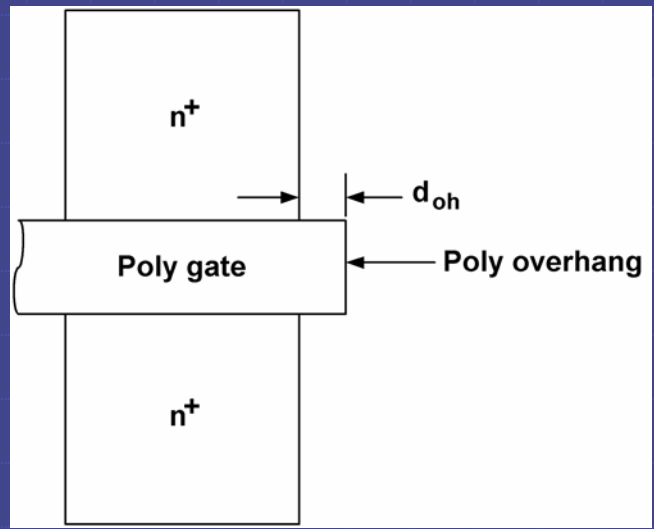
Active Area Definition in a LOCOS Process

- active area encroachment induced by the formation of the bird's beak requires that the nitride mask dimensions be layer than the final active area.



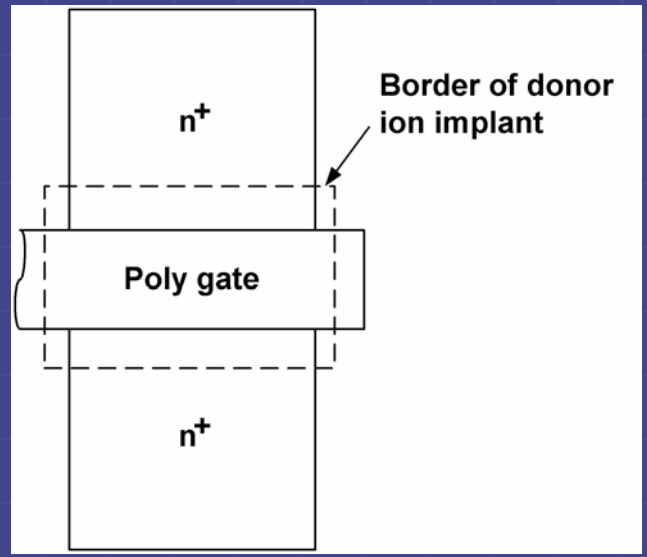
Poly gate overhang distance

- ensure that the source/drain region will be separated in the event of a misalignment between the active area and the poly mask.

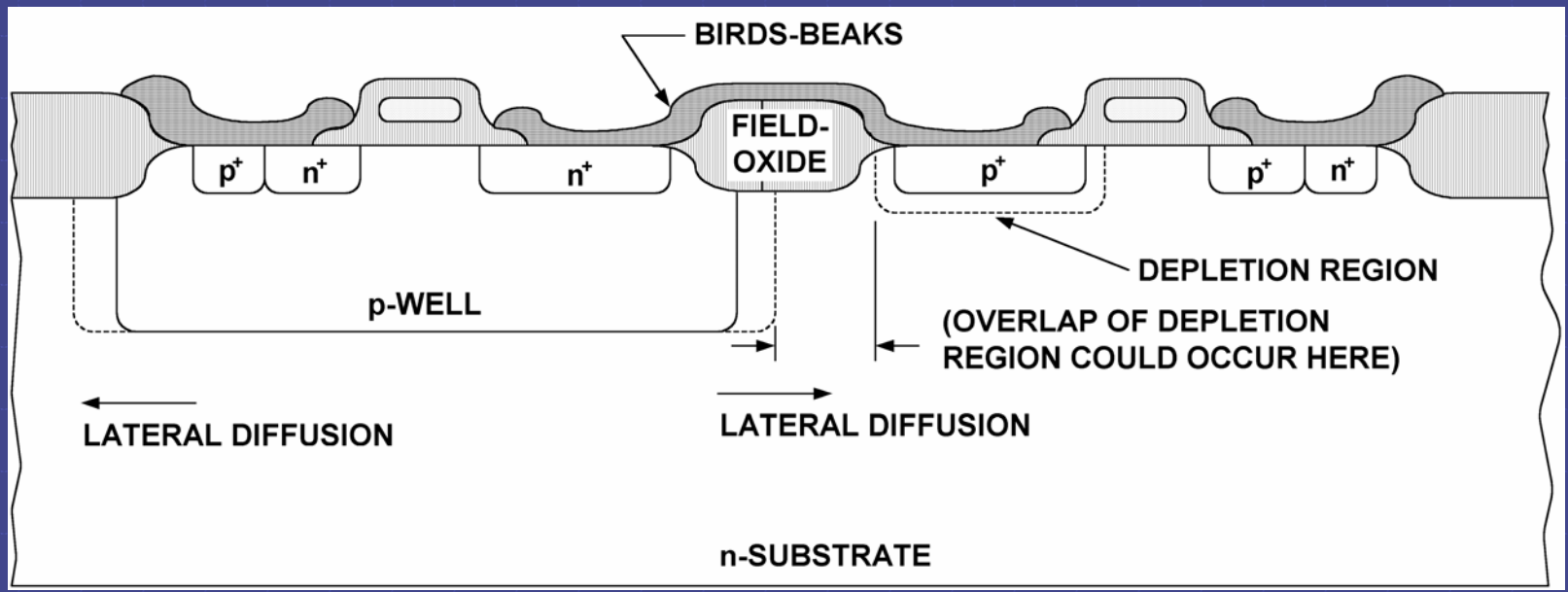


Implant in a Depletion-Mode MOSFET

- The implanted region must be large than the device active area to ensure that it misalignment occurs.



Well rules



Well Rules

- the well is usually a deeper implant compared width the transistor source/drain implant, therefore it is necessary for the outside dimension to provide sufficient clearance between the n-well and the adjacent different region.
- the inside clearance is determined by the transition of the yield oxide across the well boundary, " bird's beak " effect.
- to avoid shorten condition, active region is not permitted to across a well boundary.
- sheet resistance of well is about several kΩ/□, it is necessary thoroughly contact the well to VDD or VSS, this will prevent excessive voltage drops due to substrate current.

Transistor Rules

- where poly crosses active, the source and drain diffusion is masked by the region, the source, drain, and channel are therefore self-aligned to the gate.
- poly is necessary to extend beyond the edges of the diffusion region to the drain and source will not be shorted.
- poly and active region that do not meet intentionally to form a transistor should be kept separated.
- two of implant/diffusion layers to form the p- and n-transistor.

Contact Rules

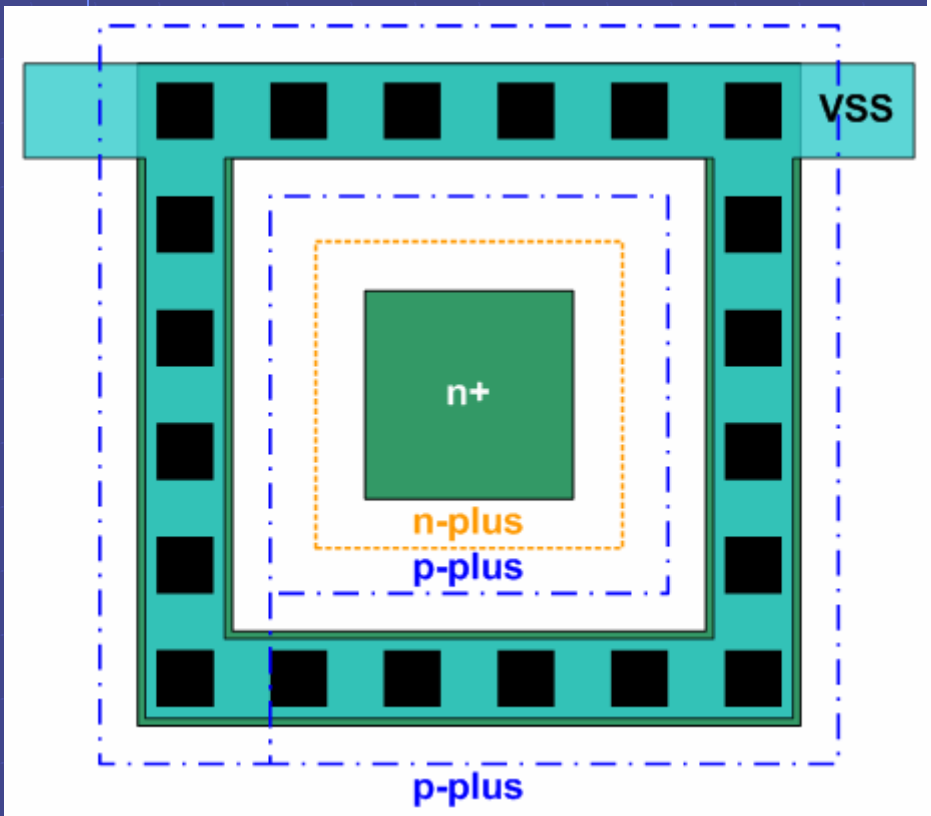
- metal to p-active (p-diffusion)
- metal to n-active (n-diffusion)
- metal to polysilicon
- VDD and VSS substrate contacts
- split (substrate constant)

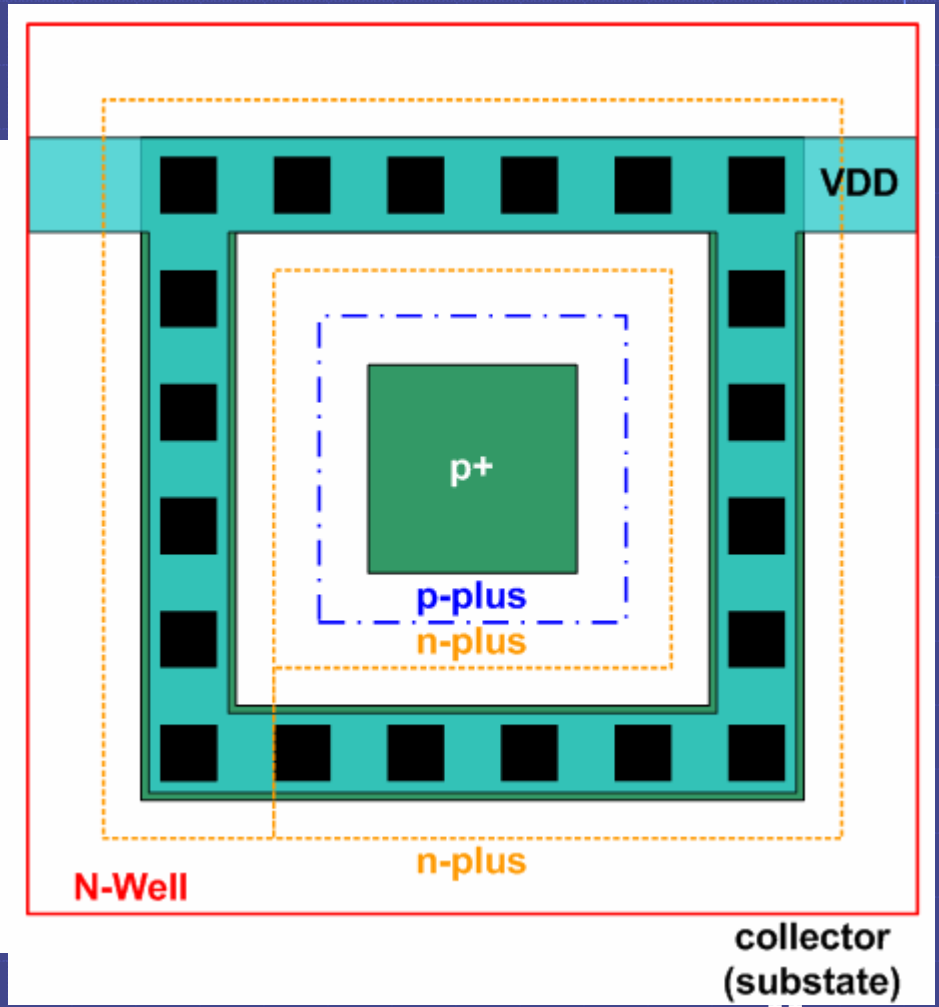
- ❖ depending on process, “buried contact” (poly-diffusion) maybe allowed. Ex : NMOS process, SRAM process.
- ❖ each isolated well must be tied to the appropriate supply voltage.
- ❖ the split or merge (butting) contact is equivalent to two separate metal-diffusion contacts that are strapped together with metal.

Layout Design Rules

Guard Ring

p+ diffusion in the p-substrate (p-well) and n+ diffusion in the n-well are used to collect injected minority carriers. n+ guard rings tied to V_{DD}. p+ guard rings tied to V_{SS}.





Metal1 rules

- metal spacing may vary with the width of the metal line (so-called fat-metal riles), this is due to etch characteristics of small versus large metal wires.
- some process require a certain proportion of the chip area to be covered with metal.

Via rules

- process may vary in whether they allow via to be placed over poly and diffusion.
- some process allow via to be placed within these areas but not allow the via to straddle the boundary of poly or diffusion, this results from the sudden vertical topology variations that occur at sublayer boundaries.

Metal2 rules

- the possible increase in width and separation of 2nd level metal are conservative rules to ensure against broken conductor or shorts between adjoining wire due to vertical topology.
- modern processes frequency have the metal1 and metal2 pitches identical.

Via2 rules

- similar to 1st via, the rules for placement of via2 may vary with process.

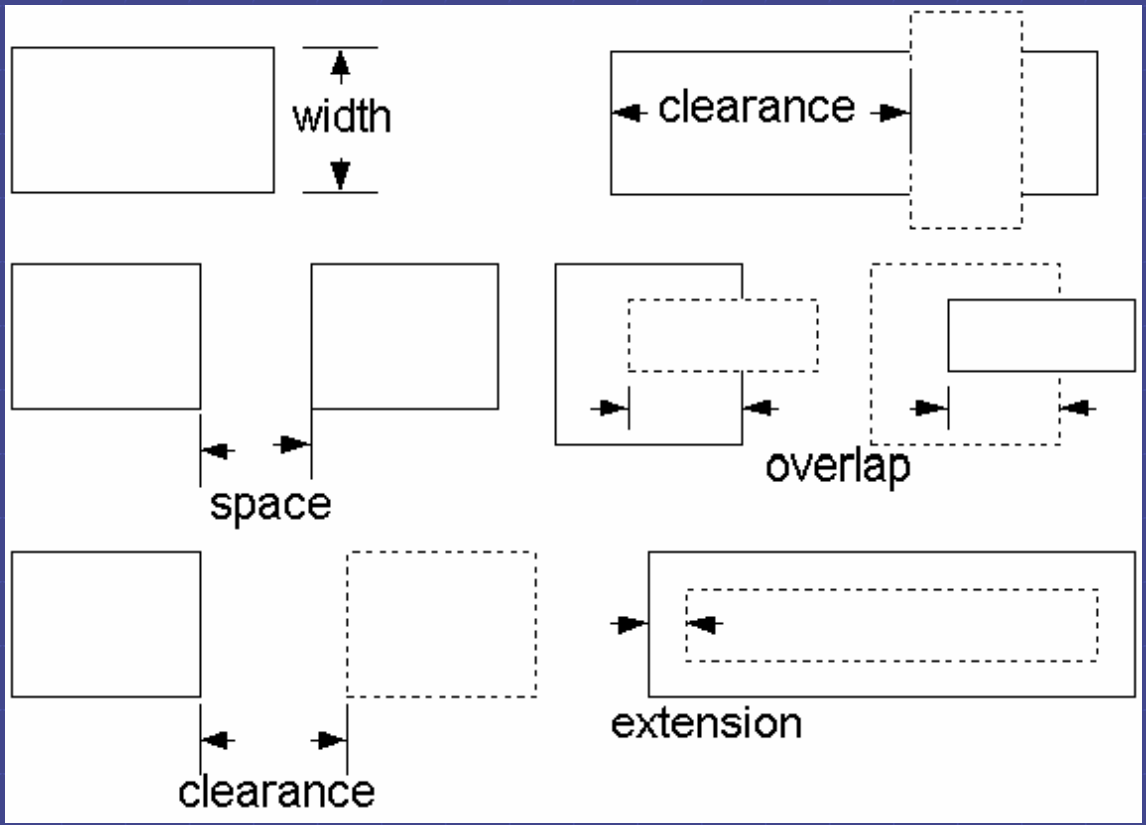
Metal3 rules

- the rules usually but not always increase in width and separation over metal2.
- metal3 is generally need primarily for power-supply connections and clock distribution.

Passivation or overglass

- this is a protective glass layer that covers the final chip, opening are required at pads and any internal test points.

Definition of the layout layers



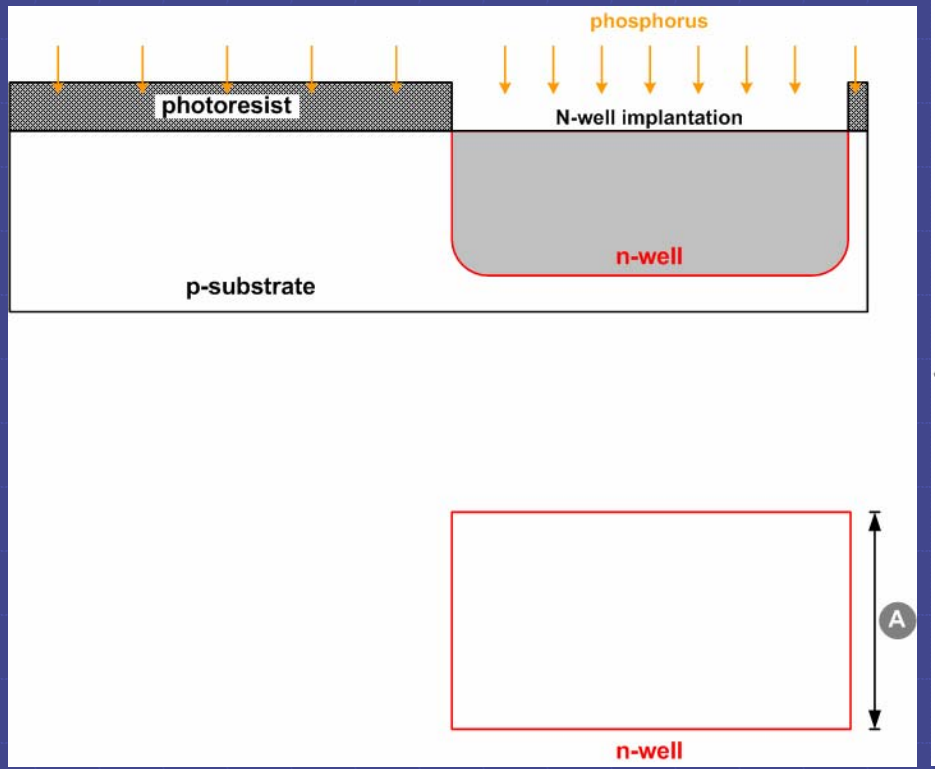
“Line of Diffusion” Rule

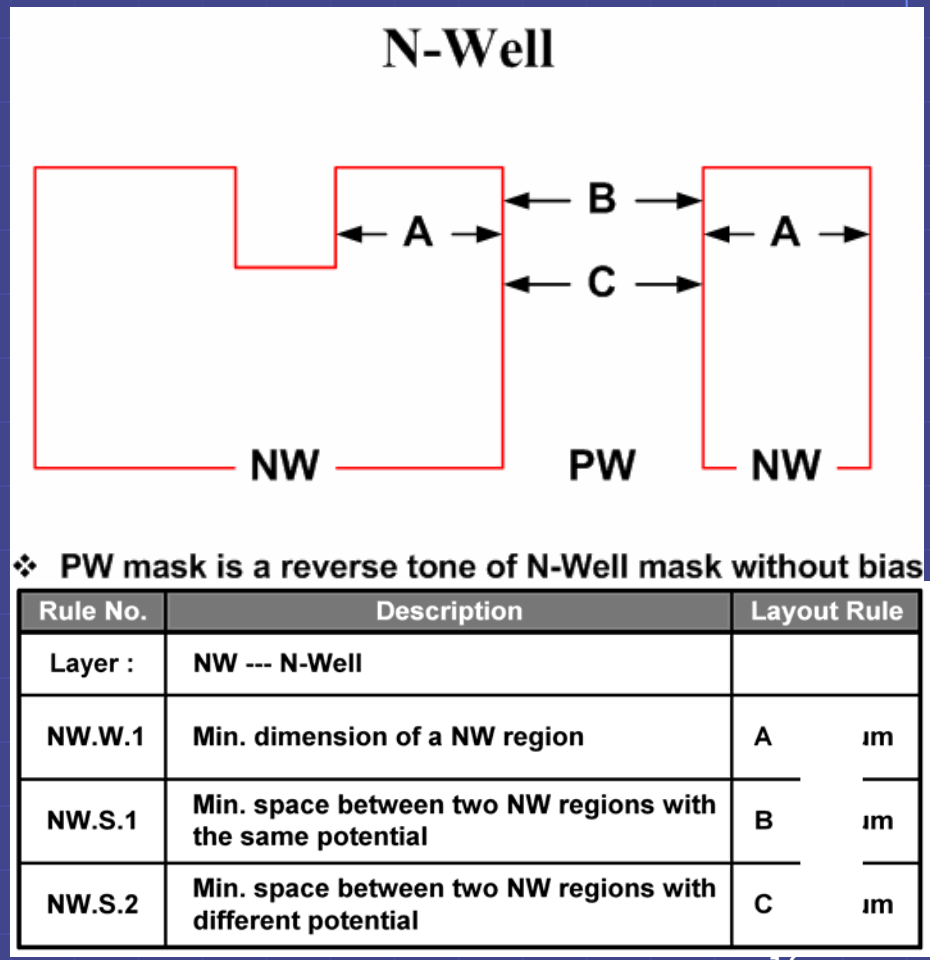
- The transistors from a line of diffusion intersected by polisilicon gate connections.
- The CMOS circuit is converted to a graph where

  (1) The vertices in the graph are the source/drain connections.

  (2) The edges in the graph are transistors that connect particular source-drain vertices.
- Two graphs, one for the n-logic tree and one for the p-logic tree result.
- The connection of edges in the graph mirror the series-parallel connection of gate signal name for that particular transistor.

N-Well
Cross-Sectional & Layout View

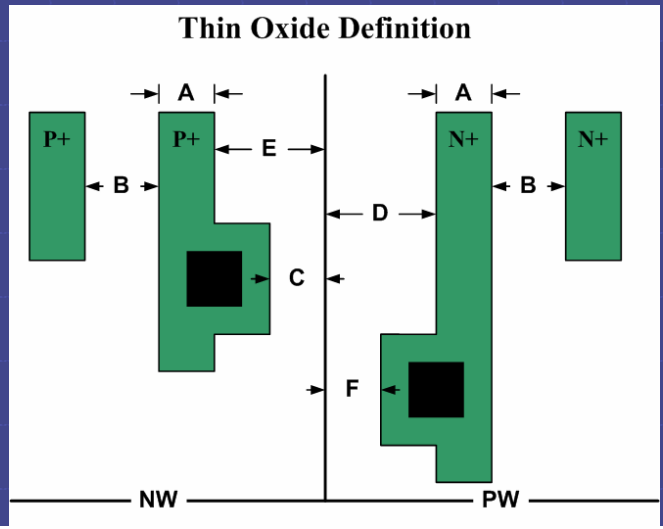


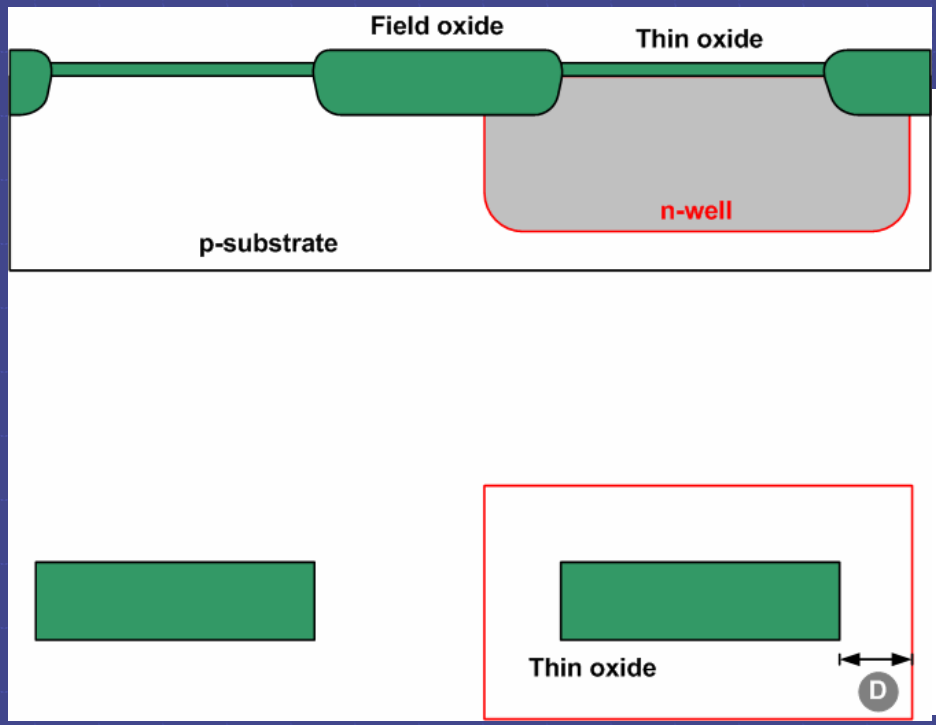


❖ PW mask is a reverse tone of N-Well mask without bias

Rule No.	Description	Layout Rule
Layer :	NW --- N-Well	
NW.W.1	Min. dimension of a NW region	A ım
NW.S.1	Min. space between two NW regions with the same potential	B ım
NW.S.2	Min. space between two NW regions with different potential	C ım

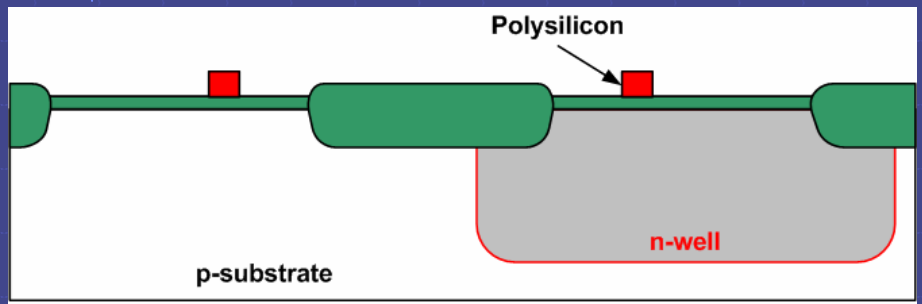
Thin Oxide
Cross-Sectional & Layout View

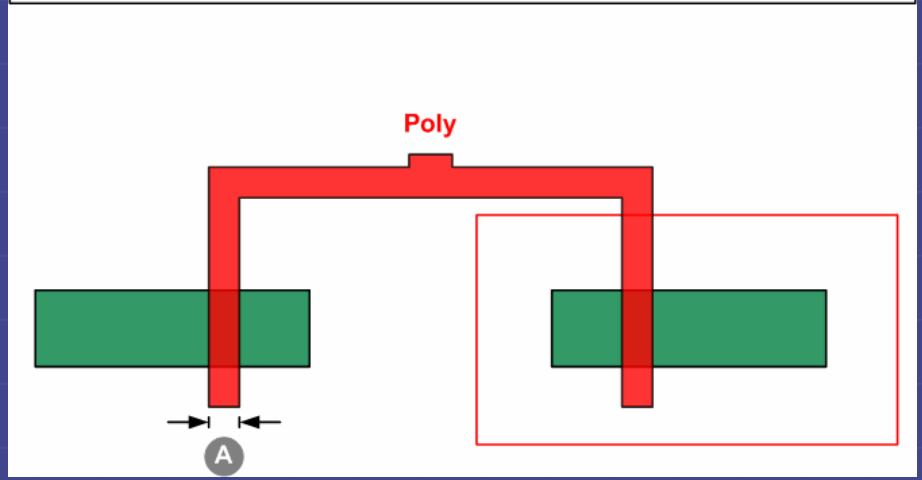


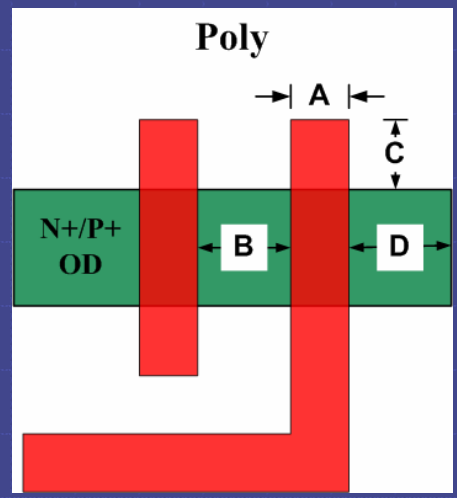


Rule No.	Description	Layout Rule	
Layer :	OD --- Thin Oxide Definition		
OD.W.1	Mini. width of an OD region	A	um
OD.S.1	Mini. space between two OD regions	B	um
OD.C.1	Mini. clearance from NW edge to a N+ OD region which is inside the NW	C	um
OD.C.2	Mini. clearance from NW edge to a N+ OD region which is outside the NW	D	um
OD.C.3	Mini. clearance from NW edge to a P+ OD region which is inside the NW	E	um
OD.C.4	Mini. clearance from NW edge to a P+ OD region which is outside the NW	F	um

Ploy
Cross-Sectional & Layout View

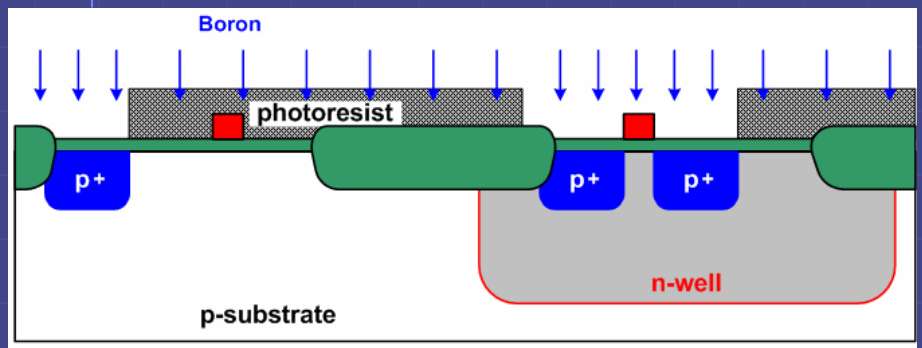


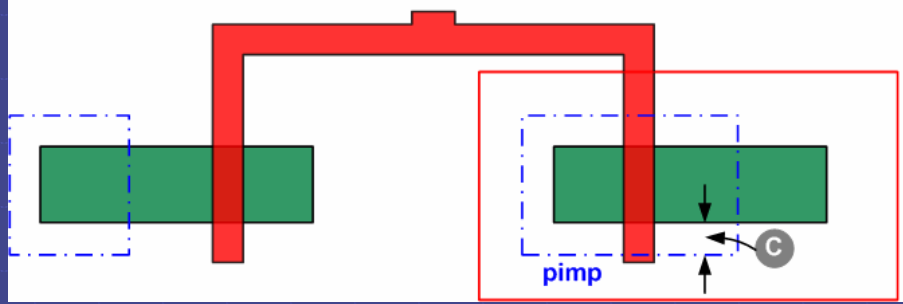


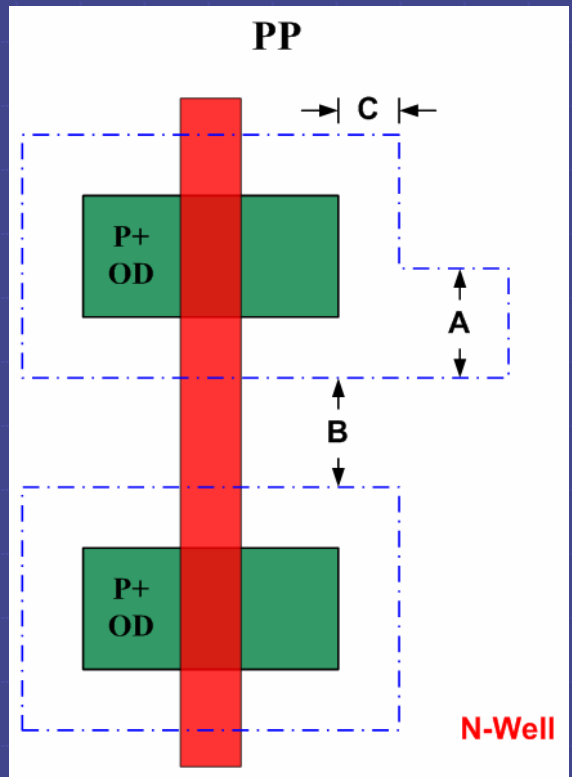


Rule No.	Description	Layout Rule
Layer :	PO --- Poly Si	
PO.W.1	Min. width of a PO region for the channel length	A um
PO.S.1	Min. space between two PO regions on OD area	B um
PO.O.1	Min. overlap of a PO region extended into field oxide (endcap)	C um
PO.C.1	Min. clearance from a PO gate to a related OD edge	D um

P+ Implant
Cross-Sectional & Layout View

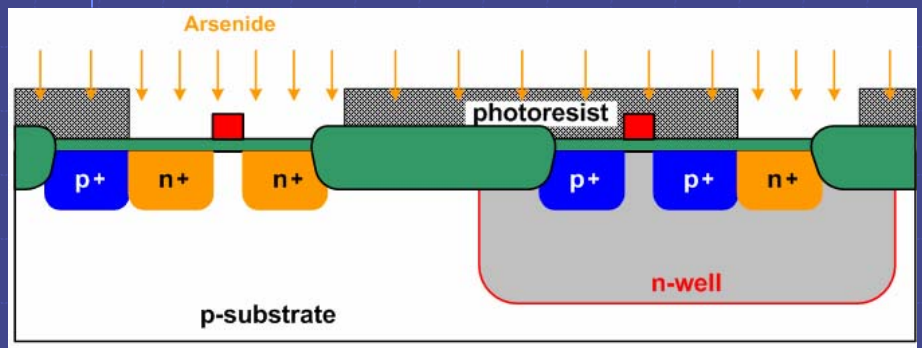


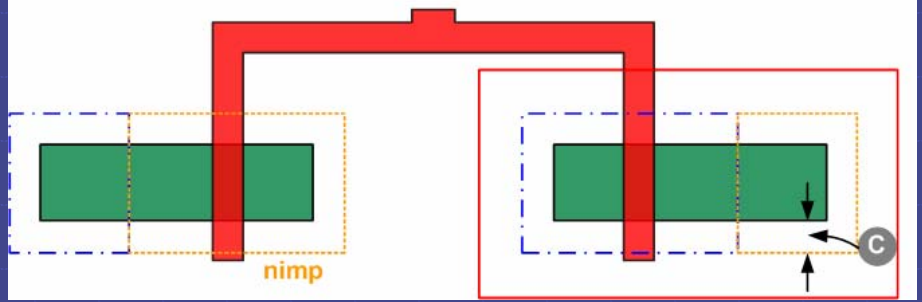


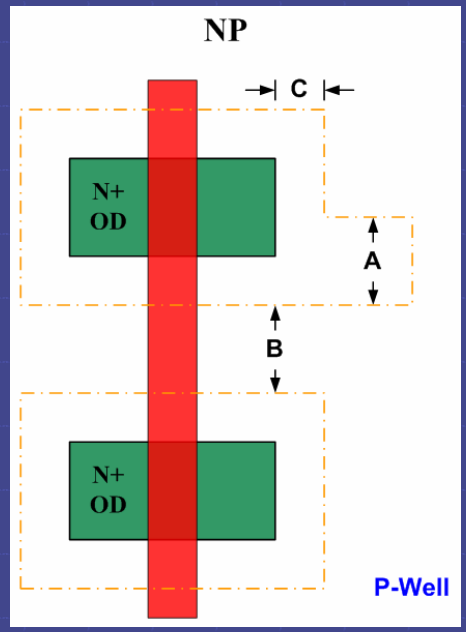


Rule No.	Description	Layout Rule
Layer :	PP --- P+ Implantation	
PP.W.1	Min. width of a PP region	A um
PP.S.1	Min. space between two PP regions	B um
PP.E.1	Min. extension of a PP region beyond a PP active OD region	C um

N+ Implant
Cross-Sectional & Layout View



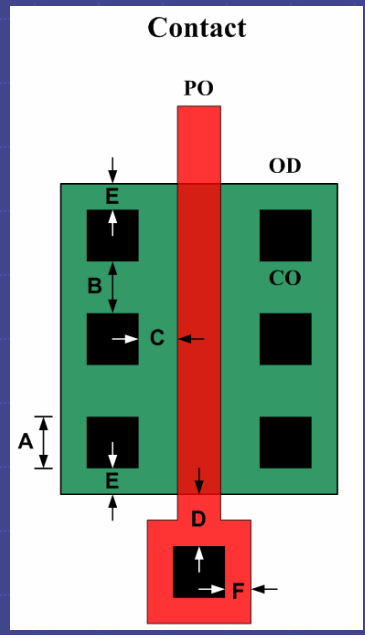


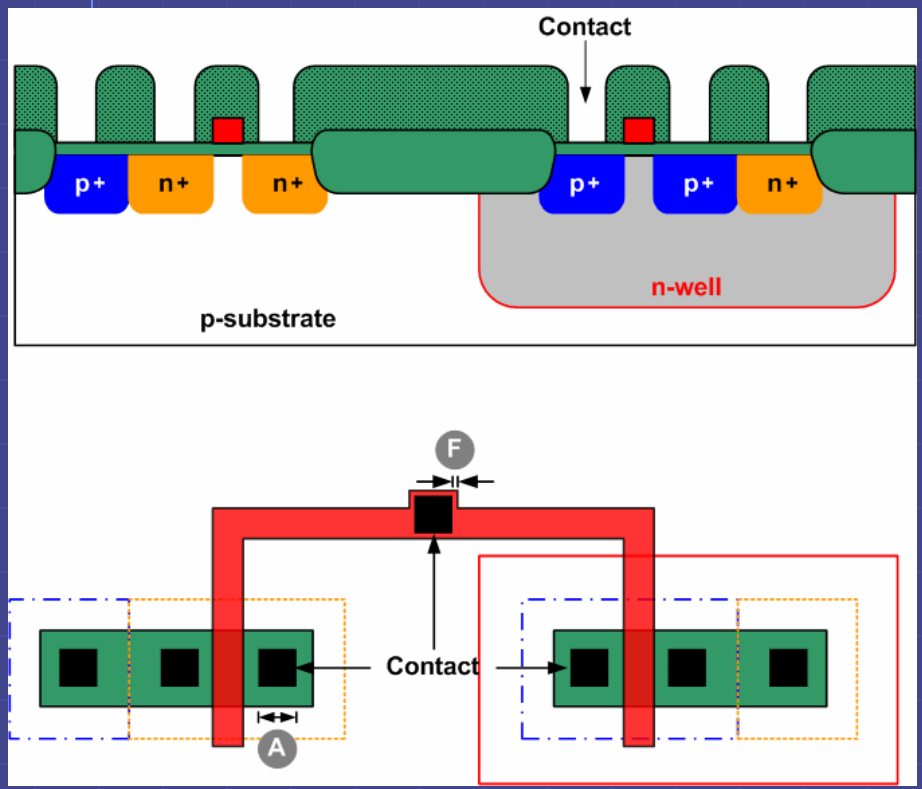


Rule No.	Description	Layout Rule	
Layer :	NP --- N+ Implantation		
NP.W.1	Min. width of a NP region	A	um
NP.S.1	Min. space between two NP regions	B	um
NP.E.1	Min. extension of a NP region beyond a NP active OD region	C	um
NP.C.1	Min. clearance between PP and NP		um

- PP and NP implant have to cover all poly to reduce the resistance

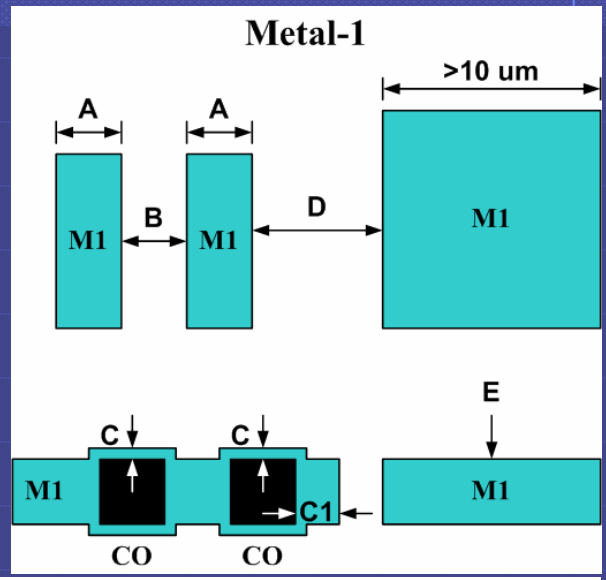
Contact
Cross-Sectional & Layout View

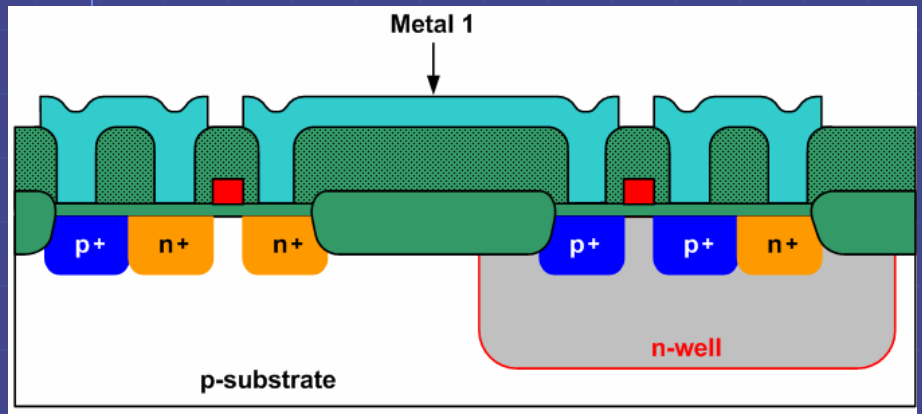


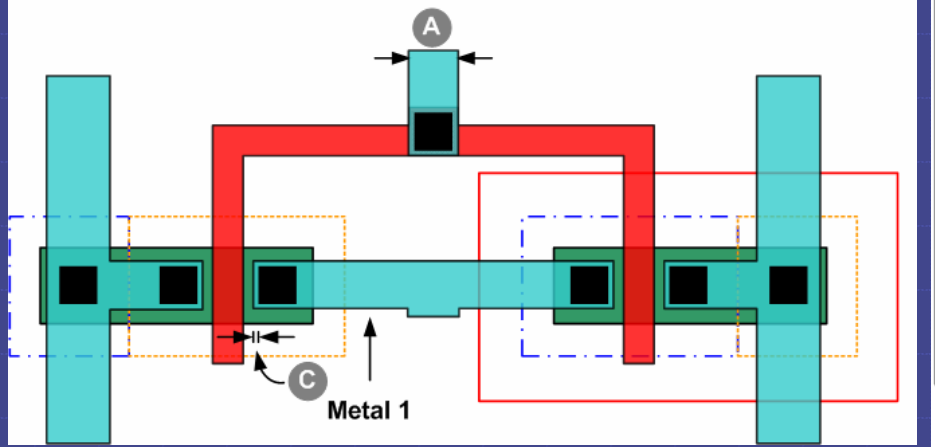


Rule No.	Description	Layout Rule
Layer :	CO --- Contact Window	
CO.W.1	Min. and max. width of an CO region	A um
CO.S.1	Min. space between two CO regions	B um
CO.C.1	Min. clearance from a CO on OD region to a PO gate	C um
CO.C.2	Min. clearance from a CO on PO region to an OD region	D um
CO.E.1	Min. extension of an OD region beyond a OD CO region	E um
CO.E.2	Min. extension of a PO region beyond a Poly CO region	F um

Metal-1
Cross-Sectional & Layout View



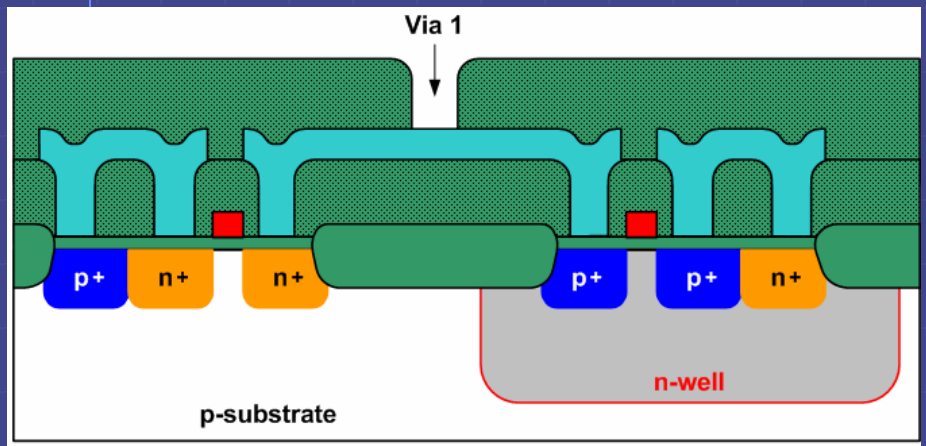


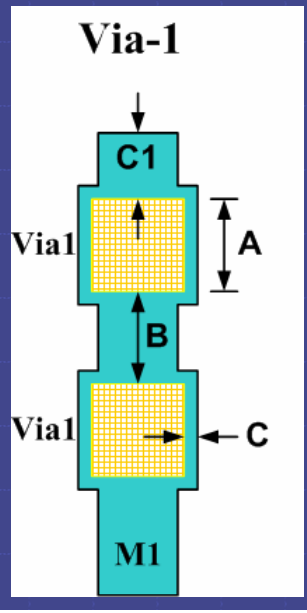


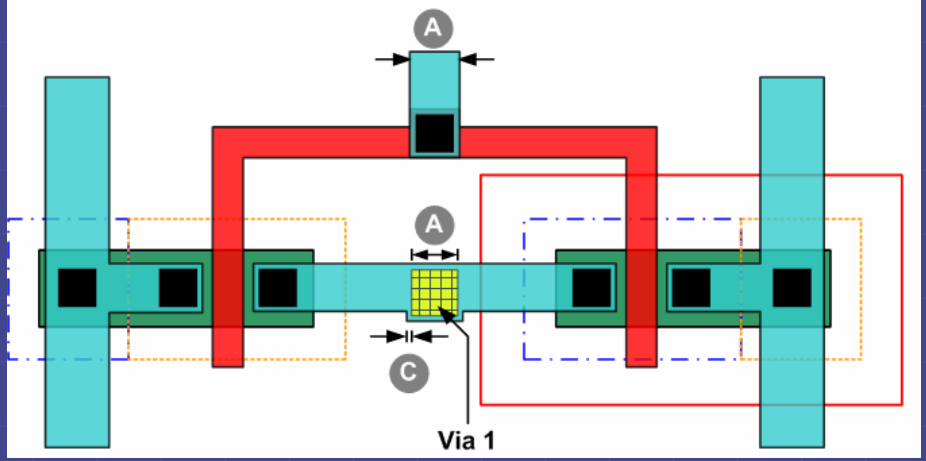
Rule No.	Description	Layout Rule
Layer :	M1 --- Metal-1	
M1.W.1	Minimum width of M1 region	A um
M1.S.1	Minimum space between two M1 regions	B um
M1.E.1	Minimum extension of M1 region beyond CO region	C um
M1.E.2	Minimum extension of M1 end-of-line region beyond CO region	C um
M1.S.2	Minimum space between metal lines with one or both metal line width and length are greater than 10um	D um
M1.A.1	Minimum area of M1 region	E um^2
M1.R.1	Minimum density of M1 area	

- Density is calculated as **Total metal layout area/chip area**

Via1
Cross-Sectional & Layout View

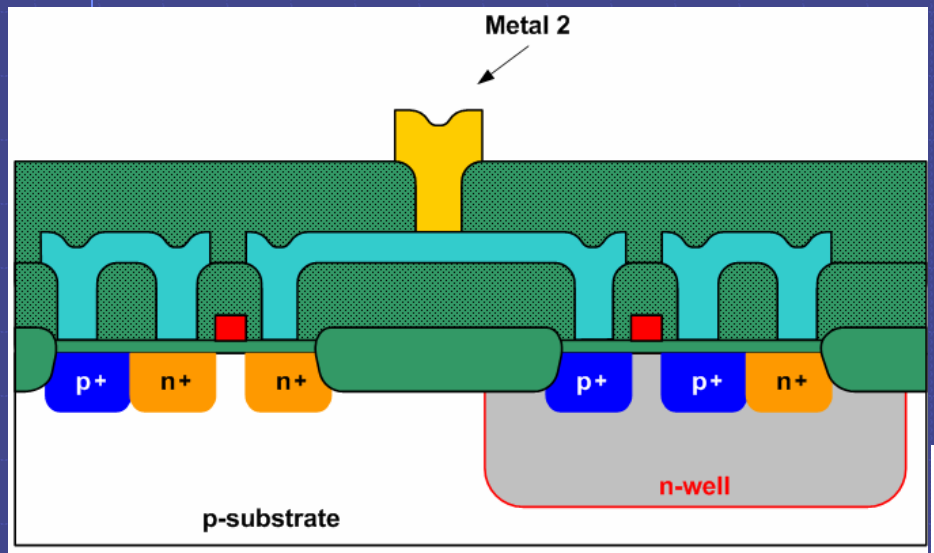


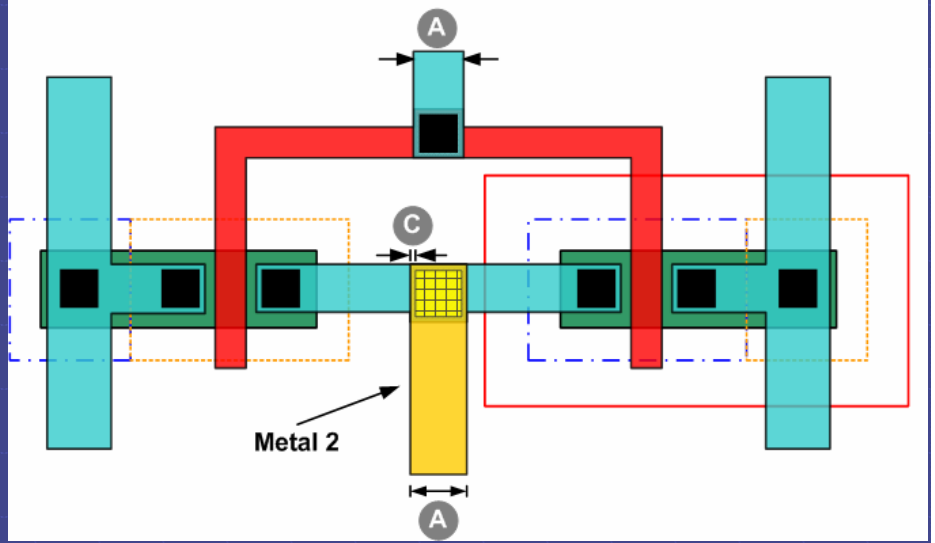


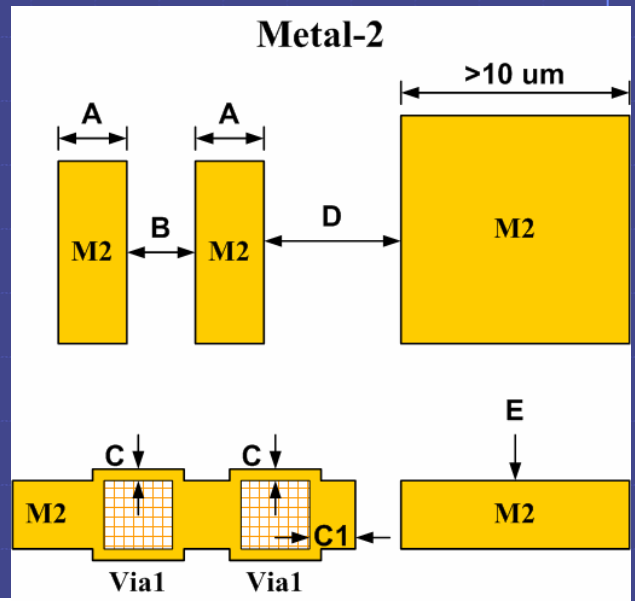


Rule No.	Description	Layout Rule
Layer :	VIA1 --- Via1 Hole	
VIA1.W.1	Min. and max. width of VIA1 region	A um
VIA1.S.1	Minimum space between two VIA1 regions	B um
VIA1.E.1	Minimum extension of M1 region beyond VIA1 region	C um
VIA1.E.2	Minimum extension of M1 end-of-line region beyond VIA1 region	D um
VIA1.C.1	VIA1 can be fully or partially stacked on CO	

Metal-2
Cross-Sectional & Layout View







Rule No.	Description	Layout Rule
Layer :	M2 --- Metal-2	
M2.W.1	Minimum width of M2 region	A um
M2.S.1	Minimum space between two M2 regions	B um
M2.E.1	Minimum extension of M2 region beyond VIA1 region	C um
M2.E.2	Minimum extension of M2 end-of-line region beyond VIA1 region	D um
M2.A.1	Minimum area of M2 region	E um^2
M2.R.1	Minimum density of M2 area	[illegible] %

- Density is calculated as **Total metal layout area/chip area**

Technology Parameters for Typical Case

TECHNOLOGY PARAMETERS FOR TYPICAL CASE:

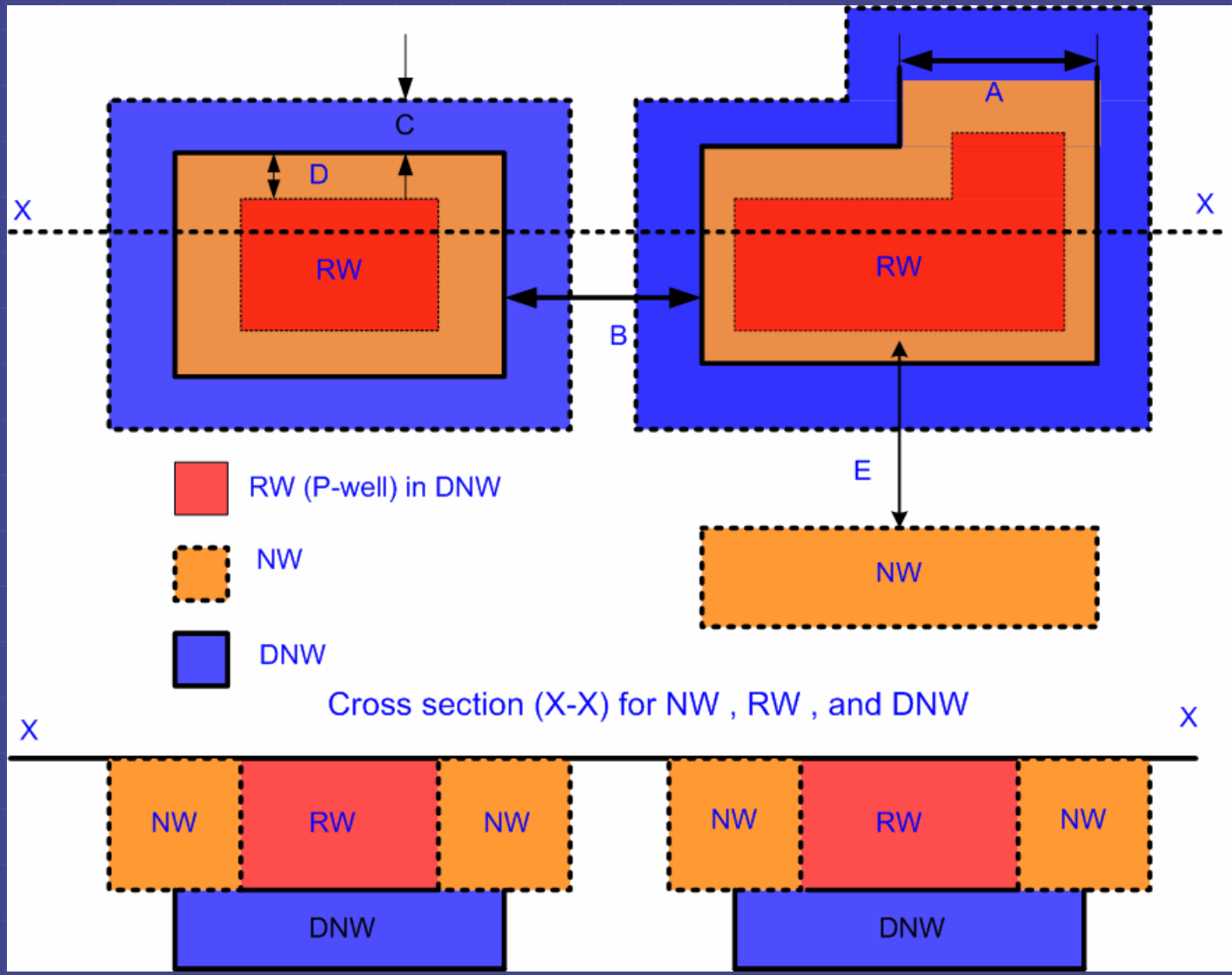
Conductor layers

Conductor	Thickness	Min.width	Min.space	Distance between conductor layer and substrate under FOX
PO1				
M1				
M2				
M3				
M4				
M5				

Dielectric layers

Dielectric	Thickness	Dielectric constant	Comment
FOX			
ILD			
IMD1			ss
IMD2			ss
IMD3			ss
IMD4			ss
PASS1 PASS2			

DNW (deep N-Well definition)



Seal Ring Rule