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Noise Analysis and Design of Amplifiers

by

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1 Noise Models in TI SPICE

To start we will state two of the noise equations coded in the BSIM3v3 model for MOSFETs that are used for simulation at Texas Instruments. The BSIM3v3 model is used for processes with gate oxides of 35 $\mathring{\text{A}}$ or greater and where r.f. frequencies are not important.

The equation for Thermal noise variance that is employed at TI and can be shown from first principles to be correct for all bias regions is

$$\overline{i_d^2} = 4k_B T \frac{\mu_{eff}\, Q_{inv}}{L^2} \Delta f \ . \tag{1}$$

If the code properly calculates the mobility μ_{eff}, the electrical channel length L and the channel charge Q_{inv} taking into account the bias point, then equation (1) is very accurate. The equation we use most of the time at TI for $1/f$ noise variance is given by

$$\overline{i_d^2} = \frac{KF\, I_D}{C_{ox}\, L^2\, f^a} \Delta f \qquad \text{and} \qquad a \approx 1 \tag{2}$$

The form of equation (2) can be derived by assuming a distribution of time constants associated with traps in the oxide (see Noise Physics at the end of this paper). However this equation is empirical because of the addition of the fitting parameters KF and a. Note that fitting a leads to a philosophical problem because of units. Equation (2) is only valid in the bias region that these parameters are fitted. This is in strong inversion and saturation. The parameter KF changes with bias as the device goes into triode.

These equations are fine for coding in SPICE to run in simulation, but we want to perform hand calculations and these equations are not the ones we need. So we will modify them to be more amenable. Starting with equation (1), a first order model for the inversion layer channel charge is

$$Q_{inv} = WLC_{ox}V_{GST} \frac{1 - n + n^2/3}{1 - n/2} \qquad \text{where} \qquad n = V_{DS}/V_{GST} \tag{3}$$

If we remember the first order theory, $g_{ds} = \mu Q/L^2$ which can be manipulated to get the Thermal noise model of van der Ziel for FETs.

$$\overline{i_d^2} = 4k_{_B}T\,\gamma\,g_{d_0}\,\Delta f \tag{4}$$

where g_{d_0} is the conductance of the channel at $V_{_{DS}} = 0$ and

$$\gamma = \frac{1 - n + n^2/3}{1 - n/2} \tag{5}$$

which is a monotonically decreasing function with end points $\gamma = 1$ in triode when $V_{_{DS}} = 0$ and $\gamma = 2/3$ in saturation. Equation (5) is valid for all regions of operation and is a very accurate equation of long channel MOSFETs (see Wang et. al.). However for amplifier all devices in the signal path must be in saturation, so a final simplification to help with deriving noise equations by hand will be introduced. This substitution is only valid when the transistor is biased in saturation.

$$g_{d_0} = g_m\,(1 + \eta)\ , \qquad \eta \equiv \frac{g_{mbs}}{g_m} \tag{6}$$

Also we need a noise equation that is models the noise "seen" at the gate of the MOSFET. But since noise analysis of circuits is *linear* we can easily equate gate voltages with drain currents through the device transconductance. $\overline{i_d^2} = g_m^2\,\overline{v_g^2}$. Therefore the Thermal noise voltage variance at the gate for a transistor in saturation can be re-written as

$$\overline{v_{g_T}^2} = 4k_{_B}T\,\frac{2(1+\eta)}{3g_m}\Delta f \tag{7}$$

Now we need to fine the same type of expression for Flicker noise. So if we take equation (2) and refer the $1/f$ noise to the gate through the transconductance, then we get

$$\overline{v_{g_f}^2} = \frac{KF\,\Delta f}{2\mu C_{ox}^2 W L f} \tag{8}$$

2 Two Stage Transconductance Amp

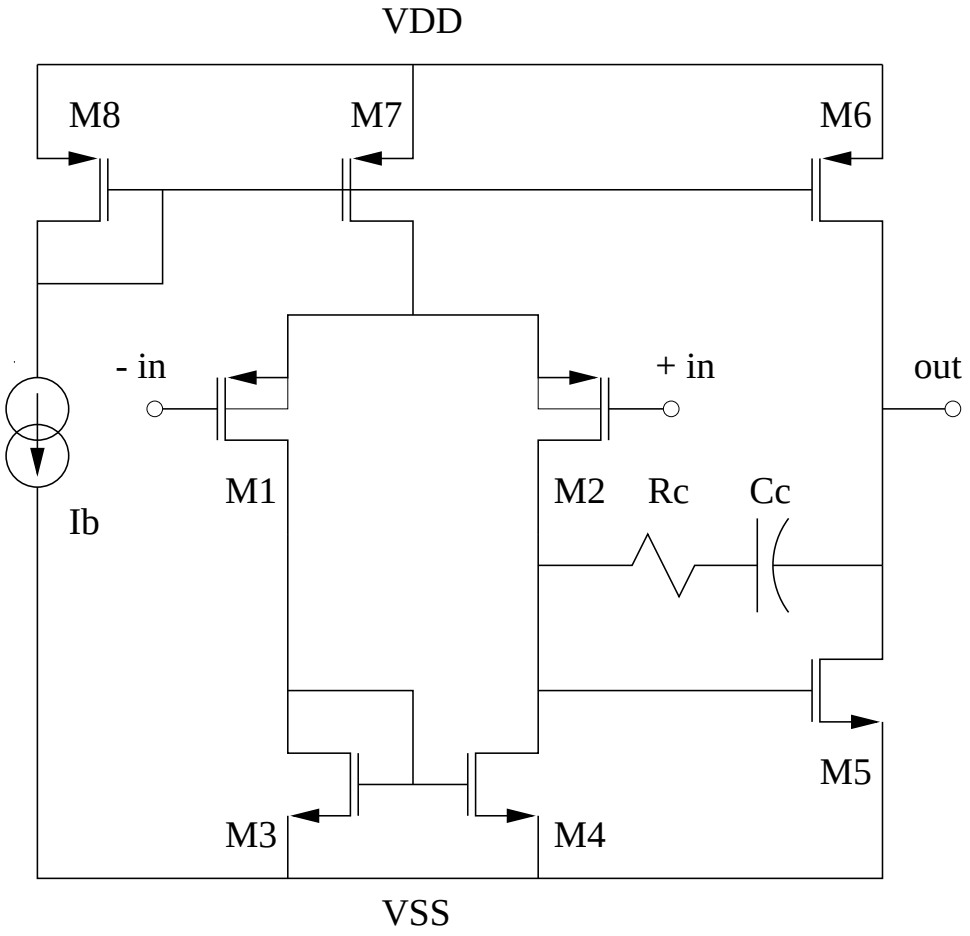

Figure 1: Two stage CMOS transconductance amplifier with PMOS inputs

To begin the noise analysis of the Transconductance (TC) Amp above:

- Only devices in the signal path are important
- Second gain stage (M5 & M6) noise not important because when referred to the input it's divided by the square of the first stage gain
- M7's noise is canceled by symmetry and matching
- Must account for noise of (M1 − M4)
- Start by summing noise currents at drains (M2 & M4)

2.1 General Noise Equation for Two-Stage TC Amp

We start the analysis by writing down the small-signal noise power equation for the Two-Stage TC amp by summing all the $\overline{i_d^2}$ for transistors M1 $-$ M4. We ignore the noise from M5 & M6 because in gain in the first stage of the amp is very large. That leads to the following equation

$$\overline{i_o^2} = g_{m_1}^2 \overline{v_{g_1}^2} + g_{m_2}^2 \overline{v_{g_2}^2} + g_{m_3}^2 \overline{v_{g_3}^2} + g_{m_4}^2 \overline{v_{g_4}^2} \; . \tag{9}$$

Because of symmetry and matching of the differential input pair and load pair, we can reduce equation (9) to

$$\overline{i_o^2} = 2g_{m_2}^2 \overline{v_{g_2}^2} + 2g_{m_4}^2 \overline{v_{g_4}^2} \; . \tag{10}$$

Equation (10) gives the total noise current density at the output of the first stage, but we want to refer this back to the input of the amp as a unique point so different amplifiers can be compared.

$$\overline{v_{g_i}^2} = \frac{\overline{i_o^2}}{g_{m_2}^2} = 2 \left[\overline{v_{g_2}^2} + \left(\frac{g_{m_4}}{g_{m_2}} \right)^2 \overline{v_{g_4}^2} \right] \; . \tag{11}$$

Equation (11) is the general noise equation for the Two-Stage TC amplifier. It can be used to determine the canonical input-referred noise equation for any given noise phenomena if its physical voltage variance $\overline{v_g}^2$ is known.

2.2 Thermal Noise Equation for Two-Stage Amp

To find the input Thermal noise for the Two-Stage amplifier, we substitute equation (7) into equation (11) which yields

$$\overline{v_{g_{T_i}}^2} = 4k_B T \, R_n \, \Delta f \tag{12}$$

where

$$R_n = \frac{4}{3g_{m_2}} \left[1 + \eta_2 + \frac{g_{m_4}}{g_{m_2}} (1 + \eta_4) \right] \; . \tag{13}$$

Now substitute the standard, first order expression for transconductance, $g_m = \sqrt{2\mu C_{ox} SI}$ into equation (13) to get at final equation that can be used to design with

$$R_n = \frac{4}{3\sqrt{2\mu_p C_{ox} S_2 I_2}} \left[1 + \eta_2 + \sqrt{\frac{\mu_n S_4}{\mu_p S_2}} (1 + \eta_4) \right], \; S \equiv W/L \; . \qquad (14)$$

Examining equation (14) leads to the following set of design rules to lower the Thermal noise in a Two-Stage CMOS transconductance amplifier and a generally valid conclusion that NMOS input device are the best choice for low Thermal noise.

- To decrease thermal noise make S_2 large
- Also increasing I_2 will decrease the noise
- Make $\mu_n \, S_4 < \mu_p \, S_2$
- It would be easier to get lower thermal noise if the amp used NMOS input devices, since $\mu_n > \mu_p$

2.3 Figure of Merit Designs of Two Stage TC Amps

The next set of tables show the same seven transistor Two-Stage transconductance amplifier designed with either NMOS, PMOS, Natural NMOS or Natural PMOS depending on the process node. The relative merit of with input type to choose can be studied.

TABLE 1; A12, $T_{ox} = 90$Å

Input Device Type	Nch (H V_t)	Nch (L V_t)	Pch (H V_t)	Pch (L V_t)
DC Gain	100.9 dB	98.98 dB	104.6 dB	105.0 dB
Unity Gain BW	6.857 MHz	7.861 MHz	5.482 MHz	6.973 MHz
Phase Margin	59.9°	55.6°	67.1°	61.2°
Gain Margin	18.1 dB	16.3 dB	21.0 dB	18.5 dB
$\int$ Noise p-weight	3.541 μV_{rms}	3.090 μV_{rms}	4.625 μV_{rms}	3.442 μV_{rms}
$\int$ Noise 1-1GHz	4.539 mV_{rms}	3.742 mV_{rms}	7.890 mV_{rms}	6.766 mV_{rms}
C_c	10 pF	10 pF	10 pF	10 pF
Load	10 pF	10 pF	10 pF	10 pF
Bias Current	309 μA	309 μA	305 μA	305 μA

TABLE 2; A10, $T_{ox} = 75$Å

Input Device Type	Nch (H V_t)	Pch (H V_t)
DC Gain	109.1 dB	111.1 dB
Unity Gain BW	6.70 MHz	5.531 MHz
Phase Margin	59.7°	65.9°
Gain Margin	18.6 dB	21.1 dB
$\int$ Noise p-weight	5.776 μV_{rms}	7.354 μV_{rms}
$\int$ Noise 1-1GHz	8.408 mV_{rms}	13.524 mV_{rms}
C_c	10 pF	10 pF
Load	10 pF	10 pF
Bias Current	290 μA	300 μA

TABLE 3; C07, $T_{ox} = 80$Å

Input Device Type	Nch (H V_t)	Pch (H V_t)
DC Gain	94.3 dB	98.7 dB
Unity Gain BW	7.054 MHz	5.824 MHz
Phase Margin	59.5°	65.3°
Gain Margin	18.2 dB	20.5 dB
$\int$ Noise p-weight	3.998 μV_{rms}	5.054 μV_{rms}
$\int$ Noise 1-1GHz	5.375 mV_{rms}	10.874 mV_{rms}
C_c	10 pF	10 pF
Load	10 pF	10 pF
Bias Current	301 μA	302 μA

TABLE 4; TSMC0.35um, $T_{ox} = 70$Å

Input Device Type	Nch (H V_t)	Pch (H V_t)
DC Gain	95.4 dB	102.3 dB
Unity Gain BW	7.029 MHz	6.243 MHz
Phase Margin	60.2°	60.9°
Gain Margin	20.0 dB	19.5 dB
$\int$ Noise p-weight	? μV_{rms}	? μV_{rms}
$\int$ Noise 1-1GHz	5.654 mV_{rms}	10.514 mV_{rms}
C_c	10 pF	10 pF
Load	10 pF	10 pF
Bias Current	302 μA	307 μA

2.4 $1/f$ Noise in Two Stage TC Amp

To find the input $1/f$ noise for the Two-Stage TC amplifier, substitute equation (8) into the general equation (11) which gives

$$\overline{v_{g_{F_i}}^2} = \frac{KF_p\,\Delta f}{\mu_p C_{ox}^2 W_2 L_2 f}\left[1 + \frac{KF_n}{KF_p}\left(\frac{L_2}{L_4}\right)^2\right] . \tag{15}$$

We have the design equation for $1/f$ noise in a Two-Stage amp. Note that there are two independent parameters in equation (15). They are the input PMOS width W_2 and the NMOS load length L_4. However the input device length L_2 is a dependent parameter that is quadratic, therefore it can be optimized. We can determine the optimal value through calculus by taking a derivative of equation (15).

$$\frac{\partial \overline{v_{g_{F_i}}^2}}{\partial L_2} = 0\,, \longrightarrow\; L_2 = \sqrt{\frac{KF_p}{KF_n}}\,L_4 \tag{16}$$

Using equation (16) the optimine input length can be found after the load lenghs are determined. The load L is usually found based on other design parameters. Studing these two noise equations leads to the following summary for good $1/f$ design.

- Notice that W_2 and L_4 are independent parameters
- Therefore increasing either will decrease $1/f$ noise
- After L_4 is choosen for best thermal noise, then L_2 is found by the optimization relation
- Note that KF_n is $4 - 16$ times larger than KF_p for all n-gate analog CMOS. For n-gate, p-gate analog CMOS KF_n is $2 - 4$ times larger and for digital CMOS since C07 KF_p is usually greater than KF_n. These facts must be taken into account when choosing which type of input device to use.

3 Folded-Cascode Transconductance Amp

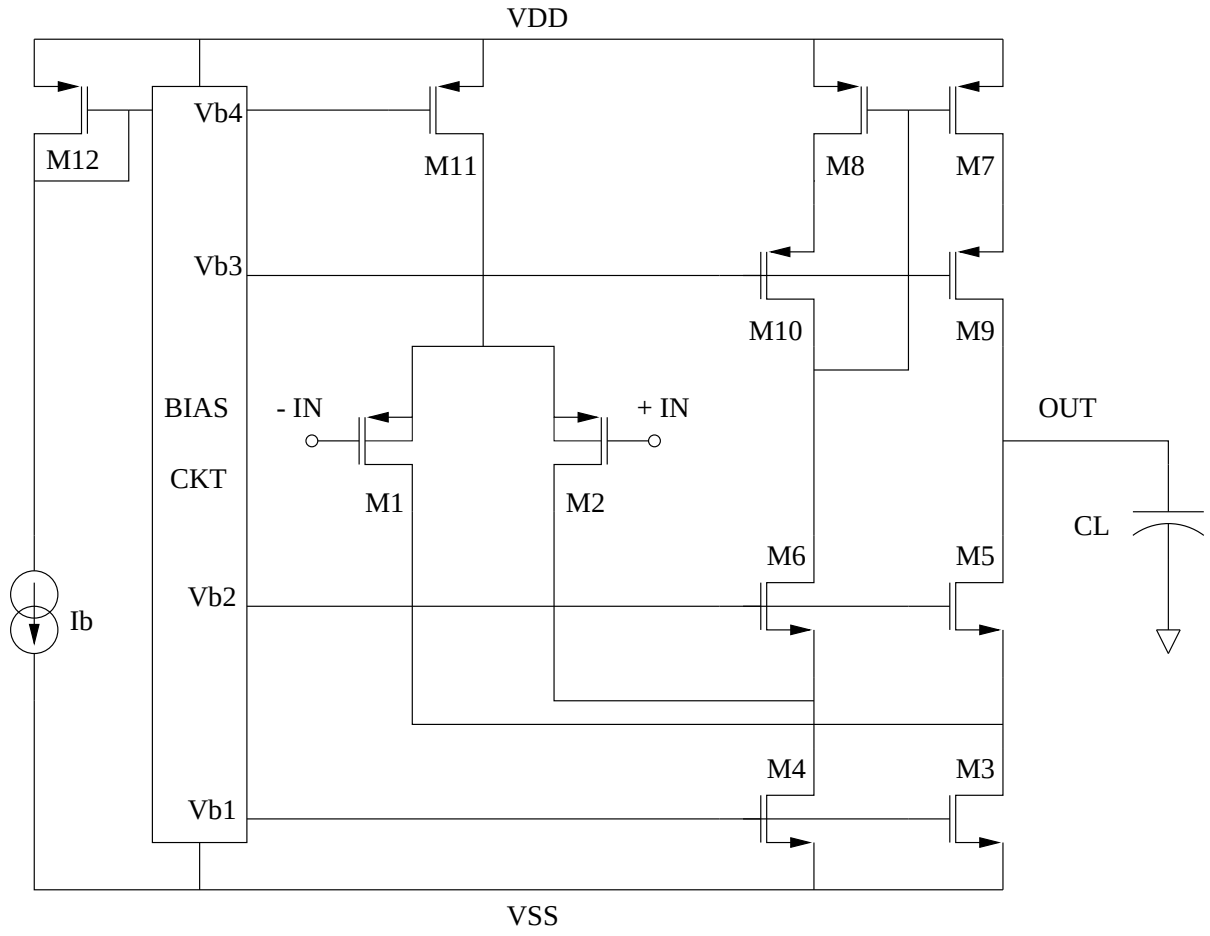

Figure 2: CMOS folded-cascode transconductance amplifier with PMOS inputs

To begin the noise analysis on the Folded-Cascode TC amp above:

- Only devices in the signal path are important
- M11's noise is canceled by symmetry and matching
- Must account for noise of (M1 − M10)
- The cascode devices are special cases
- Start by summing noise currents at the output

3.1 General Noise Equation for Folded-Cascode TC Amp

The analysis begins by writing down the small-signal noise power equation for the Folded-Cascode transconductance amplifier by summing all the $\overline{i_d^2}$ for transistors M1 − M10.

$$\begin{aligned}\overline{i_o^2} &= g_{m_1}^2\overline{v_{n_1}^2} + g_{m_2}^2\overline{v_{g_2}^2} + g_{m_3}^2\overline{v_{g_3}^2} + g_{m_4}^2\overline{v_{g_4}^2} + G_{m_5}^2\overline{v_{g_5}^2} \\ &+ G_{m_6}^2\overline{v_{g_6}^2} + g_{m_7}^2\overline{v_{g_7}^2} + g_{m_8}^2\overline{v_{g_8}^2} + G_{m_9}^2\overline{v_{g_9}^2} + G_{m_{10}}^2\overline{v_{g_{10}}^2} \ .\end{aligned}$$

The general bias condition for Folded-Cascode TC amps is to make the tail current source equal to the load current source. Then by design, $I_3 = I_{11} = 2I_1 = 2I_7$ when symmetry and matching is considered we get

$$\overline{i_o^2} = 2\left(g_{m_1}^2\overline{v_{n_1}^2} + g_{m_3}^2\overline{v_{g_3}^2} + G_{m_5}^2\overline{v_{g_5}^2} + g_{m_7}^2\overline{v_{g_7}^2} + G_{m_9}^2\overline{v_{g_9}^2}\right) \ , \tag{17}$$

where $G_m \equiv$ effective transconductance with source degeneration. The equations for the degenerated transconductances are

$$G_{m_5} = \frac{g_{m_5}}{1 + g_{m_5}\left(r_{d_1}||r_{d_3}\right)} ; \qquad G_{m_9} = \frac{g_{m_9}}{1 + g_{m_9}r_{d_7}} \ . \tag{18}$$

Now since for good design bias points $g_m r_d > 10^2$, then $G_m^2 \simeq g_m^2/10^4$. Therefore we can ignore the cascode devices. This allows the output noise current to simplify to

$$\overline{i_o^2} = 2\left(g_{m_1}^2\overline{v_{g_1}^2} + g_{m_3}^2\overline{v_{g_3}^2} + g_{m_7}^2\overline{v_{g_7}^2}\right) \tag{19}$$

Equation (19) gives the total noise current density at the output of the Folded-cascode amp, however we now want to refer this back to the input of the amp

$$\overline{v_{g_i}^2} = \frac{\overline{i_o^2}}{g_{m_1}^2} = 2\left[\overline{v_{g_1}^2} + \left(\frac{g_{m_3}}{g_{m_1}}\right)^2\overline{v_{g_3}^2} + \left(\frac{g_{m_7}}{g_{m_1}}\right)^2\overline{v_{g_7}^2}\right] \tag{20}$$

Equation (20) is the general noise equation for the Folded-Cascode TC amplifier. Now we can determine the canonical input-referred noise equation for Thermal and $1/f$ noise by substituting their physical voltage variance into equation (20).

3.2 Thermal Noise of Folded-Cascode TC Amp

As before, to find the input Thermal noise for the Folded-Cascode amplifier, substitute (7) into general noise equation (20) yielding

$$\overline{v_{g_{T_i}}^2} = 4k_B T\, R_n\, \Delta f\ . \tag{21}$$

where

$$R_n = \frac{4}{3g_{m_1}}\left[1+\eta_1+\frac{g_{m_3}}{g_{m_1}}(1+\eta_3)+\frac{g_{m_7}}{g_{m_1}}(1+\eta_7)\right]\ . \tag{22}$$

Substituting the first order expression for transconductance, $g_m = \sqrt{2\mu C_{ox} SI}$ into equation (22) to get at final equation that can be used to design with

$$R_n = \frac{4}{3\sqrt{2\mu_p C_{ox} S_1 I_1}}\left[1+\eta_1+\sqrt{\frac{2\mu_n S_3}{\mu_p S_1}}(1+\eta_3)+\sqrt{\frac{S_7}{S_1}}(1+\eta_7)\right] \tag{23}$$

Examining equation (23) leads to the following set of design rules to lower the Thermal noise in a Folded-Cascode CMOS transconductance amplifier and again the generally valid conclusion that NMOS input device are the best choice for low Thermal noise.

- To decrease thermal noise make S_1 large
- Also increasing I_1 will decrease the noise
- Make $2\mu_n\, S_3 < \mu_p\, S_1$
- Also make $S_7 < S_1$
- It would be easier to get lower thermal noise if the amp used NMOS input devices, since $\mu_n > \mu_p$

3.3 $1/f$ Noise for Folded-Cascode TC Amp

As before substitute equation (8) into general noise equation (20) for the Folded-Cascode amp to get the following

$$\overline{v_{g_{F_i}}^2} = \frac{KF_p\,\Delta f}{\mu_p C_{ox}^2 W_1 L_1 f}\left[1 + \frac{2KF_n}{KF_p}\left(\frac{L_1}{L_3}\right)^2 + \left(\frac{L_1}{L_7}\right)^2\right] \tag{24}$$

This give the design equation for $1/f$ noise in a Folded-Cascode TC amp. Note again that there are three independent parameters in equation (24). They are the input PMOS width W_1, the NMOS load length L_3 and the PMOS load length L_7. The input device length L_1 is a dependent parameter that is quadratic, so it can be optimized. We determine the optimal value through calculus by taking a derivative of equation (24).

$$\frac{\partial \overline{v_{n_i}^2}}{\partial L_1} = 0\,, \longrightarrow\ \frac{1}{L_1^2} = 2\frac{KF_n}{KF_p}\frac{1}{L_3^2} + \frac{1}{L_7^2} \tag{25}$$

Equation (25) is used to optimize the PMOS input length after the load transistor lengths L_3 and L_7 are found from other design requirements. In conclusion the following summary leads to good $1/f$ design in Foled-cascode amps.

- Cascode devices do not contribute to noise
- Notice that W_1, L_3 and L_7 are independent parameters
- Therefore increasing any of these parameters will decrease $1/f$ noise
- After L_3 and L_7 are choosen for best thermal noise, then L_1 is found by the optimization relation
- There is no clear choice between PMOS and NMOS input devices. Look at process based parameter relation, $KF/(\mu C_{ox}^2)$, for guidance.

4 Source Degeneration

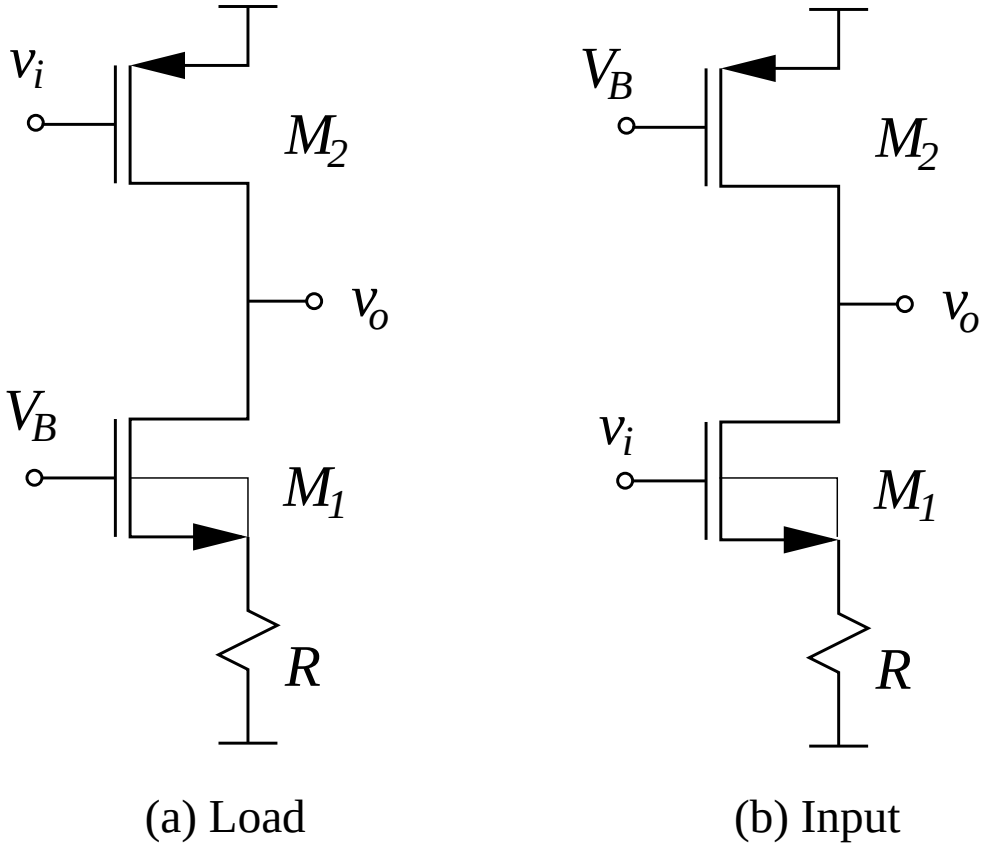

Figure 3: CMOS amplifiers with source degeneration of (a) the load and (b) the input

4.1 Noise Analysis of Amp with Degenerated Load

The first case we will consider is source degeneration of the load. Start by summing noise currents at the output (drains M_1 & M_2)

$$\overline{i_o^2} = g_{m_2}^2 \overline{v_{g_2}^2} + G_{m_1}^2 \overline{v_{g_1}^2} + K_R^2 \, \overline{i_R^2} \, , \tag{26}$$

where

$$G_{m_1} = \frac{g_{m_1}}{1 + g_{m_1} R} \; ; \quad K_R = \frac{R}{R + r_{s_1}} \; ; \quad r_{s_1} \cong 1/g_{m_1} \, . \tag{27}$$

Referring back to the input, M_2, yields

$$\overline{v_{g_i}^2} = \frac{\overline{i_o^2}}{g_{m_2}^2} = \overline{v_{g_2}^2} + \left(\frac{g_{m_1}}{g_{m_2}}\right)^2 \left[\frac{\overline{v_{g_1}^2}}{\left(1+g_{m_1}R\right)^2} + \frac{\overline{v_R^2}}{\left(1+g_{m_1}R\right)^2}\right] , \qquad (28)$$

with $\overline{v_R^2} = 4k_BTR\Delta f$.

Note we can conclude from equation (28) the following items.

- Note that the noise seen at the input from M_1 is reduced by the factor $(1+g_{m_1}R)^2$.
- This factor deduces both $1/f$ and thermal noise of M_1
- But the thermal noise of R is now included in the total
- However even this noise is reduced by the same factor
- In practice, the $1/f$ noise can be halved while the thermal noise is not increased

For a particular case with the 4/3 process, the input-referred $1/f$ noise density at 1 Hz went from 702 nV/$\sqrt{\text{Hz}}$ without any source degeneration to 462 nV/$\sqrt{\text{Hz}}$ with 88 mV of degeneration. While the input-referred Thermal noise was 16.6 nV/$\sqrt{\text{Hz}}$ without and 15.1 nV/$\sqrt{\text{Hz}}$ with. So the degeneration helps alot with $1/f$ noise and does not hurt Thermal noise.

4.2 Noise Analysis of Amp with Degenerated Input

The second case we will consider is source degeneration of the input. Again start by summing noise currents at the output (drains M_1 & M_2)

$$\overline{i_o^2} = G_{m_1}^2 \overline{v_{g_1}^2} + g_{m_2}^2 \overline{v_{g_2}^2} + K_R^2 \, \overline{i_R^2} \, , \tag{29}$$

where

$$G_{m_1} = \frac{g_{m_1}}{1 + g_{m_1} R} \; ; \quad K_R = \frac{R}{R + r_{s_1}} \; ; \quad r_{s_1} \cong 1/g_{m_1} \, . \tag{30}$$

Referring back to the input, M_1, yields

$$\overline{v_{g_i}^2} = \frac{\overline{i_o^2}}{G_{m_1}^2} = \overline{v_{g_1}^2} + \left(\frac{g_{m_2}}{G_{m_1}} \right)^2 \overline{v_{g_2}^2} + \left(\frac{K_R}{G_{m_1}} \right)^2 \overline{i_R^2} \tag{31}$$

$$\overline{v_{g_i}^2} = \overline{v_{g_1}^2} + \left(\frac{g_{m_2}}{g_{m_1}} \right)^2 \overline{v_{g_2}^2} \, (1 + g_{m_1} R)^2 + 4 k_B T R \Delta f \tag{32}$$

Note we can conclude from equation (32) the following items.

- Note that the noise seen at the input from M_2 is multiplied by the factor $(1 + g_{m_1} R)^2$.
- This factor increases both $1/f$ and thermal noise of M_2
- The thermal noise voltage of R is now seen directly in the total at the input
- In practice, source degeneration of the input device is never done if noise is the determining factor to meet spec

5 Integrated Noise for a Unity Gain Amp

The equations that have been developed are for noise density, but for total noise the density must be integrated over some bandwidth of interest. If we are interested in the total noise of a Two-Stage TC amp with unity gain feedback, then for most amplifiers we can ignore $1/f$ and only integrate the Thermal noise. Since the Thermal noise is "white" we just need to find the noise bandwidth of the one pole system (see Appendix A). We can start with the input-referred Thermal noise for the Two-Stage amp in equation (14) and re-write it with the subscripts I and L for input and load respectfully.

$$\overline{v_{n_{tot}}^2} = 4k_B T \frac{4}{3g_{m_I}} \triangle f_{BW} \ , \tag{33}$$

where

$$\triangle \equiv 1 + \eta_I + \frac{g_{m_L}}{g_{m_I}} (1 + \eta_L) \, . f_{BW} \equiv \frac{\pi}{2} f_u \tag{34}$$

The noise bandwidth is given by

$$f_{BW} \equiv \frac{\pi}{2} f_u \ . \tag{35}$$

Remembering that the unity gain frequency of an opamp is $f_u = \frac{g_{m_I}}{2\pi C_c}$. Also the ratio of backgate to frontgate transconductance for NMOS and PMOS transistors are $\eta_n \simeq \frac{1}{2}$; $\eta_p \simeq \frac{1}{3}$ respectfully which leads to $\triangle \simeq 2$ for PMOS inputs. After substitution the total noise is

$$\overline{v_{n_{tot}}^2} \cong 4k_B T \left(\frac{4}{3g_{m_I}} \right) (2) \left(\frac{\pi}{2} \right) \left(\frac{g_{m_I}}{2\pi C_c} \right) = \frac{8}{3} \frac{k_B T}{C_c} \tag{36}$$

6 Figure of Merit for Noise for Different Technologies

TABLE 5; LBC1, $T_{ox} = 425$Å

Parameter	N_{Vt_H}	N_{Vt_L}	P_{Vt_H}	P_{Vt_L}
Effective T_{ox} (Å)	425	425	425	NA
KF	13.629	9.83	1.6034	NA
μC_o (μA/V^2)	51	63	16	NA
$KF/\mu C_o^2$	32.89	19.20	12.33	NA
$\int$ 1/f (μV)	163.7	125.1	100.2	NA
$\int$ Thermal (μV)	128.1	121.5	161.3	NA
Total Noise (μV)	207.8	174.4	189.9	NA
SNR (dB)	84.17	85.70	84.95	NA

TABLE 6; LinEPIC - 50A24, $T_{ox} = 200$Å

Parameter	N_{Vt_H}	N_{Vt_L}	P_{Vt_H}	P_{Vt_L}
Effective T_{ox} (Å)	200.8	205.35	200.0	203.15
KF	49.0	21.299	3.9237	5.998
μC_o (μA/V^2)	81	96	30	29
$KF/\mu C_o^2$	35.04	12.85	7.58	11.98
$\int$ 1/f (μV)	169.2	103.7	78.54	99.54
$\int$ Thermal (μV)	114.1	109.3	137.9	139.0
Total Noise (μV)	204.1	150.7	158.7	171.0
SNR (dB)	77.84	80.47	80.02	79.37

TABLE 7; 50A21.2, $T_{ox} = 140$Å

Parameter	N_{Vt_H}	N_{Vt_L}	P_{Vt_H}	P_{Vt_L}
Effective T_{ox} (Å)	158.23	156.93	153.46	154.33
KF	41.85	29.847	12.24	10.291
μC_o (μA/V^2)	95	112	26	30
$KF/\mu C_o^2$	20.19	12.21	21.57	18.85
$\int$ 1/f (μV)	128.2	99.30	130.5	111.7
$\int$ Thermal (μV)	109.6	105.2	142.9	137.9
Total Noise (μV)	168.7	144.7	193.5	177.4
SNR (dB)	79.49	80.83	78.30	79.05

TABLE 8; 33A21.2, $T_{ox} = 90$Å

Parameter	N_{Vt_H}	N_{Vt_L}	P_{Vt_H}	P_{Vt_L}
Effective T_{ox} (Å)	99.22	99.22	99.74	102.76
KF	31.57	22.124	15.228	6.6881
μC_o (μA/V^2)	136	166	36	45
$KF/\mu C_o^2$	6.92	3.98	12.62	4.43
$\int$ 1/f (μV)	73.70	55.85	99.75	60.02
$\int$ Thermal (μV)	100.2	95.33	131.7	124.6
Total Noise (μV)	124.4	110.5	165.2	138.3
SNR (dB)	78.02	79.05	75.55	77.10

TABLE 9; 33C10.3, $T_{ox} = 75$Å

Parameter	N_{Vt_H}	N_{Vt_L}	P_{Vt_H}	P_{Vt_L}
Effective T_{ox} (Å)	80.93	NA	83.51	NA
KF	52.3	NA	77	NA
μC_o (μA/V^2)	152	NA	40	NA
$KF/\mu C_o^2$	8.06	NA	46.56	NA
$\int$ 1/f (μV)	81.04	NA	194.7	NA
$\int$ Thermal (μV)	97.46	NA	128.3	NA
Total Noise (μV)	126.7	NA	233.2	NA
SNR (dB)	77.85	NA	72.56	NA

TABLE 10; 1833C07, $T_{ox} = 80$Å

Parameter	N_{Vt_H}	N_{Vt_L}	P_{Vt_H}	P_{Vt_L}
Effective T_{ox} (Å)	83.62	NA	85.97	NA
KF	75.3	NA	46.3	NA
μC_o (μA/V^2)	144	NA	38	NA
$KF/\mu C_o^2$	12.66	NA	30.33	NA
$\int$ 1/f (μV)	101.6	NA	157.2	NA
$\int$ Thermal (μV)	98.78	NA	129.9	NA
Total Noise (μV)	141.7	NA	204.0	NA
SNR (dB)	76.88	NA	73.72	NA

TABLE 11; 18C07, $T_{ox} = 40$Å

Parameter	N_{Vt_H}	N_{Vt_L}	P_{Vt_H}	P_{Vt_L}
Effective T_{ox} (Å)	48.22	NA	49.78	NA
KF	83.966	NA	77.33	NA
μC_o (μA/V^2)	270	NA	65	NA
$KF/\mu C_o^2$	4.39	NA	16.45	NA
$\int$ 1/f (μV)	59.47	NA	118.2	NA
$\int$ Thermal (μV)	84.42	NA	113.6	NA
Total Noise (μV)	103.3	NA	164.0	NA
SNR (dB)	72.97	NA	68.95	NA

TABLE 12; 18C05AF, $T_{ox} = 40$Å

Parameter	N_{Vt_H}	N_{Vt_L}	P_{Vt_H}	P_{Vt_L}
Effective T_{ox} (Å)	47.6	NA	49.93	NA
KF	45.264	NA	68.497	NA
μC_o (μA/V^2)	230	NA	58	NA
$KF/\mu C_o^2$	2.74	NA	17.26	NA
$\int$ 1/f (μV)	47.00	NA	117.9	NA
$\int$ Thermal (μV)	87.87	NA	116.9	NA
Total Noise (μV)	99.65	NA	166.0	NA
SNR (dB)	73.28	NA	68.84	NA

Notes: All of the transistors were 1 μm/1 μm in size, biased at 1 μA of current. The noise is integrated from 1 Hz to 10 MHz. The maximum signal is 0.5 V less than the power supply.