12. Analyzing and Optimizing the Design Floorplan

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You can use the Chip Planner to perform design analysis and create a design floorplan. With some of the older device families, you must use the Timing Closure Floorplan to analyze the device floorplan. To make I/O assignments, use the Pin Planner.

Introduction

As FPGA designs grow larger in density, analyzing the design for performance, routing congestion, and logic placement to meet the design requirements becomes critical.

This chapter discusses how to analyze the design floorplan with the Chip Planner and the Timing Closure Floorplan (for supported devices only).

You can use the Design Partition Planner along with the Chip Planner to customize the floorplan for your design. For more information, refer to the *Quartus II Incremental Compilation for Hierarchical and Team-Based Design* and the *Best Practices for Incremental Compilation Partition and Floorplan Assignments* chapters in volume 1 of the *Quartus II Handbook*.

This chapter includes the following topics:

For more information about the Pin Planner, refer to the *I/O Management* chapter in volume 2 of the *Quartus II Handbook*.

Table 12–1 lists the device families supported by the Chip Planner and the Timing Closure Floorplan.

Table 12–1. Chip Planner and Timing Closure Floorplan Device Support (Part 1 of 2)

Device Family	Timing Closure Floorplan	Chip Planner
Arria® series	—	✓
Cyclone series	—	✓
HardCopy series	—	✓
Stratix series	—	✓
MAX® IIZ	—	✓
MAX II	—	✓

Table 12–1. Chip Planner and Timing Closure Floorplan Device Support (Part 2 of 2)

Device Family	Timing Closure Floorplan	Chip Planner
MAX 3000	✓	—
MAX 7000	✓	—

Chip Planner Overview

The Chip Planner provides a visual display of chip resources. It can show logic placement, LogicLock regions, relative resource usage, detailed routing information, fan-in and fan-out connections between nodes, timing paths between registers, and delay estimates for paths. With the Chip Planner, you can view critical path information, physical timing estimates, and routing congestion.

You can also perform assignment changes with the Chip Planner, such as creating and deleting resource assignments, and post-compilation changes such as creating, moving, and deleting logic cells and I/O atoms. With the Chip Planner and Resource Property Editor, you can change connections between resources and make post-compilation changes to the properties of logic cells, I/O elements, PLLs, and RAM and digital signal processing (DSP) blocks. With the Chip Planner, you can view and create assignments for a design floorplan, perform power and design analyses, and implement ECOs.

For details about how to implement ECOs in your design using the Chip Planner in the Quartus II software, refer to the *Engineering Change Management with the Chip Planner* chapter in volume 2 of the *Quartus II Handbook*.

Starting the Chip Planner

To start the Chip Planner, on the Tools menu, click **Chip Planner (Floorplan & Chip Editor)**. You can also start the Chip Planner by the following methods:

- Click the Chip Planner icon on the Quartus II software toolbar
- On the Shortcut menu in the following tools, click **Locate** and then click **Chip Planner**:
  - Design Partition Planner
  - Compilation Report
  - LogicLock Regions window
  - Technology Map Viewer
  - Project Navigator window
  - RTL source code
  - Node Finder
  - Simulation Report
  - RTL Viewer
  - Report Timing panel of the TimeQuest Timing Analyzer

If the device in your project is not supported by the Chip Planner and you attempt to start the Chip Planner, the following message appears:

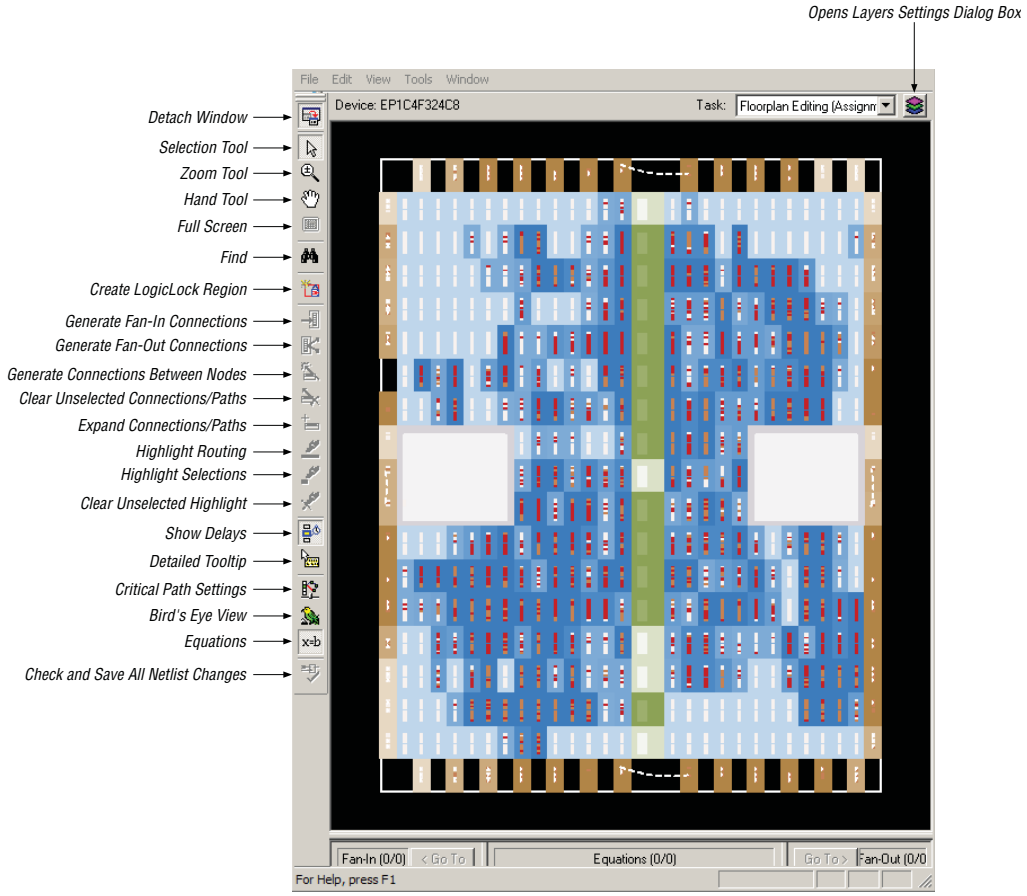
```
Can't display Chip Planner: the current device family is unsupported.
```

Use the Timing Closure Floorplan for devices not supported by the Chip Planner.

Chip Planner Toolbar

The Chip Planner gives you powerful capabilities for design analysis with a user-friendly GUI. Many Chip Planner functions are available from the menu items or by clicking the icons on the toolbar. Figure 12–1 shows an example of the Chip Planner toolbar and provides descriptions for commonly used icons located on the Chip Planner toolbar.

Figure 12–1. Chip Planner Toolbar



You can customize the icons on the Chip Planner toolbar by clicking **Customize Chip Planner** on the Tools menu (if the Chip Planner window is attached), or by clicking **Customize** on the Tools menu (if the Chip Planner window is detached).

Chip Planner Tasks and Layers

The Chip Planner has predefined tasks that enable you to quickly implement ECO changes or manipulate assignments for the floorplan of the device. To select a task, click on the task name in the Task menu. The predefined tasks in the Chip Planner are:

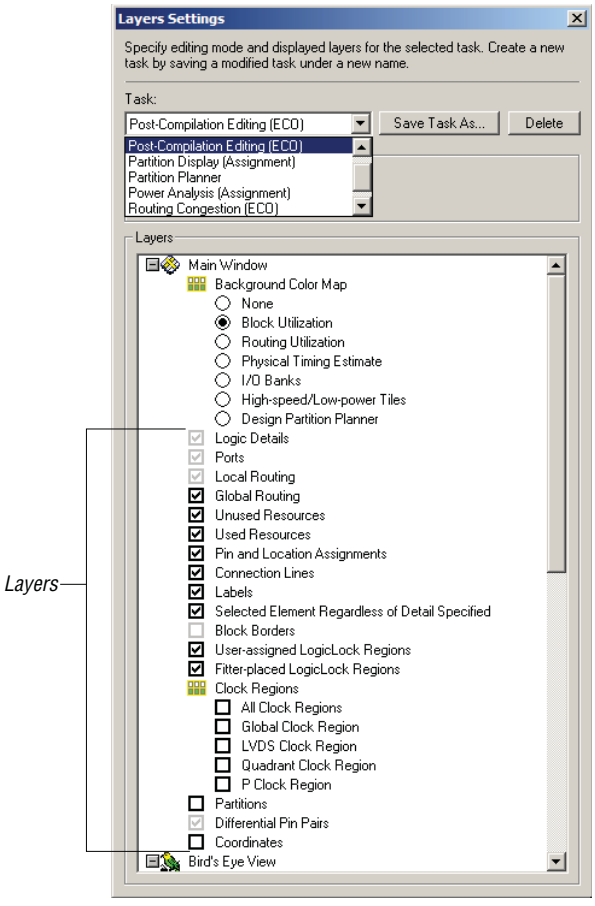
- **Floorplan Editing (Assignment)**
- **Post-Compilation Editing (ECO)**
- **Partition Display (Assignment)**
- **Partition Planner**
- **Routing Congestion (ECO)**
- **Clock Regions (Assignment)**—available for Arria GX, Arria II GX, Cyclone II, Cyclone III, HardCopy II, HardCopy III, Stratix II, Stratix II GX, Stratix III, and Stratix IV devices only

- **Power Analysis (Assignment)**—available for Stratix III and Stratix IV devices only

In the Chip Planner, layers allow you to specify the graphic elements that are displayed for a given task. You can turn off the display of specific graphic elements to increase the window refresh speed and reduce visual clutter when viewing complex designs. The **Background Color Map** can indicate the **Block Utilization**, **Routing Utilization**, **Physical Timing Estimate**, **I/O Banks**, or the High speed-Low power Tiles. When you select **Design Partition Planner** in the **Background Color Map** settings, the resources used by each partition are displayed in the Chip Planner with the same colors used for these partitions in the Design Partition Planner. For example, **Routing Utilization** indicates the relative routing utilization, and **Physical Timing Estimate** indicates the relative physical timing.

Each predefined task in the Chip Planner has a **Background Color Map**, a set of displayed layers, and an editing mode associated with the task. Click the Layers icon (shown in Figure 12–1) to display the Layers Settings window (Figure 12–2). In this window you can select the layers and background color map for each task.

Figure 12–2. Layers in the Chip Planner



The Chip Planner operates in either **Assignment** or **ECO** mode. You can perform design analyses in either of these modes. Use the **Floorplan Editing (Assignment)** task in the **Assignment** mode to manipulate LogicLock regions and location assignments in your design. The **Post Compilation Editing (ECO)** task in **ECO** mode allows you to implement ECO changes in your design. The **Partition Display (Assignment)** task allows you to view the placement of nodes and color codes the nodes based on their partition. When you select the **Clock Regions (Assignment)** task, you can see the regions in your device that are driven by global clock networks. The **Power Analysis (Assignment)** task allows you to view high and low power resources in Stratix III and Stratix IV devices.

For more information about the **ECO** mode of operation, refer to the *Engineering Change Management with the Chip Planner* chapter in volume 2 of the *Quartus II Handbook*.

You can also create and save your own custom tasks. When you create a custom task, you can turn on or off any layer by checking the appropriate box located next to each layer. You can also select different **Background Color Maps** for your custom task. After selecting the required settings, click **Save Task As** to save your custom task.

LogicLock Regions

LogicLock regions are regions you define on the device. You can use LogicLock regions to create a floorplan for your design. Your floorplan can contain several LogicLock regions. A LogicLock region is defined by its height, width, and location. You can specify the size or location of a region, or both, or the Quartus II software can generate these properties automatically. The Quartus II software bases the size and location of a region on the contents of the region and the timing requirements of the module. Table 12–2 describes the options for creating LogicLock regions.

Table 12–2. Types of LogicLock Regions

Properties	Values	Behavior
State	Floating (default), Locked	Floating regions allow the Quartus II software to determine the location of the region on the device. Locked regions are areas that you define and are shown with a solid boundary in the floorplan. A locked region must have a fixed size.
Size	Auto (default), Fixed	Auto-sized regions allow the Quartus II software to determine the appropriate size of a region given its contents. Fixed regions have a shape and size that you define.
Reserved	Off (default), On, Limited	The reserved property allows you to define whether the Fitter can use the resources within a region for entities that are not assigned to the region. If the reserved property is turned on, only items assigned to the region can be placed within its boundaries. When you set it to limited, the Fitter does not place any logic from the parent region.
Origin	Any Floorplan Location	The origin is the origin of the LogicLock region's placement on the floorplan. For Arria GX, Stratix, and Cyclone series devices, and MAX II devices, the origin is located in the lower left corner. For other Altera® device families, the origin is located in the upper left corner.

The Quartus II software cannot automatically define the size of a region if the location is locked. Therefore, if you want to specify the exact location of the region, you must also specify the size.

You can use the Design Partition Planner in conjunction with LogicLock regions to create a floorplan for your design. For more information about using the Design Partition Planner, refer to the *Quartus II Incremental Compilation for Hierarchical and Team-Based Designs* and the *Best Practices for Incremental Compilation Partition and Floorplan Assignments* chapters in volume 1 of the *Quartus II Handbook*.

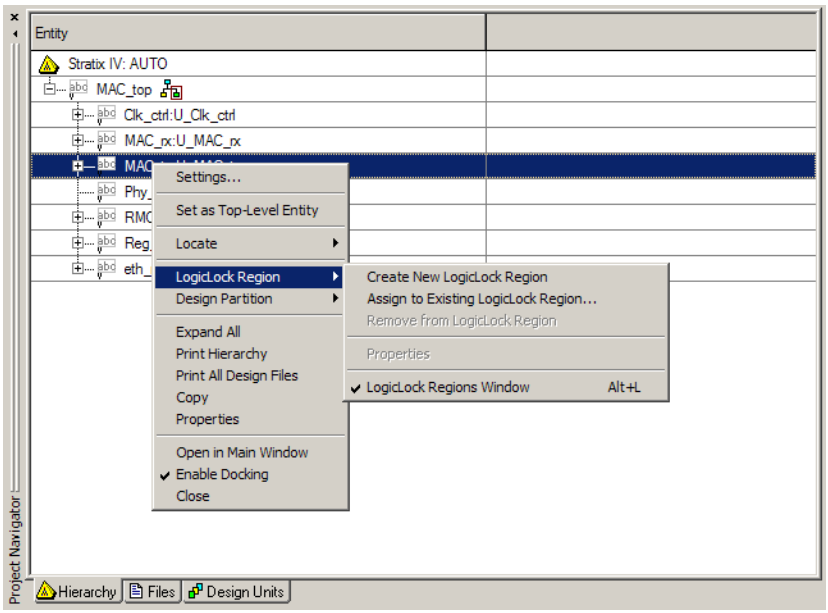
Creating LogicLock Regions

You can create LogicLock Regions from the Project Navigator, the LogicLock Regions window, or the Chip Planner.

Creating LogicLock Regions from the Quartus II User Interface

After you perform either a full compilation or analysis and elaboration on the design, the Quartus II software displays the hierarchy of the design. On the View menu, click **Project Navigator.** With the hierarchy of the design fully expanded, as shown in Figure 12–3, right-click on any design entity in the design, and click **Create New LogicLock Region** to create a LogicLock region.

Figure 12–3. Using the Project Navigator to Create LogicLock Regions



Placing LogicLock Regions

A fixed region must contain all resources required for the design block for which you define the region. Although the Quartus II software can automatically place and size LogicLock regions to meet resource and timing requirements, you can manually place and size regions to meet your design requirements. To do so, follow these guidelines:

- Place LogicLock regions with pin assignments on the periphery of the device, adjacent to the pins. For the Arria GX, Stratix, and Cyclone series of devices and MAX II devices, you must also include the I/O block within the LogicLock Region.

- Floating LogicLock regions can overlap with their ancestors or descendants, but not with other floating LogicLock regions.
- Avoid creating fixed and locked regions that overlap.

If you want to import multiple instances of a module into a top-level design, you must ensure that the device has two or more locations with exactly the same device resources. (You can determine this from the applicable device handbook.) If the device does not have another area with exactly the same resources, the Quartus II software generates a fitting error during compilation of the top-level design.

When you import a LogicLock region, the Quartus II software changes the property to **floating** and assigns a new unique name. You can change the property to **fixed** to guarantee the same placement achieved previously. You can import or export LogicLock regions across devices within a family, but not between families.

Placing Device Features into LogicLock Regions

A LogicLock region includes all device resources within its boundaries, including memory and pins. You can assign pins to LogicLock regions; however, this placement puts location constraints on the region. When the Quartus II software places a floating auto-sized region, it places the region in an area that meets the requirements of the contents of the LogicLock region.

Pin assignments to LogicLock regions are effective only in fixed and locked regions. Pin assignments to floating regions do not influence the placement of the region.

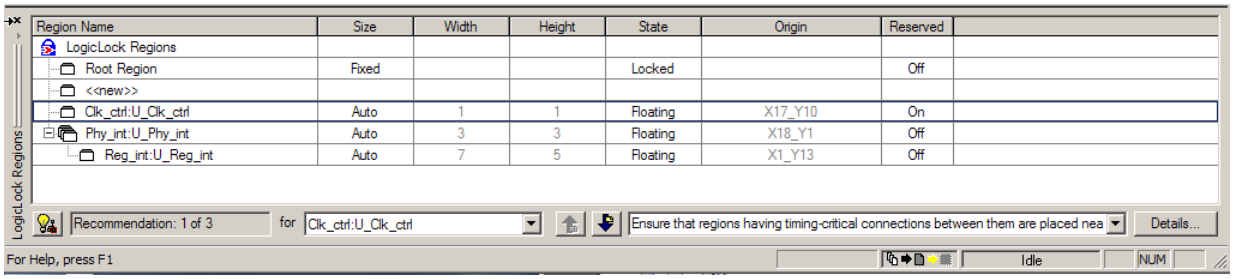
Only one LogicLock region can claim a device resource. If the boundary includes part of a device resource, the Quartus II software allocates the entire resource to the LogicLock region.

LogicLock Regions Window

The LogicLock window consists of the LogicLock Regions window (Figure 12–4) and the **LogicLock Region Properties** dialog box. Use the LogicLock Regions window to create LogicLock regions and assign nodes and entities to them. The dialog box provides a summary of all LogicLock regions in your design. In the LogicLock Regions window, you can modify the properties of a LogicLock region such as size, state, width, height, origin, and whether the region is a reserved region. The LogicLock Regions window also has a recommendations toolbar at the bottom. Select a LogicLock region from the drop-down list in the recommendations toolbar to display the relevant suggestions to optimize that LogicLock region.

The origin location varies, depending on the device family. For Arria GX, Cyclone, Stratix, and MAX II devices, the origin of the LogicLock region is located at the lower-left corner of the region. For all other supported devices, the origin is located at the upper-left corner of the region.

Figure 12–4. LogicLock Regions Window



You can customize the LogicLock Regions window by dragging and dropping the columns to change their order. Columns can also be hidden.

For designs that target Arria GX, Cyclone, Stratix, and MAX II devices, the Quartus II software automatically creates a LogicLock region that encompasses the entire device. This default region is labelled `Root_region`, and is locked and fixed.

Use the **LogicLock Region Properties** dialog box to obtain detailed information about your LogicLock region, such as which entities and nodes are assigned to your region and which resources are required. The **LogicLock Region Properties** dialog box shows the properties of the current selected regions. You can also modify the settings for LogicLock regions in the **LogicLock Region Properties** dialog box.

To open the **LogicLock Region Properties** dialog box, double-click any region in the LogicLock Regions window, or right-click the region and click **Properties**.

Creating LogicLock Regions with the Chip Planner

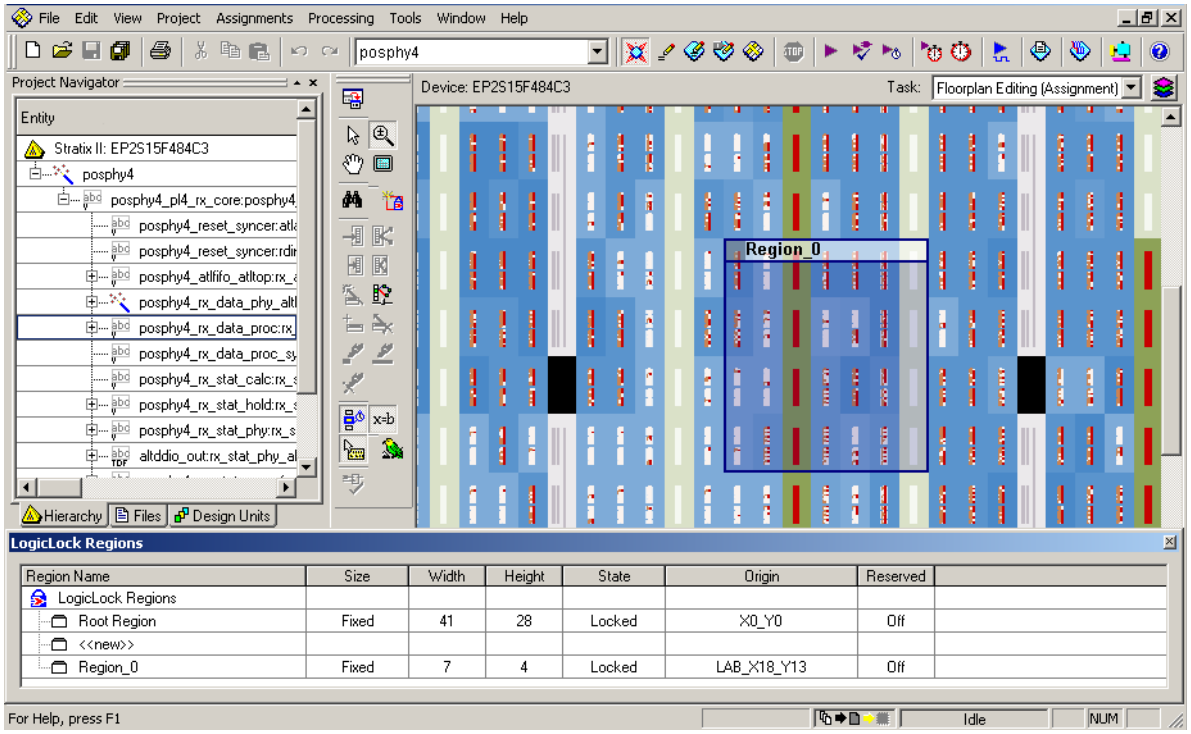
In the View menu of the Chip Planner, click **Create LogicLock Region**. In the Chip Planner, click and drag to create a region of your preferred location and size.

Assigning LogicLock Region Content

After you have created a LogicLock region, you must assign resources to it using the Chip Planner, the **LogicLock Regions** dialog box, or a Tcl script.

You can drag selected logic displayed in the **Hierarchy** tab of the Project Navigator, in the Node Finder, or in a schematic design file, and drop it into the Chip Planner or the **LogicLock Regions** dialog box. Figure 12–5 shows logic that has been dragged from the **Hierarchy** tab of the Project Navigator and dropped into a LogicLock region in the Chip Planner.

Figure 12–5. Drag and Drop Logic in the Chip Planner



You can also drag logic from the **Hierarchy** tab of the Project Navigator and drop it in the LogicLock Regions **Properties** dialog box. Logic can also be dropped into the **Design Element Assigned** column of the **Contents** tab of the **LogicLock Region Properties** box.

You must assign pins to a LogicLock region manually. The Quartus II software does not include pins automatically when you assign an entity to a region. The software only obeys pin assignments to locked regions that border the periphery of the device. For the Cyclone, Stratix, and MAX II series of devices, the locked regions must include the I/O pins as resources.

Hierarchical (Parent and Child) LogicLock Regions

You can define a hierarchy for a group of regions by declaring parent and child regions. The Quartus II software places a child region completely within the boundaries of its parent region, allowing you to further constrain module locations. Additionally, parent and child regions allow you to further improve the performance of a module by constraining the nodes in the critical path of the module.

To make one LogicLock region a child of another LogicLock region, in the LogicLock Regions window, select the new child region and drag and drop it inside its new parent region.

The LogicLock region hierarchy does not have to be the same as the design hierarchy.

You can create both fixed and floating LogicLock regions within a fixed parent LogicLock region. The location of a floating child region can float within its parent. If a child region is fixed, its location remains locked relative to its parent's origin. A locked parent region's location is locked relative to the device. If the child's location is locked and the parent's location is changed, the child's origin changes, but maintains the same placement relative to the origin of its parent. Either you or the Quartus II software can determine a child region's size; however, the child region must fit entirely within the parent region. The levels of hierarchy in LogicLock regions are unlimited, but complicated hierarchical regions might result in some LABs not being utilized; thus, effectively increasing the resource utilization in the device.

Reserved LogicLock Region

The Quartus II software honors all entity and node assignments to LogicLock regions. Occasionally, entities and nodes do not occupy an entire region, which leaves some of the region's resources unoccupied. To increase the region's resource utilization and performance, the Quartus II software's default behavior fills the unoccupied resources with other nodes and entities that have not been assigned to another region. You can prevent this behavior by turning on **Reserved** on the **General** tab of the **LogicLock Region Properties** dialog box. When you turn on this option, your LogicLock region contains only the entities and nodes that you specifically assigned to your LogicLock region. When you set the reserved property for a LogicLock region, the Fitter does not place logic from the immediate parent LogicLock region in the assigned LogicLock area, but it might place logic from other parts of your design in that area.

In a team-based design environment, the **Limited** option helps you create a device floorplan. When this option is turned on, each team can be assigned a portion of the device floorplan where placement and optimization of each submodule occurs. Device resources can be distributed to each module without affecting the performance of other modules.

Creating Non-Rectangular LogicLock Regions

When you create a floorplan for your design, you may want to create non-rectangular LogicLock regions to make some device resources accessible to design blocks outside a LogicLock region. You might also create a non-rectangular LogicLock region to place certain parts of your design around specific device resources to improve performance. You can create non-rectangular LogicLock regions in two ways: with the **Merge** command in the Chip Planner, or with the reserved property of LogicLock regions.

Creating Non-Rectangular LogicLock Regions Using the Merge Command

The **Merge** command is available for Arria II GX, Cyclone III series, Cyclone IV, HardCopy III, HardCopy IV, Stratix III, and Stratix IV series device families. To create a non-rectangular region with the **Merge** command, follow these steps:

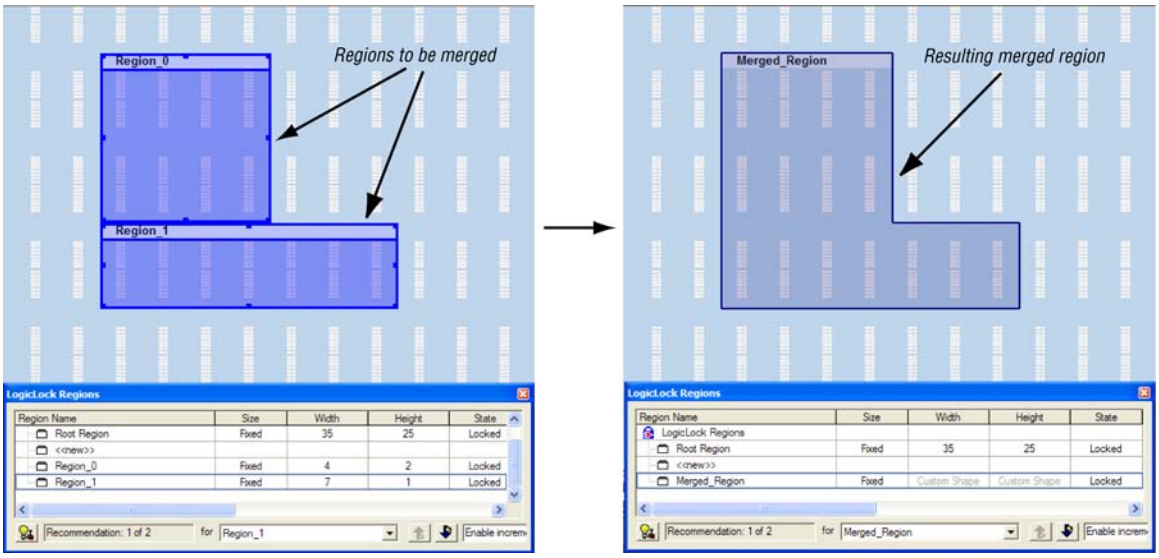
1. In the Chip Planner, create two or more contiguous or non-contiguous rectangular regions as described in "Creating LogicLock Regions" on page 12–7.
2. Arrange the regions that you have created into the locations where you want the non-rectangular region to be.

3. Select all the individual regions to be merged by clicking each of them while holding the Shift key.
4. Right-click the title bar of any of the LogicLock regions that you want to merge, point to **LogicLock regions**, and then click **Merge**. The individual regions that you have selected are now merged to create a single new region.

By default, the new LogicLock region bears the name of the component region containing the greatest number of resources; however, you can rename the new region. In the **LogicLock Regions window**, the new region is shown as having a custom shape.

Figure 12–6 illustrates two autonomous LogicLock regions combined using the **Merge** command to form a new non-rectangular region.

Figure 12–6. Using the **Merge** command to create a non-rectangular region

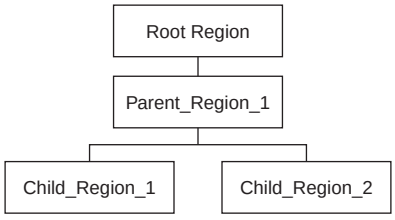


Creating Non-Rectangular Regions Using Reserved LogicLock Regions

For all devices not supported by the **Merge** command, you can use the reserved property of LogicLock regions to create regions that are non-rectangular or non-contiguous.

For example, consider a case in which there is one LogicLock region under the Root region and two child regions under this region (Figure 12–7).

Figure 12–7. Example 1

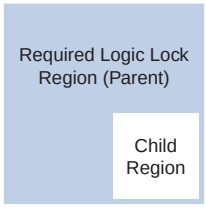


You can set the **Reserved** property of a LogicLock region to **On**, **Off**, or **Limited**. If you create a LogicLock region for Child_Region_1 with its **Reserved** property set to **Limited**, the Fitter does not place nodes that are members of Parent_Region_1 or Child_Region_2 into the boundary of Child_Region_1. However, if Child_Region_2 overlaps Child_Region_1, then logic can be placed in the overlapping area. The Fitter can also place nodes that are not members of Parent_Region_1 or Child_Region_1 (such as members of the Root_Region) into Child_Region_1. On the other hand, if Child_Region_1 is set to exclude all non-members, the Fitter can only place nodes that are members of Child_Region_1 into the region.

If the Parent Region's reserved property is turned off, then the Fitter might place other logic in the allocated region.

If you want to create a non-rectangular region as shown in Figure 12–8, you can create two rectangular hierarchical LogicLock regions. Turn off the reserved property on the parent LogicLock region and set the reserved property on the child LogicLock region to **Limited** to prevent the Fitter from placing any logic of the module assigned to the parent LogicLock region. Logic that is external to the parent LogicLock region might be placed in the area allocated to the child region. This produces a non-rectangular LogicLock region.

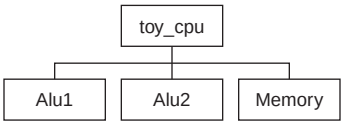
Figure 12–8. Non-Rectangular Region



Examples of Non-Rectangular LogicLock Regions Using Reserved Property

The following examples use the design hierarchy shown in Figure 12–9.

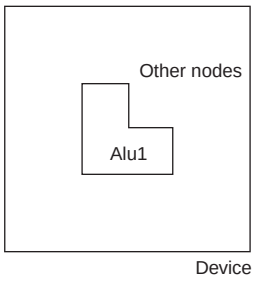
Figure 12–9. An Example Design Hierarchy



Example 1: Creating an L-Shaped Region

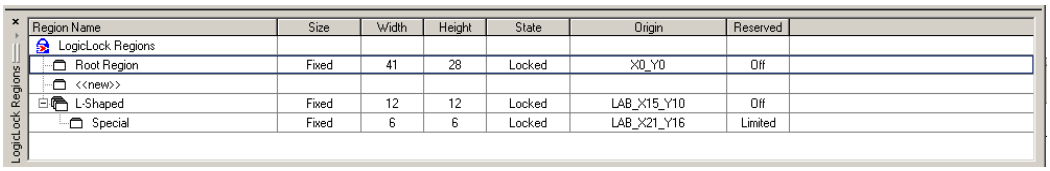
In the design hierarchy example in Figure 12–9, suppose you want to create an L-shaped region, such that the Alu1 module is placed completely inside the region, and the non-Alu1 nodes can be placed anywhere on the chip (as shown in Figure 12–10).

Figure 12–10. Creating an L-Shaped Region



The L-shaped region defines a rectangular region that is carved out by a child LogicLock region (**Special**) to achieve the L-shape effect. The **Reserved** property of this child LogicLock region is set to **Limited**, such that the Fitter does not require logic from members of Alu1 (which is the parent region of the region named **Special**) inside it while letting other nodes in. Not displayed in Figure 12–10, the Alu1 entity instance is assigned as a member to the L_Shaped region. This effect can be achieved by creating a hierarchical LogicLock region as shown in Figure 12–11.

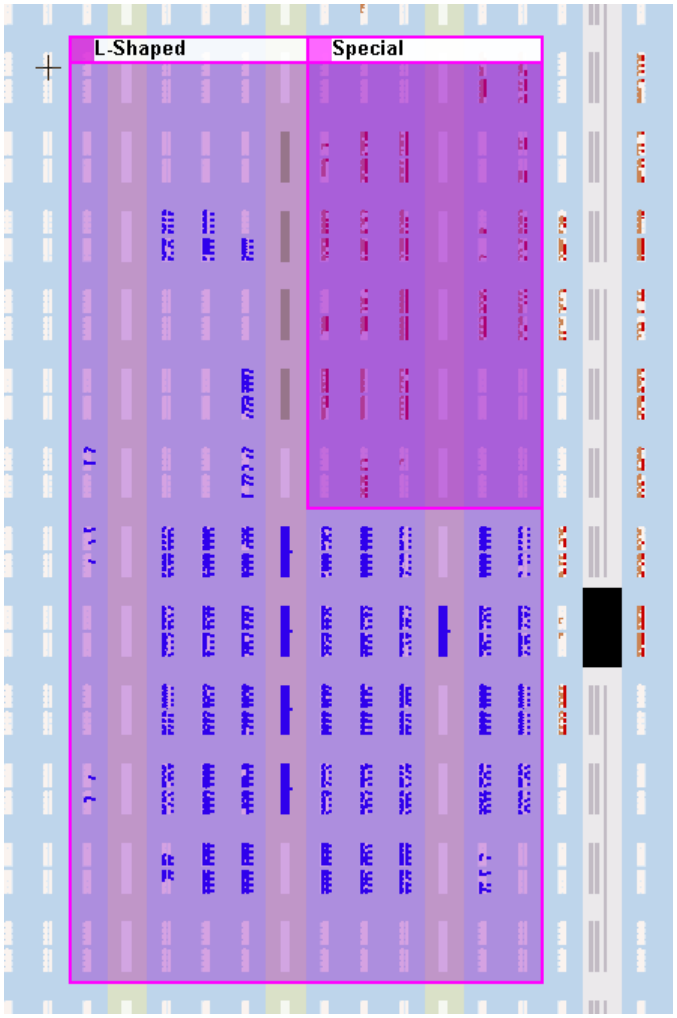
Figure 12–11. Hierarchical LogicLock Region



Region Name	Size	Width	Height	State	Origin	Reserved
LogicLock Regions						
Root Region	Fixed	41	28	Locked	X0_Y0	Off
<<new>>						
L-Shaped	Fixed	12	12	Locked	LAB_X15_Y10	Off
Special	Fixed	6	6	Locked	LAB_X21_Y16	Limited

Figure 12–12 illustrates the expected fitting results with these LogicLock regions. Nodes from the Alu1 entity instance are colored blue, while nodes from the rest of the design are colored red.

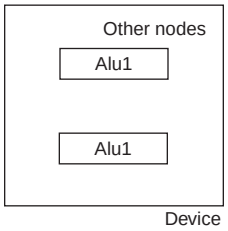
Figure 12–12. Expected Fitting Results with LogicLock Regions



Example 2: Region with Disjoint Areas

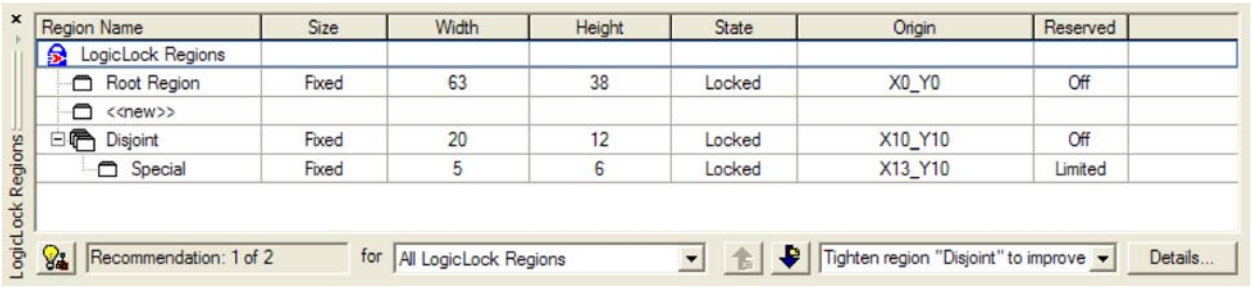
Suppose you want to create a region consisting of two disjoint rectangles (or any number of disjoint areas), such that the Alu1 module is placed completely inside the region, and the non-Alu1 nodes can be placed anywhere on the chip as shown in Figure 12–13.

Figure 12–13. Region Consisting of Two Disjointed Rectangles



You can achieve a region with disjoint areas using the region hierarchy example in Figure 12–14.

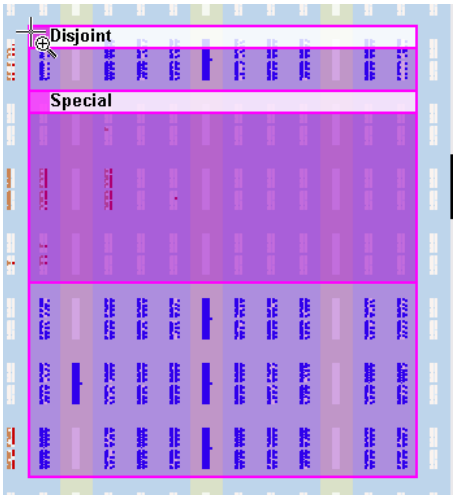
Figure 12–14. Region with Disjoint Areas



The disjoint region defines a rectangular region that is carved out by the Special child region to achieve the disjoint effect. Notice that the Special region is set to reserved "from members of parent region hierarchy" to prevent the Alu1 nodes from being placed inside it, while letting other nodes in. The Alu1 entity instance should be assigned to the Disjoint LogicLock region.

Figure 12–15 shows the expected fitting results with the LogicLock regions. Nodes from the Alu1 entity instance are colored blue, while nodes from the rest of the design are colored red and brown.

Figure 12–15. Expected Fitting Results with the LogicLock Regions



Hierarchial LogicLock assignments can increase resource usage in the device, because some design blocks might not have access to resources inside the LogicLock regions. When you create hierarchial LogicLock regions to create non-rectangular regions, keep the hierarchy assignments simple, to minimize increase in resource usage.

Excluded Resources

The Excluded Resources feature allows you to easily exclude specific device resources such as DSP blocks or M4K memory blocks from a LogicLock region. For example, you can specify resources that belong to a specific entity that are assigned to a LogicLock region, and specify that these resources be included with the exception of the DSP blocks. Use the Excluded Resources feature on a per-LogicLock region member basis.

To exclude certain device resources from an entity, in the **LogicLock Region Properties** dialog box, highlight the entity in the **Design Element** column, and click **Edit**. In the **Edit Node** dialog box, under **Excluded Element Types**, click the Browse button. In the **Excluded Resources Element Types** dialog box, you can select the device resources you want to exclude from the entity. When you have selected the resources to exclude, the **Excluded Resources** column is updated in the **LogicLock Region Properties** dialog box to reflect the excluded resources.

The Excluded Resources feature prevents certain resource types from being included in a region, but it does not prevent the resources from being placed inside the region unless the region's **Reserved** property is set to **On**. To indicate to the Fitter that certain resources are not required inside a LogicLock region, define a resource filter.

Additional Quartus II LogicLock Design Features

To complement the **LogicLock Regions** dialog box, the Quartus II software has additional features to help you design with LogicLock regions.

Tooltips

When you move the mouse pointer over a LogicLock region name on the **LogicLock Regions** dialog box, or over the top bar of the LogicLock region in the Chip Planner, the Quartus II software displays a tooltip with information about the properties of the LogicLock region.

Analysis and Synthesis Resource Utilization by Entity

The Compilation Report contains an **Analysis and Synthesis Resource Utilization by Entity** section, which reports accurate resource usage statistics, including entity-level information. You can use this feature when you manually create LogicLock regions.

Path-Based Assignments

You can assign paths to LogicLock regions based on source and destination nodes, allowing you to easily group critical design nodes into a LogicLock region. Any of the following types of nodes can be the source and destination nodes:

- Valid register-to-register path—the source and destination nodes must be registers
- Valid pin-to-register path—the source node is a pin and the destination node is a register
- Valid register-to-pin path—the source node is a register and the destination node is a pin
- Valid pin-to-pin path—both the source and destination nodes are pins

To open the **Paths** dialog box, on the **General** tab of the **Logic Lock Regions** dialog box, click **Add Path**.

Both "*" and "?" wildcard characters are allowed for the source and destination nodes. When creating path-based assignments, you can exclude specific nodes using the **Name exclude** field in the **Paths** dialog box. The Quartus II software ignores all paths passing through the nodes that match the setting in the **Name exclude** field. For example, consider a case with two paths between the source and destination—one passing through node A and the other passing through node B. If you specify node B in the **Name exclude** field, only the path assignment through node A is valid.

You can also use the Quartus II Timing Analysis Report to create path-based assignments by following these steps:

1. Expand the **Timing Analyzer** section in the Compilation Report.
2. Select any of the clocks in the section labeled "Clock Setup:<*clock name*>."
3. Locate a path that you want to assign to a LogicLock region. Drag this path from the Report window and drop it in the appropriate row in the LogicLock Region pane in the Quartus II GUI.

This operation creates a path-based assignment from the source register to the destination register, as shown in the Timing Analysis Report.

Quartus II Revisions Feature

When you evaluate different LogicLock regions in your design, you might want to experiment with different configurations to achieve your desired results. The Quartus II Revisions feature provides a convenient way to organize the same project with different settings until you find an optimum configuration.

To use the Revisions feature, on the Project menu, click **Revisions**. In the **Revisions** dialog box, you can create and specify revisions. Revision can be based on the current design or any previously created revisions. Each revision can have an associated description. Revisions are a convenient way to organize the placement constraints created for your LogicLock regions.

LogicLock Assignment Precedence

Conflicts can arise during the assignment of entities and nodes to LogicLock regions. For example, an entire top-level entity might be assigned to one region and a node within this top-level entity assigned to another region. To resolve conflicting assignments, the Quartus II software maintains an order of precedence for LogicLock assignments. The following order of precedence, from highest to lowest, applies:

- Exact node-level assignments
- Path-based and wildcard assignments
- Hierarchical assignments

Conflicts can arise within path-based and wildcard assignments when one path-based or wildcard assignment contradicts another path-based or wildcard assignment. For example, a path-based assignment is made containing a node labeled X and assigned to LogicLock region PATH_REGION. A second assignment is made using wildcard assignment X* with node X being placed into region WILDCARD_REGION. As a result of these two assignments, node X is assigned to two regions: PATH_REGION and WILDCARD_REGION.

To resolve this type of conflict, the Quartus II software maintains the order in which the assignments were made and grants the higher priority to the most recently created assignment.

Open the **Priority** dialog box by selecting **Priority** on the **General** tab of the **LogicLock properties** dialog box. You can change the priority of path-based and wildcard assignments with the **Up** and **Down** buttons in the **Priority** dialog box. To prioritize assignments between regions, you must select multiple LogicLock regions and then open the **Priority** dialog box from the LogicLock Properties window.

Normally, all nodes assigned to a particular LogicLock region reside within the boundaries of that region.

Virtual Pins

Usually, when you compile a design in the Quartus II software, all I/O ports are directly mapped to pins on the targeted device. However, there may be situations where you do not want to map all I/O ports to the device pins; use the Virtual Pin assignment in such cases.

A virtual pin is an I/O element which you do not intend to bring to the chip pins. You can create a virtual pin by assigning the Virtual Pin logic option to an I/O element. When you compile a design with some I/O elements assigned as virtual pins, those I/O elements are mapped to a logic element and not to a pin during compilation, and are then implemented as a LUT. You might use virtual pin assignments when you compile a partial design, because not all the I/Os from a partial design may drive chip pins at the top level.

The Virtual Pin assignment communicates to the Quartus II software which I/O ports of the design module are internal nodes in the top-level design. These assignments prevent the number of I/O ports in the lower-level modules from exceeding the total number of available device pins. Every I/O port that is designated a virtual pin is mapped to either an LCELL or an adaptive logic module (ALM), depending on the target device.

Bidirectional, registered I/O pins, and I/O pins with output enable signals cannot be virtual pins.

In the top-level design, these virtual pins are connected to an internal node of another module. By making assignments to virtual pins, you can place those pins in the same location or region on the device as that of the corresponding internal nodes in the top-level module. The Virtual Pin option can be useful when compiling a LogicLock module with more pins than the target device allows. The Virtual Pin option can enable timing analyses that more closely match the performance of the LogicLock module when it is integrated into the top-level design.

Apply the following guidelines when creating virtual pins in the Quartus II software:

- Do not declare clock pins as virtual pins
- Nodes or signals that drive physical device pins in the top-level design should not be declared as virtual pins

In the Node Finder, you can set **Filter Type** to **Pins: Virtual** to display all assigned virtual pins in the design. From the Assignment Editor, to access the Node Finder, double-click the **To** field; when the arrow appears on the right side of the field, click the arrow and select **Node Finder**.

Using LogicLock Regions in the Chip Planner

You can easily edit properties of existing LogicLock regions or assign resources to them in the Chip Planner. You can also create new LogicLock regions using the Chip Planner.

Viewing Connections Between LogicLock Regions in the Chip Planner

You can view and edit LogicLock regions using the Chip Planner. Select the **Floorplan Editing (Assignment)** task or any task with the **User-assigned LogicLock regions** setting enabled to manipulate LogicLock regions.

The Chip Planner shows the connections between LogicLock regions. By default, each connection is represented as an individual line drawn between LogicLock regions. You can choose to display connections between LogicLock regions as a single bundled connection rather than as individual connection lines. To use this option, open the Chip Planner floorplan and on the View menu, click **Generate Inter-region Bundles**.

In the **Generate Inter-region Bundles** dialog box, specify the **Source node to region fanout less than** and the **Bundle width greater than** values.

For more information about the **Generate Inter-region Bundles** dialog box, refer to the Quartus II Help.

Design Floorplan Analysis Using the Chip Planner

The Chip Planner helps you visually analyze the floorplan of your design at any stage of your design cycle. With the Chip Planner, you can view post-compilation placement, connections, and routing paths. You can also create LogicLock regions and location assignments. The Chip Planner allows you to create new logic cells and I/O atoms and to move existing logic cells and I/O atoms using the architectural floorplan of your design. You can also see global and regional clock regions within the device, and the connections between both I/O atoms and PLLs and the different clock regions.

From the Chip Planner, you can launch the Resource Property Editor, which you can use to change the properties and parameters of device resources, and modify connectivity between certain types of device resources. The Change Manager records any changes that you make to your design floorplan, so that you can selectively undo changes if necessary.

For more information about the Resource Property Editor and the Change Manager, refer to the *Engineering Change Management with the Chip Planner* chapter in volume 2 of the *Quartus II Handbook*.

The following sections present Chip Planner floorplan views and design analysis procedures which you can use with any predefined task—unless explicitly stated that a given procedure requires a specific task or editing mode).

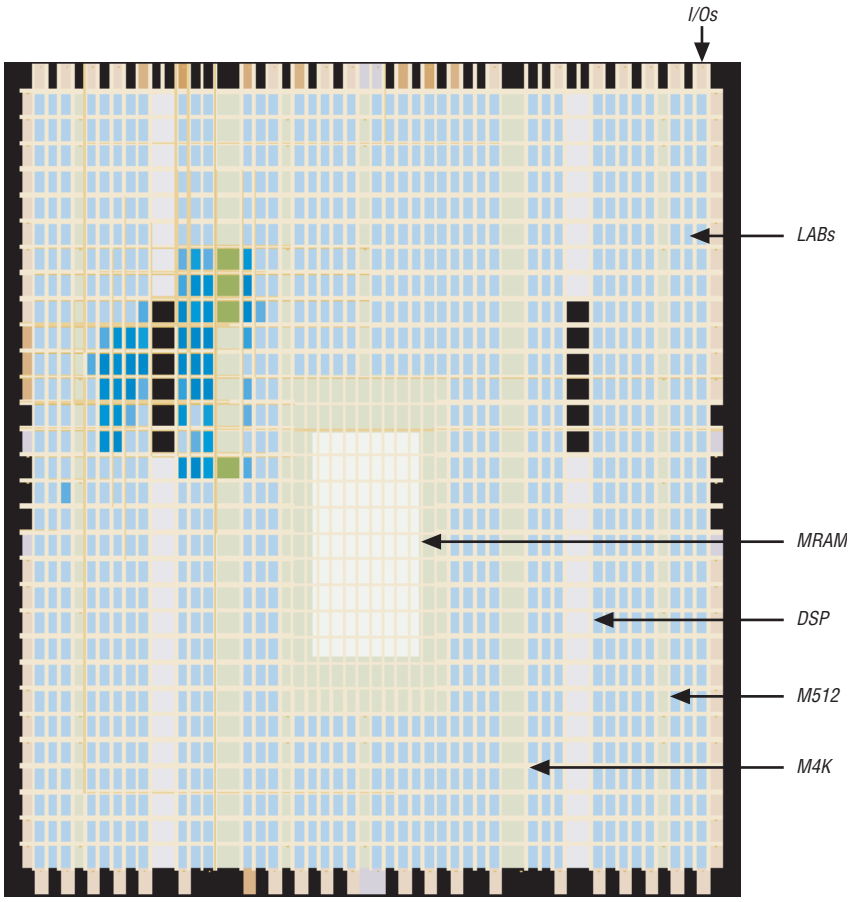
Chip Planner Floorplan Views

The Chip Planner uses a hierarchical zoom viewer that shows various abstraction levels of the targeted Altera device. As you zoom in, the level of abstraction decreases, revealing more detail about your design.

First-Level View

The first level provides a high-level view (LAB level view) of the entire device floorplan. You can locate a node and view the placement of that node in your design. Figure 12–16 shows the Chip Planner's Floorplan first-level view of a Stratix device.

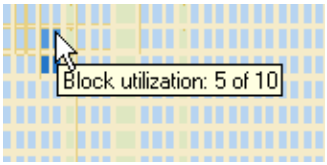
Figure 12–16. Chip Planner's First-Level Floorplan View



Each resource is shown in a different color. The Chip Planner floorplan uses a gradient color scheme in which the color becomes darker as the utilization of a resource increases. For example, as more LEs are used in the logic array block (LAB), the color of the LAB becomes darker.

When you place the mouse pointer over a resource at this level, a tooltip appears that briefly describes the utilization of the resource (Figure 12–17).

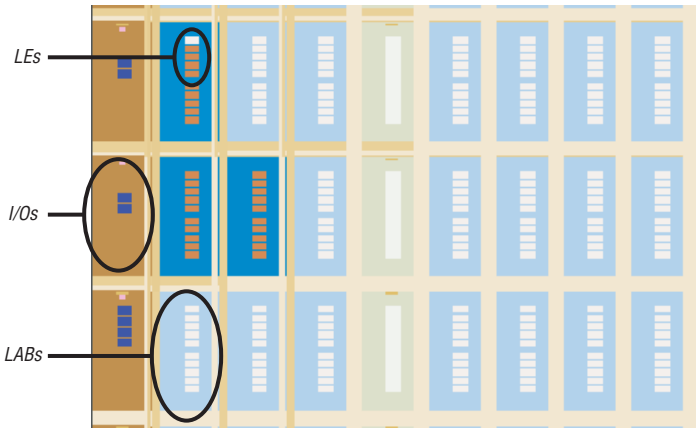
Figure 12–17. Tooltip Message: First-Level View



Second-Level View

As you zoom in, the level of detail increases. Figure 12–18 shows the second-level view of the Chip Planner Floorplan for a Stratix device.

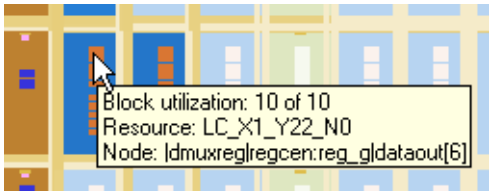
Figure 12–18. Chip Planner's Second-Level Floorplan View



At this zoom level, the contents of LABs and I/O banks and the routing channels that connect resources are all visible.

When you place the mouse pointer over an LE or ALM at this level, a tooltip is displayed (Figure 12–19) that shows the name of the LE/ALM, the location of the LE/ALM, and the number of resources that are used with that LAB. When you place the mouse pointer over an interconnect, the tooltip shows the routing channels that are used by that interconnect. At this zoom level, you can move LEs, ALMs, and I/Os from one physical location to another.

Figure 12–19. Tooltip Message: Second-Level View



Third-Level View

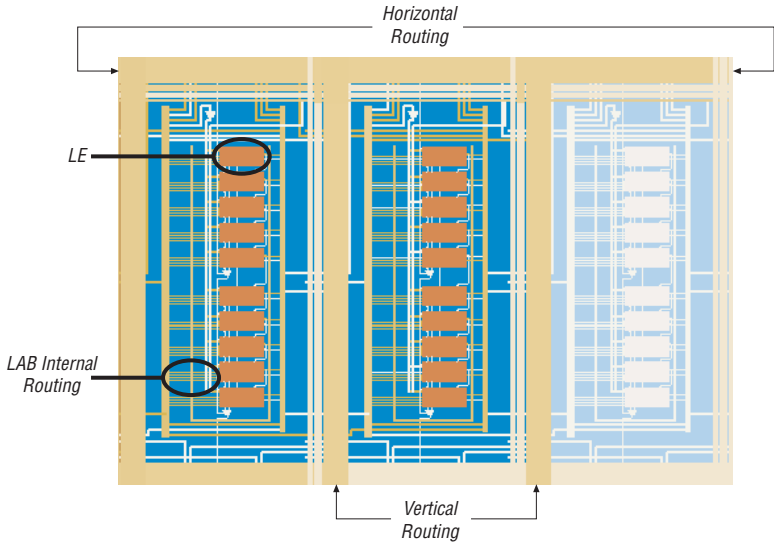
The third level provides a more detailed view, displaying each routing resource that is used within a LAB in the FPGA. Figure 12–20 shows the level of detail at the third-level view for a Stratix device.

From the third level, you can move LEs, ALMs, and I/Os from one physical location to another. You can move a resource by selecting, dragging, and dropping it into the desired location. At this level, you can also create new LEs and I/Os when you are in the post-compilation (ECO) mode.

You can delete a resource only after all of its fan-out connections are removed. Moving nodes in the **Floorplan Editing (Assignment)** task creates an assignment. However, if you move logic nodes in the **Post-Compilation Editing (ECO)** task, that change is considered an ECO change. For more information about Floorplan Assignments, refer to "Viewing Assignments in the Chip Planner" on page 12–39.

For more information about performing ECOs, refer to the *Engineering Change Management with the Chip Planner* chapter in volume 2 of the *Quartus II Handbook*.

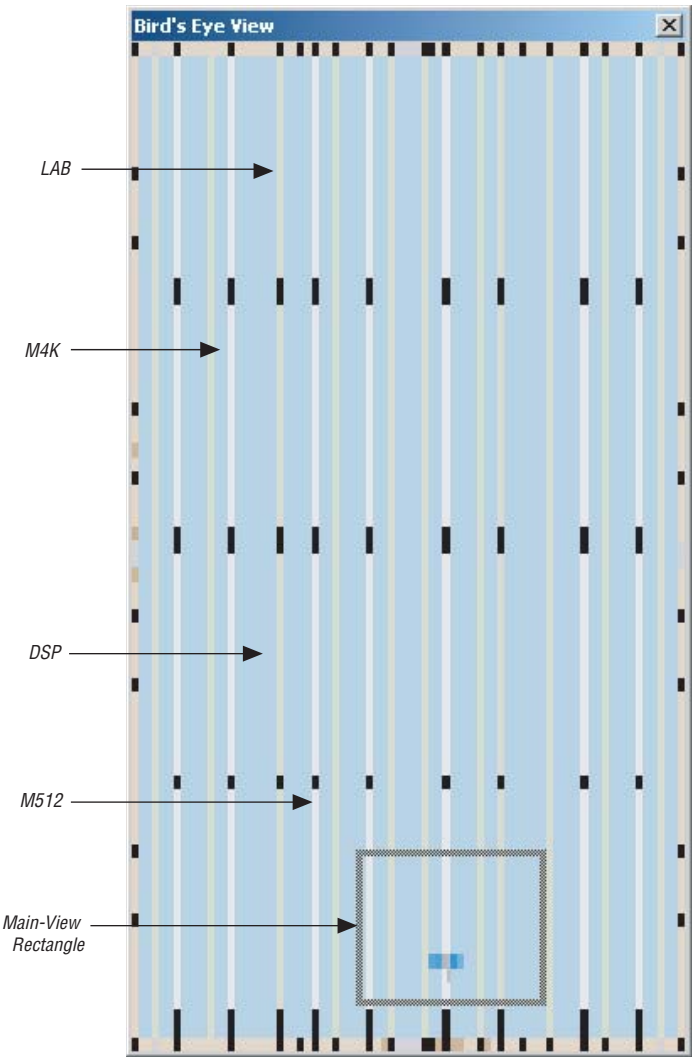
Figure 12–20. Chip Planner's Third-Level Floorplan View



Bird's Eye View

The Bird's Eye View (Figure 12–21) displays a high-level picture of resource usage for the entire chip and provides a fast and efficient way to navigate between areas of interest in the Chip Planner.

Figure 12–21. Bird's Eye View



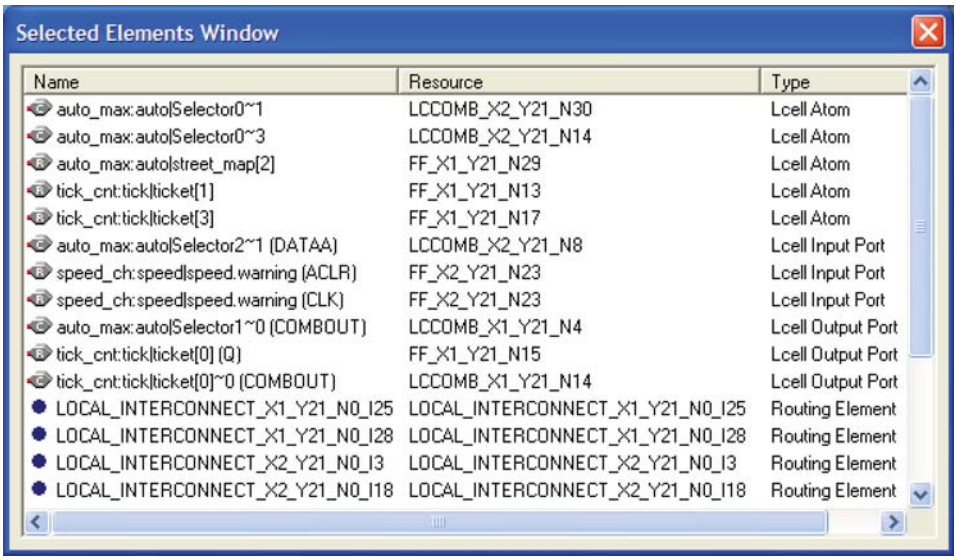
The Bird's Eye View is a separate window that is linked to the Chip Planner floorplan. When you select an area of interest in the Bird's Eye View, the Chip Planner floorplan automatically refreshes to show that region of the device. As you change the size of the main-view rectangle in the Bird's Eye View window, the main Chip Planner floorplan window also zooms in (or zooms out). You can make the main-view rectangle smaller in the Bird's Eye View to see more detail on the Chip Planner floorplan window by right-clicking and dragging inside the Bird's Eye View.

You can use the Bird's Eye View when you are interested in resources at opposite ends of the chip, and you want to quickly navigate between resource elements without losing your frame of reference.

Selected Elements Window

The Selected Elements Window lists the objects (such as atoms, paths, LogicLock regions, or routing elements) currently selected in the Chip Planner. To display the Selected Elements Window, click **Selected Elements Window** on the **View** menu in the Chip Planner.

Figure 12–22. Selected Elements Window



Viewing Architecture-Specific Design Information

With the Chip Planner, you can view the following architecture-specific information related to your design:

- **Device routing resources used by your design**—View how blocks are connected, as well as the signal routing that connects the blocks.
- **LE configuration**—View how a logic element (LE) is configured within your design. For example, you can view which LE inputs are used; if the LE utilizes the register, the look-up table (LUT), or both; as well as the signal flow through the LE.
- **ALM configuration**—View how an ALM is configured within your design. For example, you can view which ALM inputs are used, if the ALM utilizes the registers, the upper LUT, the lower LUT, or all of them. You can also view the signal flow through the ALM.
- **I/O configuration**—View how the device I/O resources are used. For example, you can view which components of the I/O resources are used, if the delay chain settings are enabled, which I/O standards are set, and the signal flow through the I/O.
- **PLL configuration**—View how a phase-locked loop (PLL) is configured within your design. For example, you can view which control signals of the PLL are used with the settings for your PLL.
- **Timing**—View the delay between the inputs and outputs of FPGA elements. For example, you can analyze the timing of the `DATAB` input to the `COMBOUT` output.

In addition, you can modify the following properties of an Altera device with the Chip Planner:

- LEs and ALMs
- I/O cells
- PLLs
- Registers in RAM and DSP blocks
- Connections between elements
- Placement of elements

For more information about LEs, ALMs, and other resources of an FPGA device, refer to the relevant device handbook.

Viewing Available Clock Networks in the Device

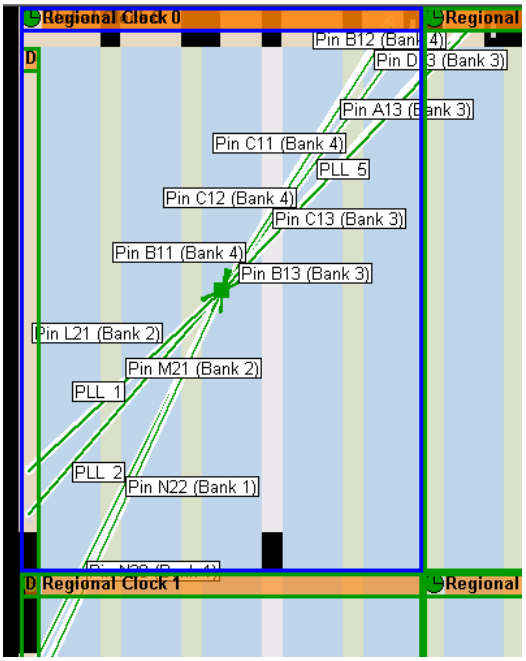
When you select **Clock Regions (Assignment)** from the **Task** list, you can display the areas of the chip that are driven by global and regional clock networks. This global clock display feature is available for Arria GX, Arria II GX, Cyclone II, Cyclone III, HardCopy II, HardCopy III, Stratix II, Stratix II GX, Stratix III, and Stratix IV device families.

When you select the **Clock Regions** task, the Chip Planner displays various types of regional and global clocks and the regions they cover in the device. The connectivity between clock regions, pins, and PLLs is also shown. Clock regions are shown with rectangular overlay boxes with name labels of clock type and index.You can select each clock network region by clicking on it. The clock-shaped icon at the top-left corner indicates that the region represents a clock network region.

Clock types are listed in the Layer Settings window. You can change the color of the clock network in the Chip Planner on the **Options** page of the Tools menu.

You can customize your view of the global clock networks by using the layers setting in the Chip Planner. You can turn on or off the display of all clock regions with the **All types** option. When the selected device does not contain a specific clock region, the option for that category is turned off in the dialog box. Figure 12–23 shows the potential fan-in in the Chip Planner.

Figure 12–23. Potential Fan-In



To trace the possible connectivity to each clock network region, select the clock network region and use the **Generate Potential Fan-In** and **Generate Potential Fan-Out** commands.

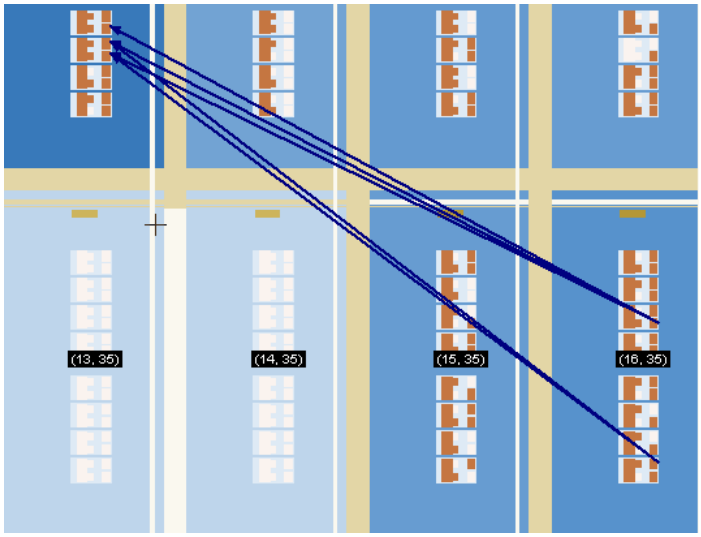
If you are interested in locating the clock regions that a pin or PLL can feed, select the pin or the PLL, then use the **Generate Fan-Out Connections** command. Connection arrows are drawn from the selected pins or PLLs to their clock regions.

When you use the **Generate Fan-In Connections** and **Generate Fan-Out Connections** commands, the Chip Planner shows connections that are actually used in the netlist for the selected clock region.

Viewing Critical Paths

Critical paths are timing paths in your design that have a negative slack. These timing paths can span from device I/Os to internal registers, registers-to-registers, or registers-to-devices I/Os. The View Critical Paths feature displays routing paths in the Chip Planner, as shown in Figure 12–24. The criticality of a path is determined by its slack and is shown in the timing analysis report. Design analysis for timing closure is a fundamental requirement for optimal performance in highly complex designs. The Chip Planner helps you close timing on complex designs with its analytical capability.

Figure 12–24. Chip Planner Showing Critical Path

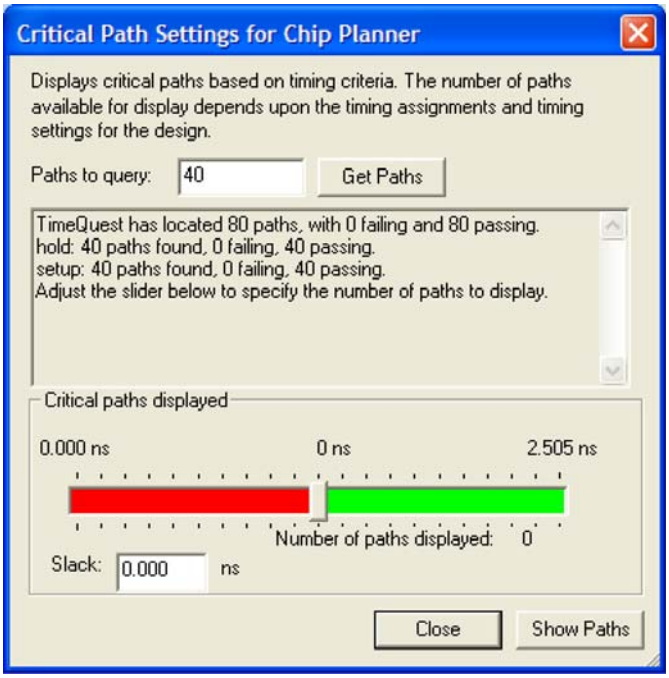


Viewing critical paths in the Chip Planner helps you analyze why a specific path is failing. You can see if any modification in the placement can potentially reduce the negative slack. You can display details of a path (to expand/collapse the path to/from the connections in the path) by clicking **Expand Connections/Paths** in the toolbar, or by clicking on the "+/-" on the label.

To view critical paths in the Chip Planner, on the View menu, click **Critical Path Settings**. In the **Critical Path Settings** dialog box, click **Show Path** (refer to Figure 12–25 on page 12–29).

If you are using the TimeQuest Timing Analyzer, you can locate the failing paths starting from the timing report. To locate the critical paths, run the Report Timing task from the Custom Reports group in the Tasks pane of the TimeQuest Timing Analyzer. From the View pane, which lists the failing paths, right-click on any failing path or node, and select **Locate Path**. From the Locate dialog box, select **Chip Planner** to see the failing path in the Chip Planner.

Figure 12–25. Critical Path Settings for the Chip Planner



When viewing critical paths, you can specify the clock in the design you want to view. You determine the paths to be displayed by specifying the slack threshold in the slack field of the **Critical Path Settings for Chip Planner** dialog box. This dialog box also helps you to filter specific paths based on the source and destination registers.

☞ Timing settings must be made and a timing analysis performed for paths to be displayed in the floorplan.

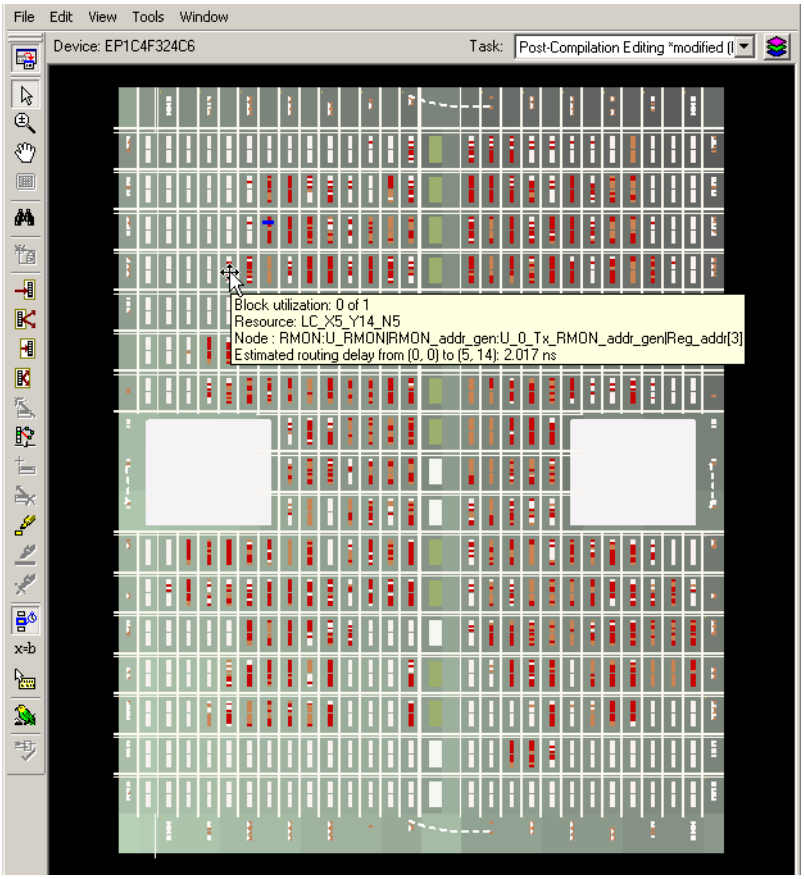
For more information about performing static timing analysis with the Quartus II Classic Timing Analyzer, refer to the *Quartus II Classic Timing Analyzer* chapter in volume 3 of the *Quartus II Handbook*. For more information about performing static timing analysis with the Quartus II TimeQuest Timing Analyzer, refer to the *Quartus II TimeQuest Timing Analyzer* chapter in volume 3 of the *Quartus II Handbook*.

Viewing Physical Timing Estimates

In the Chip Planner, you can select a resource and see the approximate delay to any other resource on the device. After you select a resource, the delay is represented by the color of potential destination resources. The lighter the color of the resource, the longer the delay.

To see the physical timing map of the device, in the Chip Planner, click the **Layers** icon located next to the Task menu. **Under Background Color Map**, select **Physical Timing Estimate**. Select a source and move your cursor to a destination resource. The Chip Planner displays the approximate routing delay between your selected source and destination register (Figure 12–26).

Figure 12–26. Chip Planner Displaying Routing Delay



You can use the physical timing estimate information when attempting to improve the Fitter results by manually moving logic in a device or when creating LogicLock regions to group logic together. This feature allows you to estimate the physical routing delay between different nodes so that you can place critical nodes and modules closer together, and move non-critical or unrelated nodes and modules further apart.

In addition to reducing delay between critical nodes, you can make placement assignments to reduce the routing congestion between critical and noncritical entities and modules. This allows the Fitter to meet the design timing requirements.

Moving logic and creating manual placements is an advanced technique to meet timing requirements and must be done after careful analysis of the design. Moving nodes in the **Floorplan Editing (Assignment)** task creates an assignment. However, if you move logic nodes in the **Post-Compilation Editing (ECO)** task, that change is considered an ECO change.

For more information about Floorplan Assignments, refer to "Viewing Assignments in the Chip Planner" on page 12–39.

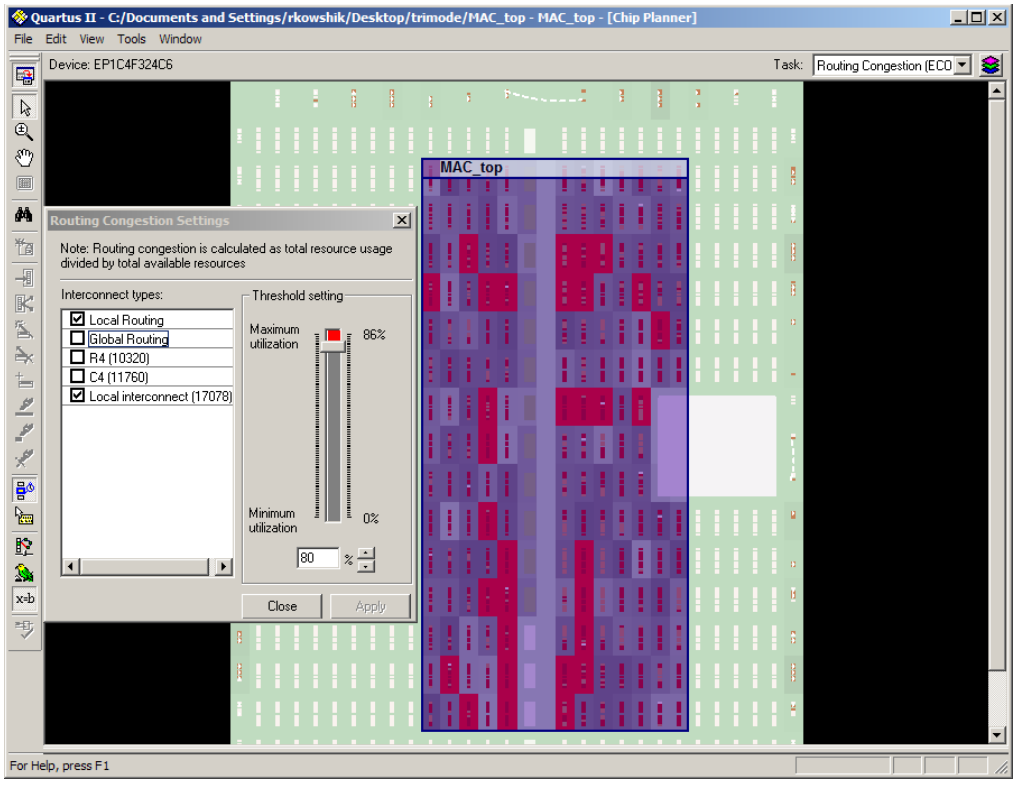
For more information about performing ECOs, refer to the *Engineering Change Management with the Chip Planner* chapter in volume 2 of the *Quartus II Handbook*.

Viewing Routing Congestion

The Routing Congestion view allows you to determine the percentage of routing resources used after a compilation. This feature identifies where there is a lack of routing resources. This information helps you make design changes that might ease routing congestion and thus meet design requirements. Congestion is represented visually by the color and shading of logic resources; darker shading represents a greater utilization of routing resources.

You can set a routing congestion threshold to identify areas of high routing congestion with the **Routing Congestion Settings** dialog box by selecting the **Routing Congestion (ECO)** task from the drop-down task list or by selecting **Routing Utilization** from the layers settings. In the **Routing Congestion Settings** dialog box, set the threshold level for congestion indication and click **Apply**. You can also select the interconnect type. All areas that exceed the specified threshold appear in red (Figure 12–27).

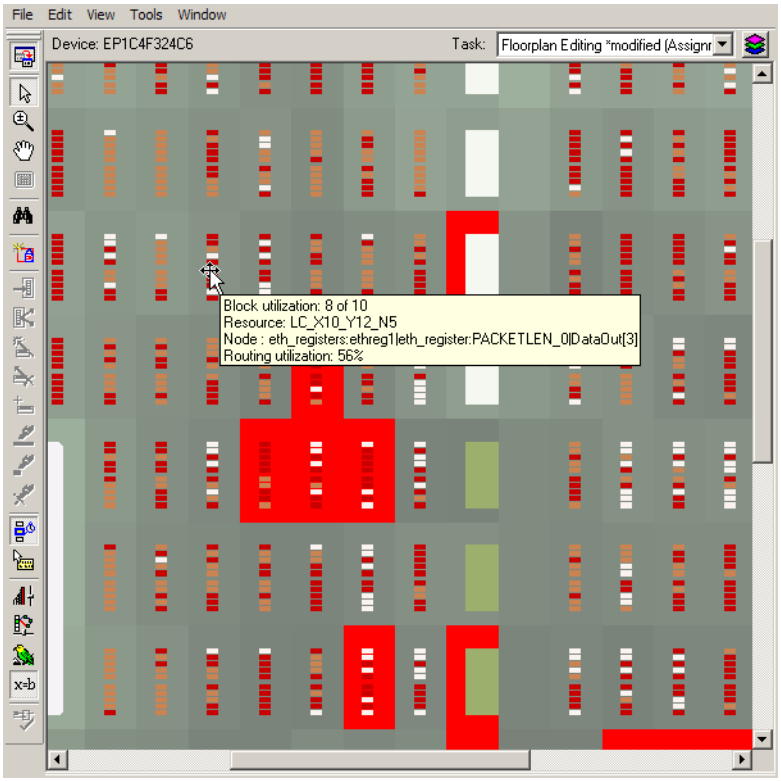
Figure 12–27. Areas Exceeding Threshold



If you are using a HardCopy II device, turn on **Routing Congestion** to see the routing congestion in the device by selecting **Routing Utilization** from the Layers Settings window.

To view the routing congestion in the Chip Planner, click the Layers icon located next to the Task menu. Under **Background Color Map**, select the **Routing Utilization** map (Figure 12–28). Any areas that exceed the threshold appear red. Use this congestion information to evaluate if you could modify the floorplan, or make changes to the RTL to reduce routing congestion.

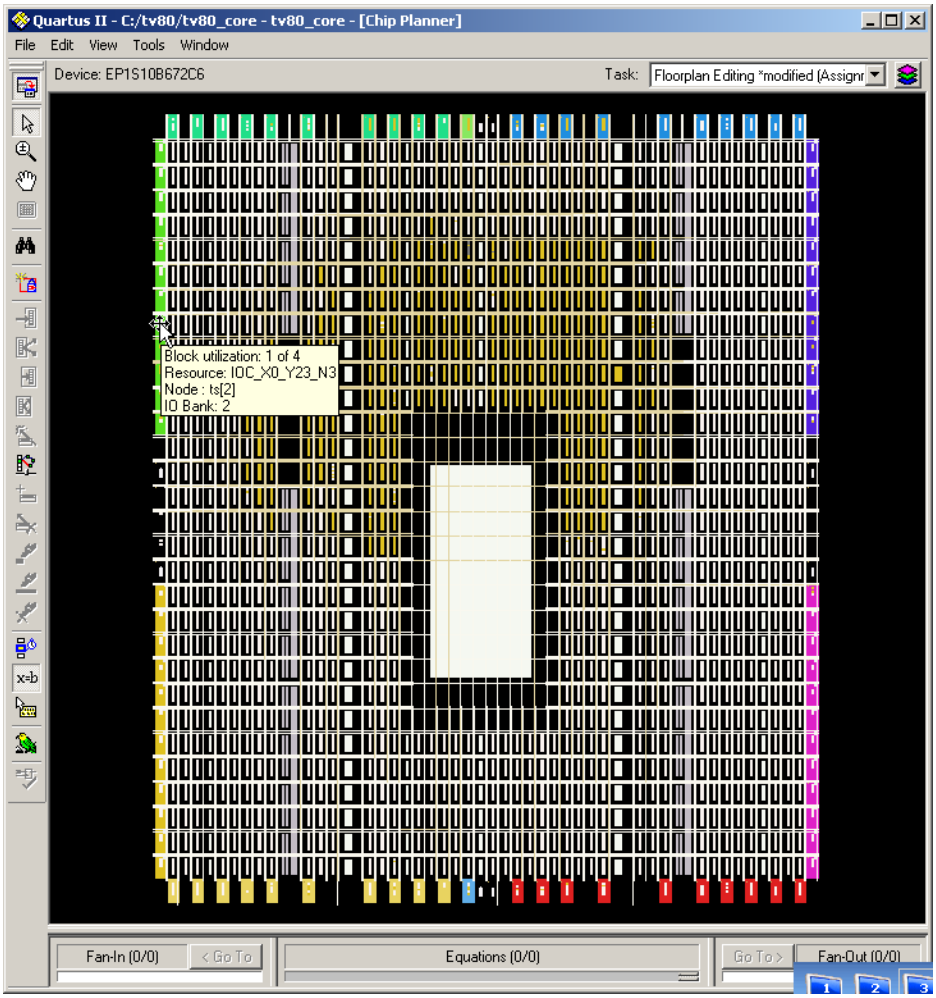
Figure 12–28. Viewing Routing Congestion Map in the Chip Planner



Viewing I/O Banks

The Chip Planner can show all of the I/O banks of the device. To see the I/O bank map of the device, click the Layers icon located next to the Task menu. Under **Background Color Map**, select **I/O Banks**. Refer to Figure 12–29.

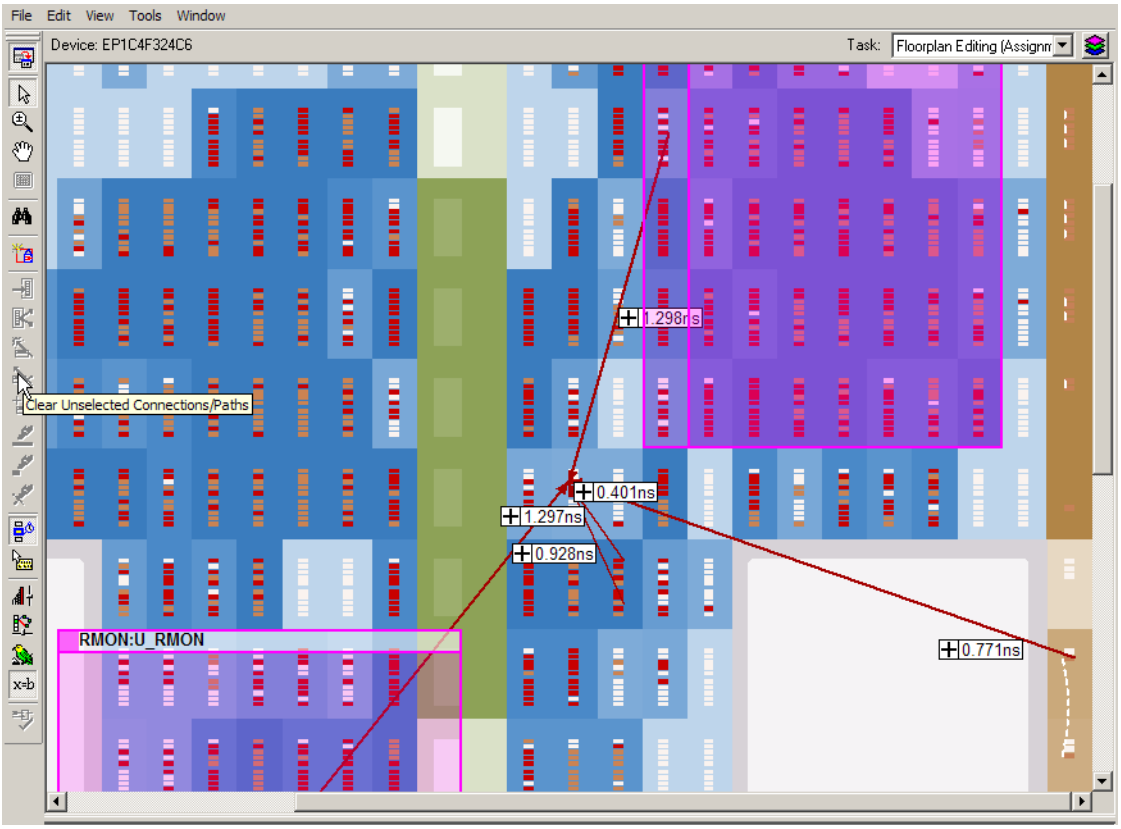
Figure 12–29. Viewing I/O Banks in the Chip Planner



Generating Fan-In and Fan-Out Connections

The ability to display fan-in and fan-out connections enables you to view the atoms that fan-in to or fan-out from the selected atom. To remove the connections displayed, use the Clear Unselected Connections/Paths icon in the Chip Planner toolbar. Figure 12–30 shows the fan-in connections for the selected resource.

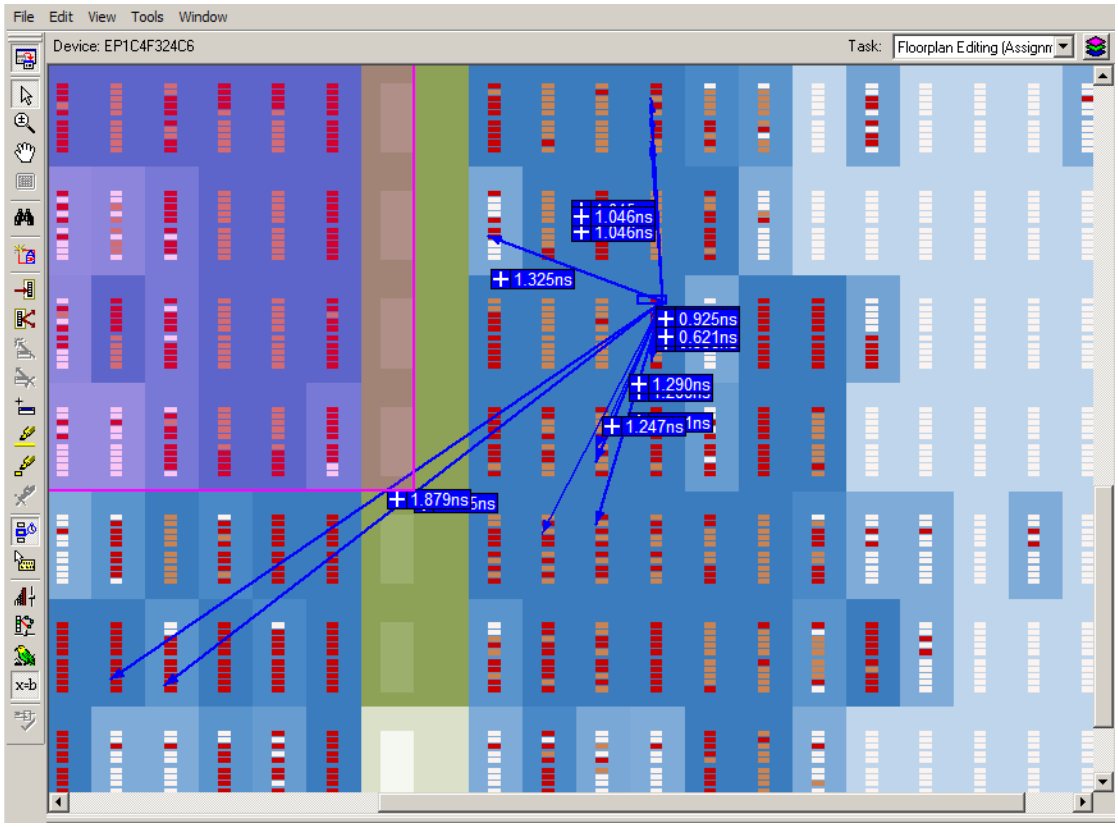
Figure 12–30. Generated Fan-In



Generating Immediate Fan-In and Fan-Out Connections

The ability to display immediate fan-in and fan-out connections enables you to view the immediate resource that is the fan-in or fan-out connection for the selected atom. For example, selecting a logic resource and choosing to view the immediate fan-in enables you to see the routing resource that drives the logic resource. You can generate immediate fan-in and fan-outs for all logic resources and routing resources. To remove the connections that are displayed, click the Clear Connections icon in the toolbar. Figure 12–31 shows the immediate fan-out connections for the selected resource.

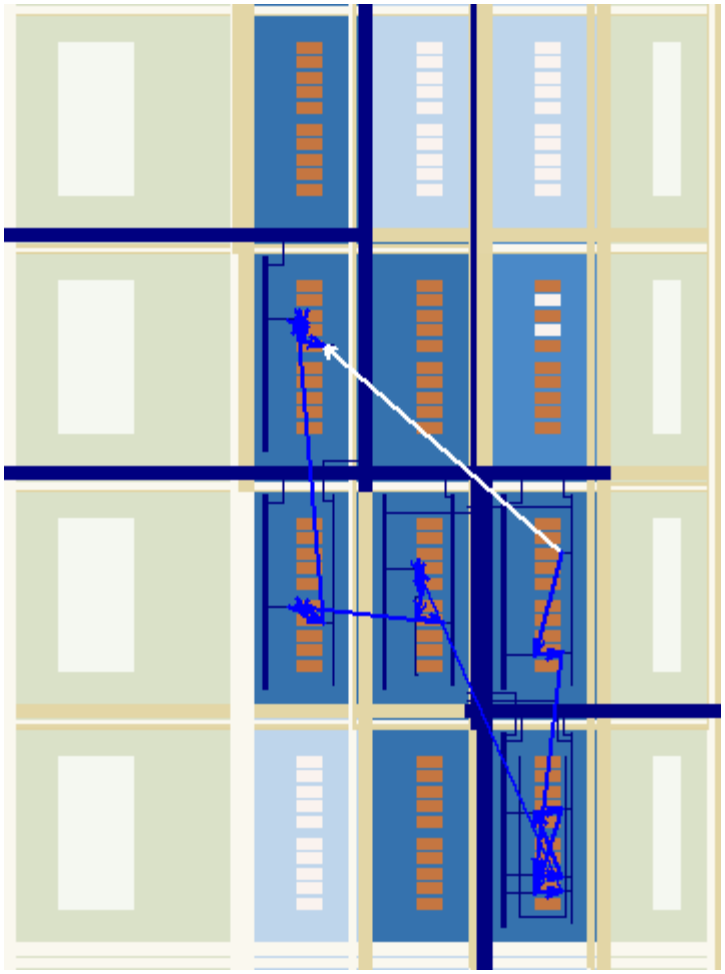
Figure 12–31. Immediate Fan-Out Connection



Highlight Routing

The **Highlight Routing** command enables you to highlight the routing resources used by a selected path or connection. Figure 12–32 shows the routing resources used between two logic elements.

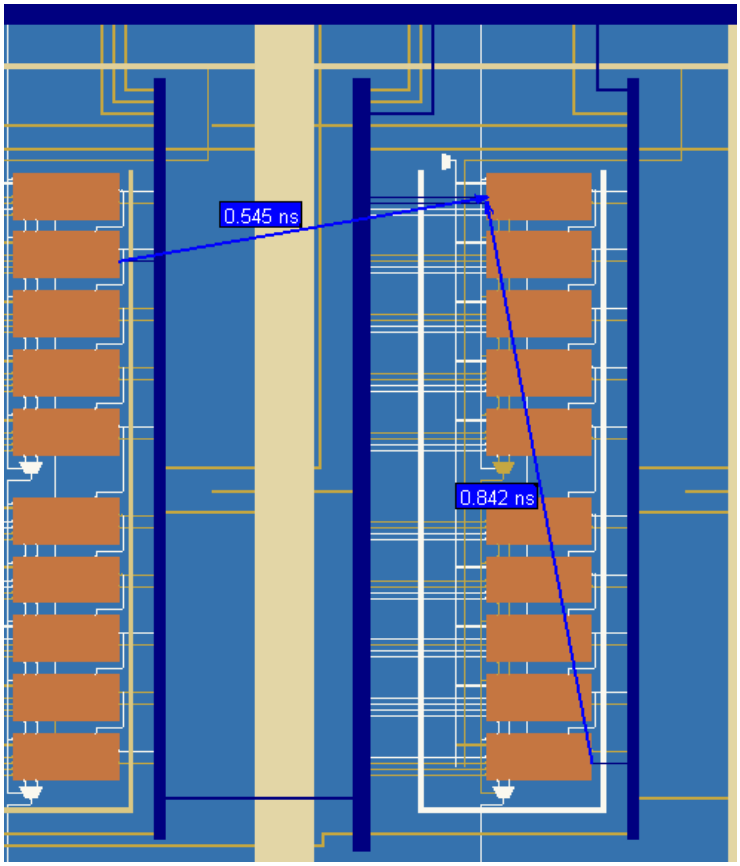
Figure 12–32. Highlight Routing



Show Delays

You can view the timing delays for the highlighted connections when generating connections between elements. For example, you can view the delay between two logic resources or between a logic resource and a routing resource. Figure 12–33 shows the delays between several logic elements.

Figure 12–33. Show Delays



Exploring Paths in the Chip Planner

You can use the Chip Planner to explore paths between logic elements. The following example uses the Chip Planner to traverse paths from the Timing Analysis report.

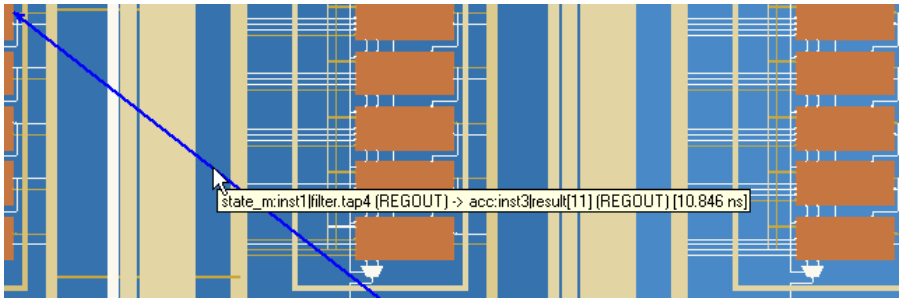
Locate Path from the Timing Analysis Report to the Chip Planner

To locate a path from the Timing Analysis report to the Chip Planner, perform the following steps:

1. Select the path you want to locate.
2. Right-click the path in the Timing Analysis report, point to **Locate**, and click **Locate in Chip Planner (Floorplan & Chip Editor)**.

Figure 12–34 shows the path that is displayed in the Chip Planner.

Figure 12–34. Resulting Path

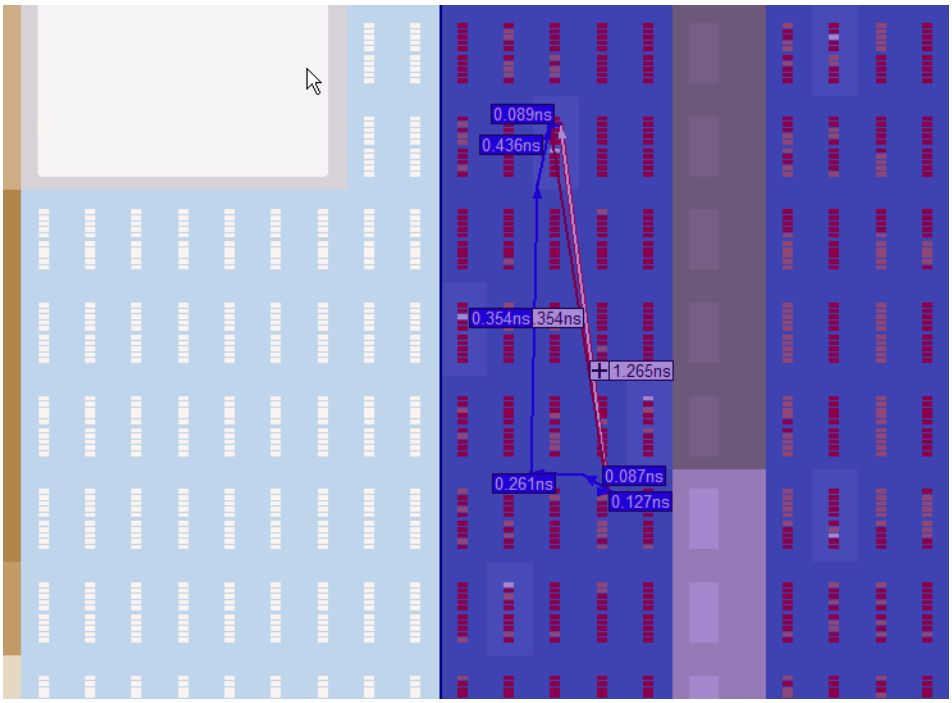


To view the routing resources taken for a path you have located in the Chip Planner, click the Highlight Routing icon in the Chip Planner toolbar, or from the View menu, click **Highlight Routing**.

Analyzing Connections for a Path

To determine the connections between items in the Chip Planner, click the Expand Connections/Paths icon on the toolbar. To add the timing delays between each connection, click the Show Delays icon on the toolbar. Figure 12–35 shows the connections for the selected path that are displayed in the Chip Planner. To see the constituent delays on the selected path, click on the "+" sign next to the path delay displayed in the Chip Planner.

Figure 12–35. Path Analysis



Viewing Assignments in the Chip Planner

You can view location assignments by selecting the appropriate layer set in the Chip Planner. To view location assignments in the Chip Planner, select the **Floorplan Editing (Assignment)** task or any custom task with Assignment editing mode. See Figure 12–36.

The Chip Planner shows location assignments graphically, by displaying assigned resources in a particular color (gray, by default). You can create or move an assignment by dragging the selected resource to a new location.

Figure 12–36. Viewing Assignments in the Chip Planner

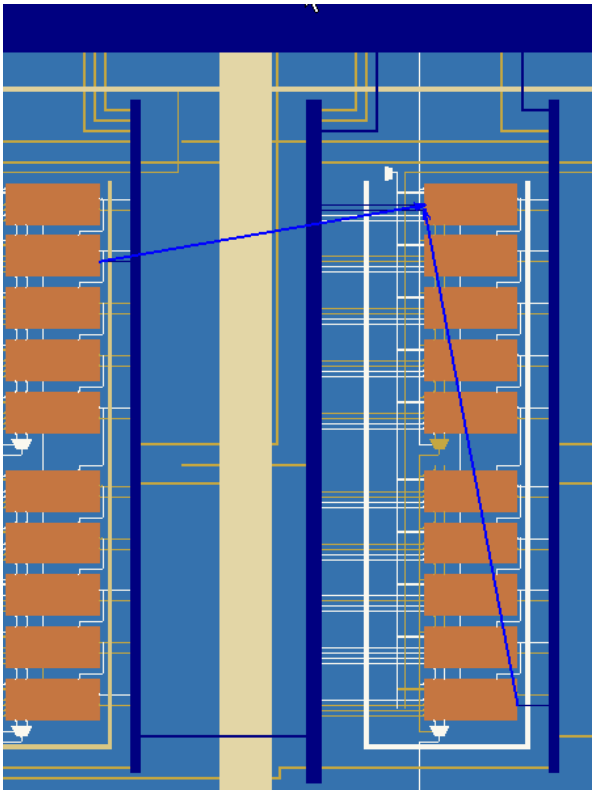
You can make node and pin location assignments and assignments to LogicLock regions and custom regions using the drag-and-drop method in the Chip Planner. The assignments that you create are applied by the Fitter during the next place-and-route operation.

To learn more about working with location assignments, refer to the Quartus II Help.

Viewing Routing Channels for a Path in the Chip Planner

To determine the routing channels between connections, click the Highlight Routing icon on the toolbar. Figure 12–37 shows the routing channels used for the selected path in the Chip Planner.

Figure 12–37. Highlight Routing

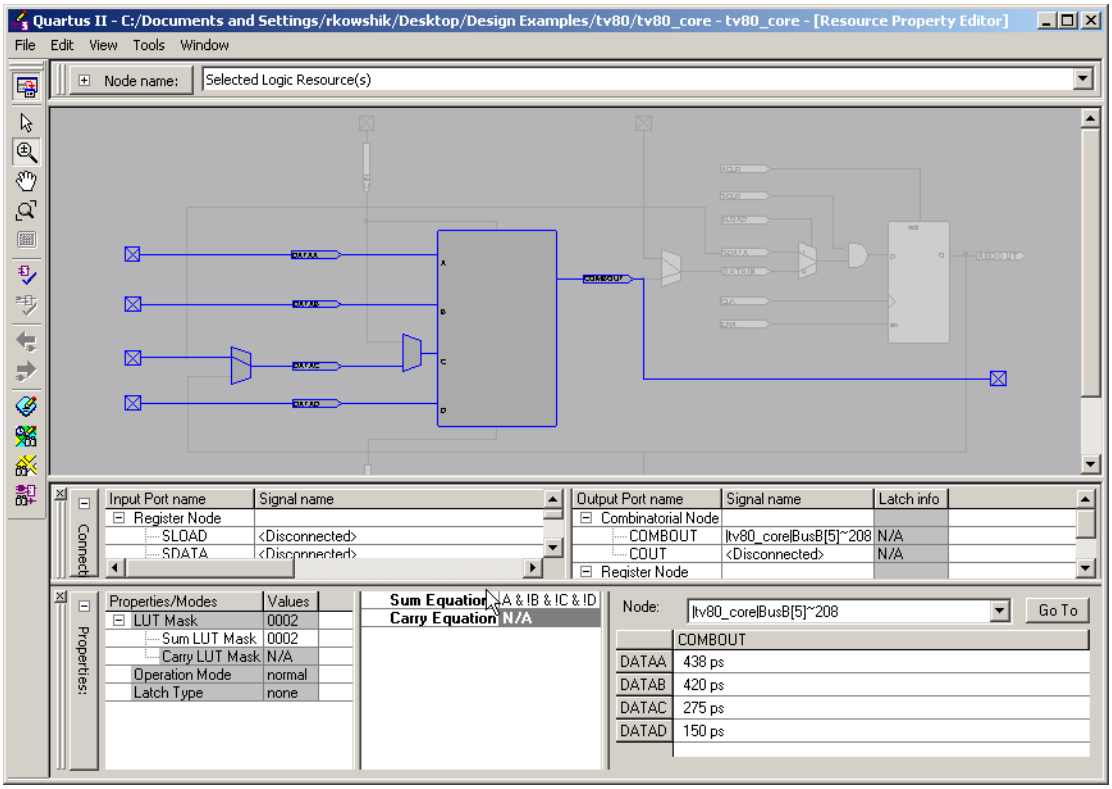


You can view and edit resources in the FPGA using the Resource Property Editor mode of the Chip Planner. For more information, refer to the *Engineering Change Management with the Chip Planner* chapter in volume 2 of the *Quartus II Handbook*.

Cell Delay Table

You can view the propagation delay from all inputs to all outputs for any LE in your design. To see the Cell Delay Table for an atom, select the atom in the Chip Planner and right-click. From the pop-up menu, click **Locate** and then click **Locate in Resource Property Editor**. The Resource Property window shows you the atom properties along with the Cell Delay Table, indicating the propagation delay from all inputs to all outputs. Figure 12–38 shows the Cell Delay Table.

Figure 12–38. Cell Delay Table



Timing numbers are displayed only when there is a direct path between the source input port and the destination output port. In cases where there is no path, or the path requires an intermediate buried timing node, the displayed cell delay is given as "N/A."

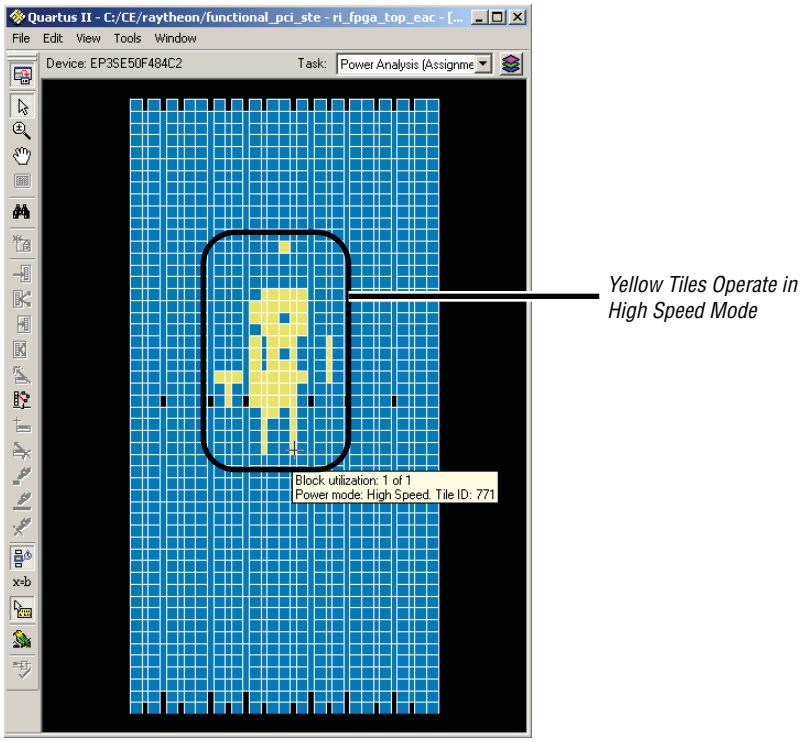
Viewing High-Speed and Low-Power Tiles in Stratix III Devices in the Chip Planner

The Chip Planner has a predefined task, **Power Analysis (Assignment)**, which shows the power map of a Stratix III device. Stratix III devices have ALMs that can operate in either high-speed mode or low-power mode. The power mode is set during the fitting process in the Quartus II software. These ALMs are grouped together to form larger blocks, called "tiles."

To learn more about power analyses and optimizations in Stratix III devices, refer to *AN 437: Power Optimization in Stratix III FPGAs*. To learn more about power analyses and optimizations in Stratix IV devices, refer to *AN 514: Power Optimization in Stratix IV FPGAs*.

When the **Power Analysis (Assignment)** task is selected in the Chip Planner for Stratix III devices, low-power and high-speed tiles are displayed in different colors; yellow tiles operate in a high-speed mode, while blue tiles operate in a low-power mode (see Figure 12–39). When you select the Power Analysis task, you can perform all floorplanner-related functions for this task, however you cannot edit tiles to change the power mode.

Figure 12–39. Viewing High-Speed and Low Power Tiles in a Stratix III Device



Design Analysis Using the Timing Closure Floorplan

For older device families not supported by the Chip Planner, you can perform floorplan analysis using the Timing Closure Floorplan. Table 12–1 on page 12–1 lists the device families supported by the Timing Closure Floorplan Editor and the Chip Planner.

The Timing Closure Floorplan Editor allows you to analyze your design visually before and after performing a full design compilation in the Quartus II software. This floorplan editor, used in conjunction with the Classic Timing Analyzer, provides a method for performing design analysis.

To start the Timing Closure Floorplan Editor, on the Assignments menu, click **Timing Closure Floorplan**.

If the device in your project is not supported by the Timing Closure Floorplan, the following message appears:

```
Can't display a floorplan: the current device family is only
supported by Chip Planner.
```

If your target device is supported by the , you can also start the Timing Closure Floorplan by right-clicking any of the following sources, pointing to **Locate**, and clicking **Locate in Timing Closure Floorplan**:

- Compilation Report
- Node Finder

- Project Navigator
- RTL source code
- RTL Viewer
- Simulation Report
- Timing Report

Figure 12–40 shows the icons in the Timing Closure Floorplan toolbar.

Figure 12–40. Timing Closure Floorplan Icons

Timing Closure Floorplan Views

The Timing Closure Floorplan Editor provides the following views of your design:

- Field view
- Interior Cells view
- Interior LAB view

The following two views open the Pin Planner:

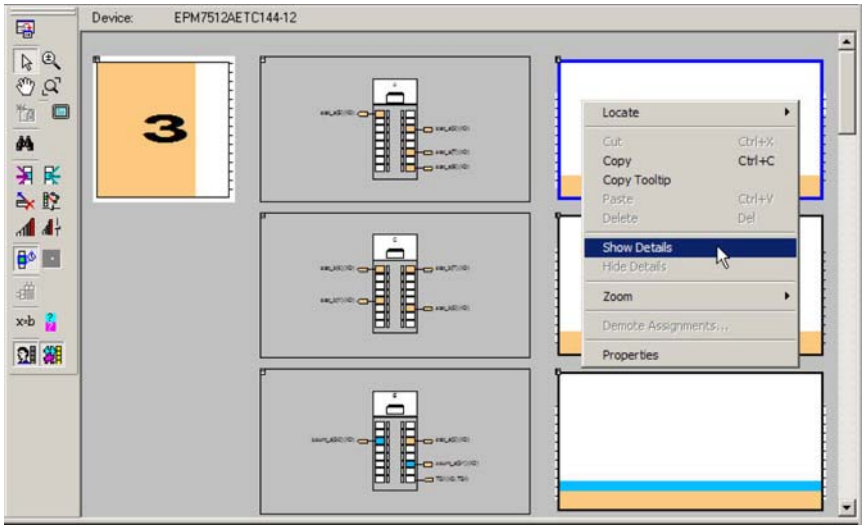
- Package Top view
- Package Bottom view

Field View

The Field view provides a color-coded, high-level view of the resources used in the device floorplan. All device resources, such as embedded system blocks (ESBs) and MegaLAB blocks, are outlined.

To view the details of a resource in the Field view, select the resource, right-click, and click **Show Details**. To hide the details, select all the resources, right-click, and click **Hide Details** (Figure 12–41).

Figure 12–41. Show and Hide Details of a Logic Array Block in Field View



Other Views

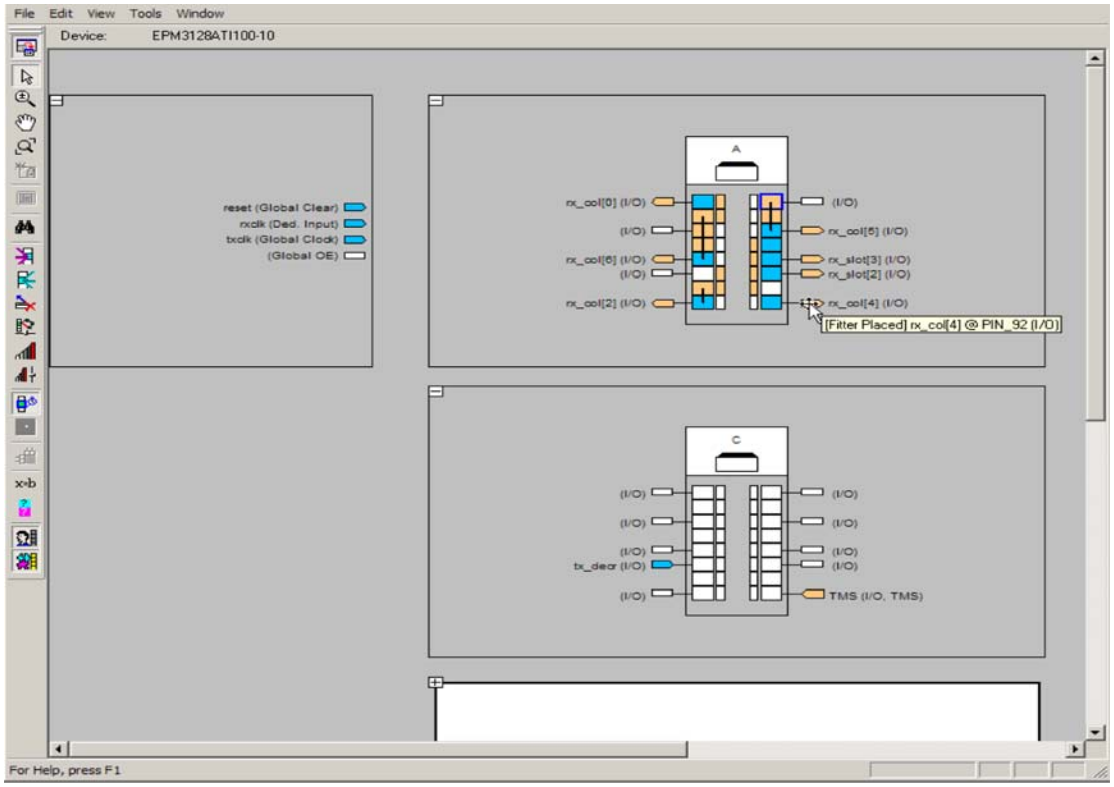
You can view your design in the Timing Closure Floorplan Editor with the Interior Cells, Interior LABs, Package Top, and Package Bottom views. Use the View menu to display the various floorplan views. The Interior Cells view provides a detailed view of device resources, including device pins and individual logic elements within a MegaLAB.

Viewing Assignments

The Timing Closure Floorplan Editor differentiates between user assignments and Fitter placements. If the device is changed after a compilation, the user assignment and Fitter placement options cannot be used together. When this situation occurs, the Fitter placement displays the last compilation result and the user assignment displays the floorplan of the newly selected device.

To see the user assignments, click the Show User Assignments icon in the Floorplan Editor toolbar, or, on the View menu, point to **Assignments** and click **Show User Assignments**. To see the Fitter placements, click the Show Fitter Placements icon in the Floorplan Editor toolbar, or, on the View menu, point to **Assignments** and click **Show Fitter Placements**. Figure 12–42 shows the Fitter placements.

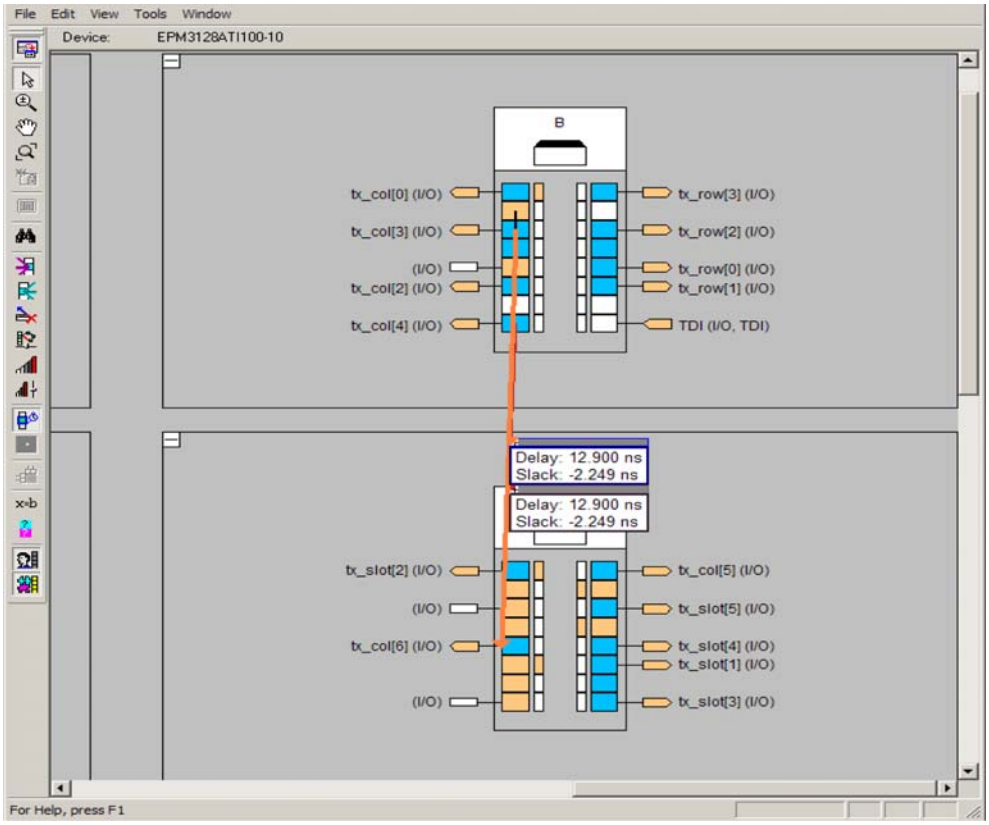
Figure 12–42. Fitter Placements



Viewing Critical Paths

The View Critical Paths feature displays routing paths in the floorplan, as shown in Figure 12–43. The criticality of a path is determined by its slack and is also shown in the Timing Analysis report.

Figure 12–43. Critical Paths



To view critical paths in the Timing Closure Floorplan, click the Critical Path Settings icon on the toolbar, or, on the View menu, point to **Routing** and click **Critical Path Settings**.

When viewing critical paths, you can specify the clock in the design to be viewed. You can determine which paths to display by specifying the slack threshold in the slack field.

You must make timing settings and perform timing analysis to view paths in the floorplan.

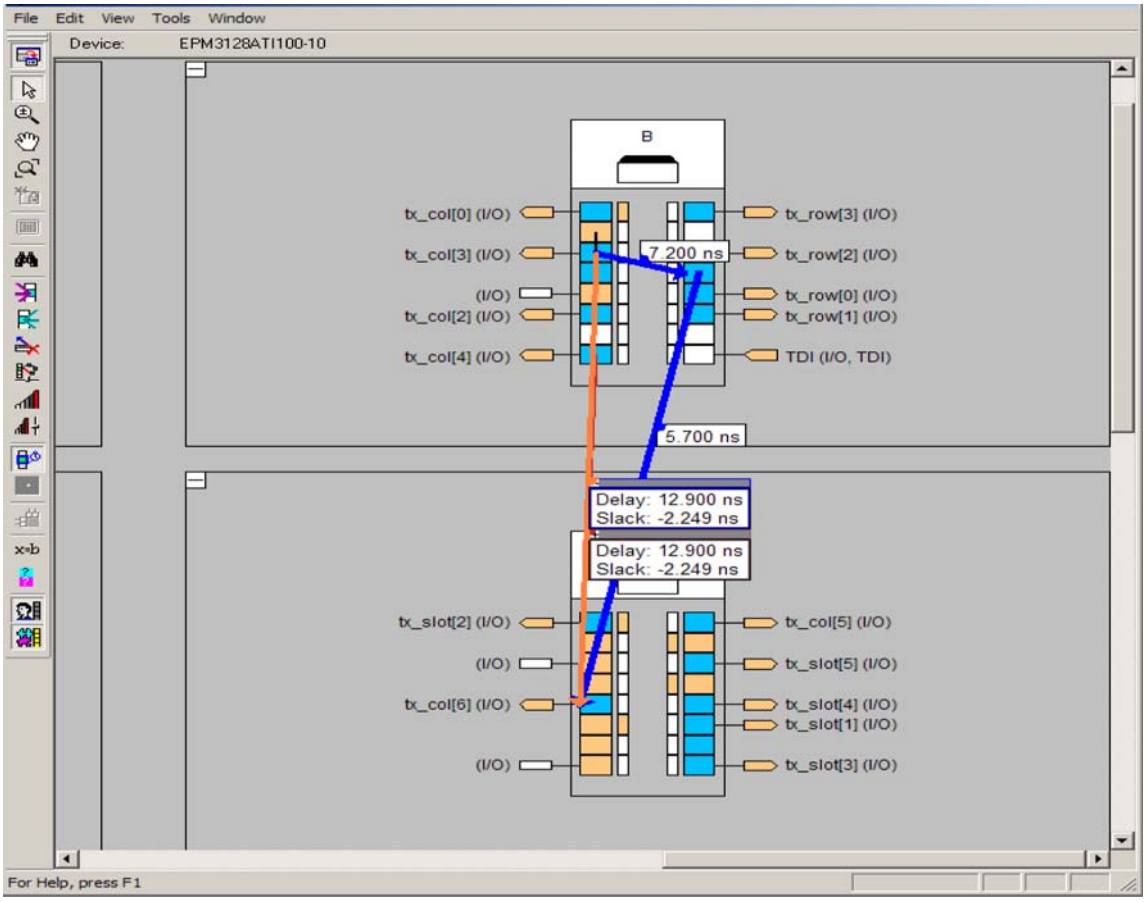
For more information about performing static timing analyses of your design with a timing analyzer, refer to the *Quartus II Classic Timing Analyzer* and the *Quartus II TimeQuest Timing Analyzer* chapters in volume 3 of the *Quartus II Handbook*.

You can view critical paths to determine the criticality of nodes based on placement. You can view the details of the critical path in a number of ways.

The default view in the Timing Closure Floorplan shows the path with the source and destination registers displayed. You can also view all the combinational nodes along the worst-case path between the source and destination nodes. To view the full path, click on the delay label to select the path, right-click, and select **Show Path Edges**. Figure 12–44 shows the critical path through combinational nodes. To hide the combinational nodes, select the path, right-click, and select **Hide Path Edges**.

You must view the routing delays to select a path.

Figure 12–44. Worst-Case Combinational Path Showing Path Edges



After running timing analysis, you can locate timing paths from the timing reports file produced. Right-click on any row in the report file, point to **Locate**, and click **Locate in Timing Closure Floorplan**. The Timing Closure Floorplan window opens with the timing path highlighted.

For more information about optimizing your design in the Quartus II software, refer to the *Area and Timing Optimization* chapter in volume 2 of the *Quartus II Handbook*. With the options and tools available in the Timing Closure Floorplan and the techniques described in that chapter, the Quartus II software can help you achieve timing closure in a more time-efficient manner.

Viewing Routing Congestion

The View Routing Congestion feature allows you to determine the percentage of routing resources used after a compilation. This feature identifies where there is a lack of routing resources.

The congestion is shown by the color and shading of logic resources. The darker shading represents a greater routing resource utilization. Logic resources that are red have routing resource utilization greater than the specified threshold.

The routing congestion view is only available from the View menu when you enable the Field view. To view routing congestion in the floorplan, click the Show Routing Congestion icon, or on the View menu, point to **Routing** and click **Show Routing Congestion**. To set the criteria for the critical path you want to view, click the Routing Congestion Settings icon, or on the View menu, point to **Routing** and click **Routing Congestion Settings**.

In the **Routing Congestion Settings** dialog box, you can choose the routing resource (interconnect type) you want to examine and set the congestion threshold. Routing congestion is calculated based on the total resource usage divided by the total available resources.

If you use the routing congestion viewer to determine where there is a lack of routing resources, examine each routing resource individually to determine which ones use close to 100% of the available resources (Figure 12–45). Use this congestion information to evaluate whether you should modify the floorplan, or make changes to the RTL to reduce routing congestion.

Figure 12–45. Routing Congestion of a Sample Design in a MAX3000A series Device

Scripting Support

You can run procedures and create the settings described in this chapter in a Tcl script. You can also run some procedures at a command prompt. For detailed information about scripting command options, refer to the Quartus II command-line and Tcl API Help browser. To run the Help browser, type the following command at the command prompt:

```
quartus_sh --qhelp ↵
```

The same information is available in the Quartus II Help, and in the *Quartus II Scripting Reference Manual*.

For more information about Tcl scripting, refer to the *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*. For more information about command-line scripting, refer to the *Command-Line Scripting* chapter in volume 2 of the *Quartus II Handbook*.

For information about all settings and constraints in the Quartus II software, refer to the *Quartus II Settings File Reference Manual*.

Initializing and Uninitializing a LogicLock Region

You must initialize the LogicLock data structures before creating or modifying any LogicLock regions and before executing any of the Tcl commands listed below.

Use the following Tcl command to initialize the LogicLock data structures:

```
initialize_logiclock
```

Use the following Tcl command to uninitialize the LogicLock data structures before closing your project:

```
uninitialize_logiclock
```

Creating or Modifying LogicLock Regions

Use the following Tcl command to create or modify a LogicLock region:

```
set_logiclock -auto_size true -floating true -region \ <my_region-name>
```

In the above example, the size of the region is set to auto and the state is set to floating.

If you specify a region name that does not exist in the design, the command creates the region with the specified properties. If you specify the name of an existing region, the command changes all properties you specify and leaves unspecified properties unchanged.

For more information about creating LogicLock regions, refer to the sections "Creating LogicLock Regions" on page 12–7 and "Creating LogicLock Regions with the Chip Planner" on page 12–9.

Obtaining LogicLock Region Properties

Use the following Tcl command to obtain LogicLock region properties. This example returns the height of the region named `my_region`:

```
get_logiclock -region my_region -height
```

Assigning LogicLock Region Content

Use the following Tcl commands to assign or change nodes and entities in a LogicLock region. This example assigns all nodes with names matching `fifo*` to the region named `my_region`.

```
set_logiclock_contents -region my_region -to fifo*
```

You can also make path-based assignments with the following Tcl command:

```
set_logiclock_contents -region my_region -from fifo -to ram*
```

For more information about assigning LogicLock Region Content, refer to "Assigning LogicLock Region Content" on page 12–9.

Save a Node-Level Netlist for the Entire Design into a Persistent Source File

Make the following assignments to cause the Quartus II Fitter to save a node-level netlist for the entire design into a **.vqm** file:

```
set_global_assignment-name LOGICLOCK_INCREMENTAL_COMPILE_ASSIGNMENT ON
set_global_assignment-name LOGICLOCK_INCREMENTAL_COMPILE_FILE <file name>
```

Any path specified in the file name is relative to the project directory. For example, specifying **atom_netlists/top.vqm** places **top.vqm** in the **atom_netlists** subdirectory of your project directory.

A **.vqm** file is saved in the directory specified at the completion of a full compilation.

The saving of a node-level netlist to a persistent source file is not supported for designs targeting newer devices such as the Stratix IV, Stratix III, Cyclone III, Arria II GX, or Arria GX.

Setting LogicLock Assignment Priority

Use the following Tcl code to set the priority for a LogicLock region's members. This example reverses the priorities of the LogicLock region in your design.

```
set reverse [list]
for each member [get_logiclock_member_priority] {
   set reverse [insert $reverse 0 $member]
{
set_logiclock_member_priority $reverse
```

Assigning Virtual Pins

Use the following Tcl command to turn on the virtual pin setting for a pin called `my_pin`:

```
set_instance_assignment -name VIRTUAL_PIN ON -to my_pin
```

For more information about assigning virtual pins, refer to "Virtual Pins" on page 12–19.

For more information about Tcl scripting, refer to the *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*.

Conclusion

Design floorplan analysis is a valuable method for achieving timing closure and timing closure optimal performance in highly complex designs. With their analysis capability, the Quartus II Chip Planner and the Timing Closure Floorplan help you close timing quickly on your designs. Using these tools together with LogicLock and Incremental Compilation enables you to compile your designs hierarchically, preserving the timing results from individual compilation runs. You can use LogicLock regions as part of an incremental compilation methodology to improve your productivity. You can also include a module in one or more projects while maintaining performance and reducing development costs and time-to-market. LogicLock region assignments give you complete control over logic and memory placement to improve the performance of non-hierarchical designs as well.

Referenced Documents

This chapter references the following documents:

- *AN 437: Power Optimization in Stratix III FPGAs*
- *Area and Timing Optimization* chapter in volume 2 of the *Quartus II Handbook*
- *Best Practices for Incremental Compilation Partition and Floorplan Assignments* chapters in volume 1 of the *Quartus II Handbook*
- *Command-Line Scripting* chapter in volume 2 of the *Quartus II Handbook*
- *Engineering Change Management with the Chip Planner* chapter in volume 2 of the *Quartus II Handbook*
- *I/O Management* chapter in volume 2 of the *Quartus II Handbook*
- *Quartus II Classic Timing Analyzer* chapter in volume 3 of the *Quartus II Handbook*
- *Quartus II Incremental Compilation for Hierarchical and Team-Based Design* chapter in volume 1 of the *Quartus II Handbook*
- *Quartus II Scripting Reference Manual*
- *Quartus II Settings File Manual*
- *The Quartus II TimeQuest Timing Analyzer* chapter in volume 3 of the *Quartus II Handbook*
- *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*

Document Revision History

Table 12–3 shows the revision history for this chapter.

Table 12–3. Document Revision History (Part 1 of 2)

Date and Document Version	Changes Made	Summary of Changes
November 2009 v9.1.0	■ Updated supported device information throughout ■ Removed deprecated sections related to the Timing Closure Floorplan for older device families. (For information on using the Timing Closure Floorplan with older device families, refer to previous versions of the *Quartus II Handbook*, available in the Quartus II Handbook Archive.) ■ Updated "Creating Non-Rectangular LogicLock Regions" section ■ Added "Selected Elements Window" section ■ Updated table 12-1	Updated for the Quartus II 9.1 software release.
March 2009 v9.0.0	■ Was chapter 10 in the 8.1.0 release.	Updated for the Quartus II 9.0 software release.

Table 12–3. Document Revision History (Part 2 of 2)

Date and Document Version	Changes Made	Summary of Changes
November 2008 v8.1.0	■ Changed page size to 8½" × 11" ■ Removed "Importing LogicLock Regions", "Exporting LogicLock Regions", Importing Back-Annotated Routing in LogicLock Regions", LogicLock Regions Versus Soft LogicLock Regions", and "Exporting Back-Annotated Routing in LogicLock Regions", and removed subsections in "Using LogicLock Methodology for Older Device Families" ■ Updated "Viewing Routing Congestion" on page 12–29 ■ Updated Table 12–2	Updated for the Quartus II 8.1 software release.
May 2008 v8.0.0	■ Updated the following sections: → "Chip Planner Tasks and Layers" → "LogicLock Regions" → "Back-Annotating LogicLock Regions" → "LogicLock Regions in the Timing Closure Floorplan" ■ Added the following sections: → "Reserve LogicLock Region" → "Creating Non-Retangular LogicLock Regions" → "Viewing Available Clock Networks in the Device" ■ Updated Table 10–1 ■ Removed the following sections: → Reserve LogicLock Region Design Analysis Using the Timing Closure Floorplan	Updated for the Quartus II 8.0 software release.

For previous versions of the *Quartus II Handbook*, refer to the Quartus II Handbook Archive.