Class D voltage-switching MOSFET power amplifier

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Abstract: An analysis of a class D voltage-switching tuned power amplifier is given, along with experimental results. Analytical equations are derived for performance parameters at any operating frequency normalised with respect to the resonant frequency and at any load resistance normalised with respect to the characteristic impedance of the resonant circuit. The analysis is carried out under the high loaded quality factor assumption, using Fourier series techniques. The behaviour of power MOSFETs in class D circuits for both capacitive and inductive loads is discussed in detail. It is shown that the operation above the resonant frequency (an inductive load) is preferred. The theoretical results were in good agreement with measured circuit performance parameters. The equations provide easy-to-use design tools, which can find a broad application, e.g. in designing DC/DC resonant converters and DC/AC inverters.

1 Introduction

Class D resonant amplifiers (also called inverters) [1–6] have long been among the most practical high-frequency switching-mode amplifiers. They can be classified into two groups: class D voltage-switching amplifiers and class D current-switching amplifiers. One of the main advantages of class D voltage-switching amplifiers is low voltage across the transistors that is equal to the supply voltage. This makes them suitable for high-voltage applications, in which, e.g. a 220 V or 277 V rectified line voltage is used to supply the amplifier. In addition, low voltage MOSFETs can be used. Such MOSFETs have low on-resistances, reducing conduction losses, operating junction temperature, and yielding high efficiency. The MOSFET's on-resistance r_{DS} increases considerably with increasing junction temperature. This causes the conduction loss $r_{DS} I_{rms}^2$ to increase, where I_{rms} is the RMS value of the drain current. Typically, r_{DS} doubles as the temperatures rises by 100°C (e.g. from 25°C to 125°C), doubling the conduction loss. The MOSFETs on-resistance r_{DS} increases with temperature T because the mobility of electrons $\mu_n \simeq K_1/T^{2.5}$ and the mobility of holes $\mu_p \simeq K_2/T^{2.7}$ decrease with T over a temperature range of 100–400 K, where K_1 and K_2 are constants. The Class D amplifiers can be used in various applications such as high-frequency electronic ballasts for fluorescent lamps, DC/AC inverters used in welding equipment, and offline DC/DC resonant convertors. In many applications, the output power or the output voltage should be controlled. This can be accomplished by varying the operating frequency f (FM control).

The purpose of this paper is to derive analytical equations describing the operation of the class D voltage-switching amplifier at any operating frequency normalised with respect to the resonant frequency, and for any normalised load resistance normalised to the characteristic impedance of the resonant circuit. There is a strong need of such material to provide easy-to-use design tools.

2 Circuit description

A circuit of the class D voltage-switching resonant amplifier is shown in Fig. 1. It consists of two bidirectional switches S_1 and S_2 and a series-resonant circuit L–C–R_L. Each switch is composed of a transistor and an antiparallel diode and can conduct either positive or negative current. However, it can only take on a voltage higher than about -1 V. The MOSFETs intrinsic body-drain pn junction diode may be used as an antiparallel diode in the case of inductive load. A positive or negative switch current can flow through the transistor if the transitor is on. If the transistor is off, the switch can conduct only a negative current which flows through the diode. The transistors are driven by nonoverlapping rectangular-wave voltages v_1 and v_2 with a dead time at the operating frequency $f = 1/T$. Switches S_1 and S_2 are alternately on and off with a duty ratio of 50%. Resistance R_G represents the gate resistance and the output resistance of the drive source. Resistance R_L is an AC load to which the AC power is to be delivered.

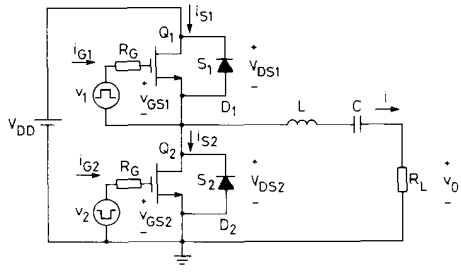

Fig. 1 *Class D voltage-switching amplifier (inverter) with a series-resonant circuit*

Equivalent circuits of the class D amplifier are shown in Fig. 2. In Fig. 2*a*, the MOSFETs are modelled by switches whose on-resistances are r_{DS1} and r_{DS2}. Resistance r_L is the equivalent series resistance (ESR) of the physical inductor L and resistance r_C is the equivalent series resistance of the physical capacitor C. In Fig. 2*b*,

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$r_S = (r_{DS1} + r_{DS2})/2 \simeq r_{DS}$ represents the average equivalent on-resistance of the MOSFETs. In Fig. 2*c*, the total parasitic resistance is represented by

$$r = r_S + r_L + r_C \simeq r_{DS} + r_L + r_C \quad (1)$$

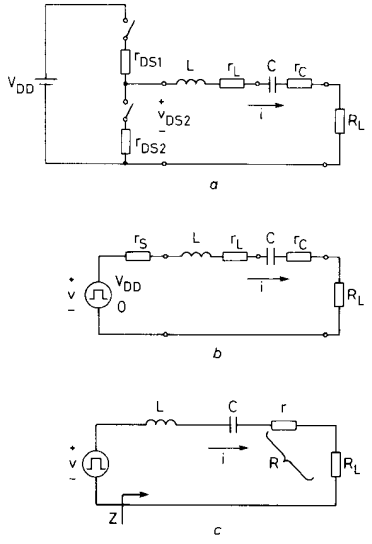

Fig. 2 *Successive simplifications of equivalent circuits of class D amplifier*

a Equivalent circuit containing various parasitic resistances
b Equivalent circuit with square wave voltage source
c Equivalent circuit in which R_L represents load resistance and r represents total parasitic resistance

yielding the overall resistance

$$R = R_L + r \simeq R_L + r_{DS} + r_L + r_C \quad (2)$$

As the DC input source V_I and switches S_1 and S_2 form a nearly ideal AC voltage source, many resonant circuits can be connected in parallel.

3 Principle of operation

The principle of operation of the class D amplifier is explained by the waveforms, sketched in Fig. 3. The voltage at the input of the series-resonant circuit is a square wave of magnitude V_{DD}. If the loaded quality factor Q_L of the resonant circuit is high (e.g. $Q_L \geqslant 2.5$), the current i through this circuit is nearly a sine wave. In many applications, the operating frequency f is not equal to the resonant frequency $f_r = 1/(2\pi\sqrt{(LC)})$ because the output power or the output voltage is often controlled by varying the operating frequency f (FM control). Fig. 3*a*, *b* and *c* shows the waveforms for $f < f_r$, $f = f_r$, and $f > f_r$, respectively. The current i flows through switch S_1 when S_1 is on and through S_2, when S_2 is on. The tolerance of the gate drive voltage is indicated by the shaded areas. Each transistor should be turned off for $f < f_r$ and turned on for $f > f_r$ during the time interval when the switch current is negative. During this time interval, the switch current can flow through the antiparallel diode. To prevent crossconduction (shoot-through current), the waveforms of the drive voltages v_1 and v_2 should be non-overlapping and have a sufficient dead time (not shown in Fig. 3). At turnoff, MOSFETs have a delay time and BJTs have a storage time. If the dead time is too short, one transistor still remains on while the other turns on. Consequently, both transistors are on at the same time and the power supply V_{DD} is shortcircuited by small tran-

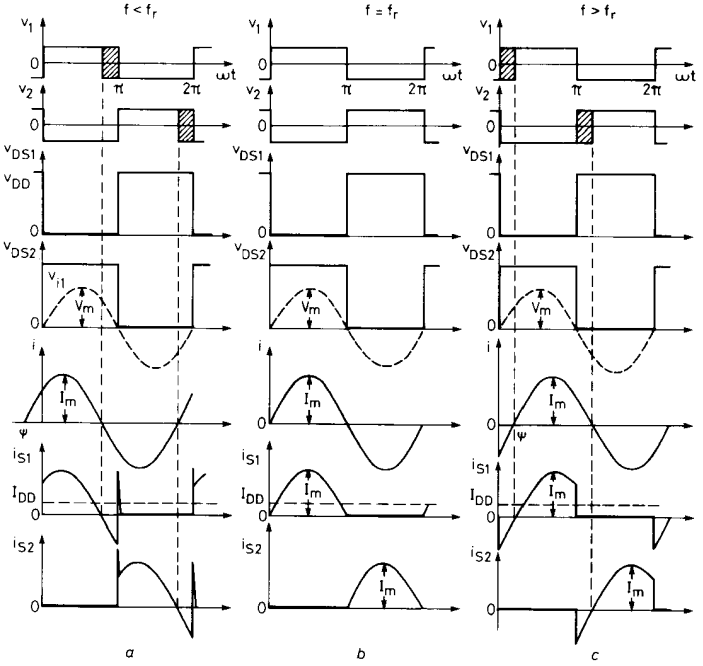

Fig. 3 *Waveforms in class D amplifier*
a $f < f_r$ *b* $f = f_r$ *c* $f > f_r$

sistor on-resistances r_{DS1} and r_{DS2}. For this reason, cross-conduction current pulses of magnitude $I_{pk} = V_{DD}/(r_{DS1} + r_{DS2})$ flow through the transistors. For example, if $V_{DD} = 200$ V and $r_{DS1} = r_{DS2} = 0.5\ \Omega$, $I_{pk} = 200$ A. The excessive current stress may cause immediate failure of the devices. The dead time should not be too long, either, as discussed in Sections 3.1 and 3.2. The maximum dead time increases as f/f_r increases or decreases because the time interval during which the switch current is negative becomes longer. The shortest dead time must be at f_r. There are available commercial IC drivers with an adjustable dead time, e.g. UC 2525 (Unitrode).

3.1 Operation below resonance

For $f < f_r$, the series-resonant circuit represents a capacitive load and the current through the resonant circuit i leads the fundamental component v_{i1} of the voltage v_{DS2} by the phase angle $|\psi|$, where $\psi < 0$. Therefore, the switch current is positive after switch turnon and is negative before switch turnoff. Consider the turnon of switch S_2. Prior to this transition, the current i flows through antiparallel diode D_1 of switch S_1. When transistor Q_2 is turned on by the drive voltage v_2, v_{DS2} is decreased, causing v_{DS1} to increase. Therefore, diode D_1 turns off and the current i is diverted from D_1 to Q_2. There are three detrimental effects at turnon:

(*a*) the reverse recovery of the antiparallel diode
(*b*) discharging of the transistor output capacitance
(*c*) Miller's effect

The most severe drawback of operation below resonance is the diode reverse-recovery stress. The MOSFETs intrinsic diode is a minority carrier device. Diode D_1 turns off at a very large dv/dt and therefore at a very large di/dt, generating a high reverse-recovery current spike (turned upside down). This spike flows through the other transistor because it cannot flow through the resonant circuit. The resonant inductor L does not allow for abrupt current changes. Consequently, the spikes occur in the switch current waveform at both the turnon and turnoff transitions. The magnitude of these spikes can be much (e.g. 10 times) higher than the magnitude of the steady-state switch current. High current spikes may destroy the transistors and always cause a considerable increase in switching losses and noise. Therefore, operation at $f < f_r$ should be avoided. During a part of the reverse-recovery interval, the diode voltage increases from -1 V to V_{DD} and both the diode current and voltage are simultaneously high, causing a high reverse-recovery power loss.

The current spikes can be reduced, e.g. by adding Schottky antiparallel diodes if V_{DD} is low. Schottky diodes have low breakdown voltages, typically below 100 V. Because the forward voltage of the Schottky diode is lower than that of the *pn* junction body diode, most if not all of the negative switch current flows through the Schottky diode, reducing the reverse-recovery current of the *pn* junction body diode. Another solution is to add a diode in series with the MOSFET and an ulstrafast diode in parallel with the series combination of the MOSFET and diode. This arrangement does not allow the intrinsic diode to conduct and thereby to store the excess minority charge. However, the higher parts count, additional cost, and the voltage drop across the series diode that reduces the efficiency are undesirable. Also, the peak voltages of the transistor and the series diode may become much higher than V_{DD}. Consequently, transistors with a higher permissible voltage and therefore a higher on-resistance should be used, increasing conduction loss. This method may reduce, but cannot eliminate the spikes. Snubbers can also be used to slow down the switching process.

The transistors are turned on at a high voltage, equal to V_{DD}. When the transistor is turned on, its output capacitance is discharged, causing a switching loss. Assuming that the transistor output capacitance C_{out} is linear, the energy stored in this capacitance before turnon is $W = (1/2)C_{out}V_{DD}^2$. This energy is lost as heat when the transistor turns on, resulting in a turnon switching loss in each transistor given by: $P_{turnon} = (1/2)fC_{out}V_{DD}^2$. In reality, the drain source *pn* step junction capacitance is nonlinear. Data sheets usually specify $C_{oss} = C_{gd} + C_{ds}$ and $C_{rss} = C_{gd}$ at $V_{DS} = 25\ \Omega$ and $V_{GS} = 0$ V. Hence, the drain-source capacitance at $V_{DS} = 25$ V is $C_{25} = C_{oss} - C_{rss}$. At $v_{DS} = V_{DD}$, $C_{ds}(V_{DD}) = 5C_{25}/\sqrt{(V_{DD})}$, the charge stored in C_{ds} is $Q_j(V_{DD}) = 10C_{25}\sqrt{(V_{DD})}$, the energy stored in C_{ds} is $W(V_{DD}) = (10/3)C_{25}\sqrt{(V_{DD}^3)}$, and the turnon switching loss is $P_{turnon} = (10/3)fC_{25}\sqrt{(V_{DD}^3)}$.

Because the gate source voltage increases and the drain source voltage decreases at the same time, Miller's effect is significant, increasing the transistor input capacitance and the gate drive requirements, and reducing the turnon switching speed.

An advantage of operation below resonance is that the transistors are turned off at nearly zero voltage, reducing the turnoff switching loss. For example, the drain source voltage v_{DS1} is held at about -1 V by the antiparallel diode D_1 when i_{S1} is negative. During this time interval, transistor Q_1 is turned off by drive voltage v_1. As v_{DS1} is constant, Miller's effect is absent during turnoff, the transistor input capacitance is not increased by Miller's effect, the gate drive requirement is reduced, and the turnoff switching speed is enhanced. Note that only the turnon transition of each switch is forced and directly controllable by the driver, while the turnoff transition is caused by the turnon of the opposite transistor (i.e. it is automatic).

The dead time should not be too long. If transistor Q_1 is turned off too early when the switch current i_{S1} is still positive, diode D_1 cannot conduct and diode D_2 turns on, decreasing v_{DS2} to -0.7 V and increasing v_{DS1} to V_{DD}. When the current through D_2 reaches zero, diode D_1 turns on, v_{DS1} decreases to -0.7 V, and v_{DS2} increases to V_{DD}. These two additional transitions of each of the switch voltages would result in switching losses.

In low-frequency high-power applications, thyristors can be used as switches. Below resonance, thyristors are turned off naturally when the switch current crosses zero.

3.2 Operation above resonance

For $f > f_r$, the series-resonant circuit represents an inductive load and the current i lags behind the voltage v_{i1} by the phase angle ψ, where $\psi > 0$. Hence, the switch current is negative after turnon (for part of switch on interval) and positive before turnoff. Consider the turnoff of switch S_1. When transistor Q_1 is turned off by the drive voltage v_1, v_{DS1} increases, causing v_{DS2} to decrease. As v_{DS2} reaches -0.7 V, D_2 turns on and the current i is diverted from transistor Q_1 to diode D_2. Thus, the turnoff switch transition is forced by the driver, whereas the turnon transition is caused by the turnoff transition of the opposite transistor, not by the driver. Only the turnoff transition is directly controllable.

The transistors are turned on at zero voltage. For example, transistor Q_2 is turned on by v_2 when i_{S2} is negative and voltage v_{DS2} is maintained at about -1 V by the antiparallel diode D_2 during the transistor turnon transition. Therefore, the turnon switching loss is

reduced, Miller's effect absent, transistor input capacitance not increased by Miller's effect, the gate drive power low, and the turnon switching speed high. The diodes turn on at a very low di/dt. The diode reverse-recovery current is a fraction of a sine wave and becomes a part of the switch current when the switch current is positive. Therefore, the antiparallel diodes can be slow and MOSFETs body-drain diodes are sufficiently fast as long as the reverse-recovery time is less than one-half of the cycle. The diode voltage is kept at a low voltage of the order of 1 V by the transistor in the on-state during the reverse-recovery interval, reducing the diode reverse-recovery power loss. The transistor can be turned on not only when the switch current is negative but also when the switch current is positive and the diode is still conducting because of the reverse-recovery. Therefore, the range of the on-duty cycle of the gate-source voltages and the dead time can be larger. If, however, the dead time is too long, the current will be diverted from the recovered diode D_2 to diode D_1 of the opposite transistor until transistor Q_2 is turned on, causing extra transitions of both switch voltages, current spikes, and switching losses.

Both the switch voltage and current waveforms overlap during turnoff, causing a turnoff switching loss. Also, Miller's effect is considerable, increasing the transistor input capacitance, the gate drive requirements, and reducing the turnoff speed.

Fig. 4 shows a Class D amplifier with various resonant circuits. In Fig. 4, circuit b, C_c is a large coupling capacitor, which can also be connected in series with the load resistance. The resonant frequency (i.e. the boundary between the capacitive and inductive load) for the circuits b–g of Fig. 4 depends on the load. Half-bridge topologies of the Class D voltage-switching amplifier are depicted in Fig. 5. They are equivalent to the basic topology of Fig. 1.

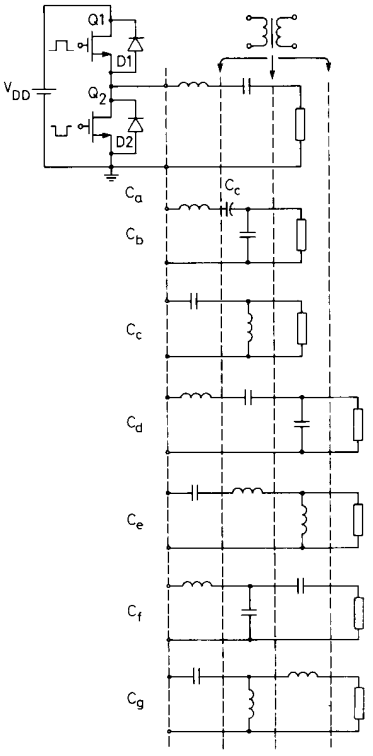

Fig. 4 *Class D zero-voltage-switching amplifier with various resonant circuits C_a–C_g*

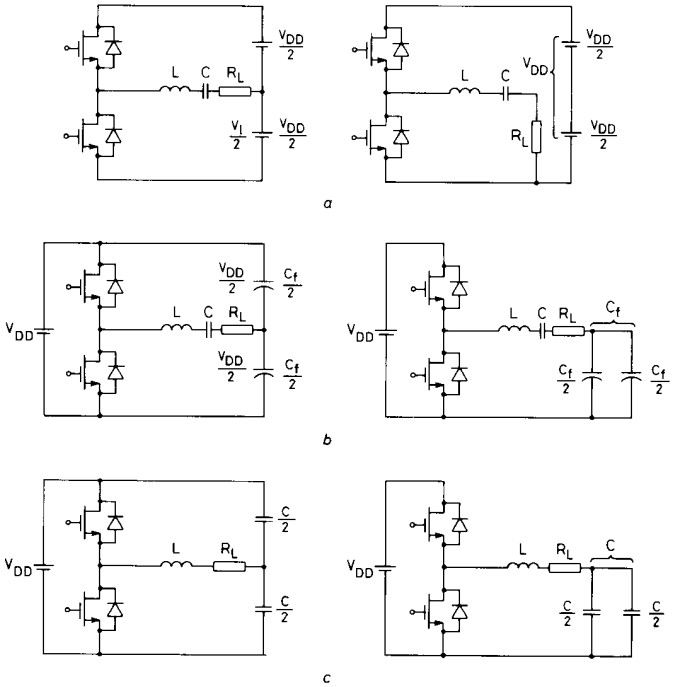

Fig. 5 *Half-bridge topologies of class D amplifier*

a With two DC voltage sources *b* With two filter capacitors *c* With a resonant capacitor split into two halves

In Fig. 5*a*, the DC voltage sources act as short circuits for the AC component. In Fig. 5*b*, filter capacitors $C_f/2$ act as short circuits for the AC component. The DC voltage across each of them is $V_{DD}/2$, but the AC power is dissipated in the ESRs of the capacitors. This is a useful circuit if the DC power supply contains a voltage doubler. In Fig. 5*c*, the resonant capacitor is split into two halves that are connected in parallel for the AC component. Fig. 6 shows a full-bridge topology of the Class D amplifier. The voltage across the series-resonant circuit is a square wave $\pm V_{DD}$. All resonant circuits of Fig. 4 can be used in both half-bridge and full-bridge topologies. Resonant DC/DC convertors are obtained by adding rectifiers at the output of Class D inverters.

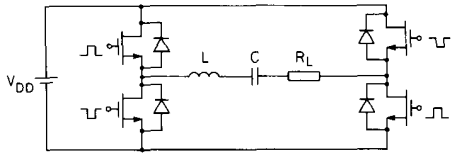

Fig. 6 *Full-bridge topology of class D amplifier*

4 Analysis

4.1 Assumptions

The analysis of the Class D amplifier of Fig. 1 is based on the equivalent circuit of Fig. 2*c* and the following assumptions:

(*a*) The transistor and diode form a resistive switch whose on-resistance is linear, the parasitic capacitances of the switch are neglected, and the switching times are zero.

(*b*) The elements of the series-resonant circuit are passive, linear, time invariant, and the self resonant frequencies of the reactive elements are much higher than the operating frequency f.

(*c*) The loaded quality factor Q_L of the series-resonant circuit is high enough so that the current i through the resonant circuit is sinusoidal.

4.2 Input impedance of the resonant circuit

The parameters of the series-resonant circuit are defined as

- the resonant frequency

$$\omega_r = \frac{1}{\sqrt{(LC)}} \tag{3}$$

- the characteristic impedance

$$Z_o = \sqrt{\left(\frac{L}{C}\right)} = \omega_r L = \frac{1}{\omega_r C} \tag{4}$$

- the loaded quality factor

$$Q_L = \frac{\omega_r L}{R} = \frac{1}{\omega_r CR} = \frac{Z_o}{R} \tag{5}$$

- the unloaded quality factor

$$Q_o = \frac{\omega_r L}{r} = \frac{1}{\omega_r Cr} = \frac{Z_o}{r} \tag{6}$$

The input impedance of the series-resonant circuit is

$$\begin{aligned} Z &= R + j\left(\omega L - \frac{1}{\omega C}\right) = R + jZ_o\left(\frac{\omega}{\omega_r} - \frac{\omega_r}{\omega}\right) \\ &= R\left[1 + jQ_L\left(\frac{\omega}{\omega_r} - \frac{\omega_r}{\omega}\right)\right] \\ &= Z_o\left[\frac{R}{Z_o} + j\left(\frac{\omega}{\omega_r} - \frac{\omega_r}{\omega}\right)\right] = |Z|e^{j\psi} = R + jX \end{aligned} \tag{7}$$

where

$$\begin{aligned} |Z| &= R\sqrt{\left(1 + Q_L^2\left(\frac{\omega}{\omega_r} - \frac{\omega_r}{\omega}\right)^2\right)} \\ &= Z_o\sqrt{\left(\left(\frac{R}{Z_o}\right)^2 + \left(\frac{\omega}{\omega_r} - \frac{\omega_r}{\omega}\right)^2\right)} \\ &= Z_o\sqrt{\left(\frac{1}{Q_L^2} + \left(\frac{\omega}{\omega_r} - \frac{\omega_r}{\omega}\right)^2\right)} \end{aligned} \tag{8}$$

$$\psi = \arctan\left[Q_L\left(\frac{\omega}{\omega_r} - \frac{\omega_r}{\omega}\right)\right] \tag{9}$$

$$R = |Z| \cos\psi \tag{10}$$

$$X = |Z| \sin\psi \tag{11}$$

From eqn. 9

$$\cos\psi = \frac{1}{\sqrt{\left(1 + Q_L^2\left(\frac{\omega}{\omega_r} - \frac{\omega_r}{\omega}\right)^2\right)}} \tag{12}$$

Fig. 7 shows a three-dimensional representation of $|Z|/Z_o$ as a function of the normalised frequency f/f_r and the normalised load resistance R/Z_o. Plots of $|Z|/Z_o$ and

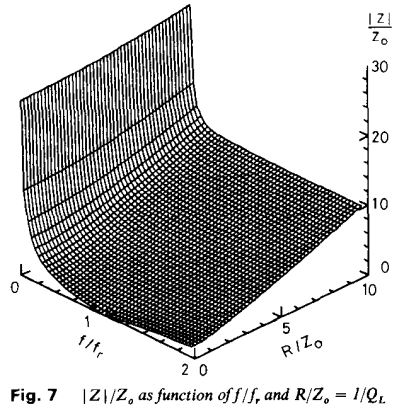

Fig. 7 $|Z|/Z_o$ *as function of* f/f_r *and* $R/Z_o = 1/Q_L$

ψ against f/f_r at fixed values of $R/Z_o = 1/Q_L$ are graphed in Fig. 8. Usually, $|Z|$ is normalised with respect to R, but it is not a good normalisation if R is variable and resonance components L and C are fixed.

4.3 Currents, voltages, and powers

Referring to Fig. 2*c*, the input voltage of the series-resonant circuit is a square-wave

$$v = \begin{cases} V_{DD} & \text{for } 0 < \omega t \leqslant \pi \\ 0 & \text{for } \pi < \omega t \leqslant 2\pi \end{cases} \tag{13}$$

The fundamental component of this voltage is

$$v_{i1} = V_m \sin\omega t \tag{14}$$

where its amplitude can be found from the Fourier analysis

$$V_m = \frac{2V_{DD}}{\pi} \simeq 0.637V_{DD} \tag{15}$$

This leads to the RMS value of v_{i1}

$$V_{rms} = \frac{V_m}{\sqrt{(2)}} = \frac{\sqrt{(2)}V_{DD}}{\pi} \simeq 0.45V_{DD} \tag{16}$$

The current through the switch S_1 is

$$i_{S1} = \begin{cases} I_m \sin(\omega t - \psi) & \text{for } 0 < \omega t \leqslant \pi \\ 0 & \text{for } \pi < \omega t \leqslant 2\pi \end{cases} \quad (17)$$

Hence, from eqns. 8, 10 and 15, one obtains the DC component of the input current

$$\begin{aligned} I_{DD} &= \frac{1}{2\pi}\int_0^{2\pi} i_{S1}\, d(\omega t) = \frac{I_m}{2\pi}\int_0^{\pi} \sin(\omega t - \psi) d(\omega t) \\ &= \frac{I_m \cos\psi}{\pi} = \frac{V_m \cos\psi}{\pi |Z|} = \frac{2V_{DD}\cos\psi}{\pi^2 |Z|} \\ &= \frac{2V_{DD}\cos^2\psi}{\pi^2 R} = \frac{2V_{DD}R}{\pi^2 |Z|^2} \\ &= \frac{I_m}{\pi\sqrt{\left(1 + Q_L^2\left(\frac{\omega}{\omega_r} - \frac{\omega_r}{\omega}\right)^2\right)}} \\ &= \frac{2V_{DD}}{\pi^2 R\left[1 + Q_L^2\left(\frac{\omega}{\omega_r} - \frac{\omega_r}{\omega}\right)^2\right]} \end{aligned} \quad (18)$$

At $f = f_r$

$$I_{DD} = \frac{I_m}{\pi} = \frac{2V_{DD}}{\pi^2 R} \simeq \frac{V_{DD}}{5R} \quad (19)$$

The DC input power can be expressed as

$$\begin{aligned} P_{DD} &= I_{DD} V_{DD} = \frac{2V_{DD}^2 \cos^2\psi}{\pi^2 R} \\ &= \frac{2V_{DD}^2}{\pi^2 R\left[1 + Q_L^2\left(\frac{\omega}{\omega_r} - \frac{\omega_r}{\omega}\right)^2\right]} \\ &= \frac{2V_{DD}^2 R}{\pi^2 Z_o^2\left[\left(\frac{R}{Z_o}\right)^2 + \left(\frac{\omega}{\omega_r} - \frac{\omega_r}{\omega}\right)^2\right]} \end{aligned} \quad (20)$$

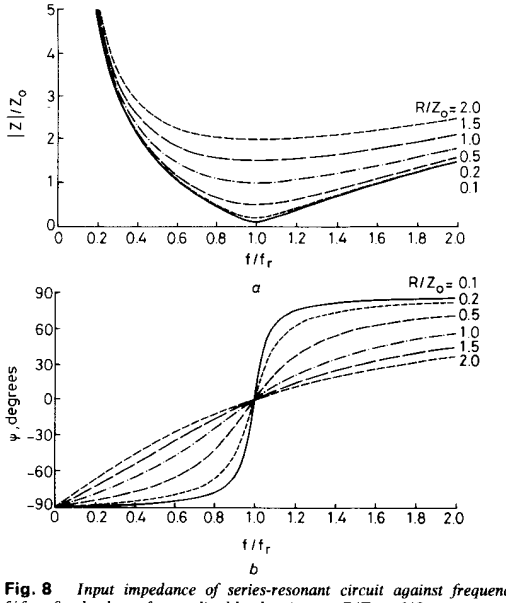

Fig. 8 *Input impedance of series-resonant circuit against frequency f/f_r at fixed values of normalised load resistance $R/Z_o = 1/Q_L$*

a Modulus of normalised input impedance $|Z|/Z_o$ against f/f_r at constant values of R/Z_o

b Phase of input impedance ψ against f/f_r at constant values of $R/Z_o = 1/Q_L$

At $f = f_r$

$$P_{DD} = \frac{2V_{DD}^2}{\pi^2 R} \simeq \frac{V_{DD}^2}{5R} \quad (21)$$

The current through the series-resonant circuit is given by

$$i = I_m \sin(\omega t - \psi) \quad (22)$$

where eqns. 10, 12 and 15 lead to

$$\begin{aligned} I_m &= \frac{V_m}{|Z|} = \frac{2V_{DD}}{\pi |Z|} = \frac{2V_{DD}\cos\psi}{\pi R} \\ &= \frac{2V_{DD}}{\pi R\sqrt{\left(1 + Q_L^2\left(\frac{\omega}{\omega_r} - \frac{\omega_r}{\omega}\right)^2\right)}} \\ &= \frac{2V_{DD}}{\pi Z_o\sqrt{\left(\left(\frac{R}{Z_o}\right)^2 + \left(\frac{\omega}{\omega_r} - \frac{\omega_r}{\omega}\right)^2\right)}} \end{aligned} \quad (23)$$

Fig. 9 shows a three-dimensional representation of $I_m Z_o/V_{DD}$ as a function of f/f_r and R/Z_o. Plots of $I_m Z_o/V_{DD}$ against f/f_r at fixed values of R/Z_o are depicted in Fig. 10. At $f = f_r$

$$I_m = \frac{2V_{DD}}{\pi R} \quad (24)$$

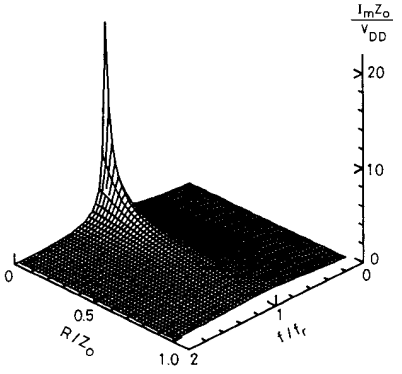

Fig. 9 *Normalised amplitude $I_m Z_o/V_{DD}$ of current through resonant circuit as function f/f_r and $R/Z_o = 1/Q_L$*

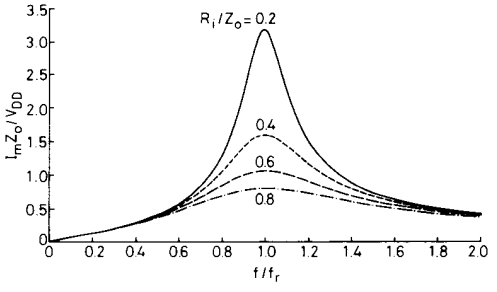

Fig. 10 *Normalised amplitude $I_m Z_o/V_{DD}$ of current in resonant circuit against f/f_r at fixed values of $R/Z_o = 1/Q_L$*

Using eqn. 23, one arrives at the output power

$$P_O = \frac{I_m^2 R_L}{2} = \frac{2V_{DD}^2 R_L \cos^2 \psi}{\pi^2 R^2}$$
$$= \frac{2V_{DD}^2 R_L}{\pi^2 R^2 \left[1 + Q_L^2 \left(\frac{\omega}{\omega_r} - \frac{\omega_r}{\omega}\right)^2\right]}$$
$$= \frac{2V_{DD}^2 R_L}{\pi^2 Z_o^2 \left[\left(\frac{R}{Z_o}\right)^2 + \left(\frac{\omega}{\omega_r} - \frac{\omega_r}{\omega}\right)^2\right]} \quad (25)$$

At $f = f_r$

$$P_O = \frac{2V_{DD}^2 R_L}{\pi^2 R^2} \simeq \frac{V_{DD}^2 R_L}{5R^2} \quad (26)$$

Fig. 11 depicts $P_O Z_o^2/(V_{DD}^2 R_L)$ as a function of f/f_r and R/Z_o. The normalised output power $P_O Z_o^2/(V_{DD}^2 R_L)$ is plotted as a function of f/f_r at different values of R/Z_o in Fig. 12.

The conduction power loss in both transistors and the resonant circuit is

$$P_r = \frac{I_m^2 r}{2} = \frac{I_m^2 (r_{DS} + r_L + r_C)}{2} \quad (27)$$

Neglecting switching losses and using eqns. 20 and 25, one obtains the efficiency of the amplifier

$$\eta = \frac{P_O}{P_{DD}} = \frac{P_O}{P_O + P_r} = \frac{R_L}{R_L + r} = \frac{1}{1 + \frac{r}{R_L}}$$
$$= 1 - \frac{r}{R_L + r} = 1 - \frac{1}{1 + \frac{R_L}{r}} = 1 - \frac{Q_L}{Q_o} \quad (28)$$

It can be seen that the efficiency increases with increasing R_L/r, or decreasing Q_o/Q_L.

The amplitude of the voltage across the capacitor C is obtained from eqn. 23

$$V_{Cm} = \frac{I_m}{\omega C} = \frac{2V_{DD}}{\pi \left(\frac{\omega}{\omega_r}\right) \sqrt{\left(\left(\frac{R}{Z_o}\right)^2 + \left(\frac{\omega}{\omega_r} - \frac{\omega_r}{\omega}\right)^2\right)}} \quad (29)$$

A three-dimensional representation of V_{Cm}/V_{DD} is shown in Fig. 13. Fig. 14 depicts plots of V_{Cm}/V_{DD} as a function of f/f_r at fixed values of R/Z_o.

Likewise, the amplitude of the voltage across the inductor L is expressed as

$$V_{Lm} = \omega L I_m = \frac{2V_{DD}\left(\frac{\omega}{\omega_r}\right)}{\pi \sqrt{\left(\left(\frac{R}{Z_o}\right)^2 + \left(\frac{\omega}{\omega_r} - \frac{\omega_r}{\omega}\right)^2\right)}} \quad (30)$$

Fig. 15 shows V_{Lm}/V_{DD} as a function of f/f_r and R/Z_o. Plots of V_{Lm}/V_{DD} against f/f_r at constant values of R/Z_o are displayed in Fig. 16. At $f = f_r$

$$V_{Cm} = V_{Lm} = Z_o I_m = Q_L V_m = \frac{2V_{DD} Q_L}{\pi} \quad (31)$$

4.4 Short-circuit and open-circuit operation

The Class D amplifier with a series-resonant circuit can operate safely with an open circuit at the output. However, it is prone to catastrophic failure if the output

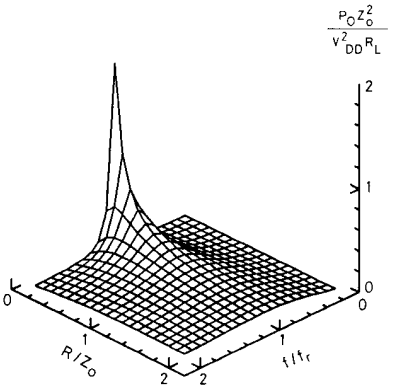

Fig. 11 *Normalised output power $P_O Z_o^2/V_{DD}^2 R_L$ as function of f/f_r and $R/Z_o = 1/Q_L$*

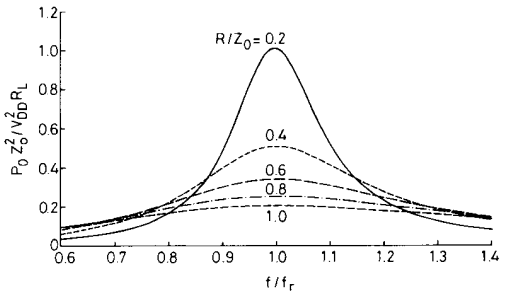

Fig. 12 *Normalised output power $P_O Z_o^2/V_{DD}^2 R_L$ as function of f/f_r and $R/Z_o = 1/Q_L$*

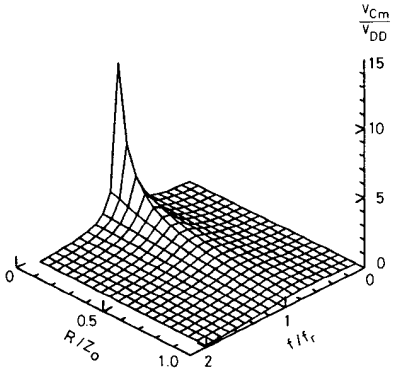

Fig. 13 *Normalised amplitude V_{Cm}/V_{DD} of voltage across resonance capacitor C as function of f/f_r and $R/Z_o = 1/Q_L$*

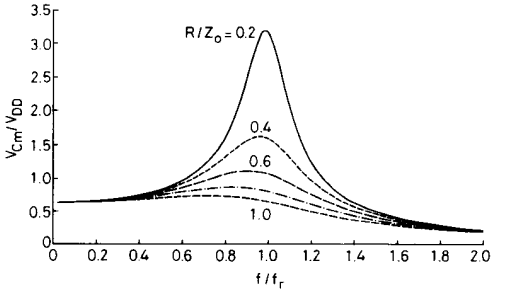

Fig. 14 *Normalised amplitude V_{Cm}/V_{DD} of the voltage across resonance capacitor C against f/f_r at fixed values of $R/Z_o = 1/Q_L$*

is short-circuited at the operating frequency f close to the resonant frequency f_r. If $R_L = 0$, the amplitude of the current through the resonant circuit and the switches is

$$I_m = \frac{2V_{DD}}{\pi r\sqrt{\left(1+\left(\frac{Z_o}{r}\right)^2\left(\frac{\omega}{\omega_r}-\frac{\omega_r}{\omega}\right)^2\right)}} \tag{32}$$

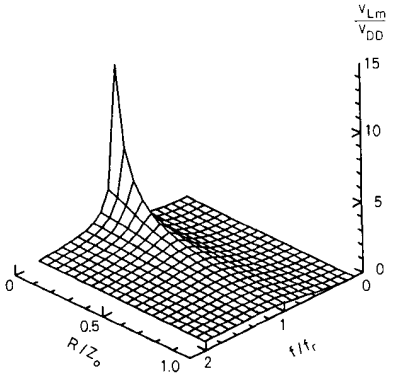

Fig. 15 *Normalised amplitude V_{Lm}/V_{DD} of the voltage across resonance inductor L as function of f/f_r and $R/Z_o = 1/Q_L$*

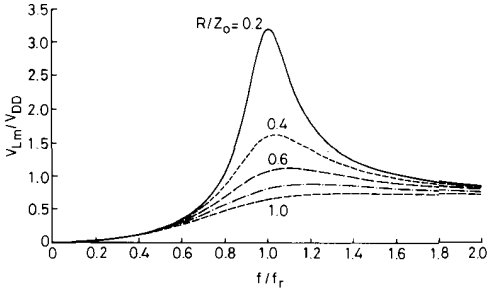

Fig. 16 *Normalised amplitude V_{Lm}/V_{DD} of the voltage across resonance inductor L against f/f_r at fixed values of $R/Z_o = 1/Q_L$*

The maximum value of I_m occurs at $f = f_r$ and is given by

$$I_m = \frac{2V_{DD}}{\pi r} \tag{33}$$

and the amplitudes of the voltages across the resonant components L and C are

$$V_{Cm} = V_{Lm} = \frac{I_m}{\omega_r C} = \omega_r L I_m = Z_o I_m = \frac{2V_{DD}Z_o}{\pi r} \tag{34}$$

For instance, if $V_{DD} = 320$ V and $r = 2\ \Omega$, $I_m = 102$ A and $V_{Cm} = V_{Lm} = 80$ kV. Thus, excessive current in the switches and the resonant circuit as well as the excessive voltages across L and C can lead to catastrophic failure of the amplifier.

5 Turnoff switching loss

The switch current and voltage waveforms during turnoff for $f > f_r$ are sketched in Fig. 17. These waveforms were observed in various Class D experimental circuits. The drain-to-source voltage v_{DS2} during voltage rise time t_r can be approximated by a parabolic function

$$v_{DS2} = a(\omega t)^2 \tag{35}$$

Since $v_{DS2}(\omega t_r) = V_{DD}$, one obtains

$$a = \frac{V_{DD}}{(\omega t_r)^2} \tag{36}$$

Hence, eqn. 35 becomes

$$v_{DS2} = \frac{V_{DD}(\omega t)^2}{(\omega t_r)^2} \tag{37}$$

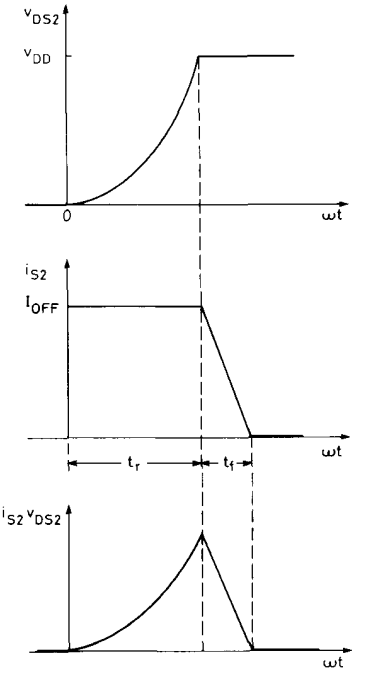

Fig. 17 *Waveforms of v_{DS2}, i_{DS2}, $i_{S2}v_{DS2}$ during turnoff for $f > f_r$*

The switch current during rise time t_r is a small portion of a sinusoid and can be approximated by a constant

$$i_{S2} = I_{OFF} \tag{38}$$

The average value of the power loss associated with voltage rise time t_r is

$$P_{tr} = \frac{1}{2\pi}\int_0^{2\pi} i_{S2}v_{DS2}\,d(\omega t) = \frac{V_{DD}I_{OFF}}{2\pi(\omega t_r)^2}\int_0^{\omega t_r}(\omega t)^2 d(\omega t)$$
$$= \frac{\omega t_r V_{DD}I_{OFF}}{6\pi} = \frac{ft_r V_{DD}I_{OFF}}{3} = \frac{t_r V_{DD}I_{OFF}}{3T} \tag{39}$$

The switch current during fall time t_f can be approximated by a ramp function

$$i_{S2} = I_{OFF}\left(1-\frac{\omega t}{\omega t_f}\right) \tag{40}$$

and the drain-to-source voltage is

$$v_{DS2} = V_{DD} \tag{41}$$

which yields the average value of the power loss associated with current fall time t_f

$$P_{tf} = \frac{1}{2\pi}\int_0^{2\pi} i_{S2}v_{DS2}\,d(\omega t)$$
$$= \frac{V_{DD}I_{OFF}}{2\pi}\int_0^{\omega t_f}\left(1-\frac{\omega t}{\omega t_f}\right)d(\omega t)$$
$$= \frac{\omega t_f V_{DD}I_{OFF}}{4\pi} = \frac{ft_f V_{DD}I_{OFF}}{2} = \frac{t_f V_{DD}I_{OFF}}{2T} \tag{42}$$

Hence, the turnoff switching loss is

$$P_{turnoff} = P_{tr} + P_{tf} = f V_{DD} I_{OFF}\left(\frac{t_r}{3} + \frac{t_f}{2}\right) \quad (43)$$

Usually, t_f is much longer than t_r. The overall power dissipation (excluding the gate drive power) is

$$P_D = P_r + 2P_{turnoff} = \frac{rI_m^2}{2} + f V_{DD} I_{OFF}\left(\frac{2t_r}{3} + t_f\right) \quad (44)$$

6 Example

A Class D amplifier of Fig. 1 will be designed to meet the following specifications: $V_{DD} = 50$ V, $P_O = 12.5$ W, and $f = 110$ kHz.

Assuming $Q_L = 5.5$, $\psi = 30°$ (i.e. $\cos^2 \psi = 0.75$) and the efficiency $\eta = 90\%$, the design procedure is as follows

$$P_{DD} = \frac{P_O}{\eta} = 13.89 \text{ W} \quad (45)$$

$$R = \frac{2V_{DD}^2}{\pi^2 P_{DD}} \cos^2 \psi = 27.35\ \Omega \quad (46)$$

$$R_L = \eta R = 25\ \Omega \quad (47)$$

$$r = R - R_L = 2.35\ \Omega \quad (48)$$

$$I_{DD} = \frac{P_{DD}}{V_{DD}} = 278 \text{ mA} \quad (49)$$

$$I_m = \sqrt{\left(\frac{2P_O}{R}\right)} = 0.956 \text{ A} \quad (50)$$

$$\frac{f}{f_r} = \frac{1}{2}\left(\frac{\tan \psi}{Q_L} + \sqrt{\left(\frac{\tan^2 \psi}{Q_L^2} + 4\right)}\right) = 1.0577 \quad (51)$$

$$f_r = \frac{f}{1.0577} = 104 \text{ kHz} \quad (52)$$

$$L = \frac{Q_L R}{\omega_r} = 230\ \mu\text{H} \quad (53)$$

$$C = \frac{1}{\omega_r Q_L R} = 10.17 \text{ nF} \quad (54)$$

from which $Z_o = \sqrt{(L/C)} = 150\ \Omega$. Hence, $V_{Cm} = V_{Lm} = Z_o I_m = 143.4$ V.

7 Experimental results

The circuit of the Class D amplifier of Fig. 1 was built, using Motorola MTP5N40 MOSFETs as switches S_1 and S_2, $L = 225\ \mu$H, $C = 10$ nF, $R_L = 25.3\ \Omega$. The resonant frequency of the series-resonant circuit was $f_r = 106$ kHz, the operating frequency was $f = 110$ kHz, and the DC supply voltage was $V_{DD} = 50$ V. The transistor on-resistance was $r_{DS} = 1\ \Omega$. The driver had independently adjustable values of both dead times from zero to 4000 ns. The transistors were coupled with the driver by transformers. Experimental waveforms are shown in Fig. 18. The gate-to-source voltages v_{GS1} and v_{GS2} were approximately rectangular waves with a low level of -10 V and a high level of 10 V. The gate current i_{G2} started to flow 400 ns after v_{DS2} had decreased to nearly zero and, therefore, Miller's effect at turnon was zero. Transistor Q_2 turned on at zero voltage, reducing the turnon switching loss. The peak values of the gate current i_{G2} were 42 and -72 mA, and the time interval when the switch current was negative lasted 800 ns. It is worth noting in Fig. 18*b* that the shape of the gate current waveform during turnoff was different than that during turnon.

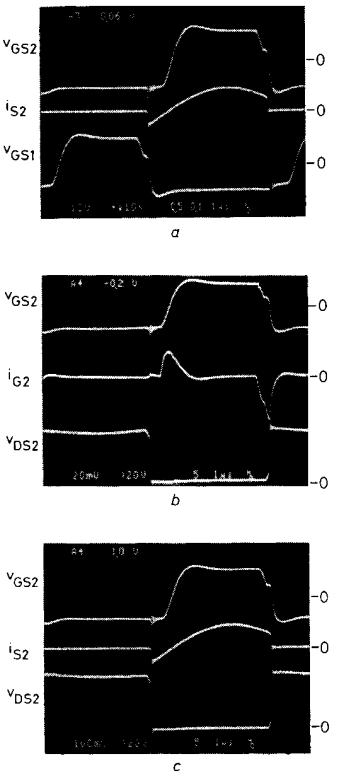

Fig. 18 *Current and voltage waveforms in class D amplifier for $f > f_r$ at $V_{DD} = 50$ V, $R_L = 25\ \Omega$, and $f = 110$ kHz*

a Waveforms of v_{GS2}, v_{S2} and v_{GS1}
b Waveforms of v_{GS2}, i_{G2} and v_{DS2}
c Waveforms of v_{GS2}, i_{S2} and v_{DS2}
Vertical: 1 A/div. for i_{S2}, 40 mA/div. for i_{G2}, 10 V/div. for v_{GS1} and v_{GS2} and 25 V/div. for v_{DS2}; horizontal: 1 μs/div.

Fig. 19*a* and *b* shows waveforms during turnon in the enlarged scale. It can be seen in Fig. 19*a* that the gate-to-source voltage v_{GS2} started to rise when the switch current i_{S2} was negative, 300 ns after v_{DS2} had decreased to -0.7 V. Thus, transistor Q_2 turned on at nearly zero voltage and a negative current. Because v_{DS2} was constant, Millers's effect was zero and did not increase the input gate capacitance C_{g2}. Therefore, the gate current i_{G2} was equal to the derivative of the gate-to-source voltage v_{GS2}, in accordance with the equation: $i_{G2} = (C_{gs2} + C_{gd2})\, dv_{GS2}/dt$. Fig. 19*c* and *d* shows waveforms during turnoff. Three time intervals can be distinguished during turnoff: delay time t_d, voltage rise time t_r, and current fall time t_f. During the delay time $t_d = 250$ ns, the gate current i_{G2} was decreased from zero to -42 mA, causing the gate-to-source voltage v_{GS2} to fall from 10 to 6 V. The bottom transistor Q_2 was still on and acted as a switch, v_{DS2} was nearly zero, and i_{S2} was forced by the current of the series-resonant circuit (i.e. $i_{S2} = -i$). During the rise time $t_r = 200$ ns, i_{G2} was decreased from -42 to -72 mA, but v_{GS2} remained almost constant at 6 V owing to a very large input capacitance caused by

Miller's effect. Voltage v_{DS2} increased slowly at first and then faster from zero to $V_{DD} = 50$ V and $i_{S2} = -i$ was determined by the resonant circuit. Because v_{GS2} was but the switch voltage waveform contained the spikes. Fig. 21*b* shows waveforms when the dead time was longer than that in Fig. 21*a*. Note that transistor Q_2 was

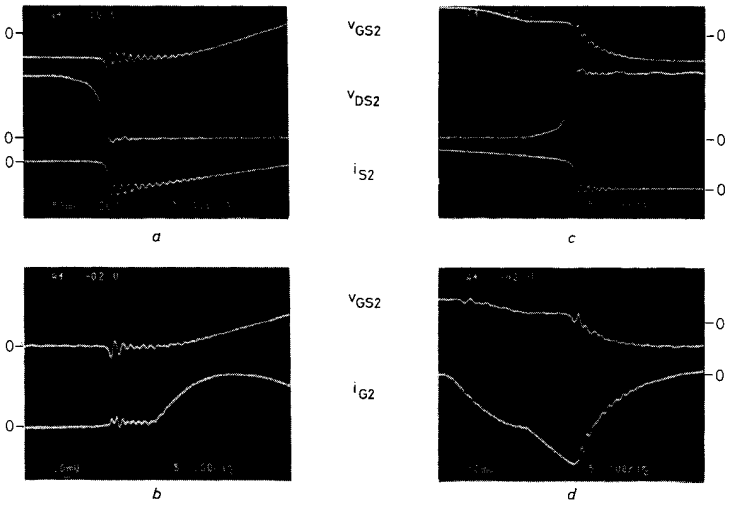

Fig. 19 *Current and voltage waveforms in the class D amplifier during turnon and turnoff for $f > f_r$ at $V_{DD} = 50$ V, $R_L = 25\ \Omega$, and $f = 110$ kHz*

a Waveforms during turnon
b Waveforms during turnon
c Waveforms during turnoff
d Waveforms during turnoff
Vertical: 0.5 A/div. for i_{S2}, 20 mA/div. for i_{G2}, 10 V/div. for v_{GS2}, and 20 V/div. for v_{DS2}

greater than the transistor threshold voltage V_t and v_{DS2} was high, transistor Q_2 was on and acted as a current source. Note that the gate current i_{G2} was not equal to the derivative of the gate-to-source voltage v_{GS2} during time t_r because of a very strong Miller's effect. During the current fall time $t_f = 20$ ns, i_{S2} decreased rapidly, v_{DS2} was equal to V_{DD}, and v_{GS2} decreased to -10 V. The theoretical waveforms of Fig. 17 are close to the experimental waveforms of Fig. 19*c*.

The power loss was estimated as follows. The measured quality factor of the inductor was $Q_{oL} = 242$ at $f_r = 106$ kHz, resulting in the equivalent series resistance $r_L = \omega_r L/Q_{oL} = 1\ \Omega$. The measured equivalent series resistance of C was $r_C = 53\ \text{m}\Omega$. Thus, the total parasitic resistance was $r = r_{DS} + r_L + r_C = 2.053\ \Omega$. The measured peak value of the switch and inductor current was $I_{SM} = I_m = 1$ A. From eqn. 27, the conduction loss was $P_r = rI_{SM}^2/2 = 1.027$ W. Using the measured parameters $V_{DD} = 50$ V, $I_{OFF} = 0.5$ A, $t_r = 200$ ns, $t_f = 20$ ns, and $f = 110$ kHz, one can calculate from eqn. 39 the power loss associated with the voltage rise time $P_{tr} = 183$ mW per transistor, and from eqn. 42 the power loss associated with the current fall time $P_{tf} = 27.5$ mW per transistor. Hence, the turnoff switching loss was $P_{turnoff} = 200.5$ mW per transistor. The overall power dissipation was $P_D = P_r + 2P_{turnoff} = 1.427$ W. The measured input DC power was $P_{DD} = 14.42$ W, resulting in the output power $P_O = 13$ W. Hence, the efficiency of the amplifier was 90%.

Fig. 20 shows waveforms when the dead time at turnoff of Q_2 was too short. There was the time interval during which both v_{GS1} and v_{GS2} were simultaneously high, causing a high spike in the currents of both MOSFETs.

Fig. 21*a* shows waveforms when the dead time was too long. The switch current waveform was still continuous, not turned on when D_2 has already turned off. Therefore, the current of the resonant circuit was diverted from switch S_2 to diode D_1. As a result, v_{DS2} was increased from zero to V_{DD} and then decreased back to zero. These two additional transitions generated a high current spike owing to the reverse recovery of diode D_1 and gave rise to switching power losses.

Fig. 22*a* shows waveforms when transistor Q_2 was turned on at a negative switch current. When v_{GS2} was

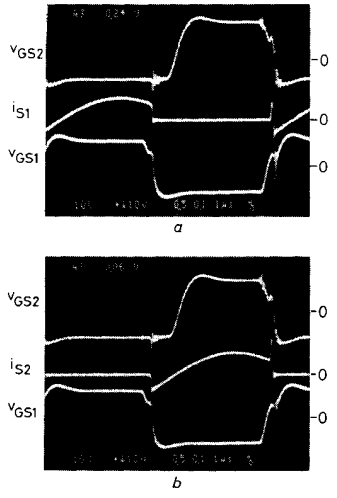

Fig. 20 *Waveforms when dead time at turnoff of bottom MOSFET was too short, causing cross conduction*

a Waveforms of v_{GS1}, v_{GS2} and i_{S2}
b Waveforms of v_{GS1}, v_{GS2} and v_{S1}
Vertical: 1 A and 10 V/div.: horizontal: 1 μs/div.

-10 V, Q_2 was off, D_2 was on, and v_{DS2} was equal to -0.7 V. When Q_2 was turned on, v_{DS2} increased from -0.7 to -0.1 V. Therefore, diode D_2 turned off and Q_2 conducted first the negative and then the positive switch current. Fig. 22*b* shows the waveforms for the case when external Schottky diodes were added as antiparallel diodes. When Q_2 was off, v_{DS2} was -0.5 V and then increased to -0.1 V. Thus, the transistor conducted a negative switch current while on.

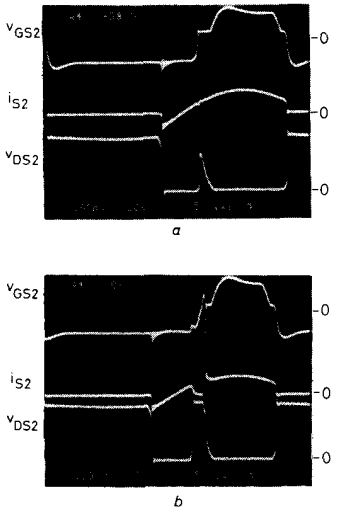

Fig. 21 *Waveforms when dead time at turnon of bottom MOSFET was too long*

a Waveforms of v_{GS2}, i_{S2} and v_{DS2} at boundary between continuous and discontinuous switch current
b Waveforms of v_{GS2}, i_{S2} and v_{DS1} when switch current is discontinuous
Vertical: 1 A/div. for i_{S2}, 10 V/div. for v_{GS2}, and 25 V/div. for v_{GS2}; horizontal: 1 μs/div.

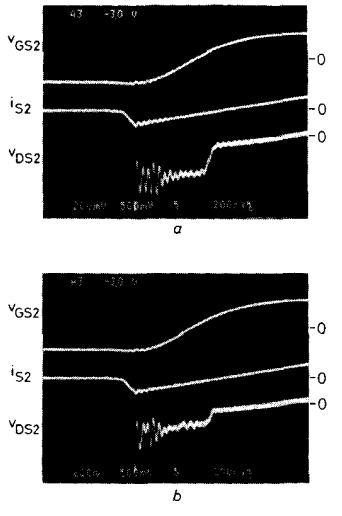

Fig. 22 *Waveforms of* v_{GS2}, i_{S2}, and v_{DS2} when switch current is negative

a Without external diodes
b With external Schottky diodes.
Vertical: 10 V/div. for v_{GS2}, 0.4 V/div. for i_{S2} m and 0.5 V/div. for v_{DS2}; horizontal: 1 μs/div.

Fig. 23 shows waveforms of Q_2 for $f < f_r$. It can be seen from Fig. 23*a* that high current spikes occurred at both the turnon and turnoff transitions. The peak value of the spikes was almost three times higher than that of the steady-state switch current. These spikes may damage the transistors. Fig. 23*b* shows waveforms for the case when Schottky diodes were added to the transistors as antiparallel diodes. As seen, the peak values of the spikes were reduced and did not exceed the peak value of the steady-state switch current, preventing the destruction of the transistors. However, the switching losses were much higher than those for $f > f_r$. There are two reasons for reduction of the spikes. First, the reverse recovery is not present in Schottky diodes. Second, the threshold voltage of Schottky diodes is lower than that of silicon *pn* junction diodes. Therefore, when the transistor is off, most of the negative switch current flows through the Schottky diode.

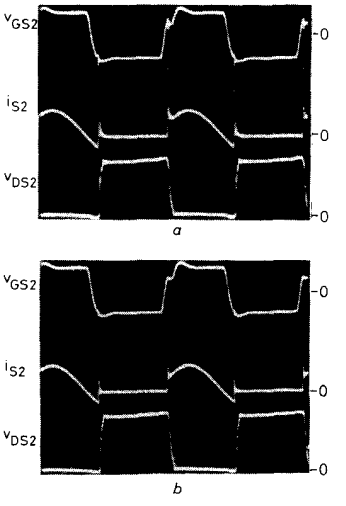

Fig. 23 *Waveforms of* v_{GS2}, i_{S2}, and v_{DS2} for $f < f_r$

a Without external diodes
b With external Schottky diodes
Vertical: 10 V/div. for v_{GS2}, 1 A/div. for i_{S2}, 25 V/div. for v_{DS2}; v_{DS2}; horizontal: 2 μs/div.

8 Conclusions

The class D amplifier was analysed and experimentally verified. Simple design equations were derived. The basic characteristics of the amplifier are listed below:

(*a*) The operation with a capacitive load (i.e. below resonance) is not recommended. The antiparallel diodes turn off at a high *di/dt*. If MOSFETs body-drain *pn* junction diodes (or any *pn* junction diodes) are used as antiparallel diodes, they generate high reverse-recovery current spikes. These spikes occur in the switch current waveforms at both the switch turnon and turnoff and may destroy the transistors. The current spikes can be reduced by adding Schottky antiparallel diodes (if V_{DD} is below 100 V) or a series diode and an antiparallel diode. The transistors are turned on at a high voltage equal to V_{DD} and the transistor output capacitance is short-circuited by a low transistor on-resistance, dissipating the energy stored in that capacitance. Therefore, the turnon switching loss is high, Miller's effect is significant, the transistor input capacitance is high, the gate drive power is high, and the turnon transition speed is reduced.

(*b*) The operation with an inductive load (i.e. above resonance) is preferred. The antiparallel diodes turn off at a low *di/dt*. Therefore, MOSFETs body-drain *pn* junction diodes can be used as antiparallel diodes because they do not generate reverse-recovery current spikes and are sufficiently fast. The transistors turnon at zero voltage. For this reason, the turnon switching loss is reduced, Miller's effect is absent, the transistor input capacitance is low, the gate drive power is low, and turnon speed is high. However, the turnoff is lossy.

(*c*) The efficiency is high at light loads because R_L/r increases with increasing R_L.

(*d*) The amplifier can operate safely with an open circuit at the output.

(*e*) It is prone to catastrophic failure if the output is short-circuited at the operating frequency f close to the resonant frequency f_r.

Although this paper has been focused on MOSFETs, other power switches can be used such as BJTs, thyristors, MCTs, GTOs, and IGBTs.

9 Acknowledgment

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10 References

1 BAXANDALL, P.J.: 'Transistor sine wave LC oscillators, some general considerations and new developments', *IEE Proc. B, Electr. Power Appl.*, 1959, **106**, (16), pp. 748–758

2 OSBORNE, M.R.: 'Design of tuned transistor power amplifier', *Electron. Eng.*, 1968, **40**, (486), pp. 436–443

3 CHUDOBIAK, W.J., and PAGE, D.F.: 'Frequency and power limitations of Class D transistor amplifier', *IEEE J. Solid-State Circuits*, 1969, **SC-4**, (1), pp. 25–37

4 KAZIMIERCZUK, M., and MODZELEWSKI, J.S.: 'Drive-transformerless Class D voltage-switching tuned power amplifier', *Proc. IEEE*, 1980, **68**, (6), pp. 740–741

5 RAAB, F.H.: 'Class D power amplifier load impedance for maximum efficiency'. RF Technology Expo'85 Conference, Anaheim, CA, USA, Jan. 1985, pp. 287–295

6 STEIGERWALD, R.L.: 'A comparison of halfbridge resonant converter topologies', *IEEE Trans. Power Electron. (USA)*, 1988, **3**, (2), pp. 174–182