A 0.9-V 0.5-μA Rail-to-Rail CMOS Operational Amplifier

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***Abstract*—A 0.9-V 0.5-μA, rail-to-rail CMOS operational amplifier designed with weak inversion techniques is presented. Depletion-mode nMOS transistors buffer a bulk-driven pMOS differential pair to realize wide input dynamic range, while the output stage architecture provides symmetric rail-to-rail output drive through the use of a low-voltage translinear control circuit.**

***Index Terms*—Analog integrated circuits, MOSFET amplifiers.**

I. Introduction

REDUCING power consumption in portable applications has made lower supply voltages increasingly common in systems with large digital content. Since many portable products operate from alkaline or rechargeable nickel–metal hydride or nickel–cadmium batteries, the operating supply voltage for these systems is migrating down to 0.9 V for a single battery cell. These decreasing supply voltages often have a detrimental effect upon analog components in these systems, however. For example, operational amplifiers may require new circuit architectures to maximize dynamic range while operating with the reduced supply voltage headroom. Additionally, the supply current of the amplifier should be minimized to improve the battery life of the product.

As an example of techniques which can be used to meet the stringent requirements of portable systems, the operational amplifier described here achieves a common-mode input voltage range which includes the supply rails, a rail-to-rail output range within 10 mV of the supplies into a 100-kΩ load, and operates with a bias current of 0.5 μA from a 0.9-V supply. The amplifier, designed in a CMOS process with weak inversion techniques [1], utilizes an input stage with a combination of depletion-mode n-channel transistors and a bulk-driven p-channel differential pair to achieve wide common-mode input voltage range. The output stage includes a low-voltage, class-AB rail-to-rail architecture with symmetrical output drive capabilities. Since the amplifier was designed with low power precision dc applications in mind, a 2.5-μm n-well CMOS process was used to minimize cost.

Section II of this paper begins with a review of rail-to-rail input stage architectures and then presents the input stage designed for this amplifier. Section III describes the output stage circuitry of the operational amplifier. Section IV discusses the bias circuitry and trim networks which were utilized. Finally, the experimental results are presented in Section V.

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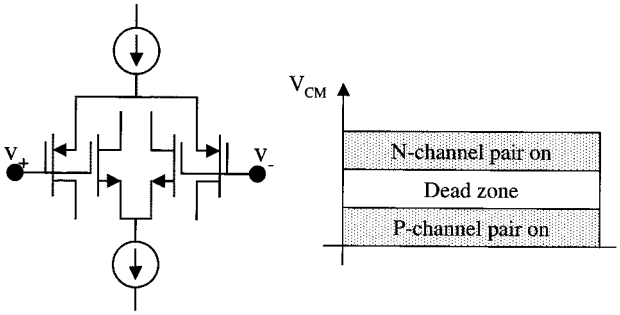

Fig. 1. Complementary differential transconductor.

II. Input-Stage Circuit Architectures

A. Rail-to-Rail Input Architectures

Perhaps the most difficult circuit design challenge for the low-voltage operational amplifier is the design of an input stage with a rail-to-rail common-mode voltage range. Much work has been reported on input stages with complementary differential pairs and associated circuit networks used to maintain constant transconductance over the input voltage range [2], [3]. However, at low supply voltages, the sum of the common-mode voltage ranges of the n-channel and p-channel differential pairs may become larger than the available supply voltage, creating a "dead zone" in the amplifier's common-mode input range [4], as shown in Fig. 1. The minimum supply voltage range of an amplifier with a complementary input stage can then be described as

$$V_{\mathrm{SUPPLY}} \geq V_{\mathrm{GS(N)}} + V_{\mathrm{GS(P)}} + 2^{*}V_{\mathrm{DS(SAT)}} \qquad (1)$$

where V_{SUPPLY} is the amplifier supply voltage, $V_{\mathrm{GS(N)}}$ and $V_{\mathrm{GS(P)}}$ are the gate source voltages of the n-channel and p-channel differential pairs, respectively, and $V_{\mathrm{DS(SAT)}}$ is the saturation voltage of each differential pair's current source bias.

The complementary input architecture also suffers from reduced common-mode rejection as the input control of the amplifier is switched from the p-channel to the n-channel differential pairs. Since the input offset voltages of the n-channel and p-channel differential pairs likely have different values, the effective input offset voltage of the amplifier may exhibit a discontinuity as the control of the input stage shifts between these differential pairs. This mechanism will degrade the common-mode rejection of the amplifier.

Another rail-to-rail input stage technique utilizes a bulk-driven differential pair for the input stage, which is shown in Fig. 2 [5]. This technique modulates the threshold voltages of the differential pair to generate transconductance (g_M), though not as efficiently as the conventional gate-driven

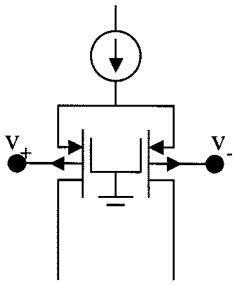

Fig. 2. Bulk-driven differential transconductor.

differential pair. For example, the g_M of a bulk-driven differential pair in this CMOS process is approximately 30% of its gate-driven equivalent. Although the bulk-driven differential pair can achieve rail-to-rail common-mode input range at low supply voltages, it suffers from a large voltage-dependent input capacitance due to the junction capacitance, and increased input bias currents at low common-mode input voltages. The input currents can become substantial as the threshold voltage increases, due to the larger source-bulk junction bias. These input currents can become problematic in the amplifier feedback network, especially with the large impedances used in low-power portable applications.

A third rail-to-rail input stage technique utilizes an n-channel depletion-mode differential pair, as shown in Fig. 3 [6], [7]. The differential pair relies upon modulating the source-bulk bias voltage as a function of the input common-mode voltage, which dynamically increases the threshold voltage of the depletion input differential pair. The transistors essentially operate as depletion-mode transistors at low common-mode voltages, where the gate-source voltage ($V_{\rm GS}$) of the transistors is negative. This allows sufficient bias voltage for the differential pair's bias current source. As the common-mode voltage increases, the threshold voltages of the transistors become more positive, their $V_{\rm GS}$ voltages become positive, and eventually the transistors operate in enhancement mode at common-mode voltages near the positive supply. This maintains the operation of the differential pair transistors in saturation.

Compared to the previously discussed rail-to-rail input architectures, the depletion-mode differential pair is the most elegant approach. However, to operate properly with a 0.9-V supply voltage, the use of the n-channel depletion-mode differential pair places constraints upon the intrinsic threshold voltage and the bulk or well doping concentration of the n-channel depletion-mode transistors. A good example of the problem occurs when the amplifier's common-mode voltage is near the negative supply, where the depletion-mode differential pair needs to provide sufficient bias voltage for its bias current source. In weak inversion operation, the $V_{\rm GS}$ voltage is a weak function of the ratio of the drain current and the device aspect ratio. But since the drain current also determines the g_M of the differential pair, it may be difficult to find the proper bias point for the circuit in a given process technology.

Further, sufficient back-gate modulation of the threshold voltage is required to generate a sufficiently large threshold voltage shift when the common-mode voltage is at the positive supply. If the increase in $V_{\rm GS}$ due to back-gate effect is too small, the differential pair transistors will not have enough drain–source voltage ($V_{\rm DS}$) to operate in saturation, and the transconductance of the input stage will decrease at high common-mode voltages. Therefore, the design flexibility for a weak inversion depletion-mode differential pair is small, since the device process parameters of threshold voltage and back-gate modulation factor dictate if the transconductor operates properly over the entire common-mode voltage range.

More design flexibility is available when biasing the depletion-mode differential pair in strong inversion, since the $V_{\rm GS}$ voltage can be designed to offer the correct source voltage to the bias current source when the common-mode voltage is near the negative supply. But since

$$(V_{\rm GS} - V_t) \propto G_M \tag{2}$$

the transconductance of the input stage is determined by this bias point constraint. A large modulation factor to shift the transistor $V_{\rm GS}$ is also still required.

B. New Rail-to-Rail Input Stage

The input stage architecture used in this amplifier is shown in Fig. 4. An enhancement, bulk-driven differential pair of p-channel transistors, MP1 and MP2, is used to generate transconductance. However, instead of driving the bulks directly from the inputs, depletion-mode n-channel transistors MN1 and MN2 are used as source followers to buffer the inputs from the p-channel bulk terminals. MN1 and MN2 also provide a common-mode dependent level-shifting function to the bulk terminals, which minimizes excess bulk currents when the input common-mode voltages are near V_{EE} potentials. The modulated drain currents of MP1 and MP2 are folded into the current summing nodes of the cascode circuit at the sources of MN3 and MN4, with current mirror MP3 and MP4 performing a differential-to-single-ended conversion to the high impedance output node V_{O1}.

The use of the depletion-mode source followers MN1 and MN2, in conjunction with the bulk-driven p-channel differential pair MP1 and MP2, allows additional design flexibility to meet the rail-to-rail input requirements of the amplifier. The input depletion-mode source followers may be designed to level-shift the input signal to MP1 and MP2 without a large impact on the overall transconductance of the input stage, which is mainly determined by MP1 and MP2 and their bias current. In fact, MN1 and MN2 can be operated in strong inversion if the process technology and bias point of the circuit dictate. This allows the input circuit architecture to be used over a greater range of threshold voltages and well concentrations for the depletion-mode transistors.

The design methodology for input source followers MN1 and MN2 is shown below. The drain current in a MOS transistor operating in weak inversion is given by [1]

$$I_D = I_{\rm DO}\frac{W}{L}\exp\left(\frac{V_{\rm GS}}{nV_T}\right) \cdot\left(\exp\left(\frac{-V_{\rm SB}}{V_T}\right) - \exp\left(\frac{-V_{\rm DB}}{V_T}\right)\right) \tag{3}$$

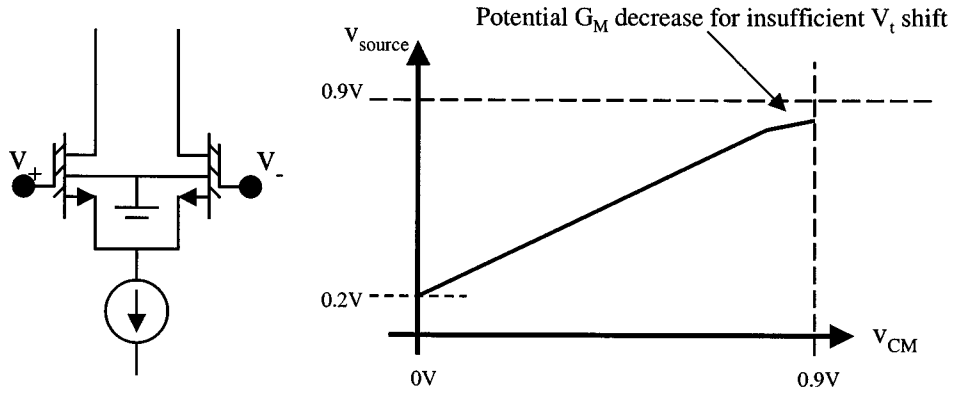

Fig. 3. Depletion-mode n-channel differential transconductor.

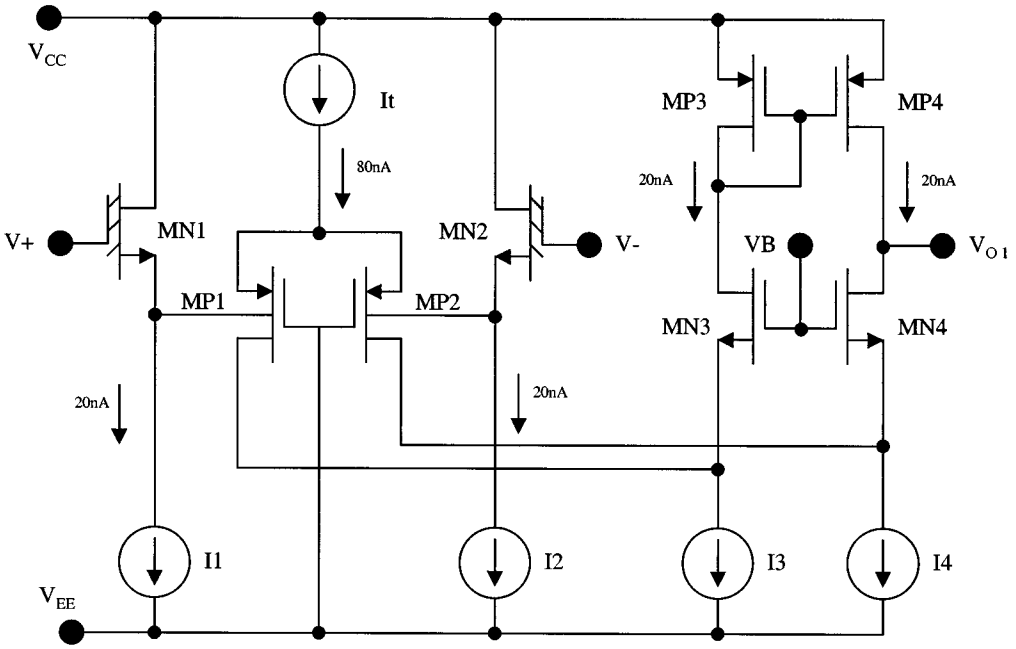

Fig. 4. Amplifier input stage.

where n is the subthreshold slope factor, $V_{\rm T}$ is the thermal voltage, and $I_{\rm DO}$ is the characteristic current of the device. Solving (3) for $V_{\rm GS}$ gives

$$V_{\rm GS} = nV_T \left(\ln\left(\exp\left(\frac{-V_{\rm SB}}{V_T} \right) - \exp\left(\frac{-V_{\rm DB}}{V_T} \right) \right) - \ln\left(\frac{I_D}{I_{\rm DO} \dfrac{W}{L}} \right) \right) \quad (4)$$

which can be further simplified (assuming $V_{\rm DB} \gg V_{\rm SB}$) to

$$V_{\rm GS} = nV_{\rm SB} + C. \quad (5)$$

Therefore, $V_{\rm GS}$ increases as a linear function of $V_{\rm SB}$. As $V_{\rm SB}$ increases to the positive supply voltage, the influence of the $V_{\rm DB}$ term may become significant if the threshold voltage modulation due to back gate effect is not sufficiently large (i.e., the transistor's $V_{\rm DS}$ voltage is small). The constant C, which is determined by the bias and aspect ratio of the transistor, can be adjusted to give a desired $V_{\rm GS}$ value when $V_{\rm SB} = 0$ ($V_{\rm CM} = 0$) to meet biasing requirements, such as for current source I_1 in Fig. 4. But since the n-channel depletion-mode transistors MN1 and MN2 act as source followers and do not substantially affect the input stage transconductance, the designer has more flexibility in meeting the bias point constraints and target transconductance of the input stage in a given process.

The minimum operating power supply of this input stage to meet rail-to-rail input common-mode requirements is determined by the threshold voltage shift due to back-gate effect in the process. Insufficient threshold voltage modulation decreases the transconductance at common-mode voltages near the positive supply, since the g_M of input follower transistors MN1 and MN2 decreases when they operate in linear mode. Conversely, the input stage will operate at supply voltages lower than 0.9 V with the common-mode range decreasing below the positive supply.

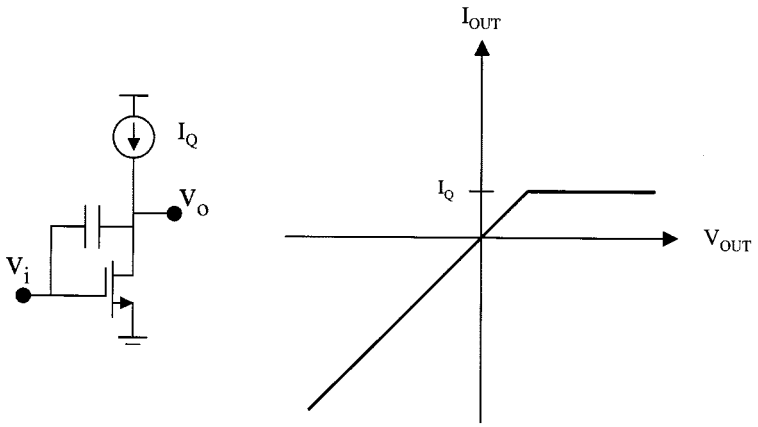

Fig. 5. Class-A common source output stage and output current versus output voltage into a resistive load.

III. New Rail-to-Rail Output Stage

The common source CMOS output stage, like the one illustrated in Fig. 5, is an example of a simple circuit capable of operating at low supply voltages down to 0.9 V. Unfortunately, it does not meet the requirements of many systems due to unsymmetrical output drive. A true rail-to-rail output stage capable of sourcing and sinking equal amounts of current is often desired. Ideally, a complementary push–pull class-AB output stage uses a predriver which provides a relationship between the sink and source currents of the output stage such that

$$I_{\mathrm{SINK}} * I_{\mathrm{SOURCE}} \propto C \tag{6}$$

where C is a constant. A minimum value for I_{SINK} or I_{SOURCE} may also be desired.

Low-voltage CMOS output stages which operate from supply voltages down to one V_{GS} and one or two $V_{\mathrm{DS(SAT)}}$ voltages have been presented [8], [9]. These architectures, which utilize differential connections at their inputs, require twice the compensation capacitance as the traditional single-ended two-stage amplifier structure. Since die area was a concern in this design, rather than frequency response, an architecture that minimized compensation capacitance and complexity was a goal. Another reported design used a switched capacitor approach to dynamically bias the output stage [10], but this would require an oscillator and clock generation.

The output stage architecture used in this design is shown in Fig. 6. The output p-channel transistor MP5 is driven directly from the high impedance node of the amplifier at node V_{O1} to attain minimal phase loss through the slower p-channel signal path. The drain current in n-channel output transistor MN8 is controlled by the current densities of a closed loop of n-channel V_{GS} voltages formed by transistors MN5, MN6, and MN7. This translinear loop provides a means of creating an inverse relationship between the drain currents of MN8 and MP5. Replica transistor MP6 provides a current proportional to the current in MP5 to current mirror MN9 and MN10. The output p-channel replica current is then introduced to the control loop, which drives the gate of MN8. Resistors R1 and R2 provide sufficient voltage for current sources $I7$ and MN10 to operate in saturation. The absolute tolerances of these resistors is not critical, and a reasonable degree of matching to 5% or less is sufficient. R1 and R2 were implemented in high-sheet-resistance polysilicon in this example. Assuming weak inversion operation in the transistors, the current in MN8 is given by

$$I_{\mathrm{MN8}} = \frac{12I^2}{\left(\frac{I_{\mathrm{MP5}}}{2} - I\right)} \tag{7}$$

where I is the unit current of 20 nA. Current sources $I5$ and $I7$ each draw a unit current I, while current source $I6$ is set to 2^*I. The inverse relationship between I_{MN8} and I_{MP5} gives the desired push–pull functionality required for the output stage. Additionally, the control circuit may drive the gate of MN8 nearly to V_{CC}, since current $I6$ is larger than $I7$. This allows output transistors MP5 and MN8 to supply large symmetrical output currents when the amplifier is overdriven to either supply.

The transconductance of the input stage and the compensation capacitor C_{C} set the unity gain bandwidth of the amplifier, assuming a single pole response. This assumption holds unless the frequency response of the output stage, due to secondary poles at the output node or in the signal path, is less than or on the order of the desired unity gain bandwidth. A further examination of the output stage frequency response is then helpful in understanding the overall amplifier characteristics.

The frequency response of the output stage is easily understood when the amplifier sources current to the output load. The input stage drives output common source transistor MP5 directly, which supplies the majority of the signal current. Increasing output source current further increases the g_M of MP5 above its quiescent point, which improves the pole-splitting behavior provided by compensation capacitor C_{C}. Alternatively, increasing the sinking current of the output stage causes the more complex signal path to output common source transistor MN8 to dominate the frequency response. MP6 converts the input signal to a current, which is then mirrored by MN9 and MN10, and added to the differential pair MN5 and MN6 to create the appropriate gate voltage to MN8. Since MP5 and MN8 have an inverse current drive relationship, the current in MP6, MN9, and MN10 decreases as the sinking current in MN8 increases. When the currents in MN6, MN9, and MN10 decrease such that the sum of the currents from $I7$ and MN10 are less than or equal to the current in $I6$, the impedance seen at the gate of output transistor MN8 increases substantially. At this

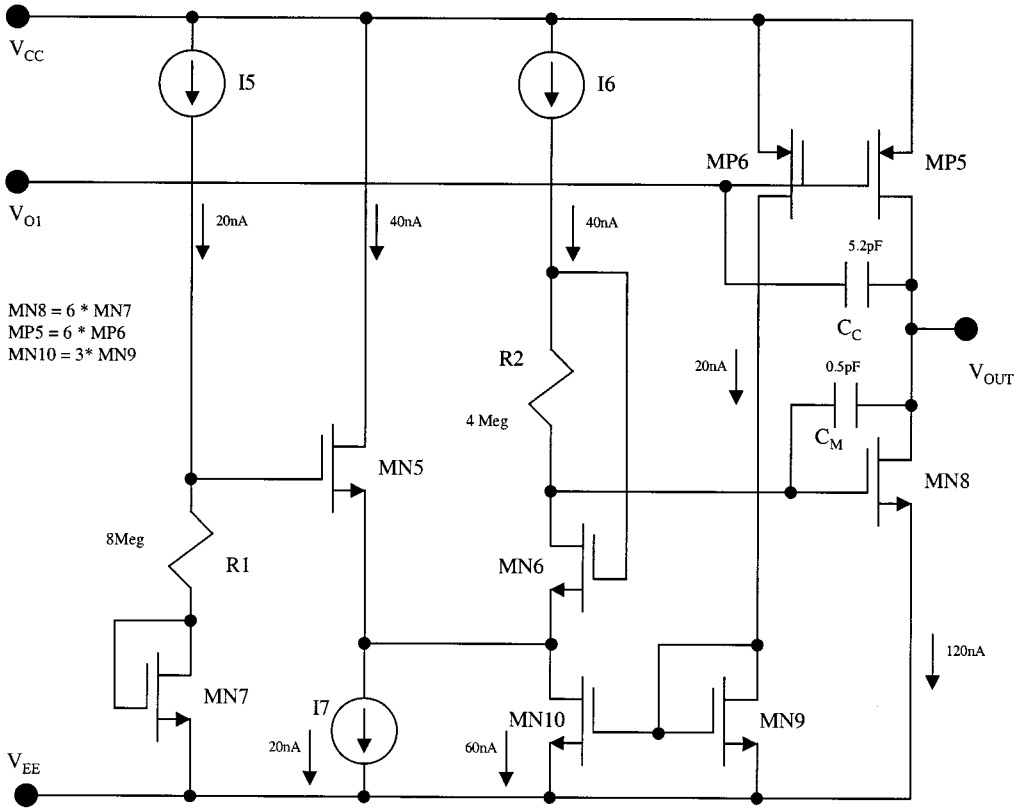

Fig. 6. Amplifier output stage.

point, the amplifier has three stages of voltage gain with a nested Miller compensation provided by $C_{\rm C}$ and $C_{\rm M}$, where the second pole of the amplifier is set by the transconductance of MP6 and $C_{\rm M}$. As long as this second pole stays at a sufficiently higher frequency than the unity gain bandwidth while sinking current, amplifier stability will be maintained. Since this amplifier had a low unity gain bandwidth of approximately 10 kHz, this restriction on the frequency response due to the translinear network was easily met.

The weak dependence of g_M on $V_{\rm GS}$ and the low $V_{\rm DS(SAT)}$ voltages of MOSFET's which operate in weak inversion (on the order of $3^*V_{\rm T}$ [1]) make the realization of sufficient dc gain in a two-stage amplifier architecture at 0.9 V possible. In strong inversion, where the g_M of transistors is a linear function of $V_{\rm GS}$, cascades of gain stages are often the only option to generate sufficient dc gain at low supply voltages, which leads to more complex compensation schemes.

IV. Bias and Trim Circuitry

Fig. 7 shows the bias circuitry used in the amplifier. MP14 and MP15 form a current mirror, which sets the currents in MN10 and MN11 to equal values. MN10 is chosen to be larger than MN11 by an integer multiple N, such that the voltage at the source of MN10 is given by

$$V_{\rm S(MN10)} = V_{\rm DS(MN13)} + nV_T \ln(N). \tag{8}$$

where $V_{\rm T}$ is the thermal voltage. The current in the bias generator is set by the choice of aspect ratio for MN12 and MN13 and

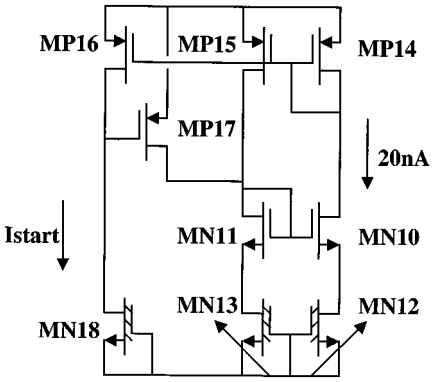

Fig. 7. Amplifier bias circuitry.

multiple N. MN12 and MN13 are depletion-mode n-channel transistors used in their linear region of operation to set the source impedances of MN10 and MN11. The effective resistance of MN12 is chosen larger than MN13, which gives the bias current by the expression

$$I_{\rm BIAS} = nV_T \ln(N) u_N C_{\rm OX} V_t \left(\frac{W}{L_{13}} - \frac{W}{L_{12}} \right) \tag{9}$$

where V_t is the depletion mode n-channel threshold voltage, u_N is the mobility, and $C_{\rm OX}$ is the oxide capacitance. Equation (9) assumes that the impedance of MN12 and MN13 is linear with $V_{\rm DS}$, which holds reasonably well for small values of $V_{\rm DS}$. MN12 and MN13 were used to set the source impedances of MN10 and MN11 in the bias circuit rather than poly resistors to

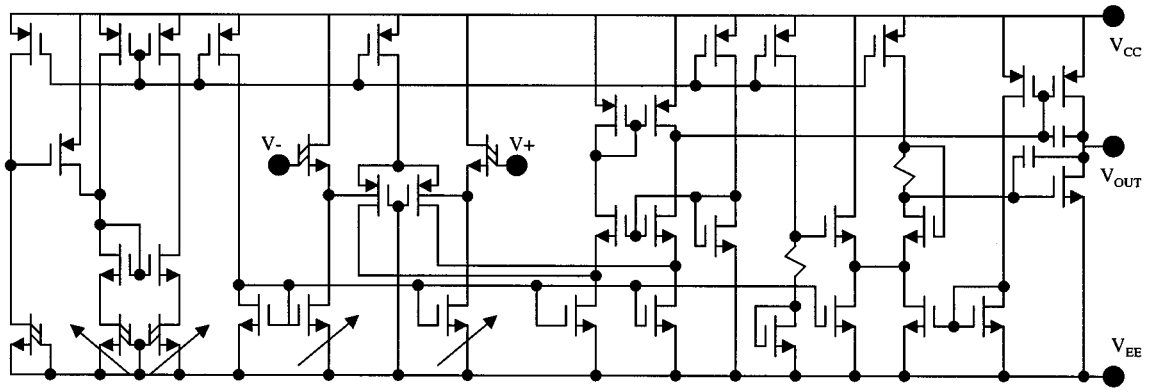

Fig. 8. Schematic of entire 0.9-V rail-to-rail amplifier.

TABLE I
PERFORMANCE SUMMARY, $V_{CC} = 0.9$ V, $V_{EE} = 0$ V, $T = 25$ C

Input Voltage Range	$V_{EE} < V_{IN} < V_{CC}$
Output Voltage Swing (R_L=100kΩ to V_{CC}/2)	+0.89V/+0.01
Supply Current	0.36μA min./0.50μA max.
Input Offset Voltage (trimmed)	< 2.6mV
Output Source Current (Vin = 10mV, Vout = V_{CC}–0.1V)	32μA min./105μA max.
Output Sink Current (Vin = 10mV, Vout = V_{EE}+0.1V)	31μA min./88μA max.
DC Gain (R_L=1MΩ)	70dB min./79dB max.
CMRR ($V_{EE} < V_{IN} < V_{CC}$)	26dB min./59dB max.
Unity Gain Bandwidth (V_{IN} = 0.45V, Z_L = 1MΩ//12pF)	5.6kHz
Phase Margin (V_{IN} = 0.45V, Z_L = 1MΩ//12pF)	62 degrees

minimize die size while generating 20-nA currents. As an additional benefit, MN12 and MN13 also provided a lower temperature coefficient than did high-sheet-resistance poly resistors. The bias current for the amplifier is adjusted at the wafer level by changing the aspect ratio of MN12 and MN13 with a trimming network of poly fuses.

Since the bias circuit uses positive feedback to set equal currents in MN10 and MN11, a startup circuit must be used to ensure the bias network does not latch to a zero current value. This is accomplished by comparing the drain current in current mirror MP16 to a startup current threshold, which is generated here with a depletion-mode n-channel current source. When the current in MP16 is lower than Istart, MP17 injects current into the bias reference node created by MN11. After MP16's drain current exceeds startup current Istart from MN18, MP17 is biased off so that the bias network is unaffected by the startup circuitry. MN18 can be replaced with a large startup resistor with similar results.

Fig. 8 shows a schematic of the entire amplifier. The amplifier utilizes a poly fuse trimming technique to adjust the input offset voltage as well as the overall bias current of the amplifier. The input offset voltage of the amplifier is adjusted by trimming the bias current to the input n-channel depletion-mode followers MN1 and MN2.

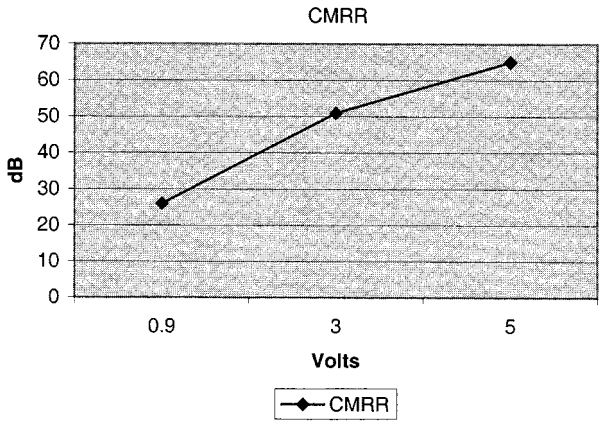

Fig. 9. Measured worst-case CMRR versus supply voltage.

V. EXPERIMENTAL RESULTS

The amplifier's characteristics are summarized in Table I for a 0.9-V supply. The amplifier is rated to operate on a supply voltage of up to 6 V. Common-mode rejection ratio (CMRR) suffers at the lowest supply voltage of 0.9 V due to insufficient threshold voltage shift in the depletion-mode nMOS followers at worst-case process and temperature corners. CMRR improves to over 50-dB worst case with a supply voltage of 3 V, since a larger change in common-mode voltage causes a larger threshold voltage change in the depletion-mode nMOS input transistors as the common-mode voltage nears V_{CC}. The CMRR for the amplifier as a function of supply voltage is shown in Fig. 9. A higher well concentration for the depletion-mode n-channel transistors would also improve the threshold voltage modulation, and thus the CMRR. The amplifier is capable of a large output drive current of over 30 μA compared to its low quiescent current of less than 500 nA, due to the drive capability of the class-AB output stage.

Fig. 10 shows the input and output waveforms of the amplifier in a unity-gain buffer configuration with a single 0.9-V supply. An input signal of greater than 1.1 V is applied to illustrate the rail-to-rail capabilities of the input and output circuits of the amplifier. An input frequency of 10 Hz is used to maintain sufficient loop gain during the measurement.

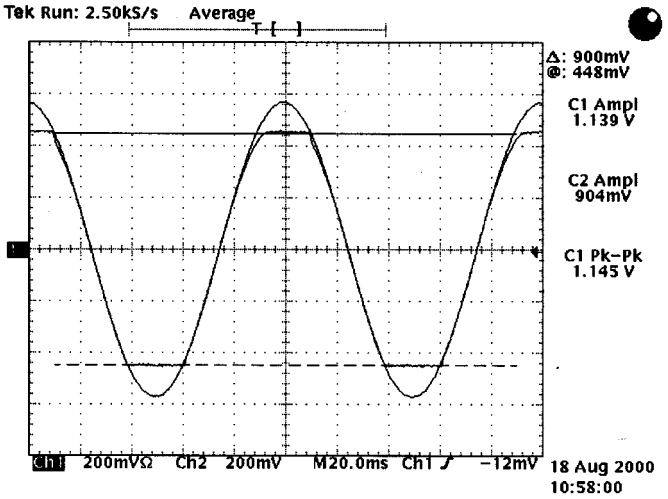

Fig. 10. Amplifier input and output rail-to-rail waveforms at 0.9-V supply.

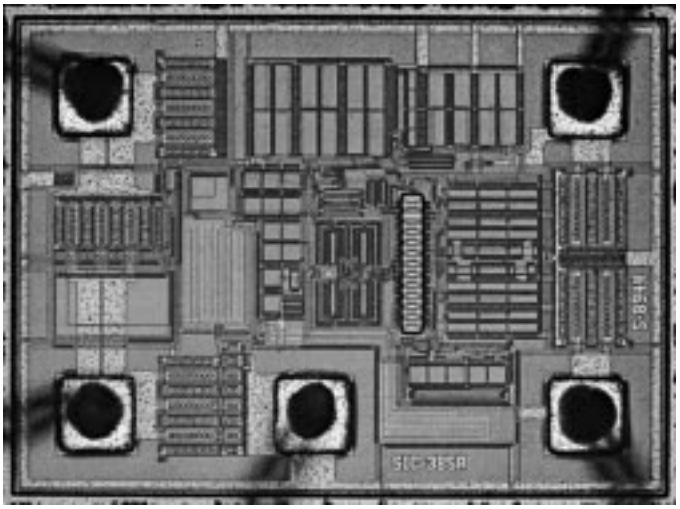

Fig. 11. Die photograph.

Fig. 11 shows a die photograph of the amplifier. The amplifier has a die area of approximately 0.5 mm^2 in a 2.5-μm n-well CMOS process. The input stage transistors were drawn in a cross-coupled quad configuration and placed in the interior of the die to minimize stress effects on transistor matching.

VI. Conclusion

A 0.9-V 0.5-μA rail-to-rail CMOS operational amplifier has been presented. A new low-voltage input stage has been described which utilizes the body effect to modulate the threshold voltage of depletion-mode n-channel input voltage followers, which level-shift the input voltage to a bulk-driven p-channel differential pair. A new output stage circuit has also been described which provides high output current drive capability at low supply voltages, while maintaining good stability and output drive symmetry. The amplifier has a dc gain of 70 dB with a 1-MΩ load, and drives over 30 μA from a 0.9-V supply.

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