Dynamic Current-Matching Charge Pump and Gated-Offset Linearization Technique for Delta-Sigma Fractional-N PLLs

Tsung-Hsien Lin, *Member, IEEE*, Ching-Lung Ti, and Yao-Hong Liu, *Member, IEEE*

***Abstract*—This paper proposes a novel charge pump (CP) circuit and a gated-offset linearization technique to improve the performance of a delta-sigma ($\Delta\Sigma$) fractional-N PLL. The proposed CP circuit achieves good up/down current matching, while the proposed linearization method enables the PFD/CP system to operate at an improved linear region. The proposed techniques are demonstrated in the design of a 2.4-GHz $\Delta\Sigma$ fractional-N PLL. The experimental results show these techniques considerably improve the in-band phase noise and fractional spurs. In addition, the proposed gated-offset CP topology further lowers the reference spurs by more than 8 dB over the conventional fixed-offset approach. This chip is implemented in the TSMC 0.18-μm CMOS process. The fully-integrated $\Delta\Sigma$ fractional-N PLL dissipates 22 mW from a 1.8-V supply voltage.**

***Index Terms*—Charge pump (CP), delta-sigma modulation, fractional-N phase-locked loop, phase-frequency detector (PFD), phase-locked loop (PLL).**

I. Introduction

PHASE-LOCKED loops (PLLs) are often adopted to implement frequency synthesizers in various wireless communication systems. The classical integer-N PLL frequency synthesizer is considered to be well understood and less complicated to design. The PLL behavior and its performance can be predicted within a reasonably good accuracy. However, the integer-N PLL has some limitations. To ensure a stable operation, the PLL loop bandwidth (f_{BW}) is constrained by the reference frequency (f_{ref}; typically, $f_{BW} < f_{ref}/10$), which is often dictated by the frequency resolution (channel spacing) of a wireless communication system. Such narrow bandwidth requirement translates to a slower loop settling behavior and less suppression of VCO phase noise. The design tradeoffs among the PLL settling speed, VCO noise suppression, and the frequency resolution seriously limit the usefulness of the integer-N PLLs.

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T.-H. Lin is with the Graduate Institute of Electronics Engineering and the Department of Electrical Engineering, National Taiwan University, Taipei 106, Taiwan (e-mail: thlin@cc.ee.ntu.edu.tw).

C.-L. Ti was with the Graduate Institute of Electronics Engineering, National Taiwan University, Taipei 106, Taiwan. He is currently with MStar Semiconductor, Inc., Hsinchu, Taiwan.

Y.-H. Liu is currently with the Graduate Institute of Electronics Engineering, National Taiwan University, Taipei 106, Taiwan.

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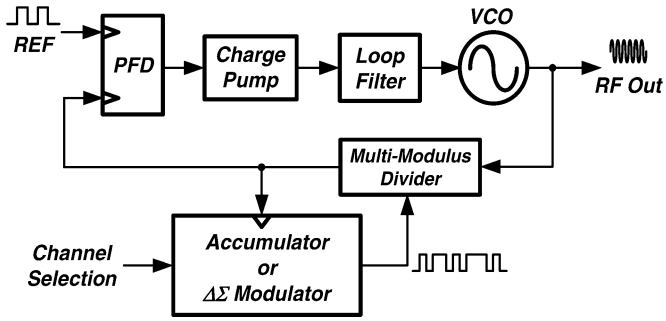

Fig. 1. Block diagram of a typical fractional-N PLL.

To decouple the relationship between the loop bandwidth and frequency resolution, the fractional-N architecture can be adopted. A fractional-N PLL can allow a wide loop bandwidth (hence fast settling) and achieve fine frequency resolution simultaneously. In addition, it can support various reference frequencies [1], [2]. However, the design complexity of a fractional-N PLL increases significantly. In particular, the PLL performance is highly sensitivity to system nonlinearity, which is attributed to various circuit imperfections. In this study, circuit techniques are proposed in order to address this design challenge.

This paper is organized as follows. In Section II, the impact of the nonlinearity on a delta-sigma ($\Delta\Sigma$) fractional-N PLL is discussed. A phase-domain model is devised to investigate this impact. In Section III, the proposed techniques to address the linearity concern and improve PLL performance are described. The realization of a 2.4-GHz $\Delta\Sigma$ fractional-N PLL which incorporates these proposed techniques is presented in Section IV. Finally, experimental results and conclusions are given in Sections V and VI, respectively.

II. Fractional-N PLL Design Issues

Fig. 1 depicts the block diagram of a typical fractional-N PLL. The operation principle behind a fractional-N PLL lies in controlling the divider operation. Instead of fixing the divide number, dithering the divide ratio of the multi-modulus divider (MMD) accomplishes an equivalent fractional divider [1], [2].

In the most basic form of a fractional-N PLL, the divide ratio is dithered with an accumulator. In this topology, the PLL suffers from the fractional spur arose from the periodical pattern of the phase comparison error. The problem of periodic phase error

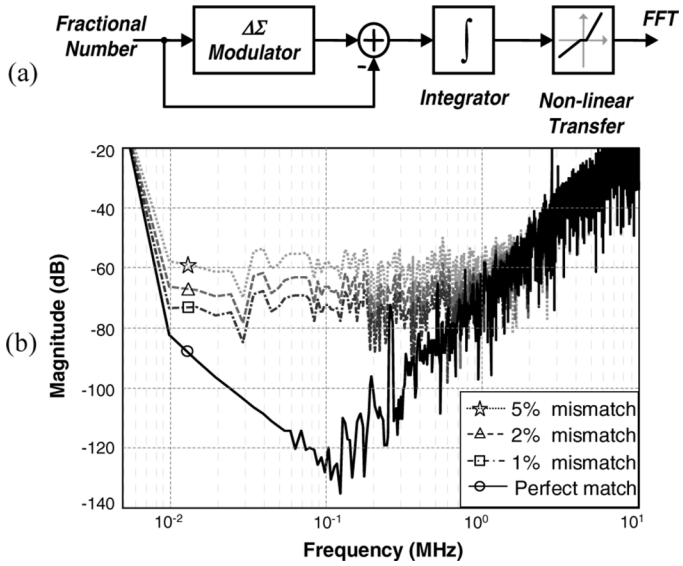

Fig. 2. (a) Phase-domain behavioral model to examine the nonlinearity effect on a $\Delta\Sigma$ fractional-N PLL. (b) Simulated phase noise at divider output under different charge pump current mismatch conditions.

may be alleviated by canceling these errors with appropriate current pulses at the charge pump output [2]. Unfortunately, finite matching accuracy limits the effectiveness of this approach [3].

Alternatively, the dithering operation can be controlled by a $\Delta\Sigma$ modulator [4]. A $\Delta\Sigma$ modulator shapes the quantization noise to higher frequencies through the feedback operation; hence, the signal-to-noise ratio (SNR) within the frequency band of interests is improved. However, if nonlinearity appears in any part of the $\Delta\Sigma$-modulated fractional-N PLL system, the effect of noise shaping is deteriorated. The modulated and shaped quantization noise will be folded back to lower frequencies and result in an increased in-band noise and elevated fractional spurs.

In a fractional-N PLL system, the sources of nonlinearity include phase-frequency detector and charge pump (PFD/CP) nonlinear transfer characteristic, jitters of the frequency dividers [5]–[7], and VCO gain nonlinearity. In the PFD/CP circuits, the nonlinearity is mainly attributed to the up/down (charging/discharging) current mismatch and the gain (slope) variation around the region of zero phase error; while in the dividers, the circuit timing jitters modulate the zero-crossing points of a signal and cause the system to exhibit nonlinear behavior.

Examining the impacts of the nonlinearity is important in designing a fractional-N PLL. Although a transistor-level transient simulation may be the most accurate way in studying these effects, such simulations are time-consuming and are difficult to carry out. Some mixed-mode simulators can speed up this process, although a considerable amount of simulation resources are still required. In this work, a phase-domain model, shown in Fig. 2(a), is adopted to study the impact of the nonlinearity on a $\Delta\Sigma$ fractional-N PLL [7]. In Fig. 2(a), the $\Delta\Sigma$ modulator output is first subtracted by the input fractional number to remove the dc component. The subtractor output represents frequency fluctuation due to the modulation operation. The phase noise is next obtained by integrating the frequency fluctuation. To see how this model can be applied to study the nonlinear effects on the noise, consider the CP up/down current mismatch effect as an example. Since the electrical charges deposited on the loop filter will be affected by the current variations of the CP, the nonlinearity due to this phenomenon can be modeled by multiplying the integrator output with a nonlinear transfer function.

Fig. 2(b) shows the simulation results when 0%, 1%, 2%, and 5% CP up/down current mismatches are applied to this model. The current mismatch is modeled as a gain (slope) variation in the nonlinear transfer function block. It is evident that the nonlinearity has the undesired effect of folding high frequency noise back to lower frequencies. With even just 1% of current mismatch, the in-band phase noise is significantly raised. Hence, techniques to improve the system linearity are indispensable in building a $\Delta\Sigma$ fractional-N PLL.

III. Proposed Linearization Techniques

Here, the proposed circuit techniques, including a novel CP circuit and linearization schemes, are presented.

A. Dynamic Current-Matching CP

As described earlier, the PFD/CP nonlinear transfer characteristic is a major cause of nonlinearity in a PLL system. The nonlinearity is mainly attributed to CP up/down current mismatch and deadzone phenomena [6], [7]. The deadzone problem can be alleviated by adding a proper delay in the PFD reset path, hence often leaving the current mismatch as the dominant source of nonlinearity. The noise degradation attributed to CP up/down current mismatch is already demonstrated in Fig. 2. This problem is further complicated by the fact that the amount of current mismatch varies with process corner variations, and is also dependent on the CP output voltage (which can span over a wide range), due to the channel-length modulation effect.

Some layout techniques (e.g., common centroid style layout) should be applied to improve the quality of matching. To mitigate the effect of channel-length modulation, long-channel transistors are employed in designing the up/down current sources. The transistor width must be scaled proportionally to keep a small overdrive voltage to allow a wide voltage varying range at the CP output. This sizing approach improves the current mismatch at the cost of increased chip area. Furthermore, large devices are accompanied by larger parasitic capacitance which corrupts the CP transient response (e.g., via clock feedthrough, charge injection, etc.) considerably, and may require strong buffering stages preceding the CP.

To address this issue, a novel CP circuit is proposed [8]. The main objective here is to design a reasonably sized CP circuit to achieve the performance of a large-sized one for area efficiency and minimizing the unwanted transient corruptions. The proposed CP circuit is depicted in Fig. 3. This CP is based on a switches-in-source architecture [9]. Two extra feedback transistors, $\mathrm{M_{fbN}}$ and $\mathrm{M_{fbP}}$, are added to the circuit. The role of these two devices is to compensate for the channel-length modulation effect of the up/down current mirrors via negative feedback. The amount of compensation is dynamically adjusted according to the CP output voltage $(\mathrm{V_{CP}})$.

The operation of the proposed CP is described below. In a conventional design (without the two extra devices), if $\mathrm{V_{CP}}$

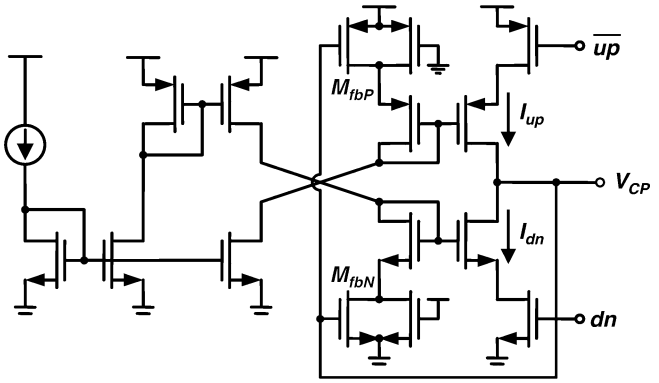

Fig. 3. Simplified schematic of the proposed dynamic current-matching charge pump circuit.

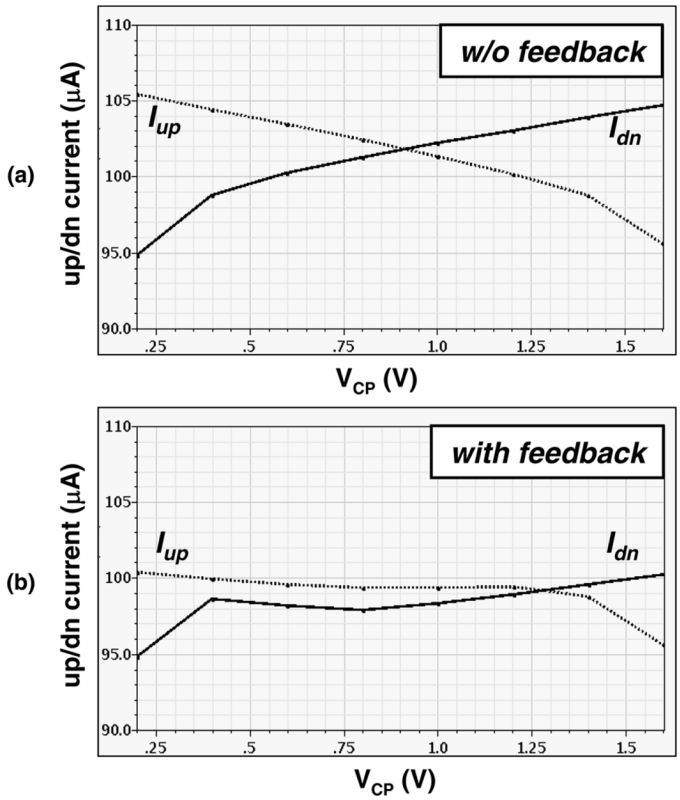

Fig. 4. CP up/down currents: (a) without feedback transistors and (b) with the proposed dynamic feedback technique.

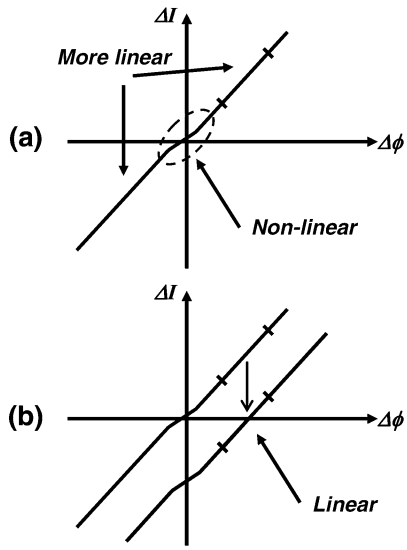

Fig. 5. (a) Conventional PFD/CP transfer characteristic and its operation region. (b) PFD/CP characteristic curve with a shifted operation.

rises during PLL operation, the down current $(\mathrm{I_{dn}})$ increases while the up current $(\mathrm{I_{up}})$ decreases, due to the channel-length modulation effect. With the addition of the two feedback transistors ($\mathrm{M_{fbN}}$ and $\mathrm{M_{fbP}}$), as the voltage further increases, transistor $\mathrm{M_{fbN}}$ enters deep triode region eventually. The lowered device on-resistance aids to reduce the amount of current mirrored to the output down current branch; hence reduces the difference between $\mathrm{I_{dn}}$ and $\mathrm{I_{up}}$. Similarly, if $\mathrm{V_{CP}}$ increases, transistor $\mathrm{M_{fbP}}$ enters the triode region. The lowered device on-resistance reduces the amount of current mirrored to the output up current branch, and improves the current matching between $\mathrm{I_{dn}}$ and $\mathrm{I_{up}}$. The proposed CP circuit dynamically adjusts the biasing conditions of the feedback transistors $\mathrm{M_{fbN}}$ and $\mathrm{M_{fbP}}$ and achieves a more balanced up/down currents.

Fig. 4 shows the simulated CP up/down currents. When the feedback transistors are added to the CP, the amount of mismatch is reduced considerably from 8% to 3% over a wide output voltage range from 0.3 to 1.5 V (under a 1.8-V supply voltage). It is further reduced to 1.5% within a range from 0.4 to 1.4 V. Note that the proposed CP circuit only requires two small extra transistors and does not need an extra amplifier to regulate the currents [10]. Therefore, the proposed circuit technique is area efficient and does not incur extra noise.

B. Linearization by Adding a Gated-Offset Current

Conventionally, the PFD/CP of a fractional-N PLL operates around the region of zero phase error $(\Delta\phi \approx 0)$ when the loop is in lock, as illustrated in Fig. 5(a). Unfortunately, the linearity near the center is often inferior, due to various practical design imperfections. If the operation region can be shifted to an upper or lower part of the transfer curve, the nonlinear operation region around the origin is avoided, as illustrated in Fig. 5(b) [6], [7]. One technique of implementing the shifting operation is to introduce a dc offset current to the CP output [Fig. 6(a)] to enable the PFD/CP system operating in a linear region.

The amount of applied offset must be sufficiently large to completely move away from the nonlinear region near the center. On the other hand, too much offset increases both the reference spurs (as will be explained next) and the CP noise contribution to the PLL. The amount of required offset current $(\mathrm{I_{offset}})$ is determined by the CP current $(\mathrm{I_{CP}})$, the desired divide ratio (N), and the variable division range of the MMD $(\Delta\mathrm{N})$. From Fig. 5(a), the phase operation range on the PFD/CP transfer curve is related to the divider ratios as

$$\phi_{\mathrm{op}} = 2\pi \times \Delta N/N. \tag{1}$$

Observed also from Fig. 5, the amount of shifting should be greater than half of the operating region (ϕ_{op}) plus the size of

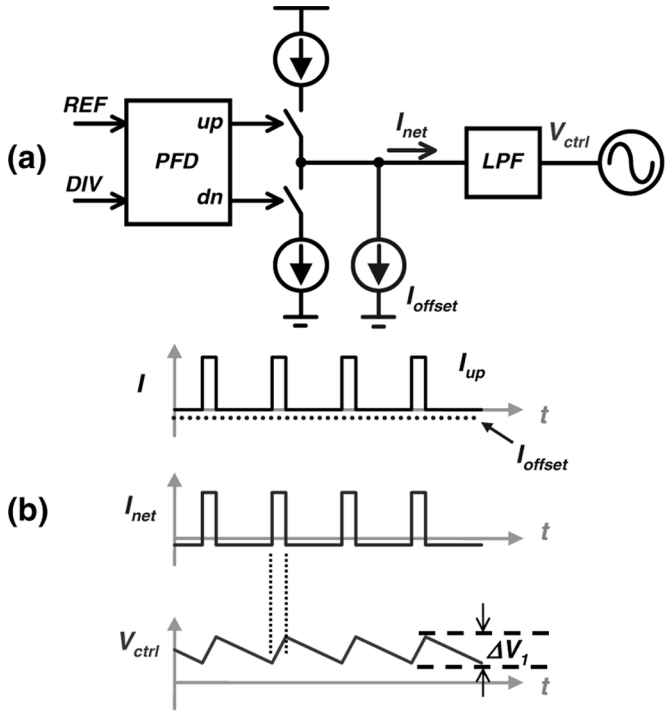

Fig. 6. (a) PFD/CP with a fixed-offset CP current. (b) Timing diagrams of the fixed-offset operation (the LPF is simplified with a capacitor only).

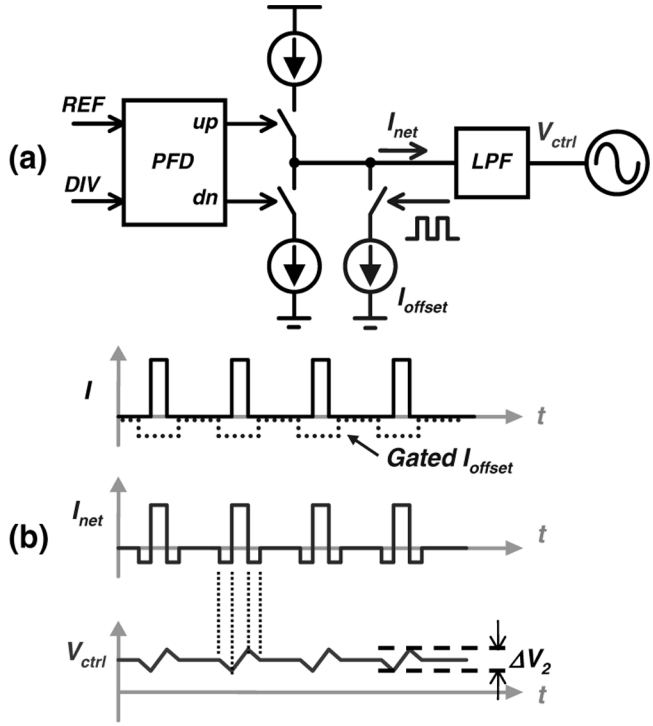

Fig. 7. (a) PFD/CP with a gated-offset CP current. (b) Timing diagrams of the gated-offset operation.

the PFD dead-zone (T_{DZ}), if any. Hence, the minimum offset current should satisfy the following:

$$I_{\mathrm{offset}} \geq \frac{I_{\mathrm{cp}}}{2} \times \frac{\Delta N}{N} + \frac{I_{\mathrm{cp}}}{2} \times \frac{T_{\mathrm{DZ}}}{T_{\mathrm{ref}}}. \tag{2}$$

For a 2.44-GHz PLL with a 20-MHz reference frequency and a third-order MASH 1-1-1 controlled MMD, N and ΔN are 122 and 7, respectively. In practice, the amount of offset to yield the optimal improvement will be greater than that predicted in (2).

Alternatively, this offset scheme can also be implemented in the PFD circuit [8]. By adding an additional fixed delay to one of the PFD reset paths (e.g., the down path), down current pulses with fixed pulsewidth are created each time a phase comparison takes place. The down pulses are balanced by the varying up current pulses. Since only the up current pulsewidth is varying, the PFD/CP operation is effectively shifted to a linear region. The nonlinearity problem is therefore alleviated. The mismatch between up and down current only adds to offset and not to the nonlinearity.

In order to see how the fixed offset current affects the reference spurs, the relationship between the voltage ripples on $\mathrm{V_{ctrl}}$ and the amplitude of the spurious tones must be derived first. Assuming the voltage ripple can be approximated as a sinusoidal signal with an amplitude of $\mathrm{V_{ripple}}$ and a frequency of $\mathrm{f_m}$. By applying the narrowband FM approximation, it can be shown that the magnitude of spurs ($\mathrm{A_{spur}}$) caused by the voltage ripple is related to the oscillation amplitude ($\mathrm{A_{VCO}}$) as follows [11], [12]:

$$\left[\frac{A_{\mathrm{spur}}}{A_{\mathrm{VCO}}}\right]_{\mathrm{dBc}} = 20\log\frac{V_{\mathrm{ripple}}K_{\mathrm{VCO}}}{2f_m}. \tag{3}$$

In (3), $\mathrm{K_{VCO}}$ is the VCO tuning gain (in Hz/V). From (3), it is readily seen that large ripple and $\mathrm{K_{VCO}}$ lead to higher spurious tones (and degrade PLL phase noise performance). In the fixed-offset CP topology [Fig. 6(a)], $\mathrm{V_{ripple}}$ can be directly calculated for a given offset current ($\mathrm{I_{offset}}$) and loop filter topology. The relative amplitude of the spurious tones (in dBc) can then be computed from (3). In this case, the modulating frequency ($\mathrm{f_m}$) of interests is the PLL reference frequency, $\mathrm{f_{ref}}$.

To preserve the advantage of linear operation of the offset-current technique while improving the reference spurs, this work further introduces the gated-offset technique. As shown in Fig. 7(a), the applied CP offset current is now duty-cycled instead of being a fixed value. If the clock signal employed to "gate" the offset current has a proper phase with respect to the current pulses from the main CP, the resulted $\mathrm{V_{ctrl}}$ ripple is reduced. This idea is conceptually illustrated in Fig. 7(b), where $\Delta\mathrm{V_2}$ will be smaller than $\Delta\mathrm{V_1}$ of Fig. 6(b), provided the offset current is gated properly. As a result, the reference spurs are reduced.

The effect of the gated-offset technique can be derived by decomposing the net current ($\mathrm{I_{net}}$) going into the loop filter into two parts: the CP current ($\mathrm{I_{cp}}$) and the gated-offset current ($\mathrm{I_{gated}}$), as depicted in Fig. 8. Assuming the current pulses have an average period of T ($\mathrm{T} = 1/\mathrm{f_{ref}}$), and the average duty cycle of $\mathrm{I_{cp}}$ is $\mathrm{d_1}$, and the duty cycle of $\mathrm{I_{gated}}$ is $\mathrm{d_2}$ ($\mathrm{d_2}$ is 50% in this design). The phase relationship between these two current pulses is denoted by ϕ. By taking the Fourier series of $\mathrm{I_{cp}}$ and $\mathrm{I_{gated}}$ and concentrating on the index terms of -1 and 1, the spur magnitude ($\mathrm{Spur_{gated}}$) at the reference frequency ($\mathrm{f_{ref}}$) is obtained. This result is then normalized to the spur magnitude

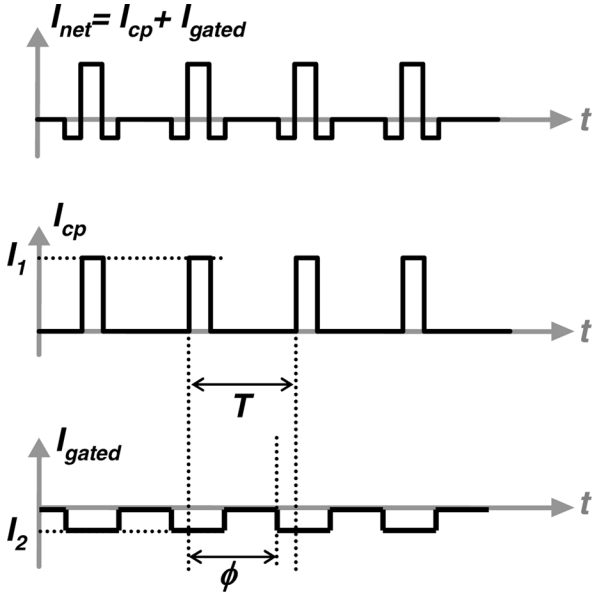

Fig. 8. Waveforms illustrating the decomposition of $\mathrm{I_{net}}$ into $\mathrm{I_{cp}}$ and $\mathrm{I_{gated}}$.

of the fixed-offset scheme, $\mathrm{Spur_{fixed}}$, for comparison. Its final form is expressed in

$$\frac{\mathrm{Spur_{gated}}}{\mathrm{Spur_{fixed}}} = \frac{\left\{\begin{array}{c}[I_1\sin 2\pi d_1 + I_2\sin(\phi+2\pi d_2) - I_2\sin\phi]^2 + \\ [I_1\cos 2\pi d_1 - I_1 + I_2\cos(\phi+2\pi d_2) - I_2\cos\phi]^2\end{array}\right\}}{[I_1\sin 2\pi d_1]^2 + [I_1\cos 2\pi d_1 - I_1]^2}. \quad (4)$$

Equation (4) indicates that the amount of spur improvement depends on the phase ϕ. By utilizing a gating clock with a proper phase, considerable spur improvement is achieved. For an effective offset of 10% and a 50% duty-cycle gated current (i.e., $\mathrm{d_1} = 0.1, \mathrm{d_2} = 0.5, \mathrm{I_2} = 0.2 \times \mathrm{I_1}$), the reference spurs can be improved by close to 9 dB.

IV. Fractional-N PLL Implementation

A. Proposed Fractional-N PLL Architecture

Fig. 9 depicts the block diagram of the 2.4-GHz $\Delta\Sigma$ fractional-N PLL, which incorporates the proposed circuit techniques: the dynamic current-matching CP and the gated-offset scheme. The 50% duty-cycle clock used to gate the offset current is derived from dividing the 40-MHz reference signal by 2. One of the four phases generated is selected to control the gated-offset current. The PFD operates at 20 MHz. In order to achieve the same effect of offsetting, the magnitude of the current in the gated scheme is twice of that in the fixed offset scheme (for a 50% gating clock). To avoid affecting the PLL settling behavior, the gated-offset technique may be enabled once the loop is phase locked. The locking condition can be detected by a PLL lock indicator.

B. Multi-Modulus Divider and Delta-Sigma Modulator

Fig. 10(a) shows the MMD architecture, which consists of seven asynchronous divide-by-2/3 stages. It is based on the truly

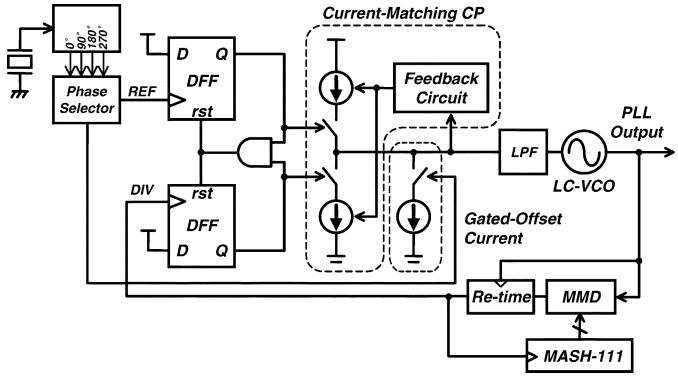

Fig. 9. Block diagram of the proposed $\Delta\Sigma$ fractional-N PLL.

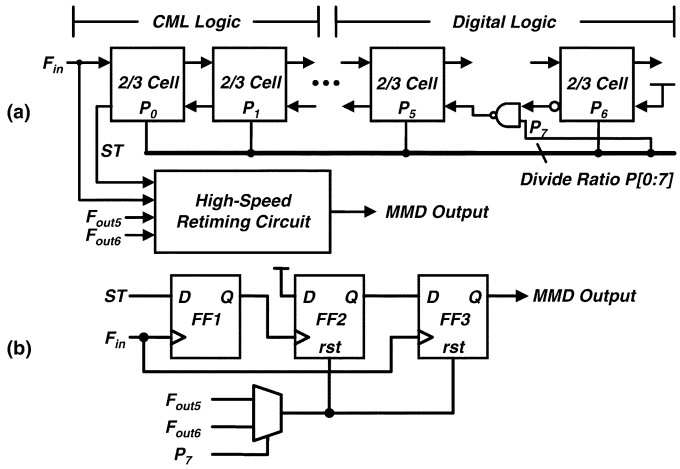

Fig. 10. (a) Block diagram of the multimodulus divider and (b) the high-speed retiming circuit.

modulus structure [13], [14]. The divide ratio ranges from 64 to 255. The high-speed portions (the first three divide-by-2/3 stages) of the MMD are implemented in current mode logic (CML), while the rest are designed in static CMOS logics for low-power and robust operation.

In the MMD, the jitter introduced in each stage will accumulate and raise the output phase noise. In addition, the jitter degrades the system linearity and causes further noise folding. To address this issue, a high-speed retiming scheme is developed to resynchronize the MMD output with the VCO signal. To ensure a robust re-timing, it is important that the re-timing operation must be completed within one input signal period under all conditions. Here, observed that the strobe signal (ST) of the first divide-by-2/3 stage appears once every MMD output cycle; hence, it can be taken as the MMD output. Since this signal experiences short propagation delay from the MMD input, it is convenient to achieve a high-speed re-timing [7]. Fig. 10(b) shows the details of the high-speed retiming circuit. The output signal ST is first re-synchronized to the VCO by FF1. FF2 is added to ensure the strobe-based MMD output has sufficient pulsewidth to drive the following PFD circuit. The pulsewidth is controllable by either $\mathrm{F_{out5}}$ or $\mathrm{F_{out6}}$. Before the signal enters the PFD, FF3 performs a final retiming operation.

The MMD division ratio is controlled by the MASH-111 $\Delta\Sigma$ modulator. The MASH architecture is preferred in this imple-

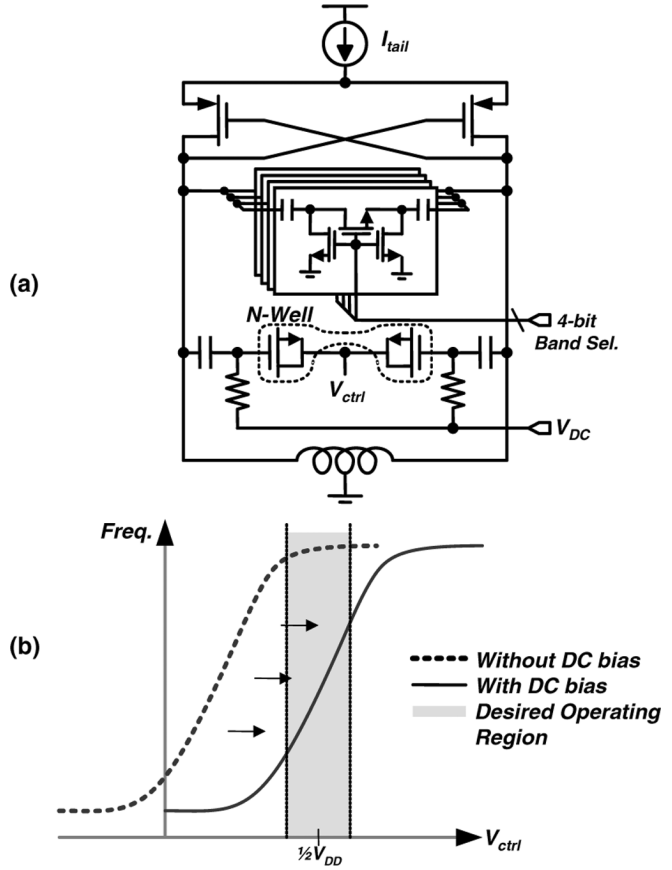

Fig. 11. (a) VCO schematic. (b) Shifting of the VCO tuning characteristic.

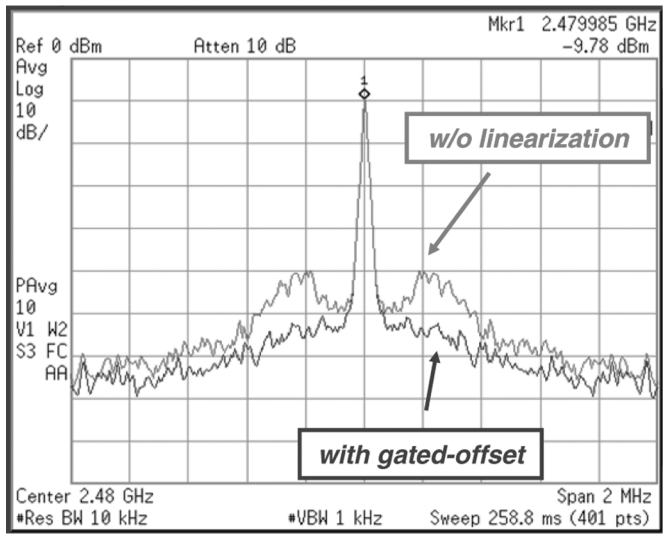

Fig. 12. Measured output spectra with and without applying the gated-offset linearization technique.

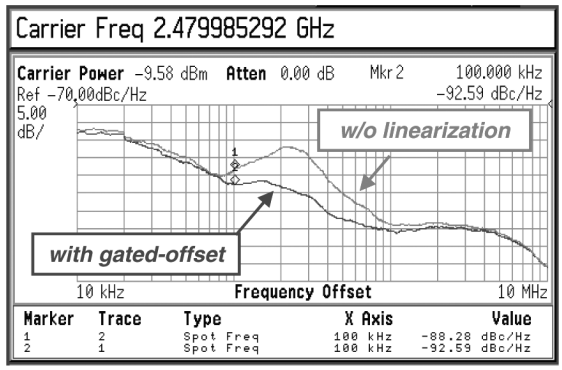

Fig. 13. Measured PLL phase noise with and without applying the gated-offset linearization technique.

mentation, for it is unconditionally stable, and it can accommodate a wide-range input. An on-chip third-order loop filter is employed to suppress the high-pass-shaped modulation noise.

C. Voltage-Controlled Oscillator

Fig. 11(a) depicts the VCO circuit. The *LC*-VCO employs a cross-coupled pMOS pair with a pMOS current source, which resides in an N-well. This topology has the benefit of less substrate noise coupling, which is an important attribute in a noisy SoC environment.

The varactor in the *LC*-tank consists of both discrete and continuous tuning capacitors. A 4-b switched-capacitor array topology is adopted to ensure the VCO turning range can span over the 2.4-GHz band across process-voltage-temperature (PVT) variations, while keeping the $K_{\rm VCO}$ small. A small $K_{\rm VCO}$ is advantageous in achieving low phase noise and decreasing reference spurs. In addition, it reduces the influence of the supply and substrate noise coupling which can result in the AM-to-PM noise modulation [12]. The MOS varactor adopts the accumulation-depletion structure. To fully utilize the capacitance tuning range over a limited $\rm V_{ctrl}$ voltage range, the varactor is biased at a more linear region by applying a DC voltage ($\rm V_{DC} = 1/2\ V_{DD}$) to shift its operating point, as illustrated in Fig. 11(b).

V. Experimental Results

The fully integrated 2.4-GHz $\Delta\Sigma$ fractional-N PLL with the proposed techniques has been implemented in the TSMC 0.18-μm CMOS process. Fig. 12 shows the PLL output spectra measured at 2.48 GHz. Without applying the linearization technique, the close-in phase noise and fractional spurs are rather poor. When a 20% offset current gated by a 50% duty-cycle clock (the amount of effective offset is 10%) is applied to the CP output (see Fig. 9), it can be clearly seen that the PLL output spectral purity is greatly improved. Fig. 13 shows the corresponding phase noise measurements, with and without applying the linearization technique. When the gated-offset method is activated, a significant improvement of phase noise is observed. These measurement results validate the effectiveness of the proposed gated-offset linearization technique.

The amount of the applied offset current will influence the PLL phase-noise performance. Fig. 14 shows the plot of the offset current versus the spot phase noise taken at 100-kHz offset frequency (measured at 2.48 GHz). When the offset current is activated and starts to increase from a small value, the phase noise reduces drastically since the PLL linearity improves considerably. However, if the applied current is further increased beyond an optimal value, the phase noise begins to degrade. This is attributed to the fact that the CP is now turned on for a longer

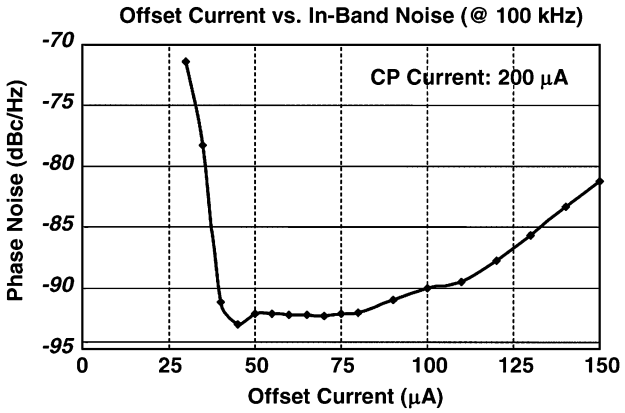

Fig. 14. Measured spot phase noise at 100 kHz versus gated-offset current.

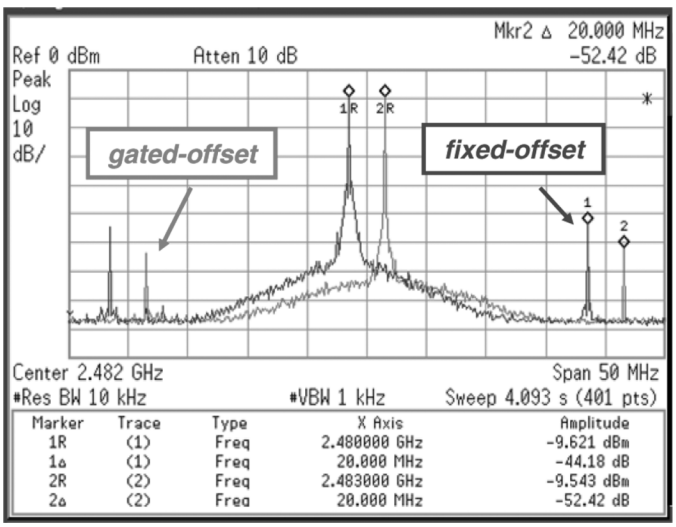

Fig. 15. PLL spectral comparison between the fixed-offset and the proposed gated-offset linearization techniques. The gated-offset method achieves lower reference spurs.

time to balance the offset current, hence injecting more noise to the loop.

The advantage of the proposed gated-offset method over the simple fixed-offset approach is demonstrated in Fig. 15. When the gating clock with a proper phase is activated, the reference spurs are lowered by about 8.2 dB (from −44.18 to −52.42 dBc). This is close to the maximum value (9 dB) predicted from (4). Here, the amount of effective offset is 10%. In fact, the recorded results agree well with those predicted by the theory and the circuit simulation.

In this implementation, the principle of gated-offset operation is demonstrated with a simple clock generation circuit. The reference spur can be further improved by heavier loop filtering or incorporating a more complex clocking scheme (with a tighter duty-cycle control) to adjust the offset current. Alternatively, the reference spur magnitude can be lowered by reducing the gated-offset current [as conceptually illustrated in Fig. 7(b)]. However, this is at the cost of possibly worsening the system nonlinearity.

Fig. 16 plots the normalized reference spur magnitude versus the gated-offset pulse position (phase ϕ). The data are gathered from calculation [from (4)], circuit simulation, and measurement, and show good agreement among them. There are only four measured data points, since only four different phases are available to control the offset current. Note that the

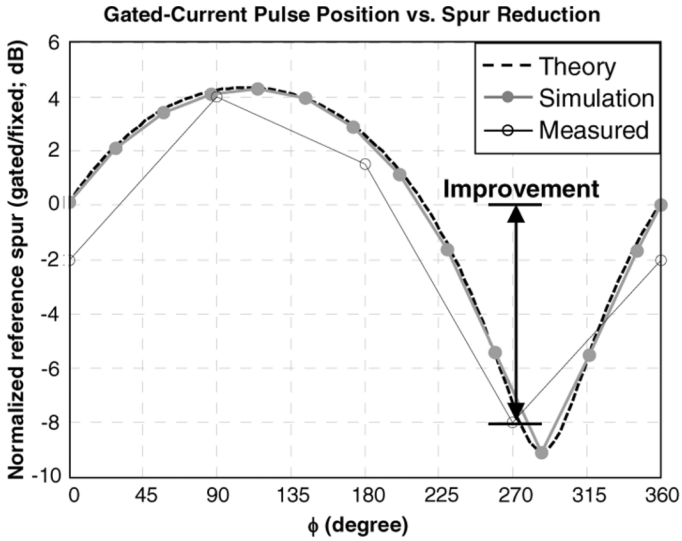

Fig. 16. Change of spur magnitude when the gated-offset technique is applied (normalized to the fixed-offset scheme).

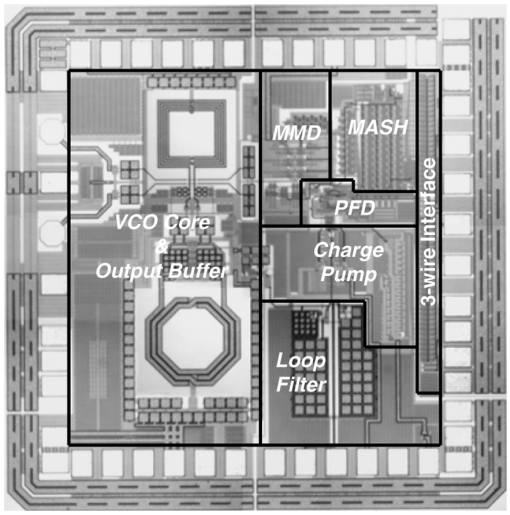

Fig. 17. Chip photograph.

TABLE I
PERFORMANCE SUMMARY

Process	TSMC 0.18-μm 1P6M CMOS
Power Supply	1.8 V
Operating Frequency	2.2 GHz ~ 2.6 GHz
VCO Phase Noise	-92.6 dBc/Hz @ 100 kHz -105.5 dBc/Hz @ 1 MHz
Frequency Resolution	4.88 kHz (12-bit ΔΣ-Modulator)
Loop Bandwidth	270 kHz
Reference Spur	< -52 dBc
Fractional Spur	< -51 dBc
Power Consumption	22 mW
Chip Area (Core Area)	1.5 mm x 1.5 mm (1.1 mm x 1.1 mm)

timing (phase) accuracy requirement of the gating clock is not demanding. As shown in Fig. 16, an 8° phase error causes only 1-dB spur degradation in the worst case.

The complete $\Delta\Sigma$ fractional-N PLL draws 12 mA from a 1.8-V supply voltage. Among which, the VCO and VCO buffer draw 5.4 mA and the divider chain with retiming dissipates 4.8 mA. Including the ESD-protection pads, this chip occupied an area of 1.5 mm × 1.5 mm, where the core area is 1.1 mm × 1.1 mm. The chip photograph is shown in Fig. 17. Finally, the experimental results are summarized in Table I.

VI. Discussion and Conclusion

The performance of a $\Delta\Sigma$ fractional-N PLL is significantly influenced by the circuit nonlinearity. Nonlinearity results in the noise-folding phenomenon which can seriously degrade the PLL in-band phase noise and raise fractional spurs. To tackle this issue, linearization techniques are proposed in this paper, with an emphasis on addressing the nonlinearity attributed to the PFD/CP.

Offsetting the PFD/CP operation to a more linear region of its transfer characteristic is an effective mean to reduce the associated nonlinearity. The shifting operation can be accomplished by introducing uneven delays to the PFD up/down reset paths [8] or incorporating an offset current in the CP design [6], [7], [15]. In [7], a constant offset current is injected to the loop filter for this purpose. This simple implementation proves sufficient to linearize the circuits and suppress the noise-folding problem with little additional hardware. The major drawback of this approach is that the PLL reference spurs are significantly raised. In [6] and [15], the same offset principle is realized by applying pulsed currents instead of a constant dc current. With a clever pulse timing control, this approach minimizes the disturbance on the loop filter from the injected current pulses, solving the reference spur issue. However, the design complexity is noticeably higher in order to generate accurate current pulses.

The gated-offset technique described in the paper presents a compromise between the tradeoffs of design complexity and level of reference spurs. Compared with [7], the reference spur is improved in this work with just an addition of a simple gating circuit. On the other hand, the technique in [6] achieves the best reference spur suppression, but at the cost of more complicated design, which increases chip area and power consumption.

In addition to the gated-offset linearization technique, the dynamic current-matching CP is also presented. This CP circuit is designed to minimize the up/down current mismatch without employing large current source transistors; hence also improves the CP transient performance (e.g., less clock feedthrough and charge injection). These techniques are incorporated in the design of a 2.4-GHz $\Delta\Sigma$ fractional-N PLL. The experimental results demonstrate the proposed design concepts and validate the effectiveness of the proposed methods.

Acknowledgment

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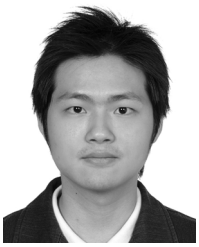
Tsung-Hsien Lin (M'03) received the B.S. degree in electronics engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 1991, and M.S. and Ph.D. degrees in electrical engineering from University of California, Los Angeles, in 1997 and 2001, respectively.

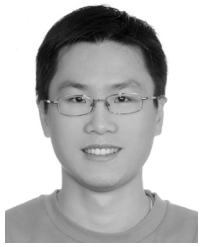
He joined Broadcom Corporation in March 2000 as a Senior Staff Scientist. While at Broadcom, he was involved in analog/RF/mixed-signal IC designs and participated in wireless transceiver developments for IEEE 802.11 a/b/g, Bluetooth, etc. He joined the Graduate Institute of Electronics Engineering and the Department of Electrical Engineering, National Taiwan University, Taipei, in 2004, where he is now an Associate Professor. His research interests are in the design of communication circuits and transducer interface circuits.

Dr. Lin was the recipient of the Best Presentation Award at the 2007 VLSI-DAT Symposium. His teaching efforts were recognized twice by the Teaching Excellence Award from National Taiwan University in 2007 and 2008. He has served in the A-SSCC Technical Program Committee since 2005. He also served as the Secretary of IEEE Solid-State Circuits Society Taipei Chapter from 2004 to 2008.



Ching-Lung Ti received the B.S. degree in electrical engineering from National Cheng-Kung University, Tainan, Taiwan, in 2004 and the M.S. degree from the Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, in 2007.

In 2007, he joined MStar semiconductor, Hsinchu, Taiwan, where he is currently working on analog and mixed-signal circuit design for LCD applications and focuses on high-speed and low-jitter DLL/PLL circuits for serial interfaces such as LVDS, DVI/HDMI, and low-noise ADC clock generators.



Yao-Hong Liu (M'04) was born in Hsinchu, Taiwan, in 1977. He received the M.S. degree in communication engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 2002. He is currently working toward the Ph.D. degree at the Graduate Institute of Electronics Engineering, National Taiwan University, Taipei.

His Ph.D. research is on the topic of low-power radio design for implantable bio-medical systems. From 2002 to 2003, he was with Terax Communication, Taiwan, as a Circuit Design Engineer and worked on CMOS RFIC for Bluetooth. Between 2003 and 2006, he was with VIA technology, Taiwan, as a Senior Analog/RF IC Design Engineer, where he has involved in GSM and WCDMA transceiver designs. In 2006, he joined Mobile Devices, Taipei, as a Staff Analog/RF Circuit Design Engineer and worked on the projects of PHS, WiFi, and WiMAX. His research interests include analog/RF and mixed-signal circuits for wireless communications and biomedical applications.