A 2.7 mW, 90.3 dB DR Continuous-Time Quadrature Bandpass Sigma-Delta Modulator for GSM/EDGE Low-IF Receiver in 0.25 μm CMOS

Song-Bok Kim, Stefan Joeres, Ralf Wunderlich, and Stefan Heinen, *Fellow, IEEE*

***Abstract*—Quadrature bandpass ΣΔ modulators based on polyphase filters are suited for analog-to-digital conversion in GSM/EDGE low-IF receivers. This paper presents a continuous-time quadrature bandpass sigma-delta (ΣΔ) modulator with a *chain of integrators with weighted capacitive feedforward summation* (CICFF) topology—which is a desirable solution for implementation in low power applications. A new compensation scheme for the polyphase filter is proposed. The summation of feedforward signals is implemented by weighted capacitors, without the necessity of any additional active components. The effectiveness of the proposed architecture is proved on a test chip which was designed in a standard 0.25 μm CMOS technology. The designed ΣΔ modulator has a power consumption of 2.7 mW at 1.8 V supply voltage, a dynamic range of 90.3 dB and a peak SNDR of 86.8 dB. The chip area is 0.5×1.4 mm^2 including pads.**

***Index Terms*—Analog-to-digital conversion, capacitive feedforward summation, CICFF, CIFF, complex filter, continuous-time circuit, polyphase filter, quadrature bandpass sigma-delta modulator.**

I. Introduction

CONTINUOUS-TIME (CT) ΣΔ modulators have become very popular in telecommunication applications over the last years, mainly due to some significant advantages over discrete-time implementations. A quadrature bandpass ΣΔ modulator as shown in Fig. 1, based on a polyphase filter is well suited for the use in low-IF receivers [1]–[3]. They directly perform the analog-to-digital conversion of quadrature analog I/Q signals within the signal bandwidth around the intermediate frequency (IF) and therefore reduce the problem of 1/f noise and DC offsets. In this case, a lower sampling frequency and a lower ΣΔ modulator order can be implemented resulting in a lower power consumption and a smaller chip area for the analog part. Hence, CT quadrature bandpass ΣΔ modulators have become state-of-the-art in GSM cellular phone architectures [3].

In recent years, several successful implementations of quadrature bandpass ΣΔ modulators have been presented [4]–[6]. Quadrature bandpass ΣΔ modulators with switched-capacitor (SC) architecture [7] have a sampled processing at their modulator inputs. To avoid alias effect, they essentially need anti-aliasing filters between the mixers and modulator inputs. In quadrature bandpass ΣΔ modulators with continuous-time architecture, the signals are sampled by quantizers inside the modulator and the CT loop filters act as anti-aliasing filter, so no additional filter is necessary.

CT quadrature bandpass ΣΔ modulators are implemented by replacing the low-pass filter of a low-pass ΣΔ modulator with the polyphase filter [8]–[10]. These polyphase filters can be obtained by cross-coupling the inputs and outputs of two low-pass integrators for the analog I/Q paths, shifting the filter characteristics from DC to intermediate frequency.

In the design of analog-to-digital converters for GSM cellular phones, the demand for low power and low voltage is extremely critical. The feedforward topology with capacitive summation is a desirable solution [11], [12]. But, the method based on two cross-coupled low-pass integrators for polyphase filter, causes an asymmetry in response of magnitude around intermediate frequency and an instability of the modulator, because the zeros by capacitive summation are still placed around DC.

In this paper, in order to implement in low power application, CT quadrature bandpass ΣΔ modulator with capacitive feedforward summation for GSM/EDGE low-IF receiver is presented. Therefore, in Section II, an additional compensation cross-coupling for the polyphase filter with capacitive feedforward summation is proposed to provide a symmetric transfer function and stability of the modulator with capacitive feedforward summation. Section III describes the architecture of a third-order CT quadrature bandpass ΣΔ modulator used in the implementation of a low-IF GSM/EDGE receiver. In Section IV, the modulator non-idealities are considered, and schematic for the proposed modulator is printed in Section V. The measurement results of test chip which was designed in a 0.25 μm CMOS technology are introduced in Section VI, and finally Section VII gives a conclusion.

II. Architecture Overview

A polyphase filter for quadrature bandpass ΣΔ modulators can be obtained by translating a low-pass filter transfer function from DC to the desired intermediate frequency ($w_c = 2\pi f_c$).

$$H_{PPF}(jw) = H_{LP}(jw - jw_c). \tag{1}$$

This translation moves all poles and zeros in the s-plane to positions centered around the intermediate frequency. Therefore, in an ideal case, the characteristics of the low-pass ΣΔ modulators are preserved in quadrature bandpass ΣΔ modulators as well, except for different center frequency. This implies that

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The authors are with the Chair of Integrated Analog Circuits, RWTH Aachen University, D-52074 Aachen, Germany (e-mail: skim@ias.rwth-aachen.de, ralf.wunderlich@ias.rwth-aachen.de; mailbox@ias.rwth-aachen.de).

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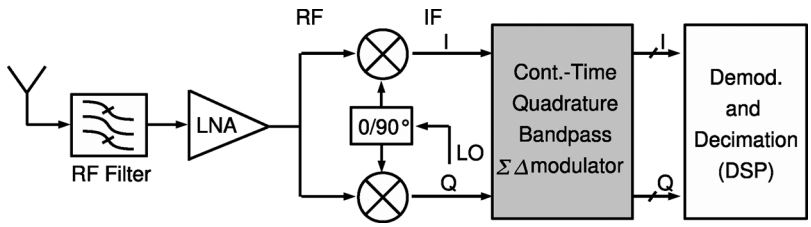

Fig. 1. CT quadrature bandpass $\Sigma\Delta$ modulator in low-IF receivers.

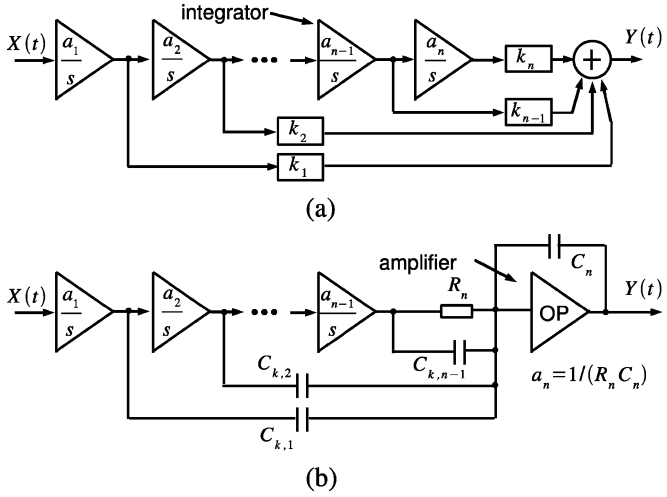

Fig. 2. Low-pass filters with (a) CIFF and (b) CICFF topology.

the selection of a low-pass filter is a main key to the design of quadrature bandpass $\Sigma\Delta$ modulators.

A. Low-Pass Filter With CICFF Toplogy

A single-loop topology is mainly used for quadrature bandpass $\Sigma\Delta$ modulators. Two main single-loop topologies exist: the *chain of integrators with distributed feedback*(CIFB) and the *chain of integrators with weighted feedforward summation* (CIFF) [13], [14].

The integrator outputs in the CIFF topology have a reduced output swing in comparison to CIFB and are therefore more desirable in low voltage application. Although the CIFF topology has several benefits, it demands extra current for the feedforward summation as shown in Fig. 2(a). This can be overcome by a capacitive feedforward summation architecture as shown in Fig. 2(b), which is a good solution for the targeted low power applications [12], [13]. The main advantage of this architecture is the elimination of the feedforward summation amplifier at the output of the filter and hence no additional power in the feedforward branches is consumed. In contrast to the feedforward summation architecture with a transconductance amplifier [3], [4], the feedforward coefficients are inherently linear. The feedforward coefficients are determined by the ratio between the feedforward capacitors and the integrating capacitor of the last integrator as shown in

$$k_i = C_{k,i}/C_n \,(i = 1 : (n-1)), \quad k_n = 1. \tag{2}$$

Due to these benefits, the *chain of integrators with weighted capacitive feedforward summation* (CICFF) topology, is best suited for the implementation of polyphase filters in low voltage, low power.

Design methods for CIFF and CIFB topologies using cross-coupled low-pass filter are commonly available. Due to additional zeros which are introduced by feedforward capacitors in CICFF topology, these are not applicable here. The following subsection proposes an implementation of a polyphase filter derived from a low-pass filter with CICFF topology.

B. Polyphase Filter With CICFF Topology

Low-pass filters with CICFF topology have a capacitive summation in the last stage integrator. Except for the last integrator, the integrators of (n-1) stages in front of last integrator are the same as that of CIFF topology. The cascade combination of (n-1) integrators and the outputs of (n-1) integrators are also identical to CIFF topology as shown in Fig. 2. Therefore, using conventional cross-coupling resistors [8]–[10], the outputs of (n-1) integrators can be translated from DC to center frequency. The cross-coupling resistors are defined as follows:

$$R_{C,i} = \frac{1}{w_c C_i} \quad (i = 1 : (n-1)), \tag{3}$$

where C_i is a integrating capacitor of a ith integrator. The output $(y_i = y_{I,i} + jy_{Q,i})$ of the ith complex integrator is

$$y_i = \frac{a_i}{s - jw_c} y_{i-1} \quad (i = 1 : (n-1)). \tag{4}$$

Hence, all inputs fed into the last stage are shifted by jw_c in low-pass integrator transfer functions. In the last stage, when using conventional cross-coupling [9], all poles are moved around jw_c, but the zeros introduced by capacitive summation are still placed around DC. The total output $\acute{Y}$ is

$$\acute{Y} = \frac{a_n}{s - jw_c} y_{n-1} + \left(\frac{s}{s - jw_c}\right) \sum_{i=1}^{n-1} k_i y_i. \tag{5}$$

The zeros introduced by capacitive summation causes an asymmetry around center frequency in an equivalent noise shaping transfer function (NTF) in the z-domain as well as in polyphase filter transfer function. Furthermore, the modulator becomes more sensitive to instability.

The last stage with the summation node should take additional compensation cross-couplings in order to move the zeros due to the capacitive summation, as well as the conventional cross-couplings in order to move the pole of the integrators to jw_c. The compensation cross-couplings can be implemented by standard resistors $R_{S,i}$, which are determined as follows:

$$R_{S,i} = R_{C,n}/k_i \quad (i = 1 : (n-1)). \tag{6}$$

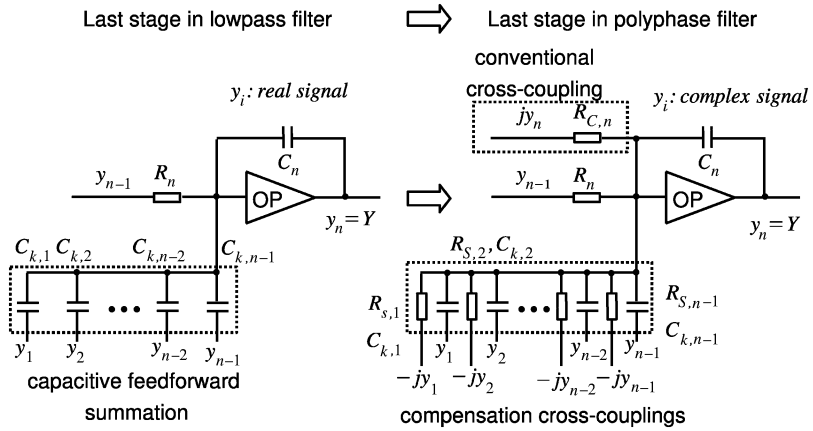

Fig. 3. Last stage of polyphase filter with capacitive summation.

It implies that $w_c = 1/(R_{S,i}C_{k,i})$ from (2) and the zeros introduced by the capacitive summation are moved by jw_c in the s-plane. Fig. 3 shows the last stage for polyphase filter with CICFF topology. Here, term jy_i means a multiplication with complex constant j and a swapping of real and imaginary part of ith quadrature complex integrator output y_i (cross-coupling). Therefore the total output Y is

$$Y = \frac{a_n}{s - jw_c} y_{n-1} + \sum_{i=1}^{n-1} k_i y_i. \tag{7}$$

The above equation is identical to that of CIFF topology. Note that the output of the polyphase filter with local feedback loop is slightly different to CIFF topology [6], but all poles and zeros are moved to jw_c. The polyphase filter with the capacitive feedforward summation was proposed in [5]. But, the summation uses an additional amplifier and therefore more power is needed.

III. CT Quadrature Bandpass $\Sigma\Delta$ Modulator for GSM/EDGE

A 3rd-order polyphase filter for CT quadrature bandpass $\Sigma\Delta$ modulator for GSM/EDGE low-IF receiver was selected. From demands of the receiver system, the center frequency was set to $f_c = 130\,\text{kHz}$, with a bandwidth of $f_B = 200\,\text{kHz}$ and a sample frequency of $f_s = 26\,\text{MHz}$. Fig. 4 shows the polyphase filter with CICFF topology, designed for GSM/EDGE. The polyphase filter includes a local feedback loop for an optimized placement of the zeros in the NTF. The optimized placement can minimize the shaped noise spectrum in passband [13]. The summation nodes for the output of second quadrature complex integrator are moved to front of the local feedback loop, in order to avoid resonance damping of the local feedback loop [12]. Note that if the last integrator is not within the local feedback loop, the capacitive summation for all signals should be implemented at the last integrator. The polyphase filter transfer function is

$$H_{PPF}(s) = \frac{k_1 a_1 (s - jw_c)^2 + k_2 a_1 a_2 (s - jw_c) + a_1 a_2 a_3}{(s - jw_c)\left[(s - jw_c)^2 + a_2 a_3 b_f\right]} \tag{8}$$

where $a_i = 1/(R_i C_i)$, $b_f = R_2/R_f$ and $w_c = 1/(R_{C,i}C_i) = 1/(R_{S,i}C_{k,i})$ in all stages. As shown in the above equation, the feedforward coefficients k_i do not affect the placement of poles in the polyphase filter, therefore there is no change in the optimized placement of zeros in the equivalent NTF. The feedforward coefficients only affect the stability of the modulator, because the poles of the NTF depend on the feedforward coefficients and the scale coefficients of the integrators.

TABLE I
Modulator Parameter

coefficients	values
$a_1, \quad a_2 = a_3$	$0.9136/T_s, \quad 0.1142/T_s$
$b_f, \quad k_1, \quad k_2$	$0.04, \quad 0.5, \quad 1.0$

The polyphase filter transfer function is shown in Fig. 5. The coefficients of the polyphase filter are optimized for a maximum open-loop phase margin, as this improves the modulator stability, allowing a relaxation of the delay requirements on the analogue circuits. The out-of-band gain of the NTF is kept below 1.5 for stability and the polyphase filter gain at in-band is selected as 70 dB to meet the required SNR. The modulator coefficients used in this design are shown in Table I. Fig. 6 shows the CT quadrature bandpass $\Sigma\Delta$ modulator for GSM/EDGE low-IF receiver. It has the proposed polyphase filter, single-bit quantizers at I/Q feedforward paths and DACs at I/Q feedback paths.

A method to find a matched $H_{PPF}(s)$ that implements the NTF designed in the z-domain is usually used for the design of a CT $\Sigma\Delta$ modulator, by means of the impulse-invariant transformation [15] as shown in following equation which is extended to the quadrature bandpass modulator.

$$Z^{-1}\left[\hat{H}_{PPF}(z)\right] = \left\{L^{-1}\left[DAC(s)H_{PPF}(s)\right]\right\}\Big|_{t=nT_s} \tag{9}$$

where $DAC(s)$[1] is the Laplace transformation of the feedback DAC pulse $DAC(t)$ and $\hat{H}_{PPF}(z)$ is the DT loop filter. Here, a non-return-to-zero (NRZ) pulse is chosen for the feedback DAC, because it has less influence on the clock jitter than other

[1]For a low f_c, NTF and DT polyphase filter $\hat{H}_{PPF}(z)$ obtained by a feedback DAC pulse centered around DC is fairly good, while for a higher f_c, a cross-coupling of the feedback DAC pulse is necessary for symmetric poles around f_c in the NTF and stability purposes [10].

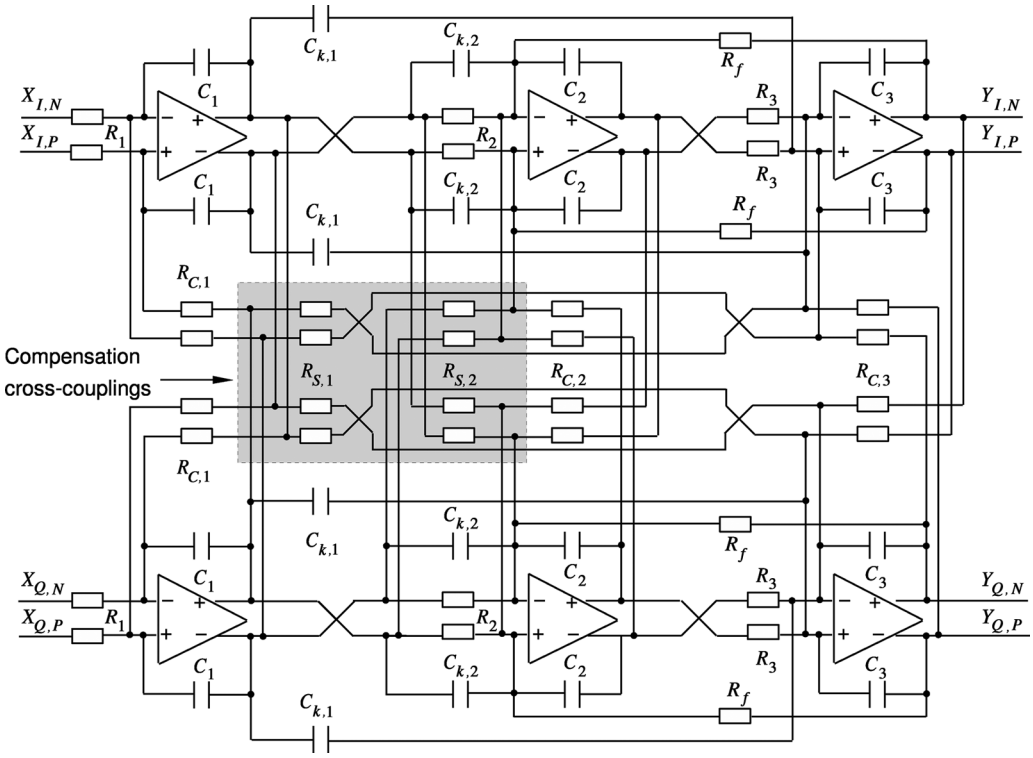

Fig. 4. Polyphase filter for GSM/EDGE.

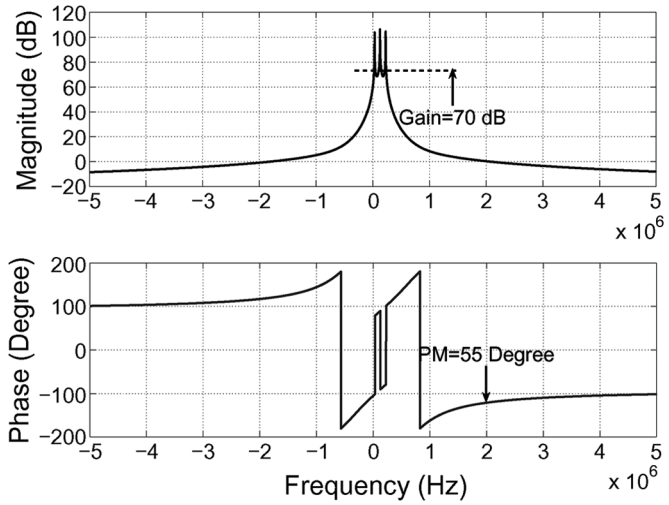

Fig. 5. Frequency response of the polyphase filter.

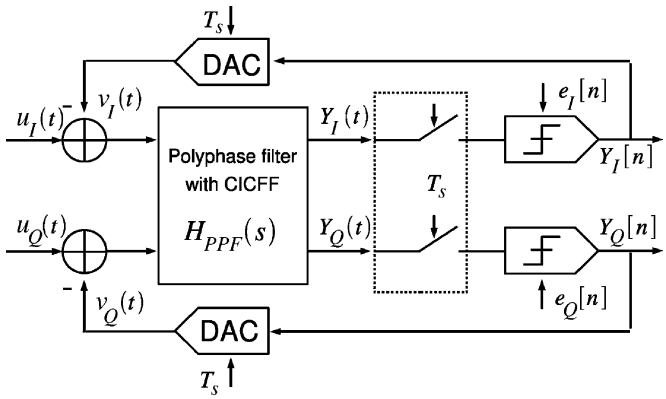

Fig. 6. CT quadrature bandpass $\Sigma\Delta$ modulator with CICFF topology.

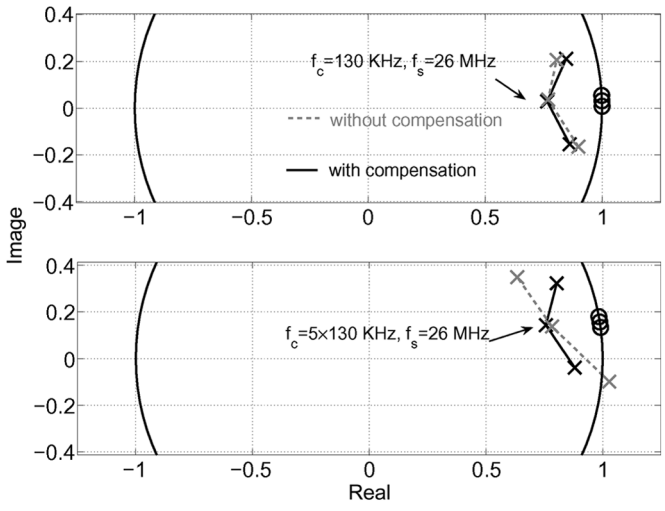

Fig. 7. Placement of the poles and zeros of NTF ("o": zero, "×": pole).

DAC analog pulses. In this design, the NTF is inversely implemented from the proposed polyphase filter and modulator parameters, and its behavior was checked by simulation in the z-domain. This method gives an easier feasibility of the optimized circuit design in CT domain, because it starts from the CT polyphase filter design. Furthermore, since the non-ideal effects in CT domain, such as finite GBW, DC gain of amplifiers and component mismatch, can be reflected in CT loop filter $H_{PPF}(s)$, this design technique might be more practical.

Fig. 7 shows the placement of the poles and zeros of the NTF equivalent from the polyphase filter, which is derived from (9) and is defined with complex coefficients. When using the proposed compensation cross-couplings, the NTF is symmetric around the center frequency. All poles and zeros are shifted by

$e^{jw_cT_s}$ toward the upper half of unit circle in the z-plane. Otherwise, without the compensation cross-couplings, the poles of the NTF are asymmetrically placed at the around $e^{jw_cT_s}$ and thus, the NTF is also asymmetric at the out-of-band. Furthermore, one pole is shifted toward the outside of the unit circle, increasing sensitivity to instability. It should be noted that without the proposed zero compensation for the capacitive feedforward coefficients, the higher the center frequency, the worse is the modulator stability, as shown in the bottom of Fig. 7. All zeros of the NTF that are spread inside the signal bandwidth maximally suppress the in-band noise around the center frequency.

IV. Modulator Nonidealities

In order to satisfy demands for GSM/EDGE applications, the ADC resolution should be in the range of 13–16 bit. In the ideal case, the peak SNDR of the proposed CT quadrature bandpass single-bit $\Sigma\Delta$ modulator is 105.8 dB at the the sampling clock of 26 MHz. Unfortunately, the SNDR of the modulator is reduced by the non-ideal effects, while causing instability.

A. Sensitivity to RC-Product Variation

In DT modulators implemented in SC technique, the integrator scales are computed by sampling clock and capacitor ratios, which are intrinsically precise [7]. In contrast, in CT $\Sigma\Delta$ modulators integrator scales are mapped into resistor-capacitor products, which largely vary over chip process and temperature. The process variations of the absolute component values of 10–20% might cause the possible variation of the RC-product to more than 35% [16]. The following equation shows a model for RC-integrator transfer function subject to a tolerance δ_{RC}.

$$INT_i(s) = \frac{1}{s \cdot R_iC_i(1+\delta_{RC})}. \tag{10}$$

The RC-product variation causes the deviation in the optimized zero and the targeted pole locations of the NTF as well as that from the center frequency. The equivalent NTF was simulated with different RC-tolerances δ_{RC}. It can be seen that the bandwidth as well as the center frequency of the modulator are severely varied as shown in Fig. 8. Here, all resistive and capactive ratios such as b_f, k_i were assumed to be preserved.

When $\delta_{RC} < 0$, the modulator becomes unstable due to an aggressive noise shaping, while increasing slightly the SNDR. When $\delta_{RC} > 0$, the degradation of the SNDR causes. For $\delta_{RC} = 0.35$, the SNDR loss is around 10 dB as shown in Fig. 9. Therefore, the RC-product variations should be suppressed or handled.

In additional, the quadrature bandpass $\Sigma\Delta$ modulators are susceptible to a mismatch between the circuit components in the I/Q paths [9], [17], which leads a severe decrease of the SNR. Since the subsequent stages in polyphase filter suppress the unwanted effects introduced by mismatch, the mismatch in I/Q paths closer to the quantizer is less problematic. The crosstalk depends mainly on the mismatch between the input resistors, and feedback DAC resistors in the first quadrature complex integrator. Therefore, it is necessary to take care in chip design for a good matching in the first stage of the modulator.

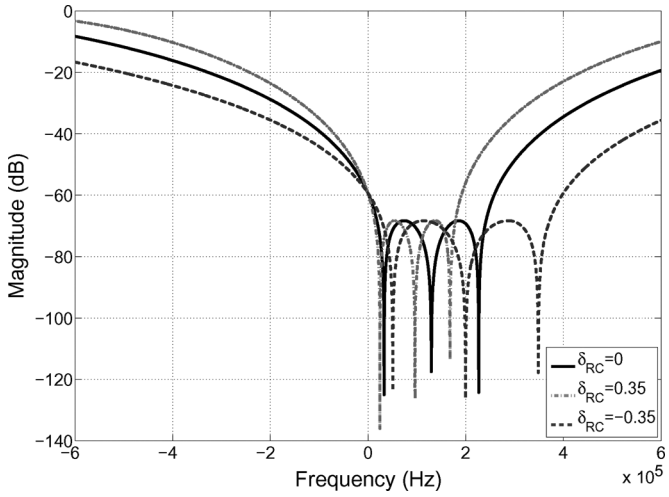

Fig. 8. The NTFs with different RC-product deviations.

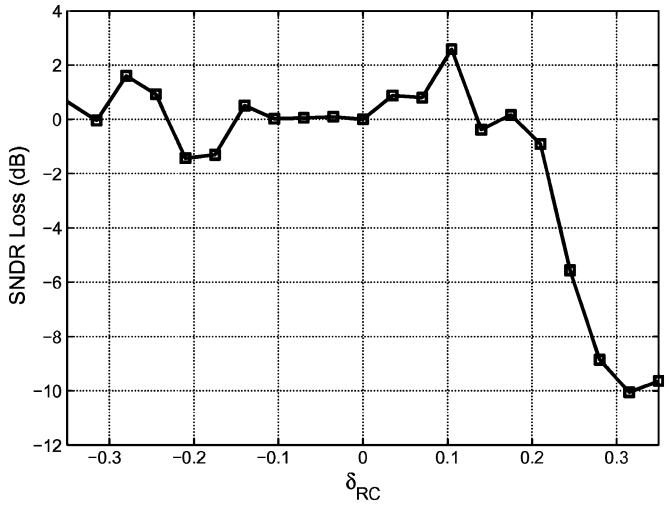

Fig. 9. SNDR loss vs. RC-product variation.

B. Excess Loop Delay

CT $\Sigma\Delta$ modulators seriously suffer from excess loop delay, which can not be seen in DT designs. It reduces the modulator performance such as the SNDR and stability [15], [18], [19].

Fig. 10 shows the placement of poles and zeros of the NTF with increasing excess loop delay, in our design based on Table I. The placement of the zeros of the NTF is not changed, but the placement of the poles has tendency toward outside of the unit circle with increasing excess loop, causing a loss of modulator stability. It can be also seen that an additional pole and zero are introduced by the excess loop delay, increasing the order of the denominator and the numerator of the NTF by one.

From simulation results, the designed CT quadrature bandpass $\Sigma\Delta$ modulator was shown that when modulator loop delay is less than 50% full sample period, the SNDR loss is less than 6 dB (Fig. 11), permiting no using an additional compensation scheme to reduce the effect of excess loop delay. The simulation was done with NRZ analog feedback DAC pulse in I/Q paths and -3 dBFS input level.

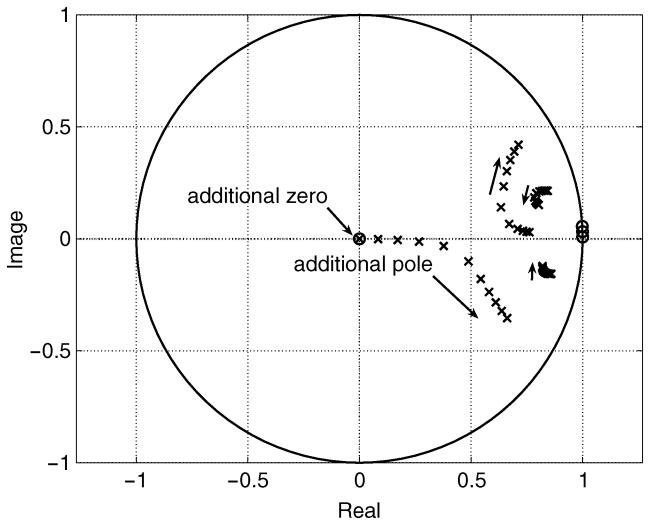

Fig. 10. The placement of poles and zeros vs. excess loop delay. The arrow denotes the increasing direction of excess loop delay (the step size 0.1 T_s).

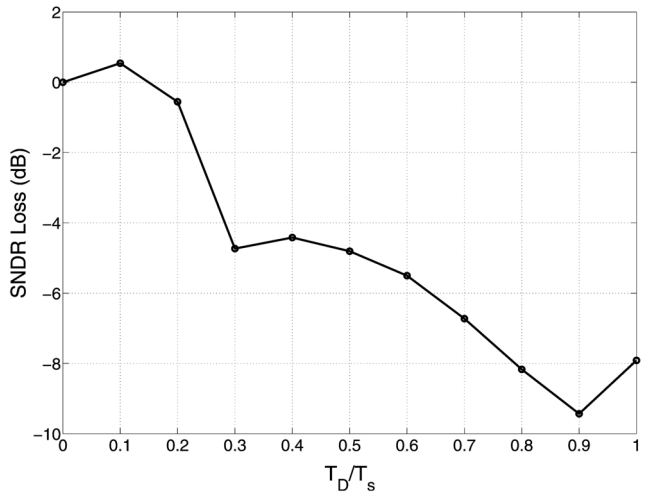

Fig. 11. SNDR loss vs. excess loop delay.

C. Clock Jitter

The performance of CT $\Sigma\Delta$ modulators is limited by the sampling clock jitter [20]–[22]. The clock jitter is a statistical variation of the clock edge, which depends on the clock source and chip design. The noise introduced by clock jitter increases the in-band noise power, and therefore decreases the SNR.

The noise spectral density by clock jitter in CT quadrature bandpass $\Sigma\Delta$ modulators with NRZ DAC pulse is derived by the same manner as in [22]

$$P_n = \left(\frac{1}{OSR}\right)\left(\frac{\sigma_J}{T_s}\right)^2 \left(P_{\delta y_I} + P_{\delta y_Q}\right) \tag{11}$$

where σ_J is the variance of the DAC clock uncertainty $\Delta T_J[n]$, and $P_{\delta y_I}$ and $P_{\delta y_I}$ are the power of $\delta y_I = y_I[n] - y_I[n-1]$ and $\delta y_Q = y_Q[n] - y_Q[n-1]$ in the quantizer outputs. The error sequences $\delta y_I[n]$ and $\delta y_Q[n]$ which take the values of ± 2 and 0 for a modulator with ± 1 outputs, are proportional to $\Delta y^2 = (y[n] - y[n-1])^2 = 4$ and the number of bit transitions of quantizer outputs in I/Q paths. The number of transitions is related to the input signal and especially the modulator design. An optimized design for reducing the number of transitions might be found by a choosing NTF [23]. In our consideration, they are taken as $\delta y_I[n] = \delta y_Q[n] = 2$. Therefore, the SNR by clock jitter in CT quadrature bandpass $\Sigma\Delta$ modulators with NRZ DAC pules is

$$SNR_{J,NRZ} = 10log_{10}\left(\frac{OSR \cdot V_{in}^2}{4 \cdot \left(\frac{\sigma_J}{T_s}\right)^2}\right) \tag{12}$$

where V_{in} is the amplitude of the input signal. Its power is twice as large as that of the low-pass modulator, due to the summation of real and imaginary powers of a complex signal. In this design, the variance of the DAC clock uncertainty should be less than 5 ps at sampling clock of 26 MHz.

D. Finite Gain-Bandwidth

When the unity gain-bandwidth (GBW) of the amplifers used in the quadrature complex integrators is finite, the performance of CT quadrature bandpass $\Sigma\Delta$ modulators is reduced. The finite GBW causes a gain error and an additional second pole of the integrator in the CT low-pass $\Sigma\Delta$ modulators [24]. When the open-loop gain of the single-pole amplifier is

$$A(s) = \frac{A_{DC}}{s/w_p + 1}, \quad GBW = A_{DC} \cdot w_p(\text{rad/s}) \tag{13}$$

then, the transfer function of the quadrature complex integrator is

$$QINT_i(s) = \frac{a_i}{(s - jw_c) + (1/A_i(s)) \cdot (s + a_i + w_c)}. \tag{14}$$

Here, $A_i(s)$ and a_i are the open-loop gain of the amplifier and the scale value for the ith integrator in the cascaded quadrature complex integrators, respectively. The transfer function has a dominant pole close to jw_c and an additional (parasitic) pole in the s-plane. The parasitic pole is located in the left-half of the s-plane, within a limitation imposed by the permissible design parameters. The dominant pole might locate at the right-half plane, depending on the selection of the complex integrator parameters. This implies that the complex integrator might become unstable. In addition, the frequency shifting is deviated from the wanted center frequency. In this design, the stability of the quadrature complex integrators is guaranteed by selected modulator parameter and the deviation from the center frequency can be neglected.

For the CIFF topology, quadrature complex integrators of the polyphase filter are identical to above equation. On the other hand, for the CICFF topology, all the stages except for the last stage quadrature complex integrator are the same as above, but the last stage has a huge capacitive load and a resistive load at the input for the capacitive summation and its compensation. The sum of the feedforward coefficients is

$$M = 1 + \sum_{i=1}^{n-1} k_i. \tag{15}$$

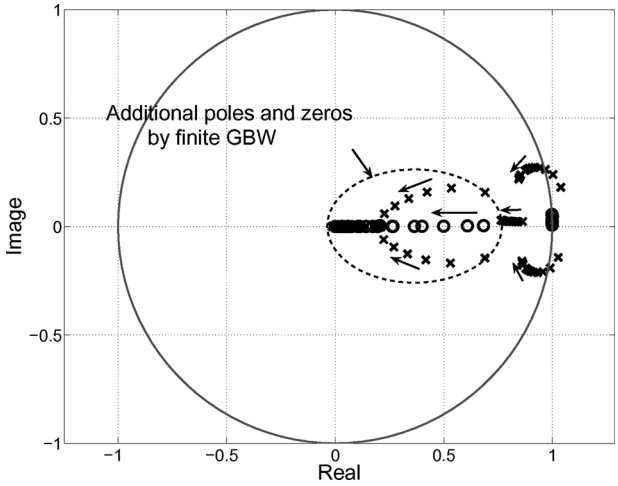

Fig. 12. Placement of poles and zeros when the finite GBW. The arrow denotes the increasing direction of finite GBW.

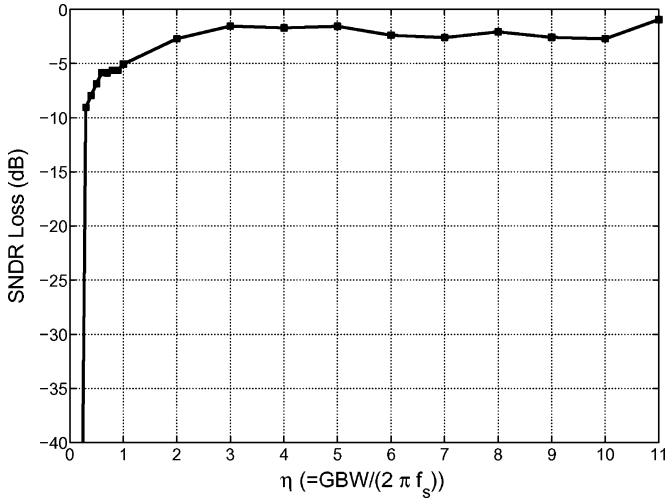

Fig. 13. SNDR loss vs. finite GBW.

Without local feedback loops, the final output of the last stage (Fig. 3) is

$$Y = \frac{a_n \cdot y_{n-1} + \sum_{i=1}^{n-1} k_i(s - jw_c) \cdot y_i}{(s - jw_c) + (1/A_n(s)) \cdot (M(s + w_c) + a_n)}. \quad (16)$$

As shown in above equation, the sum of the feedforward coefficients M affects the gain error of the polyphase filter and therefore increases the in-band level of the NTF. Obviously, when the feedforward capacitors, namely, the feedforward coefficients increase, the gain error also increases with reducing finite GBW of the last amplifier from (16). It implies that the GBW of the last amplifier should be greater than other stages. In general, the higher GBW, the greater the power consumption. Thus, it might have a loss of one of the benefits of the CICFF topology for low power. For a low center frequency, without an additional increment of the GBW of the amplifier of last stage, acceptable performances can be obtained.

All amplifiers in the designed modulator have identical structures and sizes—identical GBW and DC gain as shown in (14), because the modulator has capacitive summation nodes at the front of the second and third complex integrators. Fig. 12 shows the placement of poles and zeros of the equivalent NTF in the z-domain. It can be seen that additional poles and zeros are placed around the origin in the z-plane. With a lower GBW, some of the poles are placed outside of the unit circle and the additional poles and zeros also affect the modulator performance. Otherwise with a higher GBW, additional poles and zeros are canceled around the origin and the modulator might give an adequate performance. The SNDR loss by finite GBW is shown in Fig. 13. The severe degradation of the SNDR means the instability of the modulator. It can be shown that in our design consideration, the GBW should be at least as large as $2\pi f_s$.

Note that with a higher center frequency, the SNR degradation by finite GBW is much greater, because the cross-coupling resistors reduce and therefore it makes greater resistive load in the inputs of quadrature complex integrators. Hence, with a lower f_c, the CT quadrature bandpass $\Sigma\Delta$ modulator with CICFF topology are more suited in low power application.

V. Circuit Implementation

The top schematic for a chip of the GSM/EDGE data converter comprises the proposed 3rd-order polyphase filter with CICFF topology, dynamic latched comparators, the feedback NRZ feedback DAC pulse generators, and output buffers for measurement.

A. Integrator Design

Opamp-RC quadrature complex integrators are selected for the sake of linearity in low-voltage application. In the design of the integrator, the opamp is most important in order to satisfy desirable specifications, because its non-ideality by finite DC gain, GBW and input capacitance affect the modulator directly. In detail, the finite DC gain, GBW and input parasitic capacitance makes an error of the integrator gain and a parasitic pole.

To satisfy the bandwidth and the sampling clock demands, the opamps are designed with higher GBW than 150 MHz, with a phase margin of 56.5 degree under a load capacitance of 0.2 pF. The DC gain of the designed opamps is higher than 60 dB. In order to accommodate the low supply voltage, fully differential two stage Miller opamps were chosen, where a continuous-time common mode feedback circuit is attached as shown in Fig. 14. The simulated DC power consumption of the opamps is about 170 μA.

Because of a potentially large deviation of the RC-product due to process variations, quantized arrays of switchable capacitors are included. The capacitance value for the test chip is manually controlled by external pins until tolerance δ_{RC} of 40%.

B. Quantizer and Feedback DAC

In the real and imaginary paths, the output signals of the polyphase filter are sampled by a single-bit dynamic latched comparator with a master-slave D-flip-flop and converted to a digital signal. Fig. 15 shows the schematic of the quantizer. The simulated power consumption is less than 60 μW using a 1.8-V supply, with a sampling clock of 26 MHz. The master-slave D-flip-flop is implemented with NOR gates. The delay is 1.5 ns and DC offset is less than 3 mV.

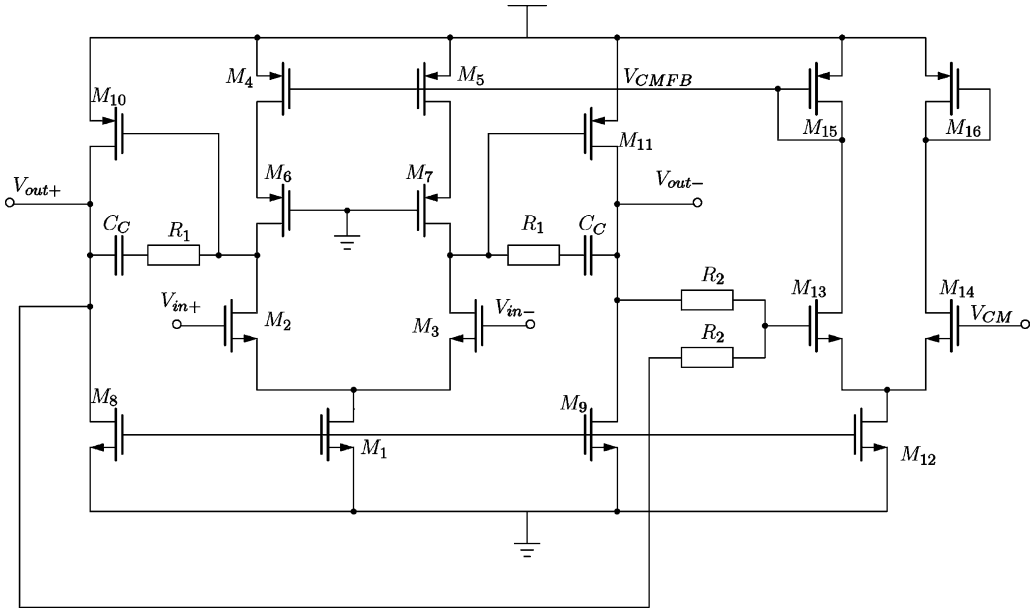

Fig. 14. Opamp with continuous-time CMFB.

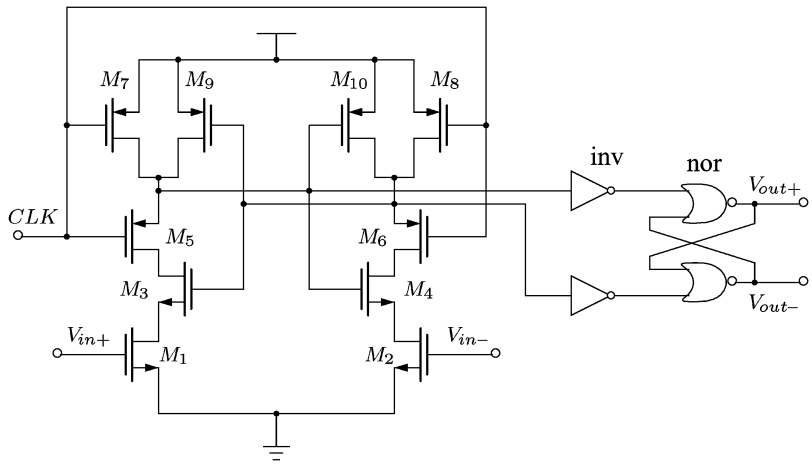

Fig. 15. Single-bit quantizer.

For the generation of the NRZ feedback DAC analog pulses, the CMOS transmission switches, which are connected to reference voltage sources, are directly driven by the buffered digital output stream of the quantizer.

VI. Measurement Results

Fig. 16 shows a chip micrograph of a designed 3nd-order CT quadrature bandpass $\Sigma\Delta$ modulator for GSM/EDGE low-IF receiver. The chip layout was designed in a 0.25 μm CMOS technology based on the following rules:

- All analog blocks were clearly separated from the digital blocks on chip in order to prevent a crosstalk from digital circuits.
- All cross-couplings of the quadrature complex integrators and all compensation cross-coupling resistors are symmetrically placed between real and imaginary channels in order to reduce the mismatch. Especially, the integrating, cross-coupling and feedback DAC resistors of the first quadrature complex integrator were carefully designed with larger width.

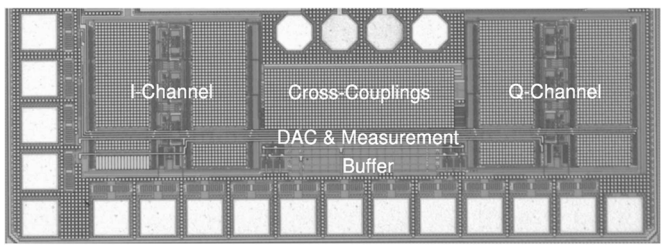

Fig. 16. Chip micrograph.

Fig. 17 shows the measurement setup used for the $\Sigma\Delta$ modulator chip. A signal generator provides the quadrature input signals with common mode DC level. These measurements were made at a sampling rate of 26 MSamples/s. The quadrature single-bit-streams are transformed to the frequency domain by an Fast Fourier Transformation (FFT) transformation in a signal analyzer. The shaped noise spectrum is observed. The bit-streams of both I/Q paths are fed through an oscilloscope to

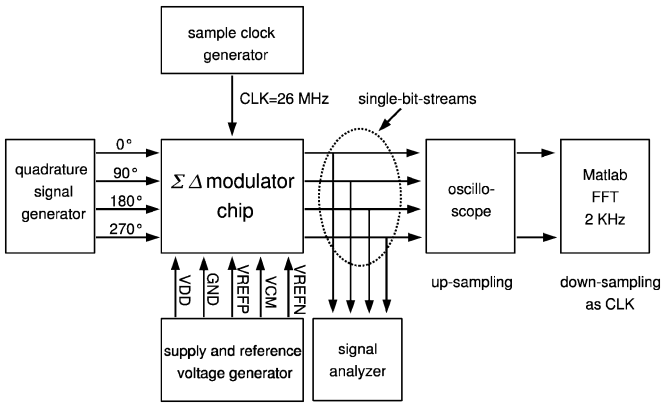

Fig. 17. Measurement setup.

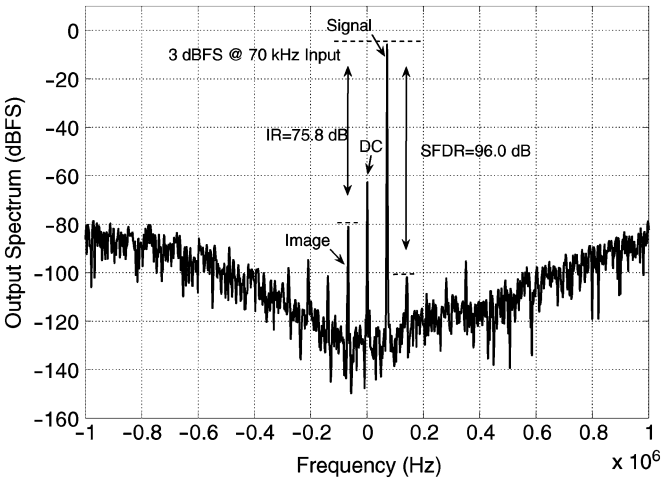

Fig. 18. Measured modulator output spectrum.

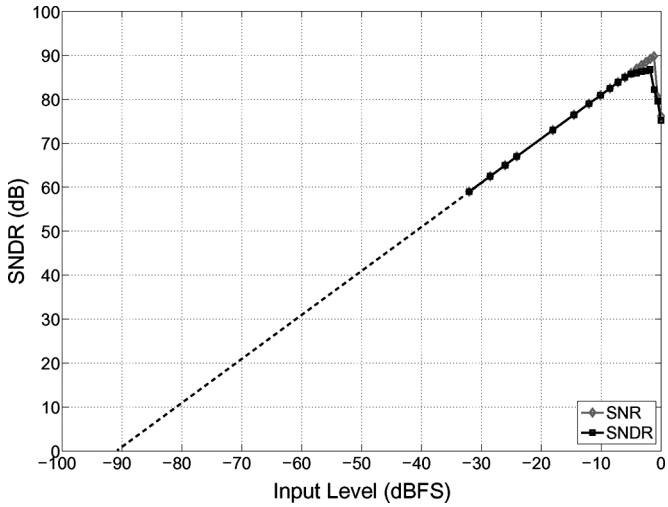

Fig. 19. SNDR versus input level.

TABLE II
IC PERFORMANCE

Parameters	Esfahani'03[3]	This work
Input IF/Bandwidth	-100 KHz/270 KHz	130 KHz/200 KHz
Peak SNDR	78.4 dB	86.8 dB
input DR	82.0 dB	90.3 dB
Image Rejection	57 dB @ mean	76 dB @ 70 KHz
Input Range	2 V_{pp}	1.8 V_{pp}
Power Dissipation	4.6 mW @ 2 V	2.7 mW @ 1.8 V
Technology	0.25μm CMOS	0.25μm CMOS
Chip area	$0.66 \times 0.59 mm^2$	$0.5 \times 1.4 mm^2$ (inc.pad)
FOM [3]	9.3×10^{15}	7.4×10^{16}

a Matlab workstation in order to estimate the SNDR and input DR.

In order to ensure that second and third harmonic tones fall within the signal bandwidth of 200 kHz centered around 130 kHz, a quadrature sinusoid at 70 kHz with -3 dBFS was selected. Measurement results demonstrate a SFDR of 96.0 dB and an image rejection (IR) of 88.3 dB as shown in Fig. 18. The SNDR of the designed chip was measured under the above conditions. These date demonstrate that input DR of 90.3 dB was achieved with a peak SNDR of 86.8 dB as shown in Fig. 19.

The measured power dissipation is less than 2.7 mW at 1.8 V supply voltage. In Table II, the measured results are summarized.

VII. CONCLUSION

This paper presents a continuous-time quadrature bandpass sigma-delta($\Sigma\Delta$) modulator with a CICFF topology for the use in GSM/EDGE low-IF receiver, which has a capacitive summation of feedforward coefficients. The CICFF topology is suited for implementation in low power applications. A new compensation scheme with cross-coupling resistors was proposed for a polyphase filter and the summation of feedforward signals was implemented by weighted capacitors, without the necessity of any additional active components. Compensation scheme needs to move of zeros to the center frequency, which are introduced due to the capacitive feedforward summation. The effectiveness of the proposed architecture is demonstrated on a test chip which was taped out in a standard 0.25-μm CMOS technology. The designed $\Sigma\Delta$ modulator has a power dissipation of 2.7 mW at 1.8 V supply voltage, a dynamic range of 90.3 dB and a peak SNDR of 86.8 dB at 26 MS/s. The area of chip is 0.5×1.4 mm^2 including pads.

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Song-Bok Kim was born in S. Hamgyong, DPR Korea, in 1976. He received the B.S. and M.S. degrees in electrical engineering from the University of Natural Sciences and Academy of Sciences, Pyongyang, DPR Korea, in 1998 and 2000, respectively.

From 2000 to 2005, he was engaged in IC design and Microelectronics Center, State Academy of Sciences, Pyongyang, DPR Korea, as a Senior Researcher where he involved with analog-to-digital converter chip developments and portable low-power applications. He is currently working toward the Ph.D. degree in RWTH Aachen University, Aachen, Germany, under the financial support of Gottlieb Daimler- und Karl Benz-Stiftung. His current research interests include mixed-signal circuit design and analog-to-digital conversion systems.

Stefan Joeres received the Dipl.-Ing. degree from RWTH Aachen University, Germany, in 2004, and the Dr.-Ing. degree from RWTH Aachen University in 2008.

His main research activities were focused on functional verification of mixed-signal, mixed-domain RF circuits. Since 2008, he is with Robert Bosch GmbH, Stuttgart, Germany, in automotive electronics.

Ralf Wunderlich was born in Dülmen, Germany, in 1971. He received the Dipl.-Ing. degree in electrical and electronic engineering from the University of Dortmund, Germany, working on analog-to-digital converters. He received the Dr.-Ing. degree in the field of integrated CMOS-only Hall sensor systems for precision length measurement at the Microelectronics Department, University of Dortmund, in 2002.

He joined the Chair of Integrated Analog Circuits at the RWTH Aachen University, Germany, where he is involved in analog and RF circuit design.

Stefan Heinen (F'07) received the Dipl.-Ing. and Dr.-Ing. degrees, both in electrical engineering, from Duisburg University, Germany, in 1988 and 1992, respectively.

After finishing the Ph.D. on noise simulation in nonlinear circuits, he joined the Siemens Semiconductor Group in 1992. He founded and headed the Siemens/Infineon Technologies RF IC design group in Duesseldorf/Duisburg, Germany. His focus has been in the area of short range wireless and cellular applications, where he has been the technical leader behind many commercial successful products for cordless phones and Bluetooth. In April 2002, he joined the Faculty of Electrical Engineering and Information Technology at RWTH Aachen University, Aachen, Germany, where he holds the Chair of Integrated Analog Circuits and is involved in the research cluster for Ultra High-Speed Mobile Information and Communication (UMIC), established under the excellence initiative of the German government. His research interests are in the area of analog and mixed-signal circuit design as well as RF system design for wireless application. From 2006 to 2008, he was on leave from RWTH Aachen University serving Infineon Technologies as a Fellow for RF Solutions.