12-bit Hybrid C2C DAC based SAR ADC with Floating Voltage Shield

Harish Balasubramaniam, Wjatscheslaw Galjan, Wolfgang H. Krautschneider and Harald Neubauer

***Abstract*—A successive approximation ADC based on the C2C DAC architecture is introduced. The ADC designed in a 0.18µm CMOS 2 Poly 4 Metal process uses a hybrid capacitive DAC combining the best of the binary weighted capacitive array and the C2C array. C2C ladder based architectures are very attractive for implementation because of its small area, high speed and low power consumption. However a major drawback associated with this DAC is the presence of high parasitic bottom plate capacitances. A concept called the floating voltage shield (FVS) is introduced to reduce the effect of these parasitic capacitances and maximize the effective use of the C2C DAC features. The converter consists of the hybrid DAC, a two stage preamplifier followed by a dynamic latch, switch array and digital circuitry for switching and control. The ADC consumes a maximum power of 630µW at a peak conversion rate of approximately 2MS/s from a 1.8V supply voltage and 40MHz clock. Use of extremely simple and yet robust analog architectures for the comparator make the ADC operation less prone to process variation errors.**

***Index Terms*—C2C DAC, CMOS data converter, Floating Voltage Shield, FVS DAC.**

I. INTRODUCTION

Efficient acquisition of analog signals requires proper integration of several low noise, high accuracy analog and digital components. In many applications such as wireless sensor networks, CMOS imagers, biomedical implants, data conversion demands stringent requirements on power and ADC characteristics.

In deep submicron technologies SAR ADC have become a popular approach to implement ADCs due to reduced analog content which is always difficult to design under low VDD conditions. Binary weighted capacitive arrays are the preferred choice for the DAC used in the successive approximation ADCs. However for each additional bit the number of capacitors rise exponentially which limits the maximum resolution of the ADC usually to around 8-10 bits due to large capacitor ratios and small area to perimeter ratio of the unit capacitor. To avoid these problems a C2C DAC can be used which provides small area, low power and high speed operation compared to binary DAC. However parasitic capacitances on the interconnecting nodes of the C2C DAC severely impede their linearity which limits their resolution to 4-6 bits.

Different approaches to minimize these parasitic effects such as the pseudo C2C ladder [1] or fixed shielding [2] have been proposed but a satisfactory solution has not been found. In each case the implementation of the C2C DAC has never been extended beyond a maximum resolution of 6 bits. In this paper the potential problem of the bottom plate parasitic capacitances in the C2C DAC is effectively reduced by using a floating voltage shield (FVS). The technique maintains the advantages of the conventional C2C ladders allowing them to be used in design of SAR ADCs and having a C2C DAC resolution which can extend beyond 8 bit resolution. To demonstrate the effectiveness of this concept a 12 bit SAR ADC is designed which incorporates the FVS concept to achieve high linearity, relatively small area footprint and low power.

The paper is organized as follows. Section II explains FVS concept. Section III overviews the architecture and functioning of the SAR ADC. The implementation of the building blocks in explained in Section IV. The simulation results of the ADC are presented in Section V.

II. FLOATING VOLTAGE SHIELD

The parasitic capacitance associated with the C2C ladder is shown in Fig.1 where $2C_p$ represents the parasitic bottom plate capacitance assuming negligible top plate parasitic capacitance. The C2C DAC loses its linearity during the conversion process because part of the charge during conversion on the floating nodes appears across these parasitic capacitors.

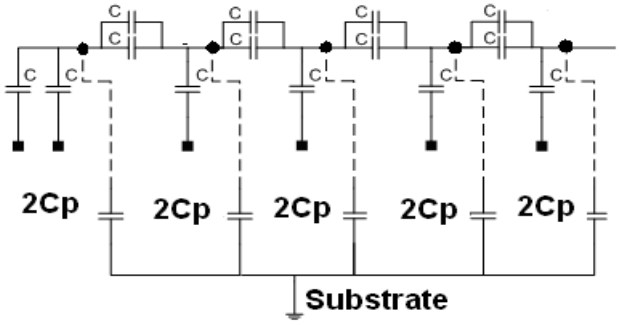

Fig. 1: Conventional C2C DAC

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The proposed concept involves shielding the bottom plates of these series capacitors using voltages generated from a similar secondary capacitor array as shown in Fig.2. The voltages generated on floating nodes of secondary array which correspond to the bottom plates of the parasitic capacitors of main array, sufficiently reduce the voltage drop across the $2C_p$ capacitor plates. Although the secondary array itself suffers from high linearity problems, huge improvement in the overall linearity of the main array of the ADC is achieved.

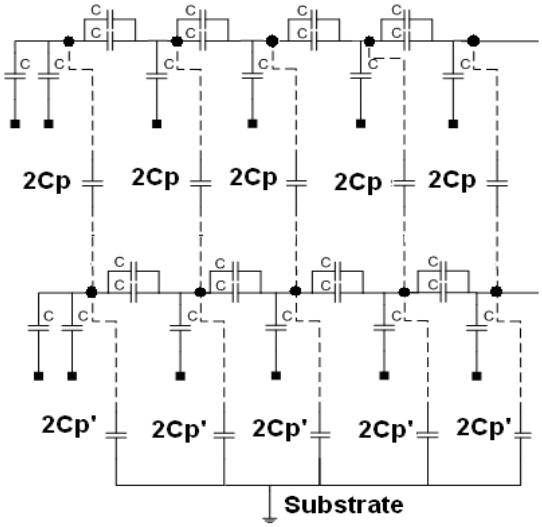

Fig. 2 Proposed FVS C2C DAC

The operation of the SAR ADC remains the same with the exception of increase in power due to the charging and discharging of the secondary capacitor array. Table I shows the results of the behavioral simulation that was done to validate the effectiveness of the concept. Three different arrays were simulated and their respective INL and DNL were calculated.

TABLE I
COMPARISON OF DIFFERENT DAC ARCHITECTURES.

Architecture (12 bit resolution)	DNL (LSB)	INL (LSB)
C2C without FVS	80	40
FVS C2C DAC	4.25	3
Hybrid DAC - (3 bit binary weighted array plus 9 bit FVS C2C array)	0.5	-1.25

It can be seen that for the 0.18µm 4 Metal 2 Poly process that is used in this design the linearity for the FVS array improves by factor of more than 10 over the conventional C2C array. Using a hybrid DAC consisting of the 3 bits of binary weighted array and 9 bits of C2C array allows the DNL to be brought under 1 LSB.

The FVS concept can be summarized as follows. The proposed concept is simple in that no major changes to the design are required except that the presence of an additional secondary capacitor array and some additional switches for generating the shield voltage. Using a process such as 0.13µm process with 8 metal options the FVS concept can extend the resolution of the C2C DAC to beyond 8 bit resolution. The linearity depends on the settling time of both the DACs and therefore it is imperative that during the process of the conversion the SAR ADC doesn't make its decision before both the DACs settle comfortably to a stable value.

III. ARCHITECTURE AND WORKING

The architecture of the ADC is depicted in Fig.3. The ADC consists of the FVS capacitor array, switching network, SAR control logic and a fully differential high resolution comparator. During the behavioral simulation all analog components were assumed ideal, therefore for hybrid DAC, 4 bit binary weighted array (2C, 4C, 8C, 16C) and 8 bit FVS C2C array was chosen. The total number of capacitors in the fully differential FVS DAC is 212. The SAR ADC is designed to handle fully differential input signal with a common mode voltage of 900mV.

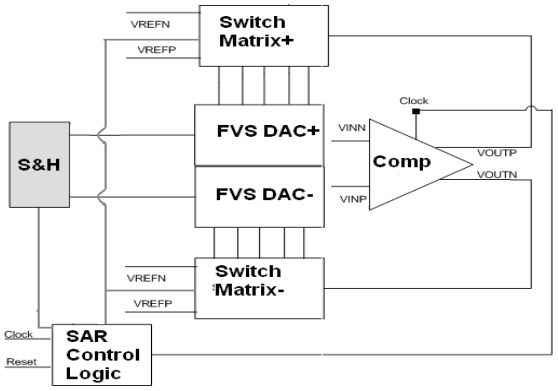

Fig. 3 SAR ADC Architecture

The SAR ADC captures the data from the comparator at each clock cycle and drives the FVS hybrid DAC bit by bit using a binary search algorithm. After n clock cycles the digital output is obtained. An additional m clock cycles are used at the beginning of each conversion to sample the fully differential signal onto the FVS hybrid DAC and autozero the comparator.

The ADC operation is controlled by the single reset pulse which initiates the conversion process. The conversion process is divided into two phases. During the first phase the comparator is autozeroed and the input voltage is sampled equally onto the FVS hybrid DAC. This phase is allotted 5 clock cycles to allow the FVS hybrid DAC sufficient time to sample the input signal and also to reduce the settling time and power requirements for the sample and hold block, so m=5.

The second phase called the bit cycling phase consists of n=13 clock cycles and implements the SAR algorithm. Each of bit cycle starts with overdrive recovery [3] to bring the preamplifier outputs quickly to common mode voltage level before the actual preamplification starts. This is done by shorting the outputs of the preamplifiers momentarily without affecting the amplified offset voltage stored on the series capacitors.

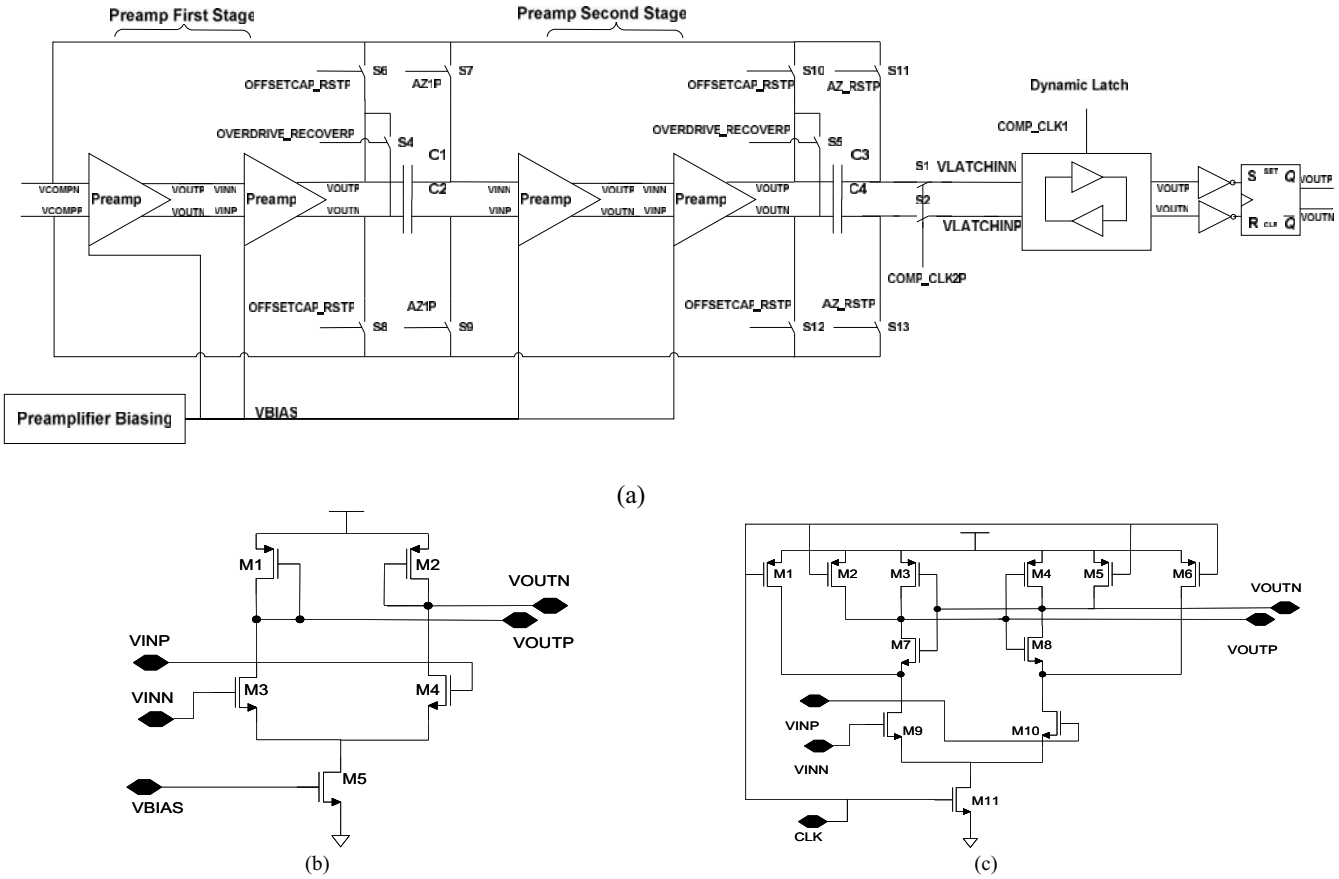

Fig. 4 (a) Comparator Architecture, (b) Preamplifier Schematic, (c) Dynamic Latch Schematic.

During this phase the bottom plates of the FVS hybrid DAC are switched from ground to common mode voltage or vice versa depending on the SAR output. After 12 clock cycles all the bits have been determined and an end of conversion flag is set to indicate the end of conversion process and initiate bit transfer.

IV. CIRCUIT DESIGN

The following section explains the various components of the ADC in detail. These components have been designed to achieve high accuracy, high conversion speed and low noise behavior and are:

1. Fully Differential Comparator.
2. SAR Control Logic and Switch Array.
3. Boosted Sampling Switch.

A. Fully Differential Comparator

The schematic of the comparator preamplifier and dynamic latch is depicted in Fig.4. The comparator in this design must be capable of detecting voltages down to 200µV for 1.8V supply. A single dynamic latch is therefore not useful in this situation and therefore a multistage comparator consisting of two preamp stages followed by a dynamic latch is employed.

Each of the two preamp stages consists of two simple amplifiers clubbed together to achieve a high dc gain during preamplification (larger than 100). Output offset cancellation techniques are employed to counteract the effect of the offsets present in the preamplifiers.

The preamplifier is a simple robust architecture consisting of n channel differential pair with diode connected PMOS loads. It provides a stable gain of over 3.5 for frequencies of up to 70MHz while consuming moderate power. The dynamic latch following the preamplifier is well explored in literature [4-6] and is popular due to its low offset of less than 5mV and very low power consumption. The amplified differential output of the preamplifier is transformed into full scale voltage by the dynamic latch due to the imbalance created by the input differential pair. When the clock is held low the output nodes of the latch are maintained at VDD.

For a clock period of 40MHz which corresponds to time period of 25ns, the comparator preamplifier consumes a time of about 18ns for the amplification of the differential signal. The rest of the time is used by the dynamic latch and the overdrive recovery phase. The overall static power consumption of the comparator is simulated to be approximately 190µW.

B. SAR Control Logic and Switch Array

The SAR control logic implements the successive approximation algorithm by successively setting and resetting the bottom plates of the FVS hybrid DAC starting from the MSB and proceeding till the LSB. Its state is controlled by the output of the comparator. The SAR control logic is well known in literature and consists of two rows of flip flops arranged in the form of sequencer and code register combination as presented in [7]. Additional flip flops are added to the sequencer to generate the control signals for the autozero phase and input signal sampling phase of the ADC.

The reference voltages used during the bit cycling correspond to ground and common mode voltage of 900mV. Therefore the switch array is made entirely of NMOS switches with the switches scaled according to the size of the capacitor in the FVS hybrid DAC. Using NMOS switches alone speeds up the operation during the bit cycling phase and maintains reduced charge injection due to the use of dummy switches.

C. Boosted Sampling Switch

The sampling of the input signal and setting the reference voltages on the top plates of the FVS hybrid DAC is done by using a boosted sampling switch. Although bootstrapped switch were explored due to their uniform charge injection effects however the increase in area/power due to charging and discharging of the capacitors in the bootstrapped switches was the limiting factor. Use of large number of such switches would have increased the power requirement which has already increased once due to presence of secondary capacitor array in the FVS hybrid DAC. Hence in this design boosted sampling switch was implemented. This switch is simplistic since it implements one clock booster [8-9] as shown in Fig.5 for boosting the gate voltage of a large number of sampling switches.

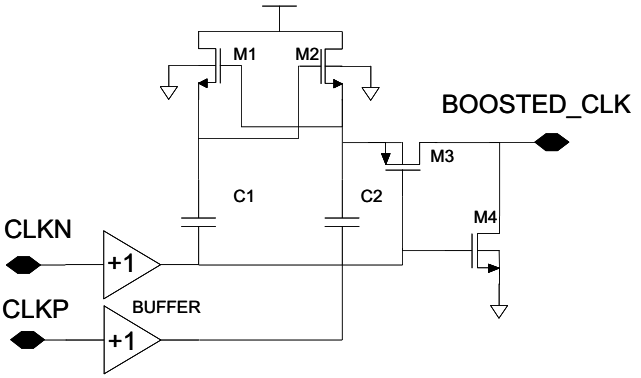

Fig. 5: Clock Booster Schematic

Gate boosting provides a uniform voltage which is little less than twice the supply voltage. Boosting the gate voltage provides a nearly constant on resistance and therefore nearly equal charge injection effects over the voltage range of (0-1.8) volts. Providing a dummy switch further reduces the charge effects although the presence of the fully differential DAC partially cancels the charge injection effects. To avoid gate reliability problems the sampling switches are implemented using the 3.3V thick oxide NMOS devices offered by the foundry.

The top plate switches use a similar design. Since the voltages on the floating nodes in the FVS hybrid DAC during the bit cycling doesn't exceed supply voltage therefore the problem due to the top plate switch turning on during bit cycling phase is also avoided.

V. SIMULATION RESULTS

Static simulation was carried out by applying a slowly varying high resolution ramp voltage at the input of the ADC. The clock frequency was chosen as 40MHz which corresponds to a conversion rate of approximately 2.2MS/s. The foundry offers the dual capacitor option of using both MIMCAPS and POLYCAPS to implement the DAC. The FVS hybrid DAC in the present design was implemented entirely using the MIMCAP option provided by the foundry with the same unit capacitance value for both the main array and the secondary array. This implies that the architecture can be implemented using a standard process as well for the FVS DAC where only MIMCAP options are provided by the foundry.

Figure 8 shows the simulated INL and DNL curves for the ADC. The DNL error is less than 0.8LSB and peak INL is about 1.8LSB. The gain error and the offset error are both insignificant with each corresponding to 0.2LSB and 0.1LSB. For applications such as CMOS Imagers where the static errors are significant the use of this type of ADC will reduce the area and power requirements while allowing higher resolution for the ADC.

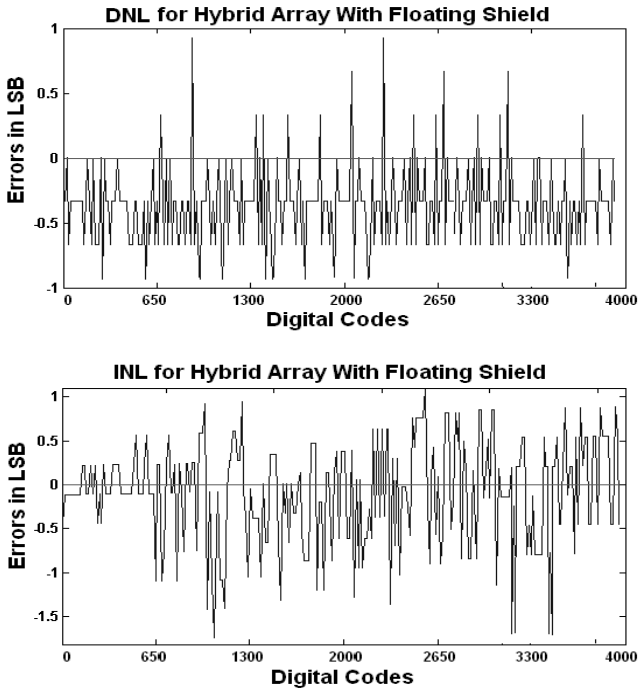

Fig. 6: INL and DNL curves.

To validate the ADC for the dynamic errors, dynamic testing was carried out with sine signal of frequencies 20 kHz and 2 MHz as input. The peak SNR for the signal of 20kHz frequency was calculated to be approx. 66dB and SINAD was found to be approx. 65dB yielding an effective number of bits (ENOB) 10.6 bits. With a 2MHz signal the values were lowered by few dB yielding ENOB of 10 bits. Depending on the application requirements lowering the clock frequency will improve the ENOB and ADC performance due to the relaxed settling time for FVS hybrid DAC. The entire results of the ADC are summarized in Table III.

TABLE II
ADC SIMULATION RESULTS

Gain Error (LSB)	0.2
Offset Error (LSB)	0.1
Integral Non Linearity (LSB)	±1.8
Differential Non Linearity (LSB)	±0.8
Effective Number of Bits @ 20KHz	10.6
Signal to Noise Ratio @ 20KHz	66.9
Signal to Noise and Distortion Ratio (dB) @20KHz	65.2
Maximum Power (µW)	630

VI. CONCLUSION

In this paper, a low power, high resolution SAR ADC designed using 180 nm technology is presented. The converter is based on hybrid capacitive DAC which combines a binary weighted and C2C array. A floating voltage shield concept to reduce the parasitic capacitance effect associated with the C2C DAC is introduced and validated through simulations. When compared to a conventional SAR ADC, the present ADC offers better performance in terms of linearity, power and area. The ADC is suitable for application existing over wide frequencies ranging from biomedical to imaging and communications.

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