Chapter 2
Basic MOS Device Physics

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Overview

- Reading
  - **Chapter 2**
- Objective
  - **Understand how the MOS transistor works**
  - **Understand the simple, large-signal model for the MOS transistor**
  - **Understand second-order effects such as body effect, channel-length modulation, and sub-threshold conduction.**
  - **Derive a MOSFET small-signal model**

We will use the simple long channel MOS model to construct our first amplifier - a common source stage. Looking at its transfer function, we'll find that treating signals as "small" with respect to the bias conditions allows us to linearize the circuit. Next, we generalize this approach and develop a more universal "small signal model" for MOS devices that are biased in the forward active region.

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2.1 General Consideration

2.1.1 MOS Device Structure

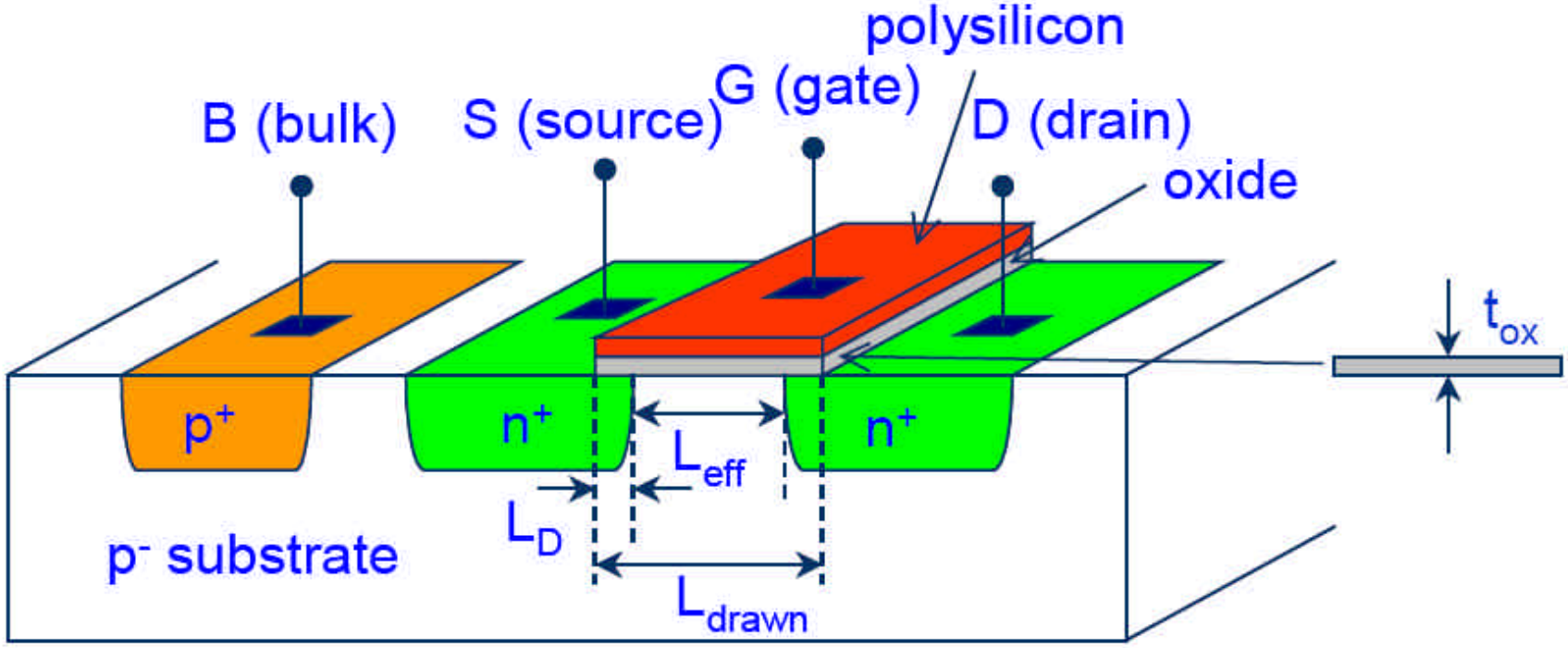

Fig.2.1 MOS Device Structure

MOSFET layout

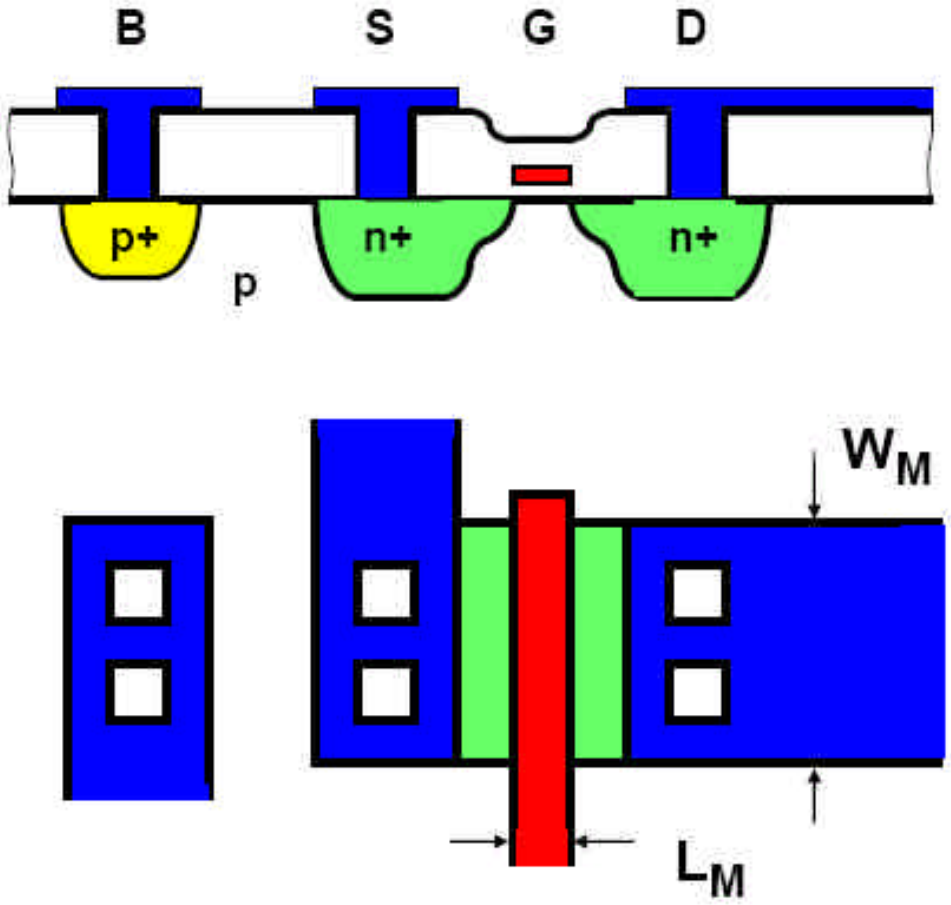

Fig.2.2 MOSFET layout

Terminals

Terminals:

- Bulk - Used to make an ohmic contact to the substrate
- Gate - The gate voltage is applied in such a manner as to invert the doping of the material directly beneath the gate to form a channel between the source and drain.
- Source - Source of the carriers flowing in the channel
- Drain - Collects the carriers flowing in the channel

Parameters Definition

W	**Gate width；**
L_{drawn}(L)	**Gate length--layout gate length；**
L_{eff}	**Effective gate length；**
L_D	**S/D side diffusion；**
W/L	**Aspect ratio.**
t_{ox}	**the gate oxide thickness, depending the technology, t_{ox} varies from 300 Å (for 1.5 μm technology) to 22 Å (0.13 μm technology).**

NMOS and PMOS with n-Well

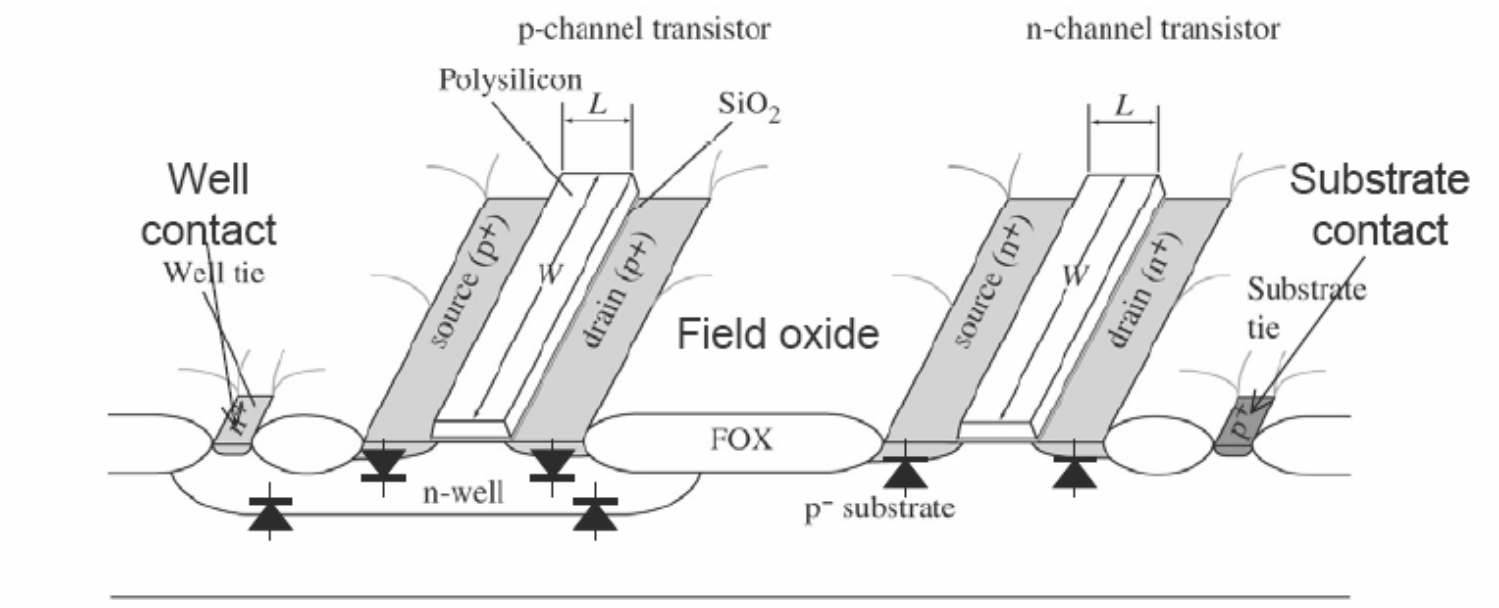

Fig.2.3 NMOS and PMOS with n-Well

- All NMOS transistors share the same bulk terminal connection – p-substrate
- PMOS transistors may share or have separate bulk terminals – n-wells.
- The diodes must all be reverse biased.

2.1.2 Symbols

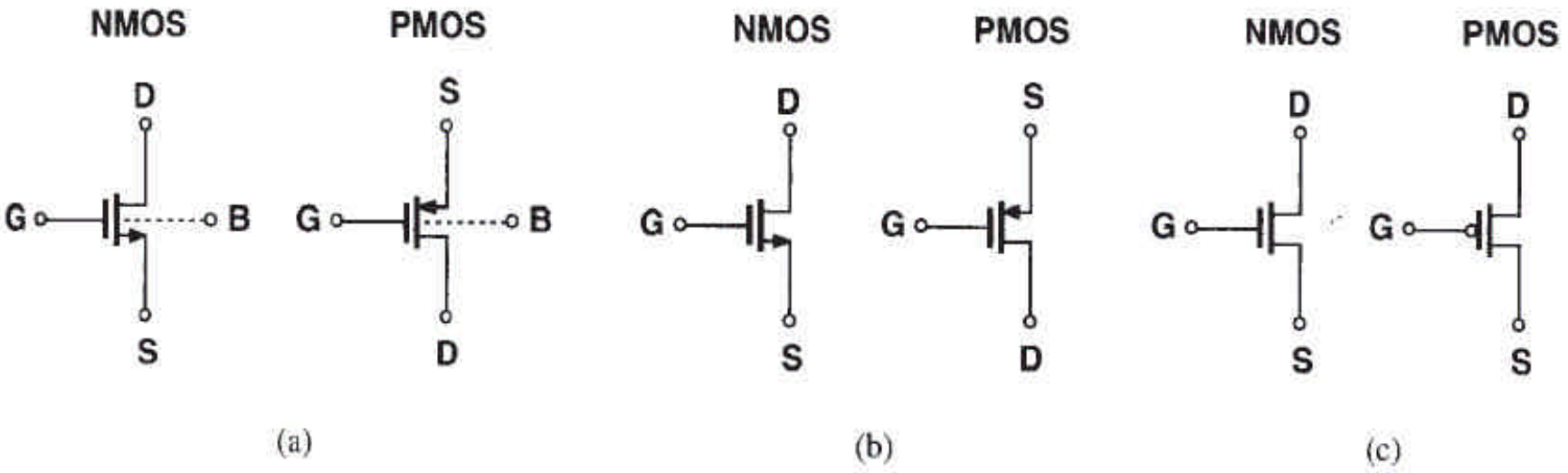

Fig.2.4 NMOS and PMOS Symbols

• If the Bulk terminal is not explicitly drawn, for NMOS (PMOS) devices, Bulk terminal to most negative (positive) power supply terminal.

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2.2 I/V Characteristics

2.2.1 Threshold voltage

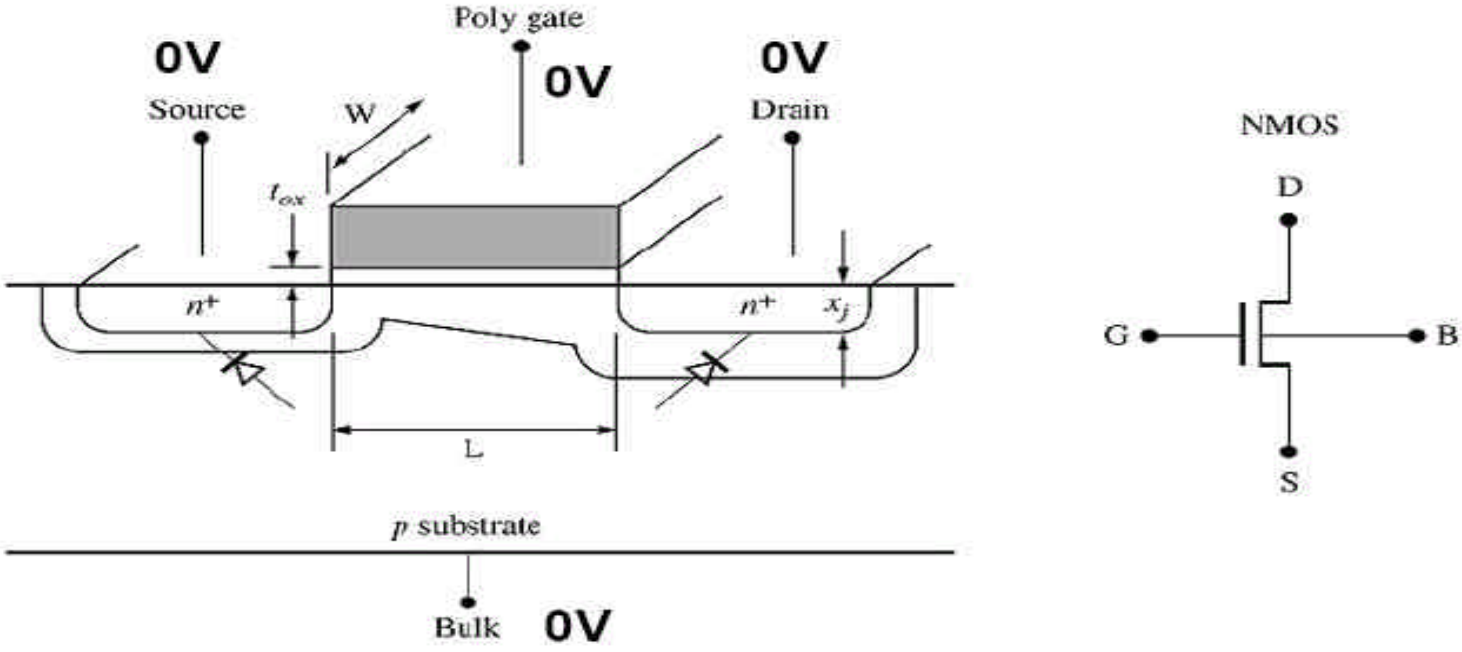


Fig.2.5 NMOS with zero voltage across all terminal pairs

- With zero voltage across all terminal pairs, device is "off"

– Back to back reverse biased PN junctions

Threshold voltage (cont.)

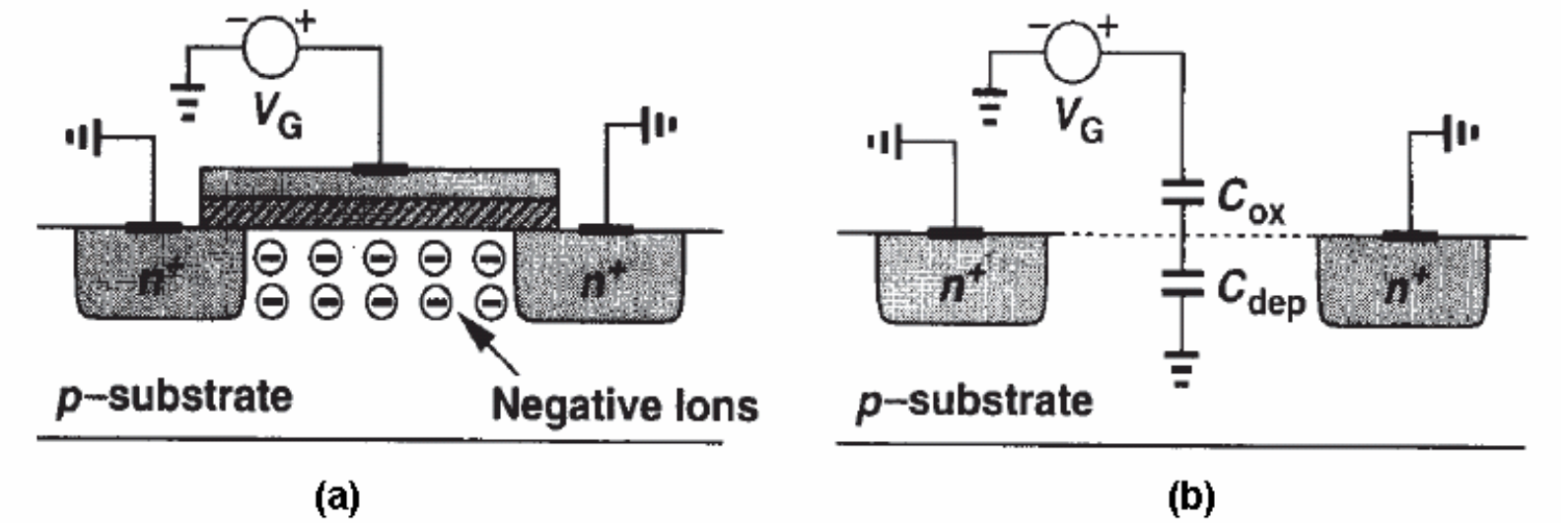


Fig. 2.6 NMOS with a positive gate bias applied V_G
(a) Formation of a depletion region (b) Onset of inversion

Since the gate and the substrate form a capacitor, as V_G becomes more positive, the holes in the p-substrate are repelled from the gate area, leaving negative ions behind so as to mirror the charge on the gate. As V_G increases, so do the depletion region and the potential at the oxide silicon interface. In a sense, the structure resembles two capacitors in series: the gate oxide capacitor and the depletion region capacitor (Fig.2.6(b)).

Threshold voltage (cont.)

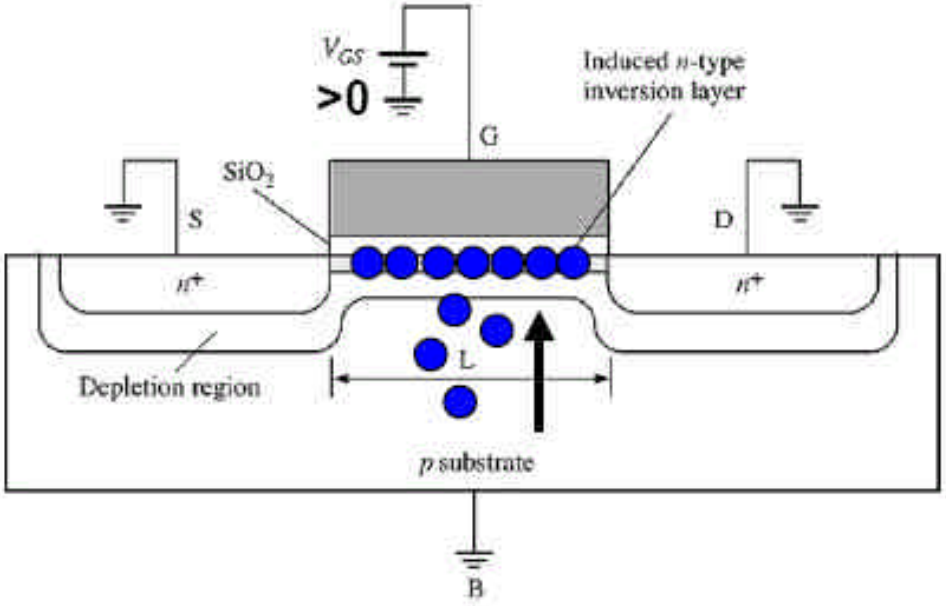


Fig. 2.7 Formation of inversion layer

As V_G increases, when the interface potential reaches a sufficiently positive value, electrons are pulled toward the positive gate electrode. Thus, a “channel” of charge carriers is formed under the gate oxide between *S* and *D*.

Threshold voltage (cont.)

We also say the interface is “inverted” (p→n type) . The value of V_G for which this occurs is called the “threshold voltage”-V_{TH}. It can be proved that,

$$V_{TH} = f_{MS} + 2f_F + \frac{Q_{dep}}{C_{ox}} \qquad (2\text{-}1)$$

Where, Φ_{MS} : the difference between the work functions of the polysilicon gate and the silicon substrate.

$$f_F = (kT/q)\ln(N_{sub}/n_i) \qquad (2\text{-}2)$$

$$Q_{dep} = \sqrt{4qe_{si}\left|\Phi_F\right|N_{sub}} \qquad (2\text{-}3)$$

q: electron charge, N_{sub}: the doping concentration of the substrate,

Q_{dep}: the charge in the depletion region, ε_{si}: the dielectric constant of silicon

C_{ox}: the gate oxide capacitance per unit area,

2.2.2 Derivation I/V Characteristics

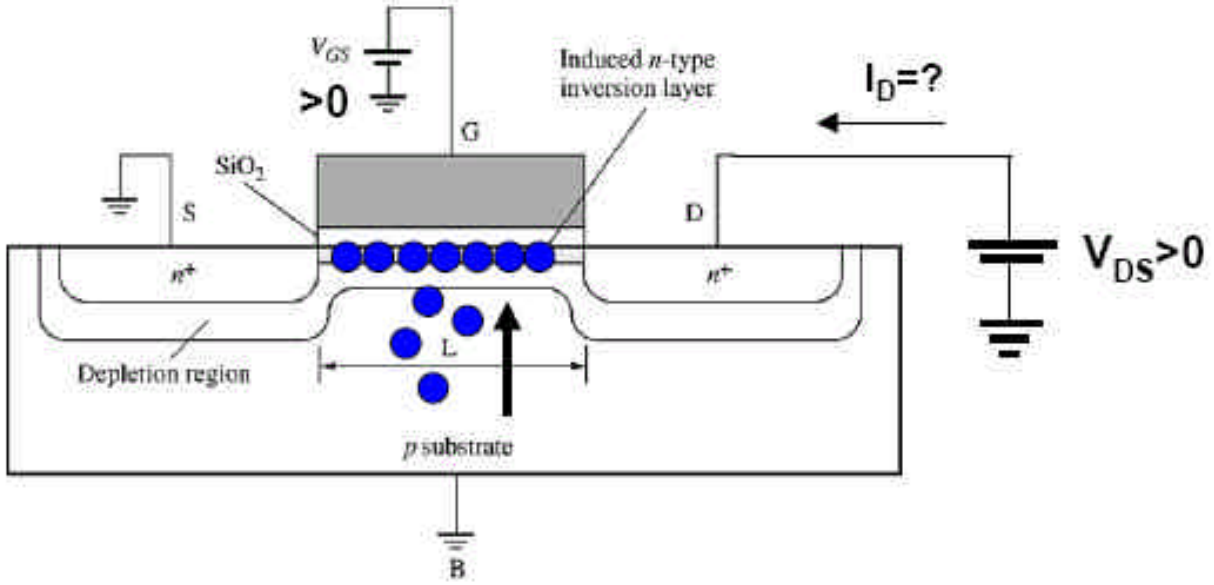


Fig.2.8 NMOS With $\mathbf{V_{GS}}$, $\mathbf{V_{DS}}$

- **If we now apply a positive drain voltage, current will flow**
- **How can we calculate this current as a function of $\mathbf{V_{GS}}$, $\mathbf{V_{DS}}$?**

Current density

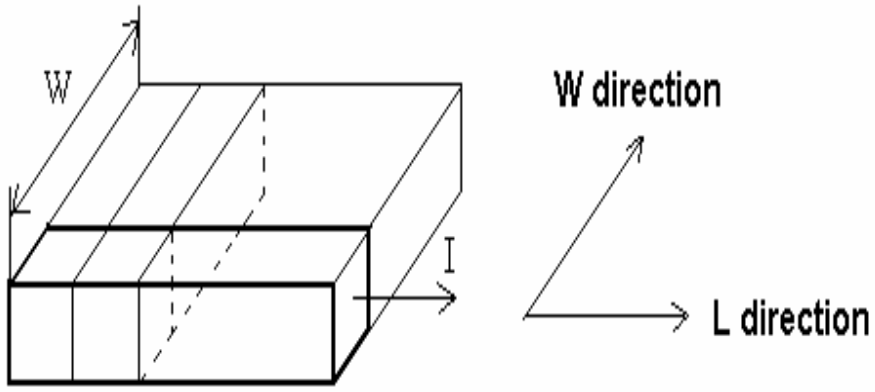


Fig.2.9 Current flow model

If the charge density along the direction of current is Q_d (C/m: Coulombs per meter) and the velocity of the charge is v (m/s: meters per second),then

$$I = Q_d \cdot v \qquad (2\text{-}4)$$

Assumptions

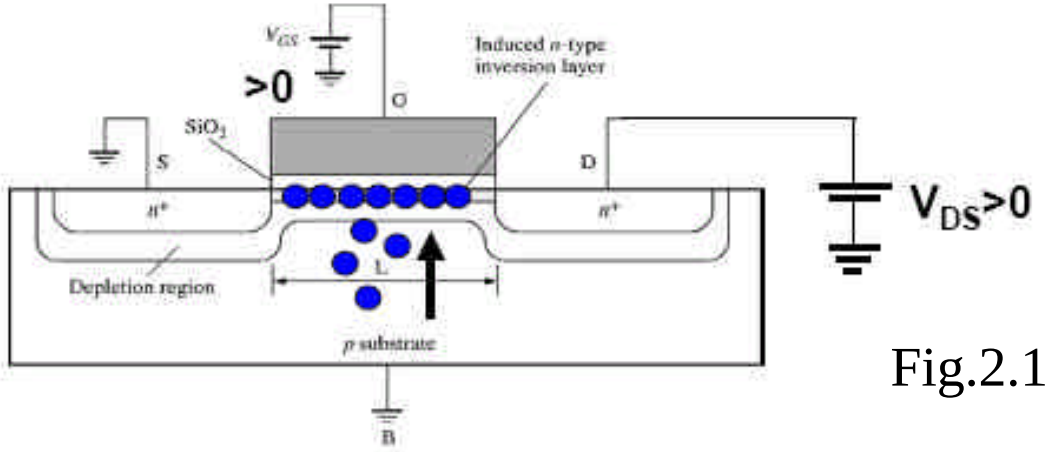


Fig.2.10 NMOS With $\mathbf{V_{GS}}$, $\mathbf{V_{DS}}$

- Current is controlled by the mobile charge in the channel. This is a very good approximation.
- "Gradual Channel Assumption" - The vertical field sets channel charge, so we can approximate the available mobile charge through the voltage difference between the gate and the channel
- The last and worst assumption (we will fix it later) is that the carrier velocity is proportional to lateral field ($v = \mu E$). This is equivalent to Ohm's law: velocity (current) is proportional to E-field (voltage)

First Order IV Characteristics (1)

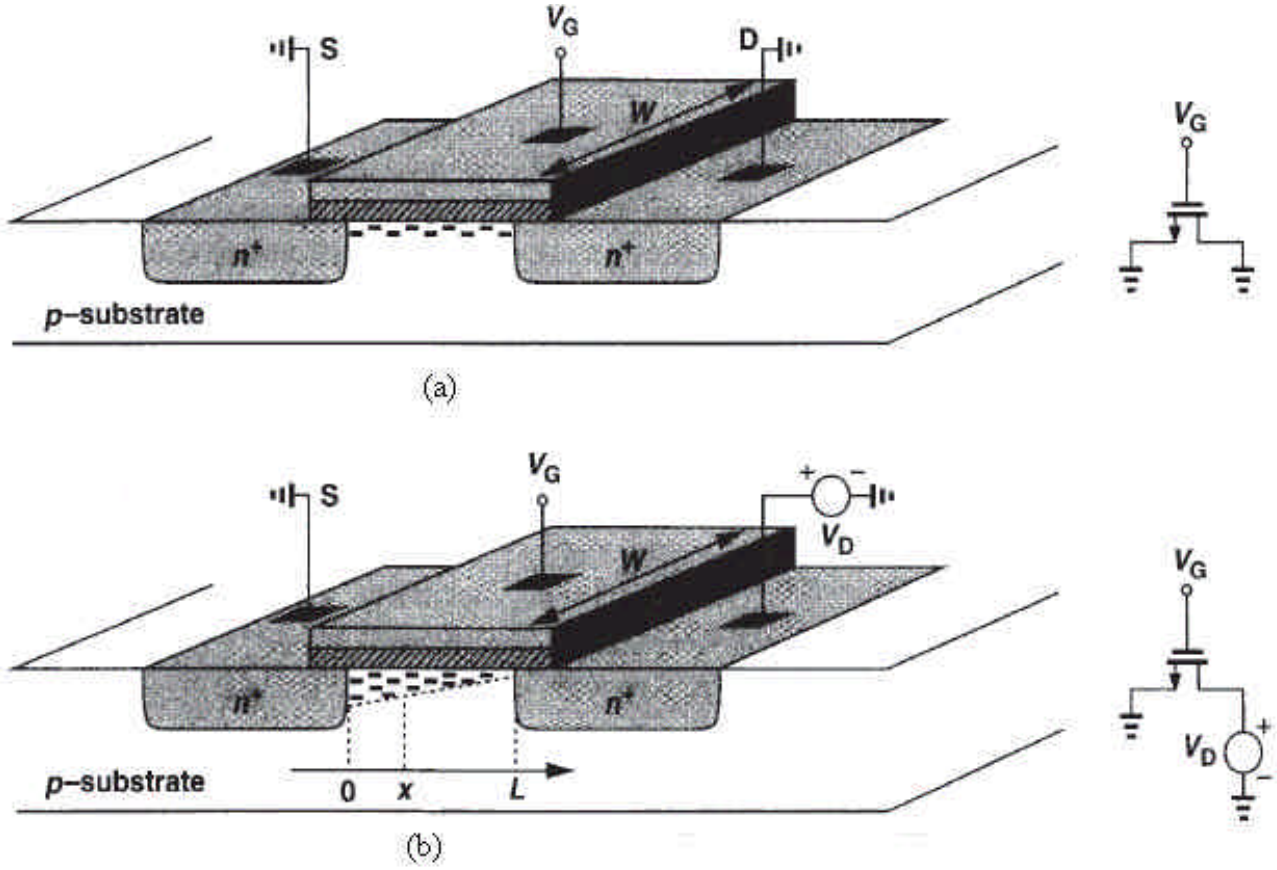
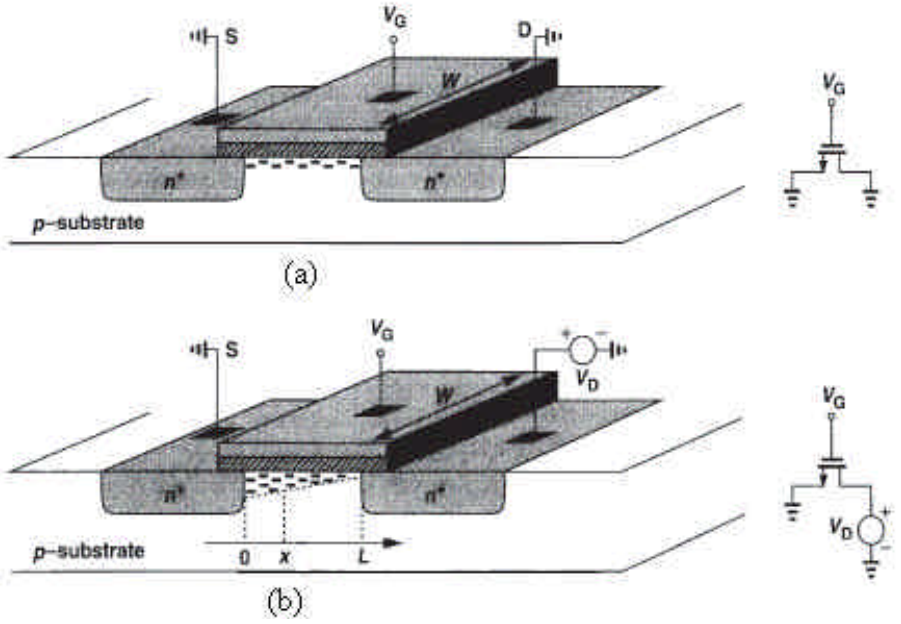


Fig.2.11 Channel charge with (a) equal source and drain voltages, (b) unequal source and drain voltages.

First Order IV Characteristics (2)



$$I = Q_d \cdot v \qquad (2\text{-}5)$$

$$Q_d = WC_{ox}(V_{GS} - V_{TH}) \qquad (2\text{-}6)$$

$$Q_d(x) = WC_{ox}(V_{GS} - V(x) - V_{TH}) \qquad (2\text{-}7)$$

First Order IV Characteristics (3)

$$I_D = -WC_{ox}[V_{GS} - V(x) - V_{TH}]v \qquad (2\text{-}8)$$

$$Given \;\; v = mE \;\; and \;\; E(x) = -\frac{dV(x)}{dx}$$

$$I_D = WC_{ox}[V_{GS} - V(x) - V_{TH}]m_n \frac{dV(x)}{dx} \qquad (2\text{-}9)$$

$$\int_{x=0}^{L} I_D dx = \int_{V=0}^{V_{DS}} WC_{ox}m_n[V_{GS} - V(x) - V_{TH}]dV \qquad (2\text{-}10)$$

$$I_D = m_n C_{ox}\frac{W}{L}[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^{\,2}] \qquad (2\text{-}11)$$

Discussing the equation (2-11)

When $V_{DS} << 2(V_{GS} - V_{TH})$, (2-11) predicts that I_D is approximately proportional to V_{DS} .This result is reasonable because the average horizontal electric field in this case is V_{DS} /L, and the average drift velocity of electrons is proportional to the average field when the field is small. Equation (2-11) is important and describes the *I-V* characteristics of an MOS transistor, assuming a continuous induced channel.

As the value of V_{DS} is increased, the induced conducting channel narrows at the drain end and (2-7) indicates that Q_d at the drain end approaches zero as V_{DS} approaches $(V_{GS} - V_{TH})$. That is, the channel is no longer connected to the drain when $V_{DS} > 2(V_{GS} - V_{TH})$. This phenomenon is called *pinch-off.*

Pinch-Off

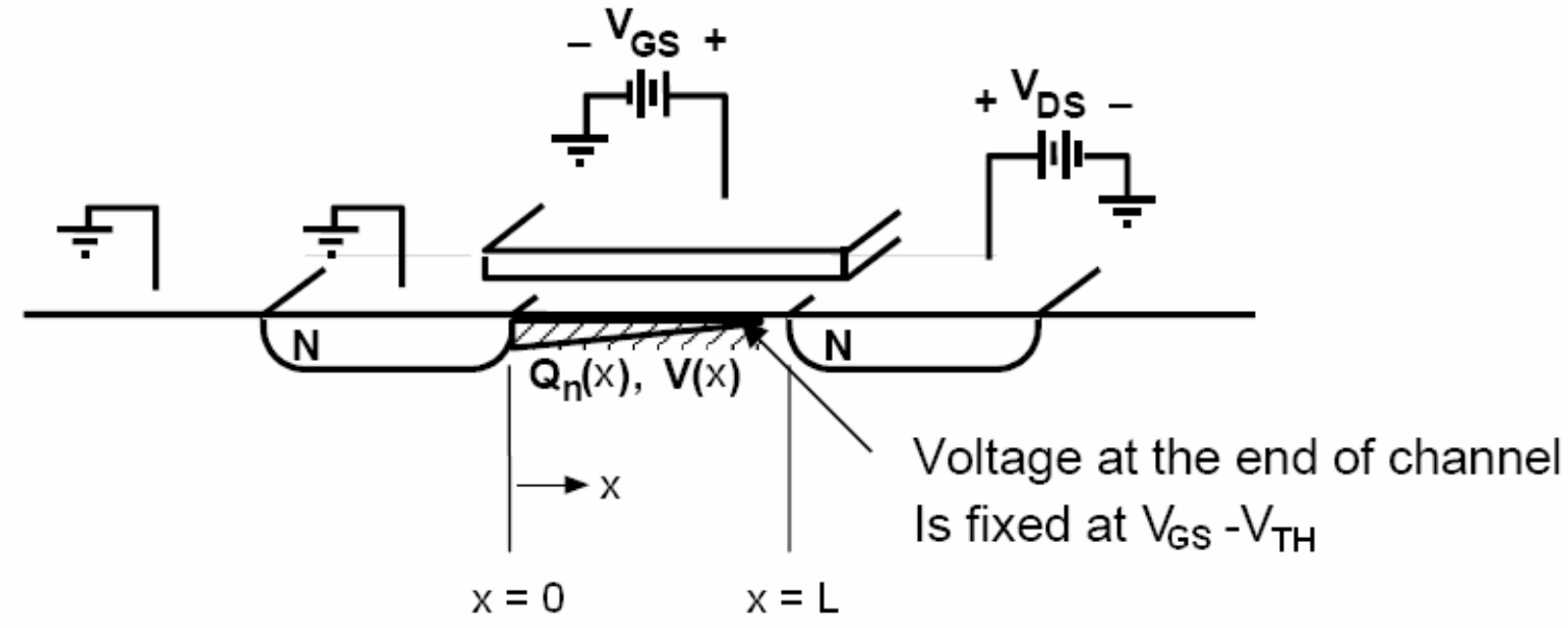


Fig.2.12 Pinch-off behavior

- After channel charge goes to 0, there is a high lateral field that ‘sweeps’ the carriers to the drain.

Operation in Active (Saturation) Region

when $V_{DS} > V_{GS}-V_{TH}$, then $V_{GD} = V_{GS}-V_{DS}$ is less than a threshold, which means that the channel no longer exists at the drain. This result is reasonable because we know that the gate-to-channel voltage at the point where the channel disappears is equal to V_{TH} by the definition of the threshold voltage. Therefore, at the point where the channel pinches off, the channel voltage is (V_{GS}-V_{TH}). As a result, the average horizontal electric field across the channel in pinch-off does not depend on the drain-source voltage but instead on the voltage across the channel, which is (V_{GS}-V_{TH}). Therefore, (2-11) is no longer valid if $V_{DS} > V_{GS}-V_{TH}$. The value of I_D in this region is obtained by substituting $V_{DS} = V_{GS}-V_{TH}$ in (2-11), giving

Operation in Active (Saturation) Region (cont.)

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

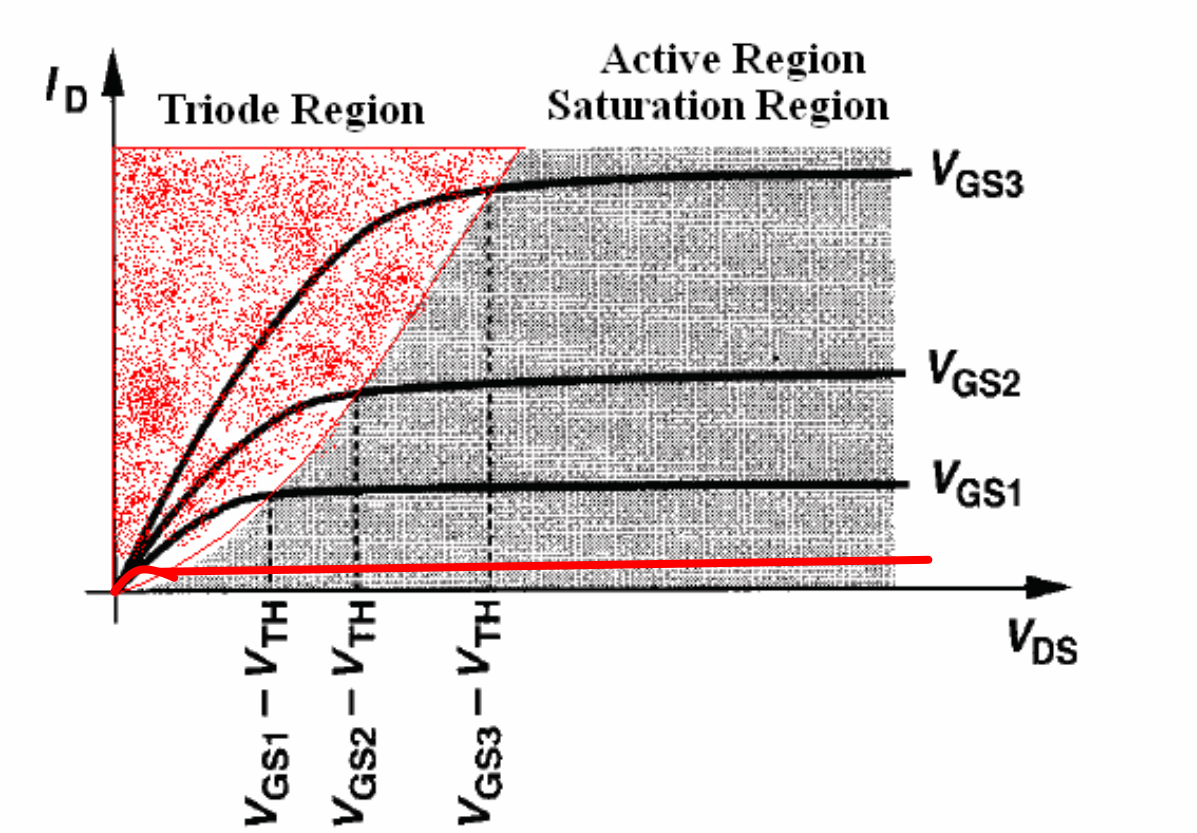
$$V'_{DS} = V_{GS} - V_{TH} \qquad (Pinch - off)$$

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2 \qquad (2\text{-}12)$$

Equation (2-12) predicts that the drain current is independent of V_{DS} in the pinch-off region. In practice, however, the drain current in the pinch-off region varies slightly as the drain voltage is varied. This effect is due to the presence of a depletion region between the physical pinch-off point in the channel at the drain end and the drain region itself. This will be discussed thoroughly more later.

NMOS device IV characteristics

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^{\,2}\right] \qquad I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2$$



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2.3 Second-Order Effects

The above equations constitute the most basic MOS IV model

- "Long channel model", "Quadratic model", "Low field model"

Unfortunately it doesn't describe modern CMOS devices accurately

- Pushing towards extremely small geometries has resulted in very high electric fields
  - Some of the assumptions on slide 15 become invalid
  - Other second order dependencies arise

2.3.1 Body Effects

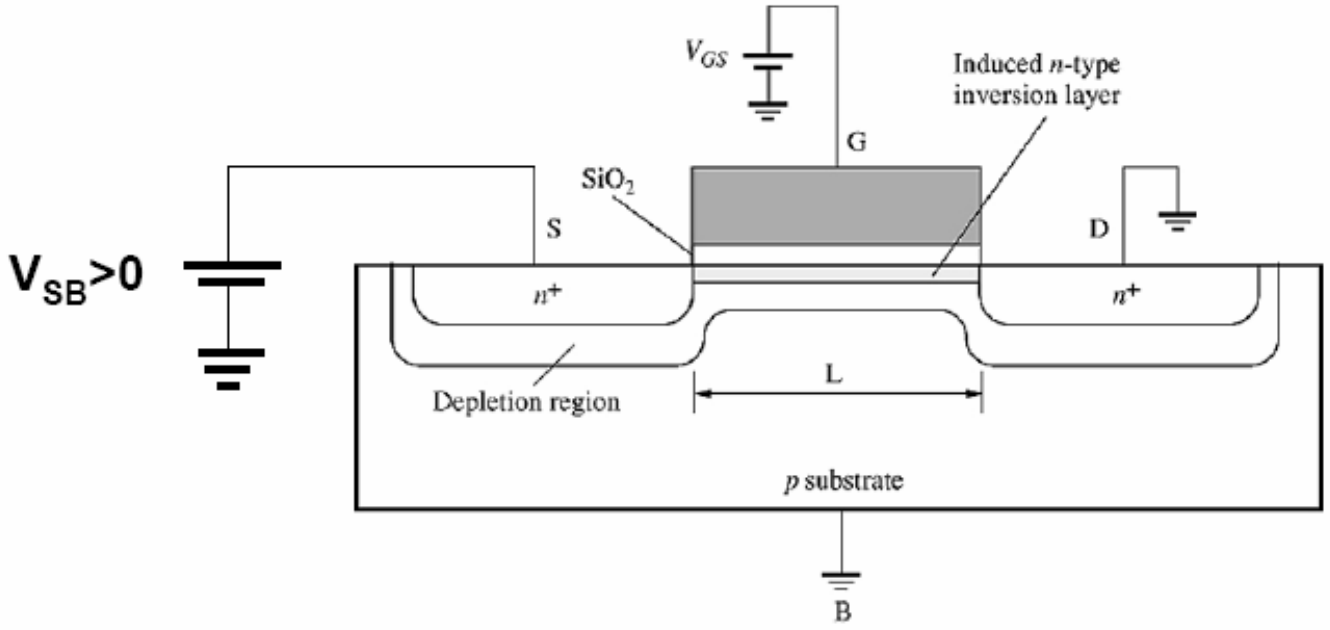

Fig.2.14

- With positive V_{SB}, depletion region around source grows
- Increasing amount of negative fixed charge in depletion region tends to "repel" electrons coming from source
  - Need larger V_{GS} to compensate for this effect

Body Effects (cont.)

- This effect is usually factored in as an effective increase in $V_{TH.}$ This is called the “body effect” or the “backgate effect.”
- Detailed analysis shows

$$V_{TH} = V_{TH0} + g\left(\sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F}\right) \qquad \text{……(2-13)}$$

Where

V_{TH0} is given by (2-1);

$g = \sqrt{2qe_{si}N_{sub}} / C_{ox}$ denotes the body effect coefficient.

Body Effects (cont.)

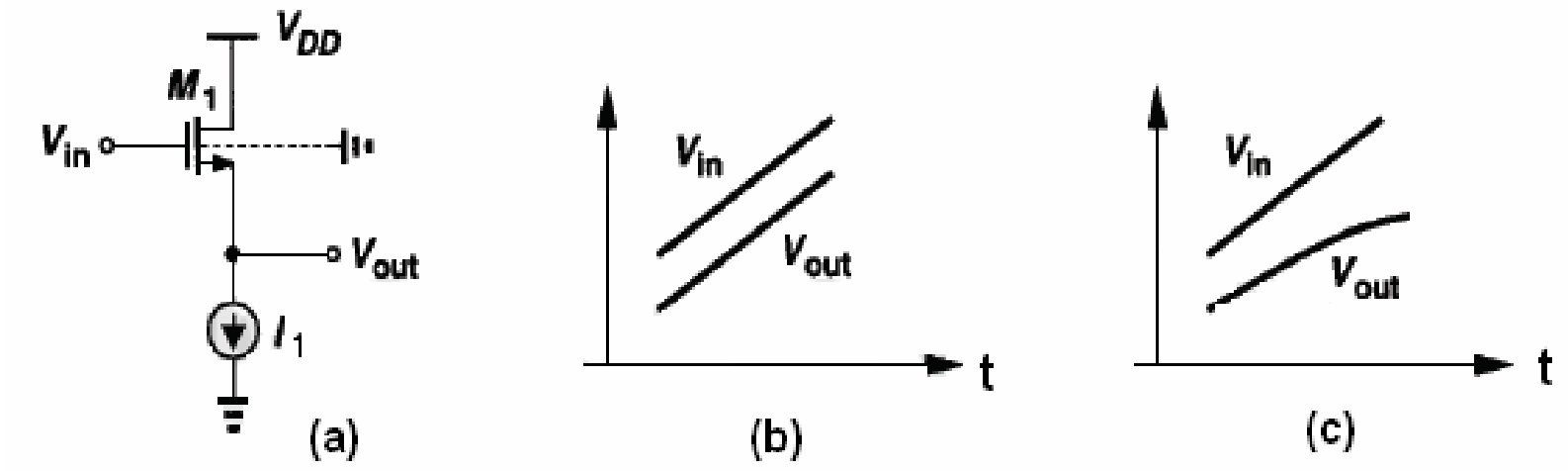

Fig 2.15 (a) A circuit in which the source-bulk voltage varies with input level, (b) input and output voltage with no body effect, (c) with body effect.

Body effect is usually undesirable. The change in the threshold voltage, e.g., as in Fig.2.15(c), often complicates the design of analog (and even digital) circuits. Device technologies balance N_{sub} and C_{ox} to obtain a reasonable value for g

2.3.2 Channel Length Modulation

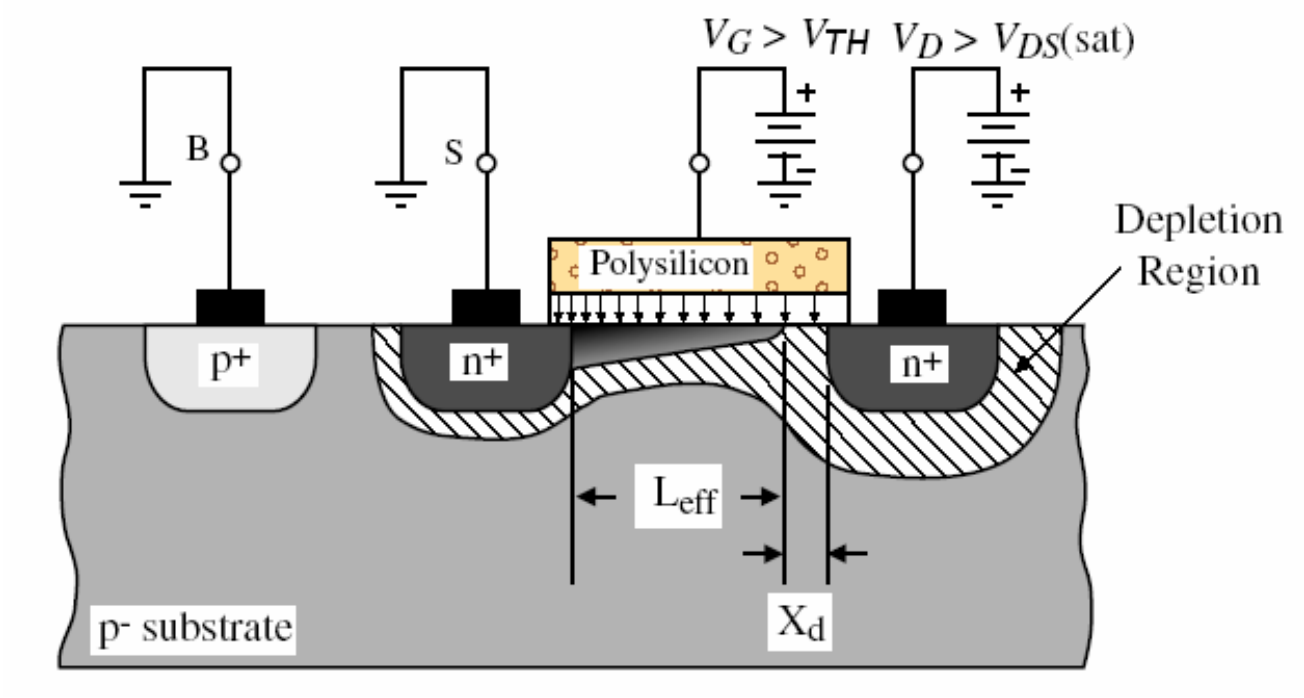

Fig 2.16 Pinch-off behavior

Channel Length Modulation (cont.)

In practice, the *effective* channel length L_{eff} in pinch-off region is given by $L_{eff}=L-X_{d.}$ This effect is due to the presence of a depletion region between the physical pinch-off point in the channel at the drain end and the drain region itself. If this depletion-layer width is X_d, then If L_{eff} is used in place of L in (2-12), we obtain a more accurate formula for current in the pinch-off region. Because X_d (and thus L_{eff}) are functions of the drain-source voltage in the pinch-off region, I_D varies with V_{DS}. This effect is called *channel-length modulation.*

Channel Length Modulation (cont.)

$$L' = L - \Delta L$$

$$\frac{1}{L'} = \frac{1}{L - \Delta L} = \frac{L + \Delta L}{L^2 - \Delta L^2} \approx \frac{1 + \Delta L / L}{L}$$

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L'} (V_{GS} - V_{TH})^2 = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{TH})^2 \left(1 + \frac{\Delta L}{L}\right)$$

$$1/L = \frac{1}{L}(1 + \lambda V_{DS}), \quad \lambda V_{DS} = \Delta L / L$$

$$I_D \approx \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS}) \quad \text{……(2-14)}$$

Channel Length Modulation (cont.)

$$l = \Delta L / L V_{DS}$$

- **λ is not a constant.**
- **It depends on the channel length.**
- **We prefer to use instead another parameter V_M, which is a constant for a certain technology.**

channel modulation voltage (V_M)

Channel Length Modulation (cont.)

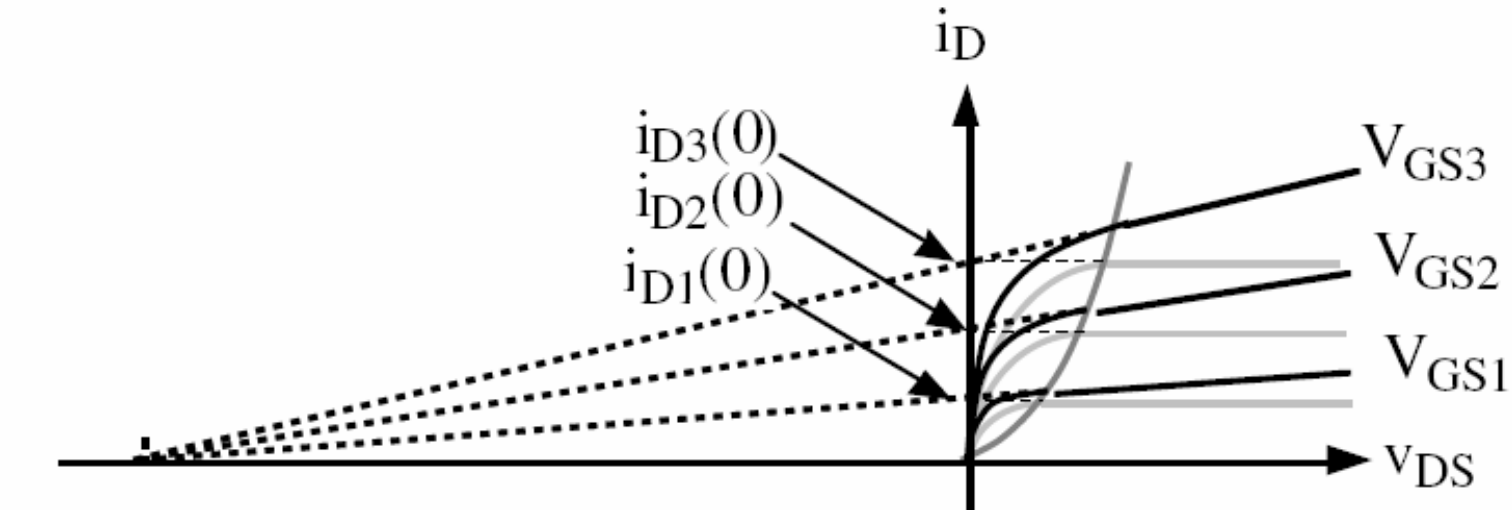

Fig 2.17 Finite saturation region slope resulting from channel-length modulation

Definition: channel modulation voltage (V_M) for MOSFET , as similar as Early voltage (V_A) for bipolar transistors

$$l = \frac{1}{V_M l} \qquad r_o = \frac{V_M l}{I_{DS}}$$

2.3.3 Subthreshold Conduction

- In previous lectures, we assume that there is no current following through the MOS transistor if V_{GS}-V_{TH} < 0 (for NMOS). Or in other words, the transistor turns off abruptly when V_{GS} reduces to V_{TH}.
- In real world, the transistor turns off gradually. When V_{GS} reduces to below V_{TH}, a small current still flows through the transistor.
- The I_D vs. V_{GS} characteristic changes from square-law to exponential.
- The *subthreshold* conduction is also called *weak inversion*, because the channel semiconductor type is weakly inverted.

Subthreshold Conduction (cont.)

- sqrt(i_D) and i_D in log scale (or log(i_D)) vs. v_{GS}

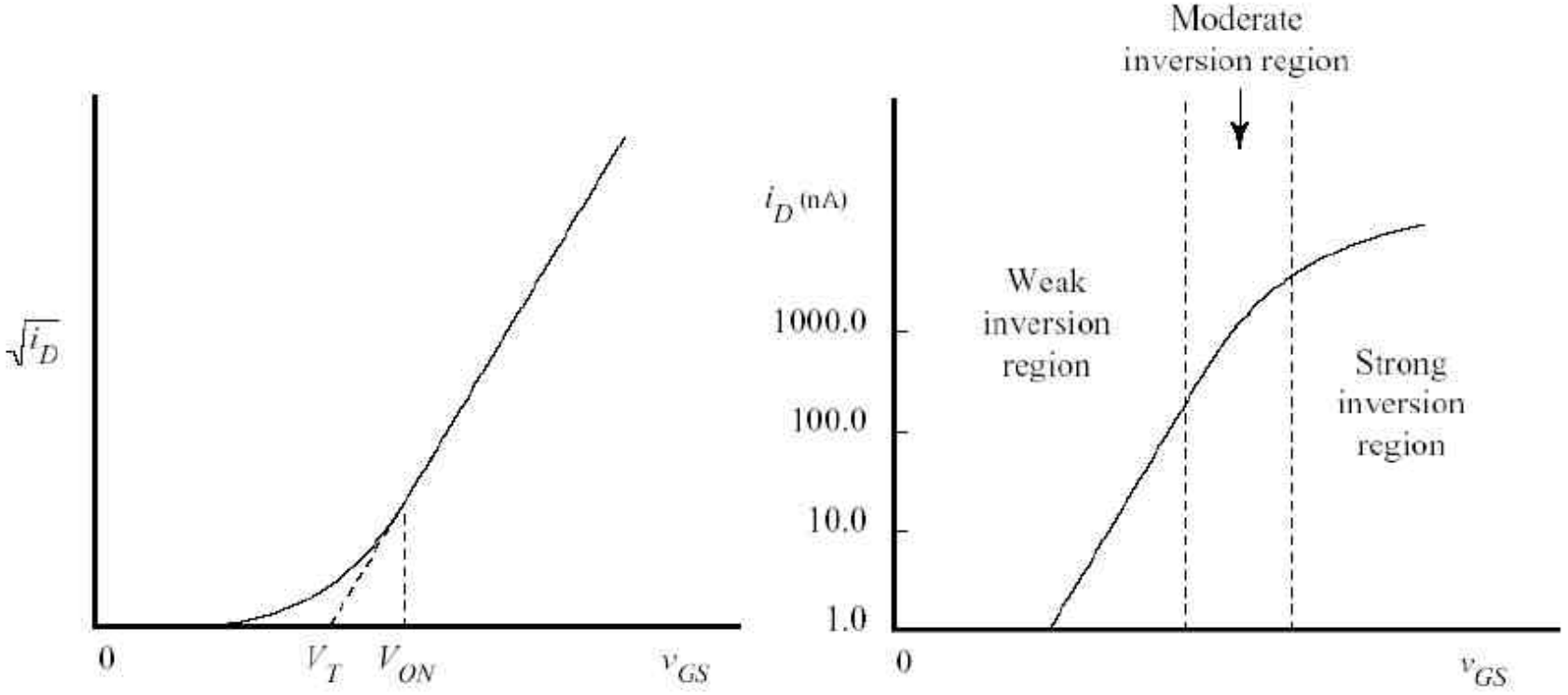

Fig 2.18 MOS subthreshold characteristics

Subthreshold Conduction (cont.)

- In subthreshold condition,

$$I_D = I_{D0}\left(\frac{W}{L}\right)\exp\left(\frac{V_{GS}}{nkT/q}\right) \qquad \text{……(2-15)}$$

- where n is subthreshold slope factor, n > 1, and usually less than 3.
- The operation region between weak-inversion (subthreshold) and strong-inversion is moderate inversion. Moderate-inversion operation is not accurately modeled.
- weak-inversion is used in low-power low-frequency applications.

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2.4 MOS Device Model Summary

- MOSFET Operation Region:

  - Cut off (or Sub threshold): When $V_{GS} < V_{TH}$;

  - Triode region: When $V_{DS} < V_{GS} - V_{TH}$, not sufficient to pinch-off the channel, we say the device operates in “triode region” or “ linear region”;

  - Saturation region: When $V_{DS} \geq V_{GS} - V_{TH}$, channel pinch-off . I_D becomes relatively constant and we say the device operates in “saturation” or “active” region.

Large Signal Model Summary (Cont.)

- **First-Order MOS Large Signal Model Summary**

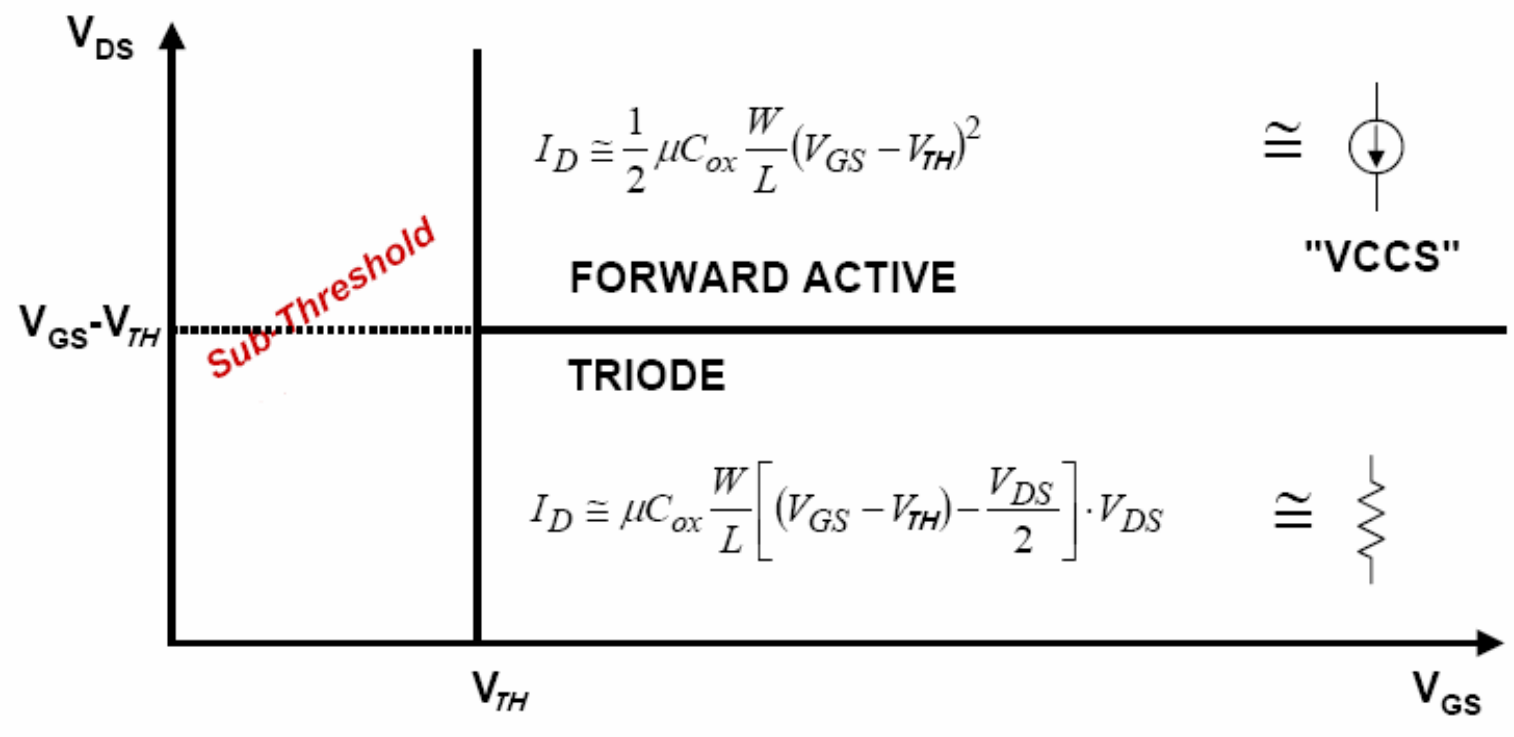

Fig 2.19 First-Order MOS Large Signal Model

Linear Resistor in Deep Triode Region

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$I_D = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})V_{DS}, \quad V_{DS} << 2(V_{GS} - V_{TH}) \quad \text{....(2-16)}$$

$$R_{on} = r_{on} = \frac{\partial V_{DS}}{\partial I_D} = \frac{1}{\mu_n C_{OX} \frac{W}{L}(V_{GS} - V_{TH})} \quad \text{.....(2-17)}$$

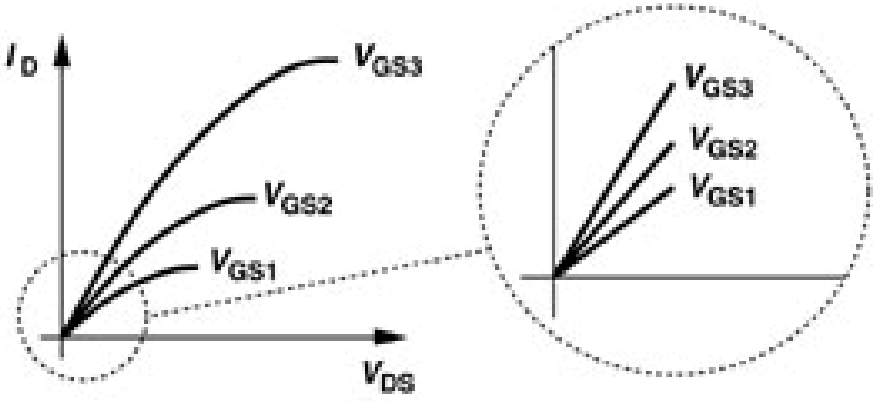

Fig.2.20 Linear operation in deep triode region

Fig.2.21 MOSFET as a controlled linear resistor

Linear Resistor in Deep Triode Region (cont.)

- A MOSFET can therefore operates as a resistor whose value is controlled by the overdrive voltage [so long as $V_{DS}<<2(V_{GS}-V_{TH})$] . This is conceptually illustrated in Fig.2.21.
- Note that in contrast to bipolar transistors, a MOS device may be on even if it carries no current.
- With the condition $V_{DS}<<2(V_{GS}-V_{TH})$, we say the device operates in deep triode region.

Example 2.1

- For the arrangement in Fig.2.17, plot the on-resistance of M1 as a function of V_G. Assume $m_n c_{ox} = 50 mA/V^2, W/L = 10$ and V_{TH} = 0.7V. Note that the drain terminal is open.

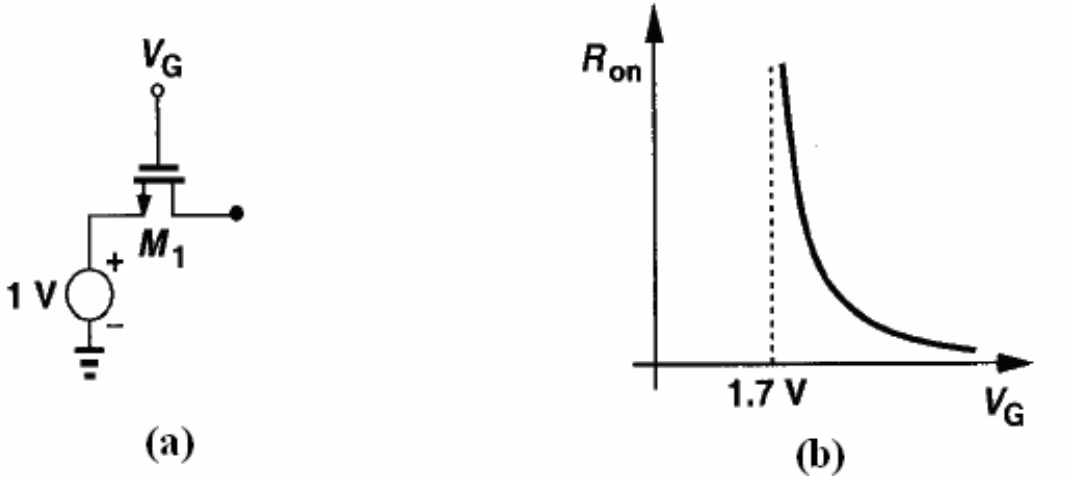

Fig 2.22

Solution

Since the drain terminal is open, I_D=0 and V_{DS}=0. Thus, if the device is on, it operates in the deep triode region. For V_G<1V+V_{TH}, M1 is off and R_{on}=∞, For V_G>1V+V_{TH}, we have,

$$R_{on} = \frac{1}{50 mA/V^2 \times 10(V_G - 1V - 0.7V)}$$

Saturated MOSFETs Operating as Current Sources

$$I_D = \frac{m_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2 \qquad (2\text{-}18)$$

A saturated MOSFET can be used as a constant current source connected between the drain and the source.

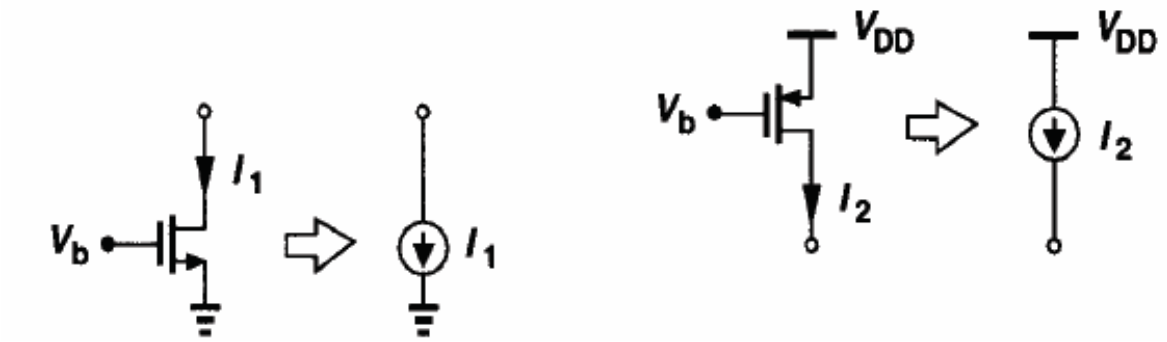

Fig.2.23 saturated MOSFETs operating as current sources

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One Way to Amplify

- **Convert input voltage to current using voltage controlled current source (VCCS)**
- **Convert back to voltage using a resistor (R)**
- **"Voltage gain"** $A_V = \triangle V_{out}/\triangle V_{in}$

  — Product of the V-I and I-V conversion factor

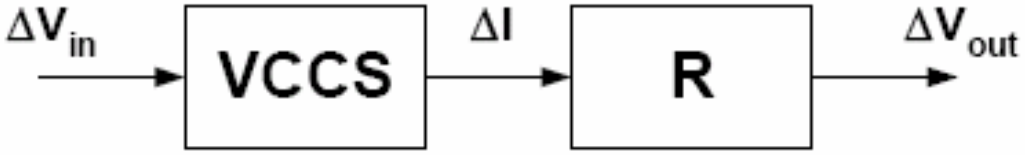


Fig 2.24 First-Order MOS Large Signal Model

Common Source Amplifier

- **MOS device acts as VCCS**

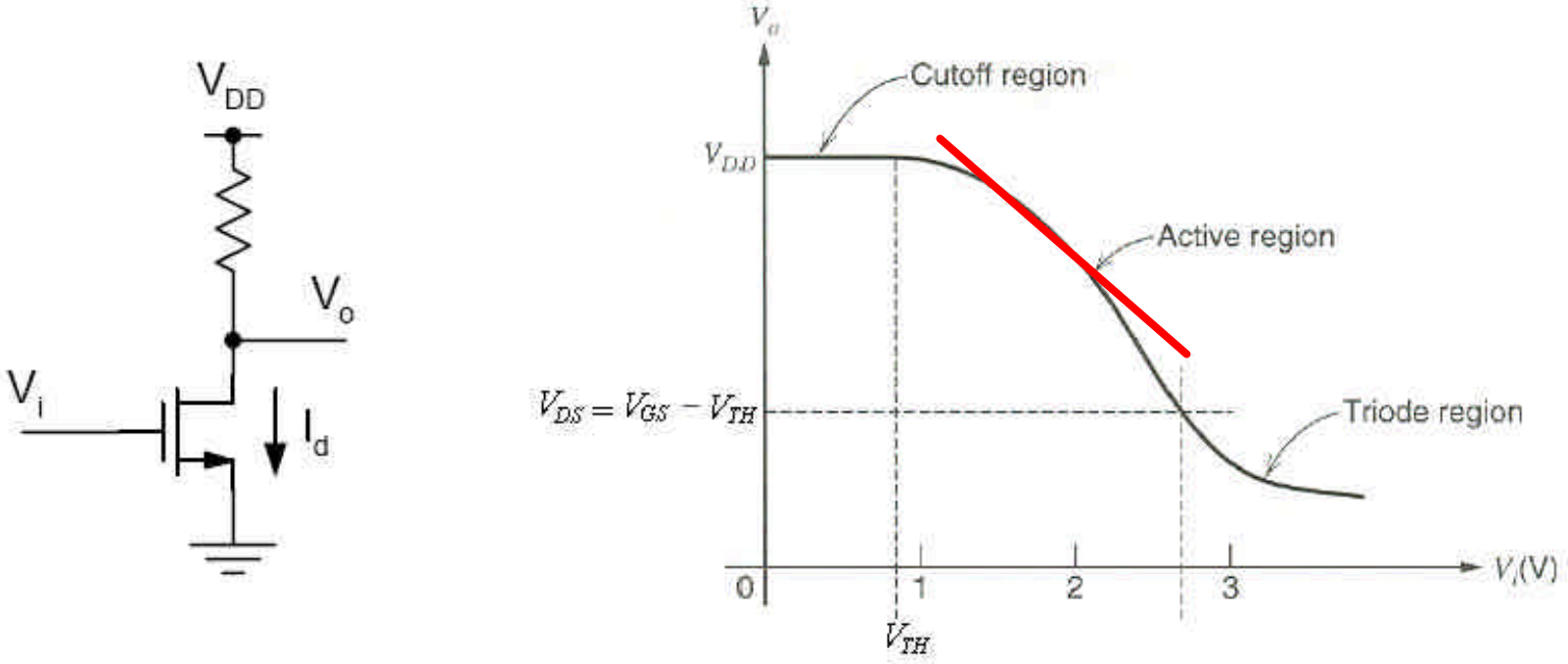


Fig 2.25 First-Order MOS Large Signal Model

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2 \qquad V_O = V_{DD} - \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2 R$$

Biasing

- **Need some sort of "battery" that brings input voltage into useful operating region**
- **Define $V_{OV}= V_I - V_{TH}$ ， "quiescent point gate overdrive"**

  -- $V_{OV} = V_{GS}-V_{TH}$ with no input signal applied

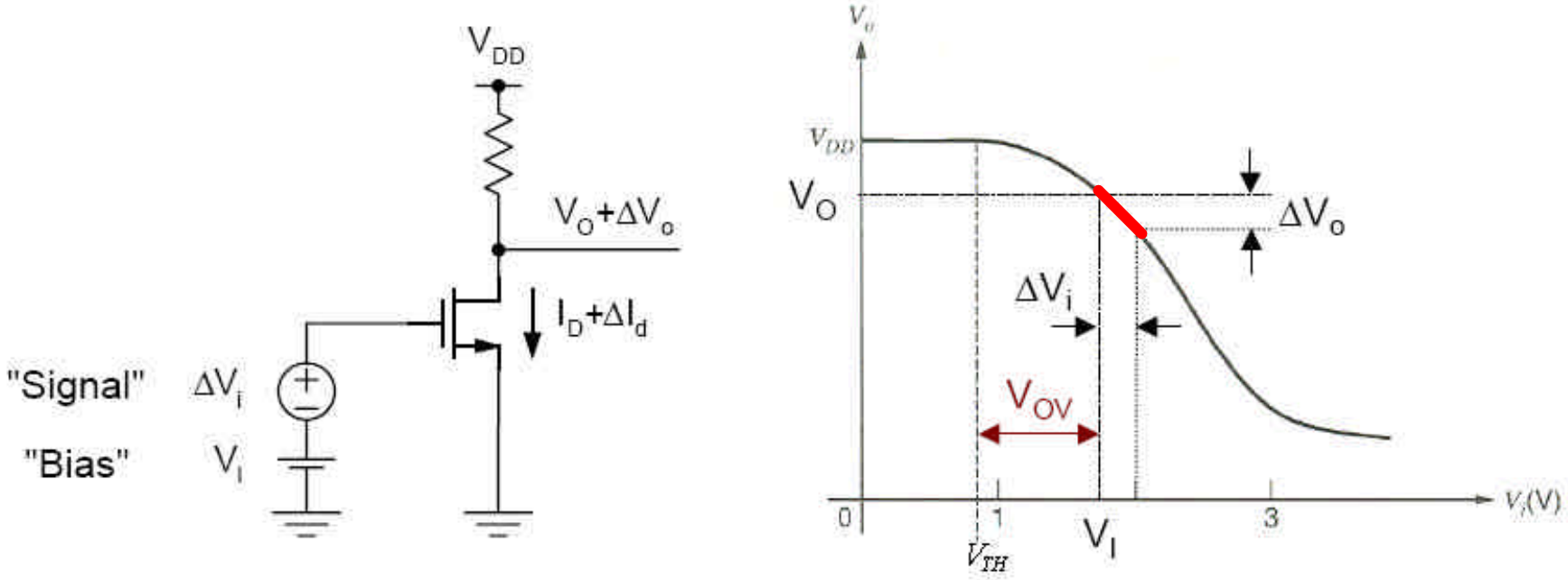


Fig 2.26 First-Order MOS Large Signal Model

Relationship Between Incremental Voltages

- **What is ΔV_o as a function of ΔV_i?** $V_O = V_{DD} - \frac{m_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2 R$

$$V_O + \Delta V_o = V_{DD} - \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{OV} + \Delta V_i)^2 \cdot R$$

$$\Delta V_o = -\frac{1}{2}\mu C_{ox}\frac{W}{L}R \cdot \left[(V_{OV} + \Delta V_i)^2 - V_{OV}{}^2\right]$$

$$= -\frac{1}{2}\mu C_{ox}\frac{W}{L}R \cdot \left[2V_{OV}\Delta V_i + \Delta V_i^2\right]$$

$$= -\frac{2I_D}{V_{OV}} \cdot R \cdot \Delta V_i\left[1 + \frac{\Delta V_i}{2V_{OV}}\right]$$

- As expected, this is a nonlinear relationship
- Nobody likes nonlinear equations, we need a simpler model
  - Fortunately, a linear approximation to the above expression is sufficient for 90% of all analog circuit analysis

Small Signal Approximation (1)

$$\Delta V_o = -\frac{2I_D}{V_{OV}} \cdot R \cdot \Delta V_i \left[1 + \frac{\Delta V_i}{2V_{OV}} \right]$$

- Assuming $\Delta V_i << 2V_{OV}$, we have

$$\Delta V_o \cong -\frac{2I_D}{V_{OV}} \cdot R \cdot \Delta V_i$$

- If we further pretend that the input voltage increment is infinitely small, we can find this result directly by taking the derivative of the large signal transfer function at the "operating point" V_I

$$\left. \frac{dV_o}{dV_i} \right|_{V_i = V_I} = -\frac{2I_D}{V_{OV}} \cdot R$$

Small Signal Approximation (2)

- Graphical illustration:

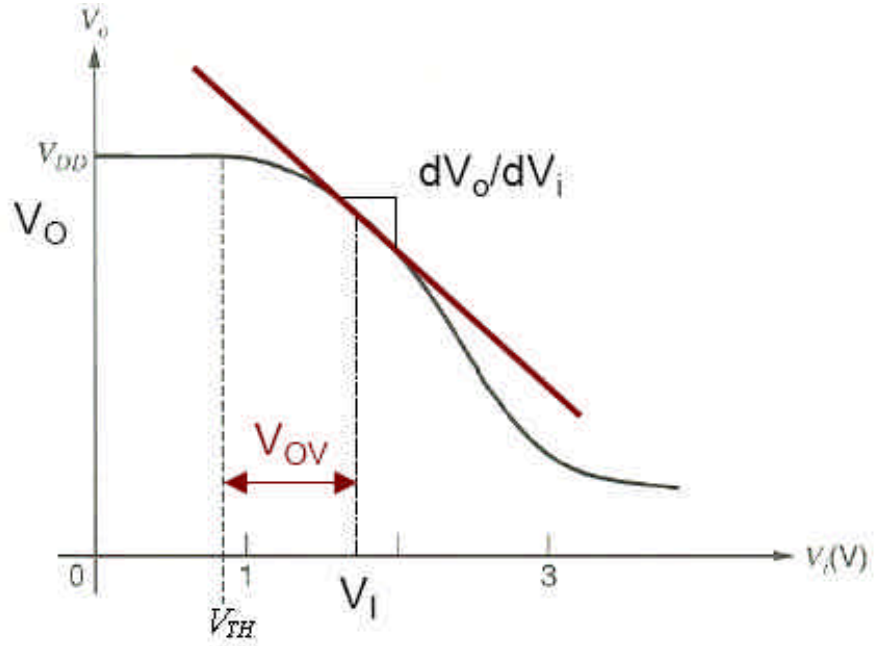


Fig 2.27

- The slope of the above tangent is the so called "small signal gain" of our amplifier

Small Signal MOS Model

- Fortunately we don't have to repeat this analysis for every single circuit we build
- Instead, we derive a linearized circuit model for the MOS transistor and plug it into arbitrary circuits

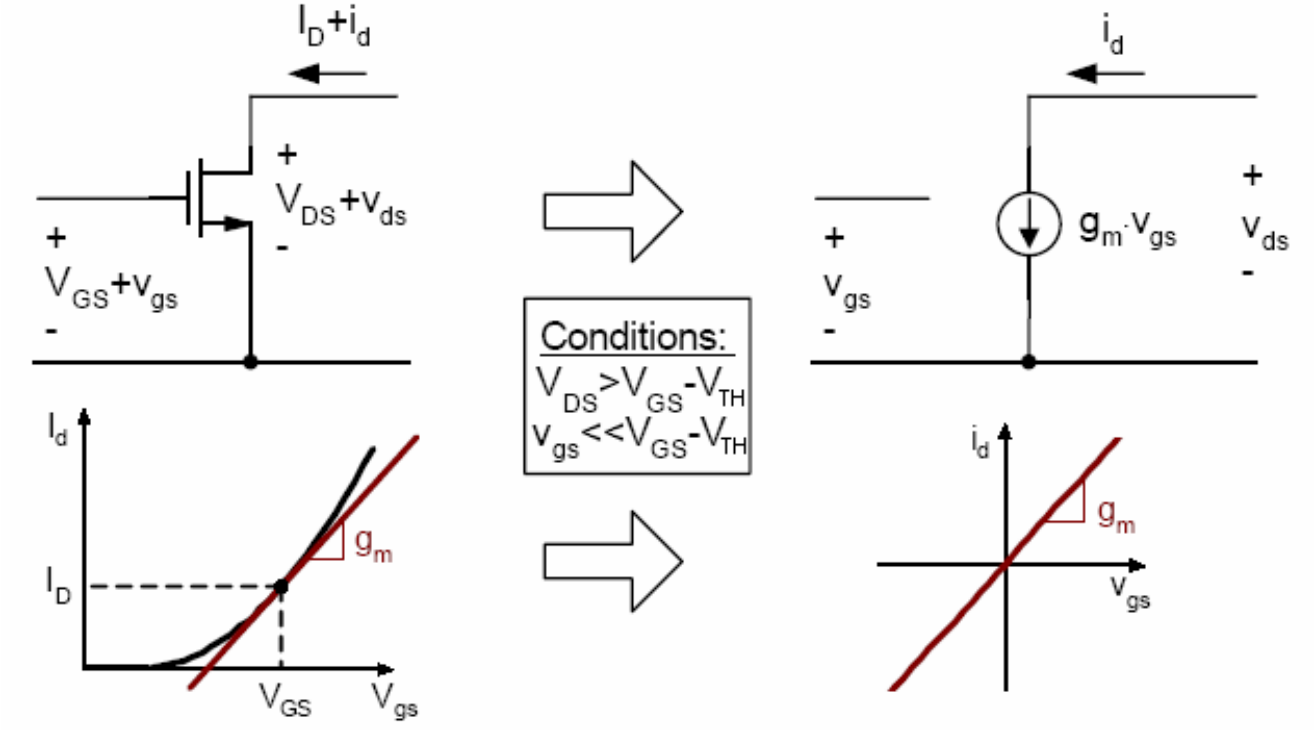


Fig 2.28

Transconductance (g_m) in Active Region

- The parameter that relates small signal gate voltage to drain current is called transconductance (g_m),
- The transconductance is found by differentiating the large signal I-V characteristic of the transistor in its operating point

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2$$

$$g_m = \frac{i_d}{v_{gs}} = \frac{\partial I_D}{\partial V_{GS}}\bigg|_{V_{DS}\ constant} = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH}) = \mu_n C_{ox}\frac{W}{L}V_{OV} \quad \text{...(2-19)}$$

$$= \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} = \frac{2I_D}{V_{OV}} \quad \text{...(2-20)}$$

Transconductance (g_m) in Active Region (cont.)

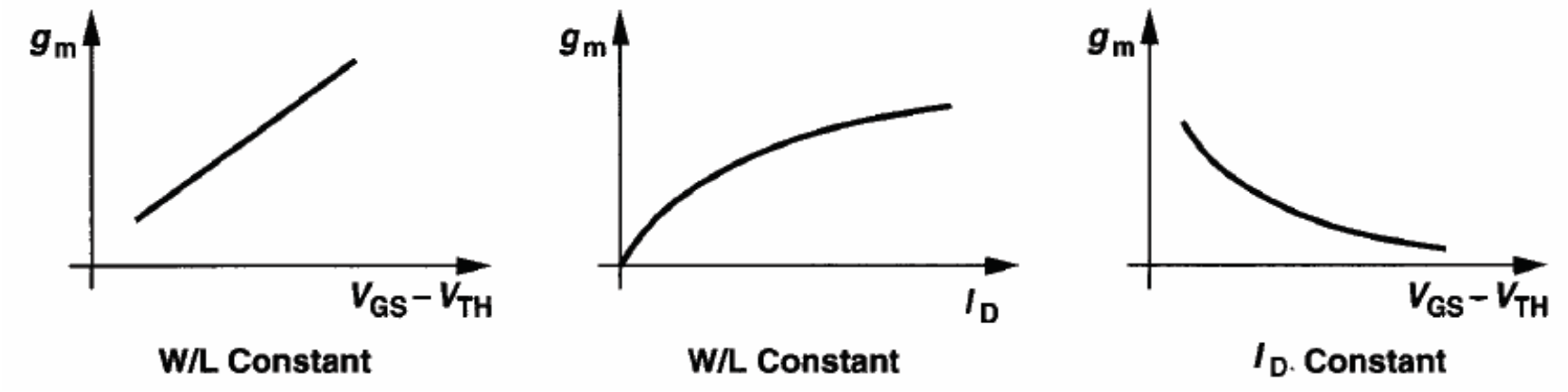


Fig.2.29 MOS transconductance as a function of overdrive and drain current

(2-19) suggests that g_m increases with the overdrive if W/L is constant whereas (2-20) implies that g_m decreases with the overdrive if I_D is constant.

Example 2.2

Ex.2.2 **For the arrangement shown in Fig.2.30, plot the g_m as a function of V_{DS}.**

Solution: It is simpler to study g_m as V_{DS} decreases from infinity. So long as $V_{DS} \geq V_b - V_{TH}$, M_1 is in saturation, I_D is relatively constant, and, from equation (2-18), so is g_m. For $V_{DS} < V_b - V_{TH}$, M_1 is in triode region and,

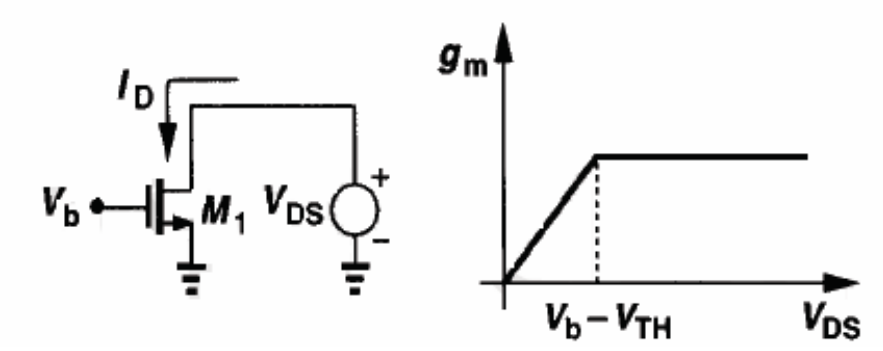


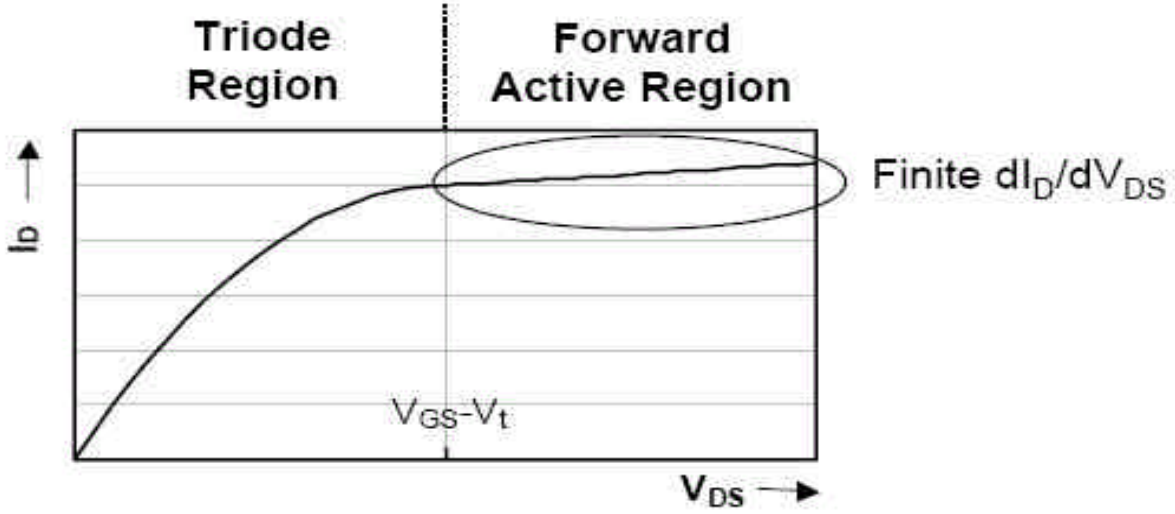
Fig 2.30

$$g_m = \frac{\partial}{\partial V_{GS}}\{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}[2(V_{GS}-V_{TH})V_{DS}-V_{DS}^2]\} = \mu_n C_{ox}\frac{W}{L}V_{DS}$$

Thus, as plotted in Fig.2.20, the transconductance drops if the device enters the triode region**. For amplification, we usually employ MOS in saturation.**

Dependence of I_D on V_{DS}

- Admittedly, our simple first order MOS I-V equation for the forward active region looks pretty unrealistic– Ideal current source!
- In reality, owing to channel-length modulation, the drain current has a weak dependence on V_{DS}

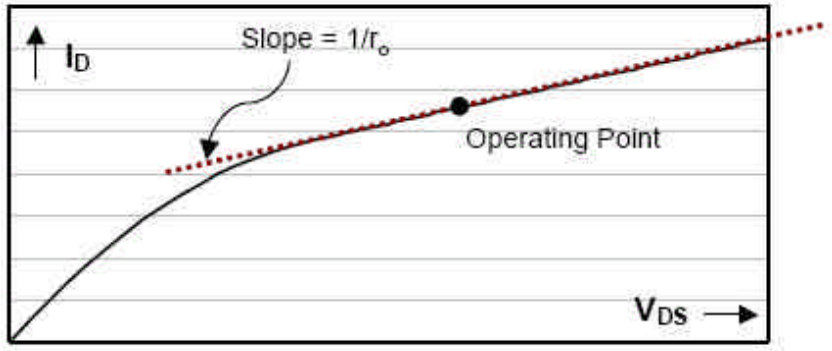


$$I_D \approx \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$

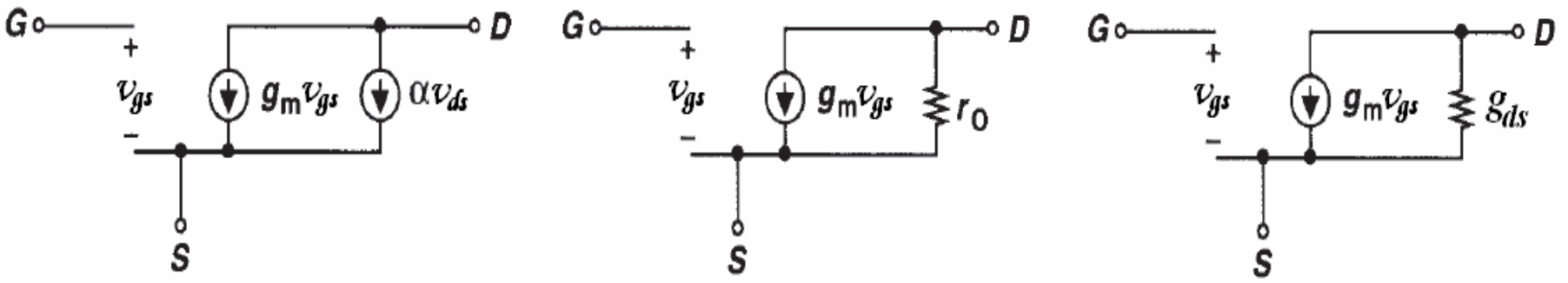
Small Signal Output Resistance

- Yet, we must somehow take the finite dI_D/dV_{DS} into account, since it quantifies how much our forward active device deviates form an ideal current source
- This effect can also be modeled by a voltage-dependent current source, but a current source whose value linearly depends on the voltage across it is equivalent to a linear resistor.
- Define "small signal output resistance" $r_{o,}$ or “small signal output transconductancd” g_{ds}.

$$\frac{1}{r_o} = \frac{\partial V_{DS}}{\partial I_D}$$



Small Signal Output Resistance (cont.)

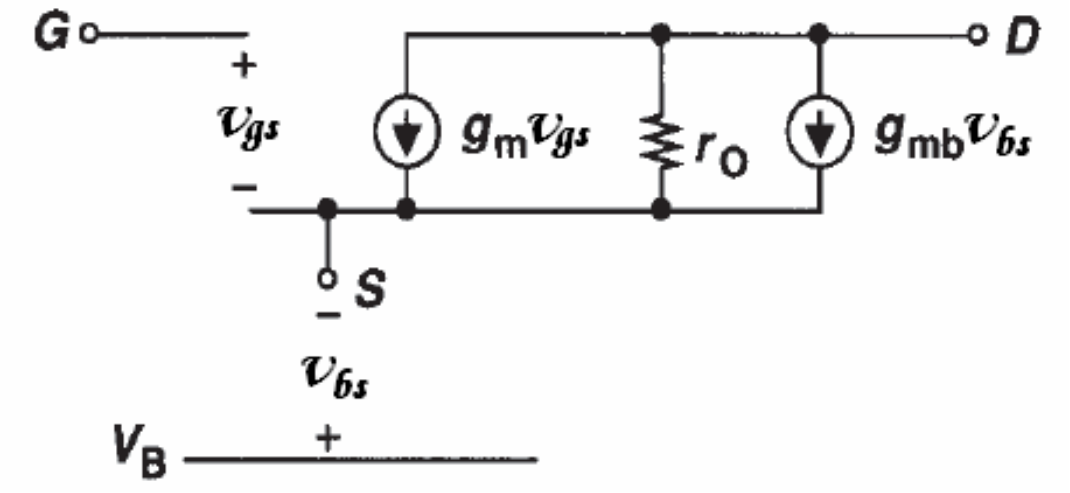


$$r_o = \frac{\P V_{DS}}{\P I_D} = \frac{1}{\P I_D / \P V_{DS}} = \frac{1}{\frac{m_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2 \, l} \approx \frac{1}{l I_D}$$

$$g_{ds} = \frac{1}{r_o} \qquad l = \frac{1}{V_M l} \qquad r_o = \frac{V_M l}{I_{DS}}$$

Bulk Transconductance, g_{mb}

- The bulk potential influences the threshold voltages and hence the gate-source overdrive.
- This effect can be modeled by a current source connected between D and S,



Bulk Transconductance, g_{mb} (cont.)

- We write the value as $g_{mb}v_{bs}$, where

$$g_{mb} = \frac{\P I_D}{\P V_{BS}} = m_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})\left(\frac{-\P V_{TH}}{\P V_{BS}}\right)$$

Also,

$$\frac{\P V_{TH}}{\P V_{BS}} = \frac{-\P V_{TH}}{\P V_{SB}} = -\frac{g}{2}(2\Phi_F + V_{SB})^{-1/2}$$

$$g_{mb} = g_m \frac{g}{2\sqrt{2\Phi_F + V_{SB}}} = h g_m \qquad h = g_{mb} / g_m$$

1st Order Small Signal Model (Forward Active)

Note:
When drawing small signal diagrams ,
(1) FIXED (constant) current source open
(2) FIXED (constant) voltage source short