Schematic/Symbol Editor User Guide

Zeni EDA System

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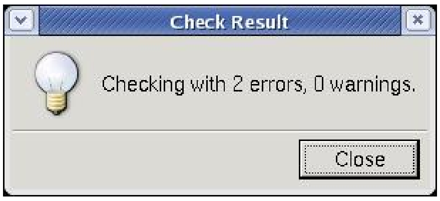
1 Schematic Editor Command

1.1 Design Menu

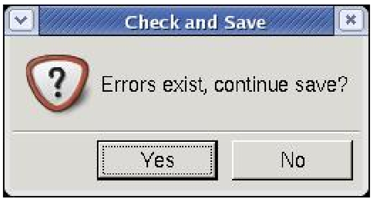
1.1.1 Design->Check and Save

Check current view and save it.

Select this command or click icon , SE checks current view and shows the results in pop-up form.



If this design is error, SE will pop up a form after you click *Close* button and inquire you save it or not with the errors.



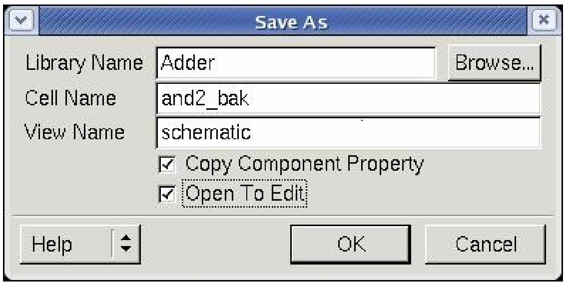
Click *Yes* button to save the view with errors. Otherwise, you need modify the design before saving.

1.1.2 Design->Save

Save current view.

1.1.3 Design->Save As

Save current view with another name.
Select this command, “Save As” form is shown as figure below.



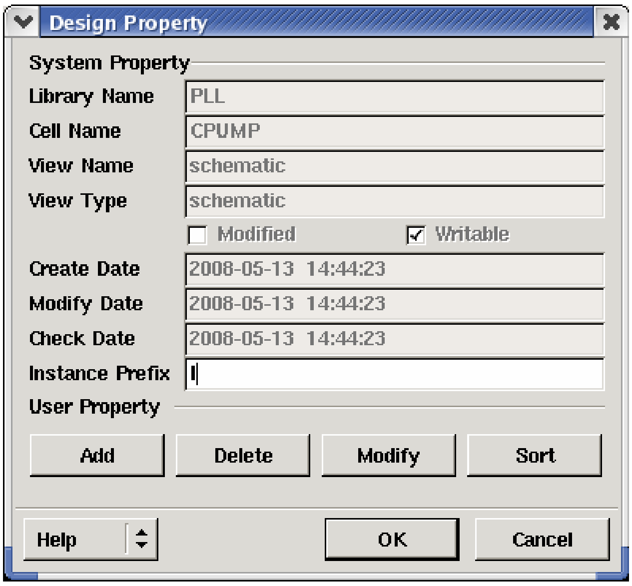
Library Name specifies the destination library name.
Cell Name specifies the destination cell name.
View Name specifies the destination view name.
Copy Component Property controls whether to copy the component property to new view.
Open To Edit controls whether SE opens the new view automatically after saving.

1.1.4 Design->Save All

Save all of opened views.

1.1.5 Design->Design Property

Display or edit property of the current cellview.

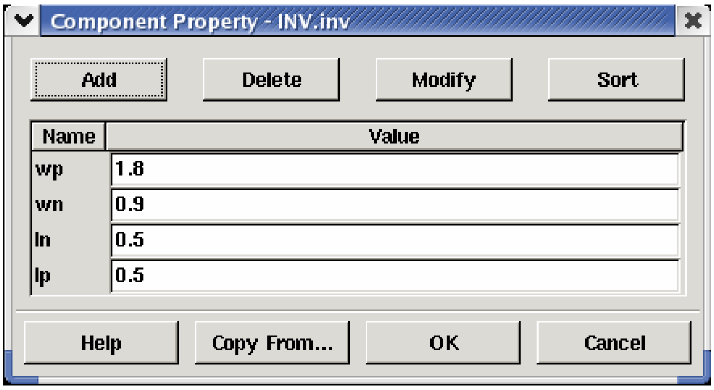


Instance Prefix specifies the prefix when current view is invoked by another view (Please refer to *Add->Instance* for details). The valid value is from 'A to 'Z'.

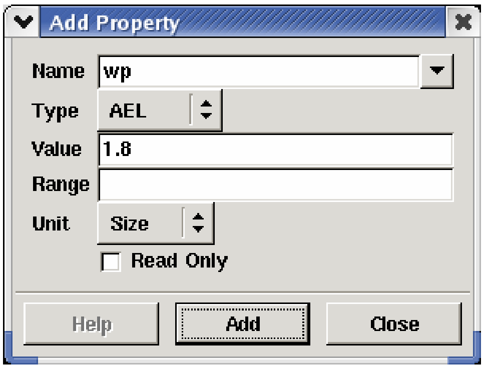
User property lets you add some properties for this cellview. Please refer to symbol editor: *design->property.*

1.1.6 Design->Component Property

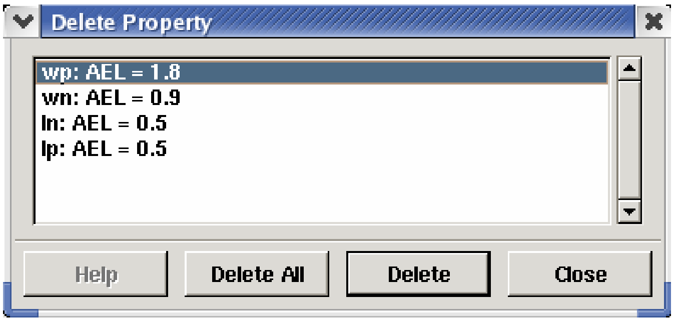
This command lets you add parameters to this cell as component parameters. When this cell is invoked by another cell, you can modify these parameters value according to different instantiation. A cell should have and only have a set of component parameters. So these parameters will be inherited by another schematic cellviews and symbol cellviews of this cell.



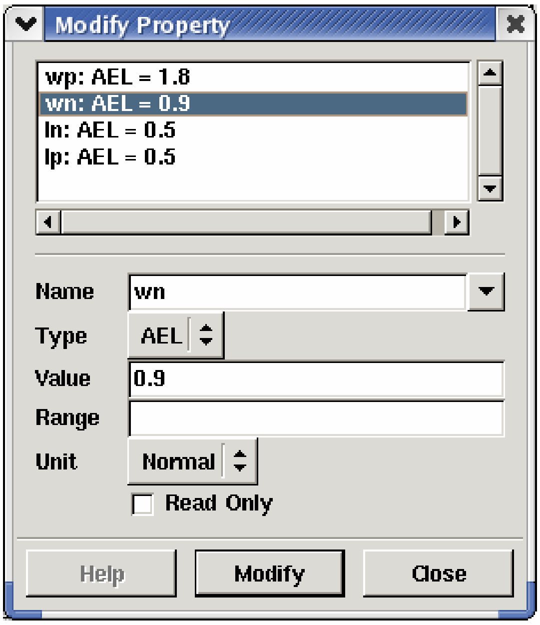
Add button lets you add a new property.



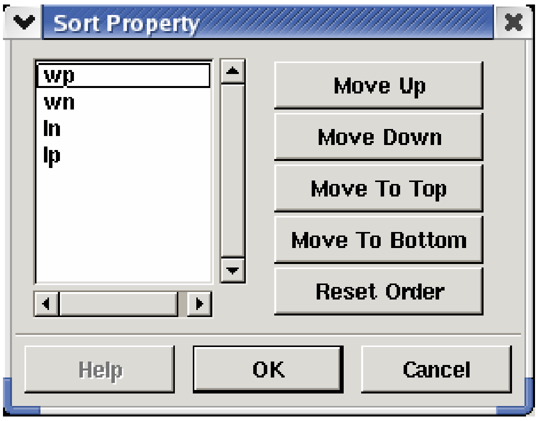
Delete button lets you delete property items



Modify button lets you modify this property value



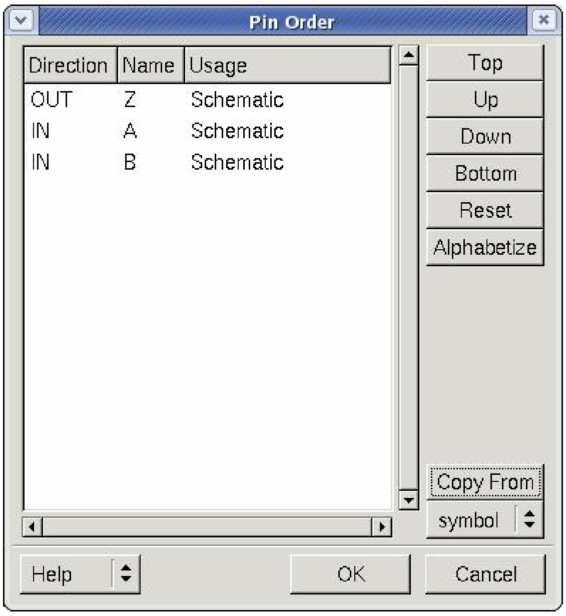
After modifying, click *Modify* to update the property.
Sort button lets you sort these properties.



Select an item and move its order by clicking *Move up*, *Move Down*, *Move To Top*, etc. Click *OK* button to get the newly order and update *Design Property* form.

1.1.7 Design->Pin Order

This command lists the order of pin. The order depends on the sequence of pin creation. You can modify the order by *Top*, *Up*, *Down*, *Bottom*, etc. Pin order in both Schematic Editor and Symbol Editor should be consistent.



Top moves the selected pin to the top of list.
Up moves selected pin to up level in list.
Down moves selected pin to down level in list.
Bottom moves selected pin to the bottom of list.
Reset restores default order.
Alphabetize sorts pins by alphabetize.
Copy From lets you copy the pins order from another view. Select a view name from *Copy From* dropdown list, and click *Copy From* button.

1.1.8 Design->Make Read Only/Make Editable

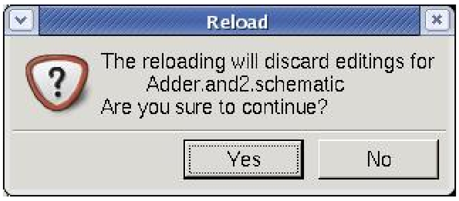
Make current view editable or read only.
Select *Design-> Make Editable* to make this view editable. At this time, you can find the command menu changes to *Make Read Only*.
Select *Design-> Make Read Only* to make this view read only. At this time, you can find the command menu changes to *Make Editable*.

1.1.9 Design->Discard Edits

To discard any modification since the design was saved last time. After doing this command, the commands Undo and Redo do not work.

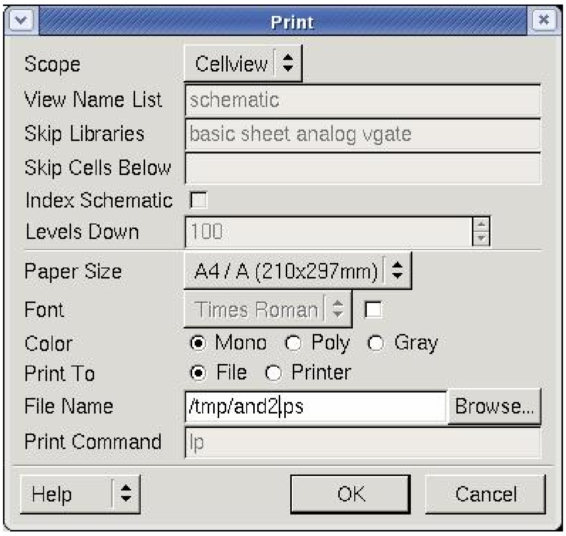
1.1.10 Design->Reload

Reload the design data from disk and refresh current view. It is useful for a project team to synchronize the design data.
If current view has already been modified, SE will pop up a form to inquire you want to continue discard modification or not before reloading.



1.1.11 Design->Print

Print current view to a printer or a postscript (.ps) file.



Scope specifies print scope.
Cellview prints current view in fit window view.
Hierarchy prints current view and its sub-cells.
Library prints all cellviews listed in *View Name List* in this library.
Window prints current view in current view state.
View Name List specifies the views you want to print. It is activated when you select *Library* from *Scope* drop-down list.
Skip Libraries specifies library list. View in this library will not be printed. It is activated when you select *Hierarchy* from *Scope* dropdown menu.
Skip Cells Below specifies to print subcells till this one specified here. It is activated when you select *Hierarchy* from *Scope* dropdown menu.
Index Schematic specifies whether to print Index Schematic or not.

Levels Down specifies how many levels in the design hierarchy to be printed. It is activated when you select *Hierarchy* from *Scope* dropdown menu.
Paper Size specifies the paper size, for example, A0-A5, B0-B5.
Font specifies output text font.
Color specifies printing color.
Mono -- monochrome
Poly -- colorful
Gray -- gray
Print To specifies printing to a ps file or to printer.
File specifies to print to a ps file, Type file name in *File Name* field.
Printer specifies print to printer. Type the print command in *Print Command* field.

1.1.12 Design->Close

Close the current cellview and exit the layout editor.
If the current cellview has been modified and not been saved, a dialog appears and enquire you whether to save it or not.

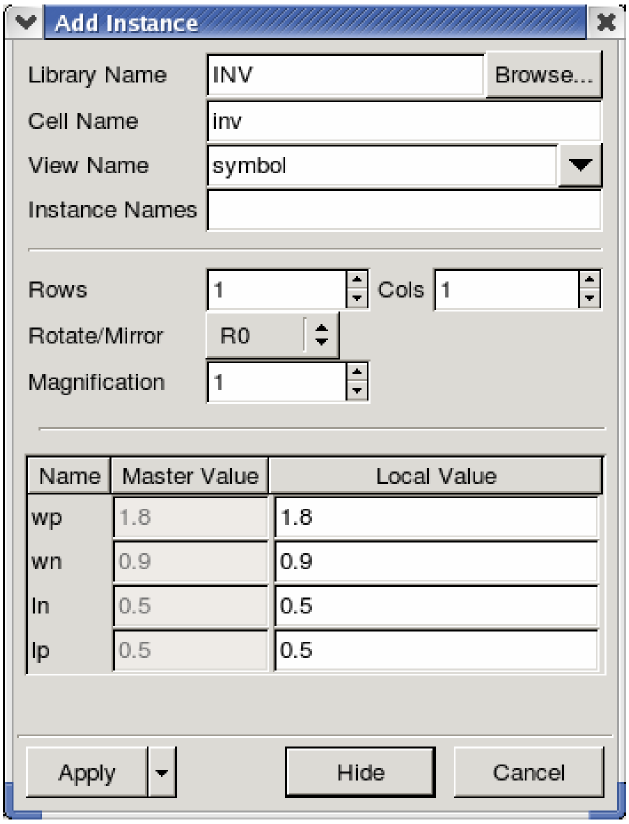
Click *Yes* to save it and exit SE. Otherwise, click *No* to exist SE without saving.

1.2 Add menu

1.2.1 Add->Instance

Place instance in your design.

Select *Add->Instance* or click icon , Add Instance form appears.



In **LibraryName**, **CellName**, and **ViewName** fields, specify the cellview of the instance.

You can also click at *Browse* button to assist you in finding the cellview you want to add.

If you do not add instance names in the **Instance Names** field, the system generates default instance names prefixed with the letter I.

Rotate/Mirror make the instance rotate.

R0/R90/R180/R270 - Rotate 0/90/180/270 degrees.

MX - Flip by X-axis.

MY - Flip by Y-axis.

MXR90 - Flip by X-axis and rotate 90 degrees.

MYR90 - Flip by Y-axis and rotate 90 degrees.

Magnification specifies enlarge instance by some times. The default value is 1.

Name. **Master Value**, **Local Value** are parameters related to the instance. You can give a set of new parameters in *Local Value* field to fit your design. If not, the instance's parameters will be the same as Master Value.

Methods of Adding Instances to Your Design:

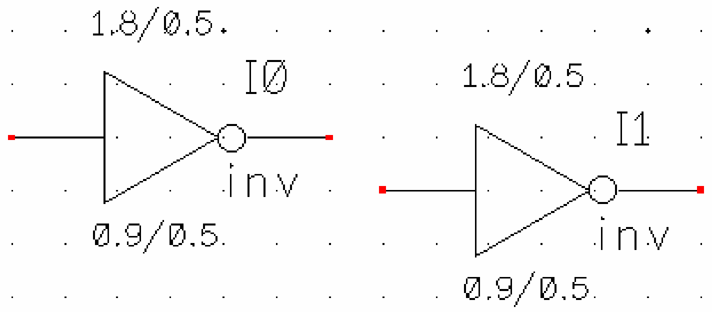
One by one

This method lets you place multiple copies of a single instance in a schematic, based on a single lib/cell/view name.

1. Choose Add – Instance;
2. In the Library, Cell, and View fields, specify the cellview of the instance;
3. Move the pointer into your cellview. The instance appears attached to the pointer. Click in your cellview to place the instance.

Note:

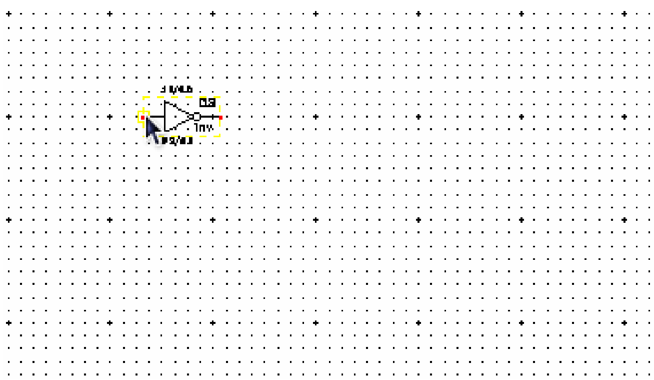
Add – Instance command is repeatable (if repeat mode is turned on), and continues to prompt you to add another instance. Please refer to *Options->Editor Command* field. To stop generating instances, press the Esc key, or choose another command.



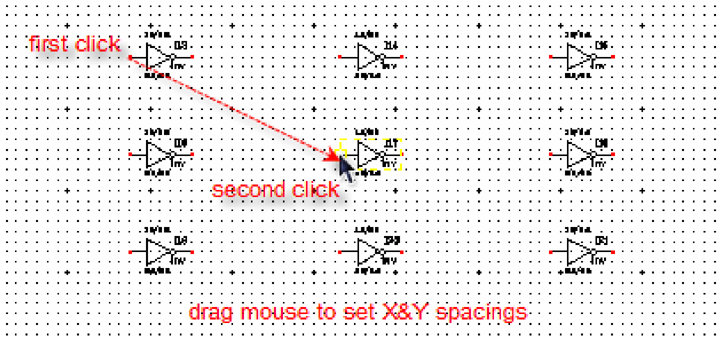
By rows and columns (an array)

Add an array of instance using rows and columns, do the following:

1. Choose Add – Instance.
2. In the Library, Cell, and View fields, specify the cellview of the instance. Fill in the Rows and Columns fields.
3. Move the pointer into your cellview. The first instance appears, attached to the pointer. Place the first instance by clicking the mouse.



4. Drag the mouse vertically and horizontally, and then click on a location to set the X and Y spacing for the array. The rest of the instances follow the cursor.



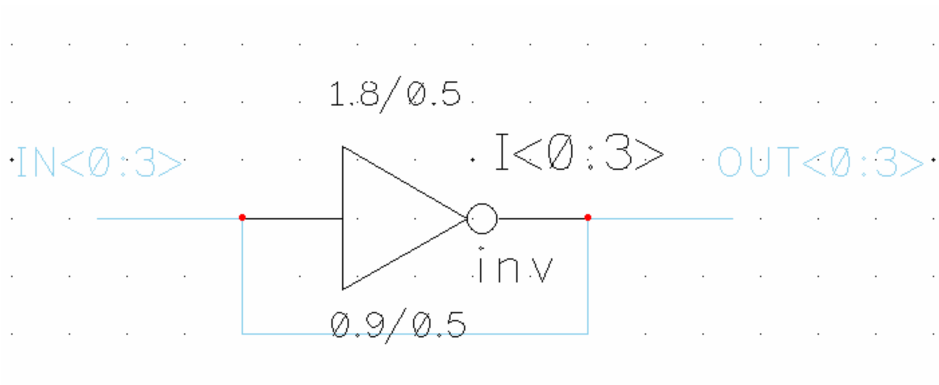
By using iterative expressions

Instance iteration is a compact way of displaying repeated instances of a symbol in your schematic. It is particularly useful in bus-type or data-flow architectures that have identical structures to handle each bit on the bus.

To save space in your design window when you need to add several instances of the same type, you can express multiple unique names with an iterative expression. For example, I<0:3> generates one graphic representing four instances: I0, I1, I2, and I3.

Add instances using an iterative expression, do the following:

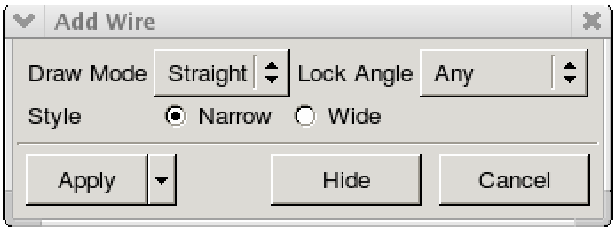
1. Choose Add – Instance.
2. Fill the form. In *nstance Names* field, type a name using iterative expression format such as I<0:3>.
3. Move the pointer into your cellview. The instance appears attached to the pointer. Click in your cellview to place the instance.



1.2.2Add->Wire

Add a wire in the current cellview.

Select *Add->Wire* or click icon  to add a wire. If you selected *Always* option in *Option->Popup Option Form* , or press "F3" key, the Add Wire form appears.



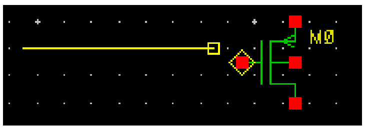
Set the form above, and then begin to draw wire in your schematic as the following steps:

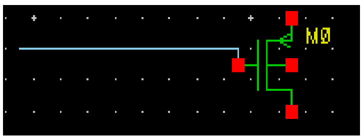
1. Click on a point to start drawing wire;
2. Drag mouse to the destination point and left click or double click anywhere to finish drawing wire.

If *option->Editor->Wire Snapping* is checked, the closest pin to mouse will be marked by a small diamond shape while drawing. Holding Shift or Ctrl and click LMB, the wire will connect to this closest pin automatically.

The snap marker appears when drawing

Holding Shift or Ctrl and clicking LMB, automatically connect to the closest pin





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Draw Mode specifies the wire entry method.

Straight (/): draw a straight line between two points on the following **Lock Angle** mode:

Any: any angle.

Orthogonal: 90 degrees angle.

Diagonal: 45 degrees angle.

XY (_|): draw line along X-axis first, then along Y-axis.

YX (|_): draws line along Y-axis first, then along X-axis.

L45 (_/): draw line along X-axis or Y-axis first, then along 45 degrees direction.

45L (_): draw line along 45 degrees direction, then along X-axis or Y-axis.

Route: route between 2 points by the following **Route Method**:

Full: draw line between two points at 90 degrees angle.

Direct: draws a straight line between two points at any angle.

Flight: draws a dotted line between two points at any angle.

Style specifies the wire width as below. If you select Wide option, Add Wire is the same as command Add Wide Wire.

1.2.3 Add->Wide Wire

Add a wide wire in the current cellview. It is the same as *Add->Wire*.

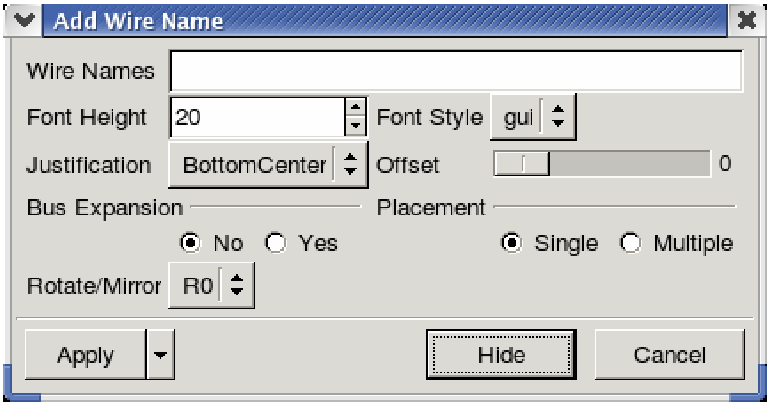
Note:

1. In *Options->Editor* menu, turn on “Always” in “Popup option form” option, Add Wire form will pop up all the time, without pressing “F3” key.
2. In *Options->Editor* menu, turn off “Wire Snapping” option, the small yellow diamond will not appear.
3. While creating a wire, you can right-click mouse to change the wire mode. If the “Add Wire” form still exists, the value of Draw Mode will be changed with each right-click mouse.

1.2.4 Add->Wire Name

Assign a name to a wire.

Select *Add->Wire Name* or click icon , the *Add Wire Name* form appears.



Wire Names specifies one or more names will be assigned to wires. You can specify multiple names, and separating each name by a space. You can also use a bus expression to name an array of wire names.
Font Height specifies the size of your wire name text as a floating-point value, in user units. The default is 0.625.
Font Style specifies the typeface that system uses to display the wire name.
Justification specifies the position of the cursor with respect to the wire name.
Offset specifies the distance between the text *Justification* and the anchor (cursor). Notice that when you select *"Center Left"*, *"Center Center"* or *"Center Right"* in

Justification, *Offset* is invalid.

Bus Expansion specifies how the system interprets bus names.

No (default) interprets the bus name as a single name and generates a single name that includes all the bits in the bus range. For example, for the name A<0:1>, the system generates only the name A<0:1>.

Yes interprets the bus name as multiple names and generates a name for each bit of a bus range that you specify in the Names field. For example, for the name A<0:1>, the system generates names A<0> and A<1>.

Placement controls whether you can place multiple wire names automatically once.

Single (default) requires you to point and click to identify each wire name location.

Multiple lets you drag your mouse between two points to designate the wires that you want to name automatically.

Rotate/Mirror specify how to rotate the wire name.

R0/R90/R180/R270: rotate wire name by 0/90/180/270 degrees

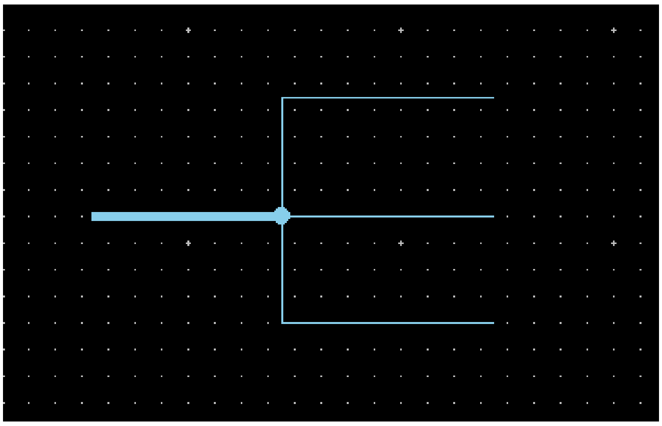
MX: flip wire name by X-axis

MY: flip wire name by Y-axis

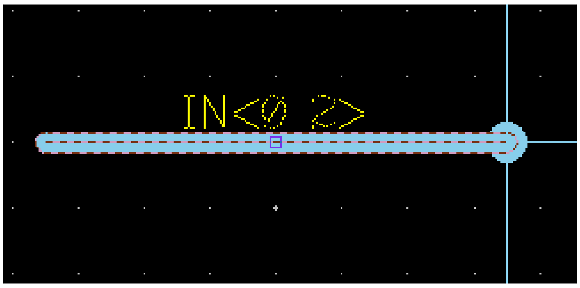
MXR90: flip wire name by X-axis and rotate 90 degrees

MYR90: flip wire name by Y-axis and rotate 90 degrees

Add wire names one by one for the following figure:



1. Click icon, fill out the Add Wire Name form with the following information.
   Wire Names: IN<0:2>
   Bus Expansion: No
   Placement: Single
2. Directly move your cursor into the wire segment as the figure below. Click left mouse button to add the wire name to this wire segment.

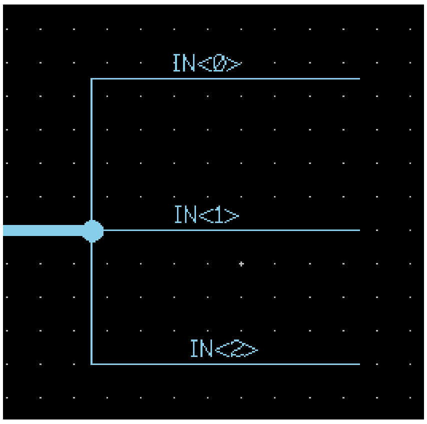


3. Choose Add->Wire Name

4. Move your cursor into “Add Wire Name” form, fill out name, like “IN<0:2>” in Wire Names field and set the option Bus Expansion to “Yes”.

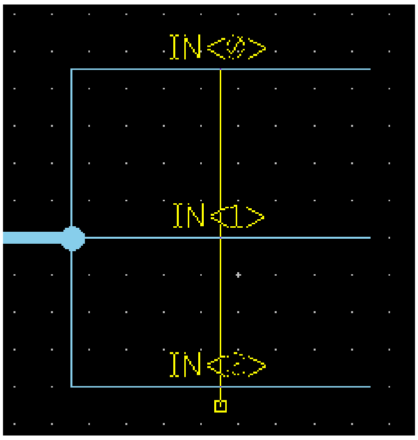
5. Directly move your cursor into Schematic Editor window. Click left mouse button to add the wire name to these tree wire segment one by one.

带格式的：项目符号和编号



Add names for bus:

1. Click icon  again, fill out the Add Wire Name form with the following information.
   Wire Names: IN<0:2>
   Bus Expansion: Yes
   Placement: Multiple
2. Hide the “Add Wire Name” form, move mouse to the first wire segment and click left mouse button to fix it.
3. Drag and move the cursor cross the other two wire segments. You can find the other names IN<1> and IN<2> appear in the cross point automatically as shown in the figure below.



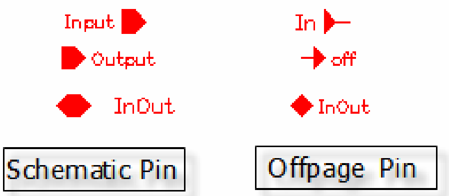
4. Click left mouse button to fix them.
5. Save and close this schematic view.

 Note:

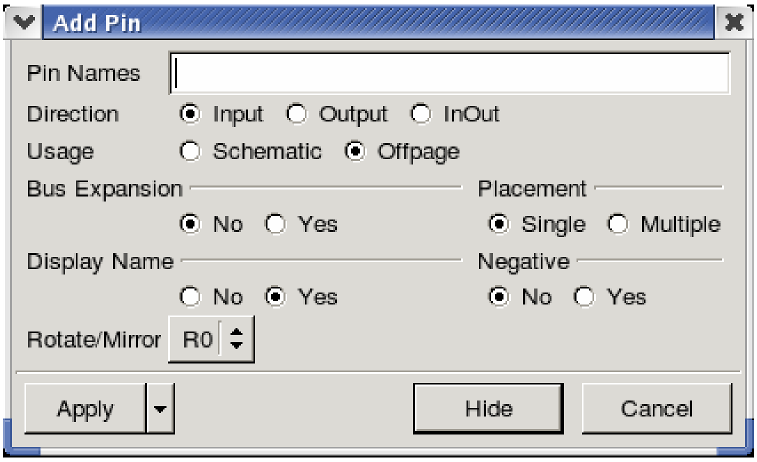
To do this operation successfully, you must make sure that “Repeat” option is turned on in Command field of menu command *Options->Editor*.

1.2.5Add->Pin

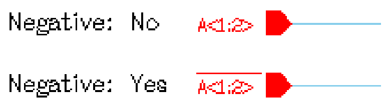
Create schematic pin or Offpage pin.
Schematic pin is an interface of input or output data in cellview. Offpage pin is as a connector connects pages. Please refer to *Page* menu.
The shape of schematic pin and Offpage pin are shown as below.



Select *Add->Pin* or click icon , the Add Pin form appears.



Pin Names specifies the pin name. It can be single pin and multiple pins. For multiple pin names, use "space" to separate names or use bus expression (for example: A<0:x>, x is digit).
Direction specifies pin type: Input, Output or InOut.
Usage specifies this pin is used for schematic pin or page connector in multi-page schematic.
Bus Expansion specifies how the system interprets bus names.
No (default) causes the system to interpret a bus name as a single name and generate a single pin that includes all the bits in the bus range. For example, for the name A<0:1>, the system generates only the pin A<0:1>.
Yes causes the system to interpret a bus name as multiple names and generate a pin for each bit of a bus range that you specify in the Pin Names field. For example, for the pin A<0:1>, the system generates pins A<0> and A<1>.
Placement controls whether you can place multiple pins automatically in one operation.
Single (default) requires you to point and click to identify the location for each pin.
Multiple prompts you to point and click to specify the first and second pin locations.
Negative specifies pin logic. If you select *Yes*, an bar is on the top of pin name.



Display Name specifies whether pin name is visible or invisible.
Rotate/Mirror is to rotate the pin name.
R0/R90/R180/R270: rotate pin name by R0/R90/R180/R270 degrees.
MX: flip pin name by X-axis
MY: flip pin name by Y-axis
MXR90: flip pin name by X-axis and rotate 90 degrees
MYR90: flip pin name by Y-axis and rotate 90 degrees

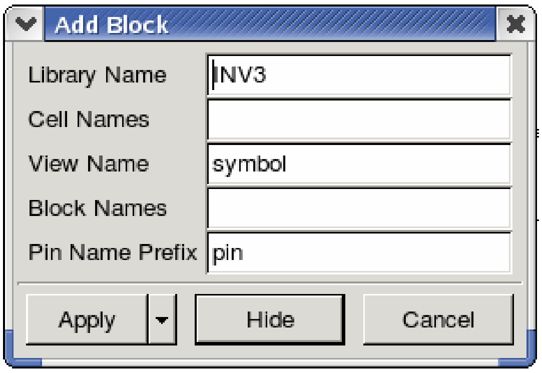
Note:

You can right-click mouse to rotate pin before you place the pin.

1.2.6Add->Block

Create a block. This method is used for design method of Top-Down.

Select *Add->Block* or click icon , the Add Block form appears.



Enter library/cell/view names in *Library Name*, *Cell Name* and *View Name* fields. In fact, SE will create a symbol view after you click *Apply* button.

Block Names specifies the block name, which is instance name. If not giving any name, "I" is as the default.

Pin Name Prefix specifies the prefix of pin name when wire connects to block editor creates a pin automatically. The default prefix is "pin".

After filling up all fields and clicking Apply button, you can start to create this block. The steps are as below:

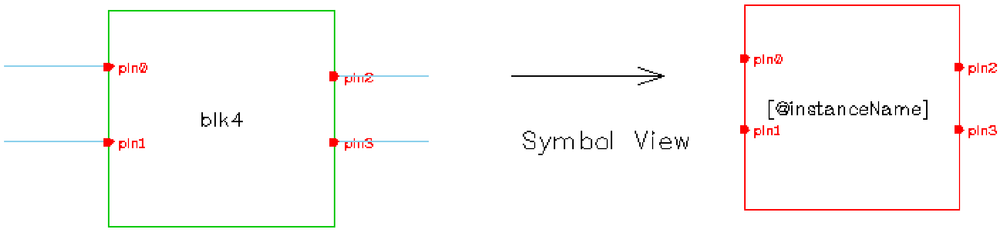
1. Move the cursor in editor window
2. Click the first point to locate the top-left corner of the rectangle
3. Drag the mouse and click the second point to locate the bottom-right corner of the rectangle.

Create Block Pin Automatically

After creating a block, you can add pin to block automatically. The steps are as below:

1. Activate *Add Wire* or *Add Wide Wire* command first.
2. Draw a wire to or from block edge.
3. Click on a point to end the wire.

The created entire block and its symbol view are as following.



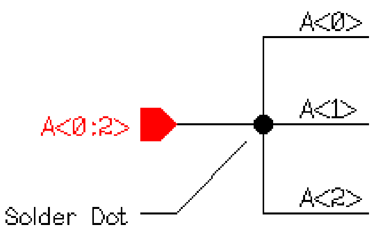
 Note:

The library that you type in Library Name field must be existed.
The symbol view that you type in View Name field must not be existed.
Block pin's direction is controlled by Option->Editor->Block Pin Order .
If you checked Freezed Pin Add in *Design->Property*, in block symbol view, you will not add pin automatically.

1.2.7Add->Solder Dot

When two wires cross like "+" shape, you need to manually add a solder dot at the intersection in order to connect two crossing wires.

Select *Add->Solder Dot* or click icon , and click at cross point.



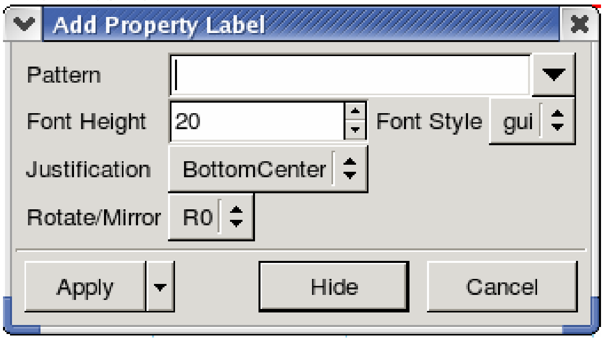
To delete a solder dot, select *Edit->Delete* or click icon , click at the solder dot you want to delete.

 **Note**:

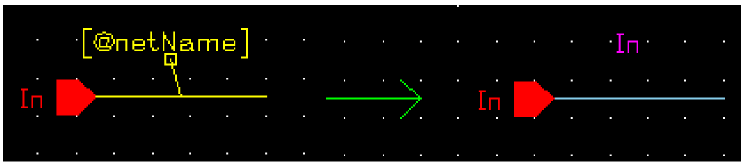
When two wires cross like "T" shape, the editor adds a solder dot at the intersection point automatically.
To remove anyone wire in "T" structure, the solder dot is deleted by editor.

1.2.8 Add->Property Label

Create a property label for an object.
Select *Add->Property Label* first, the Add Property Label form appears. Click to choose an object (wire, pin, instance, etc.) on layout, then the *Pattern* field is valid according to the object type you choose.



Pattern specifies the label pattern or a user given name. According to difference object, the label is different in pull-down menu list. For example, if you select a wire, the candidate label is "[@NetName]", "[@NetName]" specifies the current selected wire's name. If the name of this wire is changed, the label will be changed as well after *check* operation.
Font Height specifies the size of the label. Default is 20.
Font Style specifies the style of label.
Justification specifies the anchor of text.
Rotate to rotate the label.
R0/R90/R180/R270: rotate label by 0/90/180/270 degrees.
MX: flip label by X- axis.
MY: flip label by Y-axis.
MXR90: flip label by X-axis and rotate 90 degrees.
MYR90: flip label by Y-axis and rotate 90 degrees.
After setting the label, move cursor to editor window, the selected object highlights and a line attached label start from the selected object. Click a point to place the label at the desired location.

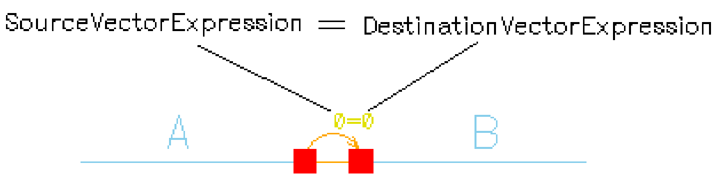


Note:

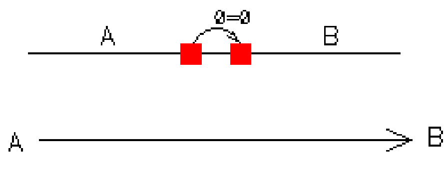
Do check operation before doing this command.

1.2.9 Add->Patchcord

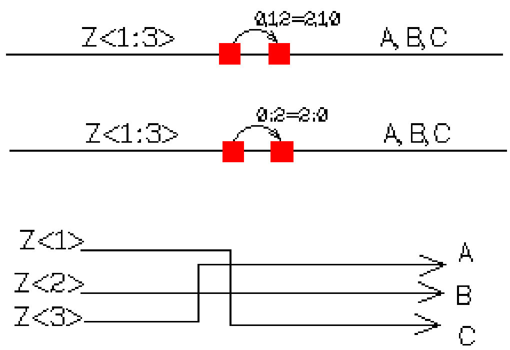
Patchcord is a connection symbol used to establish aliases between the signals of two different nets.
You can use the patchcord to map bits from one net to different bits of another net.
The patchcord connects wires in format: Source Vector Expression = Destination Vector Expression



The vector expression syntax is:
single bit: for example: "0=0" "2=2" "3=4"
multiple bits: for example: "0:2=2:4" "0,1,3= 2,3,4"
The number of bits in SourceVectorExpression must equal to the number of bits in DestionVectorExpression
In the following example, net "A" and net "B" are aliased together.

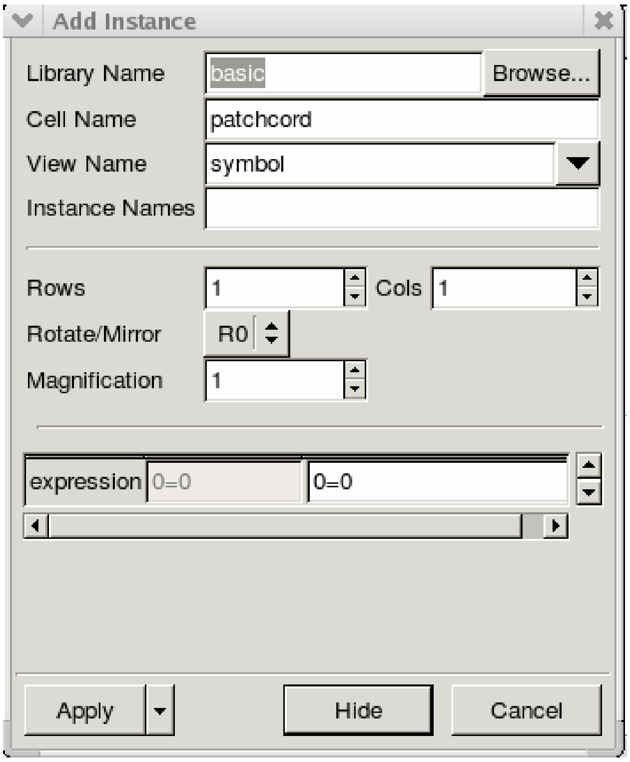


In the following example, no matter the expression is "0,1,2=2,1,0" or "0:2=2:0", the results are same, that is, signal "Z<1>" is aliased to signal "C", signal "Z<2>" is aliased to signal "B", signal Z<3> is aliased to signal "A".



Add a patchcord in your design as below:

Select Add->Patchcord or click icon, the Add Instance form appears.



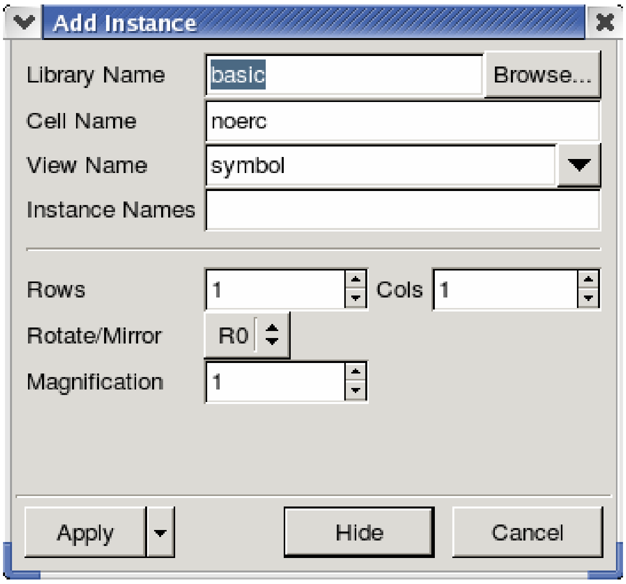
Enter vector expression in *expression*, for example: "0=1", "1=0" or "0:3=0:3", etc. The system puts 0=0 in the *expression* field, which indicates that the nets are equal to or greater than 1 bit wide. If the nets are more than 1 bit wide, you can update the expression value on the Add Instance form.

Move the cursor to editor window, the patchcord symbol attached to the cursor, click to place the patchcord at the desired location.

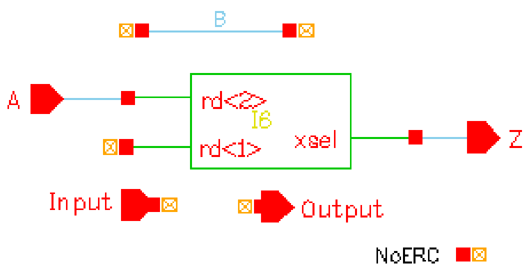
1.2.10 Add->NoERC

Used for floating nets and floating pins are not be checked by ERC.

Select *Add->NoERC*, the Add Instance form appears.

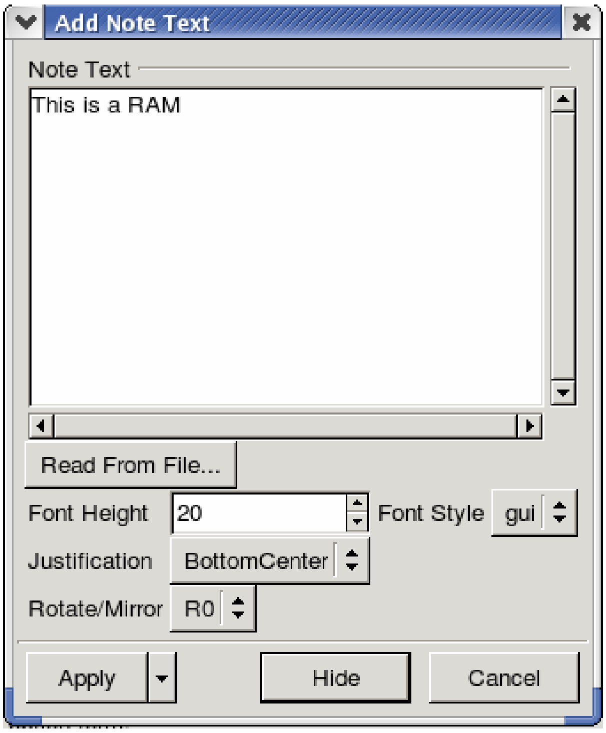


The NoERC form is filled automatically. Move the cursor to editor window, the NoERC symbol attached to the cursor, click to place NoERC at the desire location.
In the following example, the net "B", instance pin "rd<1>", pins "Input", "Output" will not be regard as floating while do ERC check.



1.2.11 Add->Note Text

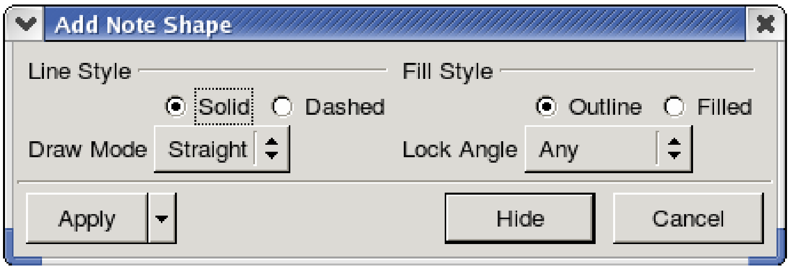
Add comments for an object or for entire schematic/symbol view.
Select *Add->Note* Text, the Add Note Text form appears.



Note Text field is used to edit the text you want to add. You still can load a note text in some file by Read From File button.
Font Height specifies the size of note text. Default is 20.
Font Style specifies the font style.
Justification specifies the anchor of note text.
Rotate/Mirror to rotate the text.
R0/R90/R180/R270: rotate text by 0/90/180/270 degrees.
MX: flip text by X-axis.
MY: flip text by Y-axis.
MXR90: flip text by X-axis and rotate 90 degrees.
MYR90: flip text by Y-axis and rotate 90 degrees.

1.2.12 Add->Note Shape

Add graphical notes to the schematic.
There are 6 note shapes that you can choose: Rectangle, Line, Polygon, Circle, Ellipse and Arc.
Select one of shapes from submenu of command *Add->Note Shape*, the Add Note Shape form appear according to the shape you choose.



Line Style section， you can choose the shape of outline is Solid line or dashed line.
Fill Style section, you can decide whether to fill the shape.
Draw Mode specifies the drawing mode:
Straight(/): draw a straight between two points
XY(_|): draw along X-axis first, then along Y-axis
YX(|_): draw along Y-axis, then along X-axis
L45(_/): draw along X-axis or Y-axis first, then at 45 degrees to the axis
45L(_): draw at 45 degrees to axis first, then along X-axis or Y-axis
Lock Angle specifies the angle while drawing line.
Any (Default): at any angle
Diagonal: at 90-degrees angle to the axes
Orthogonal: at 45-degree angle to the axes

1.3 Edit menu

1.3.1 Edit->Undo

Reverse the action of the pervious edit command. You can set the undo limit from 0 to 100 in *Option->Editor->Undo Limit*.

Select *Edit->Undo* or click icon  to do it.

 Note:

After you doing *Check and Save* , *Save*, *Check* or *Discard Edits* commands, this command does not work.

1.3.2 Edit->Redo

To cancel the previous undo commands. Select *Edit->Redo* or click icon  to do it.

1.3.3Edit->Stretch

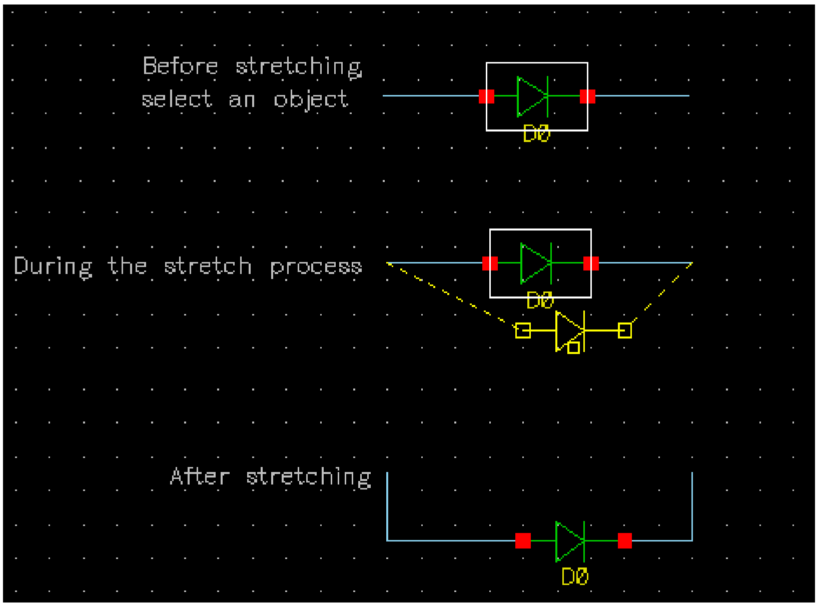
Move the selected object to another location without losing connectivity between wires and pins.

To stretch an object, do the following:

1. Select an object first.
2. Choose Edit->Stretch or click icon .
3. Click the selected object and hold LMB.
4. Drag the LMB and release it at the desired location to complete the stretch.

The editor reroutes wires to maintain connectivity.

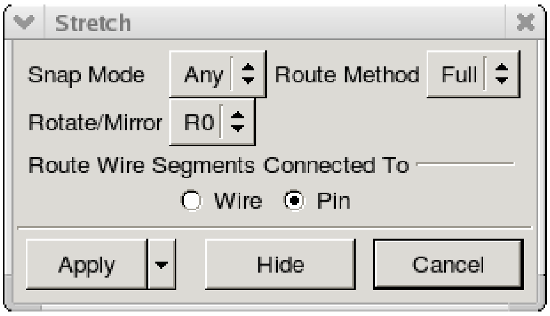
The following figure shows the stretch process.



To stretch multiple objects, you need to press Shift key while selecting objects. After activating Stretch command, you just select one object only to stretch, and then the remains are stretched at the meanwhile.

About the Stretch form:

When you activate stretch command, the Stretch form appears.



Snap Mode specifies the angles along which you can move stretched objects.

Any (default) - move stretched objects along any angle.

Diagonal - move stretched objects along 45-degree, 90-degree, and 180-degree angles from the current location.

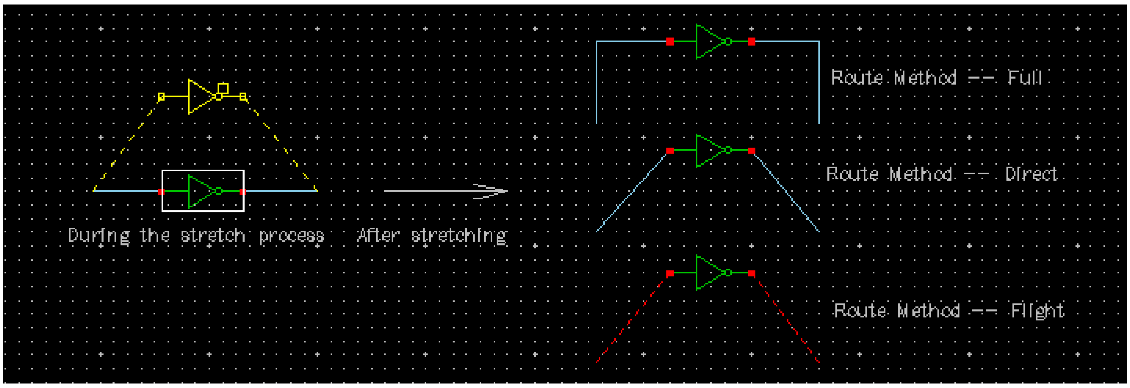
Orthogonal - move stretched objects along the X and Y axes from current location.

Route Method specifies how the editor routes wire.

Full - automatically routing by editor.

Direct -- draw a straight line between two points.

Flight -- draw a dashed line between two points.



Rotate/Mirror to rotate the stretched objects during the stretch process.

R0/R90/R180/R270 - rotate objects 0/90/180/270 degrees.

MX - flip objects by X-axis.

MY - flip objects by Y-axis.

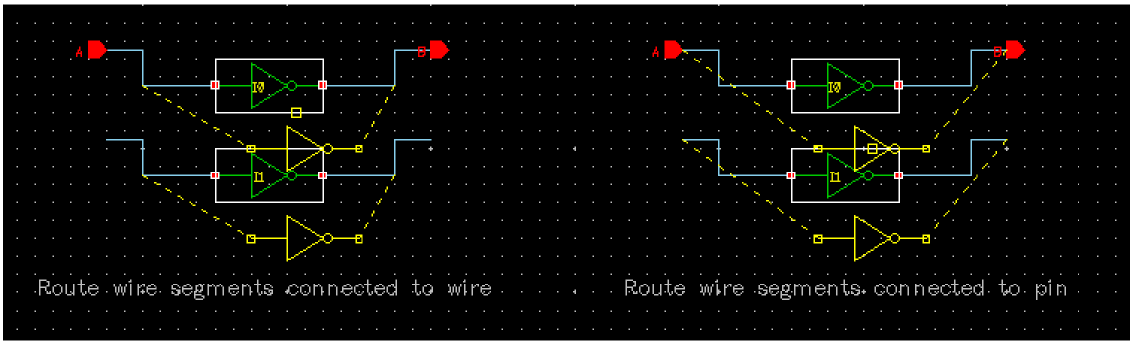
MXR90 - flip objects by X-axis and rotate 90 degrees.

MYR90 - flip objects by Y-axis and rotate 90 degrees.

Route Wire Segments Connected To specifies the point that rubberband line begin from.

Wire - the rubberband line begin from the last segment of the wires

Pin - the rubberband line begin from a pin, a solder dot, or a wire ending.



 Note:

The stretch command does not stretch objects from one cellview to another.

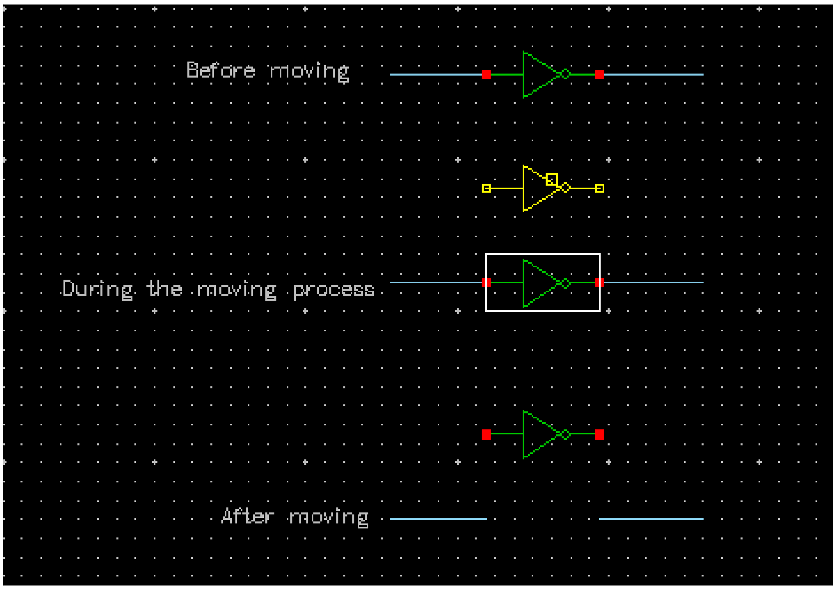
1.3.4Edit->Move

Move the selected objects to another location or cellview without keeping the connectivity between wires and pins.

To move an object, do as the following steps:

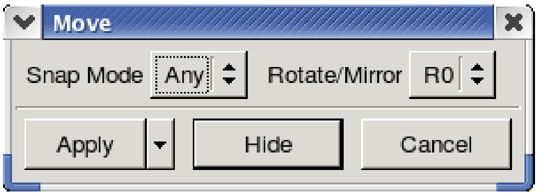
1. Select an object first.
2. Choose Edit->Move or click icon .
3. Click the selected object and hold LMB.
4. Drag the LMB and release it at the desired location to complete the move.

The following figure shows the moving process.



To move multiple objects, you need to press Shift key while selecting objects. After

activating Move command, you just select one of the objects only and move, the remains are moved at the meanwhile.
About the Move form:
When you activate move command, the Move form appears.



Snap Mode specifies the angles along which you can move objects.
Any (default) - move objects along any angle.
Diagonal - move objects along 45-degree, 90-degree, and 180-degree angles from the current location.
Orthogonal - move objects along the X and Y axes from current location.
Rotate/Mirror to rotate the moved objects during moving process.
R0/R90/R180/R270 - rotate objects 0/90/180/270 degrees.
MX - flip objects by X-axis.
MY - flip objects by Y-axis.
MXR90 - flip objects by X-axis and rotate 90 degrees.
MYR90 - flip objects by Y-axis and rotate 90 degrees.

 **Note:**

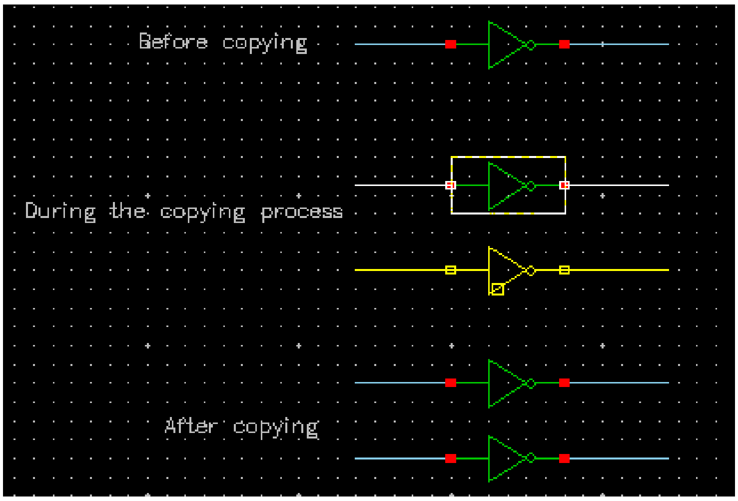
1. Move command can move objects from one cellview to another.
2. You can right-click mouse to rotate object before you place it.

1.3.5Edit->Copy

Copy objects in current cellview or to another cellview.
Copy an object, do the following steps:

1. Select an object first.
2. Choose Edit->Copy or click icon.
3. Click the selected object and hold LMB.
4. Drag the LMB and release it at the desired location to complete the copy.

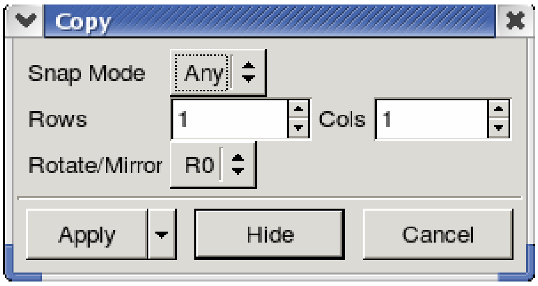
The following figure shows the copy process.



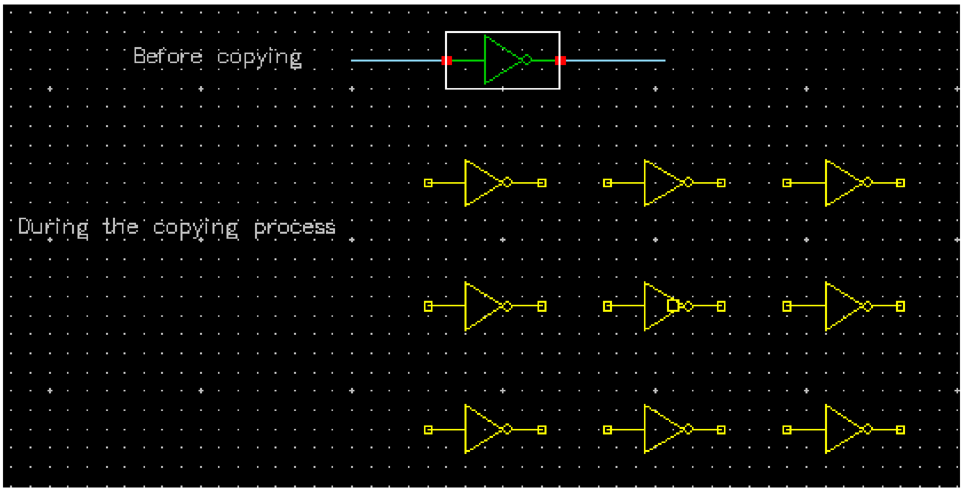
Copy multiple objects, you need to press Shift key while selecting objects, or draw a box to select objects you want to copy. After activating Copy command, you just select one of the objects to copy; the remains are copied at the meanwhile.

Copy one object to an array.

When you activate Copy command, the Copy form appears.



Rows and Cols let you copy object to make an array. For example, the following figure shows copying an instance to make a 3x3 array objects.



Make an array of objects, do as the following steps:

1. Select objects you want to copy.
2. Choose Edit->Copy or click icon .
3. Click to place the first copied objects
4. Click again to place all the other copied objects.

The editor uses the distance between the first click and the second click to determine the distance between objects.

 Note:

Copy command can copy objects from one cellview to another.

1.3.6Edit->Delete

Delete objects.

Select Edit->Delete, or press Del key, or click icon  to delete.

Usage1: Select Objects First (Pre-Selection)

You can select objects before you activate the Delete command. The Delete command ends after the selected objects are deleted.

Usage2: Select Command First (Post-Selection)

You can activate Delete command first before you delete objects. The Delete command can delete more objects by clicking at the objects. Press ESC key to end the Delete command.

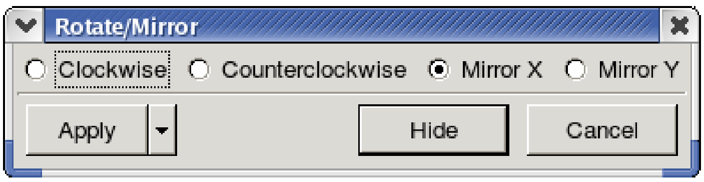
 Note:

Delete Sheet Border, you should select *Page->Add Sheet*, and then choose NONE from pull-down menu of *Sheet Name*.

1.3.7Edit->Rotate

Rotate object clockwise, counterclockwise, sideways, and upside down.

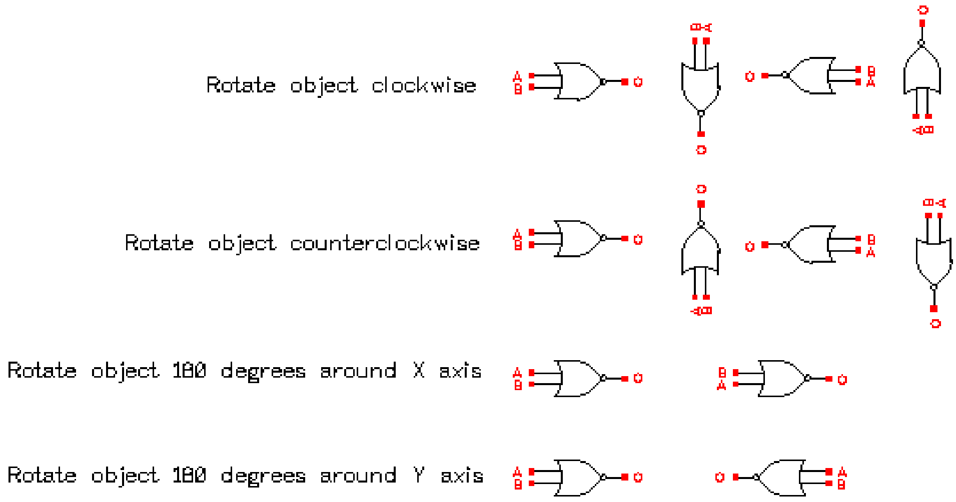
You can activate command Edit->Rotate first, or select objects first. Click at the object you want to rotate, the editor rotates the object counterclockwise. Press F3 key to modify the rotate mode.



Clockwise rotate object by 90 degrees increments clockwise.

Counterclockwise rotate object by 90 degrees increments counterclockwise.

Mirror X rotate objects 180 degrees around X axis.
Mirror Y rotate objects 180 degrees around Y axis.

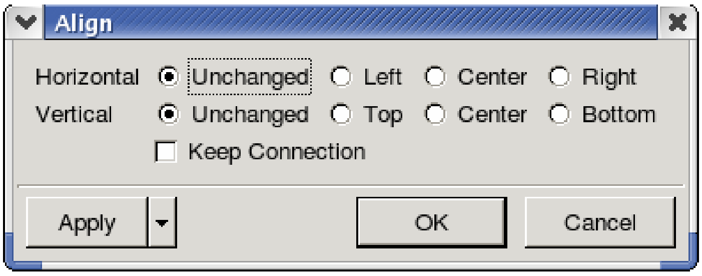


To rotate pre-selected objects, do the following steps:
1. Select objects first.
2. Click Edit->Rotate.
3. Point at a reference point around the objects.
4. Left-click mouse time by time to rotate objects.
5. Press “Esc” key to terminate the command.

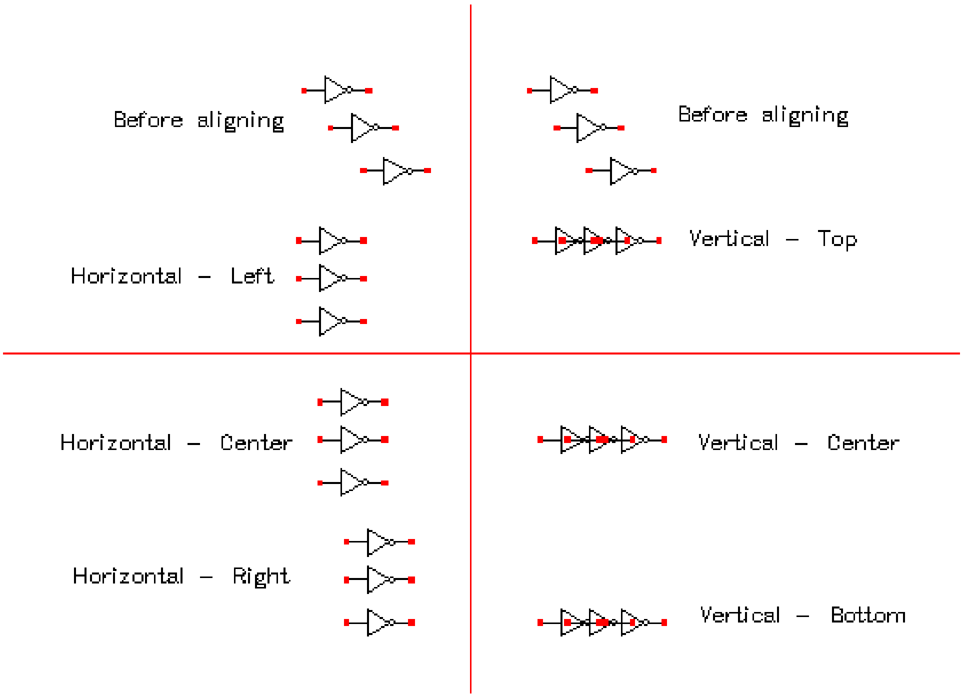
To rotate post-selected objects, do the following steps:
1. Click Edit->Rotate.
2. Select objects.
3. Point at a reference point around the object.
4. Left-click mouse time by time to rotate objects.
5. Press “Esc” key to terminate the command.

1.3.8Edit->Align

Align objects in horizontal or (and) vertical direction.
Select the objects you want to align first, choose Edit->Align, the Align form appears.

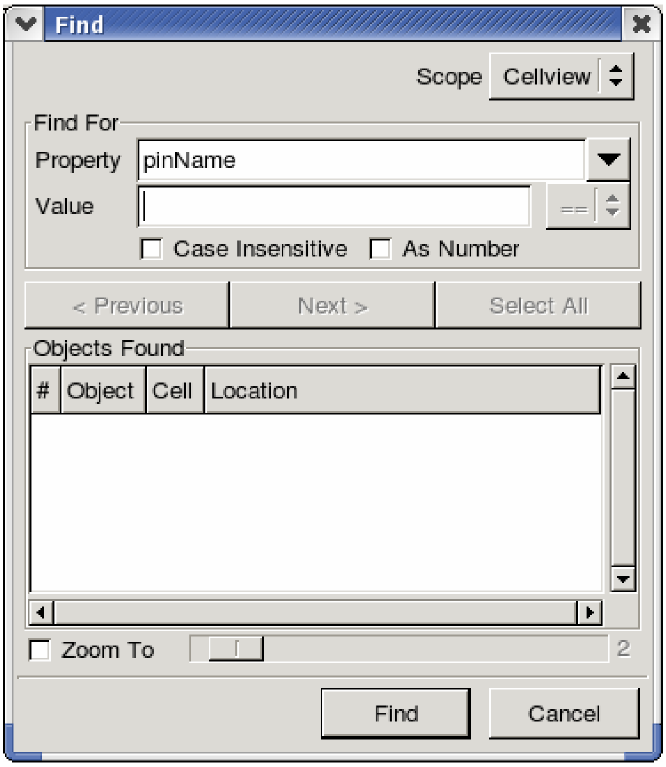


You can select align mode in *Horizontal* and *Vertical* direction, and select Keep Connection if you want to align with keeping connectivity.



1.3.9Edit->Find

Search objects with a specific property.
Select *Edit->Find*, the Find form appears.



Scope specifies searching scope. There are 3 options that you can choose: *Cellview, Hierarchy and Library*.

If you choose *Cellview*, the editor searches objects in the current cellview.

If you choose *Hierarchy*, the editor searches objects from all cellviews specified in the design hierarchy.

If you choose *Library*, the editor searches objects from all cellviews in the library.

Property specifies the object property you want to search. There are 7 object's property : instanceName, netName, pinName, wireName, libraryName, cellName and Orient.

Value specifies the value of the property. If you leave it blank or key in asterisk (*), the editor will search all objects that match the property.

Objects Found shows the result of all objects that been found. You can use *Previous, Next,* and *Select All* to select any item.

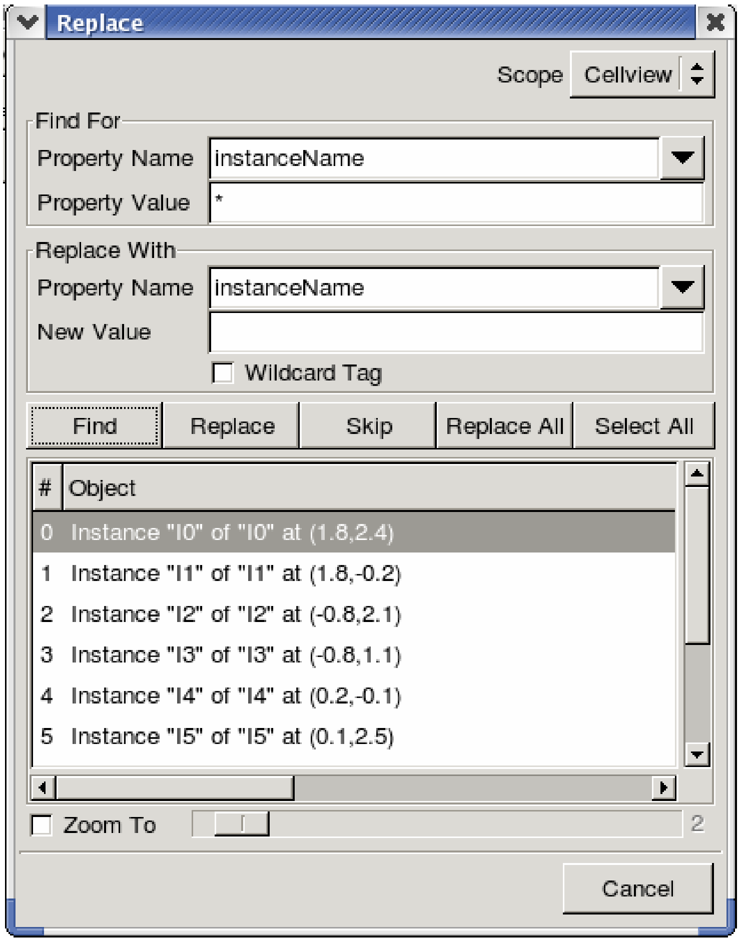
Double click at a selected item, the object will be shown on the cellview. If the object belongs to another cellview, the editor will open that cellview and show the object in it.

If you select *Zoom To*, the object will be magnified and shown on the center of the cellview.

1.3.10 Edit->Replace

Replace objects or replace property of an object.

Select *Edit->Replace*, the Replace form appears.



Find For field specifies *Property Name* and *Property Value* that you want to replace.
Replace With field specifies *Property Name* and a *New Value* that you use to replace.
Object field lists the objects that have been found by *Find* button, and then will be replaced by *Replace* or *Replace All* button.

1.3.11 Edit->Alternate View

A schematic view could have more then one symbol views, for example Symblo1, Symblo2 ... When Symbol1 view is referenced, and you can use this command to change the Symbol1 view to Symbol2 view if you need.
Select Edit->Alternate View first, or select an instance first, the difference symbol view is shown when you click at the instance continuously.

1.3.12 Edit->Renumber Instance

Assign new numbers to all of the instances in the current cellview.

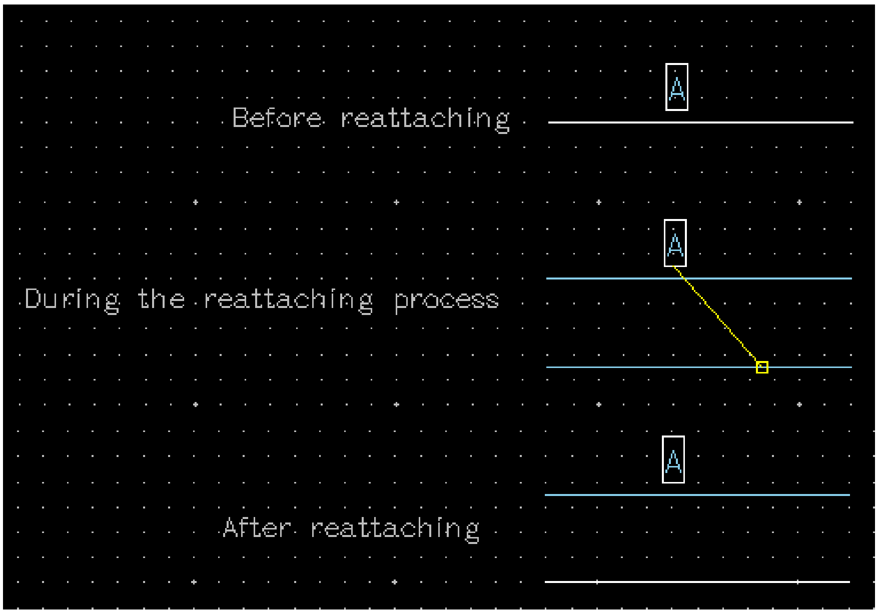
Select Edit->Renumber Instance to reset all of the instance names automatically.

Note:

If the prefix name of an instance is different from the prefix defined in *Design->Design Property->Instance Prefix* field, system doesn't renumber it.

1.3.13 Edit->Reattach Wire Name

Re-assign a wire name to another wire.
If you select Edit->Reattach Wire Name first, and then you select a wire name, a cartoon line from the wire name appears and attach to the cursor.
If you select a wire name first, and then you activate command Edit->Reattach Wire Name, a cartoon line from wire name appears and attach to the cursor.
Click at another wire, the net name is reattached to that wire.



Note:

Double click at a wire; the corresponding wire name is highlighted.
Double click at a wire name, the corresponding wire is highlighted.

1.3.14 Edit->Hide Label

Make label invisible.
Select Edit->Hide Label first, click at the label you want to hide, the label is invisible immediately. You can click at the labels to hide one by one until you press Esc key.

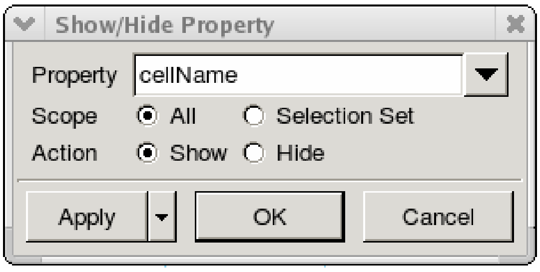
Set the label visible by *Reset-> Invisible Label*.

1.3.15 Reset Invisible Label

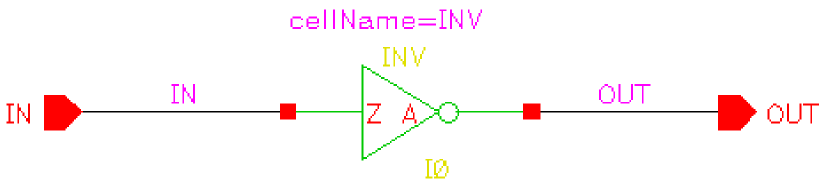
Make the hidden labels visible.
Select Edit->Reset Invisible Label first, all hidden labels will flash in the cellview. Click at a flashed label you want to be visible, the label will be displayed in the cellview immediately. You can click at labels one by one until you press Esc key.

1.3.16 Edit->Show/Hide Property

Show or hide object property.
Select Edit->Show/Hide Property, the Show/Hide Property form appears.



Fill property name in *Property* field, or select a property from drop down list.
You can show or hide properties either all of objects or one of objects you selected.
For example, in the below figure, the magenta text is property value.

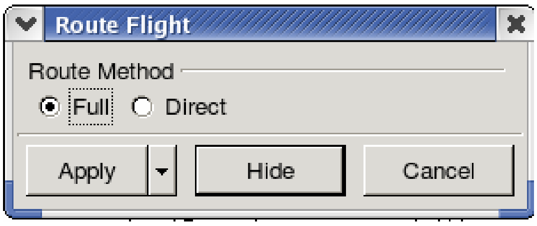


Note:

Please do *check* option after Show/Hide Property to show net name.

1.3.17 Edit->Route Flight

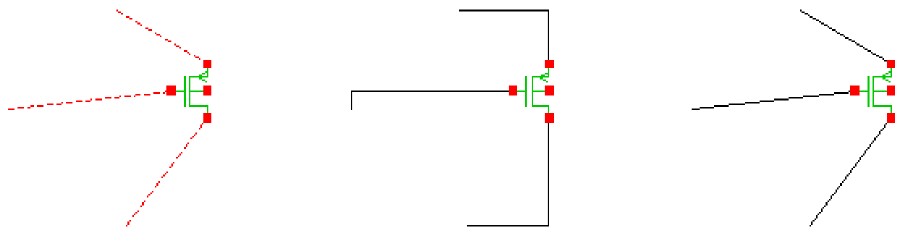
Route wires between two given points.
Select Edit->Route Flight first, click at a flight line to route wires.
You can press F3 key to change *Route Method* in the Route Flight form.



Route Method

Full Automatically route wires by editor. Sometime, the editor cannot route wires successfully, the dashed line remains there.

Direct Draw a direct line between two given points.

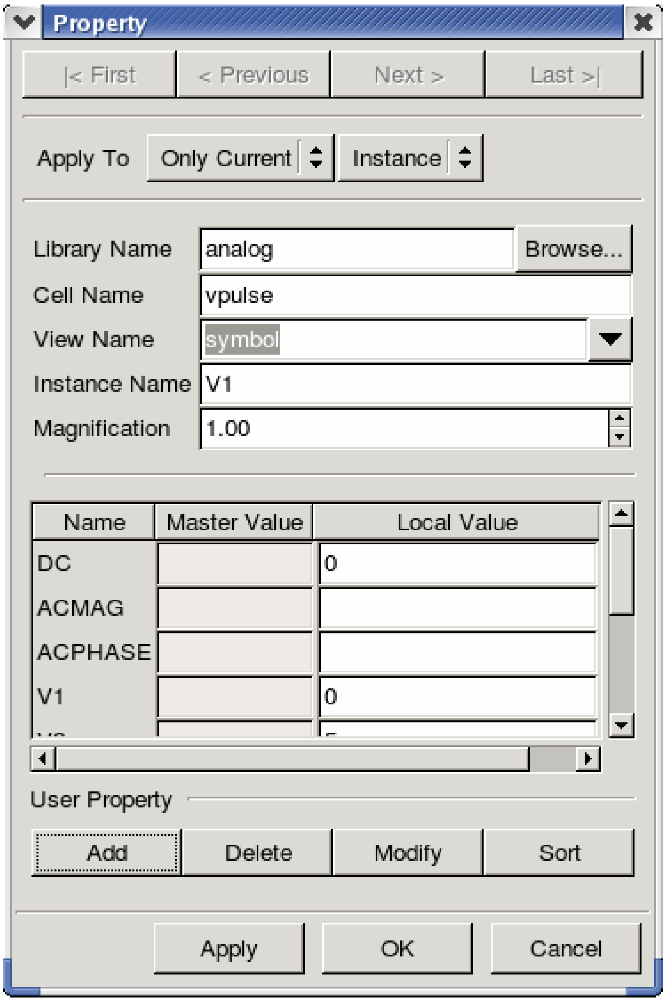


Flight line   Full -- auto route wires   Direct -- direct line

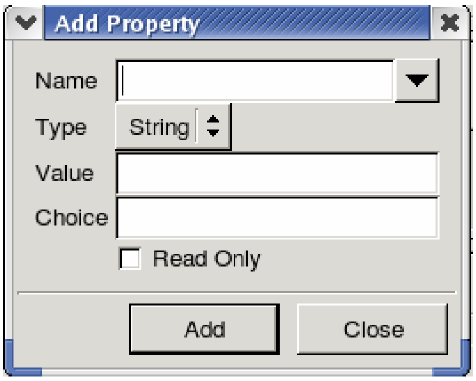
1.3.18 Edit->Property

Display and modify object's property.

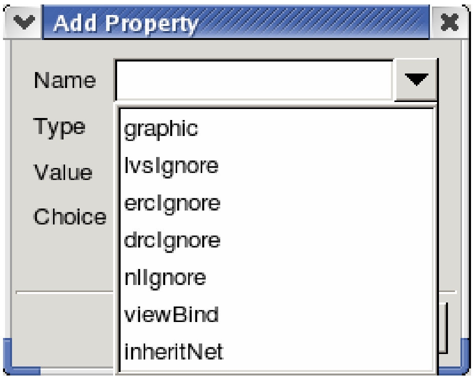
Select Edit->Property or click icon, the object-related Property form appears. You can Add/modify/Delete some properties on it.



User Property field is for you to Add/Delete/Modify/Sort user-defined properties. Click Add button to add a new property, "Add Property" form pop-up as below, you can fill the form to add a property you want:



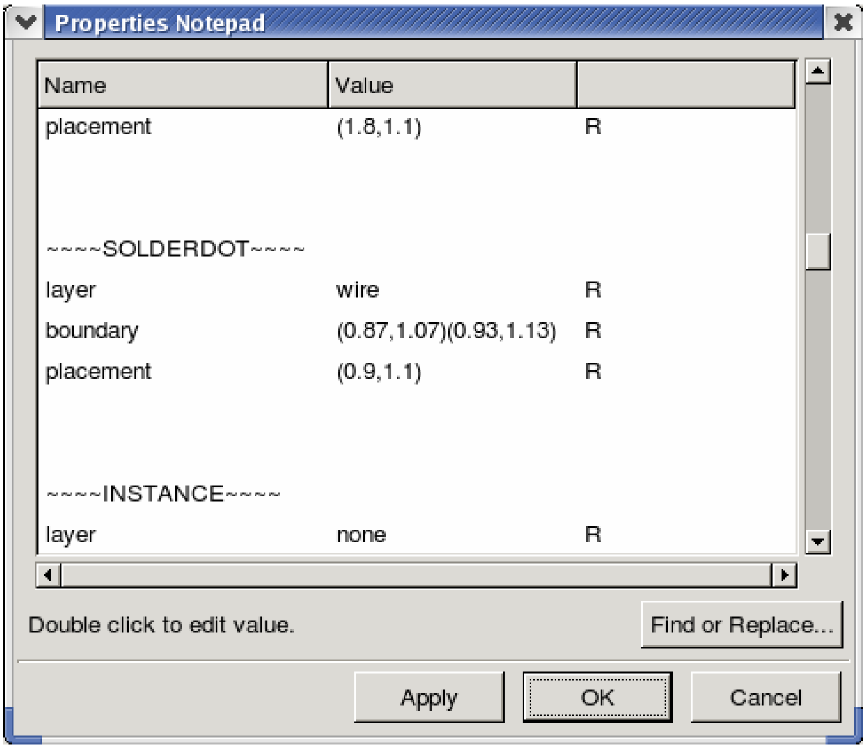
Zeni also provides you some properties on *Name* drop-down list. You can get more detail about these properties on the table below.



graphic	Instance with graphic property should have no pin, and it will not be regarded as device and will not be exported to netlist file. Mainly used for Title Box.
ercIgnore	Instance without any pin will not be checked as error if it has ercIgnore property. Mainly used for symbols come from Sheet library and Spice library.
drcIgnore	System will not do overlap checking on instances with drcIgnore property.
lvsIgnore	Instance with lvsIgnore property will not be exported to CDL netlist file; while export Spice netlist, sub-circuits in this instance will be ignored.
nlIgnore	Instance with nlIgnore property will be skipped while you export any kind of netlist.
viewBind	Bind a specified view to this instance. It takes precedence of settings on ViewNameList.
inheritNet	inheriteNet is an extension to the connectivity model that allows you to create special global signals and override their names for selected branches of the design hierarchy. This flexibility allows you to use ● Multiple power supplies in a design ● Overridable substrate connections ● Parameterized power and ground symbols

1.3.19 Edit->Property Notepad

Show and edit objects' properties in a pad text.
Select some objects, then choose *Edit->Property Notepad*, all the properties of selected objects will be shown.



1.4 Window menu

1.4.1 Window->Redraw

Refresh the entire layout window.

Select this command or click icon  to do it.

1.4.2 Window->Fit

Resize the display area and show the entire view in full window.

Select this command or click icon  to do it.

1.4.3 Window->Fit Object

Show all the objects in the current view in full window. Those objects exclude cell in "Sheet".

1.4.4 Window->Fit Selection

Only show the selected objects in full window.

1.4.5 Window->Zoom In

Display objects within a rectangle area in full window.
To do it, you should,

Select this command, or click icon  first.
Draw a rectangle area to enclose the objects you want to display in full window.

1.4.6 Window->Zoom In By 2

Magnify two times to display objects.

Select this command or click icon  to do it.

1.4.7 Window->Zoom Out

Reduce displaying all objects in a rectangle area.
To do it, you should,

Select this command or click icon  first.
Draw a rectangle area to enclose the objects you want to display in full window.

1.4.8 Window->Zoom Out By 2

Reduce two times to display objects.

Select this command or click icon  to do it.

1.4.9 Window->Center

Make a point appear in the center of the editor window.
Select this command and click on a point that you want to display in the center of the editor window. The image moves and places the reference point in the center of editor window.

1.4.10 Window->Last View

Discard current view and show the last view.

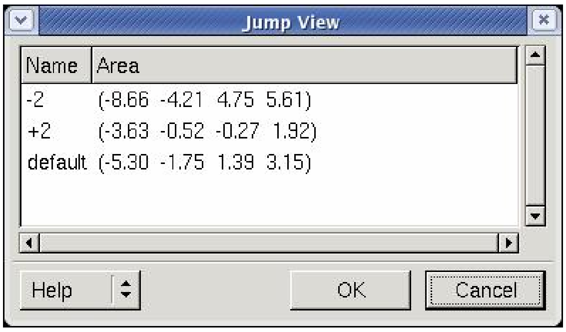
1.4.11 Window->Mark View

Record the current view status. You can jump to this marked view by *Jump View* command.
Select this command, “Mark View” form appears shown as below.

Type the maker name in *Name* field and click *OK* button. You can find this name will appear in *Jump View* form when you activate *Jump View* command.

1.4.12 Window->Jump View

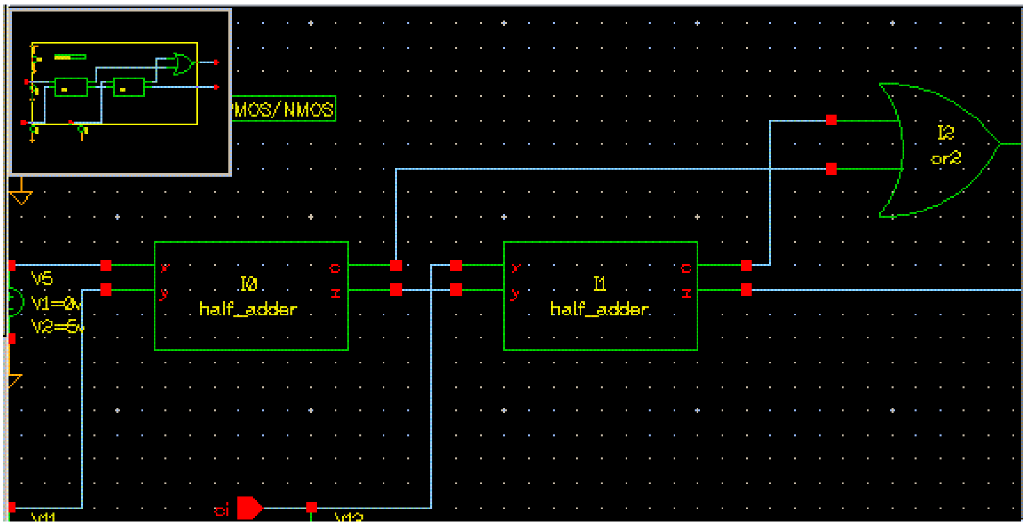
Jump to a previously marked view.
Select this command, “Jump View” appears shown as below.



The view names marked by *Mark View* are listed in this window. You can double click on a view name item or select a view name item and click *OK*, the view will be shown in editor window.

1.4.13 Window->Birds-eye View

Show the current view's panorama in a mini window. We call this mini view "Birds-eye View".
Select this command to show or hide the Birds-eye View.



In Birds-eye view window, the highlighted yellow rectangle presents an outline of a full opened cell. There are two ways to choose the area in the Birds-eye View.
One is moving the mouse cursor and click LMB at a dot, this dot is regarded as a center of the highlighted yellow rectangle, when you move the dot, the highlighted yellow rectangle will be changed. Another way is dragging the RMB to specify an area on the Birds-eye View.
The location of mini window can be set at Top Left, Top Right, Bottom Left and Bottom Right by Options->Display->Birds-eye View At.
The size of mini window can be set also by *Options->Display->Birds-eye View Size.*

1.4.14 Window->Copy Window

Duplicate current cellview window and open the new one.

1.4.15 Window->Raise Design Manager

This command raises Design Manager window to the top of the screen. It's very convenient for you to return to Design Manager window directly from schematic editor window.

1.5 Select Menu

1.5.1 Select->Area Select

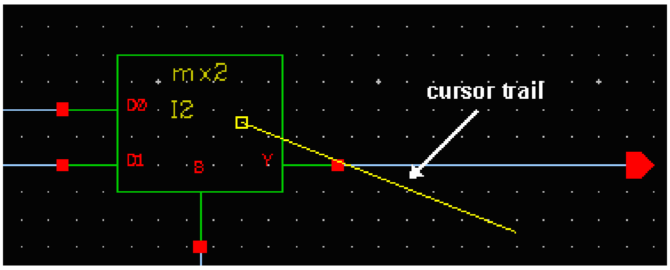
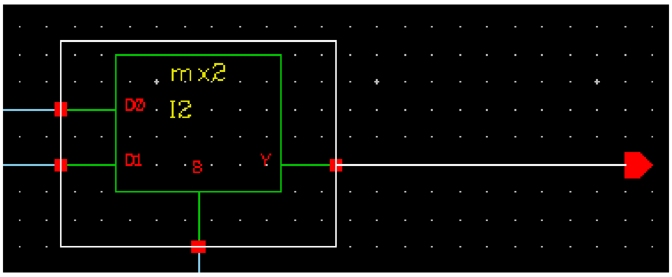
Select objects within a specified area. All objects inside this area will be selected.
To do it, you should

1. Choose this command.
2. Click the first corner of the selection area with LMB.
3. Hold and drag LMB to select the area, click to confirm the second corner.

1.5.2 Select->Line Select

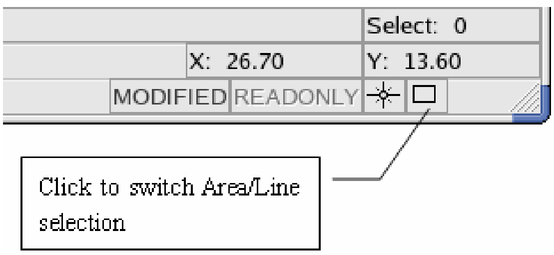
Select objects by trail of cursor. All objects cross this line will be selected.
To do it, you should
1. Choose this command.
2. Click the first point with LMB.
3. Hold and drag LMB to the second point, release LMB.

For example, below table shows the process of line selection.

Action	Illustration
Drag left mouse button to cross objects you want to select.	
Release left mouse button, objects in this trail of cursor are selected.	

Note:

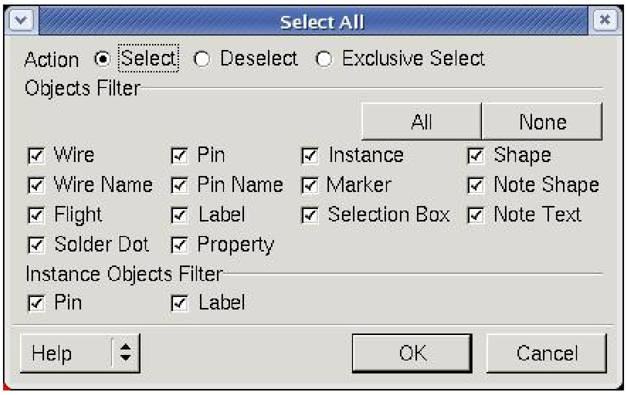
You can click a icon at the right bottom of Schematic Editor window to switch area selection or line selection.



Comparing with menu command method, this method is different. Using menu command Select->Area/Line, select only works on the current operation. When the command is finished, the default selection mode still depends on the icon command located at the right bottom of the Schematic Editor window.

1.5.3 Select->Select All

Select, deselect or exclusive select objects in current cellview.

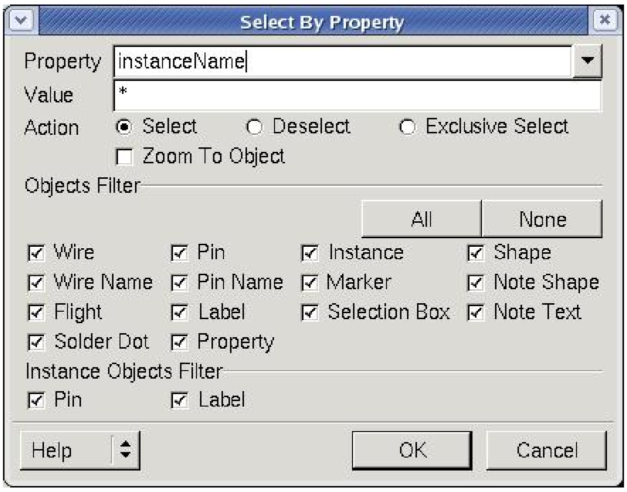


Action controls which type operation does you want in this session.
Objects Filter and **Instance Objects Filter** sections let you select the object types that will be selected/deselected/exclusive selected in current cellview.

1.5.4 Select->Select By Property

Select objects by some specified properties.

Select this command or click icon . “Select By Property” form is shown as figure below.



Property lets you type object's property or select a candidate property from drop-down list. The candidate properties are *instanceName*, *netName, pinName, wireName, libraryName, cellName* and *viewName.*
Value lets you type the value of the property. Use asterisk (*) for wildcard.
Action specifies the action of selecting.
Zoom To Object controls whether to magnify the selected object at the center of the editor window.

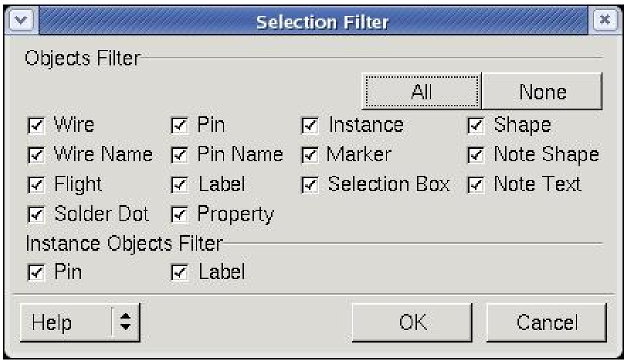
1.5.5 Select->Select Wires

Click a segment of one wire to select entire wire.

Note: You can double click a segment of a wire to select entire wire.

1.5.6 Select->Filter

Specify which type objects will be selectable.



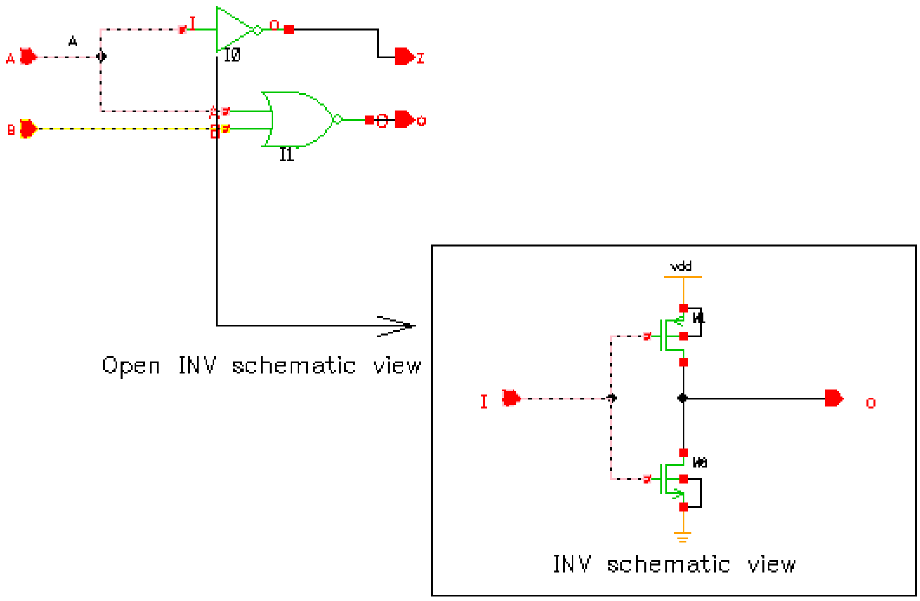
Turning on an object option means the type of object is selectable. Click *All* button to turn on all type of objects. Click *None* button to turn off all type of objects.

1.5.7 Select->Trace Net

Highlight an electrical connectivity net.
Select this command; click a segment of a net, the editor highlights the whole net in color. The editor can pass the net connectivity into its sub-cell that connected with this net.
To trace a net, do as follow:

1. select Check->Hierarchy to check full hierarchy first
2. Choose “Select->Trace Net”
3. Click on any segment of a net or a hierarchy pin

For example, the following figure shows the electrical connectivity net "A" in pink. The net "A" connects two instances "INV" and "NOR2". The editor passes the connectivity into internal of instance via instance pin. Try to open "INV" schematic view, you can find the editor highlights the net "I" in pink as well.



You can trace net one by one until you press *Esc* key. The editor allows you to specify 6 colors for tracing, when you trace the 7th net; the color is the same as the first one. As the above figure, the second tracing net "B" is in yellow.

Note:

1. Before tracing net, you must check hierarchy cell.
2. You can trace more nets one by one untill pressing "Esc" key.
3. Using *Select->Remove Trace* or *Select->Remove All Traces* to remove the highlight.
4. The color of highlighted dashed is specified in *Option->Color*.

1.5.8 Select->Remove Trace

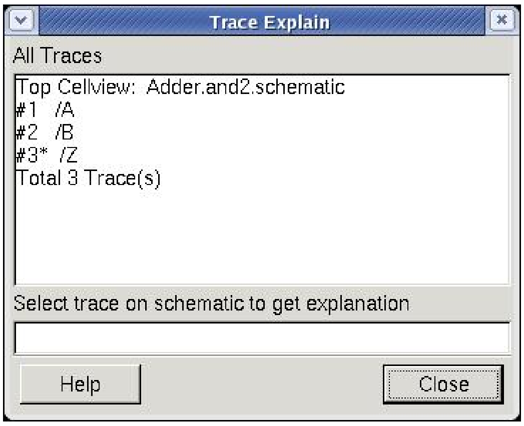
Change the highlighted net to normal. This net is highlighted by command *Trace Net* before.
Choose this command*;* click on a highlighted net, the net will be cancelled highlight.
You can remove highlighted net one by one until you press *Esc* key.

1.5.9 Select->Remove All Traces

Change all highlighted nets to normal. These nets are highlighted by command *Trace Net* before.
Choose this command; all highlighted net will be cancelled highlight.

1.5.10 Select->Trace Explain

Display information of electrical connectivity net.
After doing *Trace Net* command, select this command, information of all electrical connectivity nets is shown in "Trace Explain" form.



This form displays the top cellview name and the number of traced net. '*' represents this net is in the current cellview. Select one of nets in the current cellview editor, associated information with this net will display in *Explain Selection* field.

1.6 Hierarchy->Descend Edit

This command allows you to edit a sub-cell in current window directly, which avoids opening this sub-cell by Design Manager.

Select this command or click icon , click on an instance, editor will display all the views of the cell in a pop up menu. Select one of view, the editor will open the associated editor for editing in current window.

1.6.1 Hierarchy->Descend Read

This command allows you to open a sub-cell in current window for read.
Select this command; click on an instance, editor will display all the views of the cell in

a pop up menu. Select one of view, the editor will open the associated editor for read only in current window.

1.6.2 Hierarchy->Return

This command returns to an upper level cell.

Select this command or click icon to return to an upper level cell.

Note: The current view must be opened by command Descend Edit or command Descend Read, otherwise, this command is invalid. For example, if the current view is opened by Design Manager directly, this command does not work.

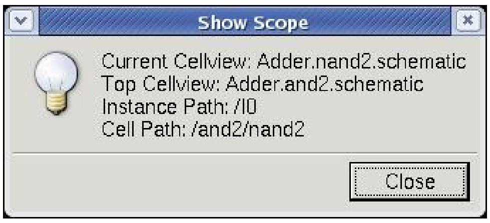
1.6.3 Hierarchy->Return To Top

Return to the top cell directly.

Note: The current view must be opened by command Descend Edit or command Descend Read, otherwise, this command is invalid. For example, if the current view is opened by Design Manager directly, this command does not work.

1.6.4 Hierarchy->Show Scope

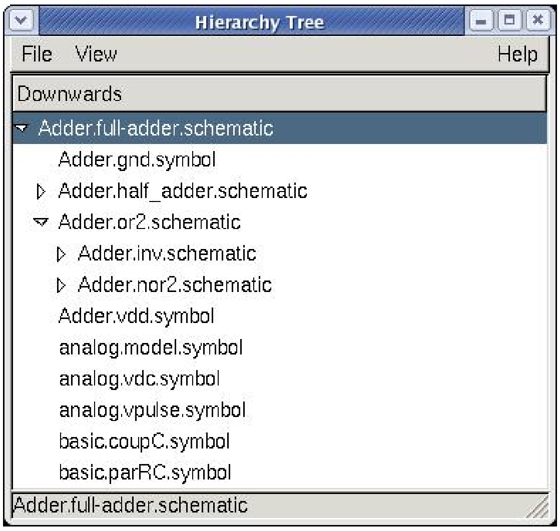
Display information of current cellview.
Select this command, “Show Scope” form is shown as figure below.



This form displays the current cellview name. If the current cell does not a top cell, it also displays the top cell name, the instance path and cell path.

1.6.5 Hierarchy->Show Tree

This command displays all sub-cells of current view.
Select this command, “Show Tree” form is shown as figure below.

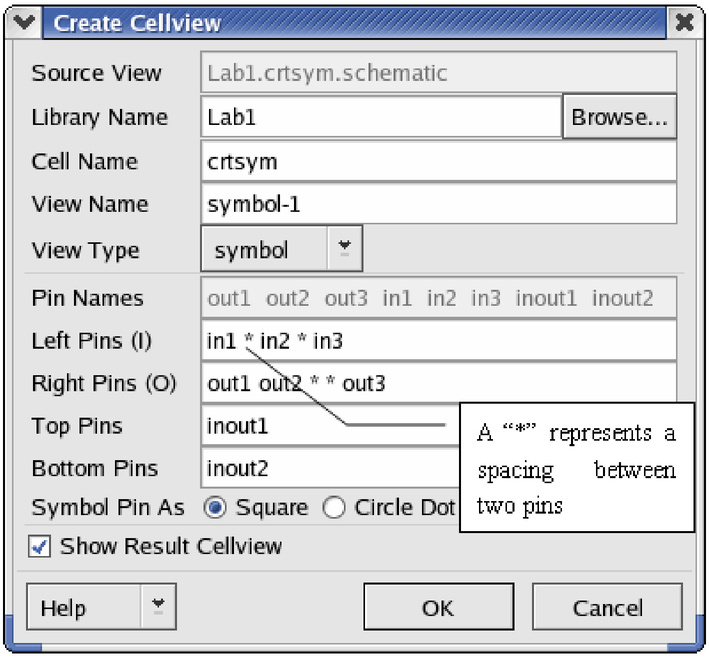


1.7 Cellview menu

1.7.1 Cellview->Create From Cellview

This command automatically creates a new cellview according to current view.

Select this command or click icon, "Create Cellview" form is shown as figure below.

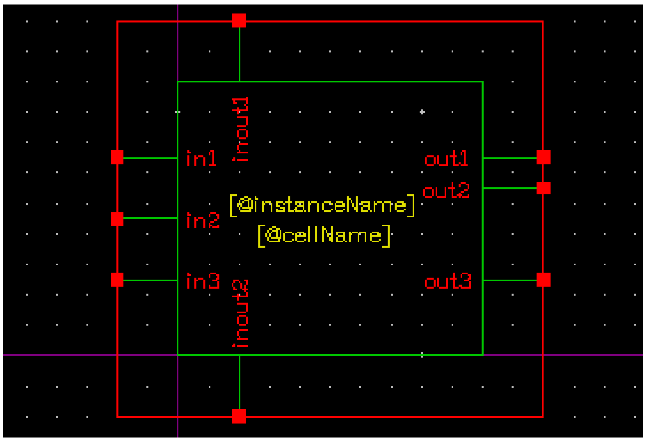


Source View specifies the current view.

Library Name specifies library name you want to create.
Cell Name specifies cell name you want to create.
View Name specifies view name you want to create.
View Type lets you choose a view type you want. If you choose "symbol" from the drop-down list, the editor will create a symbol view. This symbol view includes a rectangle and some pins, these pins are around the rectangle.
Pin Names lists all of pins in current view. The order of list follows the definition of command *Pin Order*. You cannot modify it. These pins will be created in symbol view,.You can also specify the location of these pins in following fields.
Left Pins specifies pins are on the left side of rectangle in symbol view.
Right Pins specifies pins are on the right side of rectangle in symbol view.
Top Pins specifies pins are on the top of rectangle in symbol view.
Bottom Pins specifies pins are on the bottom of rectangle in symbol view.

Note:

1. If you don't type any pin name in these fields, the system puts all of input pins or inout pins on the left of rectangle and puts all of output pins on the right of rectangle.
2. In these fields, you can use one or multiple "*" to control the distance of two pins. For example, setting all the pins as the Create Cellview form above, then the symbol will be as figure below:



Symbol Pin As specifies the shape of the pin is either *Square* or *Circle Dot* in symbol view.
Show Result Cellview opens the new view in a new window.

1.7.2 Cellview->Create From Instance

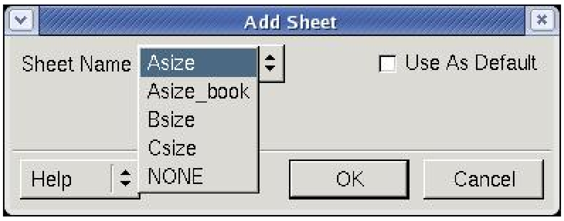
This command automatically creates a new cellview according to an instance you selected.
The form and usage are similar to command *Create From Cellview*, please refer to 1.4.1 *Cellview->Create From Cellview*.

1.8 Page menu

1.8.1 Page->Add Sheet

Add a sheet frame around the schematic cellview.
You can use default sheets in the system library “sheet” or create your own sheets and add them to “sheet” library.

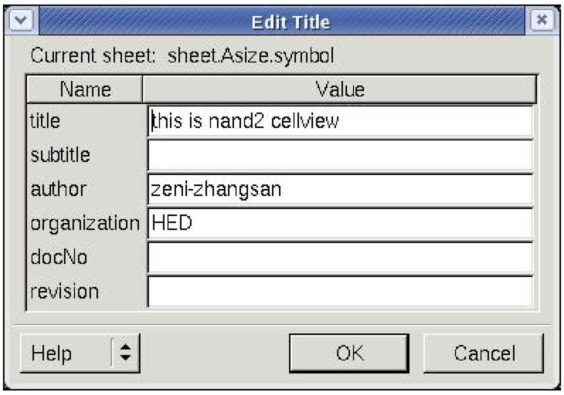
Select this command or click icon, “Add Sheet” form is shown as figure below.



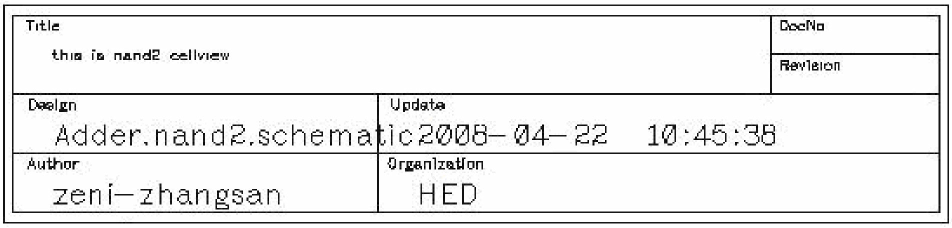
Sheet Name lets you select a sheet from dropdown list. "NONE" specifies to remove sheet from current cellview.
Use As Default lets you automatically add this sheet when creating a new schematic view.

1.8.2 Page->Edit Title

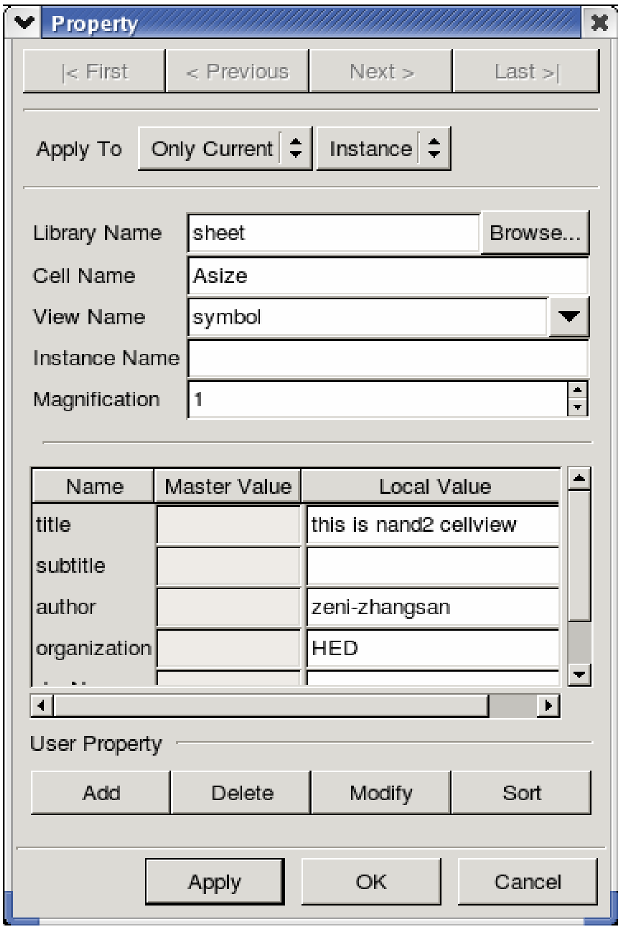
Edit the sheet information, such as title, author, organization, etc.
Select this command, “Edit Title” form is shown as figure below.



Type the valid information in this form, click *Apply* or *OK* button, the information will be display in sheet shown as below.



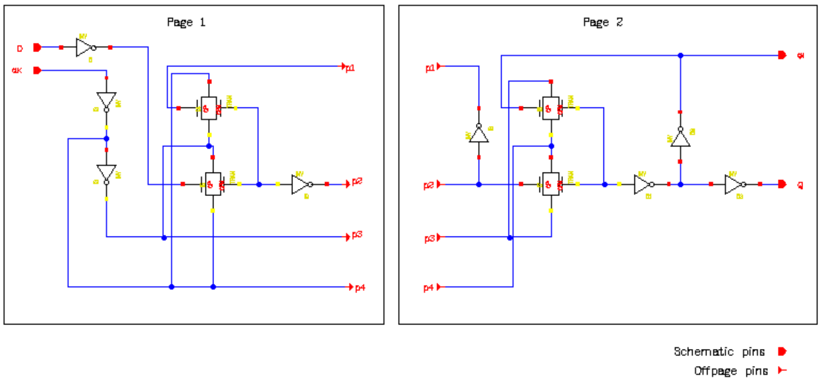
Some information, such as *Design* and *Update* are updated automatically.
You can also modify the information in sheet property form. Please refer to figure below.



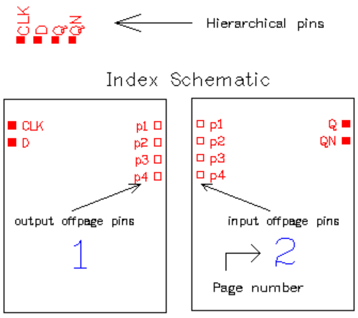
1.8.3 Page->Make Multi-Pages

Partition multi-pages schematic views to your design in several pages.
Select *Page->Make Multi-Pages*, the editor renames the current cell name to "cellname@1", which means this design is the first page design. In the meanwhile, the editor creates an index schematic named "cellname" to organize the pages; each page design is as an instance in Index schematic. To add more pages, select *Page->New Page* from the Index Schematic.

The following is an example of a design that consists of 2 pages. Offpage pins p1, p2, p3, p4 connect two pages. These offpage pins must be used twice. In page 1, offpage pin direction is output. In page 2, offpage pin direction is input.



In the top level, the index schematic is as below.



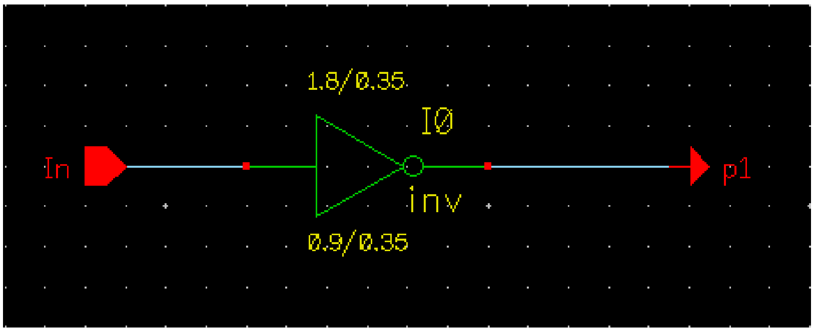
It displays all of hierarchical pins (schematic pins) and all of page symbols. In each page symbol, the input pins (schematic pins or offpage pins) are placed on the left side, the output pins (schematic pins or offpage pins) are placed on the right side.

The ■ represents this pin is a hierarchical pin.

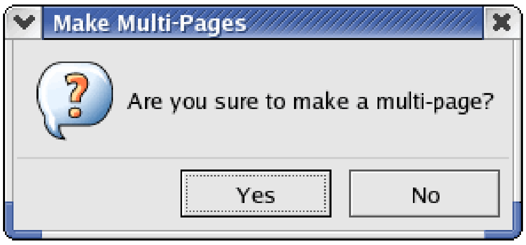
The □ represents this pin is an offpage pin.

Here is an example to show how to make Multi-Pages:

1. Create a new cellview "Lab1.page.schematic"
2. In Schematic Editor window, create following objects:
   schematic input pin "In"
   instance of cell "INVtest.inv.schematic"
   offpage output pin "p1".

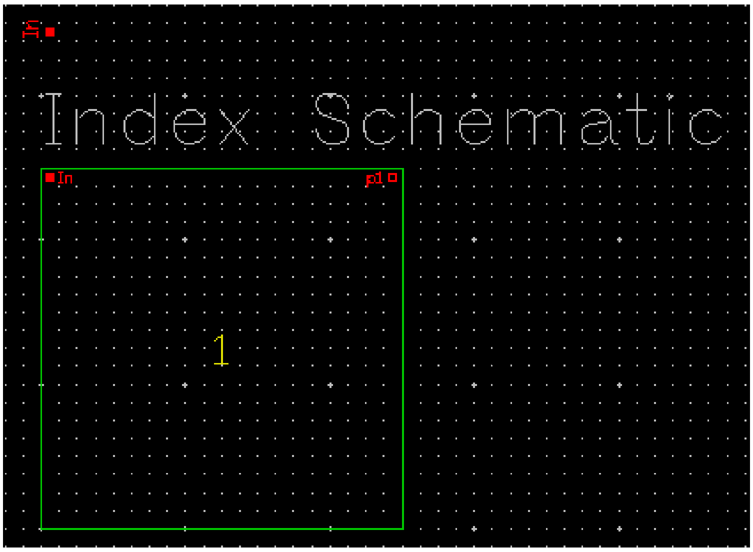


3. Save the cellview.
4. Select page->Make Multiples page. A question form appears as below.

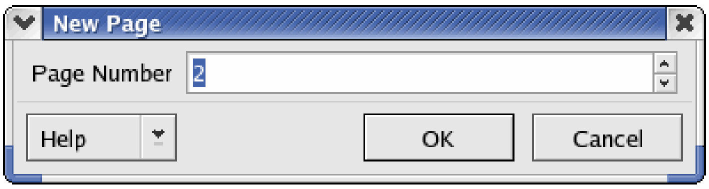


5. Yes the form.
6. The title of current Schematic Editor window becomes to "Lab1.page@1.schematic". "@1" represents the first page.

7. Close the current Schematic Editor window.
8. Open the cellview "Lab1.page.schematic", this cellview looks as the figure below.

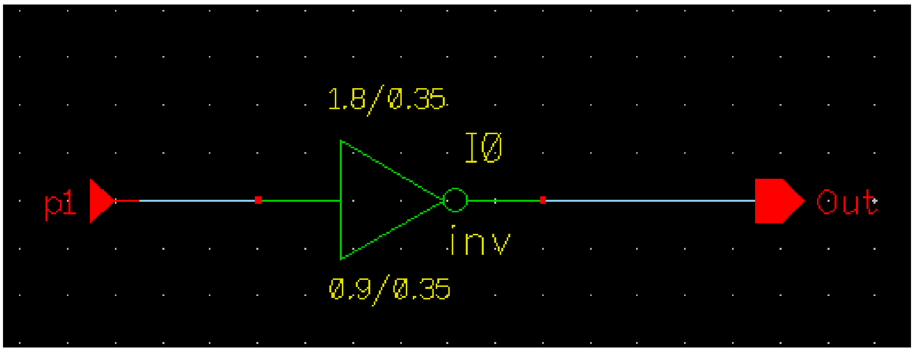


9. This cellview includes an instance of cell “page@1”, and extracts the schematic pin of cell “page@1” as schematic pin of itself.
10. In instance of cell “page@1”,
    ■ represents the schematic pin
    □ represents the offpage pin.
    Input pin is in the left, output pin is on the right
11. In this cellview window, select Page->New Page. A New Page form appears.

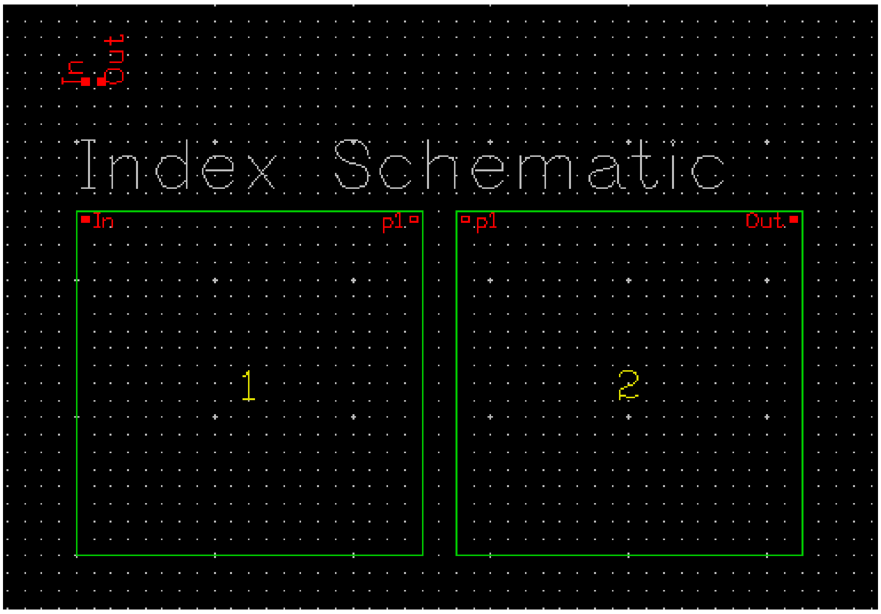


12. System automatically fills out ‘2’ in Page Number to represent the next page is the second one.
13. Ok the form. The cell “page@2” is created in Design Manager window, and the Schematic Editor pops up.

14. In Schematic Editor window, create following objects:
    offpage input pin p1.
    instance of cell “INVtest.inv.schematic”
    schematic output pin out



15. Save the current cellview.
16. Open the cellview “Lab1.page.schematic” again. There are two instances as below.



17. Save and close the cellview.

 **Note:**

Offpage pin must appear twice with reverse direction between two pages.

1.8.4 Page->New Page

Create a new page.

In index schematic view, select this command, the “New Page” form is shown as figure below.

The editor automatically fills the page number in *Page Number* field. This page number is the current maximum page number plus 1. You can modify this number as you want.

Click *Apply* or *OK* button, Design Manager will create a new cell named "cellname@3", here cellname is the cell name. Meanwhile, system will open the schematic editor in the current window.

You can use , or Hierarchy->Return, or Hierarchy->Return To Top to return to the index schematic.

1.8.5 Page->Delete Page

Delete a page design.

In index schematic view, select this command, the “Delete Page” form is shown as figure below.

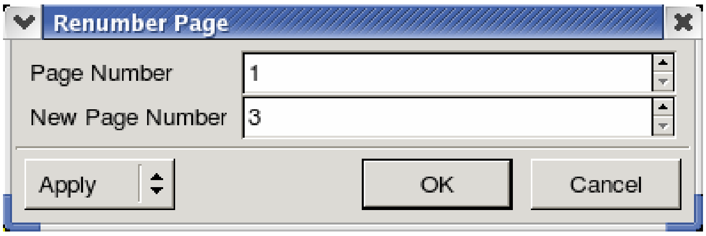
Type the page number you want to delete in *Page Number* field. Click *Apply* or *OK* button, a question dialog box pops up to enquire whether you are sure to delete this page.

Click *Yes* to delete this page design. In the meantime, the associated cell "cellname@3" is deleted.

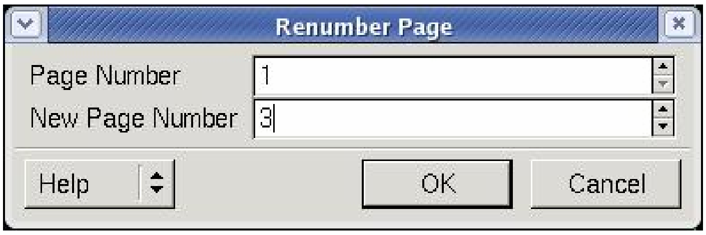
 **Note:** If you delete the page symbol with Del key or *Edit->Delete* in index schematic, the associated cell will not be deleted. This operation cannot be undone.

1.8.6 Page->Renumber

Reset the page number.
In index schematic view, select this command, the “Renumber Page” form is shown as figure below.



Specify the page number you want to reset in Page Number field.
Specify the new page number in New Page Number field.
If the new page number already exists, the editor will give you a question dialog box to enquire whether you continue to renumber this page.



Click *Yes* to renumber the page 1 to page 3, the associated cell name "cellname@1" is renamed to "cellname@3". Original page 3 will be forced renamed to page 4, the associated cell name "cellname@3" is renamed to "cellname@4".

 **Note:** This operation cannot be undone.

1.8.7 Page->Resequence

To reset sequence number of all page views.
In index schematic view, select this command, the editor renumbers all pages sequentially beginning with page 1.
For example, if there are page 2, page 3 and page 5, this command reorders the pages in sequence page 1, page 2 and page 3.

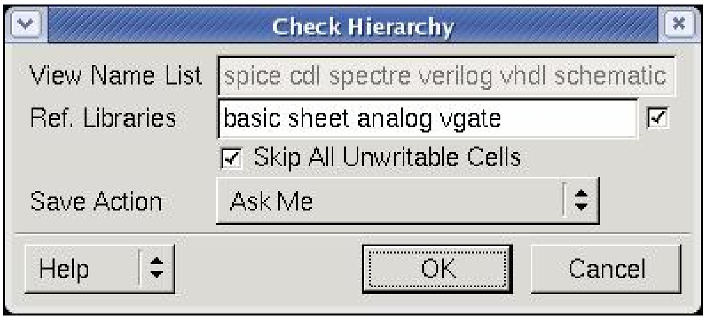
1.9 Check menu

1.9.1 Check->Current Cellview

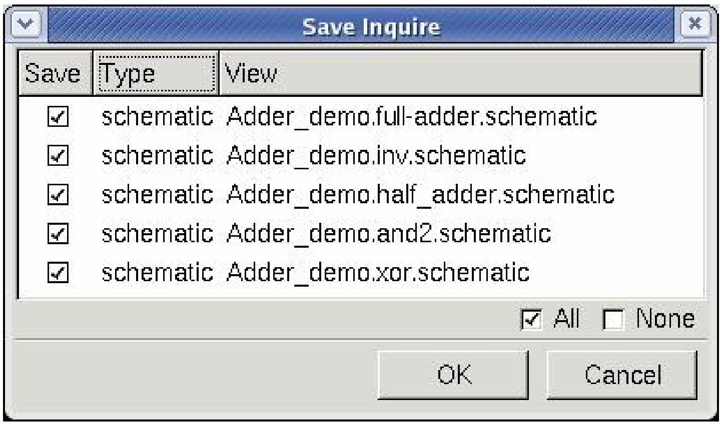
Check circuit in current cellview.
Select this command, editor will pop up a mini window and show the number of errors after checking. The detailed error information will be displayed in Design Manager.
If you turn off Prompt When 0 Errors/Warnings option in *Options->Check Rules*, editor does not pop up the mini window if no errors and warnings.
When circuit is error, the error marker and warning marker are placed in the corresponding position. You can modify the colors of error maker and warning maker by *Options->Color*. You can also remove these markers by *Check->Delete Marker* or *Check->Delete All Markers.*

1.9.2 Check->Hierarchy

To check all of related schematic views in the hierarchy design.
Select this command, the “Check Hierarchy” form is shown as figure below.

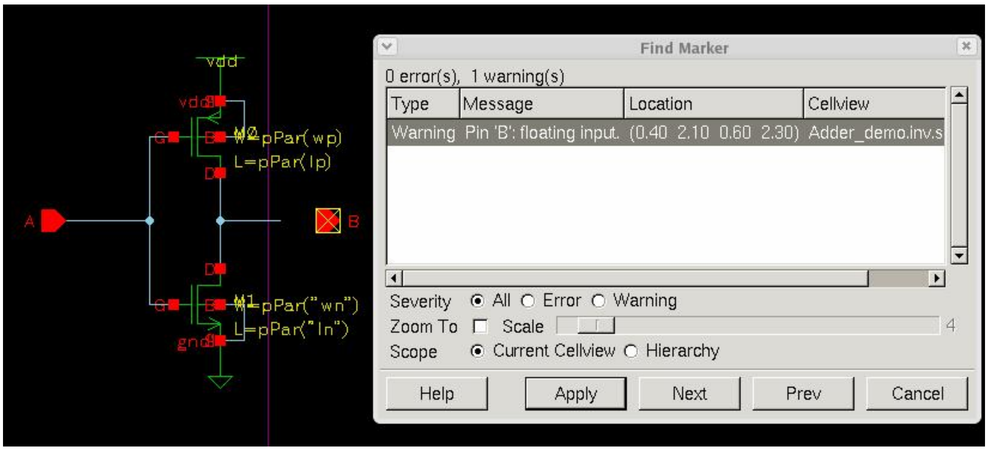


View Name List shows which view you will be checked. This list is defined in *Options->Editor* form, you have no write access here. From the heading of this list, editor will search view name one by one for related cells, and check the first founded view. This list is defined in *Options->Editor*
Ref. Libraries list some referenced libraries which will not be checked.
Save Action specifies whether editor saves checked cellviews after checking.
Auto.Save -- automatically save all of checked cellviews.
No Need Save -- don't save all of checked cellviews.
Ask Me -- pop up a dialog box to inquire you which cellview need to be saved.



1.9.3 Check->Find Marker

Find the error in cellview recorded by marker.
Select *Check->Find Marker*, the editor pops up a dialog box which displays all of the error and the warning messages generated by check. Click on an error or warning item in the list, and the editor will highlight the associated marker in the window.



Severity determines displaying what kinds of markers, *Error/Warning/All*.
All display both errors and warnings.
Error only displays all of errors.
Warning only displays all of warnings.
Zoom To lets you magnify the error object and show it in the center of window. *Scale* specifies the ratio of magnification.
Scope specifies displaying errors either in the current cellview or in all of the cellviews within the hierarchy.

1.9.4 Check->Delete Marker

Delete marker by your cursor.
Select *Check->Delete Marker* first; move your cursor to marker, no matter either error marker or warning marker, click on this marker, the marker will be removed.

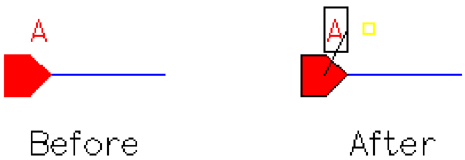
1.9.5 Check->Delete All Markers

Delete all markers.
Select *Check->Delete All Markers*, the "Delete All Markers" form is shown as figure below.

Select an option in above form,
All delete all markers.
Error only deletes error markers.
Warning only deletes warning markers.

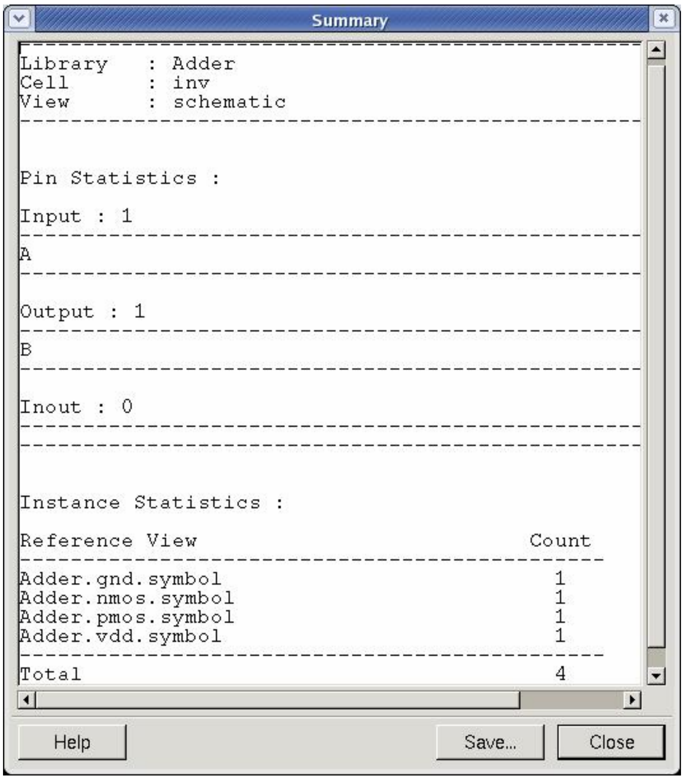
1.9.6 Check->Show Label Attachment

Highlight the association between a label and its owner (pin, wire or instance).
Select *Check->Show Label Attachment*, you click either an object (pin, wire or instance) or a label, system will draw a highlighted line between them, and highlight it. The following figure shows the result of showing label attachment.



1.9.7 Check->Summary

To display detailed information about how many pins and instances are in the current cellview.
Select Check->Summary, the "Summary" form is shown as figure below.

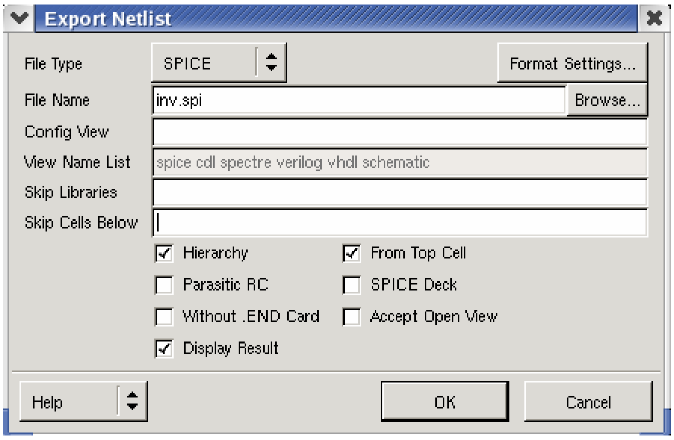


1.10 Tools menu

1.10.1 Tools->Export Netlist

This command generates 7 kinds of netlists, there are *SPICE, CDL, Verilog, Verilog-A, VHDL, Spectre* and *Mixed-Mode.*

Select *Tools->Export Netlist* or click icon, the “Export Netlist” form is shown as figure below.



File Type specifies to generate which type of netlist format. Click on the *Format Settings* button to specify the netlist format.

File Name lets you type the netlist file name. You can also fill out this field with "%C". For example, 

. Here, %C stands for the current cellview name. Suppose that the current cellview name is "inv". The netlist file name will be "/tmp/inv/inv.spi".

Config View lets you type a configuration cellview name. This cellview is used for exporting a *Mixed Mode* netlist.

View Name List comes from *options->Editor->View Name List*. Here, if you turn on the Hierarchy option, netlist generator searches related view name from this list according to exporting netlist type. For example, if you want to export verilog netlist in hierarchical, netlist generator will search verilog type cellview from the list one by one. Once find it out, netlist generator stop searching and directly add this verilog text to the export netlist file.

Skip Library specifies libraries listed here are not exported to netlist file.

Skip Cells Below specifies all sub-cells of the cell listed here are not exported to netlist file.

Hierarchy option controls whether to export entire hierarchy design or only the current level design.

From Top Cell option controls whether you can export hierarchical netlist from top level cell even though you are in sub-cell cellview window.

Parasitic RC option controls whether to export parasitic loads to netlist file or not.

SPICE Deck option controls whether to export netlist according to SPICE Deck definition or not. About *SPICE Deck*, please refer to *Tools->Spice Deck.*

Without .END Card.option controls whether to add ".end" keywords to SPICE netlist and Mixed Mode netlist.

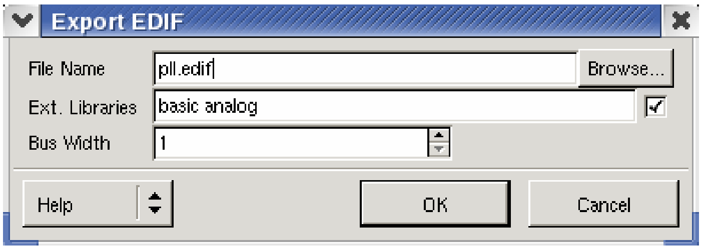
Accept Open View option specifies whether to skip it and continue to export netlist if there is no suitable view for sub-cell. When you turn on the option, ZeniSE will continue to export netlist and give warning message on Design Manage window. If you turn off the option, ZeniSE will give error message and stop exporting netlist.

Display Result option controls whether to display the netlist file after exporting.

Note: The design must be checked before exporting netlist.

1.10.2 Tools->Export EDIF

To translate current schematic data to EDIF file.
Select *Tools->Export EDIF*, the “Export EDIF” form is shown as figure below.



File Name specifies the name of edif file.
Ext. Libraries these libraries that are listed in this field are regarded as "external" library, and they are exported to edif file with keyword "external".
Bus Width defines created bus width. 10 is default.

1.10.3 Tools->SPICE Deck

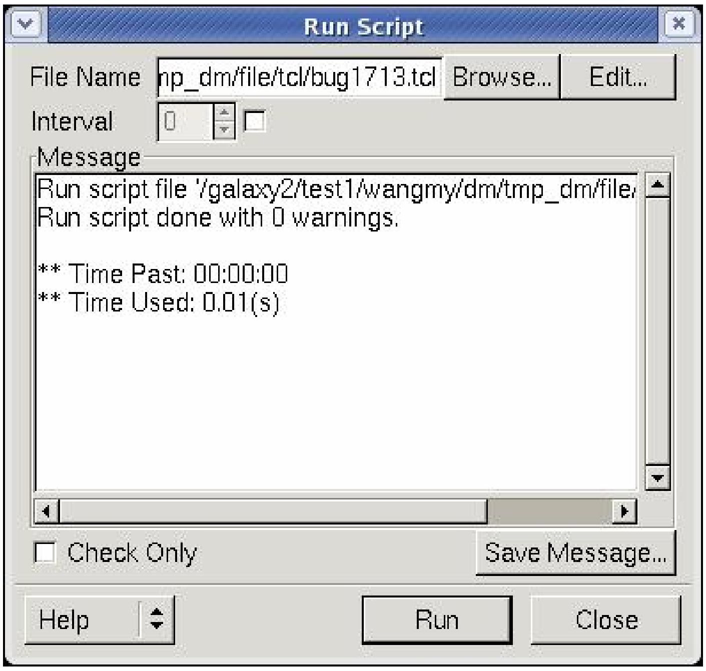
Please refer to *Using SPICE Deck Simulation Environment*.

1.10.4 Tools->External Simulation

Please refer to *8.1 Using External Simulation*.

1.10.5 Tools->Run Script

Run the script file.
Select *Tools->Run Script*, the “Run Script” form is shown as figure below.



File Name lets you type the script file name, or use *Browse* button to select the script file you want to run.
Edit button invoke editor to open and edit the script file.
Interval specify time interval between each two script commands.
Check Only shows you only check syntax, do not run the script file.
Save Message lets you store the run message to a text file.

1.10.6 Tools->Export Tcl Script

Output the Tcl script file.
Select *Tools->Export Tcl Script*, the "Export Tcl Script" form is shown as figure below.

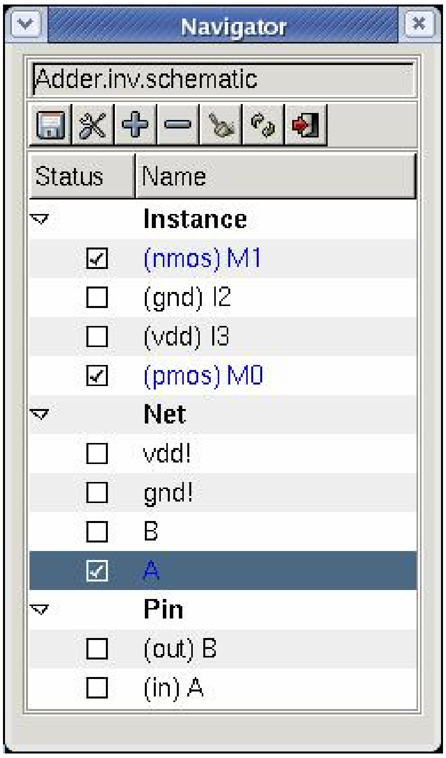
1.10.7 Tools->Clear Back Annotation

Clear the back-annotations from schematic cellview window.

1.10.8 Navigator

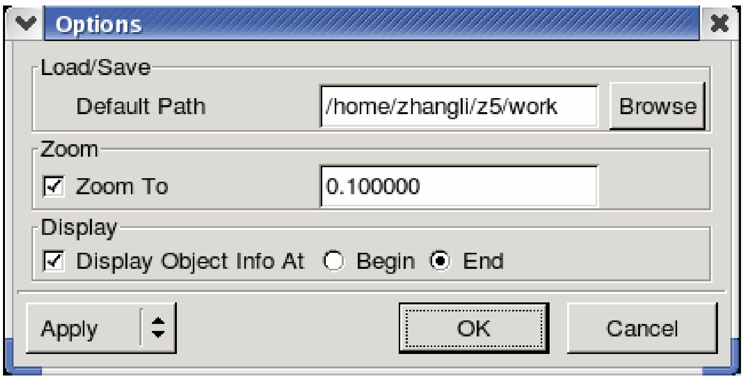
This feature is to help designer remark layout editing processes according to the schematic.

Navigator will extract information of instances, pins and nets from the current schematic cellview and show it in "Navigator" window list. You could check each item in this list to mark which instance/pin/net is finished in layout editing.



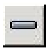
 Save button. The list can be saved to a file to record your editing status.

 Option button. The option form is shown as bellow:



Load/Save is used to set path which you want to save the file to.
Zoom Double-click any item in navigator list, SE editor window will focus on that object and zoom it to the number you specified.
Display is to set the object info shown in the list at *Begin* or *End*.

 Expand the object info list.

 Collapse the object info list.

 Clear all your check markers in the list.

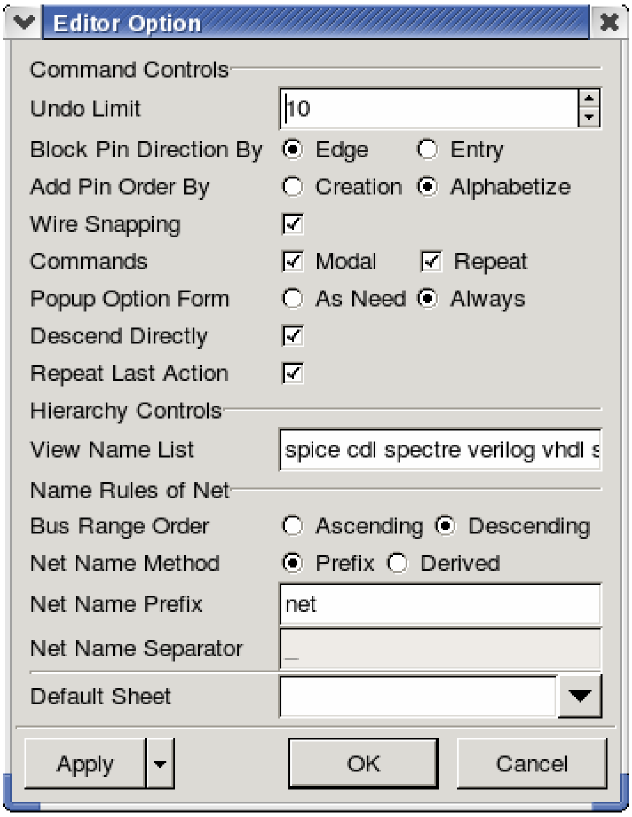
 Refresh list according to the file you saved.

 Close and exit Navigator.

1.11 Options menu

1.11.1 Options->Editor

Configure editing related options for the schematic editor.
Select *Options->Editor*. The “Editor Option” form is shown as figure below.



Undo Limits specifies the limit of Undo. Default is 10.

Block Pin Direction By specifies the block pin's direction.

Edge specifies the direction of a pin depends on its location. Drawing a wire at the left edge of the block creates an Input Pin; drawing a wire at the right edge of the block creates an Output Pin; drawing a wire at the top or bottom edge of the block creates an InOut Pin.

Entry specifies the direction of a pin is automatically determined by how the wire is drawn. Starting a wire from the edge of the block creates an Output pin; ending a wire at the edge of the block creates an Input Pin.

Add Pin Order By specifies when you add more then one pin at one time, the order of these pins is None or alphabetize.

Wire Snapping specifies to press Shift key and click LMB to connect the wire which is being drawn to the closest floating pin.

Commands specify how to cancel a command.

Modal specifies a new command cancels a previous command. Otherwise, the previous command is suspended until the new command is over.

Repeat specifies execute this command more than one time. For example, if you execute command Add Instance, when one instance was added, you can add another instance without re-active this command.

Popup Option Form specifies whether the system pops up an associated form when execute a command.

As Need -- Popup the associated form only when you press F3 key.
Always -- Popup form automatically when a command is executed. Descend Directly allows
Descend Directly you directly access the instance design with double click this instance symbol. The accessed view of instance design depends on follow:

1. If this view has a viewBind property in property command, the system will access this view specified by viewBind.
2. If there is no viewBind property, the system searches view with schematic type in View Name List.
3. If there is also no view with schematic type, the system searches view one by one from the head of View Name List.

Repeat Last Action

View name List is a list of view name. It is used to check hierarchy, export hierarchy netlist, or descend directly. According to the order of this list, system decides to check/export/descend which cellview of instance cell.
The order of cellview name is very import. For example, when you check a full hierarchy design, for instance cell, the system will search this list one by one till finding out existed schematic cellview name of instance cell. Suppose that cell “a” references an instance of cell “b”. But cell “b” has two schematic cellviews, “schematic1” and “schematic2”. When you check full hierarchy from cell “a”, the system will find the suitable schematic cellview name of cell “b” from view name list and check it. If the “schematic2” is in front of “schematic1” in the view name list, SE will check “schematic2” cellview.
Bus Range Order decides to export net name to verilog netlist in ascending order or in descending order. For example, if you name a wire as “In<0>,In<3>,In<2>”, if you turn on “Ascending” option, the wire name is exported to verilog netlist as “wire [1:3] In”, otherwise, export it as “wire [3:1] In”.

Please note that if the bus name is a pin name, it is not controlled by the option. For this case, ZeniSE checks the first second pin name order and decide to export them to netlist in ascending order or in descending order. For example, if pin name is “In<3>,In<1>,In<2>”,ZeniSE will export “Input [3:1] In” to verilog netlist. If the pin name is “In<2>, In<3>,In<1>”, ZeniSE will export “Input [1:3] In ” to verilog netlist.

In additionally, if there are 3 pins “In<1>”, “In<2>” and “In<3>”, ZeniSE checks the first second pin name order from command form “Design->Pin Order” and decide to export them to netlist in ascending order or in descending order

Net Name Method specifies how editor names the net without name.
Prefix (Default) -- uses a prefix string and a number to name the net .The prefix string is specified at the *Net Name Prefix* entry. The number starts from number “1”. For example, name the net to “net1”.
Derived -- uses the instance name, name separator and instance pin name to name

the net. The name format is <instance name><net name separator><instance pin name>. The name separator is specified at the *Net Name Separator* entry. For example, name the net to “I2-in

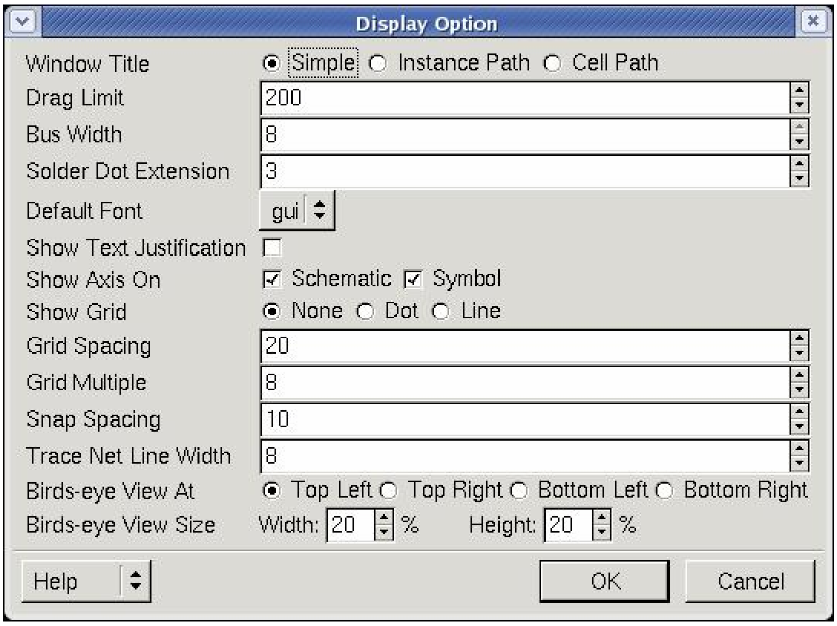
Net Name Prefix???

Net Name Separator???

1.11.2 Options->Display

This form specifies the common settings about schematic display.

Select *Options->Display*, the “Display Option” form is shown as figure below.



Window Title specifies the format of window's title. There are 3 options to define difference format of window title.

Simple--specifies the format is "< cellview type> - <cellview name>".

Instance Path-- specifies the format is "<cellview type> -- <instance path>".

Cell Path-- specifies the format is "<cellview type> -- <cell path>".

Drag Limit when you want to drag some objects, if the number of selected object is larger than the specified number, the system will use a boundary box instead of all the selected objects outlines during dragging.

Bus Width specifies bus’ width. 6 is default.

Solder Dot Extension specifies solder dot’s size. 3 is default.

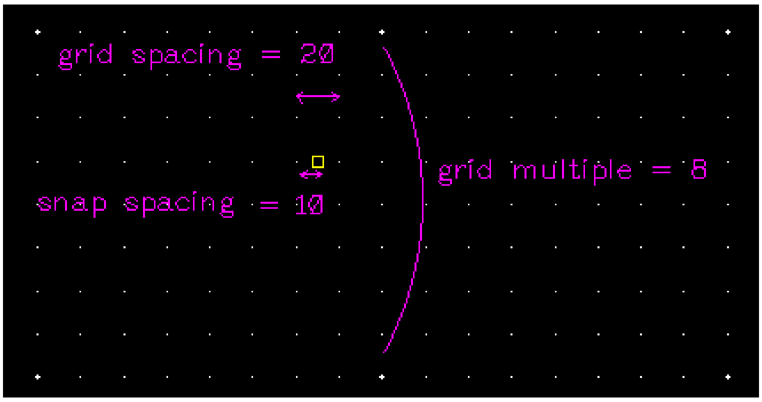
Default Font specifies text’s font, such as Note Text, Wire Name, Label, etc. gui is default.

Show Text Justification displays justification symbol "+" on the text, such as, add wire name, add note text, etc.

Show Axis On specifies to show X axis and Y axis on schematic editor window or (and) symbol editor window.

Show Grid specifies to show grid or not in editor, or show which type grid.

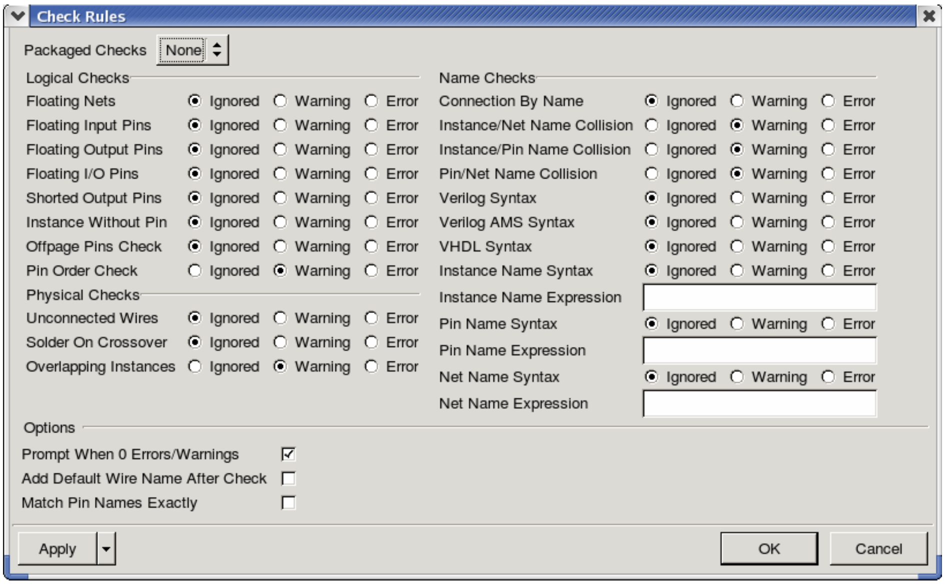
None--not show the grid
Dot--the grid shape is dot.
Line--the grid shape is line.
Grid Spacing specifies the distance between two grids.
Grid Multiple specifies how many grids constitute a grid matrix.
Snap Spacing specifies the distance of moving cursor one step.
Trace Net Line Width specifies trace net line's width.2 is default.



Birds-eye View At specifies where does the birds-eye view window locate at. There are 4 directions you can choose.
Top Left--place the birds-eye view window at the top left of the whole editor window.
Top Right--place the birds-eye view window at the top right of the whole editor window.
Bottom Left--place the birds-eye view window at the bottom left of the whole editor window.
Bottom Right--place the birds-eye view window at the bottom right of the whole editor window.
Birds-eye View Size specifies the size of birds-eye view window. Width and Height specifies what percent is in the whole editor window.

1.11.3 Options->Check Rules

As you know, it's very important to check your design for connectivity, error and rule violations. According to difference design rule, the check rule is different as well.
For each check item, there are 3 severity levels:
Ignored--do not check this rule.
Warning--if the schematic violates this rule, the system regards it as warning.
Error--if the schematic violates this rule, the system regards it as error.
You do not need to correct any warning found during the check process, but you'd better review them before you generation netlist.



Packaged Checks automatically sets the severity levels for the following predefined checks.

None sets the logical, physical, and name check severity levels to ignored.

Normal sets the logical, physical, and name check severity levels to either ignored or warning.

Logical Only sets all logical check severity levels to warning. Physical and name check severity levels are set to ignored.

Physical Only sets all physical check severity levels to warning. Logical and name checks are set to ignored.

Verilog sets logical, physical, and name check severity levels to preassigned values. *Verilog Syntax* checks are set to error.

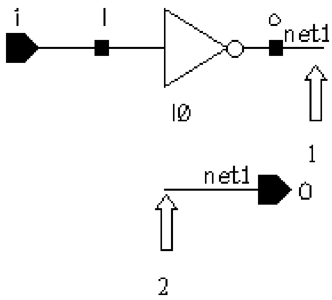
Verilog AMS sets logical, physical, and name check severity levels to preassigned values. *Verilog AMS Syntax* checks are set to error.

VHDL sets logical, physical, and name check severity levels to preassigned *values.VHDL Syntax* checks are set to error.

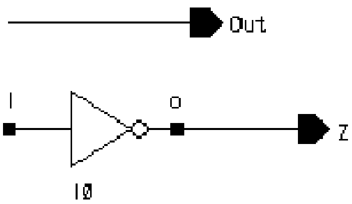
Logical checks control connectivity checking.

Floating Nets checks for wires that are logically connected to schematic pin or instance pin. Sometimes, it depends on the Connection By Name rule.

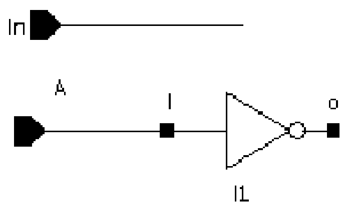
For example, in the below figure, the point 1 and the point 2 are connected to nothing, if you ignore Connection By Name rule, the system regards that point 1 connects with the point 2, and no error. Otherwise, the system regards that the point 1 and point 2 are floating.



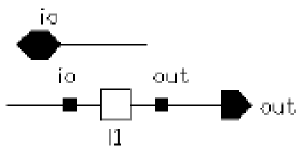
Floating Input Pins checks for instance input pins and schematic output pins that are not connected to instance output pins, schematic input pins, or schematic I/O pins.
For example, in the below figure, the system will report error messages:
"◘ (WARNING/ERROR) SE: Pin '↑ Out'├ : floating input. "
"◘ (WARNING/ERROR) SE: → Pin '↑ I'├ on instance '↑ I0'├ : floating input. "



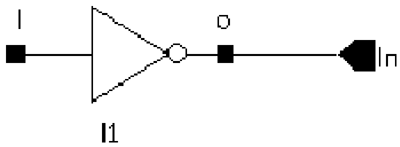
Floating Output Pins checks for instance output pins and schematic input pins that are not connected to instance input pins, schematic output pins, or schematic I/O pins.
For example, in the below figure, the system will report error messages:
◘ "(WARNING/ERROR) SE: → Pin '↑ In├ ': floating output. "
"◘ (WARNING/ERROR) SE: → → Pin ↑ 'o'├ on instance ↑ 'I1'├ : floating output. "



Floating I/O Pins checks for instance or schematic input/output pins whose signals are not connected to instance output pins, schematic input pins, or any other schematic I/O pins.
For example, in the below figure, the system will give error message:
" ◘ (WARNING/ERROR) SE: → → Pin ↑ 'io'├ : floating inout. "



Shorted Output Pins checks for instance output or schematic input pins that are connected to any other instance output or schematic input pins.
For example, in the below figure, the system will report error message:
" ◘(WARNING/ERROR) SE:→ →Pin ↑'↑ In'├ : shorted output. "
◘"(WARNING/ERROR) SE:→ Pin ↑'O├' on instance 'I1' : shorted output. "

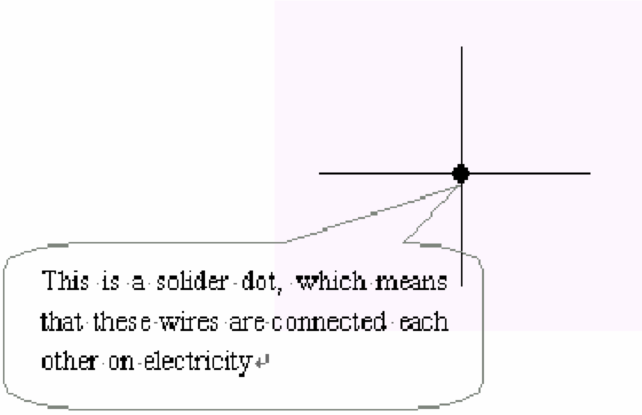


Instance Without Pin checkes for instances that without any pin. If the instance is so. the system will report error message :
" ◘(WARNING/ERROR) SE:→There is no pin in instance '↑ Ixxx'├ . "
But, If the instance are following , the system regards them as legal.
PatchCord
NoERC
Sheet Probe
Coupling Cap
with property ' ErcIgnore'
OffPage Pins Check checking for offpage connectors that appear on only one page in a multi-page design, and also checks two offpage connectors with the different directions.

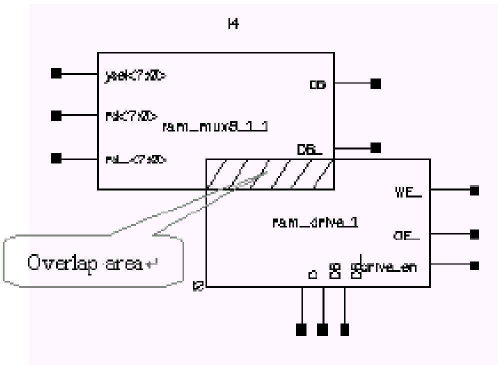
Pin Order Check specifies whether to check the pin order when you cross check between schematic view and symbol view, or check between two schematic views, or check between two symbol views.

Physical checks control checking for unconnected wires solder on crossover and overlapping instances.
Unconnected Wires checks for the wires that are connected to nothing.
For example, in the figure, the system will report error messages:
"(WARNING/ERROR) SE:→Unconnected wire at (-90, 350). "
"◘(WARNING/ERROR) SE:→Unconnected wire at (-190,260). "
Solder On Crossover checks for solder connections placed on wire crossovers.

For example, in the below figure, the system will report error messages:
→ ◘"(WARNING/ERROR) SE: Solder dot on cross over. "



Overlapping Instances checks for instances that overlap with other instances.
For example, in the below figure, the system will report error messages:
→ ◘"(WARNING/ERROR) SE: →The instance '↑ I4'├ overlaps instance '↑ I2'├ . "



Name checks control checking for syntax and collisions.

Connection By Name checks whether a signal exists in more than one physically disjointed group of wires or pins.

Instance/Net Name Collision checks whether the instance name and the net name are same, or the base name are same.

For example, the instance name is "I1", the net name is "I1" or "I1<1>", the system regards those names as illegal.

Instance/Pin Name Collision checks whether the instance name and the pin name are same, or the base name are same.

For example, the instance name is "I1", the pin name is "I1" or "I1<1>", the system regards those names as illegality.

Pin/Net Name Collision checks whether a pin name is different from a net name.

When the names are different but the bit numbers of name are same, if you select "Ignore", the system will regard those names as legal, otherwise, the system will regard those name are illegal.

For example, in the below figure, the system will report the error messages:

→ ◘"(WARNING/ERROR) SE: Pin name '↑a,b,c'├ collides with net name '↑d,e,f├'."

Verilog Syntax checks the Verilog HDL syntax for instance name and signal name. The system marks signal names or instance names when they collide with Verilog HDL reserved words or when they are invalid Verilog HDL identifiers.

Verilog AMS Syntax checks the Verilog AMS HDL syntax for instance name and signal name. The system marks signal names or instance names when they collide with Verilog AMS HDL reserved words or when they are invalid Verilog AMS HDL identifiers.

VHDL Syntax checks the VHDL syntax for instance name and signal name. The system marks signal names or instance names when they collide with VHDL reserved words or when they are invalid VHDL identifiers.

Instance Name Syntax controls name syntax checking for instances.

Instance Name Expression specifies the regular expression the checker uses in instance name syntax checks. This field is enabled only when the Instance Name Syntax check is set to warning or error.

Pin Name Syntax controls name syntax checking for pins.

Pin Name Expression specifies the regular expression the checker uses in pin name syntax checks. This field is enabled only when the Pin Name Syntax field is set to warning or error.

Net Name Syntax controls name syntax checking for nets.

Net Name Expression specifies the regular expression the checker uses in net name syntax checks. This field is enabled only when the Net Name Syntax field is set to warning or error.

Options field

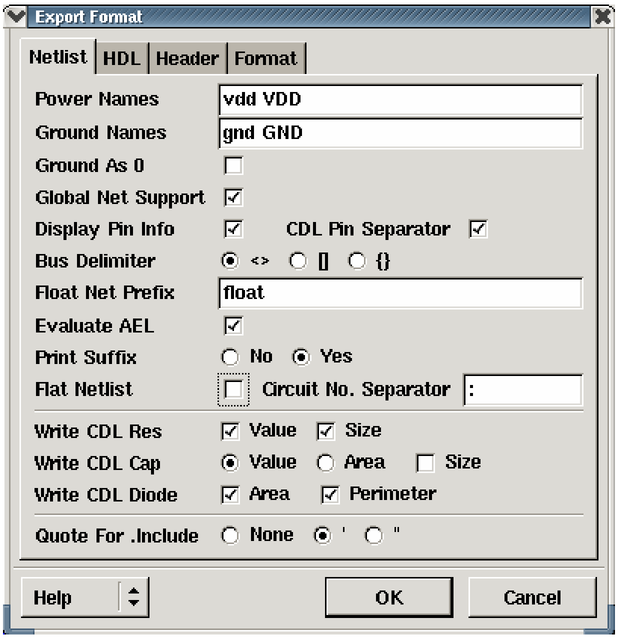
Prompt When 0 Errors/Warnings specifies whether to pop up checking result form when there is no error and warning. Please see *Check->Current Cellview* for details.

Add Default Wire Name After Check system will assign a name to a wire which has not been named by you after checking.

Match Pin Names Exactly specifies whether to check pin names are identical or not when you cross check two views. If “Ignore”*Pin Order Check*, this option will not work. For example, pin name “a<1:2>” is in schematic view, pin names “a<1>”, “a<2>” or “a<2:1>” are in symbol view. If you turn on “Warning” or “Error” options, system will give a warning or error message to you.

1.11.4 Options->Export Format

Netlist tab specifies the rules for generating SPCIE netlist or CDL netlist.



About the form above,

Power Names specifies the power names. If the pin name or net name is the same as one of the name list, netlist generator regards it as power.

Ground Names specifies the ground names. If the pin name or net name is the same as one of the name list, netlist generator regards it as ground.

In general, name must be ended with '!' in *Power Names* and *Ground Names*. If you type the name without '!', the netlist generator will add '!' at the end of the name automatically. But you should assure the net name or pin name with '!' must exist in schematic view.

Ground As 0 lets the netlist generator export '0' instead of the ground signals.

Global Net Support lets netlist generator export statement ".Global" to the netlist file.

Display Pin Info lets the netlist generator export the pin name and pin direction in statement *.PININFO" in CDL netlist.

CDL Pin Separator lets the netlist generator export the separator '/' in CDL netlist, which to distinguish that the pin is either output pin or input pin.

Bus Delimiter specifies the type of bus delimiter. Which delimiter is used depends on your simulator. For example, A<1:2>, A [3:4], A {3:5}.

Float Net Prefix specifies the float net in netlist. The entire name is as "<prefix>#<number>". For example, "float#1".

Evaluate AEL lets the netlist generator calculates the value of AEL in component property. For example, we suppose that the value of "W" is "0.9u", for expression "AD=iPar(W)*0.24u", the value of "AD" is "0.216p".If turn off this option, the value of "AD" is "0.9u*0.24u". About AEL, please refer to ***错误！未找到引用源。*** 错误！未定义书签。.

Print Suffix specifies whether to print unit “u” or “p” to netlist or not. Please refer to ***错误！未找到引用源。*** 错误！未定义书签。.

Flat Netlist lets the netlist generator export the flat netlist, not hierarchical. Export either the flat netlist or hierarchical netlist depends on your simulator.

Circuti No.Separator is special for generation flat netlist. A number followed the separator specifies the hierarchy of a device in hierarchical. For example, we set this separator to ":", a part of flatten netlist is shown as below.

```
M0:1 xdec_en net0 gnd! gnd! nmos
M1:1 xdec_en net0 vdd! vdd! pmos
M0:2 net3 net0 gnd! gnd! nmos
M1:2 net3 net0 vdd! vdd! pmos
```

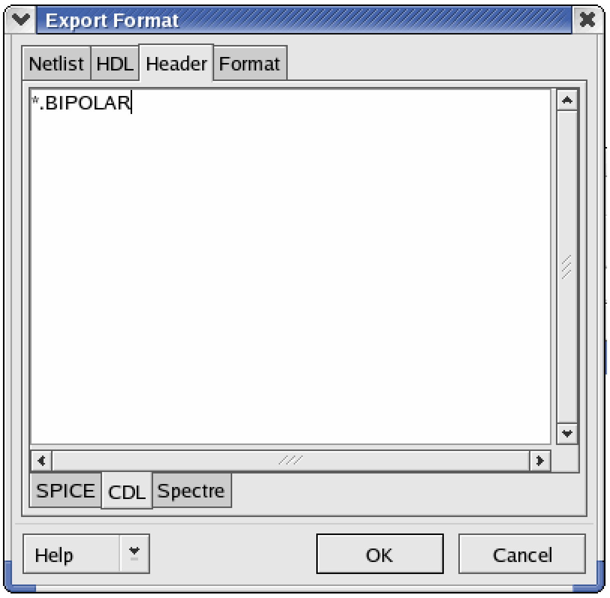
Write CDL Res specifies whether to export the value or (and) size of resistor to CDL netlist or not.

Write CDL Cap specifies whether to export the value or area of capacitor to CDL netlist or not.

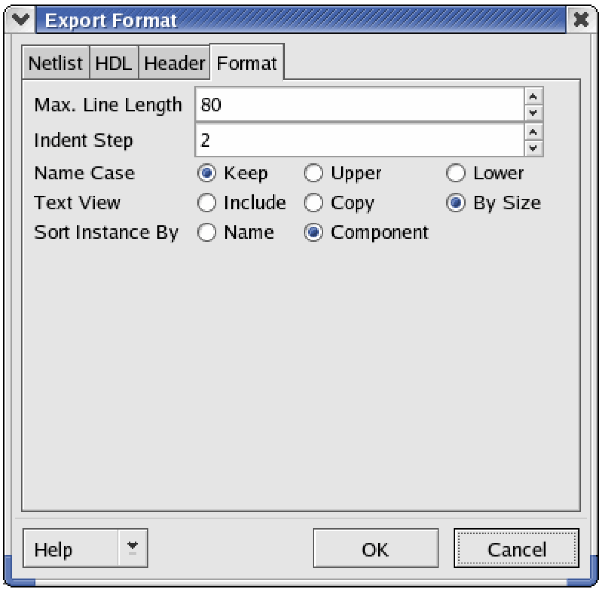
Write CDL Diode specifies whether to export the area ,size (main for capacitor)or (and) perimeter of resistor to CDL netlist or not.

Quote For .Include specifies which quotation mark is used in “.include” sentence according to different simulator.

Header tab lets you type any netlist statement or export spice/cdl/spectre netlist., the netlist generator will add these statements to the head of the netlist.



Format tab specifies the format of the netlist to be generated.



Text view specifies that when you export verilog netlist, if an instance cell has verilog cellview (netlist), netlist generator lets you add the existed verilog netlist to the exported netlist with one of the following methods.

-Include uses 'include' expression to add the existed verilog netlist to exported netlist.

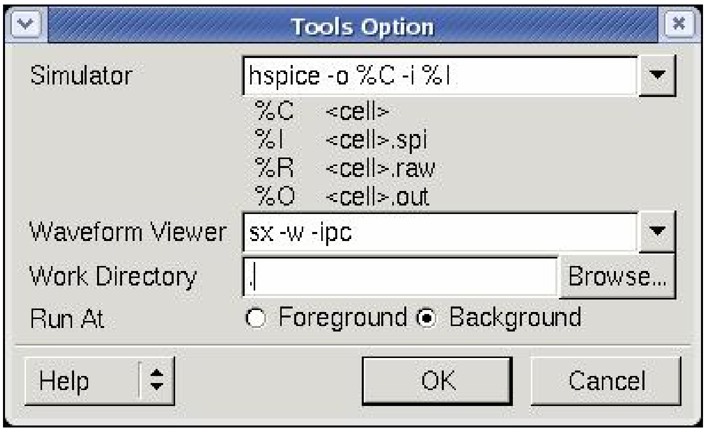
-Copy adds the whole verilog netlist text to exported netlist.

-By size specifies that if the size of existed verilog netlist is equal or larger than 1024 bytes, netlist generator uses *Include* option to generate netlist, otherwise, use

Copy option to do that.

1.11.5 Options->Tools

Select *Options->Tools* to setting up the SPICE simulator you want to use.



Simulator specifies the command line of the SPICE simulator you want to use. Four substitutions are recognized in the command line. They are

%C -- will be replace by the cell name
%I -- will be replace by the cell name suffixing ".spi"
%R -- will be replace by the cell name suffixing ".raw"
%O -- will be replace by the cell name suffixing ".out"

The system provides some common used SPICE commands in the dropdown list. They are

ngspice –r %R –b %I (for ngspice)
spice3 -r %R -b %I – (for Bekeley SPICE 3)
hspice -o %C -I %I – (for Star Hspice)
smartspice -b -r %R %I – (for Smart SPICE)
spectre +spp %I – (for Cadence spectre)
eldo -b -o %O %I – (for Mentor SPICE)
Sim %I %C.sxdat (for SIMetrix)
hsim –o %C –i %N (for HSIM)

WaveformViewer specifies the command of invoking a waveform viewer to show result waveform.
Work Directory specifies the work directory where your simulator is running;
Run At Select the run mode.
Foreground – start the simulation and the system waits its completion.
Background – start the simulation as an external process and the system can accept any other commands after startup the simulator.

1.11.6 Options->Load Options

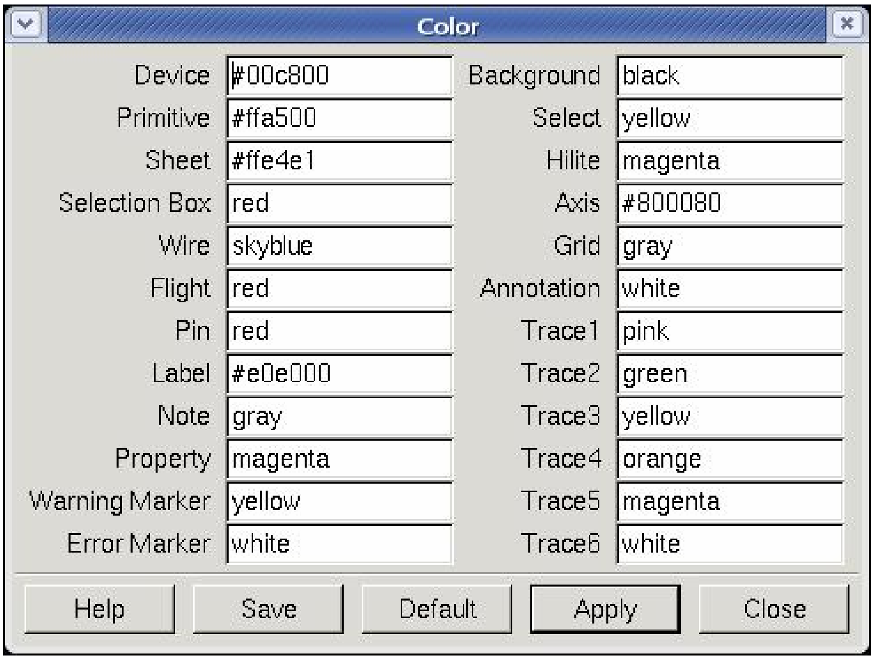
Load all of settings about Editor, Display, Check Rules, Export Format and Set Simulator.
Select *Options->Load Options* and type the setting file in File Name field. This file was saved by command **Save Options** before.

1.11.7 Options->Save Options

Save the current settings about Editor, Display , Check Rules, Export Format and Set Simulator to a setting file. The editor will load this file at the start-up.
Select *Options->Save Options* and type the file name in File Name field. By default, those settings are saved in file either "$HOME/.zeni/se.rc" or "$ZENI_USER_HOME/.zeni/se.rc".
Turn on the **Auto Save On Exit** option, the editor will save those settings automatically when it exits.

1.11.8 Options->Color

Define the colors used in the editing.
Select *Options->Color*, the “Color” form is shown as figure below.



Click **Save** button to save the current settings in color file.
Click **Default** button to load the system defaulted color settings.
Click **Apply** button to use current color settings in current editor only.

1.11.9 Options->Key Mapping

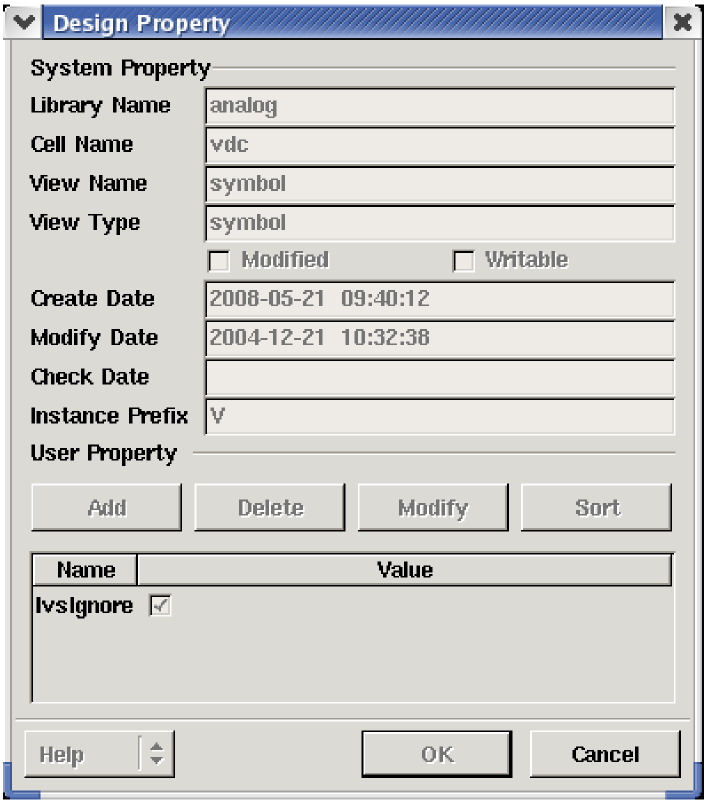
Please refer to *Options->Key Mapping* command of LE.

1.11.10 Options->Toolbox

Please refer to *Options->Toolbox* command of LE.

2 Symbol Editor Command

2.1 Design->Design Property



In *Name* field, type the property name, or select property name from drop-down list. There are special 3 property names "lvsIgnore", "ercIgnore" and "drcIgnore" in this list. *"lvsIgnore"* is a boolean parameter. it is used to design voltage source and current source. If set it to True,

1. SE does not export this view to CDL netlist.
2. SE does not export the view to SPICE netlist, if this view is invoked by another view.

"*ercIgnore*" is a boolean parameter. It is used for libraries "Sheet" and "Spice". If set it to True, SE does not report error message when the view which is no any pin is invoked.

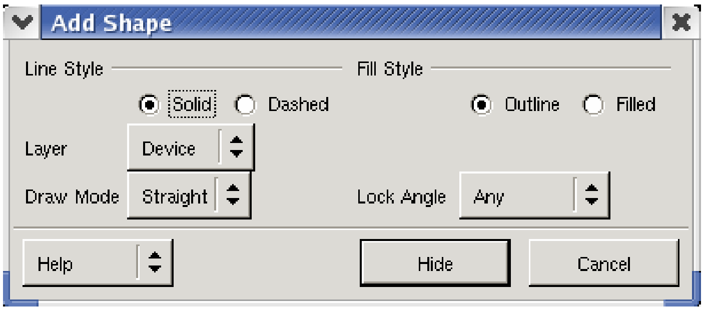
"*drcIngore*" is a boolean parameter. If this view is invoked, SE does not report error message when this view overlaps with another instance.

2.2 Add menu

2.2.1 Add->Rectangle

Draw a rectangle.

Select *Add->Rectangle*, or click icon , “Add Shape” form appears.

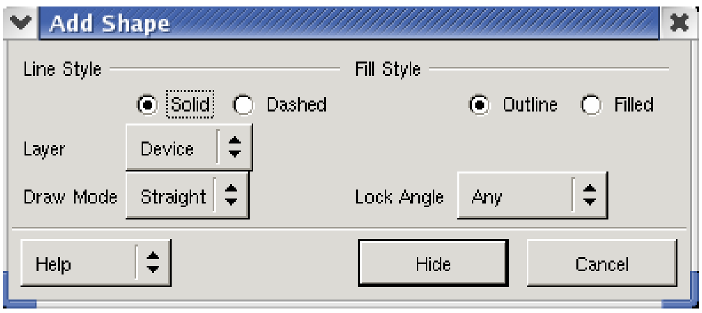


Line Style specifies the outline of rectangle is solid or dashed.
Fill Style specifies whether to fill the shape or not.
Layer specifies this shape is in which layer. Layer type includes *Device, Primitive*, and *Sheet.* Different layer type has different color. Please refer to *Options->Color* for more details.
After setting options, you can move pointer into Symbol Editor window and click to enter the first corner of the rectangle, drag pointer and click to enter the second corner of the rectangle, double click to create the rectangle.

2.2.2 Add->Line

Draw a line.

Select *Add->Line* or click icon , “Add Shape” form appears.



Line Style specifies the line is solid or dashed.
Fill Style specifies whether to fill the shape or not.

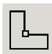
Layer specifies this shape is in which layer. Layer type includes *Device, Primitive*, and *Sheet.* Different layer type has different color. Please refer to SE *Options->Color for* more details.
Draw Mode specifies 5 types mode, there are:
Straight specifies to draw a straight line between two points at following angle:
Any: any angle.
Orthogonal: 90 degrees angle.
Diagonal: 45 degrees angle.
XY specifies to draw line along X-axis first, then along Y-axis.
YX specifies to draw line along Y-axis first, then along X-axis.
L45 specifies to draw line along X-axis or Y-axis first, then along 45 degrees direction.
After setting options, you can move pointer into Symbol Editor window and click to start the line, double click to end the line.

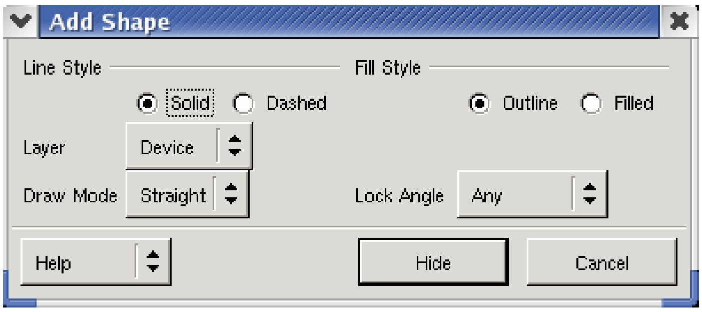
 Note:

You can click right mouse button to modify the drawing mode during drawing.

2.2.3 Add->Polygon

Draw a polygon

Select *Add->Polygon* or click icon , the “Add Shape” form appears.



Line Style specifies outline of polygon is solid or dashed.
Fill Style specifies whether to fill the shape or not.
Layer specifies this shape is in which layer. Layer type includes *Device, Primitive*, and *Sheet.* Different layer type has different color. Please refer to SE *Options->Color for* more details.
Draw Mode specifies 5 types mode, there are:
Straight specifies to draw a straight line between two points at following angle:
Any: any angle.
Orthogonal: 90 degrees angle.
Diagonal: 45 degrees angle.
XY specifies to draw line along X-axis first, then along Y-axis.
YX specifies to draw line along Y-axis first, then along X-axis.
L45 specifies to draw line along X-axis or Y-axis first, then along 45 degrees direction.

After setting options, you can move pointer into the Symbol Editor window and click starting point first, drag pointer and click the second, third ….points of the polygon. Click at the first point again or double click at the last point to complete the polygon.

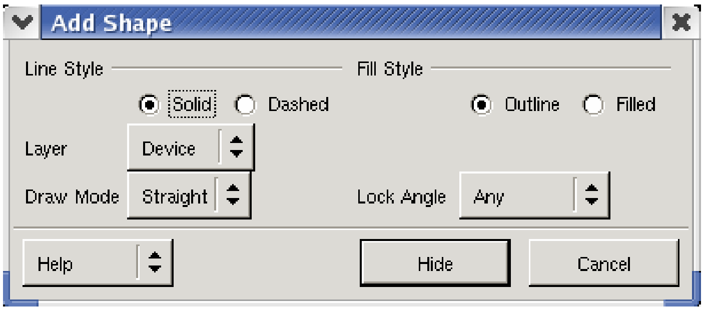
 Note:

You can click right mouse button to modify the drawing mode during drawing.

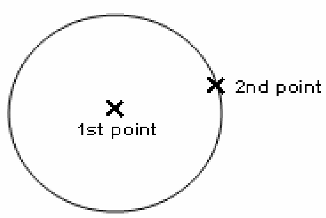
2.2.4 Add->Circle

Draw circle with any radius.

Select *Add->Circle*, or click icon , “Add Shape” form appears.



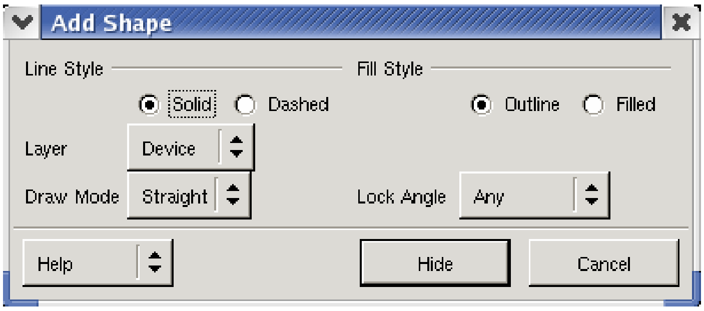
Line Style specifies the outline of circle is solid or dashed.
Fill Style specifies whether to fill the shape or not.
Layer specifies this shape is in which layer. Layer type includes *Device, Primitive*, and *Sheet.* Different layer type has different color. Please refer to *Options->Color* for more details.
After setting options, you can move the pointer into Symbol Editor window and click a point to specify the center of the circle first, move the pointer and click another point to specify the distance of the radius.



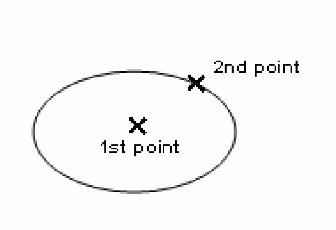
2.2.5 Add->Ellipse

Draw an ellipse.

Select *Add->Circle*, or click icon , "Add Shape" form appears.

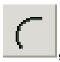


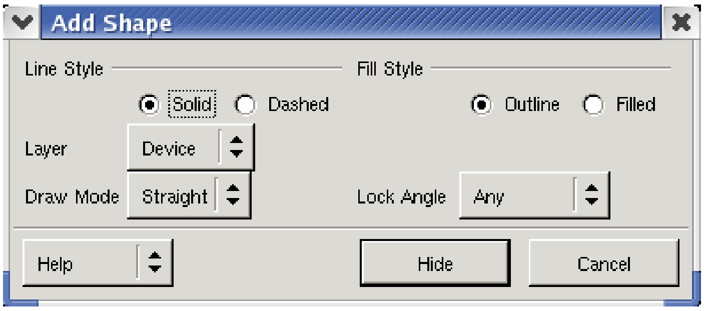
Line Style specifies the outline of ellipse is solid or dashed.
Fill Style specifies whether to fill the shape or not.
Layer specifies this shape is in which layer. Layer type includes *Device, Primitive*, and *Sheet.* Different layer type has different color. Please refer to *Options->Color* for more details.
After setting options, you can move the pointer into Symbol Editor window and click a point to specify the center of the ellipse first, move the pointer and click another point to complete the ellipse.



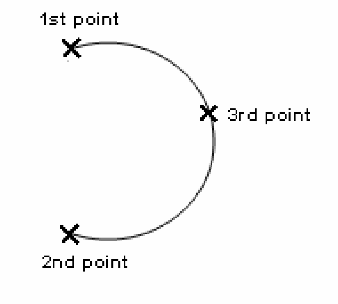
2.2.6 Add->Arc

Draw an arc.

Select *Add->Arc*, or click icon , "Add Shape" form appears.

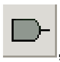


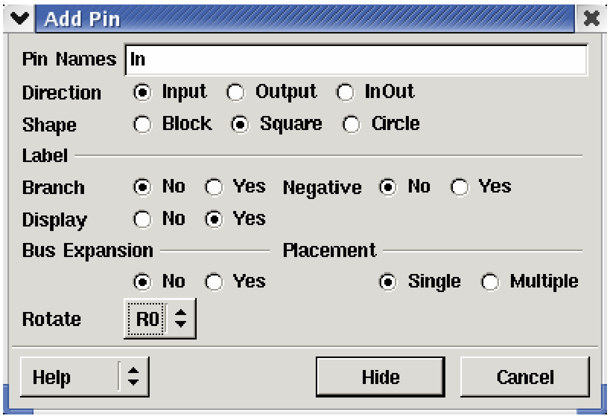
Line Style specifies the outline of ellipse is solid or dashed.
Layer specifies this shape is in which layer. *Layer* type includes *Device, Primitive*, and *Sheet.* Different layer type has different color. Please refer to *Options->Color* for more details.
After setting options, you can move the pointer into Symbol Editor window and click three points to create an arc.
Below figure shows how to create an arc.



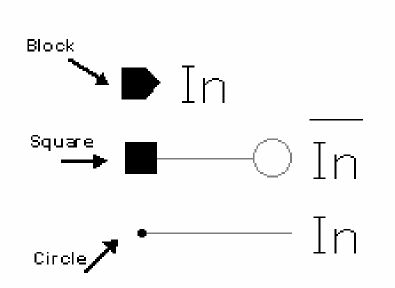
2.2.7 Add->Pin

Create a pin for a symbol.

Select *Add->Pin* or click icon , "Add Shape" form appears.

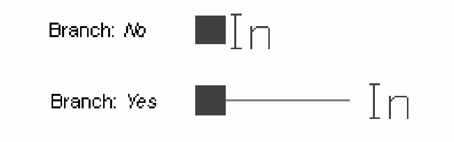


Pin Names lets you type the pin name. You can type multiple names in one job. A space separates each pin name.
Direction specifies the pin direction. There are 3 types: *Input*, *Output* and *InOut*.
Shape specifies the pin shape. There are 3 types: *Block*, *Square* and *Circle*. Please see below figure

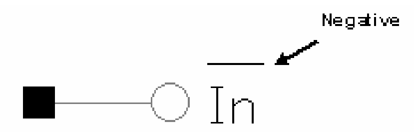


Label section rules how to show the pin name.

Branch controls whether add a line between pin and pin name. This option only acts on *Square* pin and *Circle* pin.



Negative specifies the electrical logic of a pin. If you select *Yes*, an bar is added on the top of pin name.



Display controls whether to display pin name or not. If the pin name has not been display by selection *No* option, you can use command "*Edit->Reset Invisible Label*" to make the pin name appear

Bus Expansion specifies whether expand bus pin to separate pin or not.

For example, there is a pin name "A<1:2>",

If you select *Yes* option, the pin name is expand to "A<1>" and "A<2>".

If you select *No* option, the pin name still is "A<1:2>".

Placement specifies how to place the multiple pin names.

For example, there is a pin name "In1 In2 In3 In4",

If you select *Single* option, the four pins are placed one by one with each clicking.

If you select *multiple* option, click to specify the location of the first pin, other pins will appear and move with the mouse cursor. Click again to place the other pins. The editor uses the distance between the first two pins as a reference to determine the location of the other pins.

Rotate to rotate the pin name with following direction.

R0/R90/R180/R270 specifies to rotate pin name by R0/R90/R180/R270 degrees

MX specifies to flip pin name by X-axis.

MY specifies to flip pin name by Y-axis.

MXR90 specifies to flip pin name by X-axis and rotate 90 degrees.

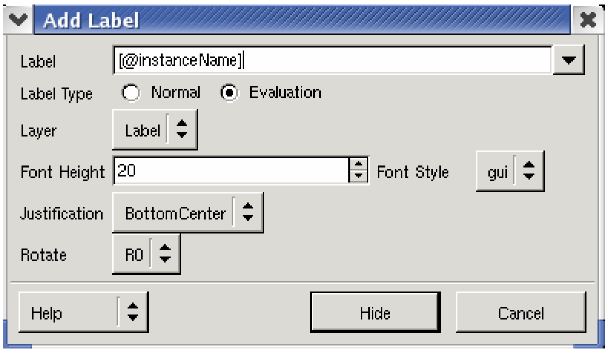
MYR90 specifies to flip pin name by Y-axis and rotate 90 degrees.

2.2.8 Add->Lable

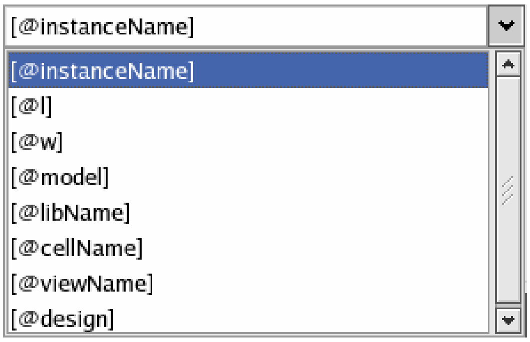
Add label text or parameter for a symbol.

Select *Add->Lable* or click icon 

, “Add Label” form appears.



Label lets you type label text or a parameter name. If the form of label text is like “[@parametername]” and *Evaluation* option is selected, Symbol Editor regards the text as a parameter name. When you add this symbol cellview into the Schematic Editor, Schematic Editor replaces this parameter name with its value, otherwise, Schematic Editor regards it as normal text. In label dropdown list, Symbol Editor pre-defines some labels shown as figure below.



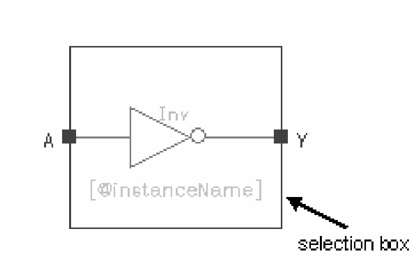
Label Type specifies the type of label. There are two types,
Normal specifies the label is a normal string.
Evaluation specifies the label whose form is like “[@text]” is a parameter name.
Layer is used to change the color of label only. It includes 4 types, Sheet, Primitive, Device and Lable. These 4 colors are specified in *Options->Color*.

2.2.9 Add->Selection Box

This command lets you define an area. This area is used that when you add this symbol cellview to Schematic Editor, Schematic Editor highlights the symbol as long as your cursor is in this area. If you click cursor in this area, this symbol (instance) will be selected. The default selection box is a rectangle that encloses all of the pins and symbol shapes, except Note text.

Select Add->Selection Box or click icon . Move pointer into Symbol Editor window and click one point to locate the top left corner of selection box, move pointer and click again to complete the selection box.

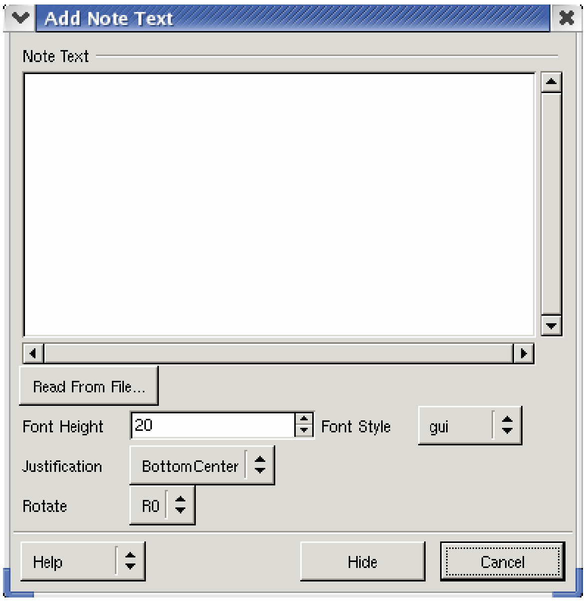
Note: Only one selection box is allowed for a symbol view.



2.2.10 Add->Note Text

Add comments for symbol.

Select *Add->Note Text* or click icon , the "Add Note Text" form appears.



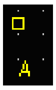
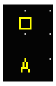
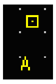
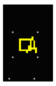
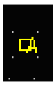
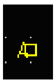
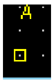
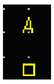
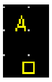
Note Text lets you type comment text in this field.

Read From File allows you add comment text loaded from a text file.

Font Height specifies the height of font.

Font Style specifies the style of font

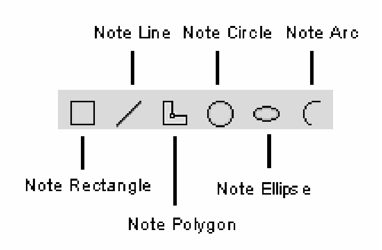
Justification specifies the anchor location. There are 9 types that you can choose, there are:

Justification	Explanation	Illustration
Top Left	The anchor (cursor) locates in the top left of text	
Top Center	The anchor (cursor) locates in the top center of text	
Top Right	The anchor (cursor) locates in the top right of text	
Center Left	The anchor (cursor) locates in the center left of text	
Center Center	The anchor locates in the center of text	
Center Right	The anchor locates in the center right of text	
Bottom Left	The anchor locates in the bottom left of text	
Bottom Center	The anchor locates in the bottom center of text	
Bottom Right	The anchor locates in the bottom right of text	

Rotate to rotate the text with following direction.
R0/R90/R180/R270 specifies to rotate text by R0/R90/R180/R270 degrees
MX specifies to flip text by X-axis.
MY specifies to flip text by Y-axis.
MXR90 specifies to flip text by X-axis and rotate 90 degrees.
MYR90 specifies to flip text by Y-axis and rotate 90 degrees.

2.2.11 Add->Note Shape

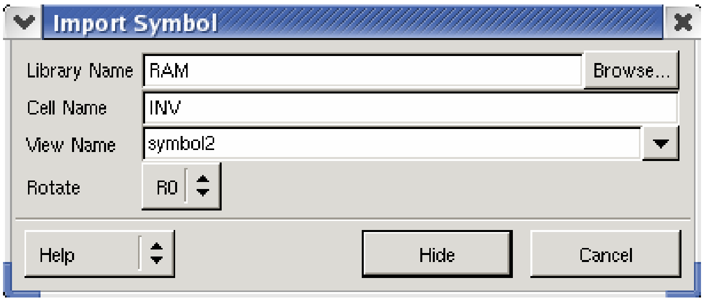
Add graphical note for symbol.
There are 6 types of note shapes; they are *Rectangle*, *Line*, *Polygon*, *Circle*, *Ellipse* and *Arc*.
Select one of shapes from submenu of command *Add->Note Shape*, or click corresponding icon from icon bar.



2.2.12 Add->Import Symbol

This command lets you import an existed symbol cellview to current Symbol Editor window.

Select Add->Import Symbol or click icon. The “Import Symbol” form appears.

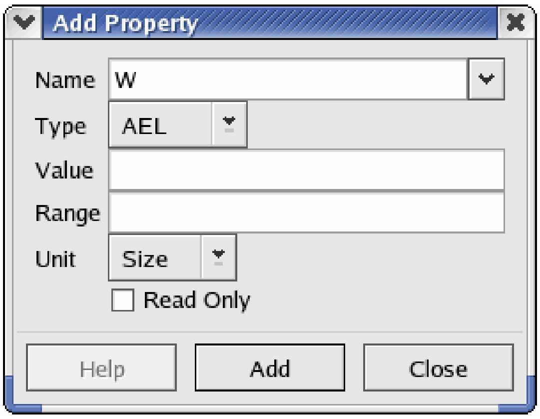


In this form, you can type library name, cell name and view name, or click *Browse* button to select an existed symbol cellview. Move pointer into Symbol Editor window and click to place the imported symbol in the current symbol cellview. You can also click right mouse button to change rotating direction during placing symbol.

3 What is AEL

AEL is the abbreviation of Analog Expression Language. It is used to create component parameter.

If you want to use “W=pPar(xxx)”feature, the parameter “W” must be set to AEL type in *Design->Component Property->Add Property* form.



For AEL type, there are three units Normal, Size and Area.

Nomal has no unit, the netlist absolutely depends on the parameter value.

Size’s unit is ‘u’. If you set the parameter to 5k, then netlist generator will print “5e+09u” to netlist.

Area’s unit is ‘p’. If you set the parameter to 5k, then netlist generator will print “5e+15p” to netlist.

For unit of Size or Area, whether netlist generator print ‘u’ or ‘p’ to netlist depends on Options->Export Format->Print Suffix option. If you turn off the option, the netlist generator will not print the ‘u’ or ‘p’ to netlist. For Normal, Print Suffix option doesn’t work.

Suppose that there are three parameters W, L and AD.

W is set to normal.

L is set to size.

AD is set to Area.

In following tables, we set three values to each parameter, right two columns are the exported value in netlist when turn on/off Print Suffix option.

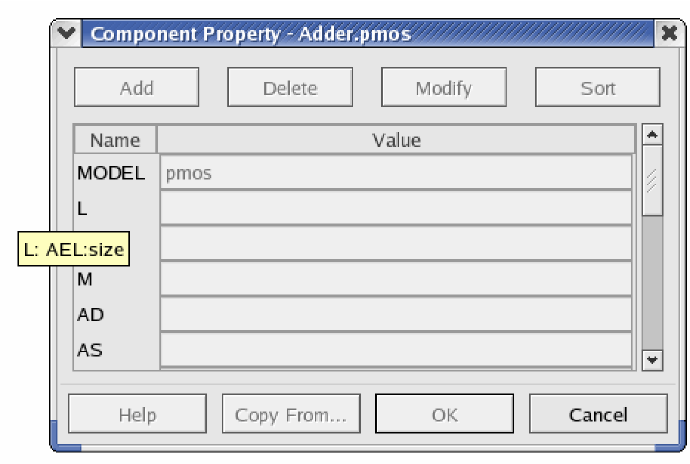
W: Normal	Print Suffix	
Value (W=)	No	Yes
5	5	5
5u	5u	5u

5k	5k	5k

L: Size Value (L=)	Print Suffix	
	No	Yes
5	5	5u
5u	5	5u
5k	5e+09	5e+09u

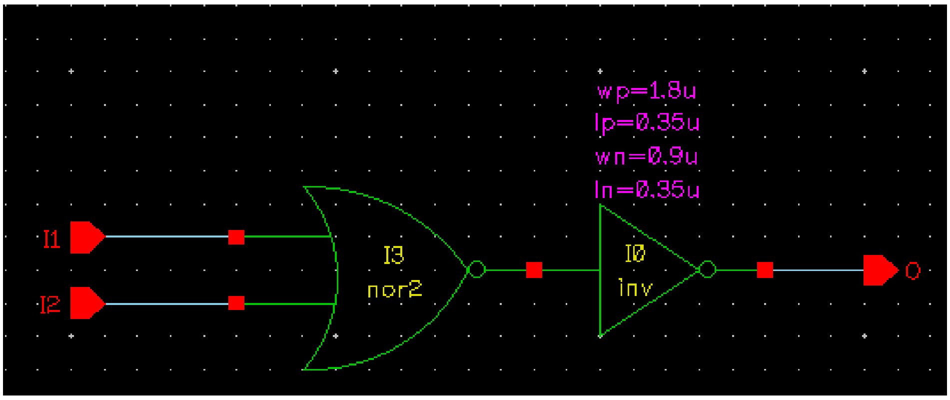
AD: Area Value (AD=)	Print Suffix	
	No	Yes
5	5	5p
5k	5e+15	5e+15p
5kp	5e+15	5e+15p

Open a view, *select Design->Component Property.* In "Component Property" form, put your cursor to a parameter name, a yellow small window will popup after a moment. It is convenient to see the parameter's property from this small window.
For example,

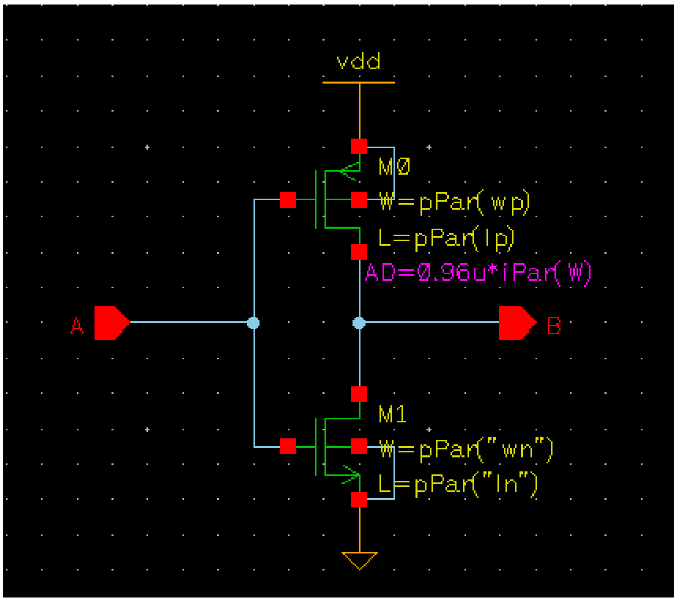


4 What is pPar(), iPar()

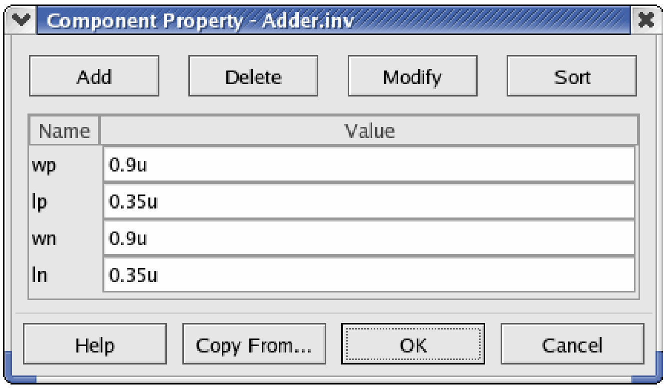
These two expressions are used to inherit parameters.
pPar() inherits parameter from up-level cell.
iPar() inherits parameter from its another parameter.
The format of pPar is pPar("component parameter"). Double quotation marks (" ") can be ignored.
The format of iPar is iPar("another parameter"). Double quotation marks (" ") can be ignored.
For example, there is a schematic cellview window shown as below.



Click icon  to enter the schematic view of instance "I0" shown as below.



For instance “M0” and “M1”, set the parameter W and L to pPar() expression, “wp”, “lp”, “wn” and “ln” are the component parameters of this cellview. Select *Design->Component Property* to check them.



For instance “M0”, set AD to iPar(W) expression, ‘W’ is its another parameter because the area of drain depends on its “W”.

Export hierarchy netlist of the schematic cellview, the sub-circuit inverter’s netlist is shown as below.

```
****************************************
* Library : Adder
* Cell    : inv
* View    : schematic
****************************************

.SUBCKT inv B A wp=0.9u lp=0.35u wn=0.9u ln=0.35u
M0 B A vdd! vdd! pmos L=lp W=wp AD='0.96u*wp'
M1 B A 0 0 nmos L=ln W=wn
.ENDS inv
```

If you export flat netlist of the cellview, the whole netlist is shown as below. The field enclosed by ellipse is the netlist of inverter

```
****************************************
* Library : Adder
* Cell    : or2
* View    : schematic
****************************************

M0:1 0 net0 vdd! vdd! pmos L=0.35u W=1.8u AD=1.728p
M1:1 0 net0 0 0 nmos L=0.35u W=0.9u
M0:2 net0 I2 0 0 nmos L=0.35u W=0.9u
M1:2 net0 I1 0 0 nmos L=0.35u W=0.9u
M2:2 net0 I2 net0:2 vdd! pmos L=0.35u W=1.8u
M3:2 net0:2 I1 vdd! vdd! pmos L=0.35u W=1.8u
```

Netlist generator automatically assign the expression pPar() and iPar() to parameter value.

Netlist generator can calculate the expression’s value because the option *Options->Export Format-> Evaluate AEL* is turned on, otherwise, the parameter “AD” cannot be calculated and exported to netlist as below.

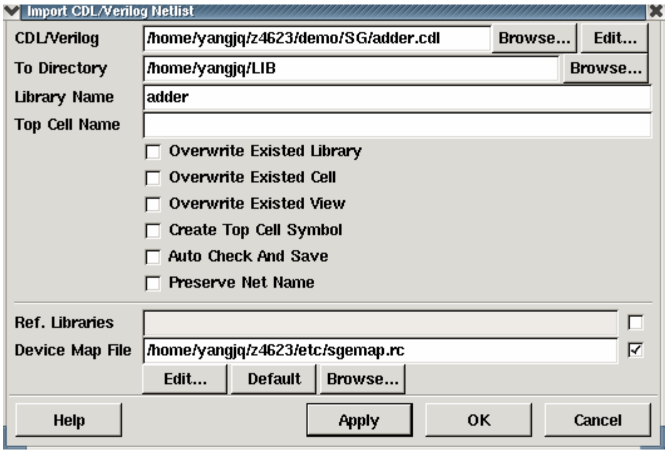
```
M0:1 0 net0 vdd! vdd! pmos L=0.35u W=1.8u AD='0.96u*1.8u'
```

5 How to Import Cadence EDIF File

Please refer to Design Manager Menu *6.1.11.3 File->Import EDIF.*

6 How to Import CDL netlist and Verilog netlist

Zeni translates CDL netlist or Verilog netlist to schematic data.
Select File->Import->CDL/Verilog Netlist, “Import CDL/Verilog Netlist” form appears.



CDL/Verilog chooses a CDL netlist or Verilog netlist you want to translate.
To Directory sets a path to locate the library.
Library Name lets you type library that netlist is translated to.
Top Cell Name regards this cell as the top level cell and only translates the cell and its sub-cells to schematic data. Zeni will translate all of cells to schematic data if the field is empty.
Overwrite Existed Library controls whether to overwrite existed library. If you turn on this option, *Overwrite Existed Cell* and *Overwrite Existed View* are turned on automatically.
Overwrite Existed Cell controls whether to overwrite existed cell. If you turn on this option, *Overwrite Existed View* option is turned on automatically. If you turn off this option, *Overwrite Existed Library* is turned off automatically.
Overwrite Existed View controls whether to overwrite exised view. If you turn off this option, *Overwrite Existed Library* and *Overwrite Existed Cell* are tuned off automatically.
Create Top Cell Symbol creates a symbol view for top cell automatically while

importing.

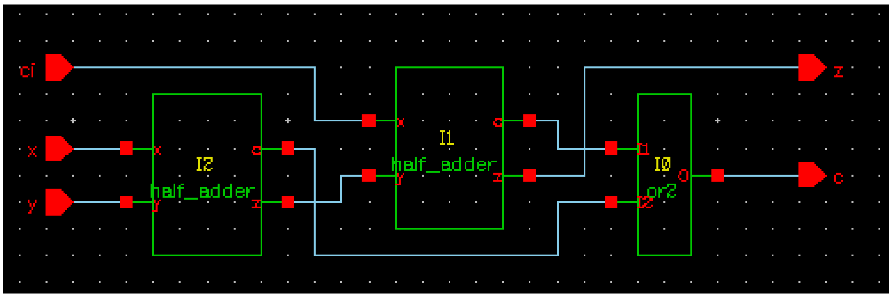
Auto Check And Save checks and saves all of cellviews after importing. If you turn on the option, need not to check full design again before export netlist if you don't modify anything.

Preserve Net Name imports the net label according to the netlist.

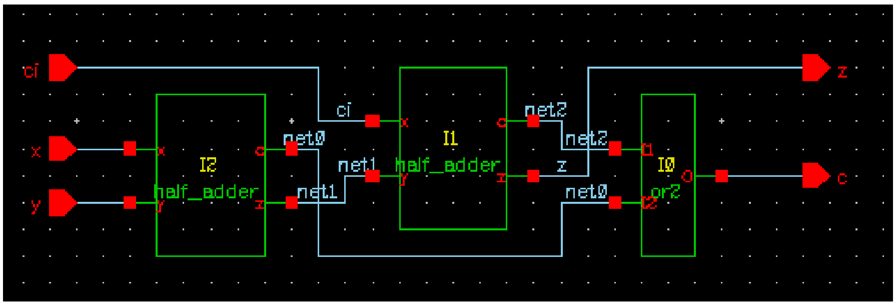
For example, a part of cdl netlist is shown as below.

```
.SUBCKT fulladder c z / ci x y
XI0 c net2 net0 / or2
XI1 net2 z ci net1 / half_adder
XI2 net0 net1 x y / half_adder
.ENDS fulladder
```

Turn off the option "Preserve Net Name", the created schematic is shown as below.



Turn on the option, the created schematic is shown as below.



Ref. Libraries specifies the reference libraries. As there is no any library information in CDL netlist or Verilog netlist, if you turn on this option, Zeni will search cell name from these library one by one to match the cell in netlist. If matching failed or you turn off this option, Zeni will translate cell information to schematic data and create a cell in library.

Device Map File specifies a device mapping table. It is only for translate CDL netlist to schematic data.

Click *Default* button to load the default map file "sgemap.rc". Click *Edit* button to open and view this file.

This file defines the mapping relation of device and global signal. Each line is a definition item.

Device Mapping

For example, a definition item as below.

analog.pmos.symbol M="pmos Pch" d=D g=G s=S b=B w=W l=L

Here,

"analog.pmos.symbol" specifies the library name, cell name and view name of device.

"M" specifies the device is a MOS.

"pmos Pch" specifies the model list of device.

"d=D g=G s=S b=B" specifies the mapping relation of pin name. On the left of "=“ specifies the pin of standard MOS, on the right of "=" specifies the pin name of view "analog.pmos.symbol".

"w=W l=L" specifies the mapping relation of parameter name. On the left of "=" specifies the parameter name in CDL netlist. On the right of "=" specifies the parameter name of "analog.pmos.symbol".

In order to understand clearly, we suppose a definition item as below:

demo.pmos.symbol M="pmos Pch" d=a g=c s=b b=d w=W l=L

As the example shows above, in the CDL netlist, if the device mode is "M" and model name is "pmos" or "Pch", Zeni will reference the device from cell "demo.pmos.symbol". "d", "g", "s" and "b" represent “drain”, “gate”, “source” and “bulk” of device MOS. Zeni is not sensitive to name case on the left of "=". These four names also can be "D", "G", "S" and "B". "a", "c", "b" and "d" are the pin name of "demo.pmos.symbol”. The values of parameter "w" and "l" in CDL view will be past to parameters "W" and "L" of "demo.pmos.symbol".

Suppose that the CDL view and CDL netlist are as follow:

/*-------- CDL view ----------*/

>M? <d> <g> <s> <b> [@MODEL] [@W:W=%] [@L:L=%] [@M:M=%]

/* end */

/*------- CDL netlist --------*/

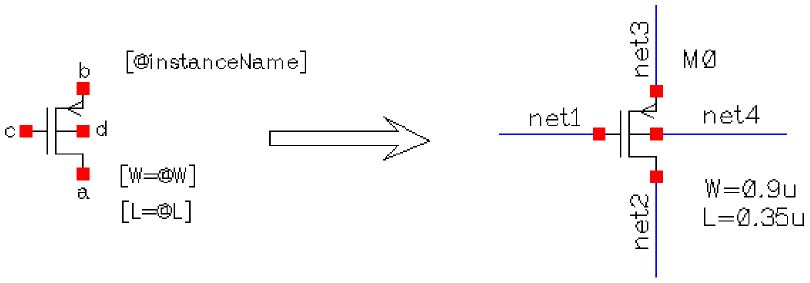
......

M0 net2 net1 net3 net4 pmos 0.9u 0.35u

......

/* end */

Zeni translates this netlist to schematic data as below.



The "demo.pmos.symbol" view

The cell "demo.pmos"
is instanced in schematic view

The left figure above is cellview “demo.pmos.symbol”, according to device map definition “demo.pmos.symbol M="pmos Pch" d=a g=c s=b b=d w=W l=L “, the created schematic data is shown as the right figure.

Global signal Mapping

For example, there are two definition items:

demo.gnd.symbol ground="gnd! gnd 0"

demo.vdd.symbol power="vdd! vcc"

Firstly, Schematic Editor searches string ".gloal" in CDL netlist, if the string is not found, Schematic Editor regards '0' existed in CDL netlist as the Ground and uses "basic.gnd.symbol" in schematic view as default. If the string is found, there will be 3 cases:

Form as ".global xx:P", schematic regards "xx" as Power, so it searches string "power" in device map file and matches the "xx" from the power name list specified on the right of "=". If matching is successful, Schematic Editor uses the symbol specified on the left of "power" as Power symbol in schematic view. Otherwise, Schematic Editor uses "basic.vdd.symbol" as Power symbol in schematic view by default.

Form as ".global xx:G", Schematic Editor regards "xx" as Ground, so it searches string "ground" in device mapping file and matches the "xx" from the ground name list specified on the right of "=". If matching is successful, Schematic Editor uses the symbol specified on the left of "ground" as Ground symbol in schematic view. Otherwise, Schematic Editor uses "basic.gnd.symbol" as Ground symbol in schematic view by default.

Form as ".global xx", Schematic Editor matches "xx" from Power name list and Ground name list respectively. If matching is successful, Schematic Editor uses the specified symbol as Power symol or Ground symbol. Otherwise, Schematic Editor regards "xx" as a global signal, that is, Schematic Editor creates a new pin named "xx!" in schematic view.

7 How to Pre-define Parasitic Parameters

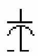
The standard design flow starts with an experienced circuit designer generating a schematic design. The designer must create his/her circuit with anticipated parasitic loads. This is difficult since there is no way to drop in parasitic loads into the schematic. The designer must add resistor/capacitor loads for every net or take a significant risk by ignoring the loads during simulation. Then the parasitic loads must be removed to pass the schematic design to the layout engineer. At this point the layout engineer must complete the layout and perform Parasitic Extraction. The parasitic loads are back-annotated to the schematic and re-simulated by the circuit designer. The whole process cycles again as the designer tweaks schematic devices and makes layout suggestions.

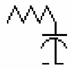
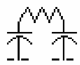
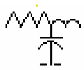
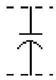
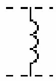
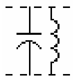
The Pre-Defined Parasitic loads function in the system allows the circuit designer to simulate with pre-defined parasitic parameters, pass the same schematic with design criteria to a layout engineer, and help the layout engineer insure specification while the layout proceeds. The previous repeated cycling between schematic, layout, and back-annotation can be reduced to a single one-way flow.

This chapter describes the following topics:

7.1 Parasitic Loads Symbols

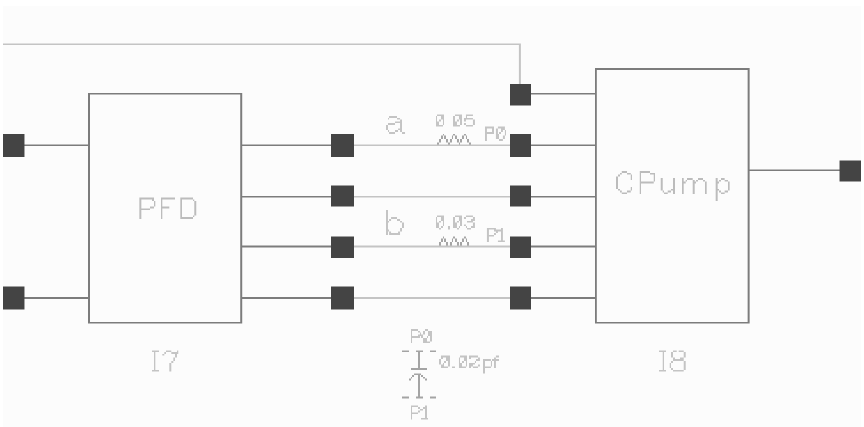
All parasitic loads symbols, listing in the below table, are in the build-in “*basic”* library.

Parasitic Loads	Symbol	Cellview Loaction
Parasitic Resistor		basic.parR.symbol
Parasitic capacitor		basic.parC.symbol
Parasitic Inductor		basic.parL.symbol

Parasitic RC		basic.parRC.symbol
Parasitic RC in ⊓ shape		basic.parRC2.symbol
Parasitic RCL		basic.parRCL.symbol
Coupling Capacitor		basic.coupC.symbol
Coupling Inductor		basic.coupL.symbol
Coupling CL		basic.coupCL.symbol

7.2 Add Parasitic On Wires

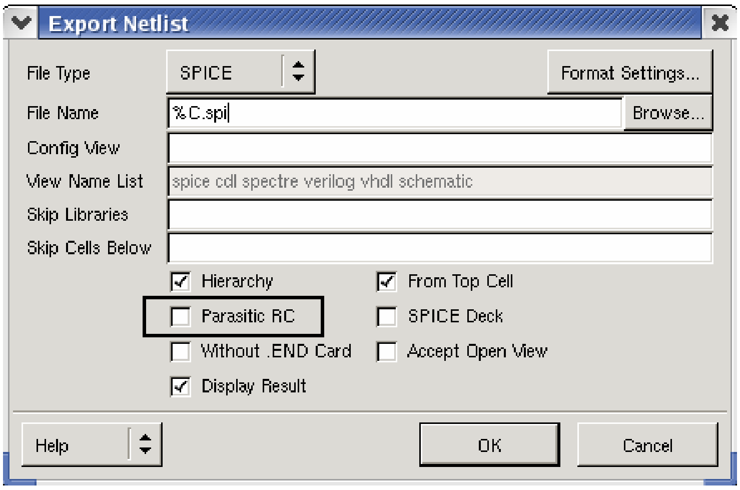
To add parasitic loads,
Click the respect parasitic icon from the top right tool bar, or use the *Add-Instance* command and specify the correct library/cell/view name.
Specify the values for resistor, capacitor, or inductor respectively.
Move the parasitic symbol over the wire segment you want to put on and click.
During moving, the parasitic symbol automatically rotates according to the wire direction on which it overrides. Click right button to rotate it by handwork.
The system repeats the placing action. Press *Esc* to stop.
Note: Do not try to drop parasitic loads on a bus or bundle wire segment. The checker will report errors in these cases and you cannot get the correct netlist to do simulation and other tasks.



In the above figure, we add pre-defined parasitic resistor “P0” to wire “a”, parasitic resistor “P1” to wire “b”, and coupling capacitor between wire “a” and wire “b” is 0.02pf.

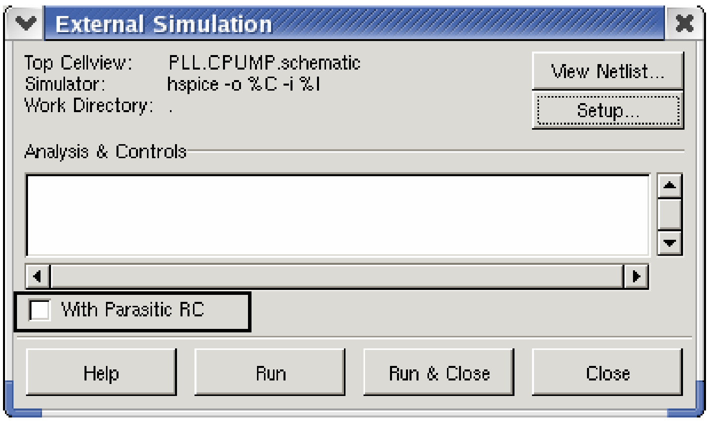
7.3 Export SPICE Netlist With Parasitic Loads

In *Tools->Export Netlist* form, turn on “*Parasitic RC*” option to export parasitic parameters into netlist.



7.4 Simulation With Parasitic Loads

To run simulation with the pre-defined parasitic parameters, turn on the *With Parasitic RC* option in the “Simulation Deck” form or the “External Simulation” form.



8 How To Do Circuit Simulation

There are two ways to do circuit simulation.
Use external tools
Use SPICE Deck simulation platform.

8.1 Using External Simulator

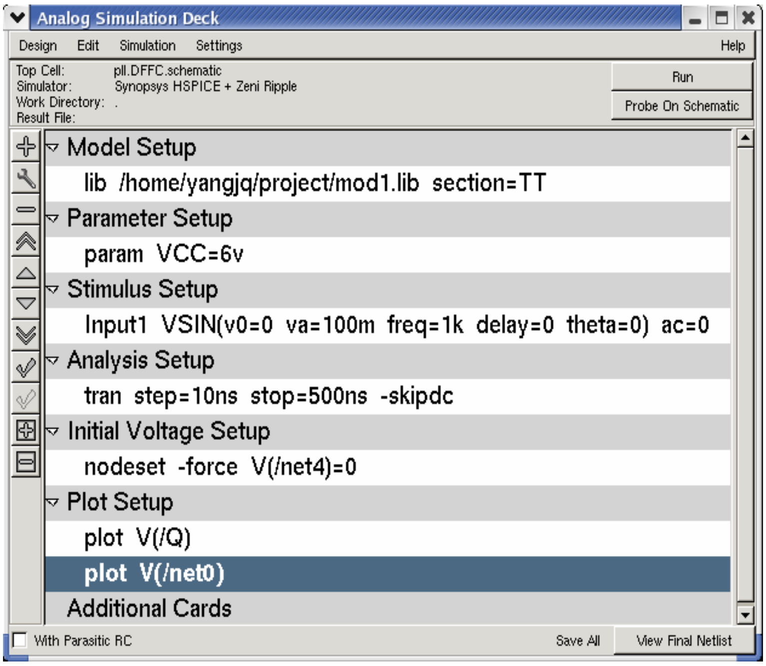
In current schematic cellview window, select *Tools->External Simulation* command to set simulation statement and run simulation.

8.2 Using SPICE Deck Simulation Environment

SPICE deck provides a consistent user interface to make it easy to start your simulation process. It integrates many major SPICE simulator tools.
You can use SPICE Deck to do the following:
Setting Up Simulation Statement
Copy From Another Deck
Setting Up Simulator
Run Simulation
View Log File
View Final Netlist File
Probe Waveform
Load Waveform File
Directly Probing
Automatically Plot Waveforms During Simulation
Plot Waveform In The Savings Section
New Waveform Window
Back-annotate DC Values

Select "*Tools->SPICE Deck*" or click icon 

. The "Analog Simulation Deck" panel appears.



The top left corner of the panel lists the top level cell name of the design to be simulated, simulator name, working directory and the name of the result waveform file, the result waveform file name will be automatically shown after doing “*Simulation->Run*” or “*Simulation->Load Results*” command.

The default top level cell is the schematic in which you start up the SPECK Deck command. You can also change it to another design through command “*Design->Load”*.

Use command “*Design->Open Schematic”* or command *“Design->Open Schematic (Read-only)”* to open corresponding schematic cellview window.

There is an icon bar in the left side of the window as shown below.

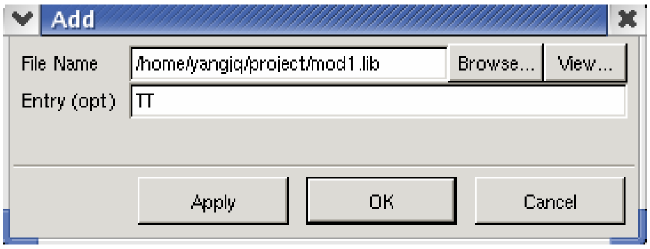
Icon	Command	Explanation
	Edit->Add	Add a setup item
	Edit->Change	Change a setup item
	Edit->Delete	Delete a setup item
	Edit->Move Top	Move a setup item to the top of all setup items in one setup section

	Edit->Move Up	Move a setup item ahead
	Edit->Move Down	Move a setup item behind
	Edit->Move Bottom	Move a setup item to the bottom of all setup items in one setup section
	Edit->Enable	Enable a setup item
	Edit->Disable	Disable a setup item
	Edit->Expand All	Expand all setup sections
	Edit->Collapse All	Fold all setup sections.

The main area of the panel shows the 7 simulation sections you need to define, including
Model Setup
Parameter Setup
Stimulus Setup
Analysis Setup
Initial Voltage Setup
Plot Setup
Additional Cards
These setup sections define the simulation environment, the stimulus to your design, the analysis you want to do, and the waveform you want to save, etc. The editing details will be explained in the following sections. To save any changes, use command "*Design->Save".*
After setup your simulation cards, you could simply click *Run* button to start the simulation and plot the waveform by probing nodes or terminals from the schematic cellview window.

8.2.1 Setting Up Simulation Statement

Setting Up Model Including
Double click *Model Setup* title, or select *Model Setup* title and click icon, the "Add" form appears.



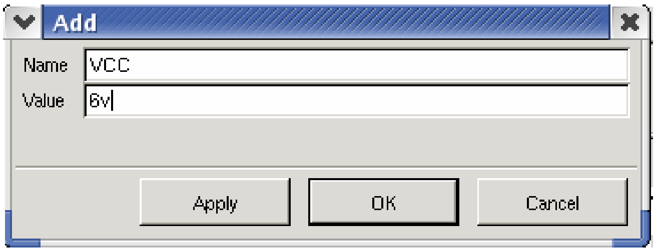
Specify the model file name in *File Name* field or click *Browse* button to pop-up the *File Selection* dialog. Click *View* button to open this file to read.

Specify the optional section name in the model file in *Entry (opt)* field

Click *Apply* or *OK*.

Setting Up Parameters

Double click *Parameter Setup* title, or select *Parameter Setup* title and click icon, the "*Add"* form appears.



Specify the parameter name in *Name* field;

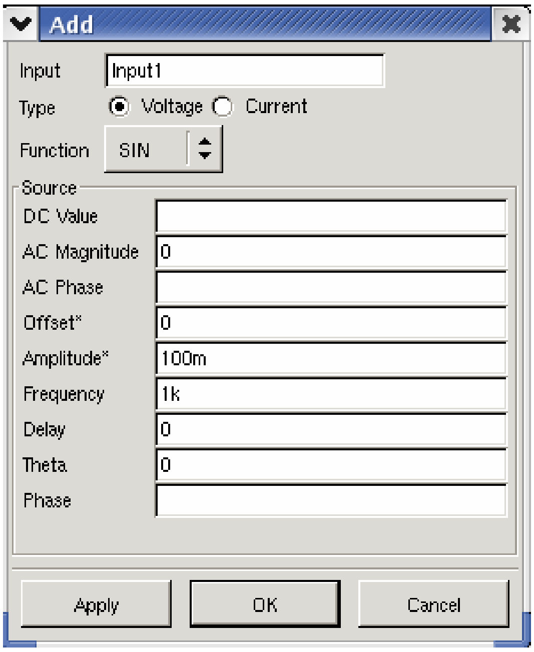
Specify the parameter value or expression in *Value* field.

Click *Apply* or *OK*.

Setting Up Stimulus

When a new deck is created, the top cell input pins and global pins are listed in the *Stimulus Setup* section. Whenever you change the schematic, please use "*Edit->Reload Inputs"* to update this pin list. Note that you cannot add or delete a pin from the list directly. It totally depends on the schematic and can be changed only through the *Reload Inputs* command.

Double click *Stimulus Setup* title, or select *Stimulus Setup* and click icon, the "Add*"* form appears.



Type the pin name in *Input* field.

Select the source type from *Voltage* or *Current*.

Select the source function from.

DC -- direct current

EXP -- exponential waveform

PULSE -- pulse waveform

PWL -- piecewise linear waveform

SFFM -––single frequency FM source waveform

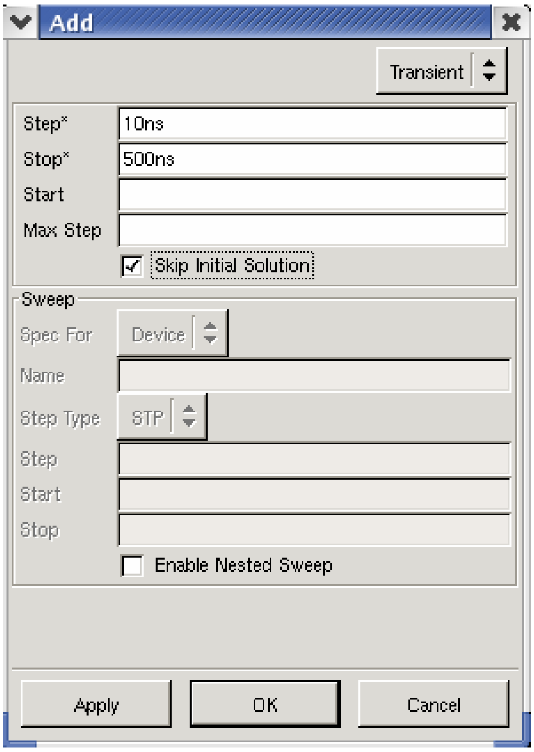
SIN -- sinusoidal waveform

Type other parameter values in the dialog. The parameters displayed in the dialog depend on the source function you selected. Refer to your simulator documents for details on setting these parameters.

Click *Apply* or *OK.*

Setting Up Analyses

Double click *Analysis Setup* title or select *Analysis Setup* title and click icon, the “Add” form appears.



Select the analysis type from top right corner of the form

Transient -–– transient analysis

DC--- direct current analysis

AC -- AC small-signal analysis

OP -–—operation point analysis

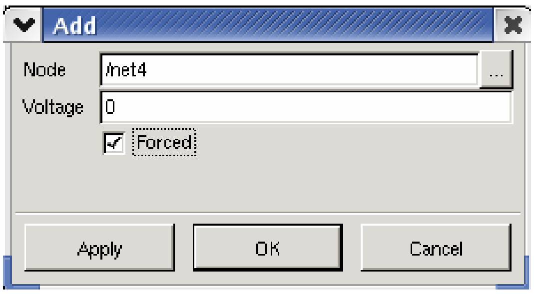
NOISE -- noise analysis

Specify other parameter values in the dialog. The parameters displayed in the dialog depend on the type you selected and the simulator you are using. Refer to your simulator documents for details on setting these parameters.

Click Apply or OK.

Setting Up Initial Voltages

Double click *Initial Voltage Setup* title or select *Initial Voltage Setup* title and click icon, the “Add” form appears.



Specify the node name. Use “…” button to select the node in schematic cellview window.

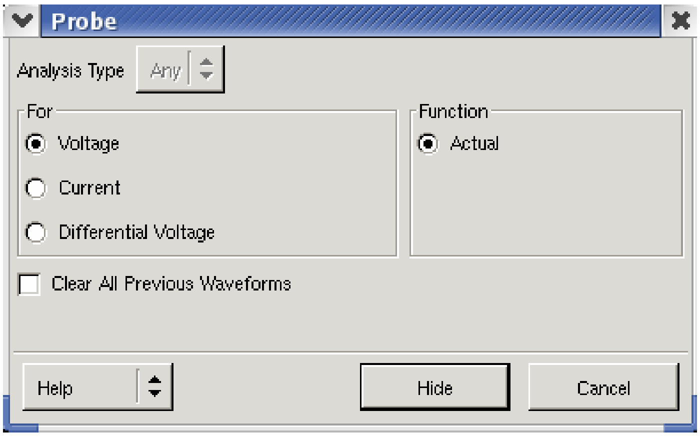
Specify the initial voltage value.

Turn on *Forced* button whenever you mean the voltage is an initial condition, otherwise the voltage is only an initial guess.

Click *Apply* or *OK*.

Setting Up Plot Saving

Double click *Plot Setup* title or select *Plot Setup* title and click icon, the “Probe” form appears.



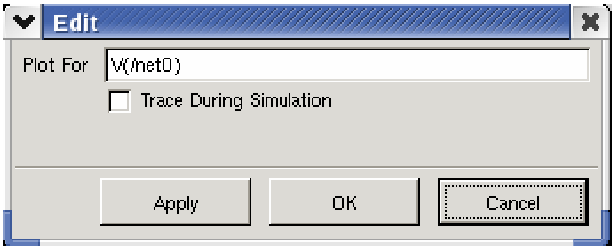
Specify Analysis Type to Any and Function to Actual.

Select probe type.

Mode point into schematic cellview window, select the corresponding net or pin you want to plot.

The selected node or pin expression is added to the plot section automatically.

Double click one item in *Plot Type* section, or select the item in *Plot Type* section and click icon to modify it.

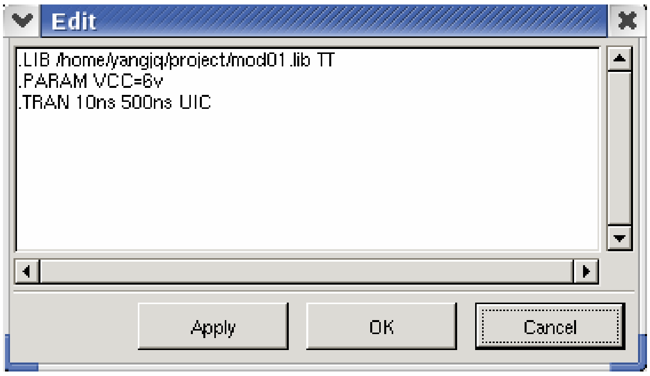


Turn on *Trace During Simulation* to let the simulator plots the waveform in real-time during the simulation process. This option depends on the simulator you are using. Refer the simulator documents to settle whether this feature is supported;

Setting Up Additional Cards

Additional card provides a way to let you enter any other simulation statements other than above sections, such as an advanced analysis special for your simulator.

Double click *Additional Cards* title or select *Additional Cards* title and click icon, the “Add” form appears.

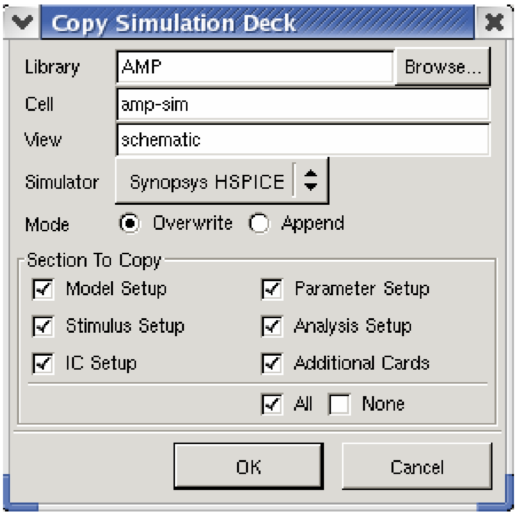


Type any simulation statements in the text area. The syntax of the simulation statements depend on the simulator you are using. Refer to your simulator documents for details on setting them.

Click *Apply* or *OK*.

8.2.2 Copy From Another Deck

To copy a deck contents from another cell or another simulator related design, select *Design->Copy From,* the *Copy Simulation Deck* form appears.



Specify the cell or the simulator you want to copy from.

Select the copy *Mode*. *Overwrite* mode totally overwrites the current deck with the copy one, *Append* mode appends the copy one to the current deck;

Select the sections you want to copy in *Section To Copy* section. For convenience, use *All* to select all the sections and use *None* to reset all;

Click OK to copy.

8.2.3 Setting Up Simulator

Before running simulation you could setup your used simulator. The system supports 5 types of simulators shown as below:

SIMetrix

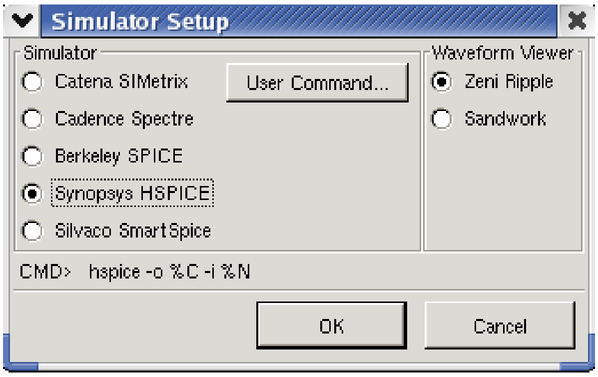
Cadence Spectre

Berkeley SPICE

Avant! Star-Hspice

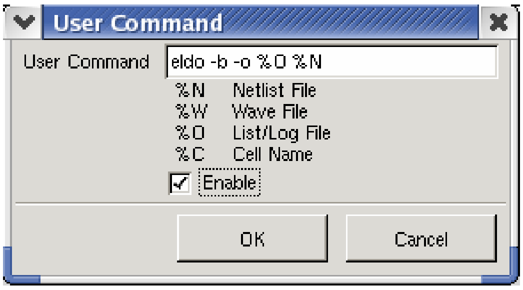
Silvaco SmartSpice

To do setup, use *Settings->Simulator Setup*. “Simulator Setup” form appears.



Select the simulator you used.

For the external simulators other than these 5 types of simulators, use *User Command* to specify the command. The system will run these simulators in the Zterm window



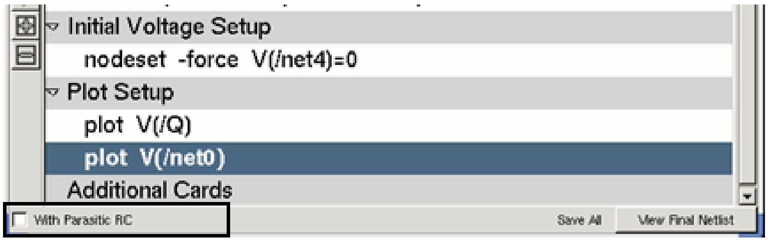
Turn on *Enable* option and click *OK*. The name of the selected simulator will be displayed on the top left corner of the deck window.

8.2.4 Run Simulation

To start the simulation, use *Simulation->Run* or simply click *Run* button on the top right corner of the deck panel. The simulation process depends on the simulator you are using. Refer to your simulator documents for details of their outputs.

The simulator will be run in the working directory which can be set through *Options->Tools* in the schematic editor window.

If you need to simulate with the per-defined parasitic, please check the *With Parasitic RC* button on the bottom left corner of the panel.



8.2.5 View Log File

Select *Simulation->View List File* to view the log file generated by the simulator

8.2.6 View Final Netlist File

Select *Simulation->View Final Netlist File*, or simply click *View Final Netlist* button on the bottom right corner of the deck panel to view the final netlist file, which includes the netlist extracted from schematic hierarchy and the statements defined in the deck.

8.2.7 Probe Waveform

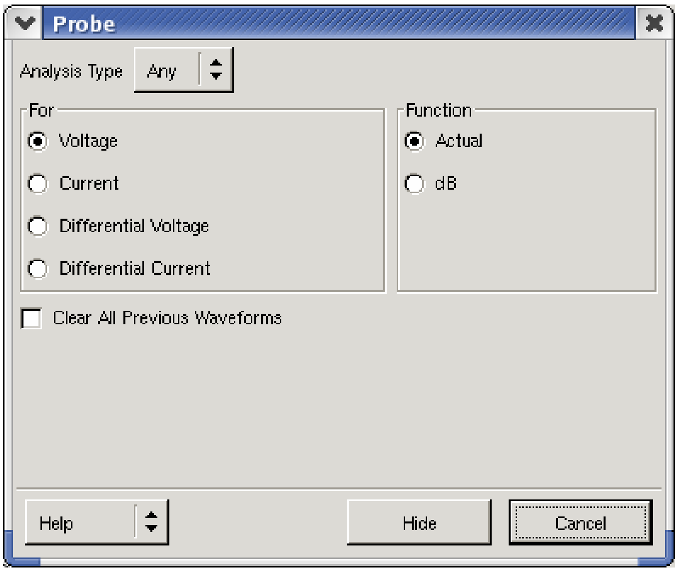
For simulator of SIMetrix, the system supports probing functions.
Probing directly show waveform by directly click nodes or terminals on schematic cellview window.
Automatically plot after simulation define a group of waveforms that can be shown when simulation is completed.

8.2.8 Load Waveform File

Before probing waveforms you should load the waveform file. This can be done through *Simulation->Load Results.* Nothing for the build-in support of SIMetrix, the waveform file is automatically loaded whenever the simulation is completed, and you can do probing directly after simulation.

8.2.9 Directly Probing

Selecte *Simulation->Probe On Schematic* or directly click the *Probe On Schematic* button on the top right corner of the deck window.
According to different simulator, “Probe” window displays different content.
For example, if simulator is SIMetrix, “Probe” form is shown as below.

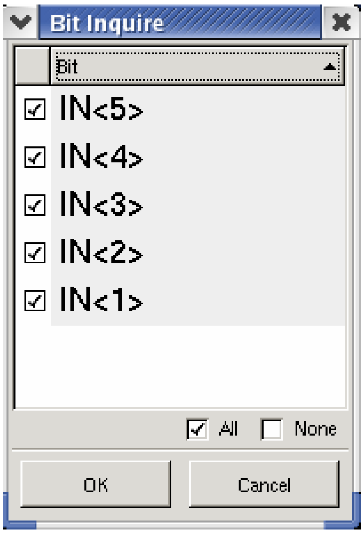


Select the Analysis Type from,
Any -- for results of current analysis.
TRAN -- only for results of transient analysis.
DC -- only for results of DC analysis.
AC -- only for results of AC analysis.

Select *Function* from
Actual -- transient voltage or current, or magnitude for AC results.
dB -- decibel scale.
Phase --AC phase of voltage or current.
Group Delay -- group delay of voltage or current.
Fourier Analysis -- fourier transform of waveform.
Nyquist -- nyquist transform of waveform.

Select the probing type from
Voltage -- voltage of node.
Current -- current of terminal.
Voltage Different -- differences between two voltages of node.
Current Different -- differences between two currents of terminal.
Power -- power of device (only for TRAN and DC).
Impedance -- impedance of terminal (only for AC).

If the net or pin is a bus or a bundle, a bit-selection dialog pops in which you select the bits you want to plot



The corresponding waveforms are plotted in the waveform viewer.

8.2.10 Automatically Plot Waveforms During Simulation

To automatically plot a waveform while simulation, turn on the *option of the plot setting*. Refer to the *Plot Setup* section for details.

8.2.11 Plot Waveform In The Plot Section

To plot waveform listed in the *Plot Setup* section, select it first and click *Simulation->Plot Selected Output*.

8.2.12 New Waveform Window

Select *Simulation->New Wave Window* to open a new waveform window,
Select *Simulation->New Wave Sheet* to open a new sheet in current waveform window
The sequential probing displays the waveforms on the new window or sheet.

8.2.13 Back-annotate DC Values

Select *Simulation->Back Annotate DC Voltage/Current* to back-annotate DC voltage/current to schematic cellview window.
Select *Simulation->Clear Back Annotation* to clear the back-annotations from schematic cellview window.