A Pseudo Differential Complex Filter for Bluetooth With Frequency Tuning

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***Abstract*—A 12th-order OTA-C complex filter with a nonconventional frequency tuning for a Bluetooth receiver is implemented in a low-cost mainstream 0.35-μm CMOS process. This proposed frequency tuning scheme is simpler than the conventional one based on phased-locked loop (PLL). Furthermore, a high-speed pseudo differential OTA using common-mode feedforward (CMFF) and common-mode feedback (CMFB) strategy is proposed. The filter bandwidth is 1 MHz and is centered at 2 MHz. Image and adjacent channels are attenuated by more than 45 and 27 dB, respectively. The integrated input referred noise is 29 μV_{rms}, and the filter chip dissipates 4.7 mA from a 2.7 V supply. The theoretical and experimental results are in good agreement.**

***Index Terms*—CMOS analog IC, Bluetooth circuits, complex filters, OTA-C, Gm-C filters.**

I. Introduction

RECENT RF receiver designs involve either high IF, low-IF or direct-conversion architectures [1]. The selection of different intermediate frequencies results in different circuit implementation tradeoffs. A high-IF receiver, which uses an IF much larger than the signal-channel bandwidth, requires high quality factor off-chip filter; hence, reducing the system integration level, and consuming extra power to drive the external filter. In addition, the high IF choice also increases the complexity of the IF band circuits and causes more power dissipation in the IF stage. In a baseband Bluetooth signal, 99% of the signal power is contained within the dc to 430-kHz bandwidth. Therefore, if a direct-conversion architecture is used, the flicker noise and dc offset might significantly degrade the signal-to-noise ratio (SNR). Hence, a low-IF architecture seems to be a suitable architecture in Bluetooth, especially when considering the relaxed image rejection requirement in Bluetooth standard [2]. To relax the image rejection requirement and reduce the folded-back interference level, a very low-IF is preferable, i.e., half of the channel bandwidth. However, such a very low-IF requires a sharp cutoff from the channel selection filter to reject the dc offset and flicker noise. On the other hand, a higher IF improves the demodulator performance, but the required selectivity of the channel selection filter will increase, and power consumption will be higher. As a good compromise, an IF of two times the channel bandwidth is chosen, i.e., 2 MHz. For a low-IF Bluetooth receiver, the image signal is an inband Bluetooth modulated adjacent channel interference, which becomes cochannel interference after frequency downconversion. It has been verified that an image rejection of 33 dB is sufficient to meet the Bluetooth specifications [3]. For the on-chip image rejection, there are several potential architectures: Hartley architecture, Weaver architecture [1], passive *RC* polyphase filter and active polyphase filter. For the Hartley architecture, the high-channel bandwidth to IF ratio makes the design of the 90° phase shifter very difficult. Weaver architecture requires an extra set of mixers, a frequency synthesizer, and high-order bandpass filters to reject the second image; thus, the power consumption and silicon area penalty is high. Polyphase filter (also called complex filter) can be used in front of the ADC or it can be embedded in a $\Sigma\Delta$-ADC loop [4]. Passive *RC* polyphase filters can achieve high-image rejection ratio [5]. However, due to their limited selectivity, they cannot achieve the required attenuation of the adjacent channel interference, especially those strong folded-back interferences. Extra filtering is then required to reject the adjacent channel interference, which is also true for Hartley and Weaver architectures. Another drawback of a passive *RC* polyphase filter is that the finite input impedance loads the RF mixers. Fortunately, an active complex filter can achieve good image rejection and adjacent channel interference rejection. Fig. 1 shows one embodiment of the low-IF receiver [3]. The RF signal is amplified and down-converted to IF by the RF front end, then, the channel selection is performed by an active complex filter, which is described and proposed in this paper, and next the IF signal is passed through an amplitude limiter which removes any amplitude perturbations. As a final stage, a frequency modulation format (GFSK) demodulator is employed [6].

The Bluetooth standard allows a transmitted center frequency offset as large as ± 100 kHz in one time slot [2]. If the frequency offset cannot be cancelled before the channel-selection filter, the passband of the filter has to be extended to pass the desired signal with frequency offsets up to 100 kHz. Since 99% of the baseband signal power is contained within 430-kHz band, the complex filter passband becomes $2(430 + 100) = 1060$ kHz centered at 2 MHz.

Complex filter designs were found in the literature [7]–[10]. However, these filters either consume significant power and area (e.g., [8], the filter draws 90 mA from 5-V supply and occupies an area 7.5 mm^2), or use a well-controlled special analog process (e.g., in [7], the process parameters are controlled within 1%). Other complex filters are reported as part of the receiver design and, therefore, details about the filter performance were not given [10].

Partial results of the proposed complex filter have been reported in [3]. In this work, a pseudo differential OTA-C complex

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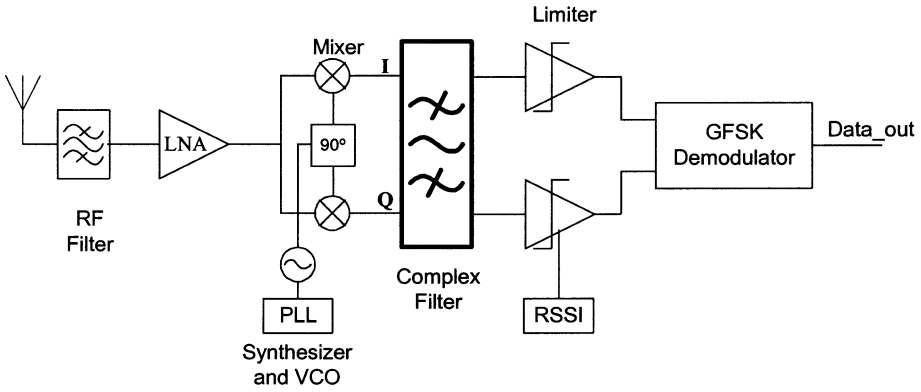


Fig. 1. Low-IF Bluetooth receiver architecture [3].

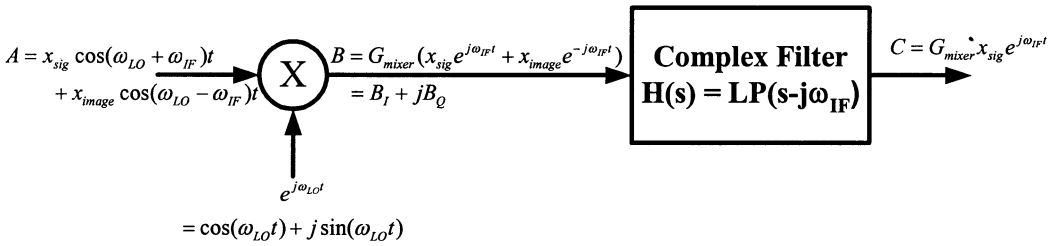


Fig. 2. Receiver image-rejection architecture in the complex domain.

filter is designed and tested. A pseudo differential OTA is used to improve filter linearity and device area. A nonconventional frequency tuning scheme, simpler than conventional frequency tuning techniques, is used to compensate for process variations in a mainstream low-cost TSMC 0.35-μm CMOS process. This makes a good step toward a highly-integrated, low-cost Bluetooth receiver.

II. Complex Filter Theory

Complex filters [11] are not new. However, to justify how to implement them, a brief theoretical discussion follows. To understand the ability of complex filters to reject the image signal, consider the complex representation of the receiver block diagram shown in Fig. 2. For the sake of illustration, we will assume that only the desired signal and its image are present at the mixer input. Without loss of generality, we will assume the signal and the image frequencies are $\omega_{\rm LO}+\omega_{\rm IF}$ and $\omega_{\rm LO}-\omega_{\rm IF}$, respectively. After eliminating the double local oscillator (LO) frequency term by the mixer output low-frequency pole, the result of mixing the LO and RF signals in the complex domain is

$$B = G_{\rm mixer}(x_{\rm sig}e^{i\omega_{\rm IF}t} + x_{\rm image}e^{-i\omega_{\rm IF}t}) = B_I + jB_Q \quad (1)$$

B_I and B_Q are the real and imaginary parts of the mixer output and can be expressed[1] as

$$\begin{aligned} B_I &= G_{\rm mixer}(x_{\rm sig}\cos(\omega_{\rm IF}t) + x_{\rm image}\cos(\omega_{\rm IF}t)) \\ B_Q &= G_{\rm mixer}(x_{\rm sig}\sin(\omega_{\rm IF}t) - x_{\rm image}\sin(\omega_{\rm IF}t)). \end{aligned} \quad (2)$$

Note that in (2), the desired (image) signal in the I branch leads (lags) the Q branch by 90°. Fig. 3 illustrates the complex mixing operation on the desired signal and its image. Note that after down-conversion, the $2\omega_{\rm IF}$ frequency separation between the signal and the image is still preserved. The complex channel select filter [11] is then a frequency-shifted version of a low-pass filter response. This means that the filter passes the signal at $\omega = \omega_{\rm IF}$, while attenuates the signal at $\omega = -\omega_{\rm IF}$. Since the

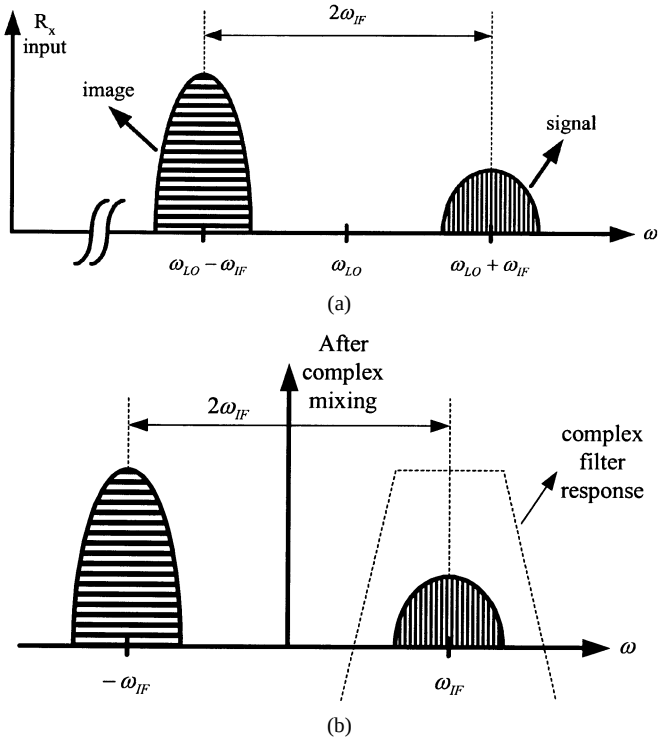


Fig. 3. Frequency translation of a complex (quadrature) mixer. (a) Before complex mixing (signal A in Fig. 2). (b) After complex mixing (signal B in Fig. 2).

[1]Note that the notations I and Q in Fig. 1 correspond to B_I and B_Q, respectively in Fig. 2.

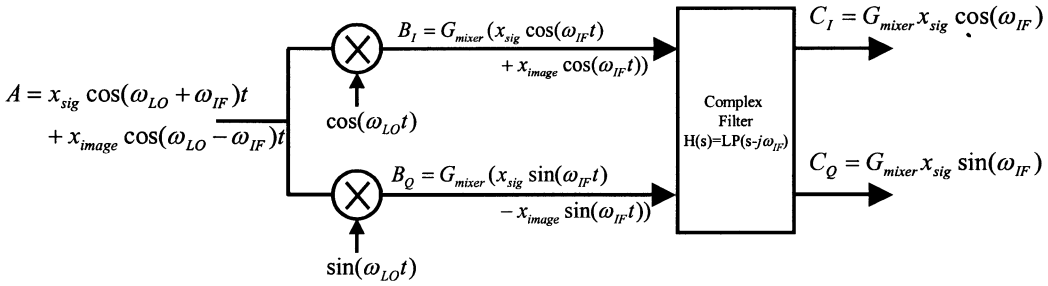


Fig. 4. Practical implementation of the receiver image rejection architecture in Fig. 2.

filter has unsymmetrical frequency response around the $j\omega$ axis, its time-domain response is complex[2] (here comes the name complex filter). However, the complex filter frequency response is symmetrical around the $\omega_{\rm IF}$. Since the blocking specifications of a receiver are symmetrical around the desired signal frequency, this is considered an advantage of complex filter over real bandpass filter (BPF) that has unsymmetrical frequency response around its center frequency.

These complex operations are practically performed as follows. Multiplication of the real RF signal by $e^{j\omega_{\rm LO}}$ is practically performed using quadrature mixer, which basically consists of two mixers whose LO inputs are in quadrature phase, as shown in Fig. 4. In the complex signal representation in Fig. 2, the desired signal at the mixer output is located at the positive IF frequency while the image signal is located at the negative IF frequency. In the real implementation in Fig. 4, the desired (image) signal in the *I* branch leads (lags) the *Q* branch by 90°. Phase and gain imbalances at the mixer output, due to LO and mixer mismatches, will cause the image signal at $-\omega_{\rm IF}$ to spill over the image band at $\omega_{\rm IF}$. As a result the image rejection ratio (IRR) will be limited by these mismatches. It can be shown that rejection limit (in decibles) is given by

$$\begin{aligned}&{\rm IRR}_{\max}\ ({\rm in\ dB})\\&\quad=10\log\left(\sin^2\left(\frac{\theta}{2}\right)+\left(\frac{\Delta}{2}\right)^2\cos^2\left(\frac{\theta}{2}\right)\right)\\&\quad\approx 10\log\left(\sin^2\left(\frac{\theta}{2}\right)+\left(\frac{\Delta}{2}\right)^2\right)\end{aligned}\tag{3}$$

where Δ and θ are the gain and phase imbalances, respectively. For example, for ${\rm IRR}>30$ dB, the maximum tolerable phase and gain mismatches (assuming equal contribution to ${\rm IRR}_{\max}$) are 2.5° and 4.2%, respectively. See also [12] about mismatch effects on complex filters.

The complex filter, in turn, is able to make the distinction between the signal and the image based on the phase difference between the *I* and *Q* branches. In the complex domain, the complex BPF is a frequency-shifted version of a low-pass filter (LPF). To convert an arbitrary LPF to a complex BPF centered at $\omega_{\rm IF}$, every frequency dependent element in the LPF [11] should be altered to be a function of s- $j\omega_{\rm IF}$ instead of s. The basic frequency-dependent element in a filter is the integrator. Consider the simple case of converting a first-order LPF with cutoff frequency $\omega_{\rm LP}$, to a complex filter BPF centered at $\omega_{\rm IF}$. The LPF response is shifted in frequency by placing it in a complex feedback loop as shown in Fig. 5(a). The complex input-output relation is given by

$$x_o=\frac{\omega_o}{s+\omega_{\rm LP}-j\omega_{\rm IF}}x_i\tag{4}$$

where $x_i=x_{iI}+jx_{iQ}$ and $x_o=x_{oI}+jx_{oQ}$, then from (4)

$$x_{oI}=\frac{\omega_o}{s+\omega_{\rm LP}}\left(x_{iI}-\frac{\omega_{\rm IF}}{\omega_o}x_{oQ}\right)\tag{5a}$$

$$x_{oQ}=\frac{\omega_o}{s+\omega_{\rm LP}}\left(x_{iQ}+\frac{\omega_{\rm IF}}{\omega_o}x_{oI}\right).\tag{5b}$$

Equations (5a) and (5b) are implemented as shown in Fig. 5(b). For illustration purposes, an active *RC* implementation of this first order complex filter is shown in Fig. 5(c). Note that an inverting amplifier is needed in the cross feedback from *Q* branch to *I* branch. If a differential implementation is used, this extra inverting amplifier can be avoided by exchanging the differential signals. The corresponding pole locus of the prototype and the complex BPF are shown in Fig. 6. For the special case of an integrator prototype, when $\omega_{\rm LP}=0$, the above transformation still holds and the integrator response will be shifted to $\omega_{\rm IF}$. If the above transformation is applied to every frequency dependent element in the LPF prototype, the entire LPF frequency response will be shifted to $\omega_{\rm IF}$.

III. Complex Filter Implementation

A. Filter Approximation

In OTA-C filters, the lowpass to complex filter transformation is done by replacing each pair of integrators, in *I* and *Q* branches, by the circuit shown in Fig. 7 for an OTA-C filter. System level simulations show that a complex filter based on a fourth-order Chebychev LPF or sixth-order Butterworth LPF may be sufficient to achieve the required selectivity. The Butterworth approximation is preferred for two reasons. First, it has small group delay variation (0.6 μs) within the passband. Second, since all the poles have the same angular frequency in a Butterworth filter, the cross-coupled OTAs will have the same transconductance value in the entire filter resulting in better matching between filter stages and between the filter and the frequency tuning circuit. The highest quality factor (Q_p) in the LPF prototype is 2. This small Q_p can tolerate process mismatches without affecting the filter performance significantly, thus it can be realized easily without using Q_p tuning. However, a frequency tuning circuit is required to compensate for the expected $\omega_{\rm o}$ variations due to the process technology variations.

[2]In real filters, complex poles are always conjugate, but in complex filters one single complex pole is possible.

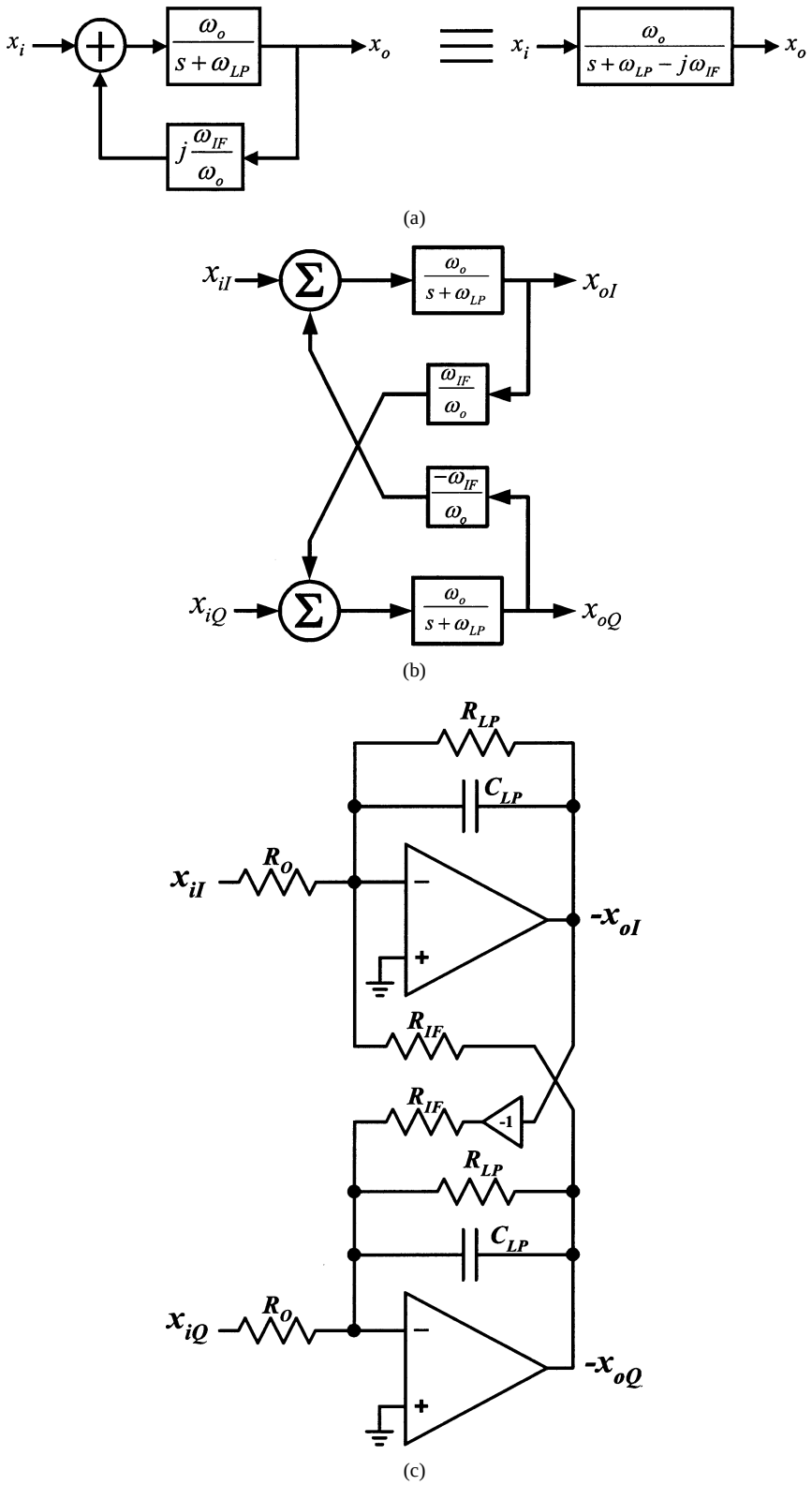


Fig. 5. LPF shifted to ω_{IF}. (a) Conceptual complex representation. (b) Actual building block implementation. (c) Active-*RC* implementation.

To simplify the LPF to BPF transformation, the LPF prototype should have only grounded capacitors. If the LPF prototype was to include floating capacitors, two pairs of cross-coupled OTAs would be used for each floating capacitor (one cross-coupled pair for each capacitor terminal) for frequency shifting. Therefore, floating capacitors in the LPF prototype means increased area and power of the complex filter. The LPF prototype is implemented using three biquads.

B. OTA Topology and CMFB

In order to reduce the input referred noise, the least number of transistors is used in the OTA, as shown in Fig. 8. This OTA

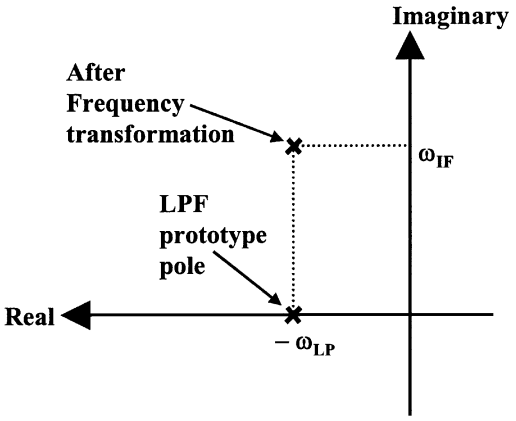


Fig. 6. Pole locus of the LPF prototype and the complex BPF.

was preferred over Nauta's transconductor [13] for two reasons. First, Nauta's transconductor has some circuitry to ensure common-mode (CM) stability which may not be needed in some cases and, therefore, may consume more power. Second, Nauta's transconductor is tuned through its supply voltage, and therefore, a buffer with high-current driving capability and low-output resistance is needed to drive the OTA supply node. The fact that both nMOS and pMOS transistors contribute to the transconductance in Nauta's transconductor is not really relevant in this case since a low-transconductance value is used.

Long-channel transistors (6 μm) are used in the OTA in Fig. 8 to enhance the output resistance, improve matching, and reduce flicker noise. A pseudo differential architecture is used to reduce the required supply voltage. The signal swing is determined by the overdrive voltage $(V_{\rm dsatn})$ of the input transistors $\rm M_1$ and $\rm M_2$. The minimum and maximum acceptable single-ended input levels to the OTA are $V_{\rm Tn}$ and $V_{\rm Tn}+2V_{\rm dsatn}$, respectively. Therefore, the minimum power supply voltage is $V_{\rm Tn} + 2V_{\rm dsatn} + V_{\rm dsatp}$. The transconductance of the OTA is linearly proportional to the input CM voltage $V_{\rm CM}$

$$g_m = K_n' \frac{W}{L}(V_{\rm CM} - V_{\rm Tn}). \tag{6}$$

If $V_{\rm b}$ is a fixed bias voltage (i.e., no CM control), the CM rejection ratio (CMRR) of the OTA equals unity. Therefore, $V_{\rm b}$ must be controlled using the CM input or output signal of the OTA to improve its CMRR.

C. CMFF and CMFB Interconnection Strategy

Here we discuss an alternative approach to avoid the use of conventional common-mode feedback (CMFB) circuits which often can be area and power hungry. Fig. 9(a) shows the CM equivalent of an OTA with no CM control. Note that input CM signal is transferred to the output through the CM transconductance, which happens to be the same value as given in (6). Unless the CM impedance at the output node is low enough, this biasing approach provides high CM voltage gain and may cause CM instability. The biasing circuit of the OTA in Fig. 9(a) is shown in Fig. 10(a). $V_{\rm CM}$ in the biasing circuit is a fixed bias voltage and is not dependent on CM input or output signals of the OTA. To enhance the CMRR of the OTAs, CMFB or common-mode feed forward (CMFF) is used. If the output CM impedance is high, then CMFB is needed to lower this impedance and to fix the dc operating point. This is illustrated in Fig. 9(b) where the output CM impedance becomes $1/{\rm g_{mfb}}$, where $\rm g_{mfb}$ is the transconductance of the CMFB loop. In Fig. 9(b), the common mode detector (CMD) senses the CM signal at the output node and feeds the correction signal to the bias voltage $V_{\rm b}$ of the OTA. To ensure CM stability, the magnitude of the closed loop CM gain ($\rm G_{CM}$) should be less than one. For a load resistance of R_L, the CM gain of the circuit if Fig. 9(b), when the OTA of Fig. 8 is used, can be expressed as

$$G_{\rm CM} = \frac{-g_{mn}R_L}{1 + \alpha g_{mp}R_L}. \tag{7}$$

Where g_{mn} and g_{mp} are the transconductances M_1 and M_3 in Fig. 8, respectively, and α is the voltage gain of the CMD which is close to unity. Since the CMFB is used in cases when the load resistance is high, we can assume that $\alpha g_{mp}R_L \gg 1$. In this case, the CM stability condition reduces to the following condition:

$$\alpha g_{mp} > g_{mn}. \tag{8}$$

On the other hand, if the output CM impedance is sufficiently small, CMFB is not needed and CMFF is used to isolate the input and output CM signal of the OTA by canceling the CM signal. This is illustrated in Fig. 9(c). The polarity of the OTA indicated in Fig. 8 is only valid in the differential mode (DM) sense. DM transconductance polarity can be changed by just exchanging the output terminals or input terminals without adding any extra components. However, the CM transconductance does not change by exchanging the output or input terminals. In fact, the CM transconductance of the OTA in Fig. 8 is always negative. Thus, a loop can be stable in DM but unstable in CM. Note also that CMD circuit has to be inverting type when used in CMFF to cancel the CM signal at the OTA output and noninverting when used in CMFB to have negative CMFB loop. The CMD circuit is illustrated in Fig. 10(b). All nMOS (and pMOS) transistors are matched. The inverting output of the CMD is inverted using the auxiliary circuit to generate the noninverting output. If the CMD is used only for CMFF, the auxiliary circuit is eliminated. Fig. 11(a) shows the I branch of one of the filter biquads. $\rm OTA_4$ provides the LP output current for the next current-mode filter stage. $\rm OTA_5$ and $\rm OTA_6$ play the same role as $R_{\rm IF}$ in Fig. 5(c) or $\omega_{\rm c}\rm C$ in Fig. 7. $\rm OTA_1$ and $\rm OTA_2$ form a negative feedback DM loop, but a positive feedback CM loop. The output node of $\rm OTA_2$, node 1 is a low impedance $(1/Qg_m)$ node due to the resistive connected $\rm OTA_3$. Hence, no CMFB is needed at this node and only CMFF is used in all the OTAs that feed this node, excluding $\rm OTA_3$. If CMFF is used in $\rm OTA_3$, the CM impedance at node 1 will be very high. Instead, the bias voltage of $\rm OTA_3$ is connected to a fixed voltage, independent of input and output CM voltages. The use of CMFF in $\rm OTA_2$ breaks the CM loop formed by $\rm OTA_1$ and $\rm OTA_2$. Without CMFB, node 2 is a CM high impedance node, and hence, needs CMFB to stabilize it. CMFB loop is formed in $\rm OTA_1$ through $\rm CMD_2$. CMFF is also used in $\rm OTA_4, OTA_5$, and $\rm OTA_6$ to isolate the CM signals in this biquad stage from the next biquad and from the corresponding biquad in the Q

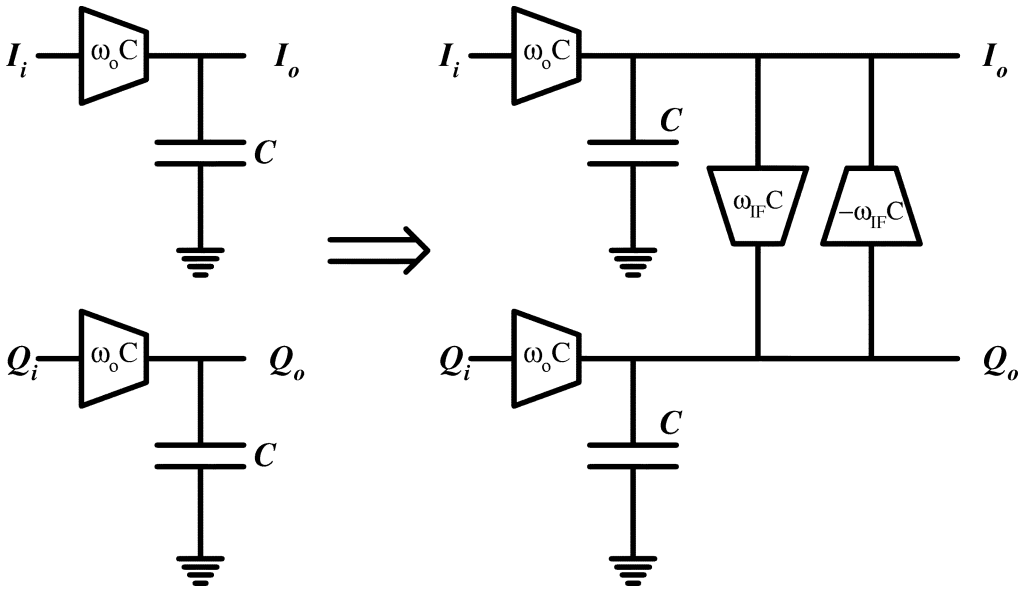


Fig. 7. Linear frequency translation to convert LPF to complex BPF.

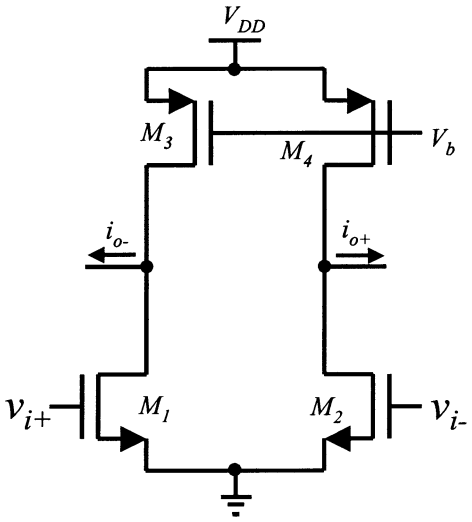


Fig. 8. Pseudo differential OTA.

branch. Only two common mode detectors are needed to form the CM control circuit in this biquad stage with six OTAs. By using the minimum number of CM control circuits, this efficient scheme saves considerable power and silicon area, and contributes less noise than using a conventional CM control circuit for each OTA, as in Nauta's transconductor [12]. The proposed CM control scheme roughly consumes only about $1/3$ of the area and power of CM control circuitry in conventional schemes. A CMRR in excess of 50 dB is obtained. Fig. 11(b) shows a block diagram for the complex biquad, which consists of two LP biquads, and two cross-coupled OTAs for each on the internal nodes 1 and 2.

D. Harmonic Distortion

Due to the long channel used in the OTA, square law characteristics can be assumed for the MOS transistors. Therefore, it can be shown that CMFF does not introduce third-order harmonics while the CMFB does. To show how CMFB introduces third-order harmonics, consider the simplified case shown in Fig. 12(a). OTA_1 is loaded with a linear resistor R_L to study the effect of CMFB nonlinearity by itself. The CMFB on OTA_1 generates a CM second-order harmonic at the output of OTA_1. This harmonic mixes with the DM fundamental output of OTA_1 due to the second-order nonlinearity of the input transistors in OTA_2. As a result, third-order harmonics appear at the output of OTA_2, and the harmonic distortion can be expressed as

$$\mathrm{HD3} = \frac{g_m R_L (g_m R_L - 1)}{32} \left(\frac{V_P}{V_C - V_\mathrm{Tn}} \right)^2 \tag{9}$$

where $\mathrm{V_P}$ is the peak voltage of the input signal. Two remarks are drawn in the above expression; 1) the HD3 is inversely proportional to the squared overdrive voltage and 2) the HD3 due to CMFB vanishes when $R_\mathrm{L} = 0$ or $R_\mathrm{L} = 1/g_m$. However, in these two cases, CMFB is actually not needed. For $g_m R_\mathrm{L} \gg 1$, the above expression reduces to

$$\mathrm{HD3} \approx \frac{1}{32} \left(\frac{g_m R_L V_P}{V_C - V_\mathrm{Tn}} \right)^2 = \frac{1}{32} \left(\frac{V_\mathrm{Pout1}}{V_C - V_\mathrm{Tn}} \right)^2 \tag{10}$$

where V_Pout1 is the signal peak at the output of OTA_1.

Another practical scenario that may generate HD3 is shown in Fig. 12(b). In this case, OTA_1 is loaded with the resistive connected OTA_2. CMFF is used for OTA_1, while OTA_2 has no CM control. The HD3 at the output is expressed as

$$\mathrm{HD3} = \frac{1}{8} \left(\frac{g_{m1}/g_{m2}}{V_C - V_\mathrm{Tn}} \right)^2 V_P = \frac{1}{8} \left(\frac{V_\mathrm{Pout1}}{V_C - V_\mathrm{Tn}} \right)^2 \tag{11}$$

where V_P and V_Pout1 are the peaks of the signals at the input and output of OTA_1, respectively. Note that in the later scenario, for the same biasing conditions, HD3 is 12 dB worse than the 1st scenario.

E. Filter Architecture

Fig. 13 shows the block diagram of the entire complex filter. Passive input high pass *RC* filters are used to isolate

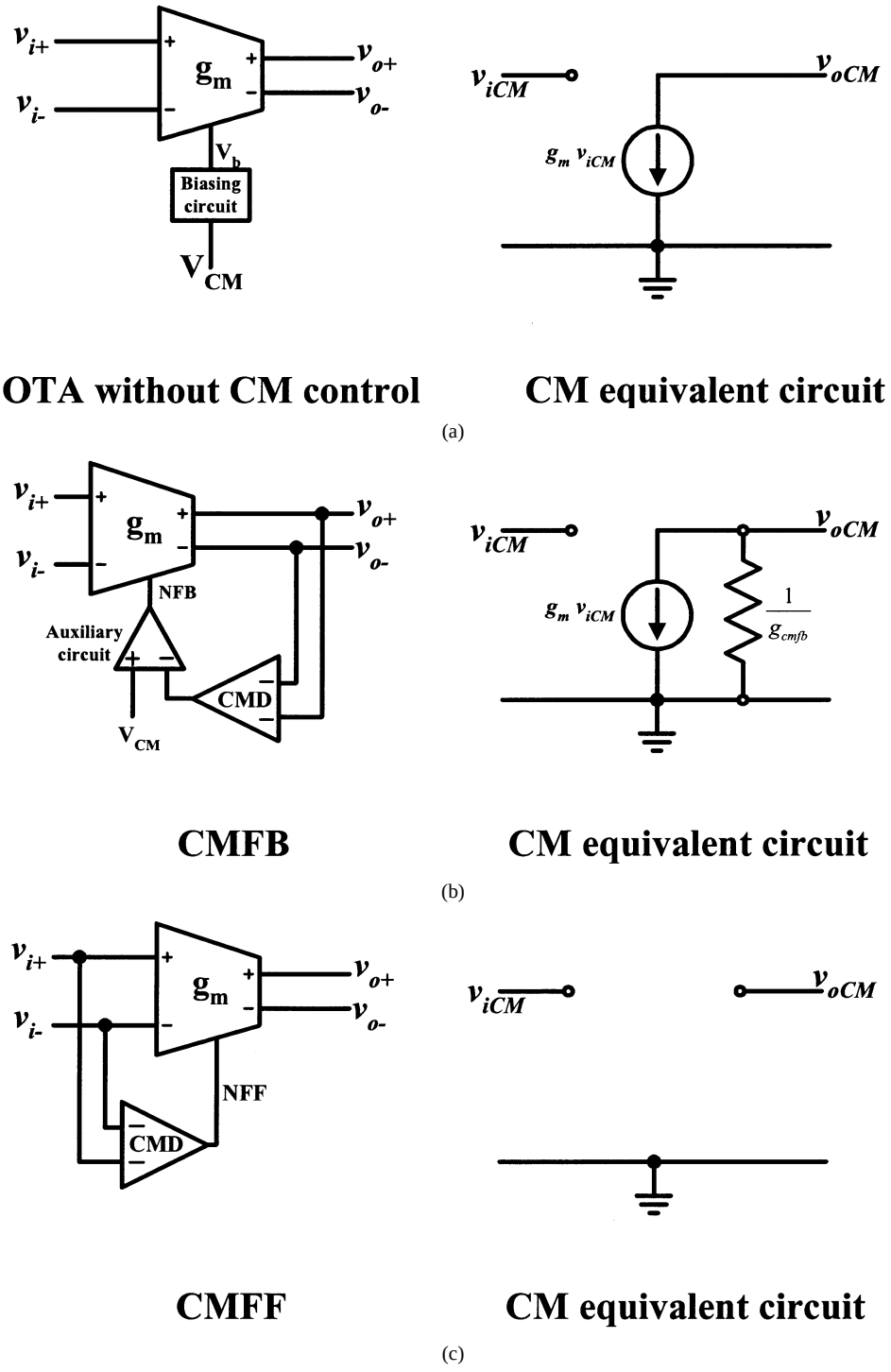


Fig. 9. (a) No CM control. (b) CMFB Circuit. (c) CMFF Circuit.

the CM mixer output from the filter CM input. The voltage V_{T1} applied through the R of the high-pass filter tunes the transconductance of the filter-input stage, which uses the same OTA architecture shown in Fig. 8. An important design issue is how to distribute the gain among the filter stages. If all the gain (15 dB) is used at the filter-input stage, the noise performance will be optimized but the linearity is degraded and *vice versa* if the gain stage is placed at the end of the filter stages. Due to the tough noise requirement on the filter, a 15-dB gain stage is placed at the filter input as shown in Fig. 13. Since Bluetooth uses a frequency modulation format (GFSK), inband linearity is not a major issue. In contrast, the filter design should be focused to improve the out-of-band linearity. Since the out-of-band blockers will be attenuated by the filter, harmonics generated by the out-of-band blockers are dominated by the filter's first gain stage. Hence, to improve the overall filter linearity, the gain stage is designed to have better linearity than the filter by using larger overdrive voltage $(V_{\mathrm{GS}} - V_{\mathrm{Tn}})$ of the input nMOS transistors M_1 and M_2 shown in Fig. 8.

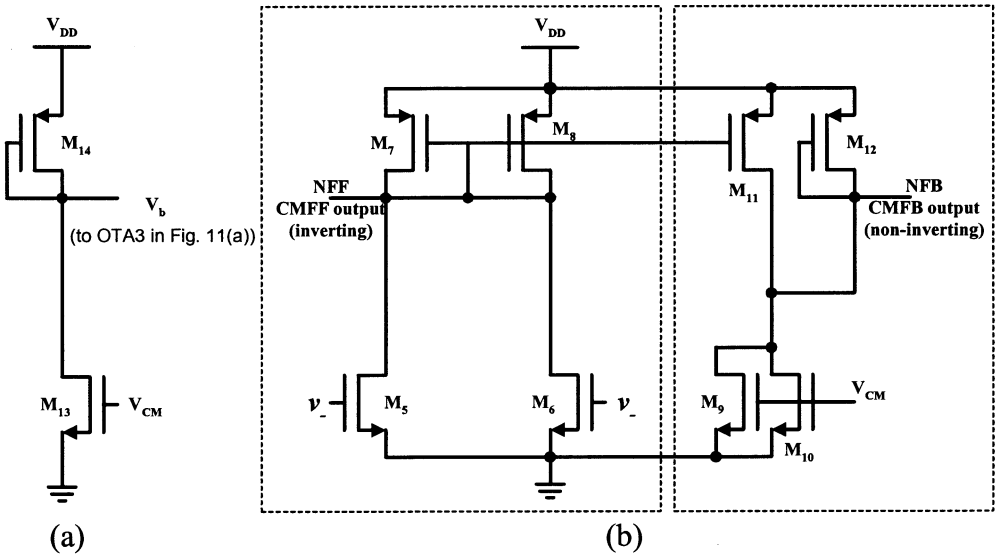


Fig. 10. (a) Biasing circuit if no CM control is used [Fig. 9(a)]. (b) The CMD and auxiliary circuit required for Figs. 9(b) and (c).

IV. Frequency Tuning Scheme

A. System Architecture

Fig. 14 shows the frequency tuning circuit of the complex filter, which is built to compensate for process variations. It consists of a relaxation oscillator, two counters to measure the oscillator and reference frequencies, a comparator, an up-down counter, and a simple D/A converter (DAC). The relaxation oscillator, discussed in the next subsection, is based on the same OTA architecture used in the filter. Under nominal conditions, the frequency of the relaxation oscillator is equal to the reference frequency (1 MHz). The operation of the tuning circuit is described as follows: after system reset, the 7-b reference and oscillator counters start counting until the reference counter reaches 64. At this time, the up/down counter is clocked to count up or down, or freezes according to the output of the digital comparator, which compares the content of the oscillator counter with $D_{\rm ref} = 64$. The content of the 7-b up/down counter is then converted to an analog voltage V_c (via a 7-bit DAC) to control the frequency of the oscillator (by controlling the value of g_m though V_b as shown in Fig. 8). When the reference counter overflows (reaches 128), it sends a reset signal to the oscillator counter to begin a new frequency comparison cycle based on the updated oscillator frequency. Eventually, the oscillator frequency will reach the reference frequency (the reference frequency is 1 MHz and is derived from the 16–MHz crystal oscillator used for the receiver chip) within an error depending on the DAC resolution. The same control voltage V_c is applied to $V_{\rm CM}$ in the filter biasing circuits and CM control circuits (Fig. 10) to tune the frequency to the correct value. A dead zone, depicted in Fig. 14, is added to the comparator transfer characteristic to avoid oscillation in the loop around the desired frequency. The width of the dead zone is three counter steps around the middle count. The maximum error in the frequency-tuning loop depends on DAC accuracy and the relaxation oscillator conversion gain. For $\pm 30\%$ process variations and a 7-bit DAC, the maximum frequency error is $\pm 0.23\%$. This error is mapped to only 4.6-kHz error in the filter center frequency, which is quite tolerable for Bluetooth application. The 7-bit DAC is implemented using resistive string to insure monotonicity and, hence, stability of the tuning loop. A nonsystematic error should also be considered due to the mismatches between the transconductance and capacitance in the passive *RC* LPF and the oscillator. These mismatches can add roughly 1% error to the frequency tuning. This is equivalent to another 20-kHz error in the center frequency of the filter, which is still within the range that a Bluetooth filter can tolerate. The advantage of such tuning circuit architecture over the conventional PLL-based frequency tuning is that it does not need a low-frequency LP-loop filter, which consumes considerable area the phased-locked loop (PLL). In addition, it uses a square wave relaxation oscillator, which is easier to build and guarantee oscillations than the sinusoidal oscillator needed in the conventional PLL.

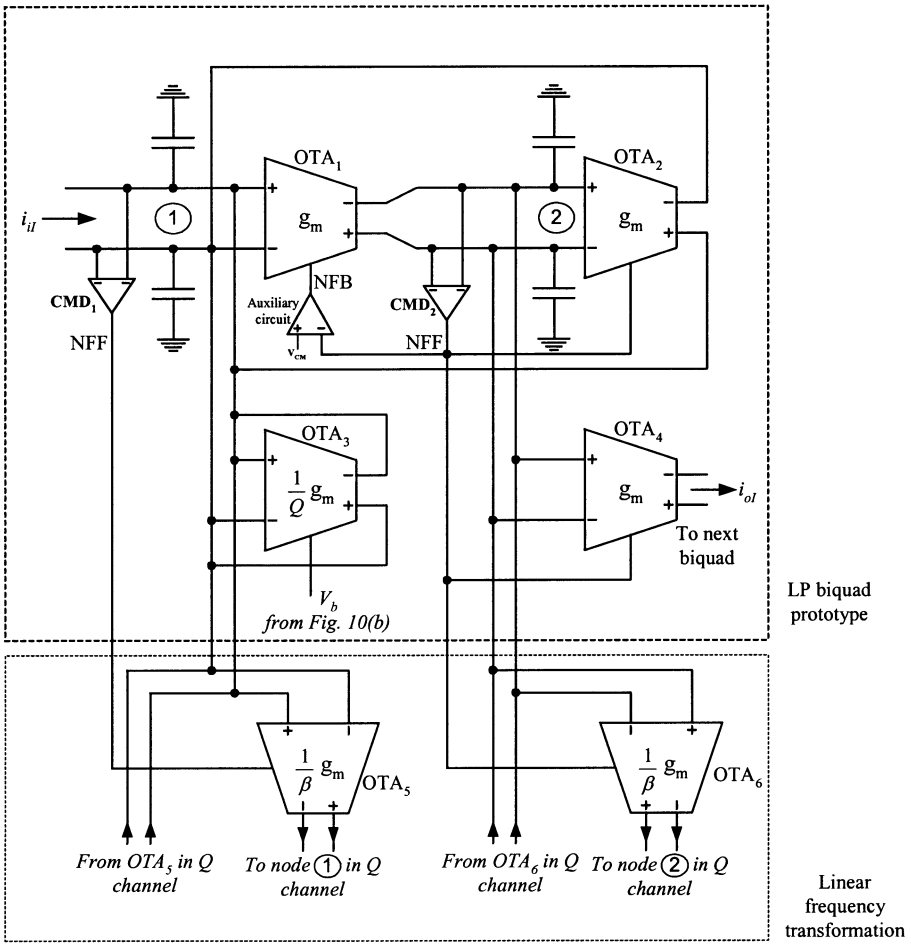
Guard rings are used to isolate the "noisy" tuning circuit from the filter. An *RC* LPF is used at the output of the tuning circuit to further attenuate the noise. A 1-MHz tone was observed at the output of the filter at 20 dB below the filter input-referred integrated noise.

B. Relaxation Oscillator

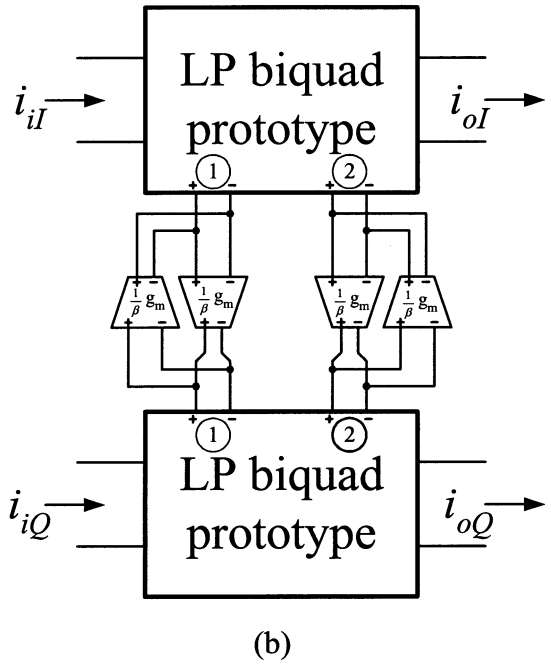
The relaxation oscillator, shown in Fig. 15, consists of an OTA, a current switch $(M_1$–$M_6)$, an integrating capacitor, and a fully differential comparator with hysteresis. The transconductance of the OTA is controlled by changing its CM input level (V_C). By applying a constant differential voltage ΔV to the OTA, the output single-ended current will be given by

$$i_o = g_m \Delta V = K'_n \frac{W}{L}(V_C - V_{\rm Tn})\Delta V. \qquad (12)$$

This output current is mirrored to the tail current source of a differential pair. The output current of the differential pair is integrated on the capacitor $\rm C_T$. The polarity of that current is controlled by the differential pair transistors. The corresponding slope of the triangular signal is $(g_m \Delta V)/(4C_T)$. The capacitor voltage is then compared with V_{B1} or V_{B2} depending on



(a)



(b)

Fig. 11. (a) I branch of the complex biquadratic section. (b) Conceptual complex biquad.

the comparator output. The voltages V_{B1}, V_{B2}, and ΔV are obtained from the same resistive string of the DAC used to convert the up/down counter content to analog voltage. The comparator output controls both the differential pair transistors and

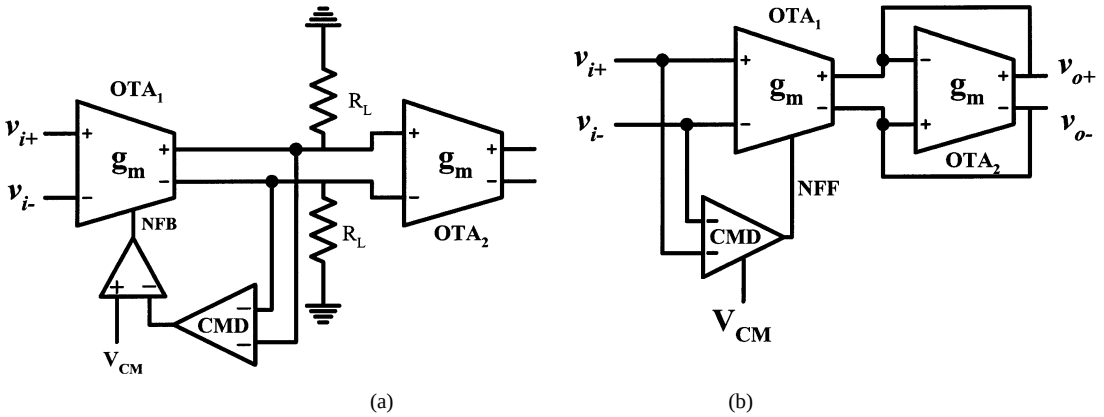


Fig. 12. (a) Circuit setup for HD3 analysis. (b) Another scenario for HD3 analysis.

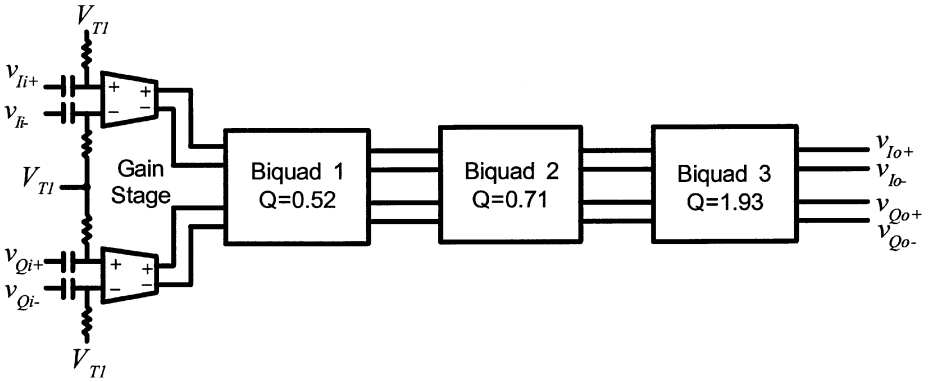


Fig. 13. Complete 12th-order complex filter.

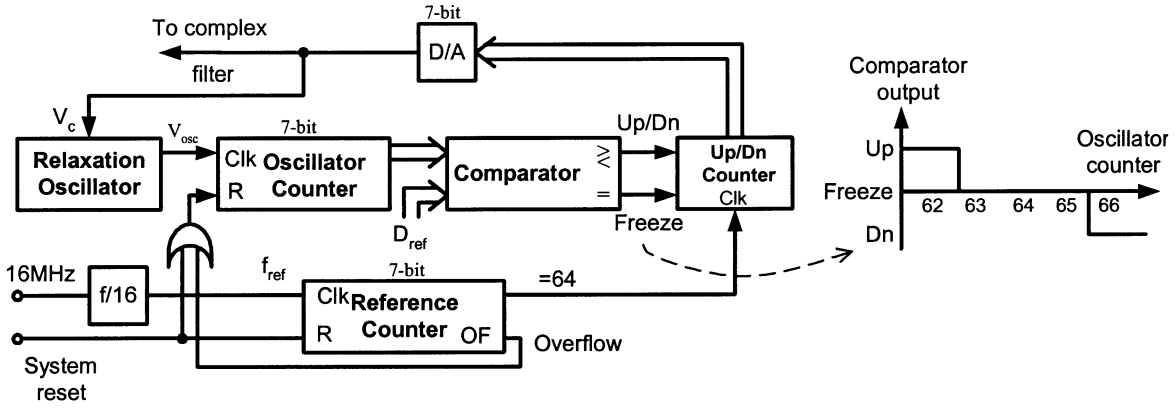


Fig. 14. Frequency tuning circuit for complex filter.

the threshold voltage of the comparator itself. The oscillation frequency can be expressed as

$$f_{\text{osc}} = \frac{1}{4}\frac{g_m}{C_T}\frac{\Delta V}{\Delta V_B} \tag{13}$$

where $\Delta V_B = V_{B1} - V_{B2}$. Since the ratio $\Delta V/\Delta V_B$ is determined by ratio of resistors in the resistive string DAC, it is independent of temperature and process variations and can be predetermined with good accuracy (depending on matching the DAC resistors). Hence, the oscillation frequency is proportional to g_m/C_T with a well-controlled constant of proportionality. The value of C_T is chosen such that, under nominal conditions, the oscillator runs at the reference frequency when the common mode voltage is at nominal (1.65 V). The feedback tuning loop ensures that the value of g_m/C remains constant in the presence of temperature and process variations.

V. Experimental Results

The filter and the frequency tuning circuit have been implemented in TSMC 0.35-μm CMOS process. The chip micrograph is shown in Fig. 16. The areas occupied by the filter and the tuning circuit are 1.6×0.8 mm^2 and 1×0.4 mm^2, respectively. The filter operates from 2.7-V power supply and draws 4.7 mA while the tuning circuit draws 0.8 mA. To test the filter frequency characteristics, quadrature sinusoidal signals are used. Polyphase *RC* network can be used to generate

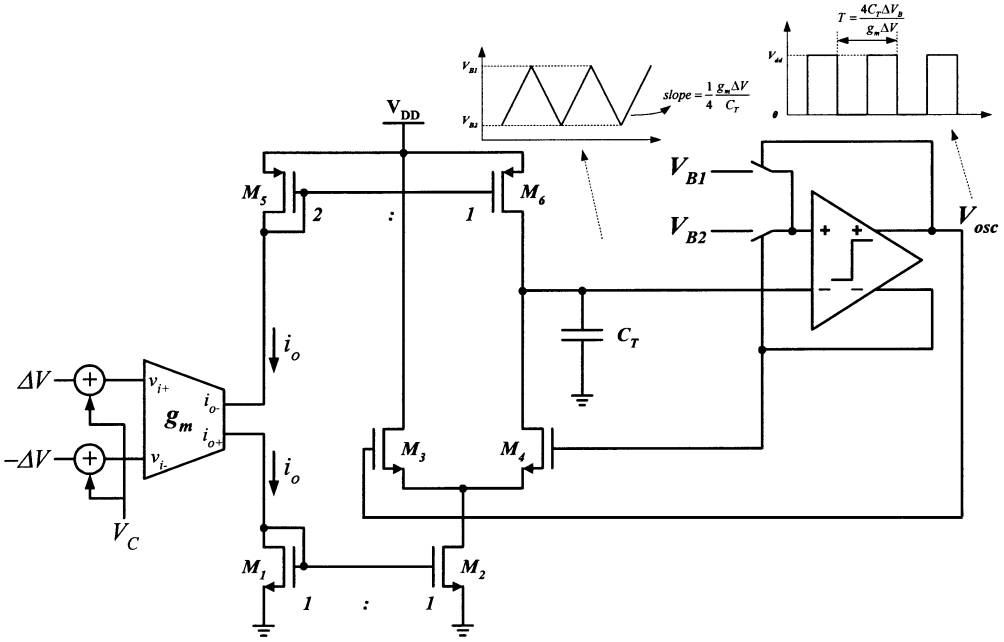


Fig. 15. The relaxation oscillator.

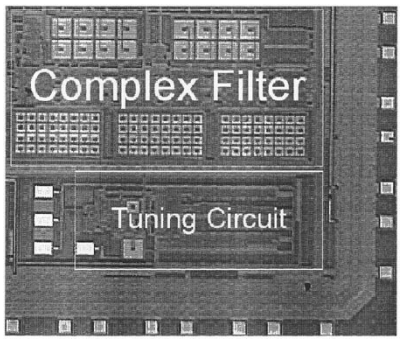


Fig. 16. The die photo (filter area $= 1.6 \times 0.8$ mm^2 and tuning circuit area $= 1 \times 0.4$ mm^2).

the quadrature signals [7]. However, polyphase *RC* filters can only generate balanced quadrature signals for a narrow frequency band and, hence, cannot be used to measure the attenuation of interference signals at positive and negative frequencies (relative to the LO frequency). Furthermore, process variations may alter the *RC* time constant, which will lead to unbalanced quadrature signals. In this case, Tektronix AFG320 signal generator is used to generate the required quadrature signals. Fig. 17 shows the filter frequency response for the signal and image sides. The figure shows that the image rejection ratio is more than 45 dB, which is enough for Bluetooth specifications . The filter attenuates the first- and second-adjacent channels by 27 and 58 dB, respectively. The filter linearity is quantified in terms of spurious-free dynamic range (SFDR). The SFDR is measured by applying two tones at the following frequencies:

$$f_1 = f_C + n \times 1\,\text{MHz} \quad \text{and} \quad f_2 = f_C + n \times 2\,\text{MHz}. \tag{14}$$

Where *n* is the two-tones separation in MHz, f_C is the filter center frequency, f_1 is the frequency of the first tone, and f_2 is the frequency of the second tone.

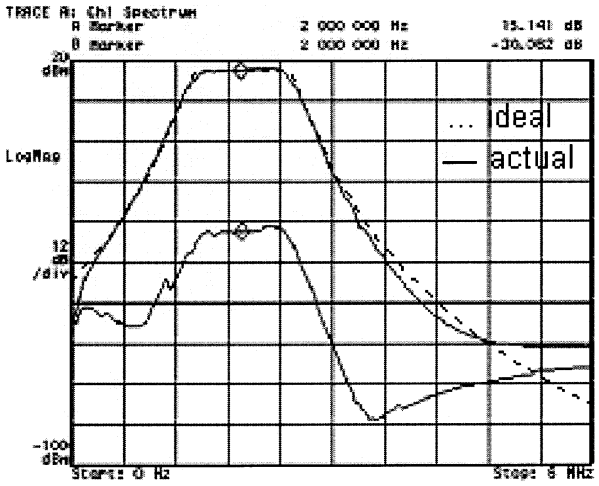


Fig. 17. Frequency response at signal and image sides (vertical axis 12 dB/div, . . . ideal, — actual).

Fig. 18 shows the measured SFDR versus *n*. The inband SFDR $(\text{n} = 0)$ is about 45.2 dB. Fig. 19 shows that the inband two-tone test from which the inband SFDR is measured. Since the filter is followed by a hard limiter (Fig. 1), the inband SFDR is not a critical parameter in this case. The out-of-band SFDR is a more important parameter to measure. In Bluetooth, the IP3 is calculated for two interferers at 3 and 6 MHz away from the desired signal on one side. The IP3 can be approximately calculated to be about $1.5 \times \text{SFDR} = 91.65$ dB above the noise floor. The total input referred noise is 29 μV_{rms} and the pass band gain is 15 dB. Fig. 20 shows the measured group delay of the filter, from which it is seen that the inband group delay variation is about 0.6 μs. Table I summarizes the experimental results of the filter. The asymmetry in the magnitude and group delay responses in Figs. 17 and 20 is a result of parasitic components and mismatches between filter components.

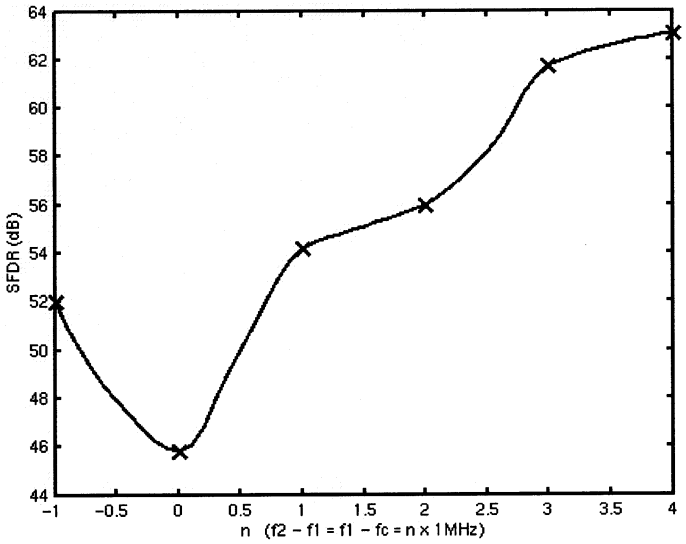


Fig. 18. The measured SFDR versus *n*.

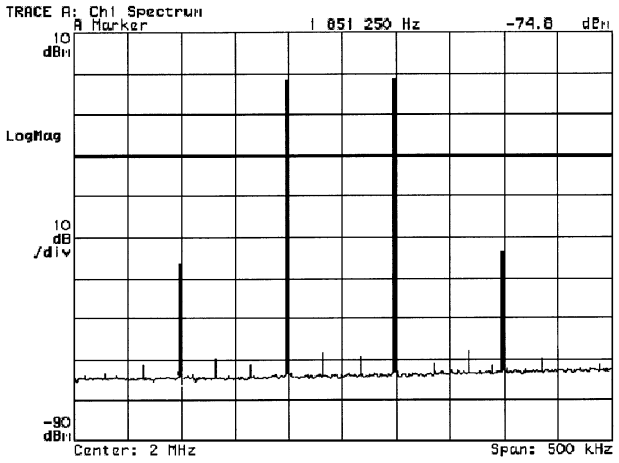


Fig. 19. IM3 test for $f_1 = 1.95$ MHz and $f_2 = 2.05$ MHz.

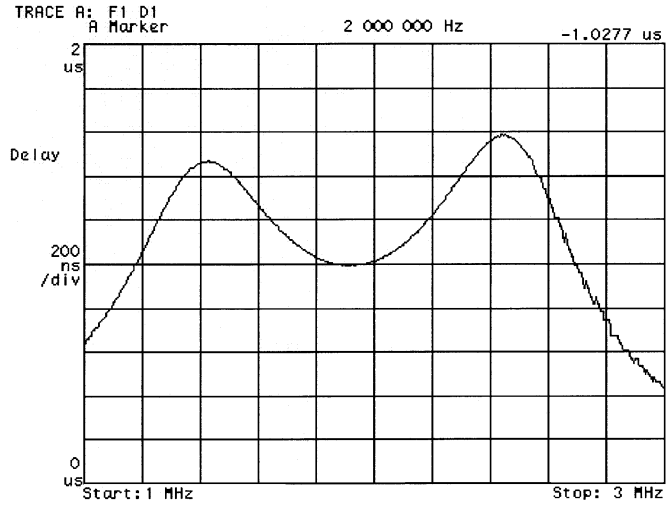


Fig. 20. Group delay response.

VI. Conclusion

A pseudo differential OTA-C complex filter design for low-IF Bluetooth receiver has been presented. The main highlights for the design are as follows: 1) A pseudo differential OTA is used to comply with low voltage operation. 2) A sound scheme for common-mode control is implemented using a minimum number of CMFF and CMFB circuits. Compared to using a separate CM control circuit for each OTA [7], the proposed CM control scheme roughly consumes only about $1/3$ of the area and power of CM control circuitry in conventional schemes. 3) Nonconventional frequency tuning circuit architecture is used that has advantages over the conventional PLL, in terms of silicon area and design complexity.

TABLE I
SUMMARIZED FILTER TESTING RESULTS

Parameter	Value
Center frequency	2MHz
-1dB bandwidth	1.47MHz – 2.53MHz
Pass-band gain	15dB
Input referred noise	$29\mu V_{rms}$
V_{dd}	2.7v
Filter current drain	4.7mA
Image rejection ratio	>45dB
Attenuation @ $f_c \pm 1MHz$	29dBc
Attenuation @ $f_c \pm 2MHz$	58dBc
CMRR	> 50dB
In-band SFDR	45.2dB
SFDR at 3 & 6MHz	61.1dB
In-band group delay variation	0.6μs
Area (filter + tuning circuit)	$(1.28 + 0.4)mm^2$

Acknowledgment

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