1.8-V 800-Mb/s/pin DDR2 and 2.5-V 400-Mb/s/pin DDR1 Compatibly Designed 1-Gb SDRAM With Dual-Clock Input-Latch Scheme and Hybrid Multi-Oxide Output Buffer

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***Abstract*—This paper describes three circuit techniques for a DDR1/DDR2–compatible chip architecture designed for both high-speed and high-density DRAMs: 1) a dual-clock input-latch scheme, which reduces the excessive timing margin for random input commands by using a pair of latch circuits controlled by dual-phase one-shot clock signals, achieves a 0.9-ns reduction in cycle time from 3.05 to 2.15 ns; 2) a hybrid multi-oxide output buffer reduces the area penalty of the output buffer caused by compatible chip design from 1.35% to 0.3%; and 3) a quasi-shielded distributed data transfer scheme enables a 2.6-ns reduction in access time to 10.25 ns in both 2-b and 4-b prefetch operations. By using these techniques, we developed a 175.3-mm^2 1-Gb SDRAM that operates as an 800-Mb/s/pin DDR2 or 400-Mb/s/pin DDR1.**

***Index Terms*—Clock, clock generation, CMOS, double data rate (DDR), DRAM, input latch, output buffer, SDRAM.**

I. Introduction

THE performance of computer systems has steadily improved, and, in conjunction with this trend, the demand for memory systems having data rates of over 800 Mb/s/pin has been increasing as well. Among the various proposed architectures, the double-data-rate-2 (DDR2) SDRAM [1]–[5] is a promising successor to the widely used DDR1 SDRAM [6]–[9] in the high-end PC and server market. Fig. 1 shows the data transfer rate and DRAM architecture trends of main memory for servers and high-end PC. The DDR1 and DDR2 are currently in a transitional stage; hence, there is a demand for various types of DRAMs to support evolving needs. To respond to this market as flexibly as possible, our approach is common-die manufacturing with compatible chip design [10], [11]. This compatible chip design has no area or access penalty, and it integrates two architectures into the same silicon die via a metal option and enables a short manufacturing turn-around time.

Table I shows the target of our work. The DDR2 architecture is suitable for compatible design with the DDR1 architecture. This is because the minimum read/write cycle time and access time (t_{AA}) can be respectively kept to 5 and 11.5 ns for data transfer rates from 200 to 800 Mb/s/pin by increasing the prefetch size and column latency (CL). However, to cover all data transfer rates and CLs by using a common die, the operating frequency and supply voltage must be from 400 to 800 MHz and from 2.5 to 1.8 V. Thus, two different types of input/output circuit are needed. To make this approach cost-effective, we employed three circuit technologies that enable high-speed operation with a smaller chip-size overhead compared with using incompatible SDRAM technologies.

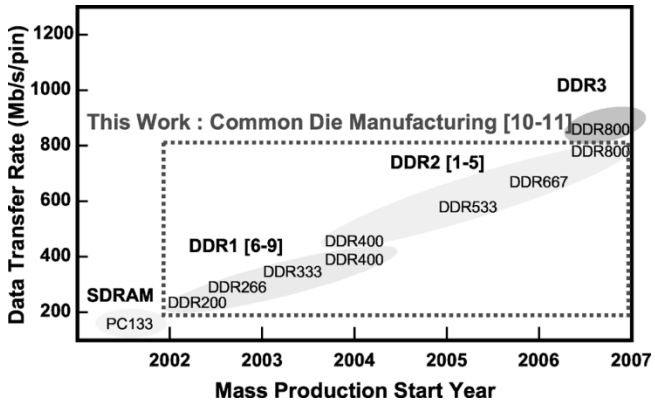

Fig. 1. Data transfer rate and DRAM architecture trends of high-end PC and servers.

TABLE I
TARGET OF THIS WORK

Speed [Mb/s/pin]	VDD [V]	Read/write cycle [ns]	Access time [ns] CL=2	2.5	3	4	5
DDR1-200	2.5	10	20	25			
DDR1-266	2.5	7.5	15	22.5			
DDR1-333	2.5	6	12	15			
DDR1-400	2.5	5		12.5	15		
DDR2-400	1.8	10			15	20	
DDR2-533	1.8	7.5			11.25	15	
DDR2-667	1.8	6				12	15
DDR2-800	1.8	5					12.5

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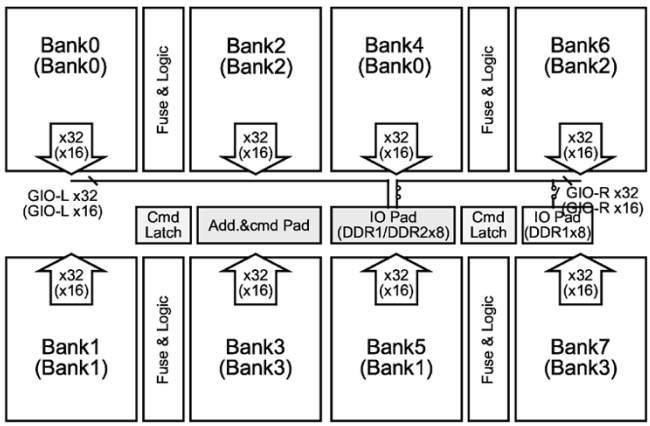

Fig. 2. DDR1/2-compatible chip architecture.

This paper presents circuit techniques that can be used to design a DDR1/DDR2-compatible SDRAM with low-cost and high-performance characteristics [11]. Section II describes the chip architecture of DDR1/DDR2 compatibly designed 1-Gb SDRAM. Sections III and IV describe the characteristics of the dual-clock input-latch scheme and the hybrid multi-oxide output buffer used to achieve both 1.8-V 800-Mb/s/pin and 2.5-V 400-Mb/s/pin operations. Section V shows fabrication results for our 1-Gb DDR1/DDR2 SDRAM using 0.1-μm technology. The paper's conclusions are stated in Section VI.

II. DDR1/2-Compatible Chip Architecture

Fig. 2 shows the chip architecture of our 1-Gb DDR1/DDR2 SDRAM. It is organized into an eight-bank 128-Mb array with eight DQs in DDR2 operation and into a four-bank 256-Mb array with 16 DQs in DDR1 operation. The operating conditions inside the parenthesis of Fig. 2 are used in DDR1 operations. This architecture has two features to reduce the access time of read/write operations.

1) The address, command, and DQ pads for the DDR2-$\times$ 8 operation are located in the center of the chip. This location shortens the length of the column access path by almost 14% in DDR2 operation.
2) The 64 global I/O (GIO) lines in the center are divided into GIO-R or GIO-L, and, in DDR2 operation, either GIO-R or GIO-L are used for the 4-b prefetch. In DDR1-$\times$ 16 operation, the right or left side of the chip is assigned to the same bank and different 8-DQs, and GIO-R and GIOL are simultaneously used for the 2-b prefetch operation. Therefore, the total length of the DDR1 access path is almost the same as that for DDR2 operation.

The quasi-shielded data transfer scheme that is used to achieve high-speed data transfer on GIO lines in both 4-b and 2-b prefetch operation is shown in Figs. 3 and 4. The main amplifier circuits [9] that reduce the excessive operating margin caused by PVT fluctuations simultaneously detect the prefetch data of the main I/O (MIO) lines, and their outputs are transferred to the GIO lines. The GIO lines are quite long, up to 12 000 μm, and the amount of simultaneous data transfer in a 4-b prefetch operation is four times that of conventional SDRAMs; therefore, wide-pitch and fully shielded GIO lines

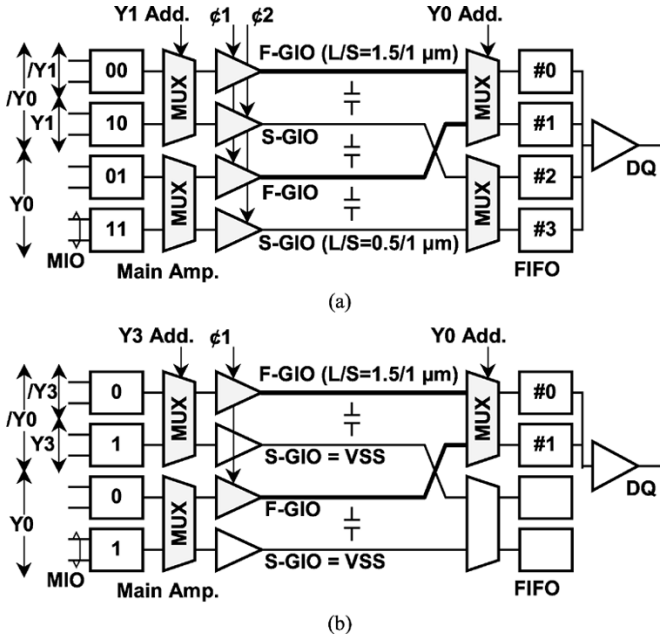

Fig. 3. Block diagram of quasi-shielded GIO data-transfer scheme. (a) DDR2 4-b prefetch operation. (b) DDR1 2-b prefetch operation.

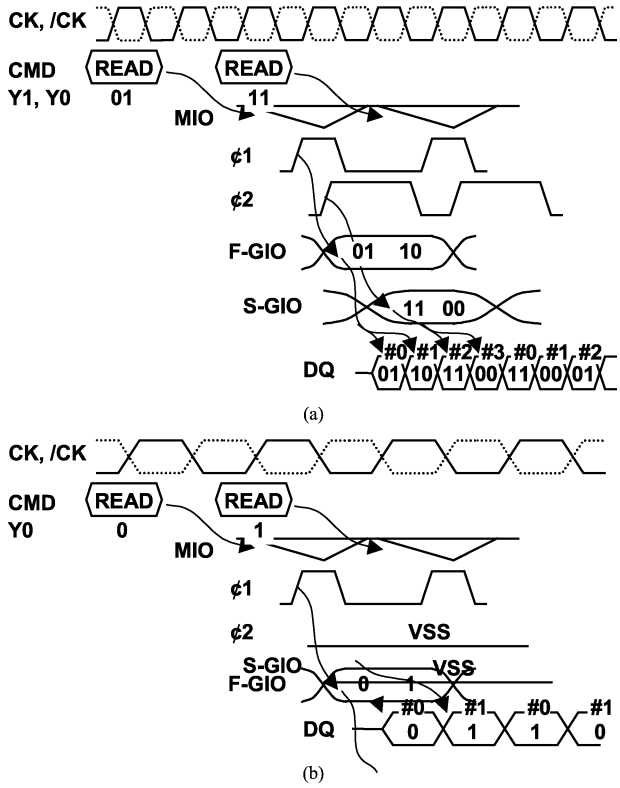

Fig. 4. Timing diagram of quasi-shielded GIO data-transfer scheme. (a) DDR2 4-b prefetch operation. (b) DDR1 2-b prefetch operation.

are needed. In this scheme, half of the GIO lines (fast-GIO) are designed with wide pitches, and the others (slow-GIO) are designed with narrow pitches. They are routed alternately. In DDR2-$\times$ 8 4-b prefetch operations, by using distributed F-GIO and S-GIO data transfer, we achieved quasi-shielded data transfer with wide-pitch GIO lines. First, the first and second sets of data of a 4-b prefetch are transferred immediately to

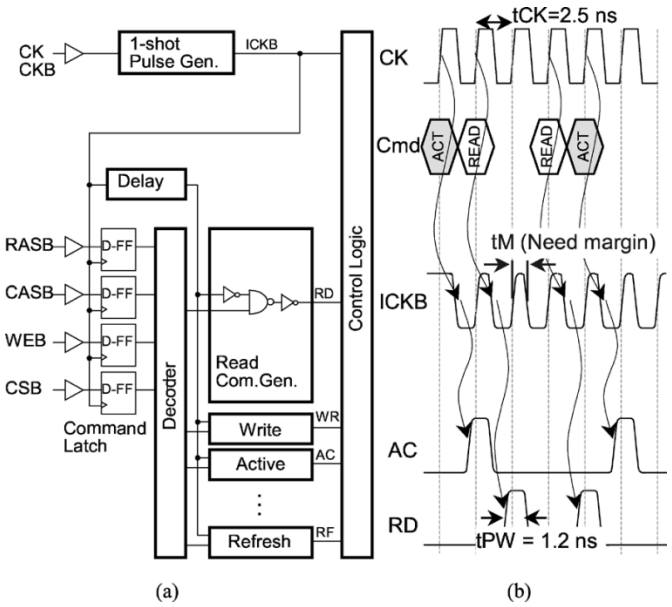

Fig. 5. (a) Block diagram of conventional input latch scheme. (b) Timing diagram of DDR2 operation.

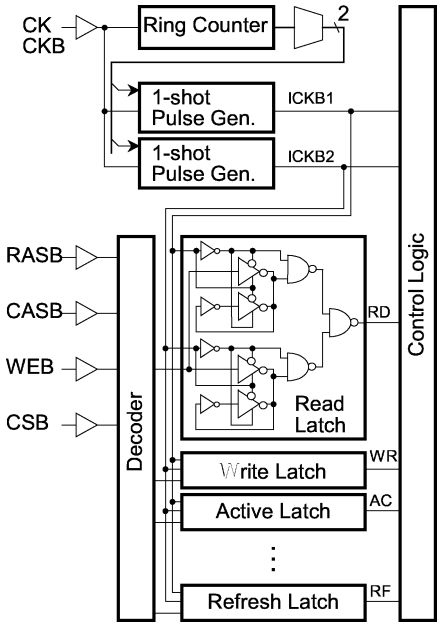

Fig. 6. Block diagram of dual-clock input-latch scheme.

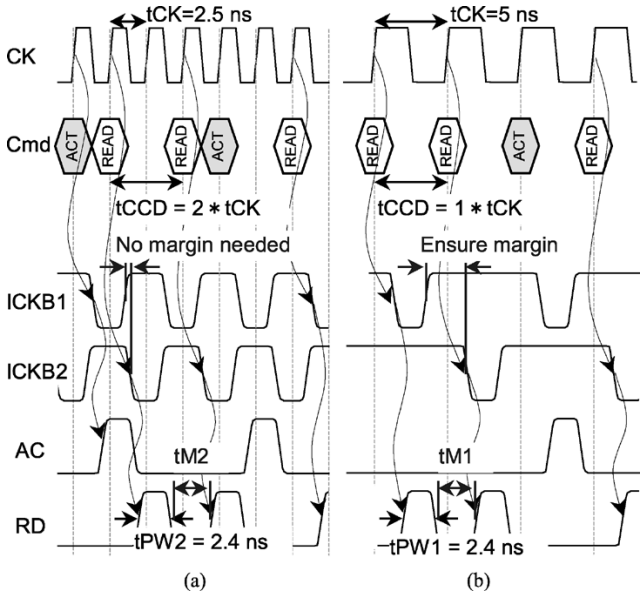

Fig. 7. Timing diagram of dual-clock input-latch scheme. (a) DDR2-800 operation. (b) DDR1-400 operation.

the F-GIO lines by the $\phi 1$ signal and prefetch address. Next, the third and fourth sets of data are transferred to the S-GIO lines by the $\phi 2$ signal with a suitable delay. Hence, the S-GIO lines can be used as shield lines during the data transfer of the F-GIO lines and the peak current of GIO output buffer can be reduced to half. The access time of the third and fourth sets of data has a 2.5-ns extra margin in 800-Mb/s/pin operation. Thus, there is no access penalty for the third and fourth sets of data in a distributed data-transfer operation. On the other hand, in the DDR1-$\times$ 16 2-b prefetch operations, the number of read/write bits from the 128-Mb array is 16, which is half that of the DDR2 operations. Therefore, by changing the connection between slow-GIO and VSS, we achieved fully shielded data transfer in DDR1 operations. Using this architecture, the DDR1 and DDR2 operations achieved a 1.2-ns reduction in access time.

III. Dual-Clock Input-Latch Scheme

Fig. 5 shows the block diagram of the conventional command latch scheme [2] and the timing diagram of DDR2 operation. This scheme is widely used because of its simple structure, but there are two problems in applying it for DDR1/DDR2-compatible design. The first problem is the small pulse width of the internal clock signal. This is because the frequencies of the external clock (CK/CKB) and internal one-shot clock (ICKB) for the command latch and generate circuits are the same. The minimum cycle time ($t_{\rm CK}$) is thus limited by the pulse width of ICKB ($t_{\rm PW}$) and timing margin of ICKB (t_M) as

$$t_{\rm CK} = t_{\rm PW} + t_M. \tag{1}$$

In DDR2-800 operation, $t_{\rm PW}$ of ICKB and the read command output signal (RD) are each no more than 1.2 ns and t_M is no more than 1.3 ns. The distribution length of ICKB is quite long, up to 14 000 μm, in 1-G b SDRAM, so the pulse width of ICKB limits the operating frequency of the conventional scheme. The second problem is the access penalty of command decoding. In the conventional scheme, the command latch circuits operate at 400 MHz and the cycle time of D flip-flop circuits is no more than 2.5 ns; thus, to ensure the setup and hold time, the input command latch must be operated before command decoding. Therefore, the internal clock for the command generation circuits must be delayed by 0.9 ns.

Fig. 6 shows the block diagram of the dual-clock input-latch scheme for high-speed and high-frequency input command latch operations. In this scheme, the two latch circuits controlled by dual-phase one-shot clock signals (ICKB1, ICKB2) are connected in parallel, and either of their command signals is outputted to control logic. A pair of one-shot pulse generator circuits and 2-b ring counter circuits are used for generating the dual-phase clock signals. In DDR2 operation, the interval of the

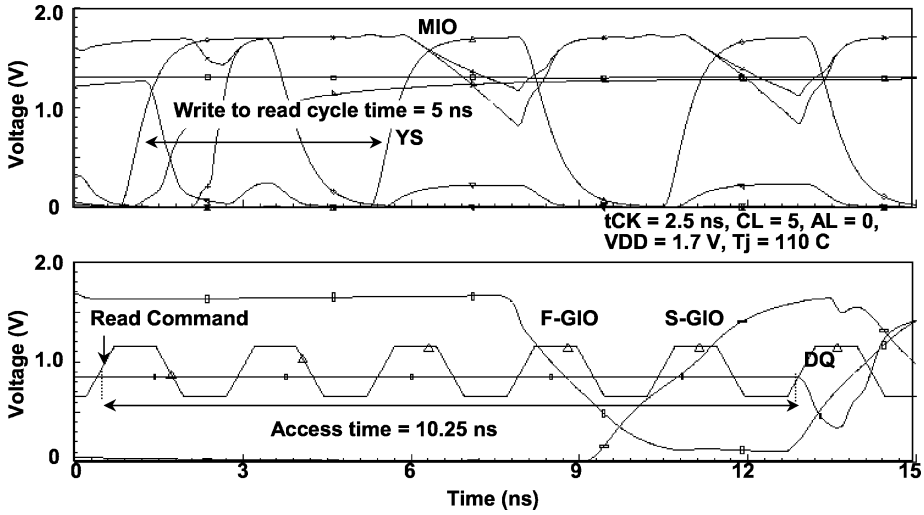

Fig. 8. Simulated waveforms in write-to-read cycles.

same command except for another bank precharge command is more than two clocks by the specification for 4-b prefetch operation, as shown in Fig. 7(a). The output signals of paired latch circuits never conflict, and there is no need for a timing margin between the rise edge of ICKB1 and fall edge of ICKB2. Thus, the minimum $t_{\rm CK}$ of DDR2 operation is given by

$$t_{\rm CK} = \frac{(t_{\rm PW}2 + t_{\rm M}2)}{2}. \tag{2}$$

Therefore, $t_{\rm PW}2$ of ICKB1 and ICKB2 are each 2.4 ns and $t_{\rm M}2$ is 2.6 ns in DDR2-800 operation, which is almost twice that of the conventional scheme. Furthermore, the command latch can be operated after command decoding in this scheme. The operating frequency of the two latch circuits is half of the external clock, so these circuits ensure the setup and hold time for 400-MHz operation and enable a 0.9-ns reduction in access time.

Fig. 7(b) shows the operating waveforms of DDR1-400 operation. The interval of the same command is only one clock. However, in the case of low-frequency operations, the timing margin between the rise edge of ICKB1 and fall edge of ICKB2 is ensured automatically, because the ICKB1 and ICKB2 are one-shot pulse signals. Thus, the minimum $t_{\rm CK}$ of DDR1 operation is given by

$$t_{\rm CK} = t_{\rm PW}1 + t_{\rm M}1. \tag{3}$$

The $t_{\rm PW}1$ and $t_{\rm M}1$ are 2.4 ns and 2.6 ns in DDR1–400 operation, which is almost the same as in DDR2-800 operation. There is no need to change command latch circuits between DDR2 and DDR1 operation, so the same design can be applied despite the different operating frequencies of the input latch circuits, which reduces the complexity of DDR1/DDR2-compatible chip design.

The simulated waveforms of the write-to-read operation are shown in Fig. 8. Fig. 9 shows the cycle time ($t_{\rm CK}$) and access time ($t_{\rm AA}$) improvement. In this architecture, the use of the dual-clock latch scheme enabled a 0.9-ns reduction in cycle time while increasing the internal clock margin. Furthermore, we

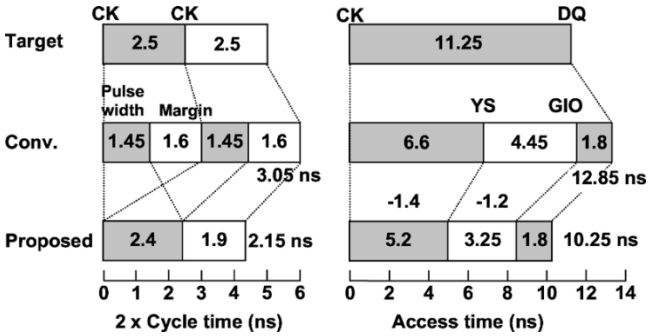

Fig. 9. Performance improvement of using the proposed scheme.

achieved a 2.6-ns reduction in access time to 10.25 ns. The contributions are 1.2-ns reduction by quasi-shielded data transfer scheme, 0.9-ns reduction by dual-clock latch scheme, and 0.5-ns reduction by concentrated center PAD location. This performance improvement is enough for stable 800-Mb/s/pin DDR2 operation.

IV. Hybrid Multi-Oxide Output Buffer

To achieve a cost-effective design in a DDR1/DDR2-compatible SDRAM, we must reduce not only the manufacturing turn-around time by using a one-metal mask option but also the chip-size overhead of a DDR1/DDR2-compatible SDRAM. In particular, the area size of output buffer circuits is quite large, which is up to 3.9% of a 1-Gb SDRAM. To achieve almost the same chip size as incompatible DDR2 SDRAM, we developed a hybrid multi-oxide output buffer.

Fig. 10 shows the problems that arise in the output buffer of DDR1/DDR2-compatible chips. The requirements for the DDR1 and DDR2 output-buffer transistor characteristics are different.

1) In DDR2 operation, the maximum capacitance specification of the DQ pad ($C_{\rm io}$) is 3.5 pF, which is 1.0 pF smaller than that of DDR1. Thus, high-performance transistors are needed for the output buffer.
2) In DDR1 operation, the supply voltage ($V_{\rm DD}$) is 2.5 V, which is 0.7 V higher than that of DDR2. Thus, transistors

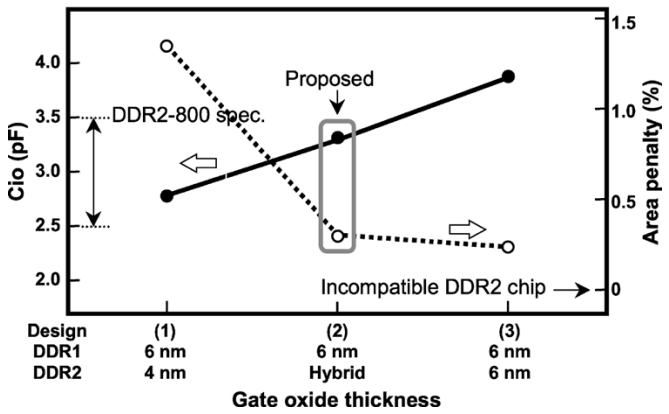

Fig. 10. Area penalty and $C_{\rm io}$ of hybrid multi-oxide output buffer.

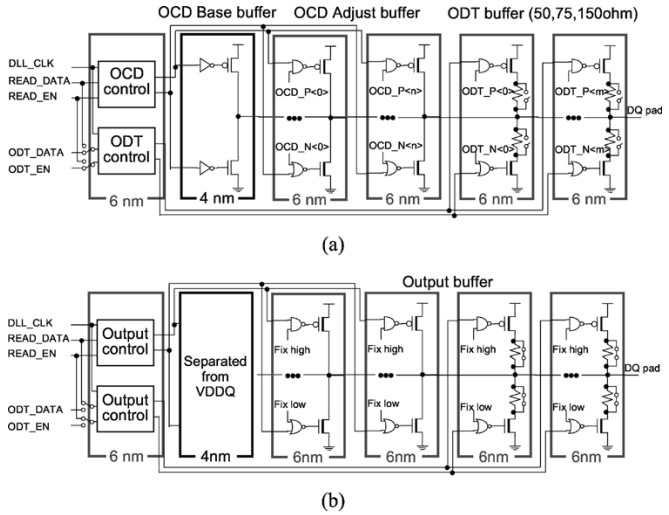

Fig. 11. Block diagram of hybrid multi-oxide DDR2 output buffer. (a) DDR2 operation. (b) DDR1 operation.

with high-voltage endurance gate oxide are needed for the output buffer.

We considered the area penalty of the output buffer and $C_{\rm io}$ of three combinations of gate oxide thickness. Design (1) used different thickness transistors for the DDR1 and DDR2 output buffers, and design (3) used same-thickness transistors. Design (1) can achieve a $C_{\rm io}$ of 2.7 pF, which is 1.2 pF smaller than that of design (3). However, the area penalty of design (1) is 1.35% more than that of an incompatible DDR2 chip, and this is because the IO pad-area size affected the increase of peripheral circuits width in this chip architecture. To solve the $C_{\rm io}$ and area penalty problems simultaneously, we developed a hybrid multi-oxide output buffer.

Fig. 11(a) shows the block diagram of the hybrid multi-oxide output buffer for DDR2 operation. The extra functions of the off-chip driver (OCD) adjustment from $+30$ to -40% and on-die-termination (ODT) of 50, 75, and 150 Ω in DDR2 operation are responsible for the increase in $C_{\rm io}$. We combined transistors with different oxide thicknesses for the output buffer. The 4-nm transistors are used for only the OCD bases buffer and 6-nm transistors are used for the OCD adjust buffer, prebuffer, and ODT buffer. By optimizing the use of 6-nm transistors, the $C_{\rm io}$ became 3.3 pF, which is 0.6 pF smaller than that of design (3), and satisfied the $C_{\rm io}$ specs of DDR2-800. Fig. 11(b) shows the block diagram of the hybrid multi-oxide output buffer for DDR1 operation. In DDR1 operation, only 6-nm transistors are used for the output buffer. This is because the gate oxide has to be able to endure a 2.5-V supply voltage. The OCD adjust buffer, prebuffer, and ODT buffer are composed of 6-nm transistors and are shared between the DDR1 and DDR2 operations. Therefore, by using the hybrid multi-oxide output buffer, the area penalty of the output buffer can be reduced from 1.35% to 0.3% compared with using incompatible DDR2 SDRAMs while satisfying the $C_{\rm io}$ specifications.

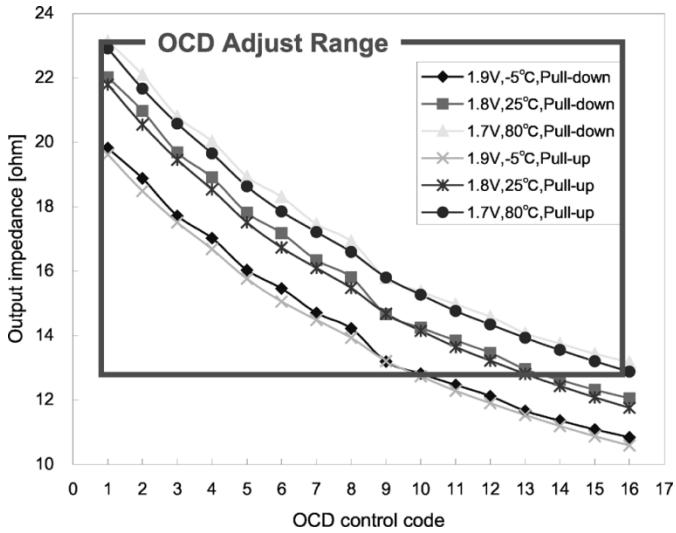

Fig. 12. Measured OCD strength as a function of the control code.

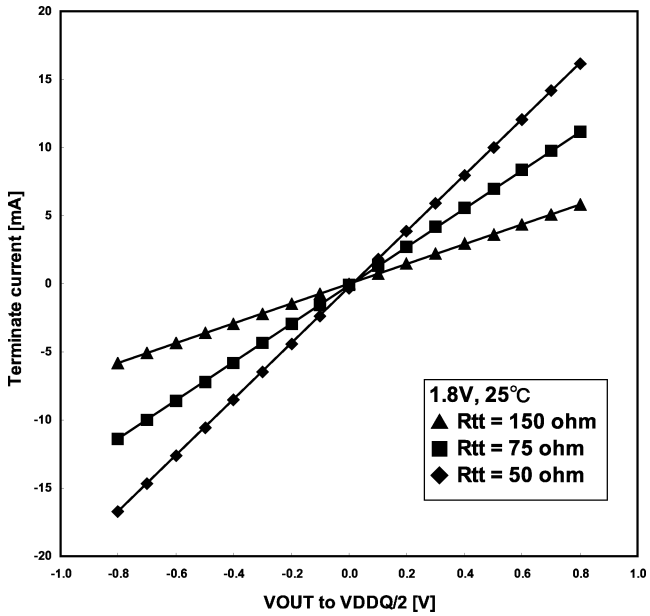

Fig. 13. Measured ODT characteristics.

The strength of the OCD measured as a function of the control code is shown in Fig. 12. The OCD adjust circuit composed with multi-oxide transistors has 16-step variable strength, where the target strength of 18 Ω $+30\%/-40\%$ can be achieved at any voltage or temperature. Fig. 13 shows the measured termination current of ODT circuits. This result indicates that the linearity of the ODT resistance is sufficient at 50, 75, and 150 Ω.

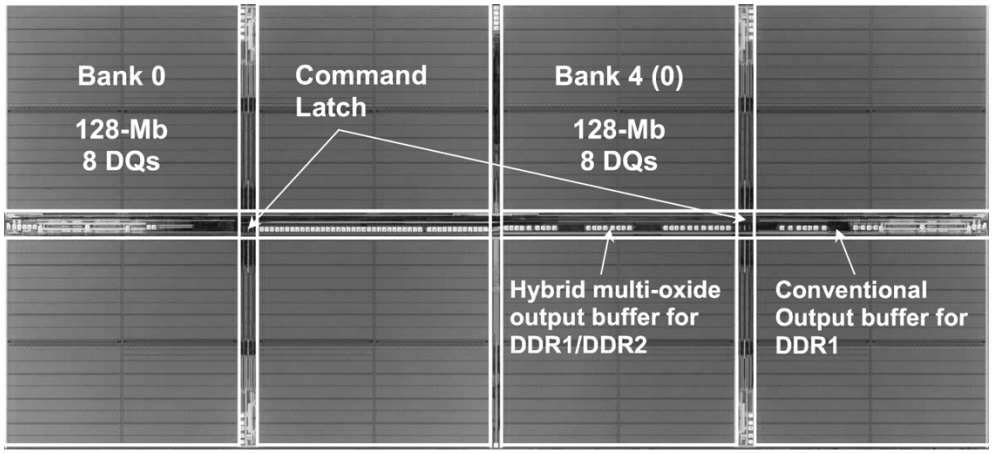

Fig. 14. Microphotograph of the 1-Gb DDR1/DDR2 SDRAM.

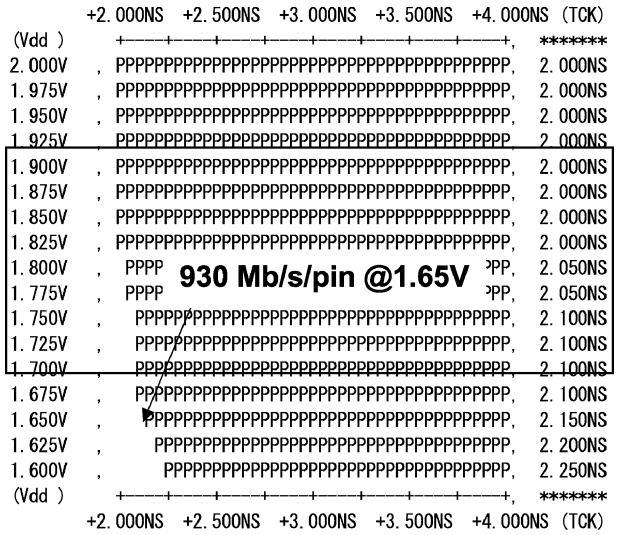

Fig. 15. Measured shmoo plot (DDR2 $\mathrm{CL} = 5$ operation).

V. Fabrication and Measurement

Fig. 14 shows a microphotograph of our 1-Gb DDR1/DDR2 SDRAM. The 128-Mb memory area is equal to one bank area for DDR2 and a half bank area for DDR1 operations. The command latch circuits are located at the right and left sides of the chip. The hybrid multi-oxide output buffer for DDR1/DDR2 is located in the right half of the pad area.

Fig. 15 shows the measured shmoo plot of the cycle time versus supply voltage. It can be seen that the maximum data rate at 1.65 V is 930 Mb/s/pin, which is enough for DDR2-800 operation with a column latency of 5.

Table II summarizes the device features of the 1-Gb DDR1/DDR2 SDRAM fabricated using 0.10-μm triple-metal CMOS process technology. The cell size is 0.098 μm^2, and the chip size is 175.3 mm^2, which is small enough to assemble in a standard 66-pin 400-ml TSOP or 68-pin μBGA.

VI. Conclusion

We have developed a 1.8-V 800-Mb/s/pin DDR2 and 2.5-V 400-Mb/s/pin DDR1 compatibly designed 1-Gb SDRAM using 0.10-μm technology. This is achieved by using three circuit techniques for a DDR1/DDR2-compatible chip architecture designed for both high-speed and high-density DRAMs. The dual-clock input-latch scheme, which reduces the excessive timing margin for random input commands by using a pair of latch circuits controlled by dual-phase one-shot clock signals, achieves a 0.9-ns reduction in cycle time from 3.0 to 2.15 ns. Furthermore, the hybrid multi-oxide output buffer reduces the area penalty of the output buffer from 1.35% to 0.3%. The quasi-shielded distributed data-transfer scheme enables a 2.6-ns reduction in access time to 10.25 ns in both 2-b and 4-b prefetch operation. By using these techniques, we developed a 175.3-mm^2 1-Gb SDRAM that operates as an 800-Mb/s/pin DDR2 or a 400-Mb/s/pin DDR1.

TABLE II
Device Features

Architecture	DDR2	DDR1
Process	0.10 µm triple-metal CMOS	
Chip Size	19.52 mm x 8.98 mm (175.3 mm^2)	
Memory Cell	0.098 µm^2	
Data rate	400 - 800 Mbps	200 - 400 Mbps
Package	68-pin µBGA	66-pin TSOP
Organization	8 Bank, x4, x8	4 Bank, x4, x8, x16
Voltage	1.8±0.1 V	2.5±0.2 V

Acknowledgment

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