A Low-Power High-Dynamic-Range Receiver System for In-Probe 3-D Ultrasonic Imaging

Hourieh Attarzadeh, *Student Member, IEEE*, Ye Xu, *Student Member, IEEE*, and Trond Ytterdal, *Senior Member, IEEE*

***Abstract*—In this paper, a dual-mode low-power, high dynamic-range receiver circuit is designed for the interface with a capacitive micromachined ultrasonic transducer. The proposed ultrasound receiver chip enables the development of an in-probe digital beamforming imaging system. The flexibility of having two operation modes offers a high dynamic range with minimum power sacrifice. A prototype of the chip containing one receive channel, with one variable transimpedance amplifier (TIA) and one analog to digital converter (ADC) circuit is implemented. Combining variable gain TIA functionality with ADC gain settings achieves an enhanced overall high dynamic range, while low power dissipation is maintained. The chip is designed and fabricated in a 65 nm standard CMOS process technology. The test chip occupies an area of 76 μm $\times$ 170 μm. A total average power range of 60–240 μW for a sampling frequency of 30 MHz, and a center frequency of 5 MHz is measured. An instantaneous dynamic range of 50.5 dB with an overall dynamic range of 72 dB is obtained from the receiver circuit.**

***Index Terms*—CMUT, digital beamforming, in-probe ultrasound receiver, ultrasound transceiver.**

I. Introduction

ULTRASOUND imaging is widely utilized for medical imaging diagnosis because it exhibits good resolution and meanwhile, is cheap and is harmless to the human body. Capacitive micromachined ultrasonic transducers (CMUTs) have recently emerged as an alternative to piezoelectric transducers using MEMs technology [1]. The CMUT technology offers advantages such as a wider bandwidth and a better integration with electronics either through silicon vias [2]–[4] or monolithic integration [5]–[7].

Modern real-time three-dimensional (3D) ultrasound imaging systems require fully-populated two-dimensional (2D) transducer arrays with both a large number of elements (hundreds or thousands) and a very small pitch. The growing number of transducers leads to an increasing number of cables required to process the signals. To avoid this, a smart signal processing is required in the tip of the probe to reduce the number of channels to the external imaging system [8]–[10]. It also prevents the system connection cables, as the most expensive part of the system, from becoming too bulky to connect each element of the transducer array to a separate system of electronics. Moreover, a front-end circuit located close to the array can lead to improved receiver sensitivity.

Several constraints apply for the design of such in-probe receiver electronics. (i) Compact circuit design: Given the area constraint due to the compact size of each CMUT element and the limited space available in the probe tip, an area efficient design is required. (ii) Low power consumption: Since the ultrasound system requires many receive channels, the average power dissipation within the probe must be optimized. This puts a strict limit on the power budget of the receiver chain, including low noise amplifier (LNA), variable gain amplifier (VGA), and ADC circuitry. (iii) High dynamic range design: To accurately monitor both small and large signals, a high dynamic range is required. This requires a low noise flexible receive circuit design with a relatively high gain setup and the ability to dynamically change the gain as with the input level changes.

Fig. 1 shows a typical ultrasound receiver system block diagram for one readout channel. To build an ultrasound image, the receiver system stores the received pulses from a focal point, aligns them in time, and adds multiple channels coherently. In analog beamforming (ABF) (Fig. 1(a)), the output signals from each transducer are amplified through a VGA, which functions as a time-gain-compensation amplifier (TGC) to compensate for attenuation of the return signal. The signals are then delayed and summed with the other channels inside a group. Then, the cables transport the analog data to a signal processing unit, which digitizes the data and obtains the final ultrasound image. In a digital beamforming (DBF) imaging system (Fig. 1(b)), the echo signals from the TGC amplifiers in all the readout channels are ultimately converted to digital with ADCs inside the probe, and a digital beamforming is also performed. DBF architectures have advantages over ABF, as finer adjustments is achieved by bringing the digital system closer to the ultrasonic transducers. However, one significant challenge is the high power consumption as an ABF imaging system needs only one ADC for all the channels, whereas a DBF system requires dedicated ADC for each single channel. Sharing the ADC between receiver channels in [11] is a solution where a 16:1 analog multiplexer is used to share the ADC for 16 channels instead of providing 16 ADC channels. However, the shared A/D converter scheme needs to perform 16 iterative operations, accessing different channels, to complete one scan. Additionally, this architecture requires extra

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The authors are with the Department of Electronics and Telecommunication, Norwegian University of Science and Technology, Trondheim 7491, Norway (e-mail: hourieh.atarzadeh@iet.ntnu.no; ye.xu@iet.ntnu.no; trond.ytterdal@iet.ntnu.no).

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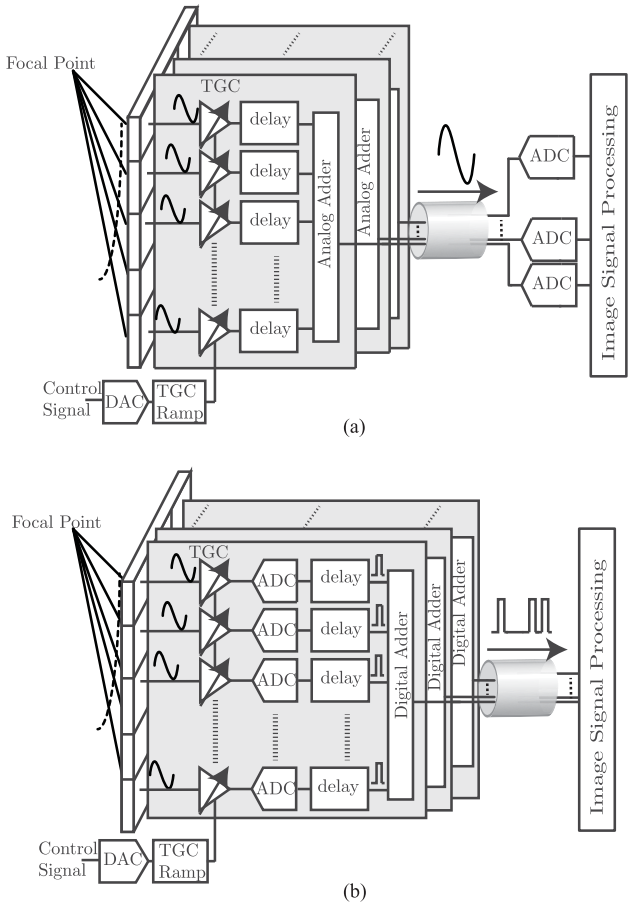

Fig. 1. (a) An analog vs. (b) digital receive ultrasound beamforming scheme.

digital controls. In [12], an analog-digital-hybrid beamforming architecture is used for the receive beamformer design, where 64 channels are fed to eight 8-channel ABFs, and then 8 outputs of the analog beamformer are applied to a DBF circuit. By using this method, the number of ADCs is reduced by 8 times. However, using this hybrid architecture, the ABF still has high power demands and large amounts of analog memory are required.

In this paper, a very low-power, high-dynamic-range receiver circuit design, as a partial implementation of a DBF system, is presented. A variable gain TIA amplifier and an ADC circuit are implemented as the key building blocks for one receive channel. The circuit is reconfigured for two modes of operation; at the beginning of the hearing phase where the ultrasound return signal is close to the full-scale voltage, the CMUT output signal is directly coupled to the ADC circuit, thus the circuit operates in a low power mode. ADC gain correction techniques are then employed to obtain a constant SNR at the output as the input signal attenuates [13]. With the input signal reflected from very deep tissue being too weak, it is not practical for the ADC to maintain a constant SNR; hence, an amplifier is plugged into the system to provide a high enough gain to map the signal to the ADC input dynamic range, thus a high dynamic range is obtained in this alternative mode. The circuit was implemented using 65 nm CMOS technology, where the CMUT ultrasound transducer equivalent circuit was replaced by an on-chip

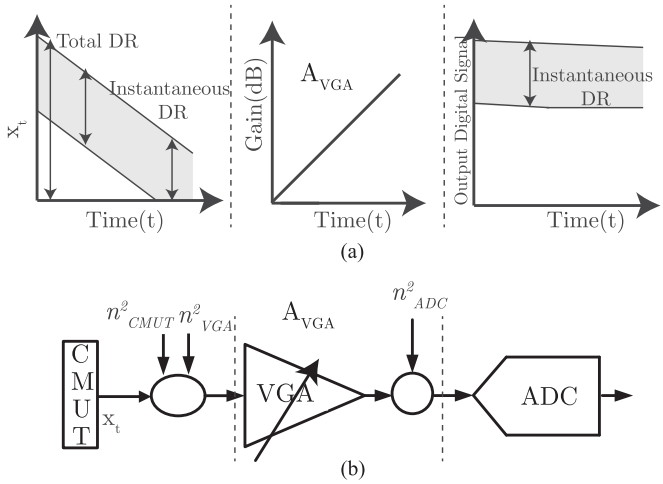

Fig. 2. (a) Input/output dynamic range of an ideal time-gain-compensation scheme (b) Time gain compensation block diagram.

equivalent circuit. Based on the promising results of a low power consumption, small area, and reasonably high dynamic range, the receiver circuit design can be scaled up in the future to a fully-integrated receiver circuit, capable of reading out a 2D array with hundreds of ultrasound elements.

The rest of this paper is organized as follows: In Section II, an ultrasound time-gain-compensation scheme is presented. In Section III, the receiver chip design is described, where different dynamic range enhancement techniques are discussed based on the design specification. Section IV presents the proposed configurable receiver circuit design and a detailed gain range for each sub-block. The CMOS chip experimental results are given in Section V, and the conclusion is drawn in Section VI.

II. Ultrasound Time Gain Compensation Scheme

During the receive cycle, the acoustic signal penetrates through the body with an attenuation rate of 1 dB/cm/MHz. For a 5 MHz center frequency and a 4 cm penetration depth, the signal attenuation is around 40 dB ($2 \times 4 \times 5$), where the prefactor 2 accounts for the return path. Adding a minimum display resolution of 50 dB [14], an approximate total dynamic range of 90 dB is required to process this signal over the full receive interval. This dynamic range is far beyond the range of a practical ADC. On the other hand, additional dynamic range can be achieved using multiple channels. For instance, in an ultrasound receiver system, a total of 128 channels increases the dynamic range by 21 dB ($10 \times \log(128)$), which still leaves 70 dB of dynamic range to be handled by the ADC.

Fig. 2(a) shows the dynamic range of the input signal x_t consisting of two parts: the instantaneous dynamic range, which depends on the characteristics of the medium, and the dynamic range, which results from propagation attenuation. By limiting the SNR of the ADC to the instantaneous dynamic range and introducing a time gain compensation amplifier that maps the attenuated signal to the available instantaneous dynamic range of the ADC, a great deal of power is saved while still maintaining a wide dynamic range.

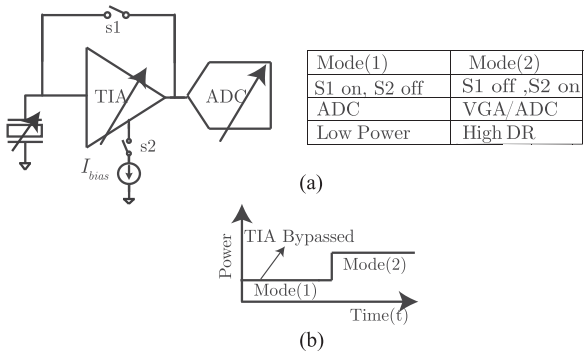

Fig. 3. (a) Proposed dual mode receive circuit architecture and (b) power consumption over the entire receive period.

The system-level noise model for the ultrasound receiver is illustrated in Fig. 2(b). Considering x_t as transducer input signal and input to the VGA, the signal to noise ratio (SNR) of the receiver is obtained by dividing the output signal power to the output noise power as follows:

$$\begin{aligned} SNR &= \frac{(A_{VGA}.x_t)^2}{\overline{n_{adc}^2} + A_{VGA}^2\overline{n_{VGA}^2} + A_{VGA}^2\overline{n_{CMUT}^2}} \\ &= \frac{1}{\frac{1}{SNR_{ADC}} + \frac{1}{SNR_{VGA}} + \frac{1}{SNR_{CMUT}}} \\ &\approx \min(SNR_{CMUT}||SNR_{VGA}||SNR_{ADC}) \quad (1) \end{aligned}$$

The CMUT thermal-mechanical noise is denoted as $\overline{n_{CMUT}^2}$, and the VGA and ADC input referred noise are denoted as $\overline{n_{vga}^2}$ and $\overline{n_{adc}^2}$, respectively. Ideally, a constant SNR is desired over the entire receive period, where SNR_{CMUT} is the ultrasound input signal dynamic range, SNR_{VGA} is the signal to noise ratio at the VGA output, and SNR_{ADC} is the ADC SNR. For an ADC with N bit resolution and a full-scale range input signal, a signal to noise ratio equal to $6.02N + 1.76$ (dB) is obtained. Over the receive cycle, A_{VGA} is adjusted in such a way that a constant SNR_{ADC} is obtained by maintaining a full-scale ADC input signal. At the beginning of each receive period, the input signal is very large, hence, $SNR_{CMUT} >> SNR_{ADC}$. Thus, the output SNR is decided by the SNR_{ADC}. Over the receive interval, the signal strength attenuates as it penetrates through tissues. Therefore, SNR_{CMUT} starts to become comparable with the SNR_{ADC}, and the Dynamic Range (DR) of the input signal starts to have a large effect on the output SNR. Alternately, in order not to degrade the output SNR, the VGA output noise level should be adaptively adjusted in such a way that $n_{VGA}A_{VGA} << n_{ADC}$ over the instantaneous dynamic range of the input signal.

III. Receiver Circuit Architecture

Fig. 3 shows the proposed circuit, which provides the flexibility of operating either in a low power consumption (mode1), or a high dynamic range mode (mode2). Fig. 4 demonstrates input/output dynamic range of the proposed dual mode compensation scheme. At the beginning of a receive cycle after the transmit pulses, the received signal from the transducer is close to the full-scale voltage. Therefore, the ADC can directly handle the input signal (mode(1)), and the TIA is bypassed by switch S1 in Fig. 3. Over time, as the received ultrasound signal becomes too weak, an ADC design which can handle such a small signal is no longer practical. Thus, a VGA is used to amplify the weak signal and map it to the ADC full-scale voltage (mode(2)). In this design, coarse discrete gain settings of a TIA amplifier are combined with the ADC reconfigurability to maintain a constant SNR at the output node. In the operating mode(1), as the switch bypasses the TIA from the receiver path, the bias current to the TIA is also switched off. As a result, the average power consumption of the TIA is largely conserved in the entire receive period (See Fig. 3(b)).

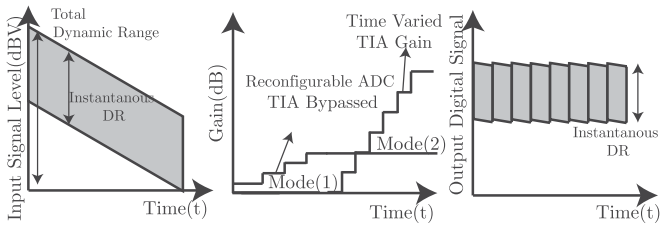

Fig. 4. Input/output dynamic range of the proposed dual mode compensation scheme.

A. Analog to Digital Converter

Requiring a small area due to the limited die area available for each receiver channel, with a high enough sampling rate and a reasonable dynamic range is the major concern in the ADC design for the ultrasound imaging application. For a digital beamforming scheme, the sampling rate of the ADC converter can be determined by the target sampling resolution, where the sampling time step determines the delay resolution. In this design, to achieve a delay resolution of around 30 ns, a sampling frequency of 30 MHz is required. For a target transducer center frequency of 5 MHz with 100% bandwidth, the bandwidth of the reflection signals will be 2.5–7.5 MHz. Therefore, an oversampling ratio of 2 for the ADC is considered. The effective bit resolution is determined based on the characteristics of the medium. In this work, the target medium is the tissue in human organs, which requires at least 50 dB of image resolution [14]. Therefore, the required effective bit resolution of the A/D converter is 9-bit.

Considering the need for a dedicated ADC for each receive channel in DBF architecture, the ADC as the most power hungry block has to maintain a very small power consumption. The pipeline ADCs are approximately one order of magnitude less energy efficient than successive approximation(SAR) and Delta sigma ADCs [15]. Delta sigma ADCs are power efficient along the higher resolution ADC [16], and SAR type ADC appears to be the architecture that is most energy efficient over a broad range of low to medium resolution [17]. Another key design guideline for digital beamforming system is the ADC area efficiency, considering the area constraint due to the compact size of each CMUT element and the limited space available in

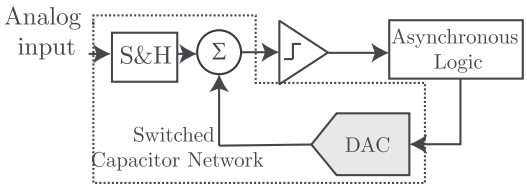

Fig. 5. SAR ADC architecture.

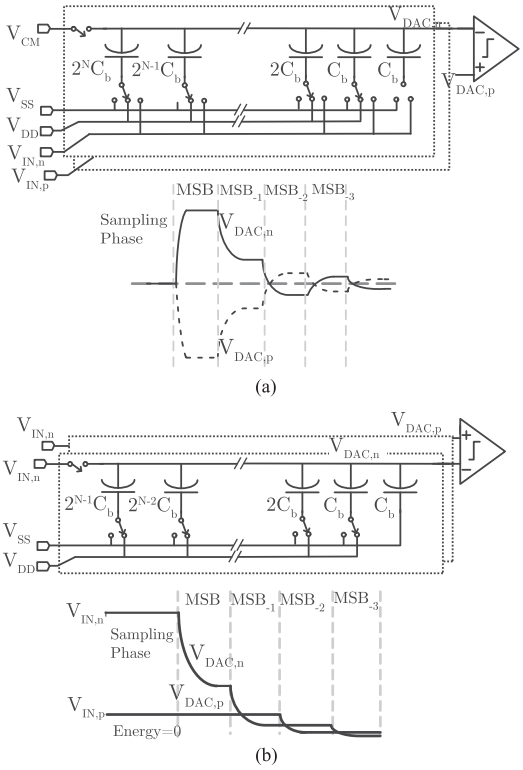

Fig. 6. (a) Conventional switching vs. (b) monotonic switching for N bit DAC array.

the probe tip. Owing to their simple architecture, a very small area can be achieved with the SAR ADC architecture. As a result, A SAR-type ADC converter was selected due to its low area and low power consumption in the target medium frequency.

1) SAR ADC: A diagram of a SAR ADC is shown in Fig. 5. The analog input signal is sampled and held first, and a comparison is made to determine if the input voltage is less than or greater than the DAC voltage. To obtain a DAC voltage, a binary search algorithm is conducted until it converges on the input signal. A switched capacitor network for sampling the input signal and implementing the DAC switching network is employed to minimize the power consumption.

Fig. 6 shows a conventional N-bit fully-differential binary-weighted capacitor network [18]. At the sampling phase, the bottom plates of the capacitors are charged to $V_{in,n}$ and $V_{in,p}$, and the top plates are reset to the common-mode voltage V_{cm}. Next, the largest capacitor 2^N is switched to the reference voltage V_{ref}, and the other capacitors are switched to V_{ss}, where N is the ADC resolution. The comparator then performs the first comparison on the DAC output voltages $V_{dac,n}$ and $V_{dac,n}$. If

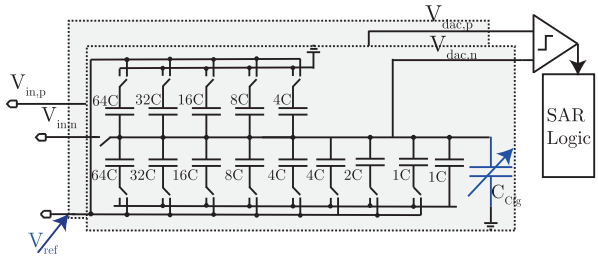

Fig. 7. Proposed split-capacitor reconfigurable DAC array.

$V_{in,p}$ is higher than $V_{in,n}$, the most significant bit (MSB) is assigned to be '1'. Otherwise, the (MSB) is assigned to be '0', and the largest capacitor is reconnected to ground. Then, the second largest capacitor is switched to V_{ref}. The comparator does the comparison again. The ADC repeats this procedure until the least significant bit (LSB) is decided. The conventional DAC switching operation is based on the trial-and-error search procedure, which is not an energy-efficient switching scheme. Fig. 6(b) shows a monotonic switch for an N-bit DAC array. By sampling the input signal directly on the top plate of the capacitors array, the comparator directly performs the first comparison without consuming any energy [19]. Moreover, the total DAC capacitor is reduced by two times. In a monotonic switching scheme, the switching in the DAC network is performed in either an upward or downward direction.

2) Split-Capacitor DAC Array Design: Fig. 7 shows the schematic of a 9-bit SAR ADC used in the receiver design. To avoid large variance in the common mode voltage of the comparator input [20], the first five MSB capacitors are split into half, and each differential array switches in complementary directions. Unlike the monotonic switching scheme, the switching in the DAC network is performed in both upward and downward directions, hence, a constant common mode voltage is maintained. A customized small-value metal-metal capacitor was used to save power and area in the DAC switching network. A minimum unit capacitor value is chosen to be 0.5 fF resulting in a total capacitance of 256 fF in a differential 9-bit ADC [17]. An asynchronous dynamic digital SAR Logic was designed to simplify circuits and minimize the switching activities.

3) Configurable Gain ADC: In this design, ADC gain techniques were used to enhance the dynamic range of the ADC [13]. The DAC switching network voltage for the positive and negative half-circuit is as follows:

$$V_{dac,p} = V_{in,p} + 0.5\sum_{i=1}^{6}\frac{C_i}{C_{tot}}V_{ref}(2b_i - 1) - \sum_{i=7}^{9}\frac{C_i}{C_{tot}}V_{ref}b_i$$

$$V_{dac,n} = V_{in,n} - 0.5\sum_{i=1}^{6}\frac{C_i}{C_{tot}}V_{ref}(2b_i - 1) - \sum_{i=7}^{9}\frac{C_i}{C_{tot}}V_{ref}(1 - b_i) \quad (2)$$

where V_{ref} is the reference voltage of the DAC, C_{tot} is the total capacitance at each DAC output node (i.e., $C_{dac} + C_{cfg}$), and C_{cfg} and C_{dac} are the configuration capacitor and the DAC capacitance, respectively. As the equation suggests, with $V_{in,p}$ and $V_{in,n}$ scaling, the DAC swing can be scaled with the same ratio by either tuning the V_{ref} or adjusting the C_{tot}. By adjusting the DAC switching voltage range, the quantization noise is updated as follows:

$$P_q = \frac{LSB^2}{12} = \frac{1}{12}\left(\frac{V_{ref}}{2^N}.\frac{C_{dac}}{C_{Cfg}+C_{dac}}\right)^2 \tag{3}$$

In this work, the DAC swing voltage adjustment is performed by connecting a programmable parallel capacitor to the main DAC, as shown in Fig. 7, and adjusting an external V_{ref} voltage.

B. TIA Circuit Design

Different types of amplifiers have been employed to measure CMUT current signal. These include switch capacitance charge integrating amplifiers [21], charge based amplifiers [22], [23] and transimpedance amplifiers [2], [7], [24], etc. Among them, transimpedance amplifier employs a resistive feedback to readout the CMUT current signal. In order to maximize the received input current, the TIAs provide low input impedance, which make them suitable for high impedance CMUTs readout [25]. Moreover, no dc settling network is required, as in charge based amplifiers, and no charge injection issue is present in the design of such amplifiers, as in switched capacitor amplifiers. Detailed discussions on tradeoff between the gain, and bandwidth and noise performance of these amplifiers are presented in [7], [24].

The schematic of the resistor feedback TIA and its full transistor implementation are depicted in Fig. 8 [26]. Having the goal of minimizing the chip area in mind, a single-stage simple cascode common source amplifier with a gain of -70 V/V is used. On the other hand, a less accurate transimpedance gain due to the low DC gain could be corrected digitally during signal processing. Therefore, a simpler design is likely a good tradeoff. Ideally, the TIA gain should vary in such a way that the gain increases continuously with time to match the rate of attenuation (See Figs. 1 and 2). However, very fine steps are required to implement such a design which complicates the design of the amplifier. In this design, to make the implementation simple, 8 discrete gain steps are provided, which are programmed by the 3-bit digital inputs, decoded and applied to the switches in the feedback resistor network (See Fig. 8(b)). The TIA amplifier is usually followed by an anti-aliasing filter that is preceded by an ADC. The anti-aliasing filter avoids the ADC from mapping high-frequency noise and extra signals beyond the maximum CMUT operating frequency. In this design, M9 and M10 are used as MOS-capacitors to filter out-of-band noise.

Fig. 8(c) depicts the wide swing cascode current mirror used to generate the bias voltages for the TIA amplifier. The bias current I_{bias} is switched off in operating mode (1), to turn the TIA power consumption off and reduce the total power consumption. A fast TIA wake-up within 20 ns is obtained.

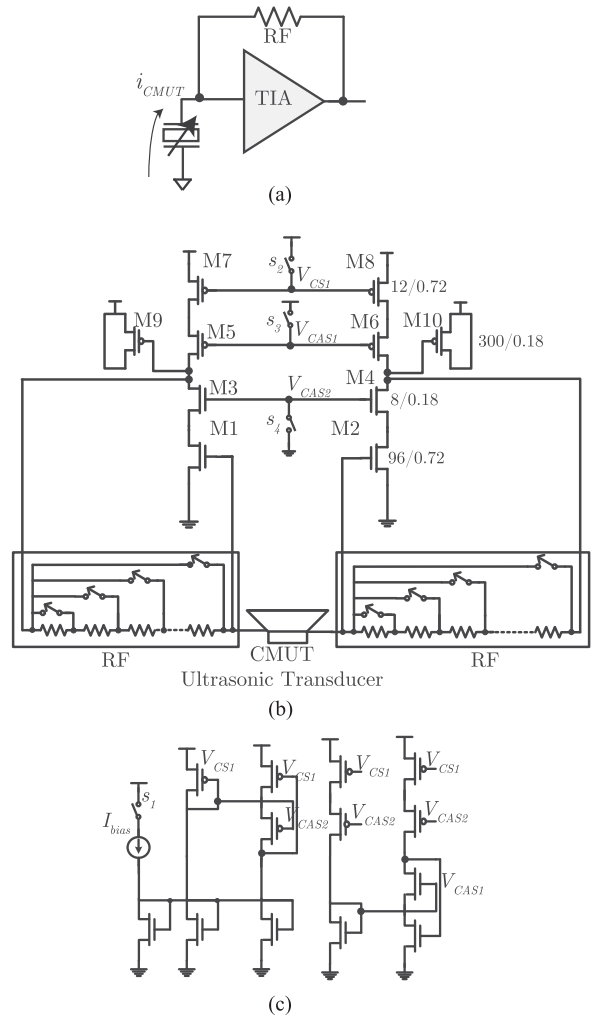

Fig. 8. (a) TIA amplifier topology (b) Resistor feedback TIA full transistor implementation (c) TIA bias circuit.

IV. Configurable Gain Receiver Design

Fig. 9 illustrates the receiver circuit interface to the CMUT ultrasound in different operating modes. The small-signal model for a CMUT element is represented by a capacitor, resistor and a current source in parallel, as shown in Fig. 9(a). The capacitor C_{CMUT}, is the parallel-plate capacitance between the CMUT element membrane and the common node; The resistor R_{CMUT}, is the medium mechanical load at the CMUT surface that is transformed to the electrical port. The small signal current source i_{CMUT}, is the current produced by the CMUT element and is proportional to the CMUT element area and its sensitivity. In this work, the front-end circuit has been designed based on the CMUT electrical parameters as shown in Fig. 9(a) [27].

In Fig. 9(b) the CMUT is connected to a TIA amplifier, where the I/V conversion for the i_{CMUT} is performed by the TIA. The TIA gain varies (R_F) in such a way that a constant voltage ($R_F i_{CMUT}$) is obtained at the ADC input as the i_{CMUT} gets weaker. In Fig. 9(c) the CMUT is directly coupled to the ADC input; as a result, the I/V conversion is preformed at the ultrasound input node, where the voltage formed at the ADC is

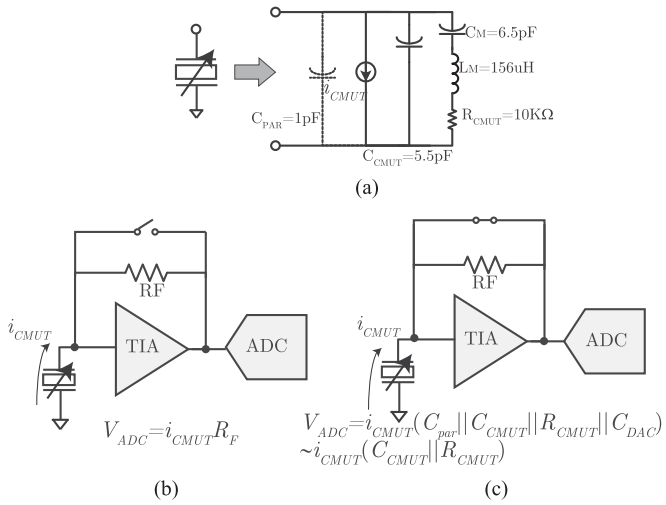

Fig. 9. (a) CMUT equivalent small signal model (b) CMUT interface to ADC in mode(2) (c) CMUT interface to TIA in mode(1).

simply equal to: $i_{CMUT}(R_{CMUT}||C_{CMUT})$. Ideally, the switching occurs automatically, and it is a part of the automatic gain compensation (AGC) unit. In this design, the switching between different modes is performed manually.

In the next sections, the implementation of the ADC and maximum and minimum gain range requirements of the TIA circuit are elaborated based on the design specification.

A. Configurable SAR ADC Design

In this work, the DAC swing voltage adjustment is performed in two different ways [13]:

(1) By connecting a parallel capacitor to the main DAC, as shown in Fig. 7, the DAC swing is modified by a ratio of $C_{dac}/(C_{dac}+C_{Cfg})$. However, to create multiple signal swings, more parallel capacitors and switches are required, which in turn increases design complexity and occupies more area. Moreover, a higher parasitic DAC increases the DAC settling time and in return limits the ADC performance.

(2) By adjusting the V_{ref} connected to the DAC switches, the DAC switching voltage is modified by a ratio of V_{dd}/V_{ref}. However, a lower reference voltage weakens the driving capacity of the switches connected to V_{ref}, which can cause incomplete DAC settling; as a result, V_{ref} can only be tuned in a certain designed range.

For a V_{ref} equal to full-scale voltage, the noise power for the DAC array and the comparator is simulated to be 0.5 mVrms and 1 mVrms, respectively. As the V_{ref} and C_{cfg} start to scale, the quantization noise scales with the same ratio, and the DAC thermal noise scales with $\sqrt{\frac{KT}{C_{dac}+C_{cfg}}}$, while the comparator noise remains constant. For instance, when the V_{ref} is set to 0.5 V, the comparator noise is simulated to be equal to the quantization noise(i.e., $1LSB$). This puts another practical limit on how far the dynamic range can be pushed by using the ADC gain techniques. In this prototype, an external voltage source is used as V_{ref}, which is varied from 0.7 V to 1 V, and a C_{cfg} of 40fF to a total C_{dac} of 128fF is added. The gain setting and the dynamic range of the ADC are summarized in Table I.

TABLE I
ADC GAIN SETTING

$V_{in}(V_{p\text{-}p,\,diff})$	DR(dB)	$V_{ref}(V)$	$C_{cfg}(fF)$	$C_{tot}(fF)$
1.8	50.5	1	0	128
1.5	50.2	0.7	0	128
0.9	50	0.7	40	168

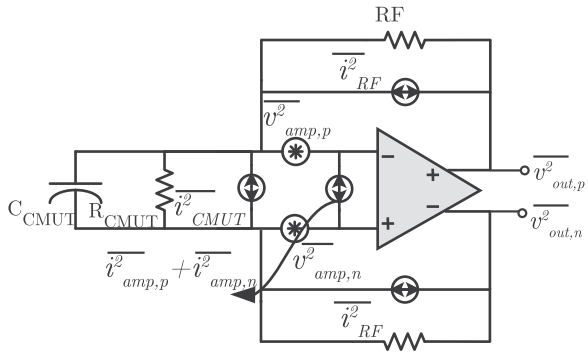

Fig. 10. The schematic of the system noise components for a fully differential TIA.

B. TIA Gain Range Design

The TIA gain varies with the transducer current in such a way that the signal strength at the TIA output (i.e., the ADC input) is constant over time. In this design, a constant output voltage needs to be maintained at the TIA output for the V_{ref} and C_{cfg} equal to 0.7 V and 40 fF, respectively.

1) Minimum TIA Gain: With the input signal being too low to be directly handled by the ADC and still too high for a high gain TIA, the TIA needs to provide a low gain for large input signals to avoid saturation of the next stage. Alternatively, to maintain a smooth transition in the ADC input voltage between two different modes as shown in Fig. 9, the requirement for the minimum gain must be fulfilled as follows:

$$\begin{aligned} V_{ADC} &= i_{CMUT}(C_{CMUT}||R_{CMUT}) = i_{CMUT}R_{F,\,\min} \\ &= > R_{F,\,\min} = 5\ \text{k}\Omega \end{aligned} \tag{4}$$

2) Maximum TIA Gain: At the TIA high gain setup, the receiver is optimized for a small-signal CMUT current. The CMUT and TIA output referred noise seen at the ADC input should be smaller than the ADC's noise ($\overline{v^2_{ADC}}$) by a predefined margin. Otherwise, the dynamic range of the ADC would be scarified.

A schematic of the noise sources of a differential TIA and the CMUT element is plotted in Fig. 10. The noise contribution of each half-circuit, as well as the CMUT is depicted individually. Ignoring the CMUT and amplifier parasitic capacitance, the

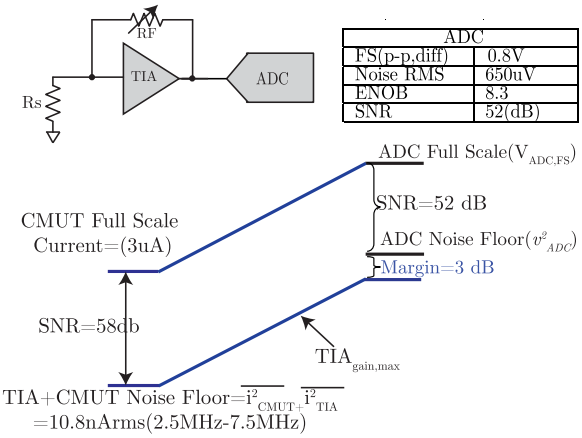

Fig. 11. Maximum TIA gain requirement analysis.

differential output noise power is expressed as:

$$\overline{v_{out,diff}^2} = 2\left[R_F^2\overline{i_{R_F}^2} + (1+\tfrac{R_F}{Z_{CMUT}})^2\overline{v_{amp}^2}\right] + 4R_F^2\overline{i_{CMUT}^2} \quad (5)$$

where $\overline{i_{RF}^2}$ is the thermal noise of the feedback resistor; Z_{CMUT} is the CMUT impedance equal to $C_{CMUT}||R_{CMUT}$; $\overline{v_{amp}^2} = \overline{v_{amp,p}^2} = \overline{v_{amp,n}^2}$ is the input equivalent voltage noise of the core amplifier. By referring the output noise to the CMUT input node, the input current referred noise is described as:

$$\overline{i_{in}^2} = \frac{\overline{v_{out,diff}^2}}{{R_F}^2} = 2\left[\overline{i_{R_F}^2} + \frac{\overline{v_{amp}^2}}{(R_F||Z_{CMUT})^2}\right] + 4\overline{i_{CMUT}^2} \quad (6)$$

Assuming $R_F >> Z_{in}$ and a noise figure of 3 dB in which the amplifier contributes the same amount of noise as the CMUT, a total input referred current noise of 10.8 nA_{rms} for 2.5–7.5 MHz is calculated at the TIA input node. As shown in Fig. 11, the maximum TIA gain is then determined as follows:

$$\begin{aligned} R_{F,\text{max}} &= 10log\left(\frac{\overline{v_{ADC}^2}}{\overline{i_{in}^2}}\right) \\ &= 20log\left(\frac{650\ uVrms}{10.8\ \text{nA}}\right) - 3\ \text{dB} = 92.5\ \text{dB}\Omega \\ &\Rightarrow\ R_{F,\text{max}} = 42\ \text{k}\Omega \end{aligned} \quad (7)$$

The total measured power consumption is summarized in Table II for different TIA/ADC gain settings. A maximum differential gain of 97 dBΩ is obtained at the center frequency of 5 MHz.

3) Bandwidth Consideration: In this design, the overall bandwidth of the system is influenced by different switching modes. The bandwidth in each switching mode is described as follows: In switching mode(2), assuming the TIA's input is a virtual ground, the bandwidth is mostly determined by the TIA.

TABLE II
TOTAL MEASURED POWER CONSUMPTION FOR DIFFERENT TIA/ADC GAIN SETTINGS AT 30 MHZ CLOCK FREQUENCY

$V_{inp\text{-}p,diff}$	Differential TIA gain(dBΩ)	total power(μW)	V_{ref}(V)	C_{fg}(fF)
1.8	0	60	1	0
1.3	0	60	0.7	0
0.9	0	60	1	40
0.53	86	240	0.7	40
0.33	89	240	0.7	40
0.24	92	240	0.7	40
0.18	95	240	0.7	40
0.13	97	240	0.7	40

The TIA transfer function is as follows:

$$\frac{v_{out}}{i_{CMUT}} = \frac{R_F w_n^2}{s^2 + 2\zeta w_n s + w_n^2} \quad (8)$$

$$w_n = \sqrt{\frac{g_m}{R_F[C_{AAF}+C_{DAC}]C_{CMUT}}} \quad (9)$$

$$\zeta = \frac{\frac{1}{R_F C_{CMUT}} + \frac{1}{R_F[C_{AAF}+C_{DAC}]} + \frac{1}{R_{CMUT}C_{CMUT}}}{2w_n} \quad (10)$$

where C_{AAF} is the anti-aliasing capacitor in the TIA preceded by the ADC (see Fig. 8), and g_m is the transconductance of the TIA input transistor. The values of which are chosen in such a way that a ζ range of 0.9–1.12 and a bandwidth range of 7.5 MHz to 10 MHz are obtained.

In switching mode (1), as shown in Fig. 9(c), the BW is determined by the CMUT itself ($R_{CMUT}||C_{CMUT}$), as well as the loading of the rest of the system. Having a high capacitive CMUT, a smaller bandwidth than the previous switching mode is obtained, which can be compensated in digital domain system design and is beyond the scope of this paper.

V. MEASUREMENT

Fig. 12 shows the test chip manufactured in a 65 nm CMOS process technology with a core chip area of 170 μm × 76 μm. The ADC in the core circuit occupies 118 μm × 76 μm, and the TIA occupies 50 μm × 70μm. For the ADC layout design, the symmetrical DAC arrays are placed sidewise, while the comparator and the digital logic are located in the middle. Custom-designed metal-metal capacitor arrays are employed to implement the DAC switching array. A central symmetrical layout is designed to increase matching between the capacitor element units. For the TIA layout design, the fully symmetrical input stages are placed aside, while the variable feedback network is placed in the middle. The TIA input stage is implemented by cascading the minimum-sized unit cells, where the poly pitch is fixed in the design. This results in a regular pattern and a uniform density design [26], [28]. A CMUT ultrasound transducer R/C equivalent circuit was also implemented on chip to form an ultrasound-receiver test circuit for the receiver circuit measurement.

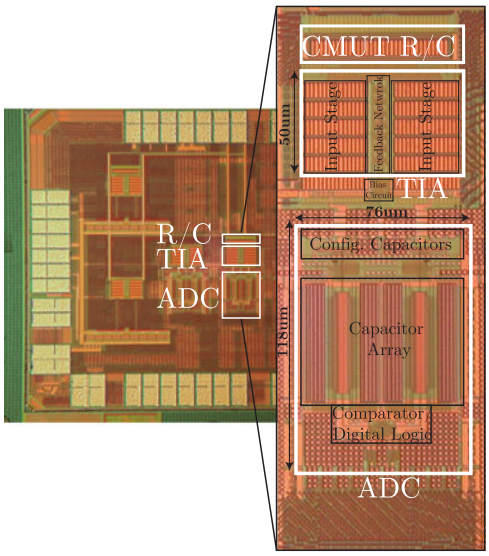

Fig. 12. Test chip micrograph.

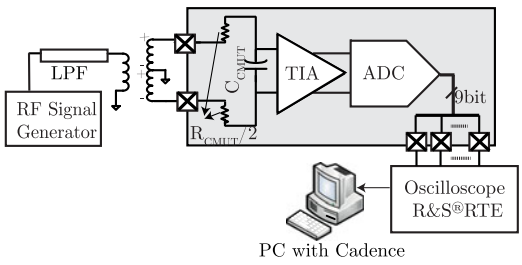

Fig. 13. Setup for measuring the test chip.

A. Measurement Setup

The test setup for the measurement is demonstrated in Fig. 13. An RC equivalent of the CMUT element is implemented on the chip. A parallel capacitor equal to C_{CMUT} and two series resistors equal to $R_{CMUT}/2$ are located after the pad. This test structure uses the Norton equivalent voltage input connected in series with the CMUT resistance R_{CMUT}. An RF balun circuit was used to convert the single-ended voltage to the differential signal. The differential voltage signals are applied to the CMUT resistor to imitate a differential current source $V_{in,diff}/R_{CMUT}$ at the input of the CMUT source model. The ADC output bits are captured using an R&S RTE digital oscilloscope with 10 logic channels, where a bus decoder generates an analog signal from the digital input signals. The analog data from the built-in DAC in the oscilloscope is then imported to cadence to perform the FFT of the signal.

The ADC requires a DC common mode input voltage roughly at 0.5 V_{DD}. Hence, in a switching mode(1), in which the CMUT is directly coupled to the ADC input, an external common mode voltage is required. In the real-life CMUT, the easiest way to create the voltage required would be a resistor voltage divider, which is switched on and off upon the TIA being turned off and on, respectively.

An oscilloscope shot of the output ADC voltage and the input voltage is shown in Fig. 14 for the two extreme TIA/ADC gain settings. Fig. 14(a) shows the ADC waveform and the measured output spectrum with the input voltage level close to the full scale voltage (1.8 $V_{p\text{-}p,\,diff}$). An SNDR of 50.5 dB is measured for the ADC with a sampling clock of 30 MHz and an input signal of 5 MHz (CMUT center frequency). Fig. 14(b) shows the maximum gain configuration for the TIA and ADC and a minimum input voltage of 130 $\text{mV}_{p\text{-}p,\,diff}$ applied. For this gain setting, V_{ref} of 0.7 V is applied, and the C_{cfg} is connected to the DAC capacitor network. With a -26 dBV input voltage applied, an SNR of 49.1 dB is achieved.

B. Dynamic Range Measurements

The receiver dynamic range is defined by calculating the ratio of the maximum input signal to the minimum input signal, which obtains SNR=0 dB at the ADC output. In this section, the dynamic range of the receiver circuit is measured for different scenarios, where different gain settings are applied for the TIA alone, ADC alone, and TIA/ADC together.

Fig. 15 shows the receiver output SNDR at the ADC output versus the input amplitude swept from 0 V to the full-scale voltage of 1.8 $V_{p\text{-}p,\,diff}$. The gain setting is only applied to the ADC and the TIA is bypassed. The peak instantaneous dynamic range is measured to be 50.5 dB. Thanks to the configurable gain feature of the ADC, the dynamic range is extended to 54 dB. Therefore, the receiver system is optimized compared to the conventional ADC design, as it offers a wider dynamic range for the system.

Fig. 16 illustrates the instantaneous SNR at the receiver circuit output for different TIA and ADC gain settings. The circuit detects small input signals of -76 dBV up to large signals of -4 dBV, which results in an overall dynamic range of 72 dB. The switching between different gain settings as (1) C_{cfg} disconnected, $V_{ref} = 1$ V, (2) C_{cfg} disconnected, $V_{ref} = 0.7$ V, (3) C_{cfg} connected, $V_{ref} = 1$ V (4) C_{cfg} connected, $V_{ref} = 0.7$ V and TIA gain from 0 dB to (6, 9, 12, 15, 18) dB creates a saw-like behavior, as shown in Fig. 16. In this work, this switching is performed manually, but in a full receiver, it should be part of the AGC, based on the input signal power.

C. Summary of Measurement Results

The measurement results for the TIA and ADC standalone and the total chip are reported in Table III. To measure the receiver TIA separately, a buffer is included in the design to drive the interconnect cable and scope capacitor. A 180 μW power consumption is measured for the TIA at 1 V supply voltage. Excluding the biasing circuit power consumption, the core TIA amplifier consumes 120 μW. The measurement result demonstrates a gain range of -0.5 dB$\sim$18 dB at the center frequency of 5 MHz. The TIA transimpedance gain range of 79–97 dBΩ is calculated directly, by dividing the measured chip voltage gain and the series input resistor of R_{CMUT}.

An Agilent E4445A spectrum analyzer was used for the noise measurements. To find the noise figure of the TIA, the noise

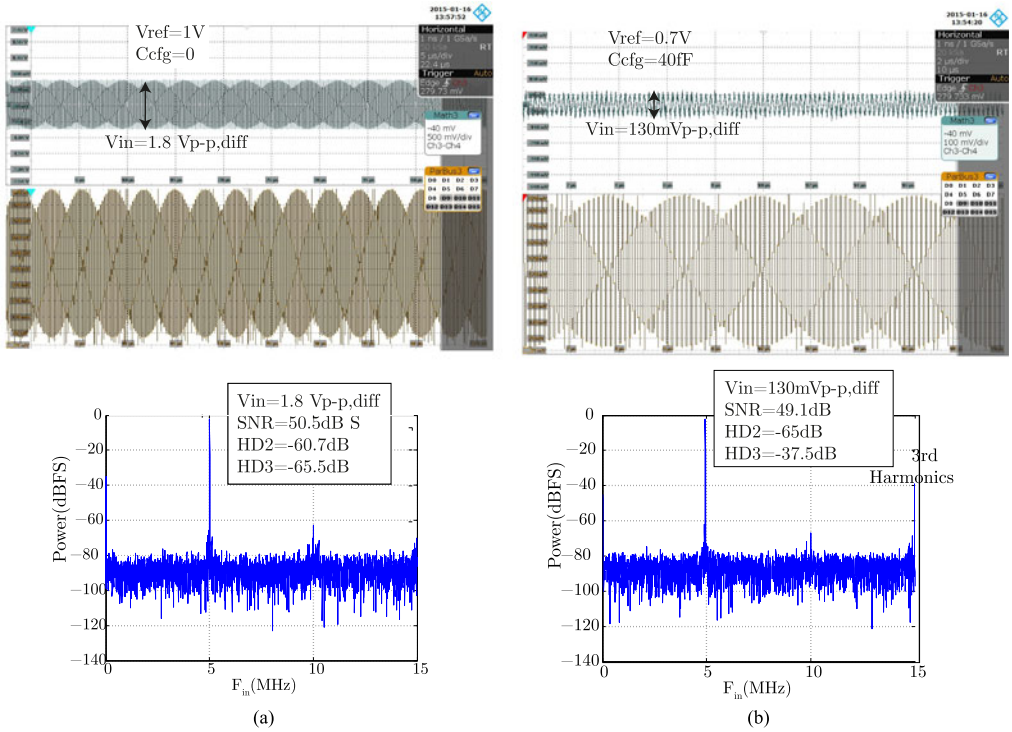

Fig. 14. (a) Minimum gain and (b) Maximum gain configuration for receiver chip.

TABLE III
SUMMARY OF THE RECEIVER CHIP MEASUREMENT

R_{CMUT}	10 kΩ
C_{CMUT}	5.5 pF
Center Frequency	5 MHz
CMUT Bandwidth	2.5–7.5 MHz
Technology	65 nm
TIA Gain Range	79 ∼ 97 dBΩ
TIA Power	180 μW
TIA Area	76 μ × 50 μm
TIA Bandwidth	7.5 MHz
HD2	−62 dB
HD3	−35 dB∼−50 dB
Input Referred Noise(@ 2.5–7.5 MHz)	4.8 pA/$\sqrt{Hz}$
NF	3 dB∼6.5 dB
Sample Rate	30 MHz
ADC Power @Fs = 30MHz	60.1 μW
SNDR @Fin=15MHz	50.3 dB
Area	76 μm × 118 μm
FOM	4.5 fJ/conv.step
DNL	0.97 LSB
INL	1.08 LSB
Total Average Chip (TIA+ADC) Power	150 μW
Total Chip Dynamic Range	72 dB
Total Chip Area	76 um × 170 um
Total NF	4.7 dB ∼ 55 dB

spectral density for the TIA, with and without a source circuit, is shown in Fig. 17. A total output-referred noise integrated over a bandwidth of 2.5–7.5 MHz is measured to be −64 dBm for the CMUT/TIA circuit and −67 dBm for the TIA standalone circuit. Hence, a 3 dB noise figure was measured for the target signal bandwidth, which indicates that the CMUT element generates the same thermal-mechanical noise as the front-end electronics. The input-referred noise current density is calculated offline from the measured output noise spectral density, to be 4.8 pA/$\sqrt{\text{Hz}}$ at the center frequency of 5 MHz.

The performance of the ADC was measured at 1 V supply, a sampling frequency of 30 MS/s and a near-Nyquist input frequency. The ADC achieves an SNDR of 50.5 dB, which equals to an ENOB of 8.1 bits. The ADC consumes 60.1 μW in total, which analog and digital circuits consume 50% of each. The peak FoM of 4.5fJ/$conv.step$ with the definition of $FoM = Power/(2^{ENOB}Fs)$, is obtained at 30 MS/s. The peak INL and DNL are measured to be −0.89 / 1.08 LSB and −0.97 /0.90 LSB, respectively.

Table IV summarizes the measurement results and compares them with those of recent receiver circuits designed for ultrasound applications. The comparison indicates that the proposed receiver design demonstrates significant power and area reduction compared with the recent works. The measured power consumptions for the TIA and the ADC are 180 μW and 60 μW, respectively. Considering the TIA to be powered off for $V_{in} > 450$ mV (see Table II), an average power range of 60 μW ∼ 240 μW for the test receiver circuit is obtained. The TIA power consumption can be further reduced by sharing the biasing circuit among other TIA amplifiers. In some ultrasound systems, delay compensation techniques may be used to produce better delay resolution than the time resolution obtained with Nyquist rate sampling. A thorough coverage is beyond the scope of this work, but examples of such systems can be found in [29]–[31].

This work focused on the receive part of the front-end circuitry. Therefore, CMUT bias circuits and receive chain

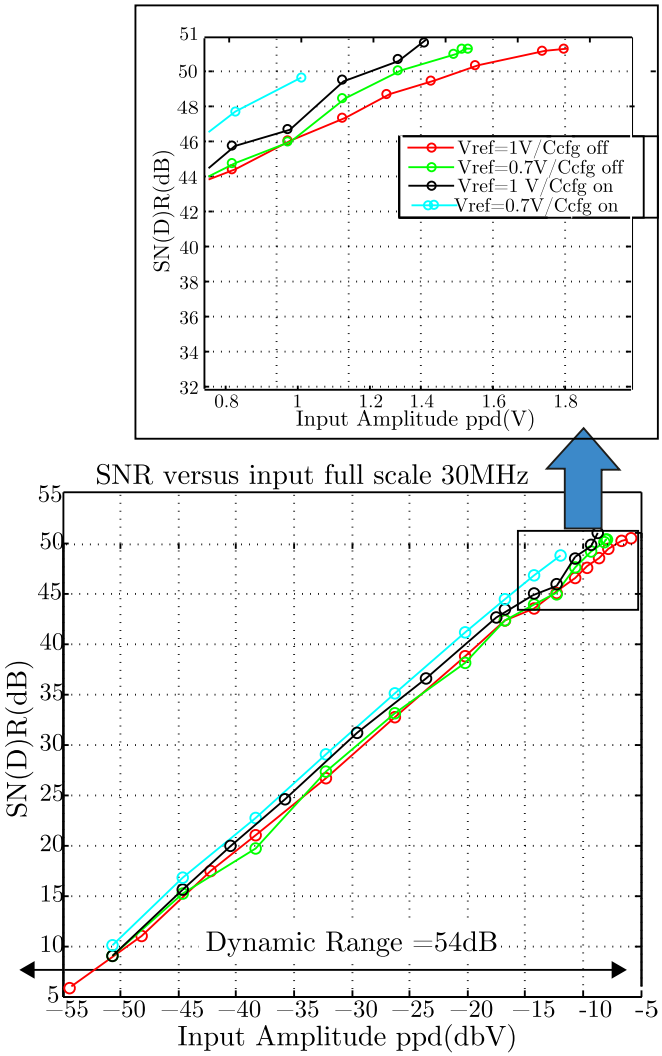

Fig. 15. Measured SNDR versus input full scale voltage for various ADC settings of V_{ref} and C_{cfg} and Fs = 30 MHz.

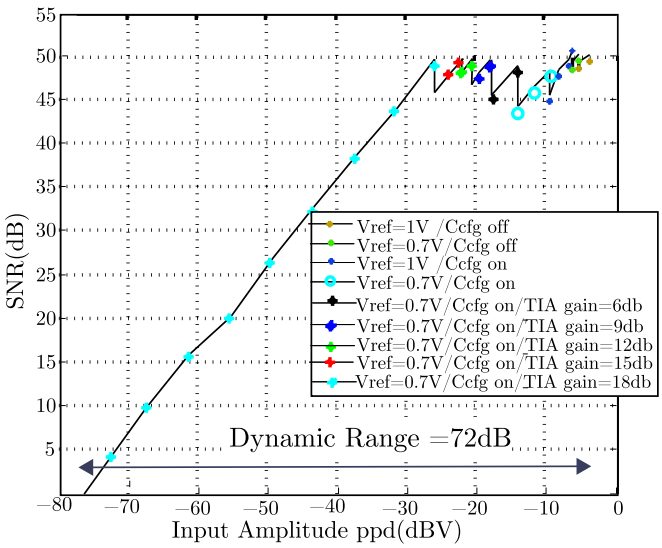

Fig. 16. Measured SNR at ADC output for various TIA and ADC gain settings at Fs = 30 MHz.

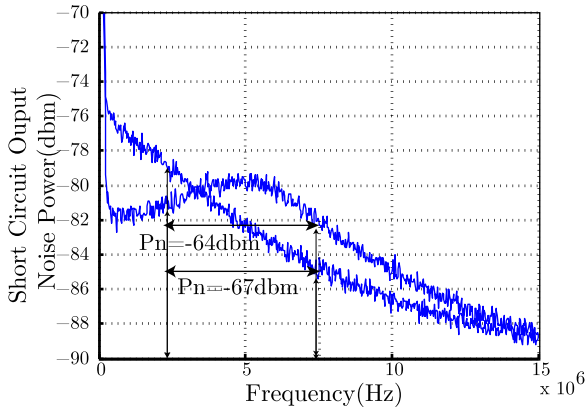

Fig. 17. Measured short circuit output voltage noise density for TIA with/without CMUT source circuit for the bandwidth 2.5−7.5 MHz

TABLE IV
PERFORMANCE COMPARISON

		This work	[32]	[33]	[23]
Preamp	Gain(dBΩ)	79-97	–	96.6	109
	Bandwidth(MHz)	7.5	–	5.2	140
VGA	Gain(dB)	–	–	–	0–30
	Bandwidth(MHz)	–	–	–	60
ADC	Resolution	9	10	–	–
	Conversion Speed(MS/s)	30	20	–	–
	Dynamic Range(dB)	72	56.8	60.5	83.2
Total chip	Power Consumption(mW)	0.06 ~ 0.240	170	14.3	3.3
	Chip size(mm^2)	0.012	3.74	0.9	–
	Technology	65 nm	0.25 um	0.18 um	0.35 um
	Number of channels	1	8	1	1

protection circuitry are not considered. However, in a complete ultrasound system, protection switches are required to protect the low voltage amplifier form the high voltage transmit pulses. Moreover, other blocks will contribute to the total power consumption which are not considered in this paper.

VI. CONCLUSION

A dual-mode receiver circuit is presented. The receiver circuit is designed for the interface with a capacitive micro-machined ultrasonic transducer (CMUT). The proposed ultrasound receiver chip enables the development of an in-probe digital beamforming imaging system. A prototype of the chip containing one receive channel with one variable gain transimpedance amplifier (TIA) and one analog to digital converter (ADC) circuit is fabricated using a 65 nm CMOS process technology. The proposed circuit provides the flexibility of operating in either a low power consumption or a high dynamic range mode. Combining the variable gain TIA functionality with the ADC gain setting achieves an enhanced overall high dynamic range while maintaining a low power dissipation. Due to its low power and

small area, the receiver circuit can be scaled up in the future to a fully-integrated receiver circuit capable of reading out a 2D array with hundreds of ultrasound elements. The test chip size is 76 um $\times$ 176 um and a total average power range of 60 μW $-$ 240 μW for a sampling frequency of 30 MHz is obtained, where a 1 V power supply, a clock sampling frequency of 30 MHz, and a CMUT center frequency of 5 MHz are used. An instantaneous dynamic range of 50.5 dB with an overall dynamic range of 72 dB is measured.

REFERENCES

[1] O. Oralkan *et al.*, "Capacitive micromachined ultrasonic transducers: Next-generation arrays for acoustic imaging?" *IEEE Trans. Ultrason., Ferroelect., Freq. Control*, vol. 49, no. 11, pp. 1596–1610, Nov. 2002.

[2] I. Wygant *et al.*, "Integration of 2D CMUT arrays with front-end electronics for volumetric ultrasound imaging," *IEEE Trans. Ultrason., Ferroelect., Freq. Control*, vol. 55, no. 2, pp. 327–342, Feb. 2008.

[3] O. Oralkan *et al.*, "Volumetric ultrasound imaging using 2-D CMUT arrays," *IEEE Trans. Ultrason., Ferroelect., Freq. Control*, vol. 50, no. 11, pp. 1581–1594, Nov. 2003.

[4] I. Wygant *et al.*, "An integrated circuit with transmit beamforming flip-chip bonded to a 2-D CMUT array for 3-D ultrasound imaging," *IEEE Trans. Ultrason., Ferroelect., Freq. Control*, vol. 56, no. 10, pp. 2145–2156, Oct. 2009.

[5] J. Zahorian *et al.*, "Monolithic CMUT-on-CMOS integration for intravascular ultrasound applications," *IEEE Trans. Ultrason., Ferroelect., Freq. Control*, vol. 58, no. 12, pp. 2659–2667, Dec. 2011.

[6] A. Nikoozadeh *et al.*, "Forward-looking volumetric intracardiac imaging using a fully integrated CMUT ring array," in *Proc. 2009 IEEE Int. Ultrason. Symp.*, 2009, pp. 511–514.

[7] G. Gurun, P. Hasler, and F. Degertekin, "Front-end receiver electronics for high-frequency monolithic CMUT-on-CMOS imaging arrays," *IEEE Trans. Ultrason., Ferroelect., Freq. Control*, vol. 58, no. 8, pp. 1658–1668, Aug. 2011.

[8] B.-H. Kim, Y. Kim, S. Lee, K. Cho, and J. Song, "Design and test of a fully controllable 64 $\times$ 128 2-D CMUT array integrated with reconfigurable frontend ASICS for volumetric ultrasound imaging," in *Proc. 2012 IEEE Int. Ultrason. Symp.*, Oct. 2012, pp. 77–80.

[9] G. Matrone, A. Savoia, M. Terenzi, G. Caliano, F. Quaglia, and G. Magenes, "A volumetric CMUT-based ultrasound imaging system simulator with integrated reception and u-beamforming electronics models," *IEEE Trans. Ultrason., Ferroelect., Freq. Control*, vol. 61, no. 5, pp. 792–804, May 2014.

[10] A. Bhuyan *et al.*, "Integrated circuits for volumetric ultrasound imaging with 2-D CMUT arrays," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 6, pp. 796–804, Dec. 2013.

[11] I. Kim *et al.*, "CMOS ultrasound transceiver chip for high-resolution ultrasonic imaging systems," *IEEE Trans. Biomed. Circuits Syst.*, vol. 3, no. 5, pp. 293–303, Oct. 2009.

[12] J.-Y. Um *et al.*, "24.8 an analog-digital-hybrid single-chip RX beamformer with non-uniform sampling for 2-D-CMUT ultrasound imaging to achieve wide dynamic range of delay and small chip area," in *Proc. 2014 IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers.*, Feb. 2014, pp. 426–427.

[13] Y. Xu, P. Harpe, and T. Ytterdal, "A 4.5fJ/conversion-step 9-bit 35MS/s configurable-gain SAR ADC in a compact area," in *Proc. 2015 IEEE Int. Symp. Circuits Syst.*, May 2015, pp. 2437–2440.

[14] H. B. Meire, *Basic Ultrasound*. Hoboken, NJ, USA: Wiley-Blackwell, 1995.

[15] B. Hershberg, S. Weaver, K. Sobue, S. Takeuchi, K. Hamashita, and U. K. Moon, "A 61.5dB SNDR pipelined ADC using simple highly-scalable ring amplifiers," in *Proc. 2012 Symp. VLSI Circuits*, Jun. 2012, pp. 32–33.

[16] Y. S. Shu, J. Y. Tsai, P. Chen, T. Y. Lo, and P. C. Chiu, "A 28fJ/conv-step CT $\triangle\Sigma$; modulator with 78dB DR and 18MHz BW in 28 nm CMOS using a highly digital multibit quantizer," in *Proc. 2013 IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2013, pp. 268–269.

[17] P. Harpe *et al.*, "A 26μW 8bit 10MS/s asynchronous SAR ADC for low energy radios," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1585–1595, Jul. 2011.

[18] J. McCreary and P. Gray, "All-MOS charge redistribution analog-to-digital conversion techniques. I," *IEEE J. Solid-State Circuits*, vol. 10, no. 6, pp. 371–379, Dec. 1975.

[19] C.-C. Liu, S.-J. Chang, G.-Y. Huang, and Y.-Z. Lin, "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 731–740, Apr. 2010.

[20] C. -C. Liu, S. -J. Chang, G.-Y. Huang, Y. -Z. Lin, and C.-M. Huang, "A 1 V 11fJ/conversion-step 10bit 10MS/s asynchronous SAR ADC in 0.18 μm CMOS," in *Proc. 2010 IEEE Symp. VLSI Circuits Symp.*, Jun. 2010, pp. 241–242.

[21] L. Cenkeramaddi and T. Ytterdal, "Analysis and design of a 1V charge sampling readout amplifier in 90 nm CMOS for medical imaging," in *Proc. Int. Symp. VLSI Des., Autom. Test, 2007*, Apr. 2007, pp. 1–4.

[22] S.-Y. Peng, M. Qureshi, P. Hasler, A. Basu, and F. Degertekin, "A charge-based low-power high-SNR capacitive sensing interface circuit," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 55, no. 7, pp. 1863–1872, Aug. 2008.

[23] D. Lemmerhirt, A. Borna, S. Alvar, C. Rich, and O. Kripfgans, "CMUT-in-CMOS 2-D arrays with advanced multiplexing and time-gain control," in *Proc. 2014 IEEE Int. Ultrason. Symp.*, Sep. 2014, pp. 582–586.

[24] K. Chen, H.-S. Lee, A. Chandrakasan, and C. Sodini, "Ultrasonic imaging transceiver design for CMUT: A three-level 30-VPP pulse-shaping pulser with improved efficiency and a noise-optimized receiver," *IEEE J. Solid-State Circuits*, vol. 48, no. 11, pp. 2734–2745, Nov. 2013.

[25] X. Huang, J. H. Cheong, H.-K. Cha, H. Yu, M. Je, and H. Yu, "A high-frequency transimpedance amplifier for CMOS integrated 2-D CMUT array towards 3-D ultrasound imaging," in *Proc. 2013 35th Annu. Int. Conf. IEEE Eng. Med. Biol. Soc.*, Jul. 2013, pp. 101–104.

[26] H. Attarzadeh and T. Ytterdal, "A low-noise variable-gain amplifier for in-probe 3-D imaging applications based on CMUT transducers," in *Proc. 2014 IEEE Comput. Soc. Annu. Symp. VLSI*, Jul. 2014, pp. 256–260.

[27] S. Berg, T. Ytterdal, and A. Ronnekleiv, "Co-optimization of CMUT and receive amplifiers to suppress effects of neighbor coupling between CMUT elements," in *Proc. 2008 IEEE Ultrason. Symp.*, Nov. 2008, pp. 2103–2106.

[28] L. Lewyn, T. Ytterdal, C. Wulff, and K. Martin, "Analog circuit design in nanoscale CMOS technologies," *Proc. IEEE*, vol. 97, no. 10, pp. 1687–1714, Oct. 2009.

[29] C.-H. Hu, X.-C. Xu, J. M. Cannata, J. T. Yen, and K. K. Shung, "Development of a real-time, high-frequency ultrasound digital beamformer for high-frequency linear array transducers," *IEEE Trans. Ultrason., Ferroelect., Freq. Control*, vol. 53, no. 2, pp. 317–323, Feb. 2006.

[30] J. A. Brown and G. R. Lockwood, "A digital beamformer for high-frequency annular arrays," *IEEE Trans. Ultrason., Ferroelect., Freq. Control*, vol. 52, no. 8, pp. 1262–1269, Aug. 2005.

[31] C. Hu, L. Zhang, J. M. Cannata, J. Yen, and K. K. Shung, "Development of a 64 channel ultrasonic high frequency linear array imaging system," *Ultrasonics*, vol. 51, no. 8, pp. 953–959, 2011. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0041624X11000850

[32] K. Kaviani, O. Oralkan, P. Khuri-Yakub, and B. Wooley, "A multichannel pipeline analog-to-digital converter for an integrated 3-D ultrasound imaging system," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1266–1270, Jul. 2003.

[33] K. Chen, H.-S. Lee, A. Chandrakasan, and C. Sodini, "Ultrasonic imaging transceiver design for CMUT: A three-level 30-VPP pulse-shaping pulser with improved efficiency and a noise-optimized receiver," *IEEE J. Solid-State Circuits*, vol. 48, no. 11, pp. 2734–2745, Nov. 2013.

Hourieh Attarzadeh received the M.Sc. degree in electronics from the Sharif University of Technology, Tehran, Iran, in 2011. She is currently working toward the Ph.D. degree in the Department of Electronics and Telecommunication, Norwegian University of Science and Technology, Trondheim, Norway. Her current research interest includes low-power analog and mixed-circuit design for ultrasound probes.

Ye Xu received the B.S. degree from Tongji University, Shanghai, China, in 2007, and the M.S. degree from Royal Institute of Technology, Stockholm, Sweden, in 2009. Since then, she has been working toward the Ph.D. degree in Norwegian University of Science and Technology, Trondheim, Norway, working on energy-efficient analog-to-digital converters. In 2013, she visited the Mixed-signal Microelectronics Group in Eindhoven University of Technology, the Netherlands, as a Guest Researcher. Since 2014, she started working as an analog and mixed-signal circuit Designer in Catena Microelectronics BV., The Netherlands. Her research interests include analog and mixed-signal nanoscale integrated circuit design.

Trond Ytterdal (SM'92) received the M.Sc. and Ph.D. degrees in electrical engineering from the Norwegian Institute of Technology, Trondheim, Norway, in 1990 and 1995, respectively. During 1995–1996, he was employed as a Research Associate in the Department of Electrical Engineering, University of Virginia and during 1996–1997, he worked as a Research Scientist in the Department of Electrical, Computer and Systems Engineering, Rensselaer Polytechnic Institute in Troy, New York, NY, USA. From 1997 to 2001, he worked as a Senior ASIC Designer at Nordic Semiconductor, Trondheim, Norway. Since 2001, he has been on the Faculty of the Norwegian University of Science and Technology, Trondheim, Norway, where he is currently a Professor in the Department of Electronics and Telecommunications. He has authored and coauthored more than 160 scientific papers in international journals and conference proceedings. He is a coauthor of the books *Semiconductor Device Modeling for VLSI* (Prentice-Hall, 1993), *Introduction to Device Modeling and Circuit Simulation* (Wiley, 1998), and *Device Modeling for Analog and RF CMOS Circuit Design* (Wiley, 2003), and has been a contributor to several other books published internationally. He is also a codeveloper of the circuit simulator AIM-Spice. His research interests include design of analog integrated circuits, behavioral modeling, and simulation of mixed-signal systems, modeling of nanoscale transistors, and novel device structures for application in circuit simulators. He is a member of The Norwegian Academy of Technological Sciences.