A 77-GHz Mixed-Mode FMCW Signal Generator Based on Bang-Bang Phase Detector

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***Abstract*—A 77-GHz mixed-mode frequency-modulated continuous-wave (FMCW) signal generator is proposed based on the bang-bang phase detector (BBPD). Instead of employing a linear digital-to-time converter (DTC), a 1-bit 3rd-order single-loop ΔΣ modulator (SLDSM3) and a hybrid finite-impulse response (FIR) filter are utilized to suppress the quantization noise induced by the BBPD. Two-stage infinite-impulse response (IIR) filters are inserted into the digital loop filter (DLF) to reduce the instant variation at output, smoothing the chirp waveform during its generation. To improve the linearity around the turning-around points (TAPs) of the chirp, a type-III slope estimator with switchable polarity is employed. The prototype is implemented in 65-nm CMOS technology, with the total power consumption of 43.1 mW. Measurement results show a 77-GHz carrier with -81.7-dBc/Hz phase noise at 1-MHz offset, as well as a generated triangle chirp that features 1-ms repetition period, 1.827-GHz bandwidth and 336-kHz root-mean-square (RMS) frequency error.**

I. Introduction

The automotive radar system has been witnessed a continuous development for its key role in the realization of autonomous driving. The automotive radar reports the information about the distance and speed of nearby vehicles, which assists for drivers and improves the driving safety. The automotive radar based on the millimeter-wave frequency-modulated continuous-time (FMCW) transceivers has been widely used due to its robustness against various environments and its low peak power characteristic [1]-[2].

As the key block in the transceiver, FMCW signal generator has attracted more attention in recent researches [1]-[4]. The charge-pump based phase-locked loops (PLLs) are typically employed for the FMCW chirp generation [1]-[2]. But it suffers from the limitation on the chirp slope and the large deviation occurred around the turning-around points (TAPs) due to its finite loop bandwidth. An all-digital PLL with two-point modulation (TPM) has been proposed to break the loop bandwidth constraint [3]. However, the wide-tuning-range digitally-controlled oscillator (DCO) needs a complex SRAM-based calibration due to its frequency overlap between two adjacent tuning curves. Replacing the DCO with a current digital-to-analog converter (DAC) and a voltage-controlled oscillator (VCO), the mixed-mode PLL [4] overcomes the overlapping issue. However, the linearity around the TAPs of the chirp is still limited by the loop bandwidth. Both the all-digital PLL and the mixed-mode PLL need a linear time-to-digital converter (TDC), which increases the design complexity.

This paper presents a 77-GHz mixed-mode FMCW signal generator. The bang-band phase detector (BBPD) is employed with a 1-bit 3rd-order single-loop ΔΣ modulator (SLDSM3) and a hybrid finite-impulse response (FIR) filter [5], avoiding the complicated linear TDC or digital-to-time converter (DTC). Two-stage infinite-impulse response (IIR) filters are exploited to smooth the chirp waveform. A type-III chirp slope estimator with switchable polarity [6] is utilized to improve the chirp linearity around the TAPs.

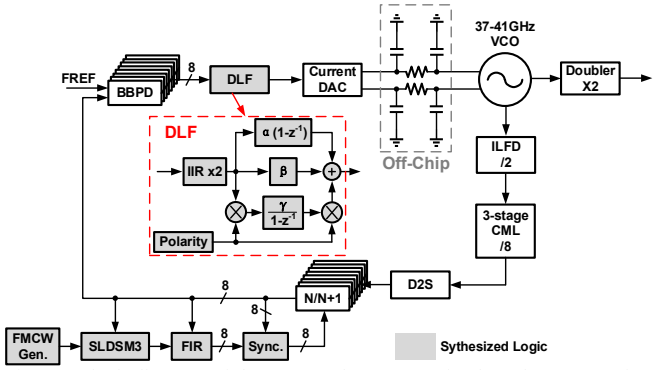

Fig. 1. Block diagram of the proposed 77-GHz mixed-mode FMCW signal generator. The blocks in the grey area are implemented with the synthesized digital logic.

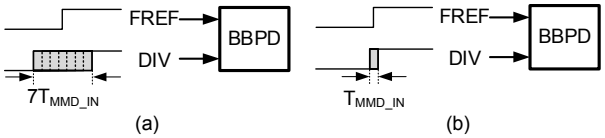

Fig. 2. Dithering range of the DIV signal with (a) 1-1-1 MASH ΔΣ modulator and (b) 1-bit SLDSM3.

II. Proposed 77-GHz Mixed-Mode FMCW Signal Generator

A. Overall Architecture

Fig. 1 shows the block diagram of the proposed 77-GHz mixed-mode FMCW signal generator, in which the frequency doubling architecture [1] is utilized, with a VCO running around 38.5 GHz. The lowered center frequency relaxes the design of the VCO as well as the frequency divider. The output of the VCO is divided by 16 with an injection-locked frequency divider (ILFD) and 3-stage current-mode logic (CML) frequency dividers. The followed multi-modulus divider (MMD) and BBPD array enables a hybrid FIR filtering, which mitigates the phase folding problem caused by the BBPD [5]. A 1-bit SLDSM3 is employed, instead of 1-1-1 MASH ΔΣ modulator, to reduce the quantization noise of the BBPD [5]. The 4th-order digital loop filter (DLF) (Fig. 1) consists of

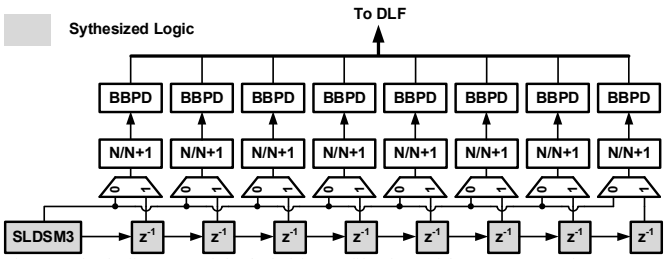

Fig. 3. Block diagram of the hybrid FIR filtering with 8 MMDs and 8 BBPDs.

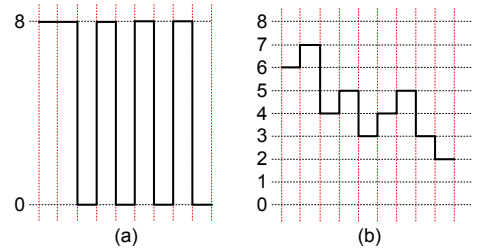

Fig. 4. Output of the 8 BBPDs with the hybrid FIR (a) turned off and (b) turned on.

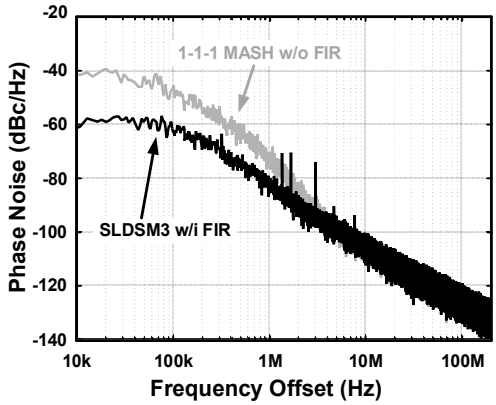

Fig. 5. Simulated phase noise at 77.531 GHz.

2 stages of IIR filters and a type-III 2nd-order loop filter, including a proportional path, an integral path and a chirp slope estimator [6]. In order to reduce the bit number of the current DAC, one of the accumulator in the DLF is moved towards the output of the differential DAC, turning into two capacitors as the analog integrator [4]. A differential RC filter between the analog integrator and the VCO provides anti-aliasing filtering for the current DAC.

B. Quantization Noise Reduction for BBPD

The larger the root-mean-square (RMS) jitter referred to the BBPD's input is, the larger the quantization noise of the BBPD would be [7]. According to the linearized gain expression of the BBPD [7]:

$$K_{BBPD} = \sqrt{\frac{2}{\pi}} \cdot \frac{1}{\sigma_{\Delta t}}, \qquad (1)$$

a larger RMS input jitter corresponds to a smaller linearized gain for the BBPD. Typically, a phase interpolator (PI) or a DTC is needed to reduce the input jitter of the BBPD [8]-[9]. However, the demand of a linear PI or DTC would increase the design complexity dramatically. Alternatively, the 1-bit SLDSM3 and hybrid FIR filtering, are employed in this work to reduce the quantization noise from the BBPD [5].

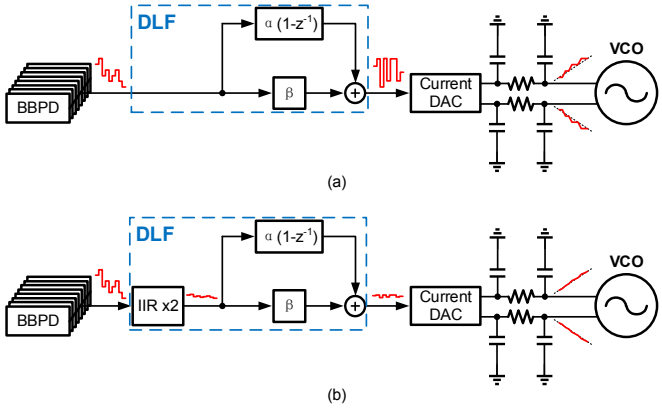

Fig. 6. Chirp generation (a) without IIR filtering and (b) with IIR filtering.

Generally, a 1-1-1 MASH ΔΣ modulator is used to realize a fractional-N frequency synthesizing. Nevertheless, its large dithering output range degrades the noise performance of the BBPD. Fig. 2 compares the dithering range of the DIV signal with 1-1-1 MASH and 1-bit SLDSM3. The 1-bit SLDSM3 provides a smaller RMS input jitter for the BBPD, which in turn suppresses the quantization noise. Furthermore, the 3rd-order loop in the 1-bit SLDSM3 guarantees a good spur performance [5].

Fig. 3 shows the block diagram of the 8-tap hybrid FIR filtering, which is composed of 8 flip-flops, 8 MMDs and 8 BBPDs. To show the effect of the hybrid FIR clearly, the BBPDs' output is evaluated when the hybrid FIR is turned on and off, respectively (Fig. 4). To perform a fair comparison, there are still 8 MMDs and 8 BBPDs but working with the same division ratio when the hybrid FIR is turned off. It is shown that, the output of the 8 BBPDs is switching between 0 and 8 with the hybrid FIR off. If the hybrid FIR is turned on, the cancellation of the deterministic phase error will be performed between the 8 paths. As a result, the output can be an arbitrary integer from 0 to 8, similar to a multi-bit TDC. Then the output dithering amplitude is decreased, which means an effectively enhanced resolution of the phase detecting.

To verify the improvement achieved by the 1-bit SLDSM3 and the hybrid FIR, a behavioral simulation based on MATLAB and Simulink is performed. The Fig. 5 compares the simulated phase noise between the 1-1-1 MASH without FIR and the 1-bit SLDSM3 with FIR. It turns out that the 1-bit SLDSM3 and hybrid FIR help to achieve 20-dB better in-band phase noise, and the loop bandwidth is about 3 times larger than that with the 1-1-1 MASH and FIR turned off. Simulation results coincide with the gain expression and the conclusions about the quantization noise of the BBPD.

C. Chirp Waveform Smoothing with IIR

In the typical DLF design, only a proportional path and an integral path are included for low complexity [5]. However, it is far from enough for the FMCW chirp generation. During the frequency chirp generation, the input tuning voltage of the VCO should vary linearly if we ignore the nonlinearity of the VCO. With the current DAC and analog integrator placed in front of the VCO, the DLF's output represents the chirp slope. Fig. 6(a) shows the situation that a typical DLF is employed in the FMCW generator. The output of the DLF exhibits a large instant

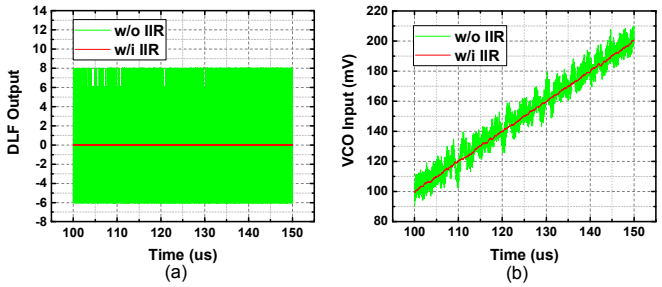

Fig. 7. Simulated transient waveforms of (a) the DLF's output and (b) the VCO's input.

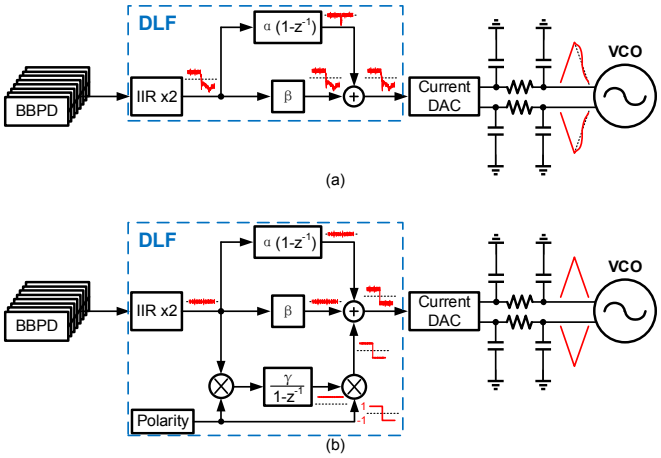

Fig. 8. Chirp generation around the TAPs (a) without the chirp slope estimator and (b) with the chirp slope estimator.

variation with the time-averaged value equal to the chirp slope. The chirp linearity will be heavily degraded with the large slope variation. In the proposed architecture, 2-stage IIR filters are inserted prior to the typical DLF in order to suppress the slope variation, as shown in Fig. 6(b). With the help of 2-stage IIR filtering, the output variation of the DLF is greatly reduced, achieving improved chirp linearity.

To verify the improvement brought by the IIR filtering, the behavioral simulation is performed with α=1 and β=2^{-7}. The poles of the two IIR filters are both set around 1 MHz to balance between the phase margin and the filtering strength. Behavioral simulation results exhibit a significant reduction in the instant frequency error of the chirp with the IIR filtering (Fig. 7).

D. Linearity Enhancement Around TAPs

The polarity of the chirp slope needs to be switched at the TAPs. In conventional FMCW generators, the instant switching of the polarity is accomplished by the loop dynamics [1]-[2], [4]. However, the switching speed is limited by the loop bandwidth. Furthermore, in the BBPD-based architecture, the loop dynamics is slowed down due to the limited output level (only "0" or "1") of the BBPD. As a result, the frequency overshooting occurs at the TAPs (Fig. 8(a)), degrading the chirp linearity. In the proposed architecture, a type-III chirp slope estimator is employed with polarity alternating capability [6], as shown in Fig 8(b), providing an adaptively-estimated chirp slope against the nonlinearity and enabling a fast polarity switching at the TAPs.

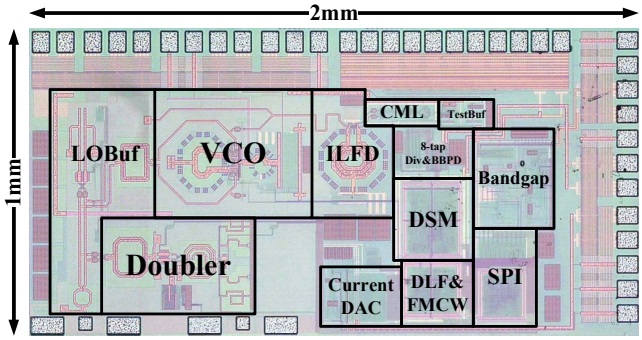

Fig. 9. Chip microphotograph of the FMCW signal generator.

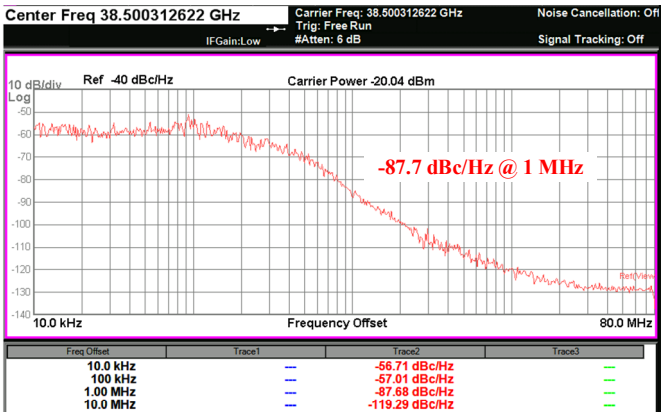

Fig. 10. Phase noise measured at the output of the VCO.

E. VCO and Frequency Doubler

A differential cross-coupled LC oscillator is employed in the proposed architecture to generate oscillating signal around 38.5 GHz. The 2.5-V differentially-tuned varactors enable 1.7-GHz tuning range within one single tuning curve. The total tuning range provided by the 2-bit capacitor array covers 37-41 GHz, with an enough overlap between the adjacent tuning curves to guarantee the continuous frequency tuning across the whole range. Tail inductor filtering and RC filtering are utilized to prevent noise injection from the tail bias.

An injection-locked frequency doubler [1] is utilized to generate 77-GHz oscillation. The 2nd-order harmonic current generated by the push-push pair is injected into the top of a coupled resonator. The free-running frequency of the coupled resonator can be adjusted from 74 GHz to 82 GHz with 5-bit digitally-controlled artificial dielectric (DiCAD) transmission lines. The input bias voltage of the push-push pair is optimized to generate the strongest 2nd-order harmonic current.

III. Measurement Results

The proposed 77-GHz mixed-mode FMCW signal generator is implemented in 65-nm CMOS technology. The chip microphotograph is shown in Fig. 9, occupying an area of 2 mm^2 with the testing pads. A 2.5-V supply voltage is applied to the current DAC and bandgap with the remain circuits working under a 1-V power supply. The total power consumption is 43.1 mW, excluding the testing buffer. The VCO and the frequency doubler draw 10.5 mA and 14.9 mA from a 1-V power supply, respectively.

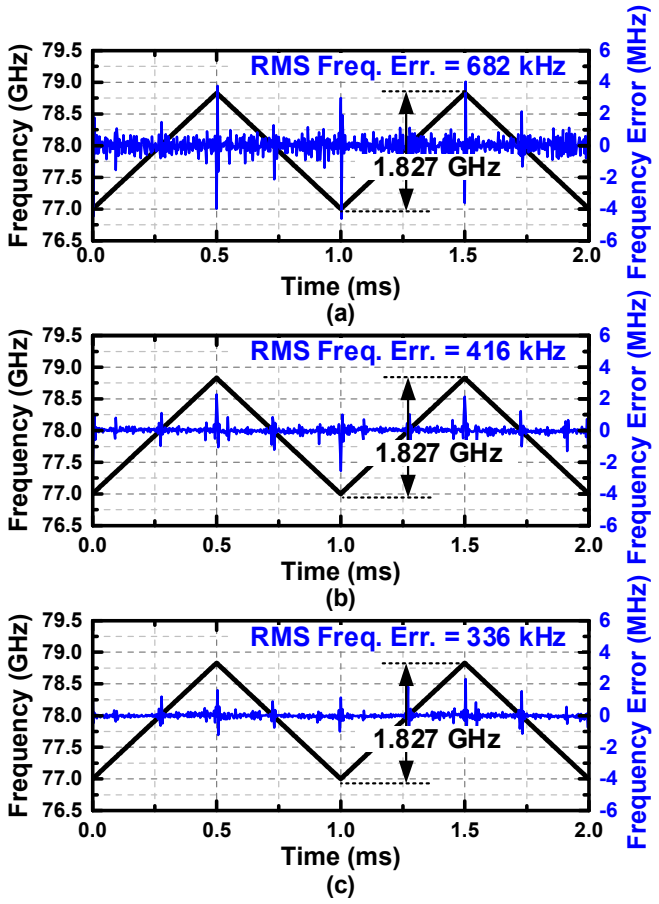

Fig. 11. Measured FMCW chirp signal and the frequency error with the period of 1 ms and the bandwidth of 1.827 GHz under three different modes: (a) with the 1-1-1 MASH, (b) with the 1-bit SLDSM3 and hybrid FIR, (c) with the 1-bit SLDSM3, hybrid FIR and type-III chirp slope estimator.

Fig. 10 shows the phase noise measured at the VCO's output with Keysight N9030A, revealing a phase noise of -87.7 dBc/Hz at 1-MHz offset. The FMCW chirp signal is measured at the 1/16 frequency prescaled output of the VCO, the frequency of which is around 2.4 GHz. The RF output is sampled by Keysight MSOV334A and demodulated with Keysight 89601B, which is multiplied by 32 to get the FMCW chirp signal and the frequency error. Fig. 11 shows the measurement results of three different modes when the period is set as 1 ms with the bandwidth of 1.827 GHz. The RMS frequency error (including the TAPs) is 682 kHz when the 1-1-1 MASH is utilized, which is improved to 416 kHz by replacing the 1-1-1 MASH with the 1-bit SLDSM3 and turning on the hybrid FIR. It is further reduced to 336 kHz with the type-III chirp slope estimator.

Table I summarizes the performance of the proposed FMCW signal generator and makes a comparison with the previously published works.

IV. Conclusion

A 77-GHz mixed-mode FMCW signal generator based on BBPD is proposed in this paper. 1-bit SLDSM3 and hybrid FIR filter are utilized to reduce the in-band phase noise, which is dominant by the quantization noise of the BBPD. 2-stage IIR filters are inserted in the DLF to smooth the chirp waveform.

TABLE I. Performance Summary and Comparison with State-of-the-Art FMCW Signal Generator

	This Work	[1]	[2]	[3]
Function	**FMCW Sig. Gen.**	TRX	TX	TX
FMCW Freq. (GHz)	**77-78.827**	76.92-78.85	77-77.31	61.6-62.6
BW/T_{mod} (GHz/ms)	**1.827/1**	1.93/2	0.312/2	1/0.42
RMS Freq. Err. (kHz)	**336** *	674	961 *	384
PN @ 1 MHz (dBc/Hz) **	**-81.7**	-81	-83.4	-90
Power (mW)	**43.1**	343	320	89
Area (mm^2)	**2**	4.64	2.74	2.2
Technology (nm)	**65**	65	65	65

* Including the turning-around points

** Estimated from lower frequency

A type-III chirp slope estimator with switchable polarity is employed to reduce the frequency error around the TAPs. The proposed FMCW signal generator is implemented in 65-nm CMOS technology with the total power consumption of 43.1 mW. The measured RMS frequency error is 336 kHz when the chirp's period is 1 ms and the bandwidth is 1.827 GHz.

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