A 16-bit Resistor String DAC with Full-Calibration at Final Test

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Abstract:
A novel, on-chip transfer function calibration scheme is introduced to the classical resistor string DAC architecture. A 16-bit, quad channel, resistor string DAC with exceptional accuracy is fabricated on an ultra-low-cost, 0.5μm, 5V CMOS process. Monotonicity is achieved by voltage interpolation and absolute accuracy errors are improved by 100X using full transfer function calibration at final test. An on-chip arithmetic logic unit (ALU) linearly interpolates calibration coefficients saving memory, and a high-effective-resolution cal-DAC preserves differential linearity (DNL) performance while correcting integral linearity errors. Separate cal-DACs correct for offset and gain errors. Each DAC channel occupies 4mm2 die area, consumes 750uA, and settles in 10μs, while offering up to +/- 500μV absolute accuracy across its transfer curve. The chip has built-in DFT and uses one time programmable memory with read-back. The device can be calibrated and tested with a single insertion at final test. This paper discusses the architecture, testing, calibration and optimization details.
Index Terms: Data converters, DAC calibration, DAC testing

1. Introduction

Resistor ladders have been traditionally used in digital to analog converters (DACs) [1], [2]. Two major resistor ladder architectures are current division using R-2R type of ladders (R-2R DACs) and voltage division using series resistor ladders (string DACs). Building such structures at 8 to 10 bit level has been common engineering practice in many IC designs. 12 bit structures are possible but require careful layout techniques. For structures 14 bits and above, either on-chip calibration or laser trimming at probe becomes necessary to overcome the inherent problem of resistor matching [3], [4].

Many industrial D/A converter designs have traditionally used processes with thin film resistors, and the segmented R-2R ladder architecture [3], [4]. Above 12 bits of resolution, such architectures can achieve monotonicity and good linearity with laser trimming at wafer probe. 16-bit D/A converters using segmented R-2R architectures are widely available but they are extremely expensive due to the cost of laser trimming, thin-film process technology, yield loss due to package shift and dual insertion testing at wafer probe and final test [5].

The D/A converter described in this paper is of series resistor ladder type. Series resistor ladder architectures (string-DACs) have historically been used in FLASH type A/D converters [6] and low bit-count, low cost D/A converters. Due to area constraints, they have not exceeded 10 to 12 bits of resolution [7], [8] and due to the need for trimming a large unary array of resistors, laser trim is rarely attempted, except for a few isolated cases where the string consists of only a few resistors [9]. To reduce area, nested resistor string architectures have been proposed [10], [11], but the success has been limited due to either the secondary string loading the primary string, or due to switch resistance between resistor strings causing large differential nonlinearity (DNL) errors. More recent advances in voltage interpolation topology [12], [13], [14], solved the problem of monotonicity, and families of very low cost, 16-bit monotonic string-DACs emerged during the last few years. Process matching and good layout techniques are used for reducing integral nonlinearity (INL). Such converters had differential linearity almost at 18-bit level however; their integral linearity hardly exceeded 10-11 bits [15], [16]. With respect to their R-2R counterparts, these string DACs offered the advantages of monotonicity, lower cost, smaller size, lower power, and lower glitch energy, and they did not cause code dependent loading for the external reference voltage generator. Nevertheless, the problem of improving the string-DAC integral linearity error remained [18], and standard laser trim methods could not be used due to the high number of resistors to be trimmed.

To achieve string-DAC INL performance improvement at the system level, piece-wise linear, *all-digital* calibration techniques are used by system designers. Other than a measurement setup, a microcontroller for evaluating piece-wise linear (PWL) arithmetic is required together with a memory structure to store the PWL coefficients. The need for digital division can be removed, and accumulation of the coefficient errors can be avoided by interpolating equi-distant voltages instead of equi-distant codes [17]. However, the problem of all digital calibration is the loss of resolution (DNL) to improve linearity (INL). Since the step size never falls negative, one can argue that all-digital calibration is monotonic, but DNL errors approaching +2 Least Significant Bits (LSBs) cannot be avoided, and a lot of values at –1 LSB can be encountered. In all digital calibration, the DAC is used to correct itself. To summarize, with all-digital calibration, by approximately doubling DNL errors, it is possible to achieve significant improvement of INL errors, provided that sufficient memory is available (See Figures 1, 2 and 3). However, for

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many small-signal applications, DNL is of primary concern and the DNL/INL trade-off is not desirable. The *all-digital* method we described can also be called a *"software"* calibration, since the DAC calibrates itself under the control of external software.

Other than multiple components on a printed circuit board, another applicable setting for all-digital string DAC calibration is multi-chip modules (MCMs), where a low performance string DAC is packaged with a microcontroller and FLASH memory, to be calibrated at final test. MCM packaging costs are prohibitive for most applications.

Figure 1 shows the basic form of all-digital, "software" calibration setup. The lookup table will be filled during system test, after a precision digitizer measures the linearity errors of the nonlinear string DAC. Figure 2 shows the geometry behind equation 1 that implements the calibration. Figure 3a shows the integral "random walk" linearity pattern from a real, 16-bit, un-calibrated string DAC. Figure 3b shows the DAC's monotonicity and low DNL errors of the same DAC. Figure 3c shows a 256 segment piece-wise linear "software" calibration of the same DAC shown in Figure 3a. Figure 3d shows the deterioration of the differential linearity after *software* calibration.

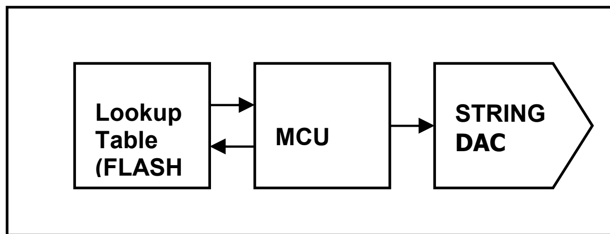

Figure 1. All digital, off-chip (software) calibration setup

A most basic form of such a software calibration algorithm implemented by the MCU is as follows (Better on-chip implementations exist [17]):

- V1x voltages are measured and stored in external memory (FLASH).
- The segment that generates the D0 voltage is first searched in memory and then found by the MCU
- Equation 1 is computed to find the DAC code I0.

$$I0 = I1 + (I2-I1)(D0-VI1)/(VI2-VI1), \qquad \text{Eq. 1}$$

where

D0: Desired voltage.
D0B: Main DAC voltage approximating D0 after PWL calibration
I0: Main-DAC code generating an approximation to the desired voltage
I0B: Main-DAC code generating the desired voltage
I1: Bottom main-DAC code generating the PWL segment that contains D0 voltage
I2: Top main-DAC code generating the PWL segment that contains D0 voltage
VI1: The main DAC voltage for the bottom main-DAC code that generates the PWL segment containing the D0 voltage.

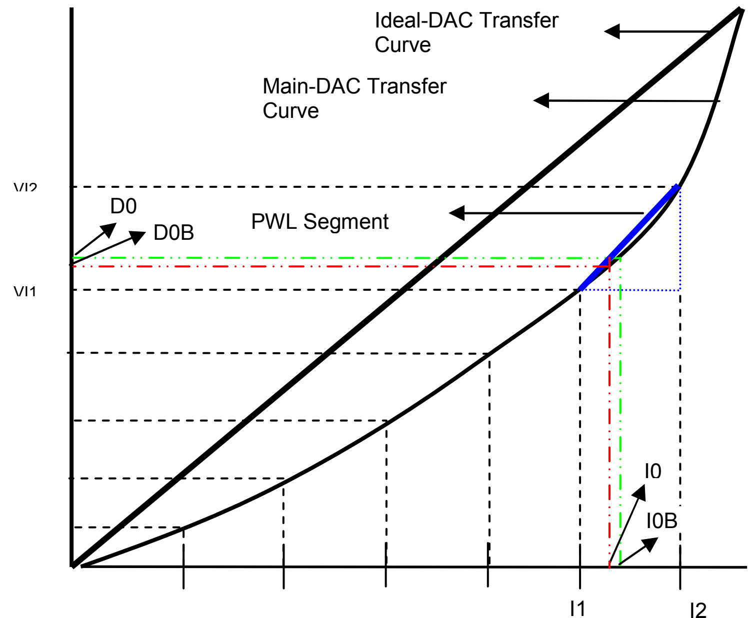

Figure 2. Approximation used in *software* calibration

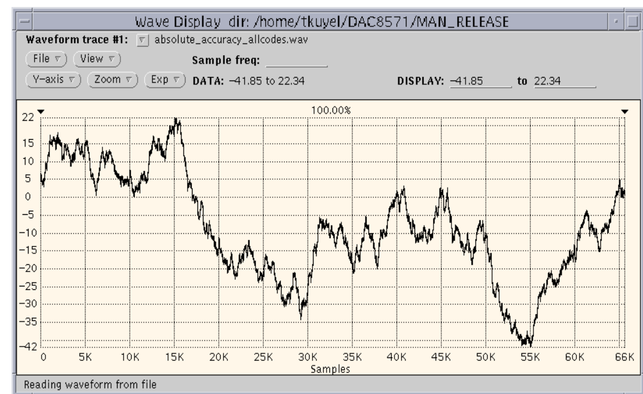

Figure 3a. Uncalibrated, 16-bit, String DAC INL (LSB vs. Input Code)

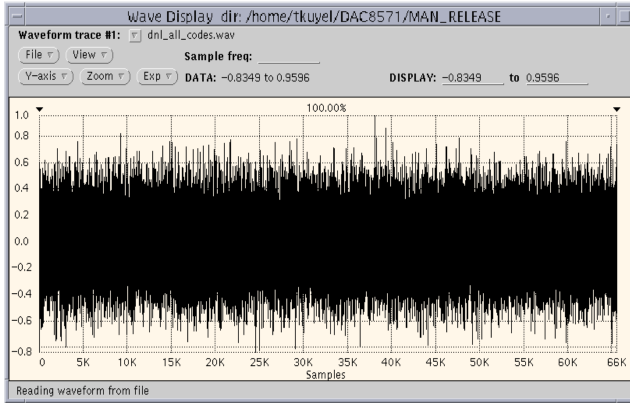

Figure 3b. Uncalibrated, 16-bit, String DAC DNL (LSB vs. Input Code)

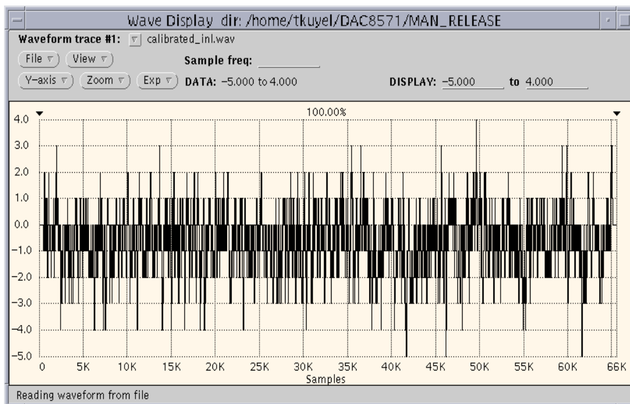

Figure 3c. Software calibrated INL (256-segments). Improved by ~10X

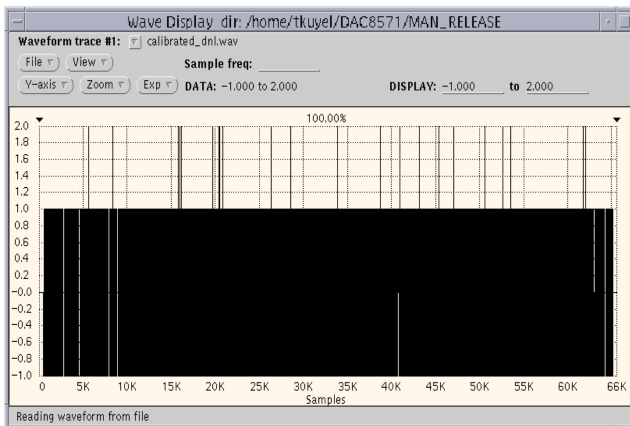

Figure 3d. DNL after software calibration, worsened by >2X.

The performance of all piece-wise linear calibration schemes depends on the number of segments used. The accuracy of the calibration improves as the number of segments increase. In the extreme case, the PWL calibration reduces to a single lookup table search. However, for a 16-bit DAC, a single lookup table would require 65536 bytes of storage, which is not cost effective. Piece-wise linear methods reduce the memory requirements at the expense of some accuracy and combinatorial logic complexity. The effect of the PWL calibration on INL is determined not by the absolute value of the initial INL error, but by the spatial frequency components of the INL error. If the INL error contains higher spatial frequencies than the half the number of segments, calibration becomes less effective. Low frequency components of the INL error are calibrated with ease.

This paper discusses the design, testing and calibration of an in-package trimmed, 16-bit, voltage output, quad channel string DAC, a first in the industry. The scope of this work is limited to DC accuracy errors: INL errors are significantly improved without sacrificing DNL errors. Up to +/- 0.5 mV absolute accuracy can be achieved across the transfer curve. The D/A converter is built using an ultra-low-cost 5V CMOS process, with low production cost including testing. Single insertion testing at final test facilitates high-volume production, eliminating the need for laser trim and probe, as well as eliminating the need for exotic thin film processes. The cal-dac is scaled to achieve 19-bits of effective resolution consuming only 100uA of power. The chip consumes 750uA per channel and settles in 10 microseconds. Design for test is implemented to verify the memory structure, arithmetic logic unit and the cal-DAC.

2. Chip Architecture

It is actually possible to improve the INL errors without significantly deteriorating DNL errors. The approach we took to improve string-DAC linearity is to include a monolithic, *mixed signal* solution where piece-wise linear arithmetic is used to load a calibration DAC (cal-DAC). A high-resolution calibration cal-DAC should be used to correct for transfer function errors. This enables fine error correction steps so that DNL performance is preserved while INL performance is improved. This approach still needs a memory block and an arithmetic logic block to load the computed codes to the cal-DAC, as seen in Figure 4.

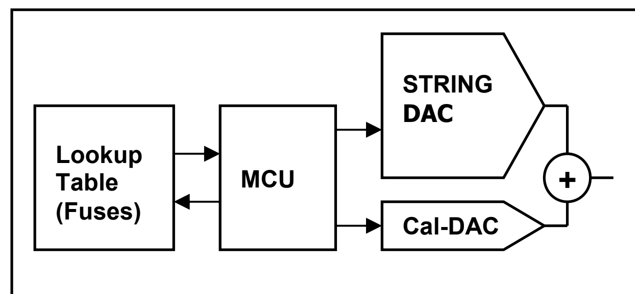

Figure 4. Inclusion of a high-resolution Cal-DAC to address the DNL

For most modern process technologies, the complexity of implementing an on-chip microcontroller is insignificant in

comparison with die area savings due to reduced amount of storage. Also implementing the chip with electrical fuses on a low cost CMOS process instead of a FLASH process can save significant cost up to a certain number of fuses. A FLASH process typically adds 30-40% to die cost. For the FLASH memory to be cost effective, the memory block should cover more than 30-40% of the total die area. This is without including the probe test cost for the FLASH memory.

2.1 Analog Subsection

The architecture of the chip is shown in Figure 5. For simplicity, a known-good, 16-bit string DAC layout is used to implement the main-DAC, and a known-good, 12-bit string DAC layout is used for implementing the cal-DAC. The voltage summation is implemented using a V-to-I current mirror forcing current onto a resistor, using a temperature independent circuit topology. The same topology also tracks the chip's external reference voltage, making the INL calibration not only temperature independent, but also reference voltage independent. This works really well on string DACs, since the INL waveform (as a percentage of full-scale), does not change with the reference voltage. Extensive care is taken to ensure the stability of the cal-dac combined with the V-to-I converter. The 12-bit INL cal-dac is scaled down to 19 bits of effective resolution in multiple stages, including the cal-dac, V-to-I converter and the output buffer. After 7-bit scaling is complete, the transfer function errors of the INL cal-dac itself become totally insignificant (divided by 128). Separate cal-dacs for offset and gain calibration are also included, in order to preserve INL calibration resolution.

2.2 Arithmetic Logic Unit

On the digital side, the arithmetic logic unit word length is optimized for the minimum circuit size that can perform the arithmetic without loss of resolution. The ALU includes a 14 by 8 multiplier, a 14-bit subtractor, and an 8-bit adder, and it generates a 12-bit result for the cal-DAC. ALU word lengths are optimized together with the cal-dac step size, so that each calibration increment does not exceed 1/8 main-DAC LSB. This preserves DNL, while saving die area. The chip has quad voltage outputs. To save further die area, the ALU is shared between the 4 channels of the chip. The chip also uses double registered inputs, for both the main-DAC and the cal-dac of each channel. Double registering makes it possible to multiplex the ALU to write into the temporary registers of each channel serially, before all channels are updated simultaneously from the previously stored temporary registers. This enables one ALU to serve 4 channels, serially loading the calibration coefficients into the INL cal-dac of each channel. All DAC decoders and register banks are grouped with their respective analog circuits to facilitate layout.

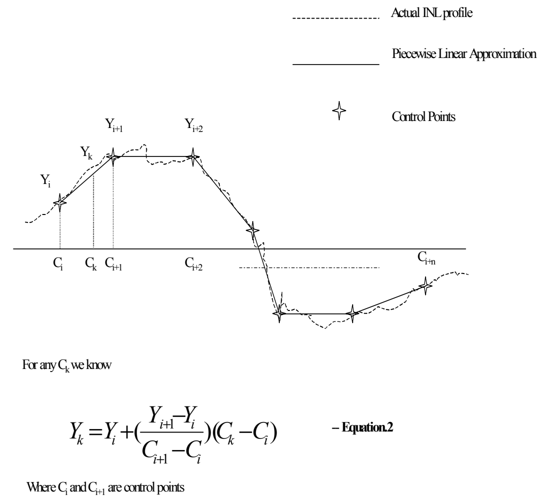

Figure 5. 32-segment PWL approximation, performed by the input data, the memory block and the ALU.

The geometry and the mathematics behind the calibration implementation is shown in Figure 5 and equation 2. The 33 control points, Ci, are input code indexes for the INL readings Yi. Ck is the input code and Yk is the 12-bit input for the Cal-dac. Note that since the control points are equally spaced at 2048 code intervals, the division can be implemented as arithmetic right-shift. There are 32 segments and 33 control points for each DAC channel. 32 segments are found to be optimal to provide sufficient accuracy without increasing the die cost outside the design targets. Depending on the input data, two consecutive control points are fetched from the memory and are loaded into the ALU to generate an input code for the 12-bit INL Cal-DAC. Such architectures preserve DNL because calibration step size can be made arbitrarily small.

2.3 One Time Programmable Memory

To reduce wafer cost, arrays of electrical fuses are used instead of FLASH memory. +/- 0.5mV absolute accuracy target is not only limited by the linearity errors but also by the offset and gain temperature drifts. Therefore, for a drift limited design, reduction of the INL from 64 LSB to 8 LSB is seen as sufficient. Judging from the earlier data, 32 segment PWL calibration is found necessary to achieve 8 LSB typical INL error. 8 LSB INL performance can be obtained at a lower cost by implementing a fuse array instead of FLASH memory. 8 LSB INL target also enables the quantization of each PWL control point with 7 fuses with some margin for calibration range. The quantization of each control point creates not more than 1 LSB of INL discrepancy. An 8th fuse is included for each control point (can be a parity fuse). A 32-segment fuse block therefore uses 33 8-bit fuses for each channel. 1056 total fuses are

therefore used for the linearity memory block. Because of the fuse count, efficient fuse layout becomes key (See Figure 10). The fuse layout includes X-Y memory decoding. To save die area, latches instead of the registers are used at each fuse block to read the fuse state. During regular operation the chip simultaneously reads from two banks of fuses (lower control point and upper control point), one channel at a time. Therefore, at any time, 16-bits of fuse data are read at once, including two unused fuse bits. 66 fuse rows and 16 fuse columns are used, however the rectangular shape of each individual fuse layout makes a square shaped fuse array. After the latches are enabled for the selected fuse banks, a 16-bit fuse output register is loaded. Specific care is taken to ensure enough current can be routed to blow each fuse in the fuse matrix. The fuse block has its own separate supply and ground pins. The fuse decoders ensure the alternation of the same control point from an upper control point to a lower control point during a consecutive segment change. Each channel also has a separate 8-bit fuse bank for offset and an 8-bit fuse bank for gain. The chip also has a master fuse, disabling all fuse programming once blown. The total fuse count is 1121. This One Time Programmable (OTP) memory block, (fuse block) consumes approximately 40% of the total die area.

2.4 Read-back Block

Working with the control logic, a flexible read-back block coordinates all the design-for test features of the design. Readback will be explained in the next section. The control unit decodes the 24-bit frame received by the serial interface and coordinates channel selection, update modes, memory read/write, calibration value test and the read-back operation. Figure 6 shows the main architectural blocks of the DAC. The read-back block is distributed and is shown as back-arrows.

2.5 Offset and Gain Correction

Figure 6 shows trimmable offset and gain errors in addition to linearity calibration. Trimming of offset and gain errors is actually implemented by additional cal-DACs, and the trim coefficients are loaded from separate memory blocks. In actual implementation, the memory for offset and gain correction are different from the memory for linearity correction. The memory for offset and gain correction needs to be read only once at power-up. However, the memory for linearity correction is read each sample, depending on the input code received for each channel. For these reasons, the memory for offset and gain are kept separate from the linearity memory block. Offset and gain memory and Cal-DACs are not included in Figure 6 for simplicity. The reason for having separate offset and gain Cal-DACs is resolution. Maximum INL error is +/- 5mV, however, the maximum offset error could be +/- 20mV and maximum gain error could reach +/- 75 mV. Having the INL Cal-DAC correct for offset/gain/INL would have meant a significant loss of resolution given a fixed number of fuses.

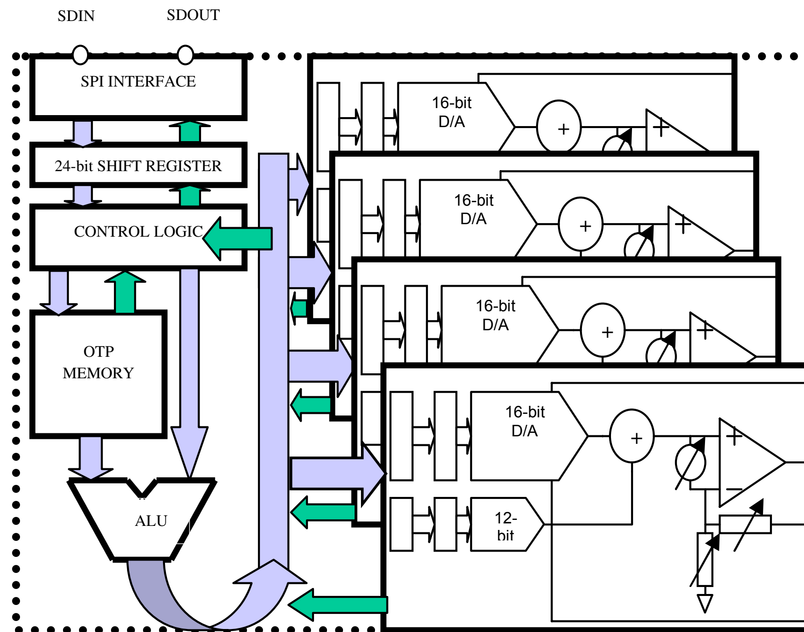

Figure 6. Quad channel D/A converter architecture with calibration

3.0 Design for Testability

The high number of fuses and the complexity of the DAC architecture require design for testability. The DAC has a 3-wire serial interface, serial data input (SDIN), serial clock input (SCLK), and frame synchronization input (FSYNC). A serial data output (SDO) pin is added to enable read-back using the serial interface. The read-back block takes up some die area including routing, but it is very flexible. The read-back has the functionality for the end user to read-back DAC data from each channel. This allows one user process to write into the chip at full speed, while another user process to intermittently check at a slower serial speed whether the data is written correctly. Such verification is useful to check data integrity when the serial bus is loaded with different devices. A control word sent through the serial interface determines the functionality of the read-back. For factory use, the read-back block can multiplex between the temporary register and the DAC register, between channels and between main DAC input and cal-dac inputs:

Read-back from

- temporary register tests the serial interface
- DAC register tests update clock timing
- 16-bit INL fuse register tests the fuse block, 2 fuse bytes at a time

- temporary cal-dac register tests the ALU (after it was loaded with different values under factory control)
- offset/gain registers tests the fuses allocated for offset/gain

SCAN is not used since the only significant state machine is the serial interface itself. The rest of the registers are parallel registers and the read-back block can check them effectively. Our read-back functionality can be considered as a simple form of SCAN.

So far we described the DFT features that could test the digital functionality including the memory block. However, the DFT features of the design also include analog DFT. The memory programming and read-back allows for a number of tests (that were not possible before) to become possible. With one-time-programmable on-chip memory, temperature drift testing of offset and gain errors can be accomplished with guaranteed specifications.

The chip has 136 bits of idle fuses accessible through read-back. These idle fuses are used for storing:

- parity check for the overall chip (1 fuse)
- parity check for blocks of 32 fuses (32 fuses)
- date for final test (9 fuses)
- device serial number (24 fuses)
- offset error, offset drift coefficients (32 fuses)
- gain error, gain drift coefficients (32 fuses)
- reserved (6 fuses)

This data is available to the factory and part of it is available for the end user, providing valuable information regarding when the device was tested, how much it drifts over temperature, and whether something went wrong with the memory block during the life-time of the product. The end user can poll a single parity bit to see if the fuse block has an error, and the factory can further zoom into where that error occurred. The factory can also trace each device to its original final test data in case of an unlikely customer return.

DFT using memory and read-back enables minimum and maximum datasheet specifications for offset drift and gain drift. Proprietary techniques based on two-temperature testing and on-chip memory calibrate drift. Reasonably linear drift characteristics (0C to 70C) of the device allow two-temperature testing for drift. Drift calibration, which is enabled by DFT, improves the absolute accuracy to within 1mV across the operating temperature range. The capability to store and read-back offset and gain errors at a certain temperature enables even tighter drift specifications, with high-drift devices being screened during production. Two-temperature, multi-insertion testing does not add much test cost as long as the only tests performed at high temperature are offset and gain tests.

4.0 Final Test

The following sections discuss the development of the full test solution.

4.1 Test Hardware

Testing a 16-bit precision D/A converter requires attention to detail. An advanced mixed signal tester platform is chosen for test capability. An 8.5 digit precision multi-meter is used for various board level calibrations and also for the measurements of offset and gain. The multi-meter is phase locked to the line cycle in order to eliminate 60Hz coupling to the results. For faster production testing, linearity is tested by a quad-channel delta-sigma digitizer. A 4-site test board is designed with high precision OP-AMPS and shielded relays. A single ground plane is used for the entire board to lower inductive coupling. Supply, reference and ground planes are stacked together on the board to work as high Q capacitors. Multiple calibration paths are included on the board to provide board self-test. Finally, a high performance contactor is used to improve contact resistance at each insertion improving the accuracy of the offset test. Each chip uses a 40-lead 6mm x 6mm package, including pins for analog and digital flexibility. To route all 4-sites effectively without affecting analog performance, a 22-layer PCB was used.

4.2 Linearity Test Algorithm Before Calibration

String DACs can be very costly to test since each resistor voltage needs to be measured. Testing a 16-bit resistor ladder would take 65536 readings. This is not possible with a precision multi-meter locked to the line cycle, as it takes a minimum of 18 minutes to complete the test, per DAC channel. Our 16-bit Main DAC uses a segmented, inherently monotonic architecture as shown in Figure 7. This is exploited during testing to reduce test time.

The use of a programmable delta sigma digitizer found in many high-end mixed signal test systems can speed-up testing without sacrificing test coverage. However, one needs to be very careful setting up the digitizer. The analog anti-aliasing filter and the digital decimation filter of the delta-sigma digitizer can filter the fast varying DNL errors of the DAC, if the measurement is taken too fast. INL will be deceivingly correct, or close to correct, whereas DNL will be grossly incorrect. If enough waiting time is inserted to avoid the filtering effect, then the test time can be prohibitively long, in the order of minutes. The best approach is to use a segmented testing that mimics the segmented architecture of the main DAC. The INL specification is 8 LSBs, 8X the DNL specification. Therefore, different speed versus accuracy trade-offs could be performed for testing INL and DNL. A capable test solution requires 3-sigma measurement error to be 0.1 LSB for DNL and 0.8 LSB for INL. This difference can be exploited. We program the input low-pass filter, modulator sampling rate, and the digital decimation filter parameters of our digitizer such that accurate DNL data is

captured from the fine DAC over a single resistor. This also enables the digitizer to be setup to use its full range over a single resistor voltage. The DNL measurement for a single tap can be taken within one second of test time, without inducing any adverse filtering effects on the DNL. Once this measurement is complete, data is stored and the digitizer is reprogrammed to take less accurate but faster measurements. This second digitizer setting is used for measuring each string tap voltage. After the tap voltages are measured, the DNL data is "stretched" according to each two tap voltages across a resistor, and the full-codes transfer curve of the entire DAC is synthesized in software from the two sets of data. Finally, INL and DNL of each DAC channel are computed from the full-codes transfer curve, using the well-known set of end-point linearity test equations:

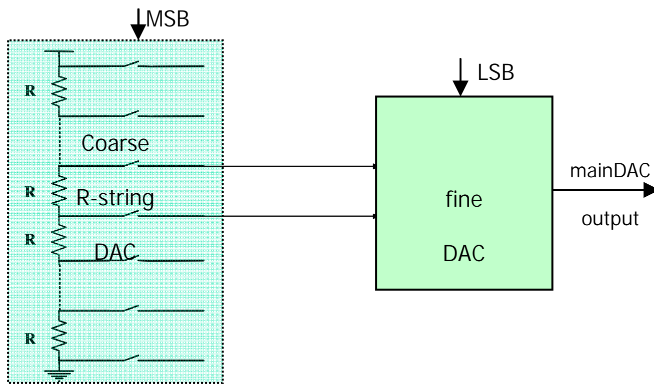

Figure 7. Main DAC architecture

$$V_{IDEAL_LSB} = (V_{65535} - V_0) / 65535$$

$$V_{IDEAL_RAMP}[k] = V_0 + k * V_{IDEAL_LSB}$$

$$INL[k] = (V[k] - V_{IDEAL_RAMP}[k]) / V_{IDEAL_LSB}$$

$$DNL[k] = INL[k+1] - INL[k]$$

The implementation of this test algorithm takes under one second for a single DAC channel. Assuming 4-site operation and 4-channels per chip, testing the full-chip for linearity takes under 1 second. This provides accurate linearity testing that correlates well with multi-meter measurements, with dramatic test time reductions.

To make sure that the decoders and the switches between the coarse DAC and fine DAC are functional, a very fast, selected codes testing is additionally performed to screen for digital faults.

4.3 Calibration Algorithms

Given fixed number of control points (33), the simplest form of calibration algorithm is one that nulls the INL at the control points. The chip has the DFT feature of verifying how well the calibration value performs before actually blowing the fuses. Figure 8 shows a simulated case where nulling the control points is not very effective.

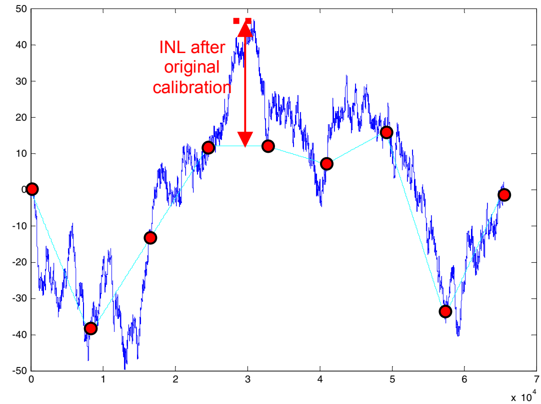

Figure 8 Simulated illustration of residual INL error shown after nulling the control points

The advantage of such a simple algorithm could be the fact that the evaluation of the initial INL at all codes is not necessary, and only the uncalibrated voltages at the control points are needed. One can also argue that the algorithm would work perfectly with a very high number of segments. However, our goal is to improve INL as much as possible, given our memory size and die cost constraints. Therefore, we seek optimization methods for calibration that use full information from the uncalibrated transfer curve.

It can be shown that nulling control points can reduce the total INL by a factor of $\sqrt{(n_{trim}-1)/1.5}$ on a statistical average sense, when the number of independent resistors in each segment remains much larger than 2. For example, if 33 trim points are used, we can reasonably expect the INL to be improved by a factor of about $\sqrt{32/1.5} \approx 4.6$. Based on initial results, this 4.6 number slightly over-estimates actual measurement data, where +/- 40LSB typical INL readings reduce to +/- 10 LSB readings after nulling the control points.

We used an iterative, non-optimal algorithm to improve calibration. The next step in our research will be to find an optimal algorithm for the trim, but our current optimization scheme provides significant value. First, a least square method is used to find the trim values at the knots. That is, INL with respect to a least squares "best fit" line is evaluated and nulled at the control points (some manufacturers specify INL with respect to a "best fit line"). This method provides a good starting point. Other starting points may provide comparable performance, such as the end point adjusted line. In the second step, the maximum positive and maximum negative deviations between two consecutive segments are determined. The third step makes adjustment to the trim values at each knot

so that the maximum deviation on the positive side and that on the negative side are about equal in size. Since the adjustment in step 3 will usually affect the results in step 2, steps 2 and 3 are repeated until the results no longer change significantly. The trim optimized calibration curve obtained from this optimization algorithm is shown in Figure 9 as the purple curve (simulation). Notice that the trim values at the knots are no longer on the original INL_k curve. This will increase the resultant INL_k at the knots but reduce the overall INL since the deviation will be more evenly distributed on both the positive and negative sides around each knot. This technique is not optimal but it provided significant (about 20% average improvement of INL on actual silicon).

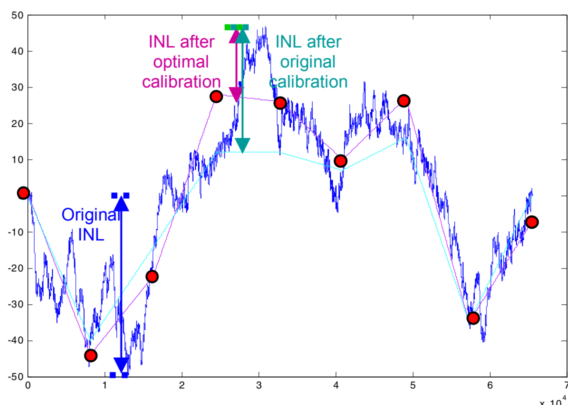

Figure 9. Simulated illustration of iterative INL optimization

4.4 Test Algorithm after Calibration, Test Cost

One needs to be careful about how to test the device after INL calibration. Once the Linearity Cal-DAC starts generating non-zero waveforms to correct for the main-DAC INL, a lot of assumptions we made about main-DAC segmentation, INL and DNL becomes invalid. Moreover, it is still cost prohibitive to make an all-codes linearity testing.

The approach we are taking is to measure the INL cal-DAC range of each channel during production testing. The INL cal-DAC range is measured for a pair of control points that are maximally apart. Due to significant scaling, the DC errors of the cal-DAC are not significant, the only significant parameter is range. Using the range measurement and Cal-DAC resolution, we deduct the maximum voltage increment that can be contributed by the Cal-DAC for two consecutive main-DAC codes. As specified in the chip architecture, this value is very close to 1/8 main-DAC LSBs. Therefore, the DNL after calibration will be nothing but the *measured DNL before calibration* plus approximately 1/8 LSBs.

The DNL is accurately measured before calibration, and it is measured after calibration that it will not worsen by more than ~1/8 LSBs. INL can now be measured at all codes, using a fast setting for the delta-sigma digitizer. All-codes fast measurement of INL after calibration takes approximately 2 seconds of test time per channel, and it is shown to be +/- 0.5 LSB accurate for INL (correlated with a volt-meter). As mentioned before, this fast measurement with a delta-sigma ADC will filter DNL errors significantly, but will not affect the INL errors.

The optimization algorithm described in the previous section does not exercise the DAC multiple times. Once the uncalibrated data is captured, and once cal-DAC range is measured for each channel, the optimization algorithm operates on a software model of the main DAC and cal-DAC and therefore it operates very fast.

The software model can also predict the INL after calibration accurately, therefore the all-codes measurement that uses fast digitizer settings is performed after fuse blowing operation, further reducing test time. Note that the software model uses measured data from the main DAC and the cal-DAC.

Once the calibrated INL is within specification, the fuses are blown. At an increased fuse VDD voltage of 5.5V, 4 fuses can blow simultaneously in 5ms. Blowing more than 8 fuses in parallel can be unreliable. As the 200mA clamped power supply continuously charges the 10uF fuse capacitor, the fast rising fuse blow current is sourced by the capacitor itself, which is placed very close to FUSEVDD pin. Once the fuse array data is placed in tester's digital source memory, fuses can be blown for 4 sites in parallel, 4 fuses at each site, enabling 16 fuses blown simultaneously. The total test time for the fuse blow operation is surprisingly low, well under 1 seconds. Once the fuses are blown the parity bits are also programmed.

Once the fuses are blown, they are checked 16 at a time using read-back.

After all fuse programming is complete the master fuse is blown, the device is checked (for INL) by an all-codes linearity test at a fast digitizer setting (Notice that the filtering of DNL can be tolerated since we previously have accurate DNL data).

Total target test time, full-chip, 1 site (4 sites) is as follows:

- Uncalibrated, segmented INL evaluation: 4 (1.5) seconds
- Software optimization: 0.2 (0.2) seconds
- Fuse blow: 0.5 (0.2) seconds.
- Calibrated all-codes INL evaluation: 8 (2) seconds
- All other tests combined: 3 (1.2) seconds

In a multi-site setting, a total test time in the order of 5 seconds is very reasonable for this device. It can be argued

that the calibration increased the overall test cost by only about 3 seconds per chip, in a 4-site setting. The goal of the test solution is achieved, by keeping the test cost slightly over package cost and significantly under the die cost.

5.0 Results

The DAC is manufactured on an ultra-low cost, 0.5u 5V CMOS process. The die area is 4mm x 4mm. The package is a 40-lead, 6mm x 6mm x 1mm QFN package. Due to cheap process and reasonable test cost and single insertion testing, this design can offer high performance at a low cost. Dual insertion testing will further enhance the performance by guaranteeing a tight offset drift and tight gain drift at the expense of a minimal test cost increase. The chip layout is seen in Figure 10.

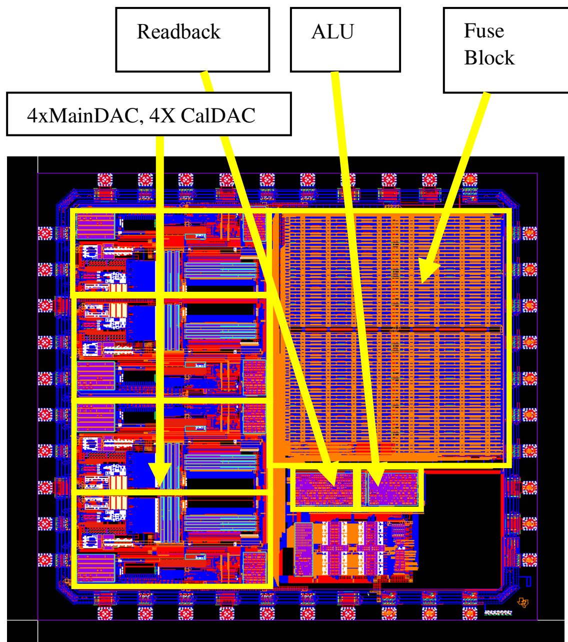

Figure 10. Chip Layout

Significant development is made to ensure a testable design. Also significant algorithmic development is made to reduce test cost.

Figures 11, 12 and 13 constitute readings from actual silicon. Channel D data is shown. Other channels perform similarly. Compare and contrast with figures 3a, 3c, and 3d to see the INL improvement without a significant DNL penalty. Also notice that the number of PWL segments used limits the INL improvements to within 4X to 5X.

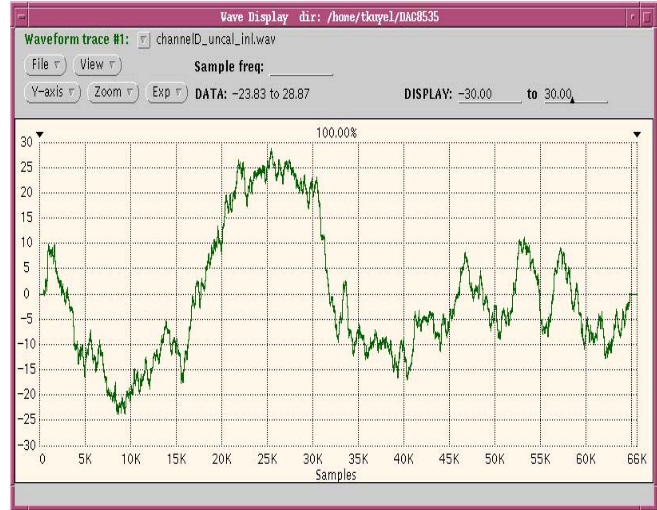

Figure 11. Actual Silicon: INL (LSBs) before calibration

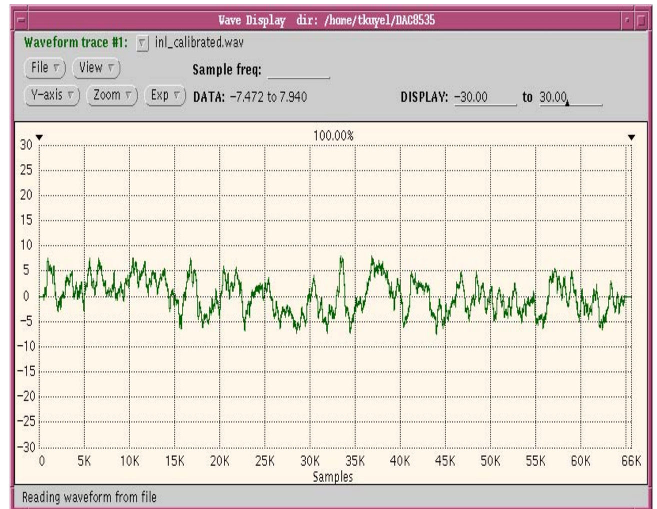

Figure 12. Actual silicon: INL (LSBs) after calibration

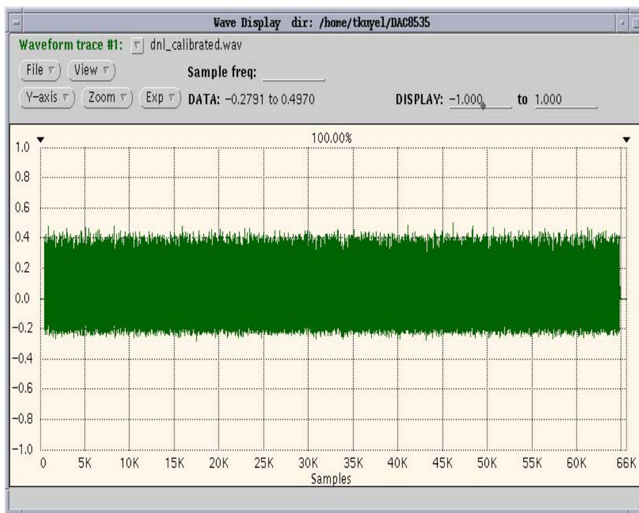

Figure 13. Actual silicon. DNL is preserved after calibration

6.0 Conclusions

A mixed-signal, piece-wise linear calibration solution is introduced to improve DC transfer function errors of resistor string DACs. The calibration uses a single insertion at final test. This implementation eliminates the need for exotic thin-film processes, expensive laser trimming setups and costly wafer probing, which are traditionally used for designing accurate D/A converters. Unlike software-only techniques, the calibration method does not strongly trade-off DNL for INL. The method is implemented on monolithic silicon, and the silicon is fabricated, packaged and tested on an ATE. The implementation was done using fuse links on an ultra low cost CMOS process with poly-silicon resistors. To obtain 5X better linearity, die area almost doubled and power increased by about 30%. However, the low cost CMOS process and the low-power overall design provide enough room for such a trade-off.

This work is protected by multiple US and foreign patents assigned to Texas Instruments Inc.

7.0 Acknowledgments

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8.0 References

[1] R. Geiger, P. Allen, N. Strader, *VLSI Design Techniques for Analog and Digital Circuits*, McGraw-Hill, 1990
[2] B. Razavi, *Data Conversion System Design,* IEEE Press, 1995
[3] S. Wilensky, “High Accuracy D/A Converter and Transient Elimination System”, US Patent 4,338,592, 1980
[4] J. Naylor, “A Complete High-Speed, Voltage Output, Monolithic DAC”, IEEE JSSC, Vol. SC-18, No. 6, 1983
[5] Texas Instruments Inc. *DAC7634 Datasheet*, 2000.
[6] A. Dingwall, V. Zazzu “An 8MHz 8b CMOS Subranging ADC”, *ISSCC*, 1985
[7] Texas Instruments Inc., *TLC5618 Datasheet*, 1997
[8] M. Pelgrom, “A 10-b 50-MHz CMOS D/A Converter with 75 ohm Buffer”, *IEEE JSSC*, Vol. 25, No. 6, 1990
[9] M. G. Tuthill, “High Resolution Digital to Analog Converter”, US Patent 4,491,825, 1985
[10] R. Neidorf, “D/A Converter Having Multiple Resistor Ladder Stages”, US Patent 5,554,986, 1996
[11] J. Ashe, “D/A Converter with Segmented Resistor String”, US Patent 5,495,245, 1996
[12] W. Rempfer, “Digital to Analog Converter”, US Patent 5,396,245, 1995
[13] M. Imamura, “Multi-channel D/A Converter Utilizing a Coarse D/A Converter and a Fine D/A Converter”, US Patent, 5,801,655, 1998
[14] A. Yilmaz, “LSB Interpolation Circuit and Method for Segmented D/A Converter”, US Patent 6,246,351, 2001
[15] Texas Instruments, *DAC8531 Datasheet*, 2001
[16] Linear Technology Corporation, *LTC2601 Datasheet*, 2004
[17] T. Kuyel, US Patent Pending, Filed December 2004
[18] T. Kuyel, K. L. Parthasarathy “Piece-wise Linear Calibration Method and Circuit to Correct for Transfer Function Errors of D/A Converters”, US Patent, 6,642,869, 2003