LOW KICKBACK NOISE TECHNIQUES FOR CMOS LATCHED COMPARATORS

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ABSTRACT

The latched comparator is utilized in virtually all analog-to-digital converter architectures. It uses a positive feedback mechanism to regenerate the analog input signal into a full-scale digital level. Such high voltage variations in the regeneration nodes are coupled to the input, disturbing the input voltage - *kickback noise*. This paper reviews existing solutions to minimize the kickback noise and proposes two new ones. HSPICE simulations verify the effectiveness of our techniques.

1. INTRODUCTION

The basic operation of an Analog-to-Digital Converter (ADC) is the *comparison*. The *latched comparators* work synchronously with the clock signal and indicate, through their digital output level, whether its differential input signal is positive or negative. They use a positive feedback mechanism to regenerate the analog input signal into a full-scale digital signal (regenerative amplification), because this is much faster and power efficient than performing multi-stage linear amplifications [1].

The large voltage variations on the regeneration nodes are coupled, through the parasitic capacitances of the transistors, to the input of the comparator. As the circuit preceding the comparator does not have zero output impedance, this disturbs its input voltage and may degrade the accuracy of the converter. In flash ADCs, where a large number of comparators are switched at the same time, this may affect the input and reference voltages of the converter [2]. When the latched comparators are used after resistive interpolation [3] in parallel-type ADCs (flash, two-step, folding), the location of the code transition voltages may be altered. Also, in some pipeline architectures, the settling of the amplifiers in each stage may be degraded, due to this phenomenon [4].

This paper is divided in 5 sections, the first of which is the present Introduction. Section 2 classifies existing CMOS latched comparators, and analyzes the existing techniques to minimize the kickback noise. Section 3 presents two new techniques that can be utilized in existing comparator architectures, which achieve a remarkable level of kickback noise reduction. Finally, in section 4, Conclusions are drawn.

2. EXISTING SOLUTIONS

There is a large variety of CMOS latched comparators, and it would be impossible to present a complete survey, in a paper of this dimension. We will, nevertheless, suggest a classification and present the main characteristics of the comparators belonging to each category.

2.1. Static latched comparators

The first category incorporates the *static latched comparators* [5-10]. A representative example of this group is the comparator *adapted* from [5], represented in Fig. 1.

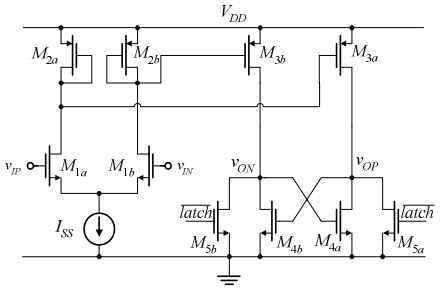

Figure 1: Example of a static latched comparator.

In the reset phase, $\overline{latch} = high$, M_{5a}/M_{5b} push the outputs to ground. Transistors M_{1a}, M_{1b}, M_{2a}, M_{2b}, act as a pre-amplifier, whose current is mirrored to the output nodes, through M_{3a}/M_{3b}. When $\overline{latch}$ goes *low*, M_{5a}/M_{5b} turn off and the current flowing in M_{3a}/M_{3b} charge the output nodes. Depending on the input voltage, one of the regeneration transistors, M_{4a} or M_{4b}, turns on first, initiating the regeneration of the output voltages. Having presented an example, the common characteristics of the comparators in this group can now be summarized:

- There is *static power consumption*, which does not vary during the reset phase and most part of the regeneration process. After the regeneration is completed one of the regeneration transistors (M_{4a} or M_{4b} example of Fig. 1) cuts off and the supply current changes.
- The regeneration is done by two class A (constant current) cross-coupled inverters; in Fig. 1, the two class A cross-coupled inverters are formed by M_{3a}/M_{4a} and M_{3b}/M_{4b}.
- There is always a differential pair acting as pre-amplifier, whose output current is either mirrored [5-7] or injected through a cascode transistor [8-10] in the regeneration nodes.

The kickback noise is caused by the voltage variations on the nodes that are capacitively coupled to the input, i.e., the nodes where the drains of the differential pair are connected to. In this type of comparators these are isolated from the regeneration nodes, where the voltage variations are large; this results in low kickback noise. The comparator proposed in [8] still has considerable voltage variations at the drains of the differential pair. This is improved in [9], by limiting the voltage excursion on the regeneration nodes, using MOS diodes.

The correct operation of the comparators depends on their sensitivity to variations in the input voltage. This type of comparators has, at least, two poles in the transfer function between input and regeneration nodes: the pole in the intermediate node, where the drains of the differential pair connect, and the pole in the regeneration nodes.

Another drawback of these comparators is their slow regeneration process, due to their current limited class A operation. These two issues, along with the fact that these comparators are always consuming, even when they have already decided, does not make them very attractive for high-speed and low power operation.

2.2. Class AB latched comparators

A second type of comparators, which we will name *class AB latched comparators*, addresses these speed limitation problems. An example of this type of comparators is shown in Fig. 2.

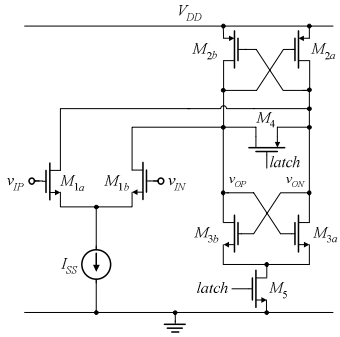

Figure 2: Example of a class AB latched comparator.

When *latch* is *low* (*reset phase*), M_5 is in cutoff, which prevents any current flow in M_{3a} and M_{3b}. M_4 is the reset switch and forms, along with M_{2a} and M_{2b}, the load to the differential pair constituted by M_{1a} and M_{1b}. When *latch* goes *high* the *regeneration phase* starts: the reset switch is opened and transistors M_{2a}/M_{3a} and M_{2b}/M_{3b} form two back-to-back CMOS inverters that regenerate the small output voltage, found in the beginning of this phase, to full-scale digital signals. This comparator should be designed to have, in the reset phase, an output voltage that is interpreted as the *high* logic value.

Other examples of this type of comparators may be found on [4,11-15]. The main characteristics of the comparators in this group may be summarized as follows:

- The regeneration is done by two cross-coupled CMOS inverters. *Their current increases momentarily, during the regeneration process, to charge the output nodes faster* – class AB operation. Faster regenerations can be achieved with lower power dissipation, in comparison to the static latched comparators
- In all cases, except [11], the drains of the input differential pair are directly connected to the regeneration nodes. The circuit reacts quicker to input voltage variations, because there is only one pole. Unfortunately, this also increases the kickback noise because there are now rail-to-rail signals at nodes capacitively coupled to the inputs. In [11] the current of the differential pair is still mirrored to the regeneration nodes.

Several kickback reduction techniques have been proposed. The most common solution is to add a pre-amplifier before the comparator [2,16], at the cost of increased power consumption. Reference [4] utilizes source followers.

In [14,15] the drains of the input differential pair and the regeneration nodes are isolated with switches, which are opened when regeneration starts. However, this forces the transistors of the input differential pair into triode region, and the voltages at their drains still vary, generating kickback noise. In [15] a pre-amplifier is still used.

So, the existing kickback noise reduction techniques for these comparators either do not solve the problem completely or increase considerably the power dissipation.

2.3. Dynamic latched comparators

The class AB latched comparators are faster and more power efficient than the static comparators. However, there is still supply current in the reset phase and after the comparator has finished regeneration. In the *dynamic latched comparators* there is only current flowing during the regeneration. An example is the comparator shown on Fig. 3, which is *adapted* from [17].

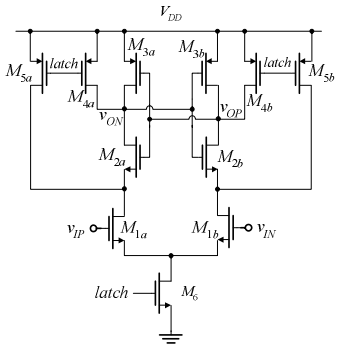

Figure 3: Example of a dynamic latched comparator.

When *latch* is *low* (reset phase), the transistors M_{4a}/M_{4b} and M_{5a}/M_{5b} reset the output nodes and the drains of the differential pair (M_{1a}/M_{1b}) to V_{DD}. M_6 is off and no supply current exists. When *latch* goes *high* the reset transistors are opened; current starts flowing in M_6 and in the differential pair. Depending on the input voltage, one of the cross-coupled inverters that make the regeneration, M_{2a}/M_{3a} or M_{2b}/M_{3b}, receives more current, which determines the final output state.

After regeneration is completed one of the output nodes is at V_{DD}; the other output and both drains of the differential pair a have 0 V potential. There is, in this situation, no supply current, which maximizes power efficiency. Other examples of this type of comparators can be found in [18,19].

The dynamic comparators also have kickback noise problems. Adding a pre-amplifier before the comparator attenuates this problem, but introduces static power dissipation. MOS switches can be inserted at the inputs of the comparator, and opened when the regeneration phase starts [20]. This effectively eliminates the kickback noise during the regeneration phase. There is, however, kickback noise in the beginning of the reset phase, when these switches are closed again. We will discuss this issue on the next section.

A neutralization technique is used in [21], which accomplishes moderate improvements. This will also be further discussed in the following section.

3. PROPOSED KICKBACK REDUCTION TECHNIQUES

In this section we propose two kickback noise reduction techniques. The first can be applied to any class AB comparator, where the drains of the differential pair are directly connected to the regeneration nodes. The second technique can be used in *any* latched comparator, and it is specially suited to the cases where the circuit preceding the comparator is in reset phase, during the regeneration of the comparator. This situation is, for example, found in parallel type ADCs [22].

3.1. Technique I

This technique aims the reduction of kickback noise in the comparators that have the input differential pair directly connected to the regeneration nodes. It consists on two steps:

1. **Minimize the voltage variations on the drains of the differential pair.** The differential pair drains are isolated from the regeneration nodes, using switches which are opened during the regeneration phase. An alternative path for the current of the differential pair *must then be provided*, preferably keeping its drain voltages near the values found in the reset phase.
2. **Use the neutralization technique.** When the drain voltages of the input differential pair vary, the circuit preceding the comparator, which has non zero impedance, must provide the charge current for the C_{GD} parasitic capacitances of the differential pair. The disturbance caused by these charge currents

is the kickback noise. Adding two capacitances with a value $C_N = C_{GD}$ in the way represented in Fig. 4, cancels the kickback noise, if the voltage variations at the drains are complementary. This happens because the charge current comes now from the capacitances added and not from the circuit preceding the comparator (the arrows on Fig. 4 represent the currents flowing when v_{D2} increases and v_{D1} decreases).

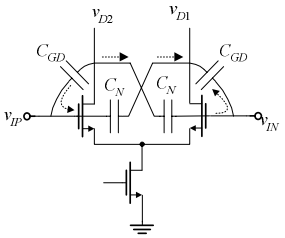

Figure 4: Neutralization technique.

The neutralization compensates the effect of the drain voltage variations which may still exist, after the changes in step 1 have been applied. One could think that the kickback problem could be solved using only neutralization, as [21] does. This, however, is not enough because the voltage variations on the regeneration nodes are not perfectly balanced.

Fig. 5 shows the comparator of Fig. 2, modified to incorporate the kickback reduction technique just described. In reset phase (*latch = low*) M_{6a}/M_{6b} connect the drains of M_{1a}/M_{1b} to the regeneration nodes, and M_{7a}/M_{7b} are off. Consequently this comparator operates, in the reset phase, similarly to the one of Fig. 2. When *latch* goes *high* M_{6a}/M_{6b} open, isolating the drains of M_{1a}/M_{1b} from the regeneration nodes. Transistors M_{7a}/M_{7b} become diode connected loads to the differential pair. These transistors should be sized to maintain the drain voltages of M_{1a}/M_{1b} similar to the value found in the reset phase. Finally, M_{8a}/M_{8b} perform the neutralization. These should have minimum length, and half the width of M_{1a}/M_{1b}.

Fig. 6 shows the circuit used to evaluate the kickback noise. The stage preceding the comparators is modelled using a Thévenin equivalent. We have used $R_{TH} = 8$ kΩ in our simulations.

Fig. 7 shows the differential input voltage at the input of the comparators of Fig. 2 - case (b) - and of Fig. 5 – case (c) - which are running at 200 MHz. Curve (a) is the voltage at the terminals of the Thévenin voltage source (see Fig. 6), which changes at $t = 8$ ns, from 300 mV to –1 mV.

When the comparator of Fig. 2 is used, the voltage at its inputs is greatly disturbed in every *latch* signal transition. In the comparator of Fig. 5 the kickback noise is virtually eliminated: when the input voltage is 300 mV the perturbations at the input of the comparator have a peak value of 4 mV and disappear rapidly, as shown in Fig. 7; when the input voltage is -1 mV no perturbation is observed. *Thus, a kickback noise reduction of, at least, two orders of magnitude is obtained.*

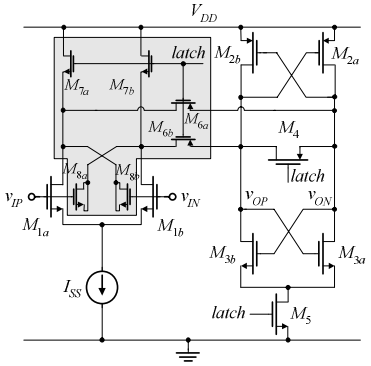

Figure 5: Application of kickback noise reduction technique I.

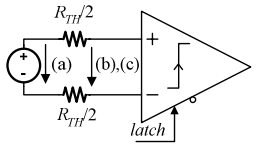

Figure 6: Circuit used to evaluate the kickback noise.

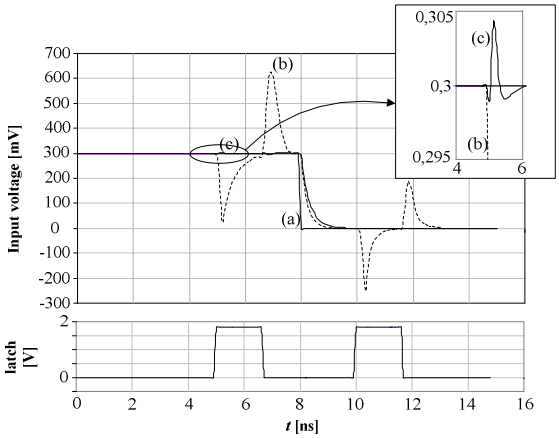

Figure 7: Simulation results of Technique I.

3.2. Technique II

This kickback reduction technique can be used with any latched comparator, where two modifications must be performed:

1. **Insert sampling switches before the input differential pair, which are opened in the beginning of its regeneration phase.** This eliminates the kickback noise generated in this phase, and implements a sampling function, which may be useful in some cases.
2. **Detect when the latched comparator has already decided and make an asynchronous reset of the sampled input voltage.** This prevents the previous sampled voltage from disturbing the next comparison.

Fig. 8 shows an example of the application of this technique. The latched comparator regenerates in *ph*1. Two inverters are used to buffer its outputs and a SR latch memorizes the comparison result in the reset phase. In this example it is assumed that, in the reset phase, the outputs of the latched comparator go to V_{DD}, like in the comparator of Fig. 3, or at least are near V_{DD}, like in the comparator of Fig. 2. This type of arrangement is typical [9,10,13,15,22].

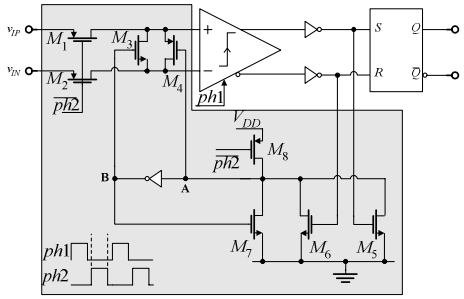

Figure 8: Application of kickback noise reduction technique II.

The transistors that implement the kickback reduction are inside the shaded area. In the reset phase (*ph*1 = *latch* = *low*, *ph*2 = *high*) the input switches, M_1/M_2, are on. Node **A** is pushed to V_{DD} by M_8, turning off the input reset transistors, M_3 and M_4. The outputs of the latched comparator are at V_{DD}, which means that M_5 and M_6 are off; M_7 is also

off because node **B** is *low*. At the end of *ph*2 M_1/M_2 turn off, therefore preventing any kickback noise from reaching the inputs, when regeneration starts. M_8 is also turned off, leaving node **A** near V_{DD}. Some time after the *ph*1 has changed to *high* (start of regeneration phase), one of the inputs of the SR latch reaches V_{DD}, turning on either M_5 or M_6. This pushes nodes **A** to *low* and **B** to *high*, which turns on M_3/M_4 and resets the sampled input voltage. *This can be done because the latched comparator has already decided*. In this way, any influence from previously sampled input voltages is eliminated.

Transistor M_7 guarantees that M_3/M_4 are maintained *on*, in the non-overlap time between the end of *ph*1 and the beginning of *ph*2. This is done because, when *ph*1 goes *low*, the comparator starts the reset and M_6/M_5 may turn off. Using M_7 the reset of the sampling nodes only ends when *ph*2 goes *high* (because M_8 pushes node **A** to V_{DD}), which is also when the input switches turn on.

To verify the effectiveness of this solution, the comparator of Fig. 3 was used in the simulations, whose results are shown in Fig. 9.

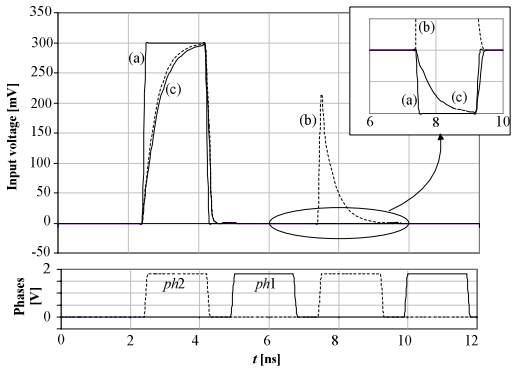

Figure 9: Simulation results of Technique II.

Curve (a) is the voltage at the terminals of the voltage source of the Thévenin equivalent (see Fig. 6) of the preceding stage, which is assumed to be in reset during the regeneration phase of the comparator (*ph*1); this situation is usual in parallel type converters [22]. The case where the comparator alone is simulated is not shown, because it yields results similar to those found in Fig. 7, for the comparator of Fig. 2: the input voltage suffers perturbations every time the *latch* signal of the comparator, in this case *ph*1, has a transition.

Curve (b) is the input voltage, *when sampling switches are used in the inputs* (M_1 and M_2 in Fig. 8) – this technique is proposed in [20] to reduce kickback noise in the regeneration phases (*ph*1 on). However, it creates a large kickback on the reset phase (*ph*2 on), because of the charge previously stored in the sampling nodes. In the example of Fig. 9 the kickback is so large that the input voltage does not have time to reach negative values (it should get near -1 mV): *the comparator makes, in this case, a wrong decision.* Finally, case (c) is obtained with the solution of Fig. 8 – the input voltage always goes smoothly to the final values and *the kickback noise is eliminated*.

The reset transistors (M_3/M_4) have the minimum length and a width near the minimum allowed by the technology. Therefore the input capacitance of the comparator remains almost unchanged. The increase on power dissipation, when this technique is used, is acceptably small (about 10 % in the case presented).

4. CONCLUSIONS

This paper reviewed the main latched comparator architectures and compared them in terms of kickback noise, speed and power dissipation. It was concluded that the most power efficient comparators generated more kickback noise. Previously used kickback noise reduction techniques were also examined; these either do not solve the problem completely or increase considerably the power dissipation. Two new kickback noise reduction techniques were then proposed, which achieve remarkable results, as it is demonstrated with HSPICE simulations.

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