9.7 A 20MHz BW 68dB DR CT ΔΣ ADC Based on a Multi-Bit Time-Domain Quantizer and Feedback Element

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Low-power, small-area, 20MHz-BW ADCs that can be integrated in nanoscale CMOS technologies are of immense interest to the wireless communication industry. Implementation of high-performance analog circuits in nanometric technologies faces several challenges [1]. Time-domain digital signal processing (TDSP) [2] can be used as an alternative for some analog circuits to overcome these challenges. The TDSP technique utilizes the high timing resolution available in nanoscale technologies, and can be implemented using digital circuits that are inherently less susceptible to noise. Circuits using this technique also become faster, smaller and consume less power with technology scaling. Hence, solutions using TDSP with as many digital circuits as possible are desired. An ADC architecture that uses a VCO-based time-domain quantizer is presented in [3]. This architecture uses a conventional feedback element (multi-element DAC with DEM) and 950MHz sample rate that leads to high power consumption. In this work, a pulse-width modulator (PWM) and an all-digital time-to-digital converter (TDC) are used to implement the quantizer as well as the feedback element in the time domain. This approach achieves the necessary linearity in the feedback path without DEM or calibration, and allows a low output rate of 250MS/s.

Figure 9.7.1 illustrates how the conventional ΔΣ ADC architecture is modified to process signals in the time domain. During each clock period, a pulse with discrete levels of width in time steps of T_0 is used to represent the sample instead of the usual discrete levels of amplitude in voltage steps of V_0. The PWM converts the voltage at the output of the loop filter to a pulse p(t) with corresponding width. The TDC generates digital codes that are discrete representations of the edges of the p(t) signal, and also generates a 'time-quantized' feedback pulse $p_q(t)$ that corresponds to the output code, which is fed back to the loop filter. The loop filter shapes the quantization error of the TDC and also the nonlinearity error of the PWM.

Figure 9.7.2 shows a timing diagram to illustrate the input and outputs of the TDC with a simple example of 8 quantization steps. For the p(t) shown, output codes of DR_{out}=2 and DF_{out}=6 are generated for rising and falling edges, respectively. The TDC also generates $p_q(t)$ with rising and falling edges that are aligned to CK2 and CK6, respectively. A simplified 8-level TDC example is shown in Fig. 9.7.2. Flip-flops driven by clocks CK0–3 (CK4-7) register a thermometer code that yields DRout (DFout) upon binary conversion. The output of the OR gate O1 (O2) goes 'high' when the first flipflop driven by clocks CK0–3 (CK4-7) goes 'high.' O1 and O2 drive the S and R inputs of a latch to generate $p_q(t)$. The full schematic of the TDC used in the ADC is also shown in Fig. 9.7.2. A total of 50 quantization steps with T_0=80ps in a 4ns period are implemented with 25 levels for each of the rising-edge and falling-edge quantizations. Fifty clock phases are generated using delay elements, whose delays are tuned for process variations with the help of a phase detector. The main design requirements for the TDC are the linearity of the time steps of $p_q(t)$ (σ< 800fs) and its in-band timing jitter (σ< 250fs). Several measures are taken in the design to meet the linearity. First, the digital inverters used to generate the delayed clocks (CK1-52) and the 25-input OR gates are carefully sized and laid out to form a uniform pattern. Second, every Nth flip-flop output is ANDed with the (N+2)th clock, reducing the error probability due to the data-dependent delay of the flip-flops to an insignificant value. Third, the 25-input OR gates are built using wired-NMOS NOR gates to ensure equal delay for all steps. To minimize the parasitic capacitance, the gate is built in 2 stages using five 5-input NOR gates followed by a 5-input NAND gate. Most of the timing jitter is contributed at the middle of the switching event (when current is maximum) and is suppressed by using dynamic logic.

The schematics of the loop filter and the PWM are shown in Fig. 9.7.3. This active-RC loop filter implements a 3rd-order inverse-Chebyshev NTF. INT1 and INT2 are implemented with 2-stage Miller-compensated amplifiers and INT3 uses a pair of inverters with CMFB as the amplifier to minimize excess phase for the loop-delay compensation path. The array of inverters driving MOSCAPs connected to the virtual ground of INT3 implements a programmable direct-feedback path for loop-delay compensation. A current proportional to $p_q(t)$ is injected at the virtual ground of INT1 by using a differential pair. The PWM signal is generated by comparing the input with a ramp waveform V_r. The input signal is sampled twice during each clock period by non-overlapping clocks CLK1 and CLK2. This scheme provides the superior linearity of asymmetric PWM and obtains twice the normal OSR for the given throughput rate. V_r is generated by switching currents into capacitors using a clocked differential pair. The comparators are implemented by using inverters as transconductors (a single-ended version is shown in Fig. 9.7.3) with outputs tied together and fed to a cascade of 2 inverters that generate p(t). The nonlinearity due to sampling switches, nonideal ramp waveform and the signal-dependent comparator delay can easily be tolerated up to 40dB due to noise shaping.

The ADC is fabricated in a 65nm digital CMOS technology. The TDC operates from a 1.3V supply and consumes 4.5mW, and the rest of the modulator (including non-overlapped clock generators) operates from 1.2V while dissipating 6mW. The output data captured using a logic analyzer represent the quantized pulse-timing edges and are used to reconstruct the $p_q(t)$ in Matlab. In the real system, a special FIR decimation filter [4] that processes pulse edges (rather than amplitudes) must be used for reconstruction of data. Figure 9.7.4 shows the measured spectrum of the output data captured for 3.9MHz, -5dBFs and -30dBFs sine-wave inputs (0dBFs is $1.2V_{pp}$). Measurement plots of SNR and SNDR (calculated in 120kHz-to-20MHz BW) for various amplitudes of a 3.9MHz input are shown in Fig. 9.7.5. From Fig. 9.7.5, the dynamic range (defined as the amplitude range with SNR > 0dB) is found to be 68dB. The peak SNR and SNDR are about 62dB and 60dB, respectively, and are observed for -4dBFs input. Figure 9.7.6 compares the performance of the ADC with that of state-of-the-art ΔΣ ADCs with no calibration in the feedback element, and Fig. 9.7.7 shows the die micrograph. The FOM in Fig. 9.7.6 is defined as Power/(2×BW×2^{ENOB}), where ENOB is calculated from SNDR. Although the FOM is comparable to the state of the art, the new architecture with all-digital quantizer and feedback element is better equipped to reduce power with technology scaling. Also, the lower output rate of the modulator can reduce power in the decimation filters.

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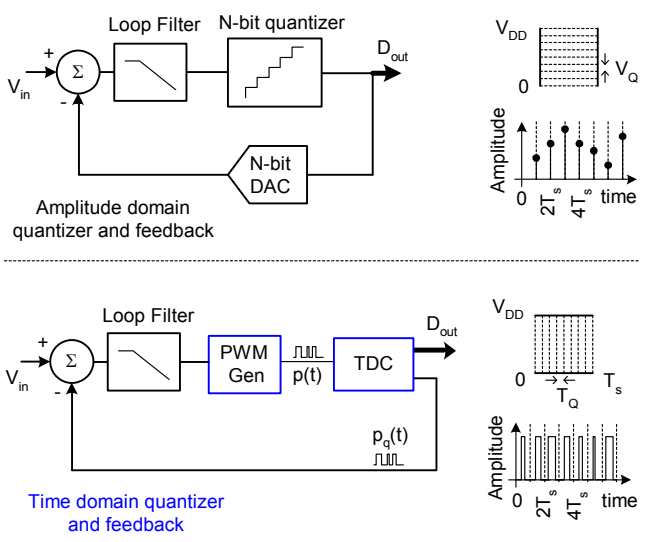

Figure 9.7.1: Conventional and proposed CT ΔΣ ADC architectures.

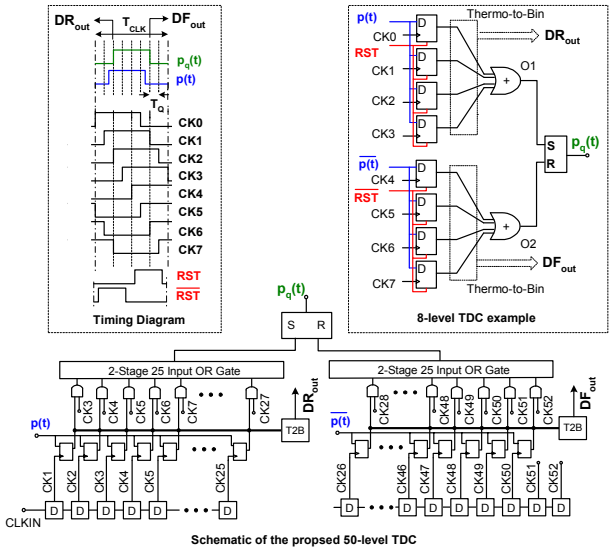

Figure 9.7.2: Example 8-level TDC, timing diagram and schematic of the TDC.

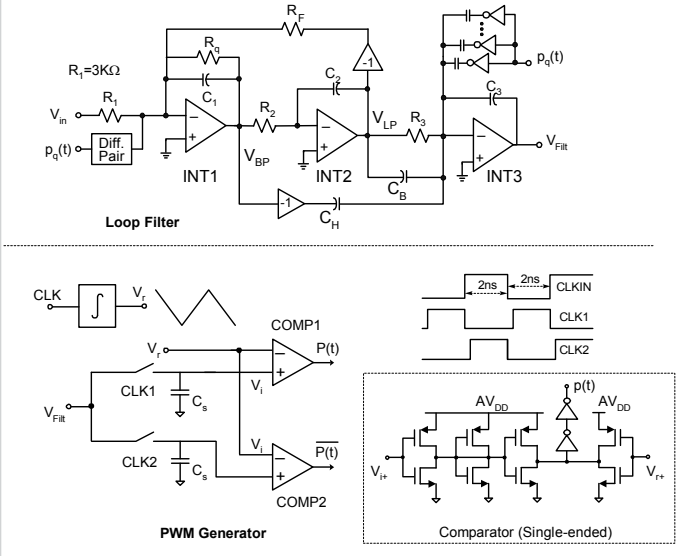

Figure 9.7.3: Simplified single-ended schematics of the loop filter and the PWM.

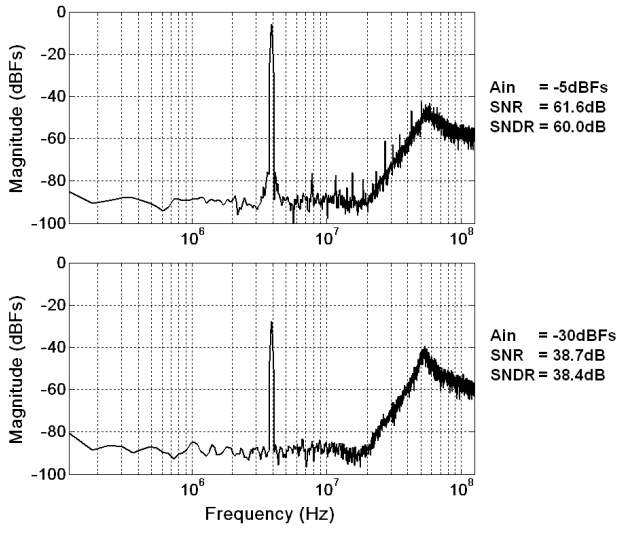

Figure 9.7.4: Measured output spectrum (8192-point Welch periodogram) for 3.9MHz, -5dBFS and -30dBFS inputs.

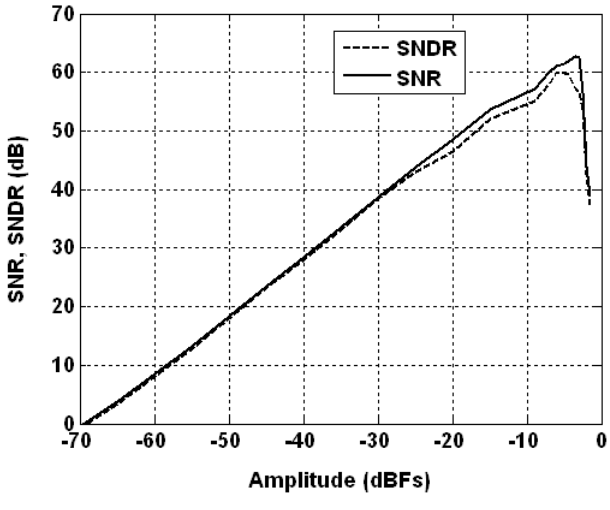

Figure 9.7.5: Measured SNDR and SNR across input amplitudes.

	[3]	[5]	[6]	Proposed
SNDR (dB)	55	69	70	60
Power (mW)	38	28	27.9	10.5
FOM (fJ/conversion-step)	2058	304	270	319
Area (mm^2)	0.19	0.25	1.0	0.15
Output Rate (MS/s)	950	680	420	250
Technology (nm)	130	90	90	65

Figure 9.7.6: Comparison with state-of-the-art 20MHz ΔΣ ADCs.

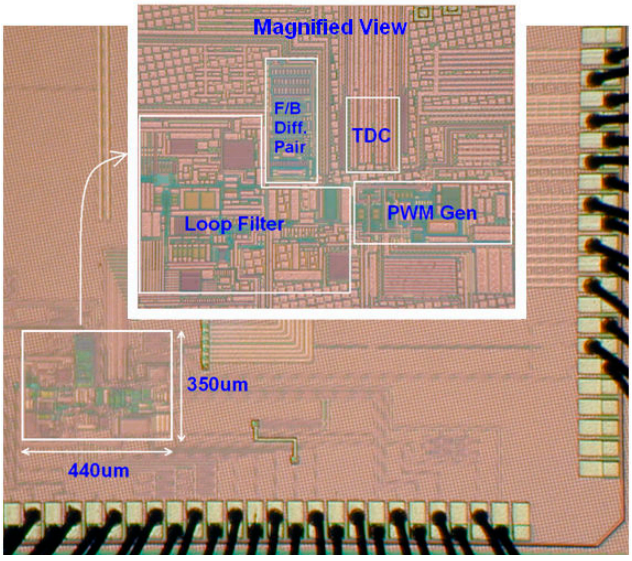

Figure 9.7.7: Die micrograph.

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