Noise in Phase-Locked Loops [Invited]

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Abstract

Jitter and phase noise properties of phase-locked loops (PLL) are analyzed, identifying various forms of jitter and phase noise in PLLs. The effects of different building blocks on the jitter and phase noise performance of PLLs are demonstrated through a parallel analytical and graphical treatment of noise evolution in the phase-locked loop.

Introduction

Phase-locked loops (PLL) [1] can be used to maintain a well-defined phase, and hence frequency, relation between two independent signal sources. Due to their versatility, PLLs are usually preferred over other methods of maintaining phase lock, such as injection locking [2]. Monolithic phase-locked loops have been used for clock-and-data recovery in communication systems (*e.g.*, [3]), clock generation and distribution in microprocessors (*e.g.*, [4]), and frequency synthesis in wireless applications (*e.g.*, [5]). In this paper, we will review some of the underlying properties of PLLs, and particularly focus on noise properties of such loops using a companion analytical and graphical treatment of the subject.

Basic Properties of PLLs

In this section, a very brief review of some of the basic properties of PLLs will be presented. The analysis in this section is by no means comprehensive and only addresses the effects that are of central importance for the noise performance of high-frequency PLLs. Properties of PLLs have been studied extensively and can be found in references such as [6]-[16].

Fig. 1a shows a general PLL consisting of a phase detector (PD), a loop filter with the transfer function, $H(s)$, a voltage controlled oscillator (VCO), and a frequency divider denoted as /N. The phase detector generates an output proportional to the phase difference between its two inputs. The first input, V_{in}, is usually generated by an external source, while the second input is directly related to the output of the VCO, V_{out}. Under the locked condition, the negative feedback adjusts the dc value of the VCO control voltage in such a way that the two inputs of the phase detector have a constant phase difference and hence are at exactly the same frequencies. For this to happen, the VCO output frequency has to be N times larger than the input frequency.

The frequency divider in the feedback path is usually used to generate a low noise, high frequency digitally-programmable signal from a low-frequency low-noise crystal oscillator [12]-[18]. The frequency division may be performed using an analog frequency divider [19]-[34] or by a digital synchronous or asynchronous counter [35]-[43].

Properties of the PLL in the locked condition can be best analyzed using the equivalent phase-domain linear time-invariant (LTI) model shown in Fig. 1b, where K_P is the gain of the phase detector in volts/radian and K_V is the VCO gain in Hz/volts. Since phase is the integral of the frequency and the output frequency of the VCO is proportional to its control voltage, the VCO acts as an ideal integrator for the input voltage when the output variable is phase. Therefore, its frequency response can be simply expressed as K_V/s. An ideal frequency divider divides the phase of the input signal by its division ratio, N, and is modeled as an attenuation by a factor of $1/N$ in phase domain. The phase domain transfer function for the system of Fig. 1b is

$$\frac{\Phi_{out}(s)}{\Phi_{in}(s)} = \frac{NK \cdot H(s)}{K \cdot H(s) + Ns} \quad (1)$$

where $K = K_P K_V$. Now we consider this transfer function in two different illustrative cases:

First-Order Loop with No Divider (N=1)

In a first-order loop, no explicit filter, $H(s)$, exists and the phase detector is usually implemented using an analog multiplier or an XOR gate. Assuming no divider (N=1), the input-output phase transfer function of (1) reduces to

$$\frac{\Phi_{out}(s)}{\Phi_{in}(s)} = \frac{K_P K_V}{K_P K_V + s} = \frac{1}{1 + s/\omega_{loop}} \quad (2)$$

where $\omega_{loop} = K_P K_V$ is the loop bandwidth.

It can be easily shown that in a first-order loop, the only way to lower the steady-state phase error is to increase the loop bandwidth. Higher-order loops are more common because they are not limited by this strong coupling between the bandwidth and the steady-state phase error of a first-order loop [6]. A first-order loop, however, can be a useful tool to understand the fundamental noise properties of PLLs.

Charge-Pump PLLs with Higher-Order Loops

Although it is possible to increase the order of the PLL by introducing a filter in the forward path of the loop, the static error does not disappear unless an extra ideal integrator is introduced in the forward path [6]. The static phase error can be eliminated by introduction of a pole at the origin. This can be implemented using a phase-frequency detector (PFD) and a charge-pump (CP) combination, as shown in Fig. 2.

In a charge pump PLL, the PFD has two edge-sensitive inputs and two outputs called *UP* and *DOWN*. If the VCO runs at a lower frequency than the input, the *UP* signal will be non-zero and turn on its associated switch intermittently, while the *DOWN* pulse will be zero continuously. This will inject charge into the charge pump capacitor, C_P, which in turn results in an increase in the output voltage, V_{out}, to adjust the VCO frequency. As long as the dynamics of the loop are much slower than the signal, the charge-pump can be treated as a continuous time integrator. Usually a zero is introduced by adding a resistor in series with the charge-pump capacitor to improve the stability of the loop.

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The voltage on the capacitor grows without bound if the input and output do not have the right phase relationship and therefore no static phase error can persist under the locked condition. In other words, two integrations in the forward path guarantee zero phase error. Thus, the PFD/CP architecture has two advantages over the lowpass architecture, namely, zero steady-state phase error and larger capture range limited by the VCO tuning range.

The phase domain block diagram of Fig. 1b is valid for charge pump PLLs as long as charge-pump switches much faster than the loop dynamics. Under this constraint the combined phase-detector/filter transfer function is given by

$$K_P \cdot H(s) = \frac{I}{2\pi C_P} \cdot \frac{\tau_z s + 1}{s} \tag{3}$$

where $\tau_z = 1/R_Z C_P$ is the frequency of the zero, and I and C_P are the current source and the capacitor in Fig. 2, respectively. Equations (1) and (3) lead to the following closed-loop transfer function for a charge-pump PLL

$$\frac{\Phi_{out}(s)}{\Phi_{in}(s)} = \frac{N(\tau_z s + 1)}{s^2 / \left(\frac{K_V I}{2\pi N C_P}\right) + \tau_z s + 1} \tag{4}$$

Fig. 3 shows this transfer function vs. frequency. Note that the x-axis will become the offset frequency from the carrier when we look at the voltage power spectrum [44]. As shown in the figure, depending on the parameters of the loop, peaking in the phase transfer function of the PLL may be observed. Note that the transfer function of (4) reduces to N for small frequencies, and to $K_V I \tau_z / 2\pi C_P \omega$ for large ωs.

Noise Properties of PLL Building Blocks

To be able to investigate the noise properties of the PLL, it is necessary to have a basic understanding of the noise properties of its building blocks. Now we investigate some of these noise properties.

VCO Noise

Many extensive studies have been dedicated to the noise properties of free running oscillators and VCOs. It is possible to exploit techniques such as noise timing [44], amplitude enhancement [45], and symmetry adjustment [49] to lower the noise of a VCO. A general methodology to optimize a VCO has also been reported [48]. Regardless of the method(s) used to design and optimize a VCO, its frequency- and time-domain properties can be characterized using phase noise and jitter, respectively. In the frequency domain, the power spectrum of phase, $S_{\phi out}(\omega)$, of the VCO demonstrates regions with slopes of $1/f^3$ and $1/f^2$, and a flat region, as shown in Fig. 4a [44]. In the time domain, the uncertainties in the transition times accumulate continuously, increasing the timing jitter of the oscillator [46]. Uncorrelated uncertainties add in a mean-square sense and hence result in square root dependence on the delay from the reference edge, *i.e.*, $\sigma_\tau = \kappa\sqrt{\tau}$, where σ_τ is the rms jitter τ seconds after the reference, and κ is the proportionality constant [47]. If there is a correlated part among transition uncertainties, their magnitudes add directly resulting in an

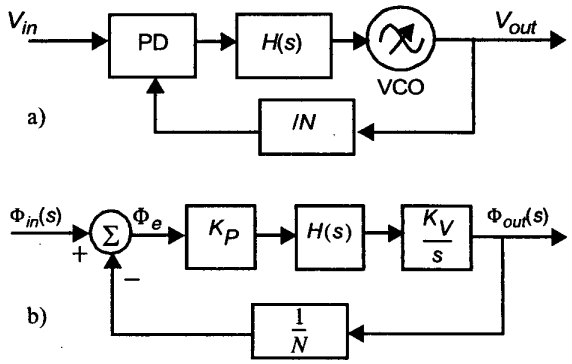

Fig. 1. a) A typical phase-locked loop, b) the equivalent phase domain LTI model for the phase-locked loop of a).

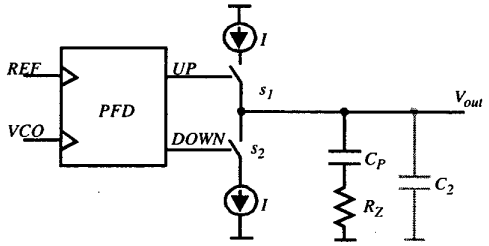

Fig. 2. Phase/frequency detector and charge pump arrangement to implement higher order loops.

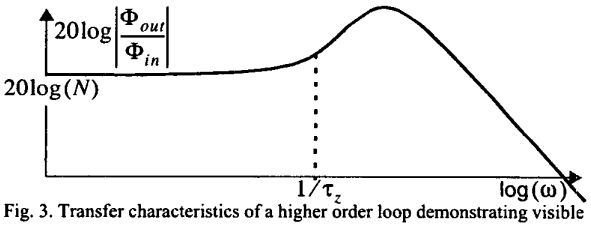

Fig. 3. Transfer characteristics of a higher order loop demonstrating visible peaking in the frequency domain response.

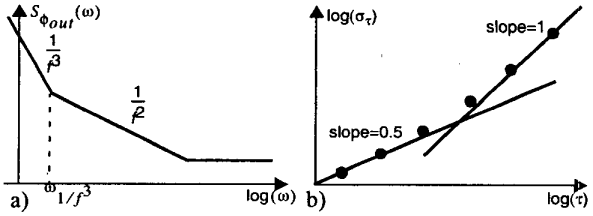

Fig. 4. Typical a) phase noise and b) timing jitter of a free running VCO.

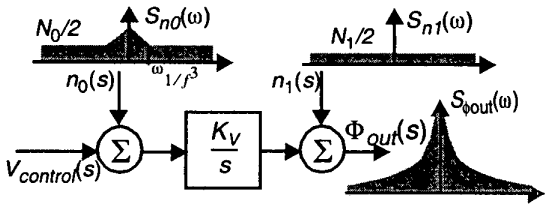

Fig. 5. Equivalent model for the phase noise of a VCO.

additional region with a slope of one [49], as shown in Fig. 4a, which is the time-domain counterpart of Fig. 4b.

The noise properties of a VCO can be modeled using a noiseless VCO with an additive noise source at its input and output, as shown in Fig. 5. The input source, $n_0(s)$, has white and $1/f^2$ noise portions that will generate the $1/f^2$ and $1/f^3$ regions in the output spectrum. This result can be easily understood noting that the VCO acts as an ideal integrator. The output source, $n_1(s)$, models the noise floor shown in Fig. 4. The output power spectrum can be calculated in terms of the input power spectrum, *i.e.*,

$$S_{\phi_{out}}(\omega) = \left|\frac{K_V}{j\omega}\right|^2 S_n(\omega) + \frac{N_1}{2} = \frac{K_V^2 N_0}{2\omega^2}\left(1 + \frac{\omega_{1/f^3}}{\omega}\right) + \frac{N_1}{2} \quad (5)$$

where $N_0/2$ and $N_1/2$ are the double-sideband power spectral densities of the input and output white noise sources, $n_0(s)$ and $n_1(s)$, and ω_{1/f^3} is the $1/f$ noise corner of the input behavioral noise source, $n_0(s)$, that is equal to the $1/f^3$ noise corner of the VCO. Note that ω_{1/f^3} is not equal to the actual device $1/f$ noise corner and is generally smaller [44]. For a given VCO, parameters $N_0/2$, $N_1/2$, and ω_{1/f^3} are chosen so that $S_{\phi out}(\omega)$ corresponds to the correct numerical value of VCO phase noise at all offset frequencies.

It should be noted that the spectrum of the output voltage is related to the spectrum of the phase through a nonlinear phase modulation and for that reason the spectrum of the output voltage will not grow without bound as does the spectrum of the $\phi_{out}(\omega)$.

Frequency Divider Noise

The frequency divider in the feedback path may have a significant contribution to the total phase noise of the PLL depending on its implementation and other properties of the loop. If an input with a fundamental frequency term, $\cos[\omega t + \phi(t)]$, is applied to an ideal $1/N$ frequency divider, the output will have a fundamental component of $\cos[\omega t/N + \phi(t)/N]$. Therefore, an ideal frequency divider reduces the *inherent* phase noise of the input signal by a factor of $20\log(N)$. However, it does not reduce the noise floor of the VCO induced by additive white noise, such as that of $n_1(s)$ in Fig. 5, as it does not appear in the argument of the cosine function and is not attenuated.

Real world frequency dividers introduce noise in excess of the noise generated by the VCO. Particularly, digital counters can introduce significant additive noise in the form of white and $1/f$ noise, when used as frequency dividers [35]-[43]. A frequency divider cannot directly introduce integrated noise (*i.e.*, $1/f^2$ and $1/f^3$ noise) as its noise sources are outside the feedback loop of the VCO.

Due to their resonant nature, analog regenerative [19]-[31] and injection-locked [32]-[34] dividers are generally less noisy than their digital synchronous and asynchronous counterparts. Unfortunately, unlike digital dividers, they are not capable of providing large and/or programmable division ratios. Re-synchronization can be used to lower the introduced noise of a digital dividers but cannot eliminate it completely [35].

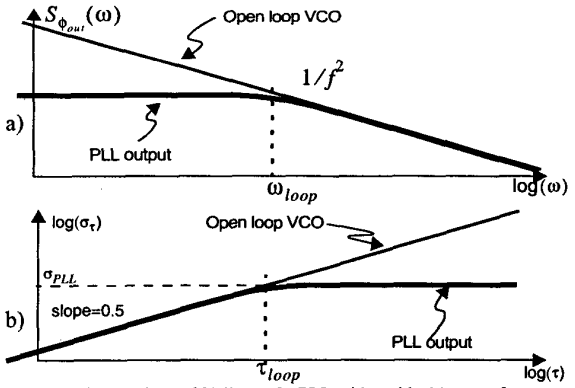

Fig. 6. a) Phase noise and b) jitter of a PLL with an ideal input reference and noisy VCO.

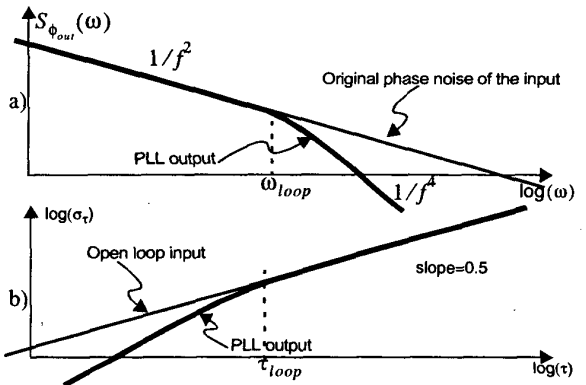

Fig. 7. a) Phase noise and b) jitter of a PLL with and ideal VCO and noisy input.

The excess noise of a digital divider can be modeled as an additive noise source at its output, as shown later in Fig. 11. In a PLL, this noise usually appears directly at the input of the phase detector and experiences the same transfer function as the noise on the input terminal.

Phase Detector Noise

Mostly due to their lower frequency of operation, phase detectors can be designed in such a way to contribute small amount of noise to the PLL. However, if special attention is not paid to their design, PDs will be still susceptible to noise, particularly, $1/f$ noise, substrate and supply noise. Usually, the phase detector is not a major source of noise in a PLL. Their noise properties have been studied to some extent in [9] and [18].

Phase Noise and Jitter in PLLs

Having studied the essential features of PLLs and the noise properties of their building blocks, the noise properties of PLLs can be analyzed. We start by investigating first-order loops with no dividers and then extend the analysis to the more general case of a higher-order loop with frequency division.

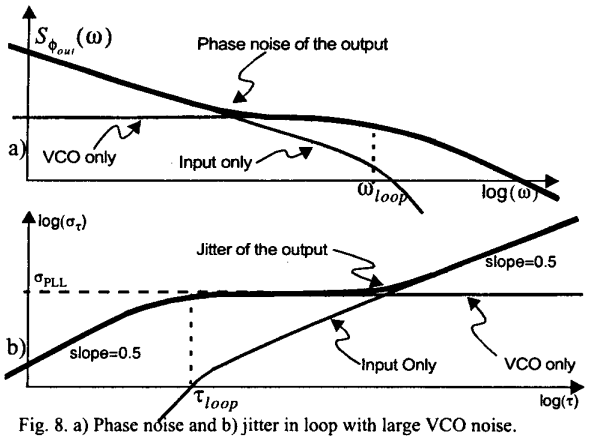

Fig. 8. a) Phase noise and b) jitter in loop with large VCO noise.

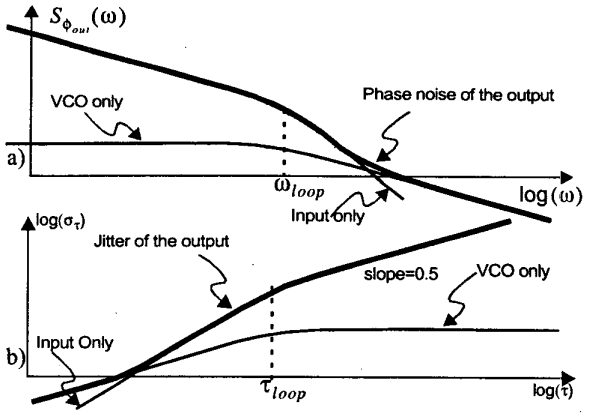

Fig. 9. a) Phase noise and b) jitter in loop with large input reference noise.

Phase Noise and Jitter in First Order Loops

A first order phase-locked loop with no divider can be analyzed using the equivalent block diagram of Fig. 1b with $H(s) = 1$ and $N = 1$. Assuming an ideal phase detector[1], there are two sources of noise which affect the phase noise of the output, Φ_{out}, namely, VCO phase noise and the phase noise of the input. Assuming that the phase noise of the input is not correlated with the phase noise of the VCO, the phase noise power spectrum at the output can be calculated using superposition. In other words, the output spectrum due to each source can be evaluated independently and the total phase noise will be given by their sum. The lack of correlation between the phase noise of the VCO and the input is a reasonable assumption, as long as they are generated by independent physical processes. If both of them share the same dominant source of noise, such as substrate and supply noise, there will be correlations and this assumption will fail.

Assuming a noiseless input and assuming that the VCO noise is dominated by its $1/f^2$ noise, the effect of VCO phase noise can be calculated using the transfer function from $n_0(s)$ to $\Phi_{out}(s)$, which is

$$\frac{\Phi_{out}(s)}{n_0(s)} = \frac{K_V}{K_P K_V + s} \tag{6}$$

and therefore,

$$S_{\phi_{out}}(\omega) = \frac{N_0}{2}\frac{K_V^2}{(K_P K_V)^2 + \omega^2} \tag{7}$$

which is shown in Fig. 6a. The effect of $1/f^3$ noise and the noise floor can be taken into account in a similar fashion. Comparing (5) and (7), it is evident that the phase noise of the output is the same as the phase noise of the VCO for offset frequencies larger than ω_{loop}. This should be intuitively clear as the loop adjusts VCO's control voltage to compensate for its slow random variations which are slower than loop's dynamics. However, it is unable to react fast enough to fast random changes in the VCO output and hence, they appear directly on the output, as can be seen in Fig. 6a.

The time domain view of this concept is shown in the timing jitter vs. delay graph of Fig. 6b. As mentioned earlier, in an open loop oscillator the timing jitter grows without bound as the delay from the reference edge, τ, increases. However, in a phase locked loop, timing jitter does not increase for the time scales larger than loop time constant, τ_{loop}, [47] because the feedback adjusts the VCO control voltage so that the VCO phase follows the input jitter, as shown in Fig 6b. The amount of jitter at the plateau is usually referred to as the PLL jitter and is shown with σ_{PLL} hereafter.

An actual expression for jitter vs. τ in a PLL can be obtained using the Khinchin theorem relating power spectral density to autocorrelation function [49]. It can be shown that in a first order PLL with a bandwidth of ω_{loop}, the timing jitter is related to τ through

$$\sigma_\tau^2 = \frac{NK_V^2}{2\omega_0^2}\cdot\frac{1}{\omega_{loop}}\cdot(1 - e^{-\omega_{loop}\tau}) \tag{8}$$

where ω_0 is the center frequency of the output. For $\tau \ll \tau_{loop}$, (8) reduces to

$$\sigma_\tau^2 = \frac{NK_V^2}{2\omega_0^2}\cdot\tau \tag{9}$$

as shown in Fig. 6b.

Now let us assume a noiseless VCO and evaluate the response of the loop to the phase variations in the input, Φ_{in}. The input is usually generated by another oscillator, which will have its own phase noise characteristics. Taking into account only the phase noise in the $1/f^2$ region, its power spectrum can be written as $S_{\phi_{in}}(\omega) = \alpha/\omega^2$, where α is a constant characterizing the phase noise of the input. Using (2), the power spectrum of the output is easily calculated

$$S_{\phi_{out}}(\omega) = \frac{\alpha}{\omega^2}\cdot\frac{\omega_{loop}^2}{\omega_{loop}^2 + \omega^2} \tag{10}$$

which has the power spectrum shown in Fig. 7a. The corresponding time domain picture is shown in Fig. 7b.

1. Effect of phase detector non-ideality has been discussed in [6].

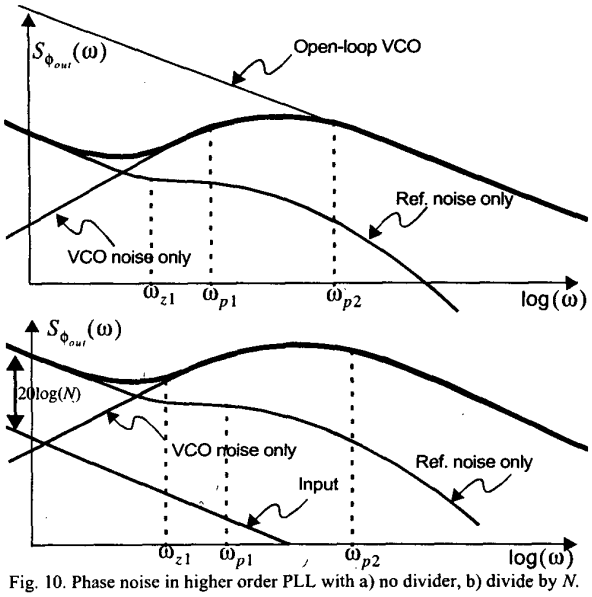

Fig. 10. Phase noise in higher order PLL with a) no divider, b) divide by N.

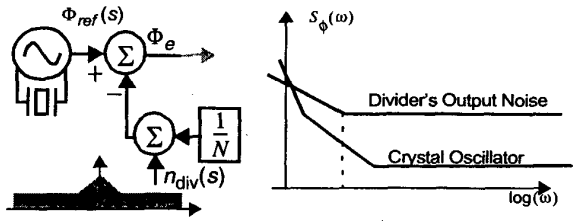

Fig. 11. Equivalent model for frequency divider noise.

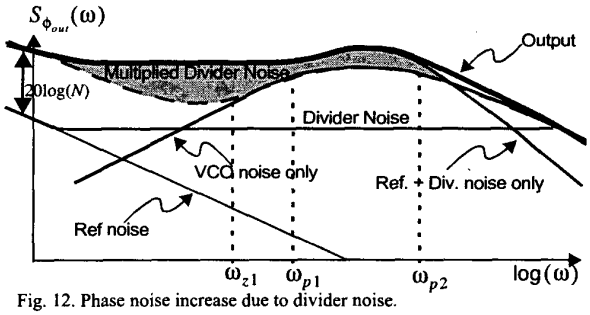

Fig. 12. Phase noise increase due to divider noise.

The phase noise of the input can be larger or smaller than the phase noise of the VCO depending on the application in which the PLL is being used. In applications such as microprocessor clock distribution and frequency synthesis, the input usually has a much smaller phase noise than the VCO, and therefore the total effective output phase noise of the PLL will have a shape similar to that of Fig. 8a. Generally PLL phase noise is dominated by the input phase noise for small offset frequencies and by the VCO phase noise for large frequency offsets. Phase noise pedestals, such as the one in Fig. 8a are common in synthesizers outputs. Fig. 8b shows timing jitter vs. delay, τ, for this case. Note that if the input signal has better frequency stability compared to the internal time base used in the phase noise/jitter measurement system, phase noise at low offsets (jitter at large delay times) will be dominated by the phase noise (jitter) of the measurement system.

In certain other applications, such as clock recovery, the phase noise of the input signal can be comparable to, or even larger than, the phase noise of the VCO. If this is the case, the phase noise spectrum and timing jitter of the output can have a different shape, as shown in Fig. 9a and b.

Jitter and Phase Noise in Higher-Order Loops

Once phase noise behavior in the first order loop is understood, it is easy to extend the concept to higher order loops. Consider the example of a charge-pump PLL with a compensation zero described by the phase transfer function (4). The transfer function from VCO input noise to output phase is easily calculated to be

$$\frac{\Phi_{out}(s)}{n_0(s)} = \frac{2\pi C_P N}{I} \cdot \frac{s}{s^2 / \left(\frac{K_V I}{2\pi C_P N}\right) + \tau_z s + 1} \tag{11}$$

The output phase noise spectrum with a noiseless input signal can be calculated in a fashion similar to (7). It will have a spectrum similar to the one shown in Fig. 10a. The transfer function for the input noise is given by (4). Therefore, the overall phase noise at the output of a PLL with no divider will have the form of 10a. As can be seen, the phase noise is still dominated by the VCO at large offset frequencies and by the input at small offsets. The bump in the phase noise spectrum of the output is usually referred to as *jitter peaking*.

Noise Contribution of the Frequency Divider

Assuming that the phase detector is not a major source of noise in the PLL, the input phase variations are multiplied by N at the output. Therefore the phase noise power spectrum of the output at low offset frequencies will be N^2 times the input phase fluctuations and hence the effect of an *ideal* frequency divider is to increase the phase noise of the input by a factor of 20log(N).

Digital dividers usually have a large white noise floor at their output. In the case of a frequency synthesizer, this white noise directly adds to the noise of the crystal reference at the input of the phase detector, as shown in Fig. 11. Therefore, it can be modeled as an artificially large white noise floor for the crystal reference. If the divider is implemented using active devices with large $1/f$ noise, it may even swamp the noise of the reference completely. This scenario is schematically shown in Fig. 11b. The output phase noise of a PLL with a frequency divider can be determined using these parameters. One such example is shown in Fig. 12.

The foregoing discussions demonstrate the noise properties of a PLL and the effects of various building blocks on its performance. The companion analytical/graphical time/frequency approach can be extended to analyze noise in other more sophisticated PLLs.

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