CMOS Bandgap References With Self-Biased Symmetrically Matched Current–Voltage Mirror and Extension of Sub-1-V Design

Yat-Hei Lam, *Member, IEEE*, and Wing-Hung Ki, *Member, IEEE*

***Abstract*—A series of bandgap references (BGRs) using a self-biased symmetrically matched current–voltage mirror (SM CVM) in reducing systematic offset, thus achieving an excellent line regulation, is presented. By replacing the operational amplifier with a CVM in the feedback loop, current consumption is much reduced. An SM buffer stage that is capable of driving a resistive load with minor degradation in temperature coefficient (TC) and line regulation is also presented. The technique is extended to design a sub-1-V BGR with a TC-cancellation output buffer. All circuits are designed using a 0.35-μm CMOS process, and experimental results are presented, confirming the analysis.**

***Index Terms*—Bandgap reference (BGR), CMOS, line regulation, self-biased, symmetrical matching (SM).**

I. Introduction

IN MANY SYSTEMS, a voltage reference that is independent of temperature, power supply, and load variations is essential. Bandgap references (BGRs) inspired by Widlar [1] and Brokaw [2] are extensively employed. They combine the correct ratio of the negative temperature coefficient (TC) of the base–emitter voltage of a bipolar transistor and the positive TC of the thermal voltage to achieve a temperature-stable voltage that is related to the bandgap voltage of silicon. In standard CMOS processes, only parasitic bipolar transistors are available [3], and in an n-well process, for example, the collector terminal of these parasitic p-n-p transistors has to be connected to ground. Under this restriction, the generic topology of a CMOS BGR takes the form shown in Fig. 1. The following observations are in place.

1) The operational amplifier (opamp) consumes power that may be a constraint for ultralow-power (in microwatts) applications.
2) Transistors $\mathrm{Q_1}$ and $\mathrm{Q_2}$ and resistor $\mathrm{R_1}$ constitute a proportional-to-absolute-temperature (PTAT) loop if $V_X = V_Y$, and the matching accuracy is affected by the offset voltage of the opamp.
3) The channel length modulation of $\mathrm{M_{p1}}$ and $\mathrm{M_{p2}}$ affects the matching accuracy of I_X and I_Y. A second $\mathrm{R_2}$ could be inserted in the I_Y branch for better matching, but it would take up much silicon area.
4) The bandgap voltage V_{BG} cannot be used to drive a resistive load.
5) The common-mode voltage of the opamp of around 0.6 V at V_X and V_Y makes it difficult to operate with a sub-1-V supply voltage [4].

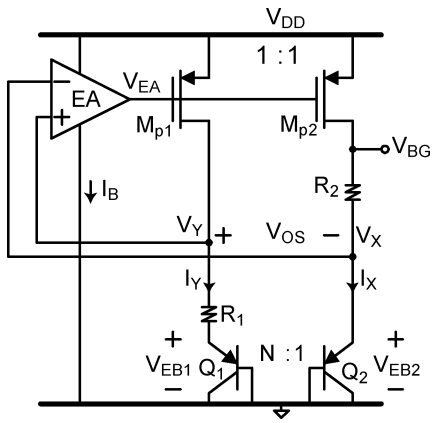

Fig. 1. Generic topology of CMOS bandgap voltage reference.

In this paper, we propose new circuit techniques in improving a BGR's power supply rejection (PSR) and ability to drive a resistive load. Section II discusses the use of a well-known four-transistor (4T) cell to replace the opamp in Fig. 1[3], [5]. Power is reduced but matching is compromised. PSR or power supply sensitivity of offset current, offset voltage, and bandgap voltage are computed to serve as references for comparison. Section III introduces the principle of symmetrical matching (SM) in reducing systematic offset and enhancing PSR. It is illustrated by an SM 8T cell in minimizing the mismatch of the 4T cell. Section IV presents the design of a series of BGRs based on the 8T cell. The first is labeled SMI (I stands for integrated TC cancellation) BGR. It integrates $\mathrm{R_2}$ into the 8T cell to save a third current branch for power reduction. The second is labeled SMB (B stands for buffered output) BGR. It has an output buffer with TC cancellation for driving resistive load, and the buffer design is based on the SM principle without using an opamp. The third is labeled LV-SMB BGR that could operate with a

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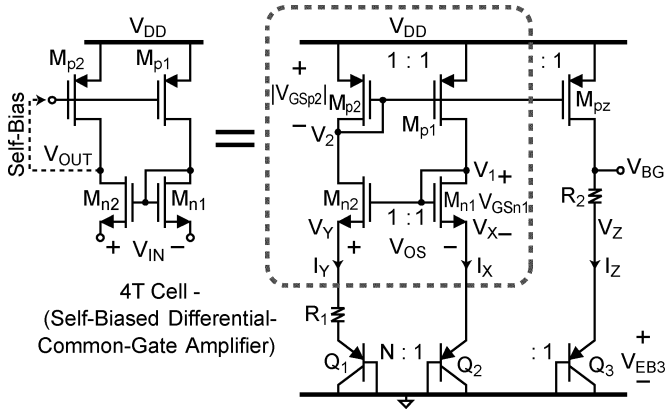

Fig. 2. BGR with 4T cell (4T BGR).

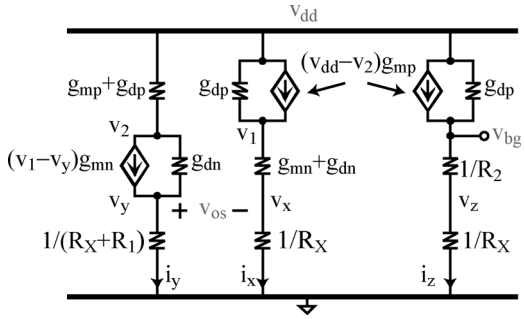

Fig. 3. Small-signal model of the 4T BGR.

supply voltage below 1 V. It makes use of the 8T cell as a transimpedance amplifier (TIA) with input currents injected from folded resistor strings. It also has an SM output buffer with TC cancellation for driving resistive load. The BGRs are designed using a 0.35-μm CMOS process. Section V presents experimental results on temperature performance, line regulation, PSR, and load transient responses of the fabricated BGRs, and Section VI concludes our research efforts.

II. 4T BGR

With reference to Fig. 1, the feedback loop constructed by $\mathrm{M_{p1}}, \mathrm{M_{p2}}$, and the error amplifier (EA) forces $I_X = I_Y$ and $V_X = V_Y$. The input common-mode voltage $V_X = V_Y$ is too low for an nMOS common-source differential pair with normal threshold voltage, and a pMOS input stage should be used instead [4]. An output stage is needed to provide the V_{DD}-referenced gate drives for $\mathrm{M_{p1}}$ and $\mathrm{M_{p2}}$. The two stages are not stackable, and their biasing currents cannot be shared. Moreover, the current consumed by the EA is not reused by $\mathrm{Q_1}$ and $\mathrm{Q_2}$. For a fixed current budget, tradeoffs in allocating biasing currents to the EA (I_B) and the PTAT loop (I_X and I_Y) have to be made.

Instead of using an opamp, a 4T self-biased cell could be stacked on $\mathrm{Q_1}$ and $\mathrm{Q_2}$, as shown in Fig. 2[3], [5]. We label it *4T BGR*. The 4T cell serves as a self-biased differential common-gate amplifier (D-CGA), and its biasing current is reused to bias $\mathrm{Q_1}$ and $\mathrm{Q_2}$. The 4T cell is justifiably called a *current-voltage mirror* (CVM) because of the following reasons: 1) $\mathrm{M_{p1}}$ and $\mathrm{M_{p2}}$ serve as a current mirror, forcing $I_X = I_Y$, and 2) $\mathrm{M_{n1}}$ and $\mathrm{M_{n2}}$, with their gates being connected together and with the same drain currents, serve as a voltage mirror, forcing $V_Y = V_X$. In fact, the PTAT currents I_X and I_Y could only be generated accurately when $V_X = V_Y$. The transistors $\mathrm{M_{n1}}$ and $\mathrm{M_{p2}}$ are diode connected to ensure an overall loop with negative feedback. An additional current branch ($\mathrm{M_{pz}}$, $\mathrm{R_2}$, and $\mathrm{Q_3}$) is necessary for TC cancellation because the 4T cell has occupied the original location of $\mathrm{R_2}$. The $\mathrm{M_{pz}}$ branch, in general, consumes less current than an opamp.

From Fig. 2, it is clear that, except when $V_{\mathrm{DD}} = V_{\mathrm{BE2}} + V_{\mathrm{GSn1}} + |V_{\mathrm{GSp2}}|$ (such that $V_1 = V_2$), the V_{DS}'s of the paired transistors $(\mathrm{M_{p1}}, \mathrm{M_{p2}})$ and $(\mathrm{M_{n1}}, \mathrm{M_{n2}})$ are different. Channel length modulation makes I_X slightly different from I_Y and leads to error in the V_{GS}'s of $\mathrm{M_{n1}}$ and $\mathrm{M_{n2}}$, which translates to systematic offset error at V_X and V_Y. This offset voltage $V_{\mathrm{OS}} = V_Y - V_X$ can be improved by cascoding transistors [5], [6]. However, the minimum supply voltage of the modified BGR has to be higher. Regulating the supply voltage to the BGR could also help but with extra power consumed by the supply regulator [7], [8]. Now, with V_{OS} not equal to 0 V, the inaccurate mirrored current affects the accuracy of the bandgap voltage, resulting in poor line regulation. Computing line and load regulation ($\Delta V_{\mathrm{BG}}/\Delta V_{\mathrm{DD}}$ and $\Delta V_{\mathrm{BG}}/\Delta I_o$) amounts to solving a set of nonlinear simultaneous equations, and not much insight could be obtained. Hence, these quantities are usually obtained by measurement. The PSR of the bandgap voltage $v_{\mathrm{bg}}/v_{\mathrm{dd}}$ could give some ideas on the line regulation as it is usually a weak function of the supply voltage. The PSRs of the offset voltage $v_{\mathrm{os}}/v_{\mathrm{dd}}$ and the offset current $i_{\mathrm{os}}/v_{\mathrm{dd}}$ are computed as intermediate steps in obtaining $v_{\mathrm{bg}}/v_{\mathrm{dd}}$ and, more importantly, for evaluating the performance of both current and voltage mirroring of the CVM. To compute the aforementioned quantities, we need the small-signal model of the 4T BGR with v_{dd} as an input, which is shown in Fig. 3. The transistors $\mathrm{M_{p1}}$, $\mathrm{M_{p2}}$, and $\mathrm{M_{pz}}$ have the same W and L, and so do their g_{mp} and r_{dsp}. Similarly, $\mathrm{M_{n1}}$ and $\mathrm{M_{n2}}$ have the same g_{mn} and r_{dsn}.

To simplify the analysis, we define $g_{\mathrm{dp,n}} = 1/r_{\mathrm{dsp,n}}$. The KCL equations are

$$\begin{aligned} i_x &= (v_{\mathrm{dd}} - v_2)g_{\mathrm{mp}} + (v_{\mathrm{dd}} - v_1)g_{\mathrm{dp}} \\ &= \frac{v_1}{R_x + \frac{1}{g_{\mathrm{mn}}+g_{\mathrm{dn}}}} = \frac{v_x}{R_x} \end{aligned} \tag{1}$$

$$\begin{aligned} i_y &= (v_{\mathrm{dd}} - v_2)(g_{\mathrm{mp}} + g_{\mathrm{dp}}) \\ &= (v_1 - v_y)g_{\mathrm{mn}} + (v_2 - v_y)g_{\mathrm{dn}} = \frac{v_y}{R_x + R_1} \end{aligned} \tag{2}$$

$$i_z = (v_{\mathrm{dd}} - v_2)g_{\mathrm{mp}} + (v_{\mathrm{dd}} - v_{\mathrm{bg}})g_{\mathrm{dp}} = \frac{v_{\mathrm{bg}}}{R_x + R_2} \tag{3}$$

where R_x is the dynamic resistance of $\mathrm{Q_1}$, $\mathrm{Q_2}$, and $\mathrm{Q_3}$, because they have essentially the same bias currents. Solving v_x and v_y in terms of v_{dd} soon becomes too involved because they are numerically very close to each other, and inappropriate approximation would make $v_{\mathrm{os}} = v_y - v_x$ to be off by a large margin. Whenever approximation could be invoked, we note that, for our designs, g_{mn} and g_{mp} are on the order of 50 μA/V, and r_{dsn} and r_{dsp} are on the order of 10 MΩ, such that $g_m r_{\mathrm{ds}}$ and $g_m R_x$ are on the order of 500 and 1, respectively. After solving the simultaneous equations, the PSR of V_{OS} is given by

$$\frac{v_{\rm os}}{v_{\rm dd}} \cong \frac{1}{g_{\rm mn}(r_{\rm dsp}||r_{\rm dsn})}. \tag{4}$$

Also, for $i_{\rm os} = i_y - i_x$, we have

$$\frac{i_{\rm os}}{v_{\rm dd}} \cong \frac{1}{r_{\rm dsp}}. \tag{5}$$

Equation (5) shows that the PSR of $I_{\rm os}$ depends on the channel length modulation of the pMOS pair $\rm M_{p1}$ and $\rm M_{p2}$. The PSR of the bandgap voltage is given by (6)

$$\begin{aligned}\frac{v_{\rm bg}}{v_{\rm dd}} &\cong (R_2+R_x)\left(\frac{\alpha}{R_1}\frac{v_{\rm os}}{v_{\rm dd}} + \frac{1}{r_{\rm dsp}+R_2+R_x}\right)\\ &\cong (R_2+R_x)\left(\frac{\alpha}{R_1 g_{\rm mn}(r_{\rm dsp}||r_{\rm dsn})}\right.\\ &\qquad \left. + \frac{1}{r_{\rm dsp}+R_2+R_x}\right)\end{aligned} \tag{6}$$

where

$$\alpha = 1 + g_{\rm mn}R_x\frac{r_{\rm dsp}||r_{\rm dsn}}{r_{\rm dsp}} > 1. \tag{7}$$

The PSR of $V_{\rm BG}$ depends on two terms/mechanisms. First, the bipolar transistors $\rm Q_1$ and $\rm Q_2$ have the same dynamic resistance of R_x, and the $V_{\rm OS}$ variation w.r.t. $V_{\rm DD}$ is, in fact, effectively acting on R_1, resulting in significant PTAT current variation w.r.t. $V_{\rm DD}$ that is mirrored to the output through $\rm M_{pz}$. Second, the finite output resistance of $\rm M_{pz}$ contributes to the second term of $(R_2+R_x)/(r_{\rm dsp}+R_2+R_x)$.

For the 0.35-μm CMOS process used in this design, $|V_{\rm tp}| \approx$ 750 mV at 5 °C, $V_{\rm EB2} \approx$ 0.7 V, and $V_{\rm DS(sat)} \approx$ 50 mV, and the 4T BGR is functional for $V_{\rm DD} >$ 1.75 V. From the measurement result of a fabricated 4T BGR, with $V_{\rm DD} =$ 2.5 V, the bandgap voltage $V_{\rm BG}$ shows a low-temperature dependence of 12.85 ppm/°C ($\Delta V_{\rm BG} =$ 1.39 mV out of $V_{\rm BG} =$ 1.2 V for a range of 5 °C–95 °C). However, the line regulation of the bandgap voltage $\Delta V_{\rm BG}/\Delta V_{\rm DD}$ is 28 mV/V ($\Delta V_{\rm BG} =$ 49 mV for $\Delta V_{\rm DD} =$ 3.5 V − 1.75 V = 1.75 V) and is relatively high. More measurement results will be presented in Section V.

III. BGRs Using Self-Biased SM CVM

The current and voltage mirroring of the 4T BGR is poor due to the systematic mismatches of both the current and the voltage. These mismatches are supply voltage dependent and cannot be eliminated completely by postfabrication trimming techniques. Note that when two transistors $\rm M_1$ and $\rm M_2$ of the same type are matched, their W/L ratios are the same, i.e., $(W/L)_1 = (W/L)_2$, and in most cases, $W_1 = W_2$ and $L_1 = L_2$. However, their drain currents may not be the same due to channel length modulation. If, in addition to having the same W/L ratio, $\rm M_1$ and $\rm M_2$ are forced to have essentially the same drain, gate, and source voltages, then they are called symmetrically matched (SM), and the matching between their drain currents is much better than that in the previous case. To enhance the matching accuracy of the CVM, 8T self-biased *SM CVMs* were proposed [9], [10]. Fig. 4 shows an improved BGR using a self-biased SM CVM and is labeled *SM BGR*. Similar to the 4T CVM of the 4T BGR, the SM CVM reuses the PTAT currents I_X and I_Y to achieve low current consumption. Note that all BGRs need a startup circuit, and the start-up circuit discussed in [9] could be used.

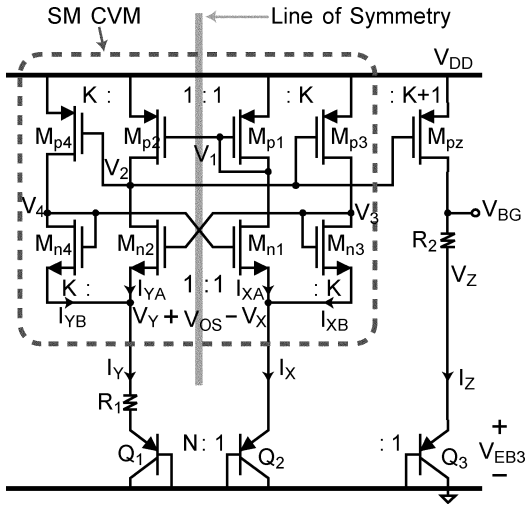

Fig. 4. Improved BGR with SM CVM.

The dc analysis of the SM CVM is as follows. When the PTAT loop is activated, the current I_X that flows in $\rm Q_2$ is equal to $I_{\rm XA} + I_{\rm XB}$. The W/L ratio of $\rm M_{p1}$ and $\rm M_{p3}$ is 1: K, and $I_{\rm XB}$ is approximately equal to $K \times I_{\rm XA}$. To provide the correct gate drive for $\rm M_{p3}$, the feedback action of the SM CVM drives V_2 to be essentially equal to V_1. Now, with the $V_{\rm SG}$ of $\rm M_{p1}$ being equal to the $V_{\rm SG}$ of $\rm M_{p2}$, $\rm M_{p1}$ is then symmetrically matched to $\rm M_{p2}$. Arguing in a similar fashion, we conclude that all transistor pairs $(\rm M_{n1}, M_{n2})$, $(\rm M_{p1}, M_{p2})$, $(\rm M_{n3}, M_{n4})$, and $(\rm M_{p3}, M_{p4})$ are symmetrically matched, and thus, $V_Y = V_X$. Note that, unless $V_{\rm DD} = V_{\rm EB2} + V_{\rm GSn3} + |V_{\rm GSp1}|$, $I_{\rm XB}$ is not exactly equal to $K \times I_{\rm XA}$ because V_3 is then not equal to V_1. Nevertheless, $I_{\rm XA}$ matches well with $I_{\rm YA}$, and $I_{\rm XB}$ with $I_{\rm YB}$, such that $I_X = I_{\rm XA} + I_{\rm XB} = I_{\rm YA} + I_{\rm YB} = I_Y$. It is evident that the SM CVM has a line of symmetry (the gray line in Fig. 4) and that I_X, $I_{\rm XA}$, $I_{\rm XB}$, V_X, V_1, and V_3 are matched with I_Y, $I_{\rm YA}$, $I_{\rm YB}$, V_Y, V_2, and V_4, respectively. To generate the BGR voltage $V_{\rm BG}$, the PTAT current I_X $(= I_Y)$ is mirrored out using $\rm M_{pz}$ such that $\rm M_{p1,2} : M_{pz} = 1 : K + 1$. With $\rm Q_2 : Q_3 = 1 : 1$, V_Z is then essentially the same as V_X, and $V_{\rm BG}$ is given by

$$V_{\rm BG} = V_{\rm EB3} + \frac{R_2}{R_1}\ln(N) \times V_T \tag{8}$$

where N is the size ratio of $\rm Q_1/Q_2$ and $V_{\rm T}$ is the thermal voltage.

The core transistors $\rm M_{n1}$, $\rm M_{n2}$, $\rm M_{p1}$, and $\rm M_{p2}$ constitute a D-CGA with $v_{\rm os} = v_y - v_x$ as input and v_2 as output. The outer transistors $\rm M_{n3}$, $\rm M_{n4}$, $\rm M_{p3}$, and $\rm M_{p4}$ serve as level shifters to provide the gate drives for the common-gate differential pair $\rm M_{n1}$ and $\rm M_{n2}$ and, through feedback action, force $V_2 = V_1$ to reduce systematic offset. For computing $v_{\rm os}/v_{\rm dd}$, we refer to the small-signal model of the SM BGR shown in Fig. 5.

The W/L ratio of $\rm M_{n1,2} : M_{n3,4}$ is 1: K, and that of $\rm M_{p1,2} : M_{p3,4} : M_{pz}$ is $1 : K : K + 1$, so

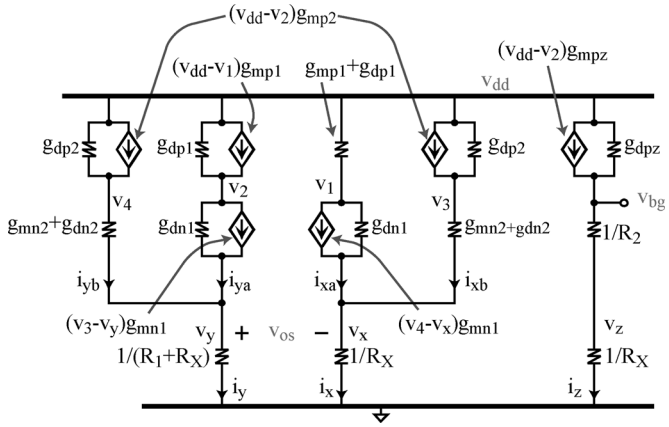

Fig. 5. Small-signal model of the improved BGR with SM CVM.

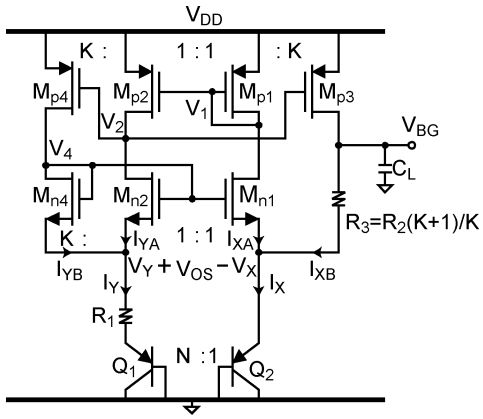

Fig. 6. Proposed SMI BGR.

$$g_{\rm mpa} : g_{\rm mpb} : g_{\rm mpz} = g_{\rm dpa} : g_{\rm dpb} : g_{\rm dpz} = 1 : K : K+1. \tag{9}$$

A similar relation holds for $g_{\rm mn}$'s and $g_{\rm dn}$'s. The offset voltage equation is

$$v_{\rm os} = v_y - v_x = (i_{\rm ya} - i_{\rm xa} + i_{\rm yb} - i_{\rm xb})R_x + (i_{\rm ya} + i_{\rm yb})R_1 \tag{10}$$

with $i_{\rm os} = i_{\rm osa} + i_{\rm osb} = (i_{\rm ya} - i_{\rm xa}) + (i_{\rm yb} - i_{\rm xb})$. It is trivial in relating paired parameters to $v_{\rm os}$, e.g.,

$$\begin{aligned} i_{\rm osa} &= i_{\rm ya} - i_{\rm xa} \\ &= -v_{\rm os}\left[(2-\delta)g_{\rm mn1} + g_{\rm dn1}\right]\frac{g_{\rm dp1}}{g_{\rm dp1} + g_{\rm dn1}} \end{aligned} \tag{11}$$

$$\begin{aligned} i_{\rm osb} &= i_{\rm xa} - i_{\rm xb} \\ &= -v_{\rm os}(g_{\rm mn2} + g_{\rm dn2})\delta \end{aligned} \tag{12}$$

where

$$\delta = \frac{g_{\rm dp1,2}}{g_{\rm mn1,2} + g_{\rm dn1,2} + g_{\rm dp1,2}}. \tag{13}$$

The offset current of the inner branches $i_{\rm osa}$ and that of the outer branches $i_{\rm osb}$ are on the order of $g_{\rm mn1}v_{\rm os}$ and $g_{\rm dp2}v_{\rm os}$, respectively. It is clear that the overall offset current $i_{\rm os} = i_y - i_x$ is mostly due to the inner branches. To compute $v_{\rm os}/v_{\rm dd}$, however, is not trivial at all, and after extensive computation with appropriate approximations, we have

$$\frac{v_{\rm os}}{v_{\rm dd}} \cong \frac{1}{2g_{\rm mp1}g_{\rm mn1}(r_{\rm dsp1} \| r_{\rm dsn1})^2} \tag{14}$$

$$\frac{i_{\rm os}}{v_{\rm dd}} \cong -\frac{1}{g_{\rm mp1}(r_{\rm dsp1} \| r_{\rm dsn1})r_{\rm dsp1}}. \tag{15}$$

Comparing (14) with (4) and (15) with (5), we conclude that the SM CVM gives a much better PSR of the offset voltage and current, and hence, the line regulation of the SM BGR is better. With the help of (14) and (15), the supply sensitivity of $v_{\rm bg}$ is computed as

$$\frac{v_{\rm bg}}{v_{\rm dd}} \cong \left(-\frac{1}{r_{\rm dspz}} - \frac{1}{r_{\rm dsn1}} + \frac{1}{r_{\rm dspz} + R_2 + R_x}\right)(R_2 + R_x). \tag{16}$$

In general, $r_{\rm dspz} \gg R_2 + R_x$. Therefore

$$\frac{v_{\rm bg}}{v_{\rm dd}} \approx -\frac{1}{r_{\rm dsn1}}(R_2 + R_x). \tag{17}$$

From (16), we learn that, with appropriate transistor sizing of $\rm M_{p1-4}$ and $\rm M_{pz}$, the loop dynamics of the SM BGR helps to cancel out the output resistance of $\rm M_{pz}$ and replaces it with that of $\rm M_{p1}$. If the SM BGR consumes the same power as the 4T BGR, then the $I_{\rm YA}$ in Fig. 4 is only $1/(K+1)$ of the I_Y in Fig. 2, and $r_{\rm dsp1} = (K+1)r_{\rm dspz}$. In our design, $K = 5$, and an improvement of the PSR of $V_{\rm BG}$ by 20 dB could easily be achieved.

IV. Practical BGR Designs With SM CVM

A. SMI BGR With Reduced Current

The three currents I_X, I_Y, and I_Z of the SM BGR are all PTAT currents. An immediate question for a current-efficient design is whether one of the branches could be eliminated. With reference to Fig. 4, we learn that $\rm M_{n1}$ and $\rm M_{n2}$ have similar gate voltages, and potentially, their gates can be connected together. If they are connected to V_4, then $\rm M_{n3}$ is left as a diode-connected transistor with a PTAT current of $I_{\rm XB}$. We may substitute $\rm M_{n3}$ with a resistor $\rm R_3$ that has the value of $R_2 \times (K+1)/K$ to generate the BGR voltage, as shown in Fig. 6, which is given by

$$V_{\rm BG} = V_{\rm EB2} + \frac{R_3}{R_1}\frac{K}{K+1}\ln(N) \times V_T. \tag{18}$$

This BGR has a TC-cancellation branch that consists of $\rm R_3$ integrated into the SM CVM cell, and it is labeled *SMI BGR*. The voltage drop across $\rm R_3$ is not exactly equal to the $V_{\rm GS}$ of $\rm M_{n3}$, and the SMI BGR is not as symmetrically matched as the SM BGR. However, both V_4 and $V_{\rm BG}$ are ground-referenced potentials, and simulation results show only minor performance deviation from the SM BGR. More importantly, the current consumption is reduced by 33%. One may suggest replacing $\rm M_{n4}$ (instead of $\rm M_{n3}$) with $\rm R_3$. However, the positive-feedback action on the right-hand side of the circuit ($\rm M_{p3} \rightarrow R_3 \rightarrow M_{n1} \rightarrow M_{p1} \rightarrow M_{p2}$) is attenuated by the filtering capacitor $\rm C_L$ and the

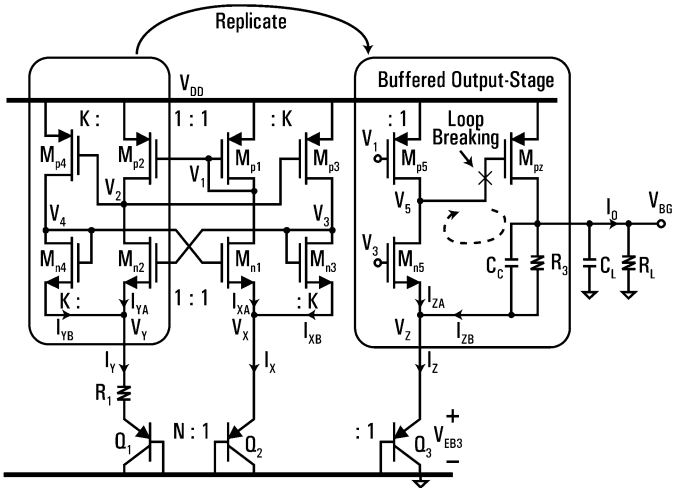

Fig. 7. Proposed SMB BGR.

BGR is stable, while replacing $\mathrm{M_{n4}}$ with $\mathrm{R_3}$ would make the system unstable.

B. SMB BGR With Buffered Output

The V_{BG} of the 4T and SMI BGRs cannot be used to drive any resistive load, and a buffer is needed if multiple voltages have to be derived from V_{BG} using a resistor divider. Instead of using an opamp with unity-gain feedback, a low-impedance output can be obtained by replicating and modifying half of the PTAT generator using the SM CVM, as shown in Fig. 7. This BGR is labeled *SMB BGR*. Transistors $\mathrm{M_{n5}}$ and $\mathrm{M_{p5}}$ are designed to have the same W/L ratios and gate voltages as $\mathrm{M_{n1}}$ and $\mathrm{M_{p1}}$, respectively, and $\mathrm{Q_3}$ has the same size as $\mathrm{Q_2}$. Now, $\mathrm{M_{n5}}$, $\mathrm{M_{p5}}$, and $\mathrm{Q_3}$ work as a CGA. In the steady state, V_1 and V_3 bias $\mathrm{M_{p5}}$ and $\mathrm{M_{n5}}$, respectively, to give $I_{\mathrm{ZA}} = I_{\mathrm{XA}}$, which could be satisfied only if $V_Z = V_X$. The transistor $\mathrm{M_{pz}}$ supplies both I_{ZB} and the load current I_O. Supposing that I_{ZB} is smaller than I_{XB} such that $I_Z < I_X$, then $V_Z < V_X$. With a larger gate drive voltage $V_{\mathrm{GSn5}} = V_3 - V_Z$, the drain current of $\mathrm{M_{n5}}$ would be larger than I_{XA}. As $\mathrm{M_{p5}}$ can only supply I_{XA}, so $\mathrm{M_{n5}}$ is forced to go into the triode region, and V_5 goes down. As V_5 drops, the gate drive of $\mathrm{M_{pz}}$ increases, sourcing more current to both R_3 and R_L. Therefore, in the steady state, I_{ZB} is regulated to be equal to I_{XB} to give $V_Z = V_X$. Hence, a unity-gain buffer is achieved by the CGA with feedback. More often, $\mathrm{M_{n5}}$, $\mathrm{M_{p5}}$, and $\mathrm{Q_3}$ are regarded to form a TIA, with the input being the current $I_{\mathrm{ZB}} = (V_{\mathrm{BG}} - V_Z)/R_3$ that is injected into V_Z. Zero TC is achieved if R_3 is set to be equal to $R_2 \times (K+1)/K$, and the bandgap voltage is given by (18), with V_{EB2} being replaced by V_{EB3}.

If the load resistance R_L is very large ($\rightarrow \infty$), we may design $(W/L)_{\mathrm{pz}}$ to be the same as $(W/L)_{\mathrm{p4}}$ such that $\mathrm{M_{pz}}$ and $\mathrm{M_{p4}}$ have the same current density, and V_5 matches well with V_2 to minimize systematic offset. In practice, a larger $(W/L)_{\mathrm{pz}}$ could be used to source a larger output current. In such a case, minimum channel length can be used for $\mathrm{M_{pz}}$ to minimize chip area and enhance the speed of the output buffer. Negative-feedback action in the buffer loop takes care of the larger channel length modulation by adjusting V_5 appropriately with a minor increase in systematic offset.

The output buffer requires frequency compensation. Loop breaking could be performed at V_5, as shown in Fig. 7. Without the compensation capacitor $\mathrm{C_c}$, the loop has two poles. The first pole p_1 is due to the drain impedance of $\mathrm{M_{n5}}$ and $\mathrm{M_{p5}}$ (r_{dsn5} and r_{dsp5}) and the gate capacitance of $\mathrm{M_{pz}}$ (C_{gz}) and is located at

$$p_1 = \frac{1}{C_{\mathrm{gz}}(r_{\mathrm{dsp5}} \| r_{\mathrm{dsn5}})}. \tag{19}$$

The second pole p_2 is due to the filtering capacitor $\mathrm{C_L}$ at the output of the SMB BGR and is located at

$$p_2 = \frac{1}{C_L\left[R_L \| \left(R_3 + \frac{1}{g_{\mathrm{mn5}}} \| R_x\right)\right]}. \tag{20}$$

These two poles could reduce the phase margin of the negative-feedback loop response close to 0° easily. Adding C_c introduces one zero z_c and one pole p_c to enhance the phase margin. With $C_c \ll C_L$ such that it does not alter p_2 too much, the additional zero z_c is located at

$$z_c = \frac{1}{C_c R_3} \tag{21}$$

while pole p_c is located at

$$p_c = \frac{1}{C_c\left(R_3 \| R_x \| \frac{1}{g_{\mathrm{mn5}}}\right)}. \tag{22}$$

Obviously z_c appears at a lower frequency than p_c. The additional zero can be placed around the unity-gain frequency of the feedback loop to increase the phase margin.

C. Low-Voltage SM BGR With Buffered Output

To generate the BGR voltage by running a PTAT current through a resistor in series with a diode (or diode-connected p-n-p transistor) requires a supply voltage that is larger than 1.3 V. One attempt of sub-1-V design is to fold the PTAT resistive branches of Fig. 1 downward and place them in parallel with the inverse PTAT diode voltages to generate a temperature-independent current to be mirrored to a third resistive branch [11]; however, this scheme cannot give a sub-1-V BGR without using a special process. As discussed in [12]–[14], the minimum supply voltage of the BGR is limited by the input common-mode range of the opamp. TIA was employed in [12] to overcome this restriction. However, an additional current compensation circuitry is needed to eliminate the current offset introduced by the finite dc input voltage of the TIA. In [13], the inputs of the opamp are connected to a lower voltage of the resistor strings to achieve the first sub-1-V BGR. In [14], unity-gain buffers are required, which consume extra current.

Here, we propose a low-power sub-1-V BGR that integrates the SM CVM and the common-gate buffer with the aforementioned techniques. It is labeled *LV-SMB BGR* (Fig. 8). The SM CVM, together with $\mathrm{R_{5B}}$ and $\mathrm{R_{6B}}$, can be treated as a self-biased SM TIA. Resistors $\mathrm{R_{5A}}$ and $\mathrm{R_{6A}}$ sense V_5 and V_6, respectively, and inject currents into the SM TIA. Since $\mathrm{R_{5A}} = \mathrm{R_{6A}}$ and $\mathrm{R_{5B}} = \mathrm{R_{6B}}$, the SM TIA forces $V_Y = V_X$, $I_{5\mathrm{A}} = I_{6\mathrm{A}}$, and

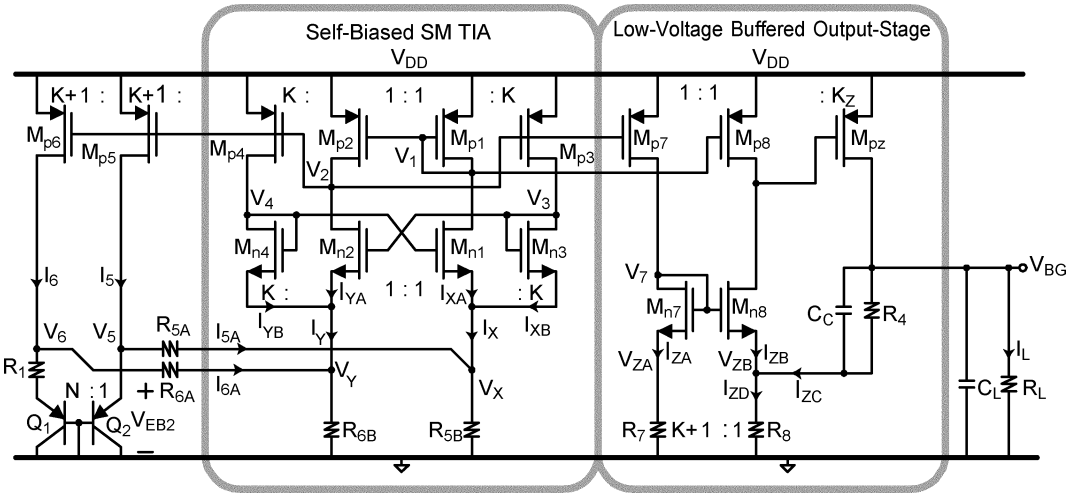

Fig. 8. Proposed LV-SMB BGR.

$V_5 = V_6$. The resistor dividers constructed by $\mathrm{R_{5A}}$, $\mathrm{R_{5B}}$, $\mathrm{R_{6A}}$, and $\mathrm{R_{6B}}$ effectively lower V_5 and V_6 to V_X and V_Y such that the SM CVM can operate at a lower V_{DD}. The dc input voltage of SM TIA at V_X and V_Y is given by

$$V_X = V_Y = \left(\frac{V_{\mathrm{EB2}}}{R_{5\mathrm{A}} + R_{5\mathrm{B}}} + I_{\mathrm{REF}}\right) R_{5\mathrm{B}} \tag{23}$$

where

$$I_{\mathrm{REF}} = I_X = I_Y = I_5 = I_6. \tag{24}$$

The transistors are sized according to the ratios shown in Fig. 8, and the temperature-independent reference current I_{REF} is given by

$$I_{\mathrm{REF}} = \frac{1}{R_{5\mathrm{A}} + 2R_{5\mathrm{B}}} \left[V_{\mathrm{EB2}} + \frac{R_{5\mathrm{A}} + R_{5\mathrm{B}}}{R_1} \ln(N) V_T\right]. \tag{25}$$

The proposed SM TIA is self-biased, and as shown in (25), the output current I_{REF} shows no dependence on the dc input voltages V_X and V_Y of the SM TIA. The LV-SMB BGR can operate at

$$V_{\mathrm{DD}} > \left(\frac{V_{\mathrm{EB2}}}{R_{5\mathrm{A}} + R_{5\mathrm{B}}} + I_{\mathrm{REF}}\right) R_{5\mathrm{B}} + |V_{\mathrm{tp}}| + V_{\mathrm{DS(sat)}}. \tag{26}$$

A buffered output stage similar to the one used in the SMB BGR is used to drive the resistive load. Transistors $\mathrm{M_{n7}}$ and $\mathrm{M_{p7}}$, together with $\mathrm{R_7}$, generate the appropriate bias for $\mathrm{M_{n8}}$. Since $\mathrm{R_7} : \mathrm{R_8} = K + 1 : 1$, so $I_{\mathrm{ZA}} = I_{\mathrm{XB}}/K = I_{\mathrm{YB}}/K$, giving $I_{\mathrm{ZA}} \approx I_{\mathrm{ZB}}$, and the TIA formed by $\mathrm{M_{p8}}$, $\mathrm{M_{n8}}$, and $\mathrm{R_8}$ senses V_{BG} through $\mathrm{R_4}$ and drives $\mathrm{M_{pz}}$ such that $V_{\mathrm{ZB}} = V_{\mathrm{ZA}}$ and $I_{\mathrm{ZC}} = K \times I_{\mathrm{ZB}} = I_{\mathrm{XB}} = I_{\mathrm{YB}}$. As a result, the output of the LV-SMB BGR is given by

$$V_{\mathrm{BG}} = I_{\mathrm{REF}} \left(\frac{K}{K+1} R_4 + R_8\right). \tag{27}$$

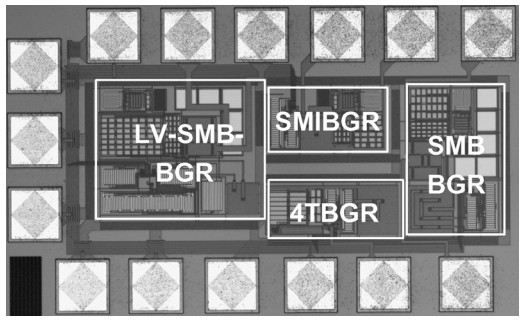

Fig. 9. Chip micrograph.

Similar to the design of the SMB BGR, a compensation capacitor $\mathrm{C_c}$ is needed to stabilize the buffered output stage.

V. Experimental Results

The 4T, SMI, SMB, and LV-SMB BGRs were designed and fabricated using a 0.35-μm CMOS process. The chip micrograph is shown in Fig. 9. To minimize channel length modulation, particularly for the 4T BGR, the transistor lengths were chosen to be $L = 7$ μm for all designs. All resistors were implemented by high-resistive poly resistors with a typical sheet resistance of 1.2 kΩ/sq. The first-order TC is -0.75×10^{-3}/K, and the second-order TC is 3.8×10^{-6}/K. The compensation capacitors $\mathrm{C_c}$'s in the SMB BGR and the LV-SMB BGR were implemented by poly–poly capacitors with a typical area capacitance of 0.86 fF/μm^2. The PTAT currents I_X and I_Y were designed to be around 3 μA each. For all the designs, trimming was conducted to achieve the best TC performance.

A. 4T BGR

The 4T BGR occupies an area of 0.0206 mm^2. It was measured to consume 10.2 μA at 25 °C. As mentioned in Section II, the 4T BGR starts to work at $V_{\mathrm{DD}} = 1.75$ V at 5 °C. Fig. 10 shows the variation of V_{BG} w.r.t. temperature and V_{DD}. The V_{BG} variation w.r.t. V_{DD} is much larger than the variation w.r.t.

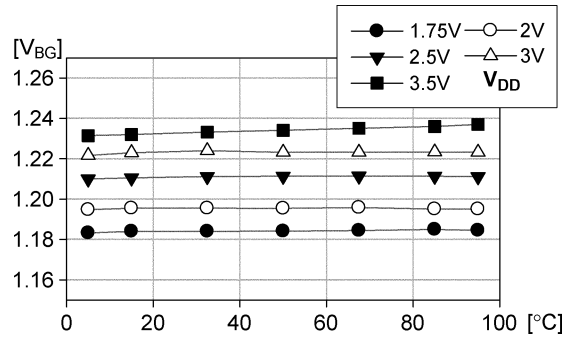

Fig. 10. Measured temperature and $V_{\rm DD}$ sensitivity of 4T BGR.

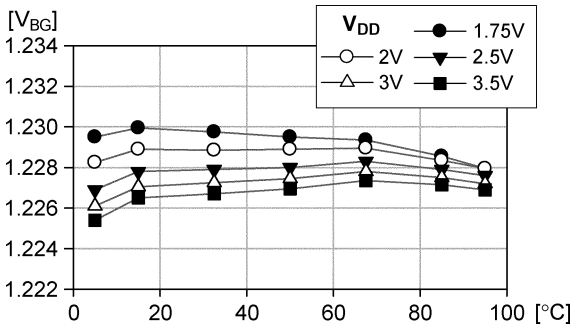

Fig. 11. Measured temperature and $V_{\rm DD}$ dependence of SMI BGR.

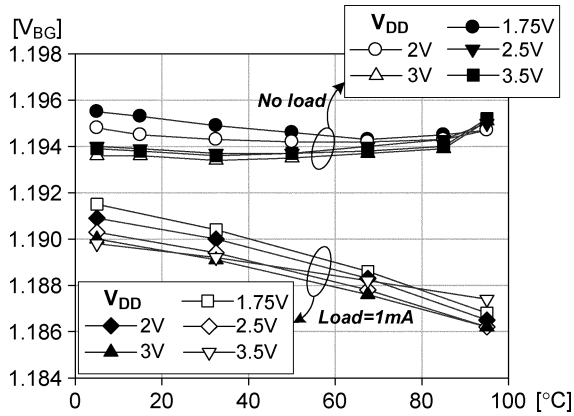

Fig. 12. Measured temperature, $V_{\rm DD}$, and load current dependence of SMB BGR.

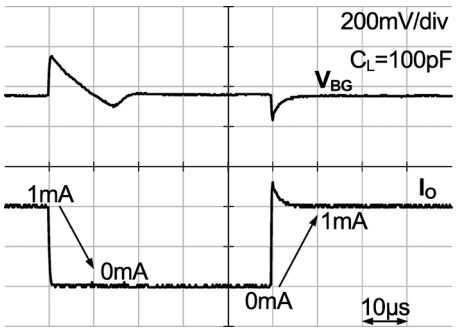

Fig. 13. Load transient response of SMB BGR.

temperature and is due to the channel length modulation of the unsymmetrical circuit structure.

B. SMI BGR

The SMI BGR has one fewer branch and thus occupies a slightly smaller area of 0.0200 mm^2. The current consumption is only 6.6 μA, which is two-thirds of the current consumed by the 4T BGR. As shown in Fig. 11, the TC of $V_{\rm BG}$ after trimming is 12.67 ppm/°C, which is similar to the 4T BGR. However, at 25 °C, the measured line regulation is only 1.8 mV/V, which is much better than that of the 4T BGR. The line regulation is slightly worse than that of the SMB BGR (to be discussed in Section V-C) because $\rm M_{n3}$ was replaced by $\rm R_3$, and the symmetrical cross-coupled structure of $\rm M_{n1}$ and $\rm M_{n2}$ was also altered. At 95 °C, the BGR shows lower sensitivity w.r.t. $V_{\rm DD}$ variation. This is due to the fact that, at 95 °C, $V_{\rm GSn4}$ $(V_4 - V_Y)$ matches with the voltage drop on $\rm R_3$ $(V_{\rm BG} - V_X)$ better than that at other temperatures.

C. SMB BGR

The SMB BGR occupies an area of 0.0432 mm^2 and is twice as large as the 4T BGR, mainly due to the large pass transistor $\rm M_{pz}$ used for sourcing an output current of 1 mA and the on-chip compensation capacitor of $C_c = 5$ pF for stabilizing the output buffer with an off-chip decoupling capacitor of $C_L = 100$ pF. The current consumption is 9.8 μA including the buffer. The SMB BGR was trimmed to have the lowest TC at no load, which was measured to be 12.1 ppm/°C, very close to that of the 4T and SMI BGRs. Fig. 12 shows the measured variation of $V_{\rm BG}$ w.r.t. temperature, $V_{\rm DD}$, and load current. At 25 °C, the line regulation at no load is 1 mV/V for a supply sweep from 1.75 to 3.5 V and is more than 28-dB improvement of that of the 4T BGR, confirming the results obtained by small signal analysis in Sections II and III.

When the load current of the SMB BGR was increased to 1 mA, the TC of $V_{\rm BG}$ reads 38.3 ppm/°C, which is not as good as that of the no-load case but still maintained at a reasonably low value. The line regulation measured 0.7 mV/V at 25 °C, which is even better than that of the unloaded case. It is because the current density of the pass transistor $\rm M_{pz}$ was designed to match with that of $\rm M_{p1-4}$ at $I_O = 1$ mA such that V_5 could match better with V_2 (refer to Fig. 6). Load transient was measured by switching the load current between 0 and 1 mA. The bandgap voltage could settle within 20 μs, as shown in Fig. 13.

D. LV-SMB BGR

The LV-SMB BGR needs several large resistors, and hence, it occupies a larger area of 0.0590 mm^2. The supply voltage could be as low as 0.9 V, and the bandgap-derived reference voltage was designed to be 635 mV at no load. Although this design needs two extra branches of currents (I_5 and I_6), the total current consumption is still only 16.6 μA at 25 °C. Fig. 14 shows that the line regulation is 3.5 mV/V at no load and increased to 9.23 mV/V due to the dropout voltage of the pass transistor at low $V_{\rm DD}$. The TCs of the trimmed reference voltage are 24.6 ppm/°C at no load and 20.0 ppm/°C at $I_O = 1$ mA. The degradation compared to the SMI BGR and the SMB BGR is readily explained by the resistive division in generating $I_{\rm REF}$. It is also due to the slight mismatch between the buffered output stage

TABLE I
PERFORMANCE SUMMARY OF BGRS

	Unit	4T BGR	SMI BGR	SMB BGR	LV-SMB BGR	[15]	[11]	[13]	[14]
Process		0.35-μm CMOS 4M/2P process with high-resistive poly-resistor and poly-poly capacitor				1.5-μm E²PROM CMOS	1.2-μm CMOS	0.6-μm CMOS	0.35-μm CMOS
Active Chip Area	mm^2	0.0206	0.0200	0.0432	0.0590	1.6	1	0.24	1.2
Supply Voltage V_{DD}	V	1.75-3.5			0.9-3.5	2.7-9	1.2	0.98-1.5	1.4
Output Voltage V_{BG}	V	1.2			0.635	1.250	1	0.603	0.858
Supply Current	μA	10.2	6.6	9.8	16.6	0.5	500	18	115.7 #2
Temperature Range	°C	5 to 95				-40 to 80	0 to 100	0 to 100	-20 to 100
TC @ V_{DD}=2.5V (V_{DD}=1.5V for LV-SMB BGR)	ppm/°C	12.85	12.67	12.1 @ 0mA 38.3 @1mA	24.6 @ 0mA 20.0 @ 1mA	<1	<200 #4	15	12.4
Line Regulation @ 25°C	mV/V	28	1.8	1 @ 0mA 0.7 @ 1mA	3.5 @ 0mA 9.23 @ 1mA #1	N. A.	N. A.	8.46 #3	N. A.
Supply Sensitivity @100Hz	dB	-26.2	-51	-53.30 @ 0mA -57.85 @ 1mA	-47.6 @ 0mA -47.6 @ 1mA	<-25	-20 (@1kHz)	-44 (@10kHz)	-68
Load Regulation @ 25°C	mV/mA	N. A.	N. A.	4	7	N. A.	N.A	N. A.	N. A.

Remarks
#1 3.2 mV/V from 1 to 3.5 V
#2 162 μW at 1.4 V
#3 $\pm$2.2 mV from 0.98 to 1.5 V
#4 Untrimmed TC, $< \pm 1\%$ variation

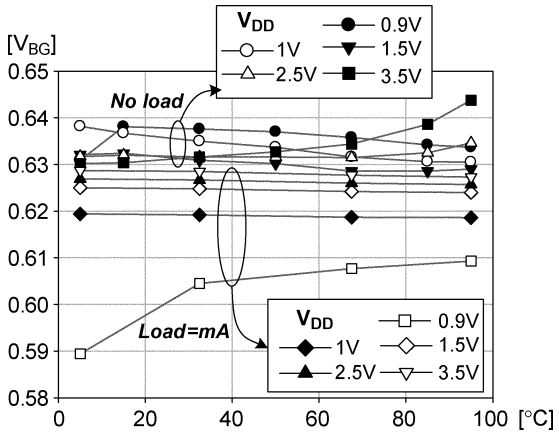

Fig. 14. Measured temperature, $V_{\rm DD}$, and load current dependence of LV-SMB BGR.

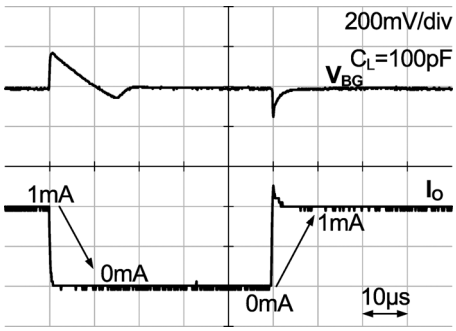

Fig. 15. Load transient response of LV-SMB BGR.

and the $I_{\rm REF}$ generator. Fig. 15 shows that the LV-SMB BGR has load transient response similar to that of the SMB BGR.

E. Measured PSR Versus Frequency of All BGRs

The PSRs of all the BGRs are shown in Fig. 16. All BGRs were driving an output capacitor of 100 pF. At low frequencies, the PSR of the 4T BGR was -26 dB, while that of all three BGRs with SM CVMs were lower than -48 dB. The bandwidths of the SM CVMs were limited by the biasing currents. Therefore, the PSR started to get worse at around 100 Hz, 300 Hz and 1 kHz for the LV-SMB, SMI, and SMB BGRs, respectively. For better PSRs, larger biasing currents have to be used. At high frequencies, all SM BGRs with no load converged to around -30 dB that was governed by the attenuation due to the output capacitor and the parasitic capacitor between $V_{\rm DD}$ and $V_{\rm BG}$.

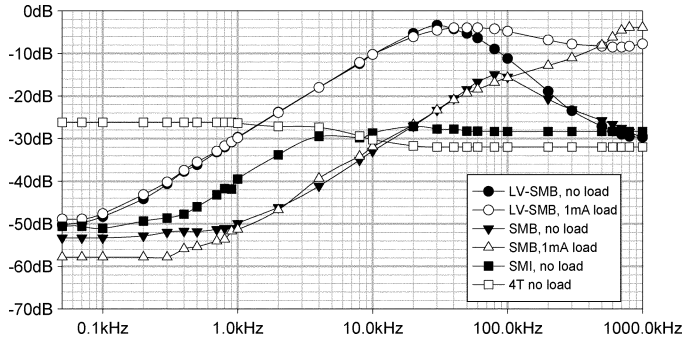

Fig. 16. Supply sensitivity $(v_{\rm bg}/v_{\rm dd})$ of all the BGRs.

Table I compiles all important design parameters and performances of various BGRs presented in this paper. The design parameters of some previously published designs are included for reference. Our proposed BGRs have the smallest chip area and are ideal for cost-sensitive applications. Even if they are implemented using a CMOS technology with a larger feature size, their areas would still be smaller than that of other designs because they have relatively few components.

Although [15] demonstrated a lower power consumption and TC, our designs give better PSRs and could operate at a lower supply voltage. The LV-SMB BGR has a buffered output, and the current consumption and chip area are the lowest when compared to prior low-voltage designs.

VI. Conclusion

Novel BGRs have been designed successfully using a self-biased SM CVM. Systematic offset and power supply sensitivity were minimized due to the symmetrical circuit structure. Their performances were estimated by small-signal analysis and were experimentally characterized and compared with a conventional 4T BGR design, showing that the proposed designs had improved supply rejection, current efficiency, and reduced output impedance (for BGRs with buffered output). The design methodology was also extended to achieve a sub-1-V BGR that could be employed in low-voltage applications.

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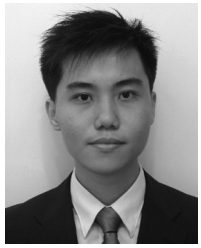

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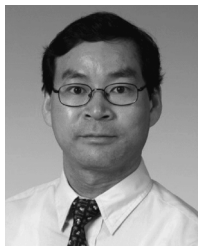
Dr. Lam was a recipient of the Special Feature Award (2006) of the LSI University Design Contest organized by the IEEE Asia and South Pacific Design Automation Conference.



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