PLL 及應用 - 2004

Phase-Locked Loops

Ching-Yuan Yang

National Chung-Hsing University
Department of Electrical Engineering

Overview

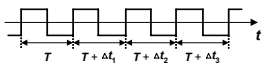
- Main Readings
  - B. Razavi, Chapter 15 of *Design of Analog CMOS Integrated Circuit*, 2002.
  - Cicero S. Vaucher, Chapter 2 of *Architectures for RF Frequency Synthesizers*, 2002
  - Dean Banerjee, *PLL Performance, Simulation, and Design*.

- Outline
  - Simple Phase-Locked Loops
  - Charge-Pump Phase-Locked Loops
  - Nonideal Effects in PLLs
  - Jitter/Noise in PLLs
  - Applications of PLLs
  - Behavior Simulation

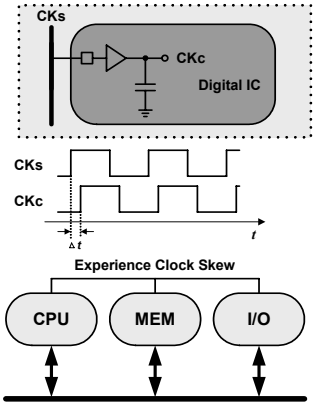
Simple Phase-Locked Loops

Why phase-lock ?

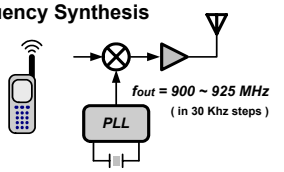
- Jitter Supression

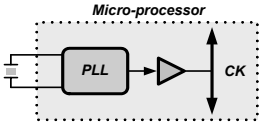


- Skew Reduction

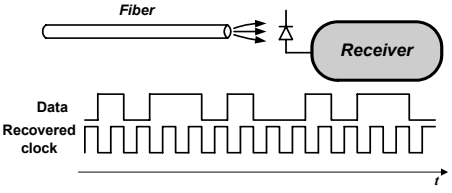


- Frequency Synthesis

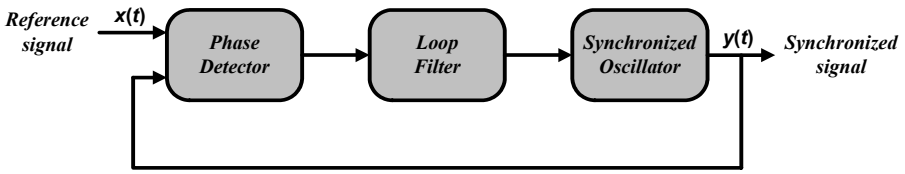




- Clock Recovery



What is PLL ?



- Operates on excess phase of $x(t)$ and $y(t)$.
- Feedback system with PD as an error amplifier.
- "Locked" when phase difference between input and output is constant with time.

History of PLL

- First PLL: 1932 by de Bellesize, Coherent communication
- First PLL IC: 1965, purely analog (Linear PLL)
- First Digital PLL: around 1970 (using Digital Phase Detector)
- All Digital PLL: Digital Filters, NCO (Numerically Controlled Oscillator), …
- Software PLL: Using DSP
- 1990s: Most of the PLL is Charge Pump PLL

Terminology

- Locking

  When VCO output is in phase as well as in frequency with the reference input signal
- Lock Range

  Input frequency range over which the loop can maintain locking
- Capture Range

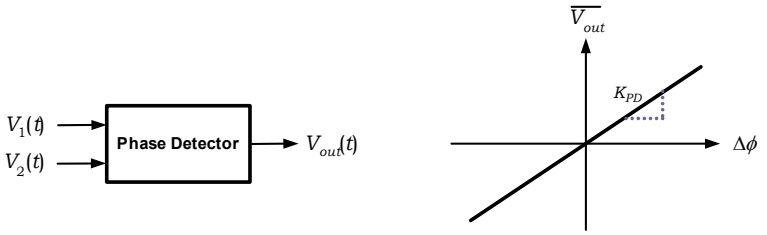
  Input frequency range onto which the loop can lock
- Free Running Frequency

  VCO running frequency when no input applied
- Acquisition Time: Pull-in time + Settling time

  Time required for the PLL to lock itself on to the reference clock
- Phase Offset or Phase Error (Steady State)

  When PLL is locked, the phase difference between input and output

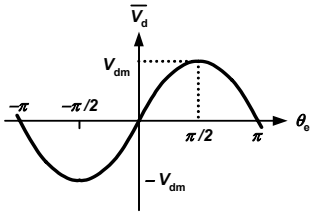
Phase detector

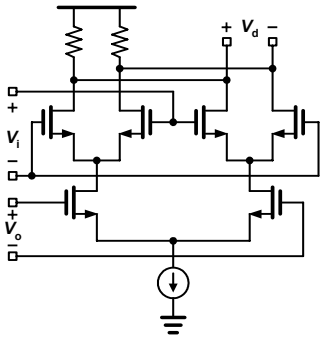


- A phase detector is a circuit whose average output, $\overline{V_{out}}$, is linearly proportional to the phase difference, $\Delta\phi$, between its two inputs.
- In the ideal case, the relationship between $\overline{V_{out}}$ and $\Delta\phi$ is linear, crossing the origin for $\Delta\phi = 0$.
- The operation of phase detectors is similar to that of differential amplifiers in that both sense the *difference* between the two inputs, generating a proportional output.
- Gain K_{PD}: the slope of the line, is expressed in $\mathrm{V/rad}$.

Phase detector : Multiplier

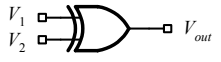
- Phase Detector using Analog Multiplier
- Gilbert multiplier
  - *Output voltage dependent on the input signal amplitudes*
  - *Narrow linear range* (*Narrow lock range*)
  - *Cannot discriminate frequency difference*

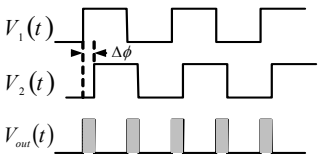




$$\overline{V_d} = V_{dm}\sin(\theta_e) + V_{offset}$$

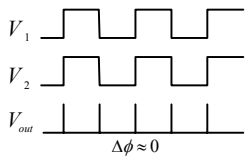
Phase detector : XOR

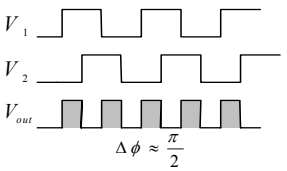


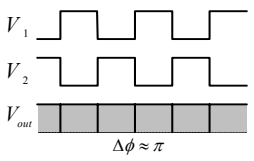


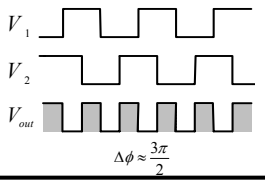
$$\overline{V}_{out} = 2 \cdot V_0 \cdot \frac{\Delta\phi}{2\pi} = \frac{V_0}{\pi} \cdot \Delta\phi$$

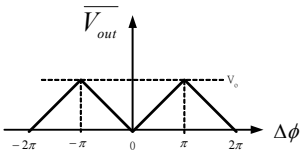
$$K_{PD} = \frac{V_0}{\pi} \quad \textit{independent of the input frequency}$$











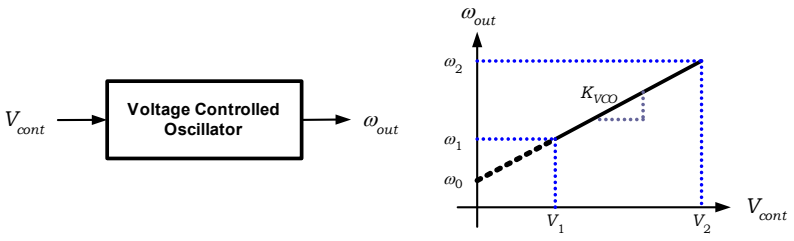
Phase detector : XOR (cont'd)

- When locked, the phase difference is 90 degree
- Output voltage *independent* on the input signal amplitudes
- Output voltage *dependent* on the input duty cycles
- Narrow linear range (Narrow lock range) ⇨ $\pm \pi/2$
- Cannot discriminate frequency difference
- Use for Data/Clock Recovery PLL: input noise dominant

  - Hybrid PLL (Analog PLL + Digital PLL)

- *No Dead Zone*

Voltage-controlled oscillators (VCOs)



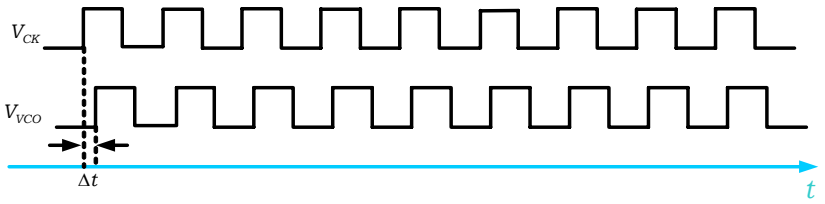
An ideal VCO is a circuit whose output frequency is a linear function of its control voltage:

$$\omega_{out} = \omega_0 + K_{VCO}\, V_{cont}$$

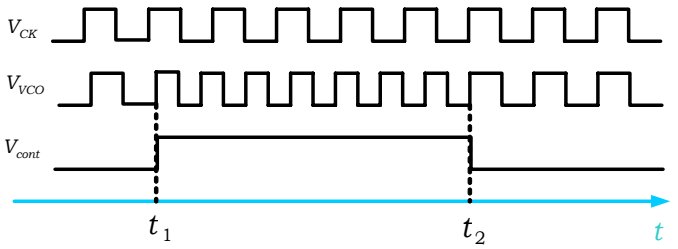
- ω_0 represents the intercept corresponding to $V_{cont} = 0$.
- K_{VCO} denotes the *gain* or *sensitivity* of the circuit (expressed in $\mathrm{rad/s/V}$).
- The achievable range, $\omega_2 - \omega_1$, is called the *tuning range*.

Basic PLL topology

- Two waveforms with a skew



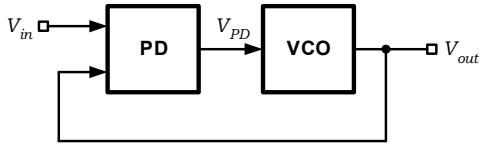
- Change of VCO frequency to eliminate the skew



- Discussion
  - To vary the phase, we *must* vary the frequency and allow the integration
    $\phi = \int (\omega_0 + K_{VCO} V_{cont}) dt$ to take place.
    ⇨ Phase alignment can be achieved only by a (temporary) frequency change.
  - The output phase of a VCO can be aligned with the phase of a reference if
    - the frequency of the VCO is changed momentarily,
    - a phase detector is used to determine when the VCO and reference signals are aligned.
  - *Phase locking* is a task of aligning the output phase of the VCO with the phase of the reference.

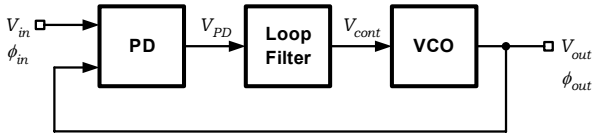
Basic PLL topology (cont'd)

- Feedback loop comparing input and output phases



  - The PD compares the phases of V_{out} and V_{in}, generating an error that varies the VCO frequency until the phases are aligned, i.e., the loop is locked.
  - The topology must be modified because
    - the PD output, V_{PD}, consists of a dc component (desirable) and high frequency components (undesirable),
    - the control voltage of the oscillator must remain quiet in the steady state, i.e.,the PD output must be filtered.

- Simple PLL

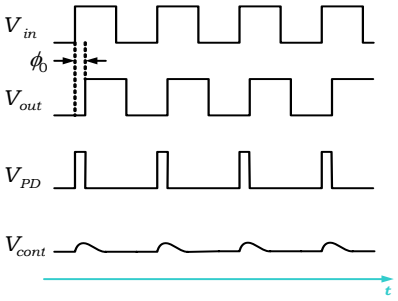


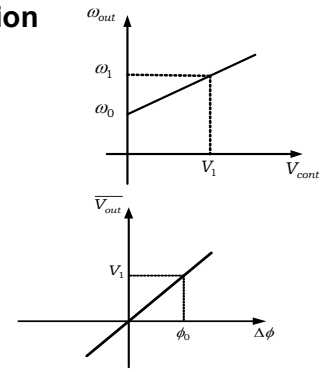
  - A low-pass filter is interposed between the PD and the VCO, suppressing the high-frequency components of the PD output and presenting the dc level to the oscillator.
  - The feedback loop compares the phases of the input and output. If the loop gain is large enough, the difference between the input phase, ϕ_{in}, and the output phase, ϕ_{out}, falls to a small value in the steady state, providing phase alignment
  - Phase lock condition: $\phi_{out} - \phi_{in}$ is constant and preferably small.

$$\frac{d\phi_{out}}{dt} - \frac{d\phi_{in}}{dt} = 0 \qquad \Rightarrow \quad \omega_{out} = \omega_{in}$$

When locked, a PLL produces an output that has a small phase error with respect to the input but exactly the same frequency.

PLL waveforms in locked condition





- If the input and output frequencies are equal to ω_1, then the required oscillator control voltage is unique V_1. Since $\omega_{out} = \omega_0 + K_{VCO}V_{cont}$ and , we can write

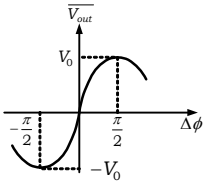
$$V_1 = \frac{\omega_1 - \omega_0}{K_{VCO}} \quad \text{and} \quad \phi_0 = \frac{V_1}{K_{PD}} = \frac{\omega_1 - \omega_0}{K_{PD}K_{VCO}}$$

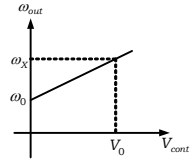
- It reveals two important points:
  - as the input frequency of the PLL varies, so does the phase error,
  - to minimize the phase error, $K_{PD}K_{VCO}$ must be maximized.

PLL waveforms in locked condition (cont'd)

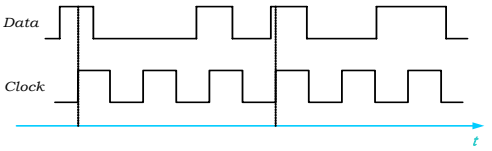
- Nonlinear PD

  If the frequency is high enough (= ω_x) to mandate $V_{cont} = V_0$, then the PD must operate at the peak of its characteristic. However, the PD gain drops to zero here and feedback loop fails. Thus, the circuit cannot lock if $\omega_{in} = \omega_x$.

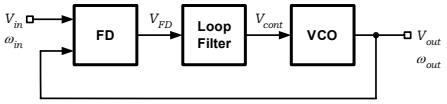


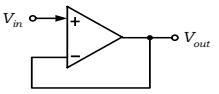


- Drift of data with respect to clock in the presence of small frequency error



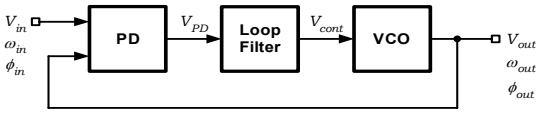
- Frequency-locked loop



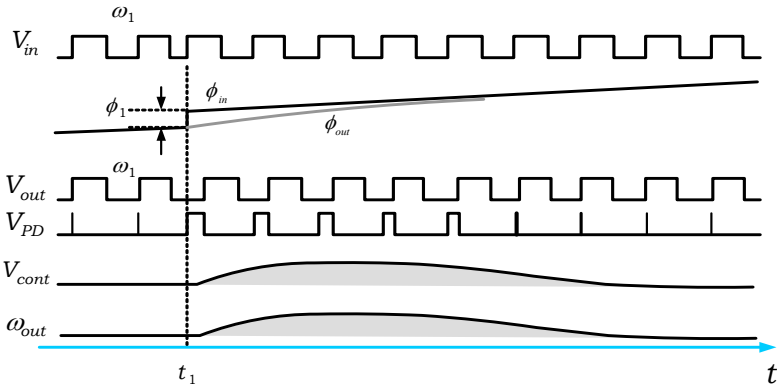


The frequency detector (FD) would suffer from a finite difference between ω_{in} and ω_{out} due to various mismatches and other nonidealities.

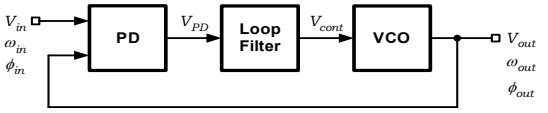
Response of a PLL to a phase step

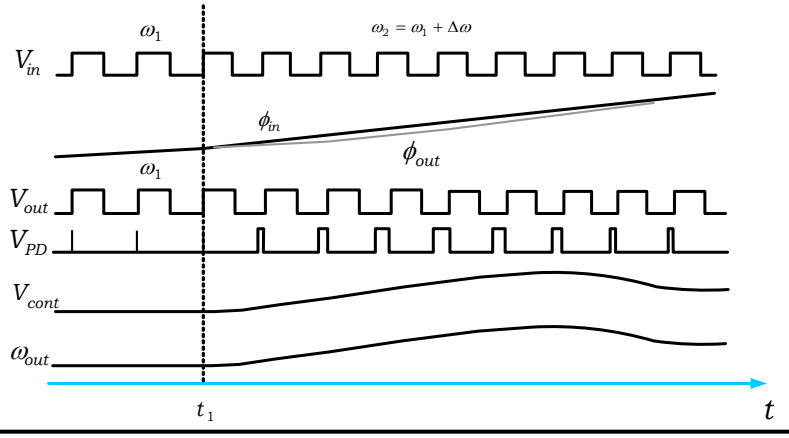


After the loop returns to lock, all of the parameters, $\phi_{in} - \phi_{out}$, V_{cont}, and ω_{out} remain their original values.

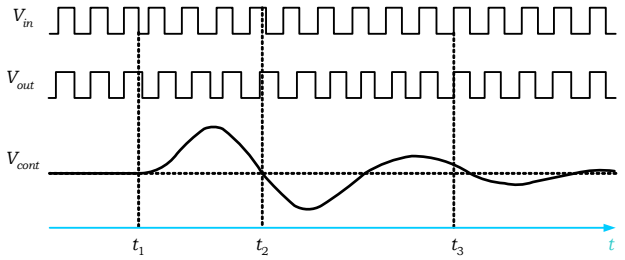


Response of a PLL to a frequency step





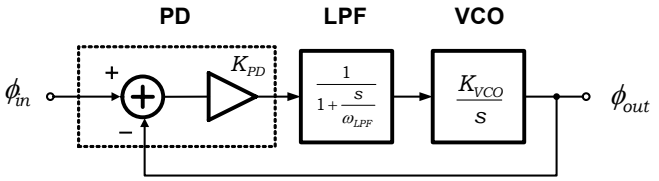
Example of phase step response



- The control voltage of the oscillator can serve as a suitable test point in analysis of PLLs. While it is difficult to measure the time variations of phase and frequency, V_{cont} (= V_{LPF}) can be readily monitored in simulations and measurements.
- The state of the loop:
  - At $t = t_2$, the output frequency is equal to its final value but the loop continues the transient because the phase error deviates from the required value.
  - At $t = t_3$, the phase error is equal to its final value but the output frequency is not.

  For the loop to settle, both the phase and the frequency must settle to proper values.

Linear model of type I PLL



- The open-loop transfer function is given by

$$H(s)\Big|_{\text{open}} = \frac{\phi_{out}}{\phi_{in}}(s)\Big|_{\text{open}} = K_{PD}\cdot\frac{1}{1+\frac{s}{\omega_{LPF}}}\cdot\frac{K_{VCO}}{s}$$

  revealing the poles at $s = -\omega_{LPF}$ and $s = 0$. Since the loop gain contains a pole at the origin, the system is called "type I."
- Owing to the pole at the origin, the loop gain goes to infinity as s approaches to zero. Thus, the PLL ensures that the change in ϕ_{out} is exactly equal the change in ϕ_{in} as s goes to zero
- The closed-loop transfer function can be written as

$$H(s)\Big|_{\text{close}} = \frac{\phi_{out}}{\phi_{in}}(s)\Big|_{\text{close}} = \frac{K_{PD}K_{VCO}}{\frac{s^2}{\omega_{LPF}}+s+K_{PD}K_{VCO}} = \frac{\omega_{out}}{\omega_{in}}(s)$$

  If $s \to 0$, $H(s) \to 1$ because the infinite loop gain. Since the loop gain contains a pole at the origin, the system is called "type I."
- Since a change in ω_{out} must be accompanied by a change in V_{cont}, we have $H(s) = K_{VCO}\cdot\frac{V_{cont}}{\omega_{in}}(s)$

  The response of V_{cont} to variations in ω_{in} indeed yields the response of the close-loop system.

Linear model of type I PLL (cont'd)

- 2nd order transfer function: $H(s) = \dfrac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$

  where natural frequency $\omega_n = \sqrt{\omega_{LPF} K_{PD} K_{VCO}}$ and damping ratio $\zeta = \dfrac{1}{2}\sqrt{\dfrac{\omega_{LPF}}{K_{PD} K_{VCO}}}$

- The two poles of the closed-loop system are given by

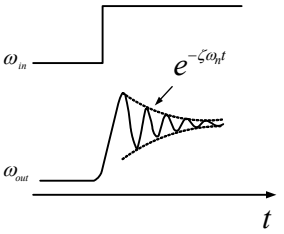
  $$s_{1,2} = -\zeta\omega_n \pm \sqrt{(\zeta^2 - 1)\omega_n^2} = (-\zeta \pm \sqrt{\zeta^2 - 1})\omega_n$$

  - If $\zeta > 1$, the system is overdamped.
  - If $\zeta < 1$, the pole are complex, the system is underdamped and the response to an input frequency step $\omega_{in} = \Delta\omega\, u(t)$ is equal to

  $$\omega_{out} = \left[1 - \frac{1}{\sqrt{1-\zeta^2}} e^{-\zeta\omega_n t} \sin\left(\omega_n\sqrt{1-\zeta^2}\, t + \theta\right)\right]\Delta\omega u(t)$$

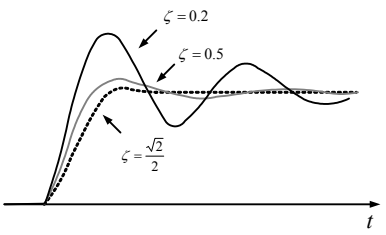
  where ω_{out} denotes the change in the output frequency and $\theta = \sin^{-1}\sqrt{1-\zeta^2}$

  The step response contains a sinusoidal component with a frequency $\sqrt{1-\zeta^2}$ that decays with a time constant $(\zeta\omega_n)^{-1}$.



Linear model of type I PLL (cont'd)

- Settling speed of PLLs: The exponential decay determines how fast the output approaches its final value, implying that $\zeta\omega_n$ must be maximized. For the type I PLL, we have $\zeta\omega_n = \dfrac{1}{2}\omega_{LPF}$
  - It reveals a critical trade-off between the settling speed and the ripple on the VCO control line: the lower ω_{LPF} the greater the suppression of the high-frequency components produced by the PD but the longer the settling time constant.
- Underdamped response:



- 900 MHz PLL:

  $\omega_{LPF} = 2\pi\cdot(20\text{KHz})$,

  $f_{out} = 901\text{MHz} \rightarrow 901.2\text{MHz}$,

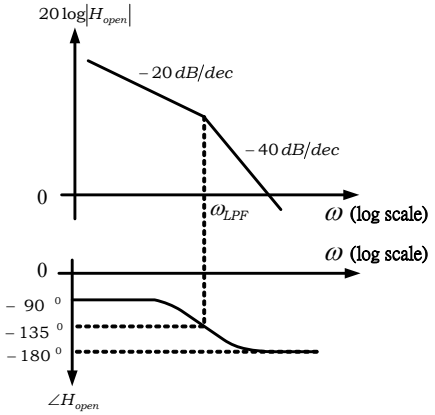
  how long does the PLL output frequency take to settle within 100Hz of its final value?

  In the worst case, we have

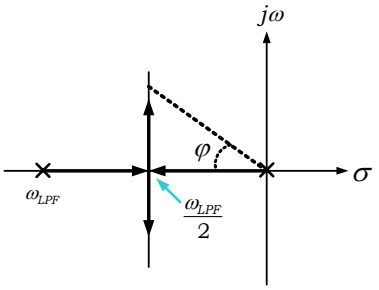
  $$e^{-\zeta\omega_n t_s} \approx \frac{100\text{ Hz}}{200\text{ KHz}} \Rightarrow t_s = 0.12\text{ms}$$

Linear model of type I PLL (cont'd)

- **Bode plots**

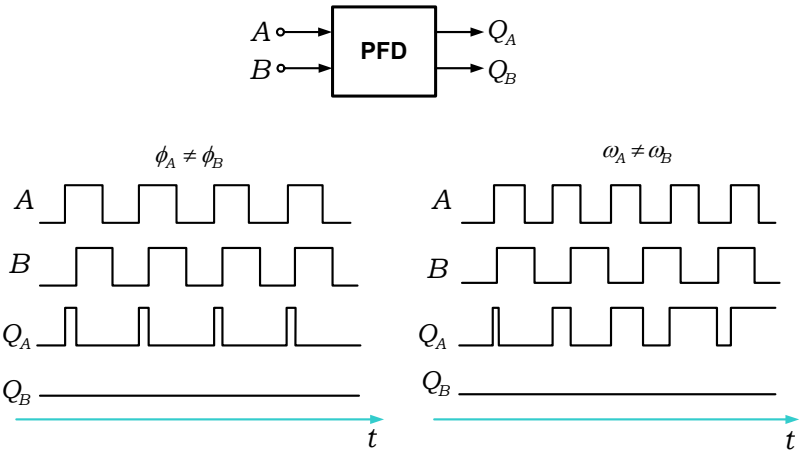


- **Root locus**

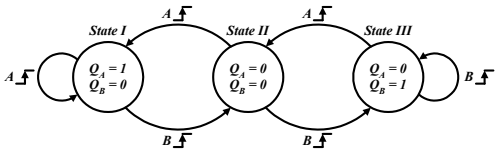


Charge-Pump Phase-Locked Loops

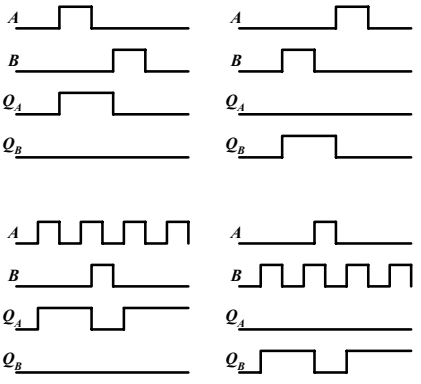
Conceptual operation of a phase-frequency detector (PFD)



Phase detector : PFD – three-state PD

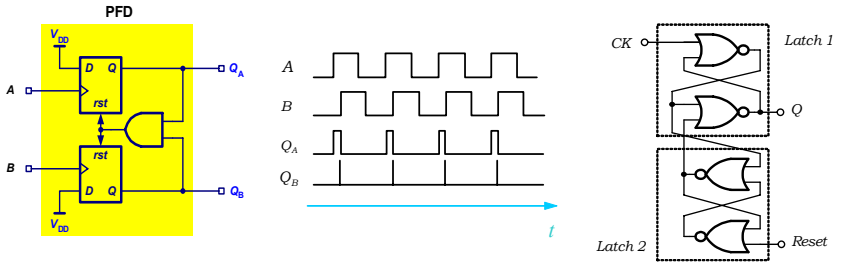


State diagram

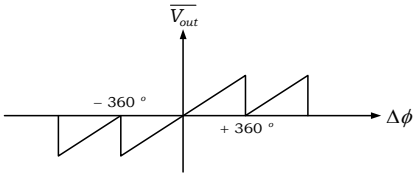


Timing diagram

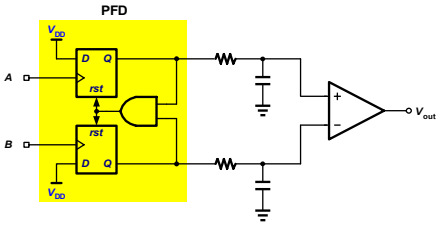
- Implementation of PFD



Input-output characteristic:



PFD followed by low-pass filters:

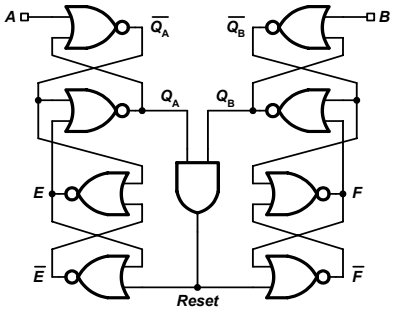


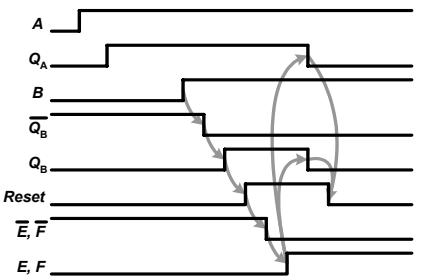
- Phase detector : PFD

- **When locked, the phase difference is 0 degree**
- **Output voltage *independent* on the input signal amplitudes**
- **Output voltage *independent* on the input duty cycles**
- **Wide linear range (Wide lock range) ⇨ ± 2π**
- **Discriminate frequency difference**
- **Use carefully for Data/Clock Recovery PLL**

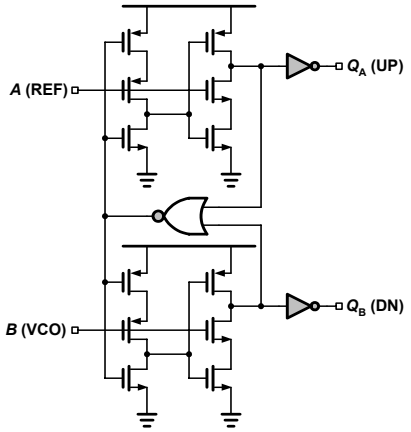
  - Hybrid PLL (Analog PLL + Digital PLL)
- ***Dead Zone problem***
  - ***Due to finite gate delay***
  - ***Introduce large jitter or poor phase noise***

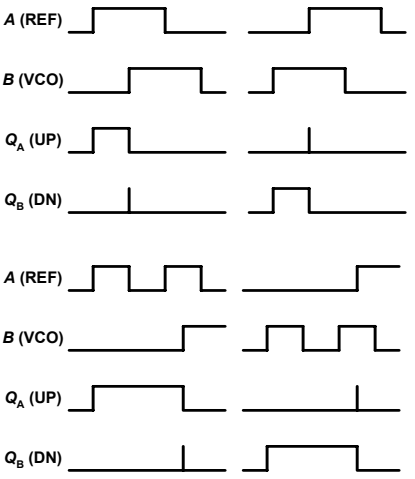
- The width of the narrow reset pulses





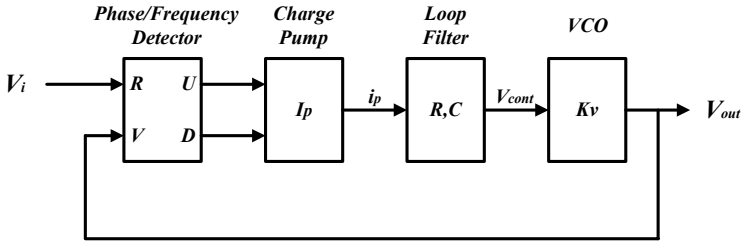
- Dynamic CMOS PFD





Kim, JSSC, May 1997

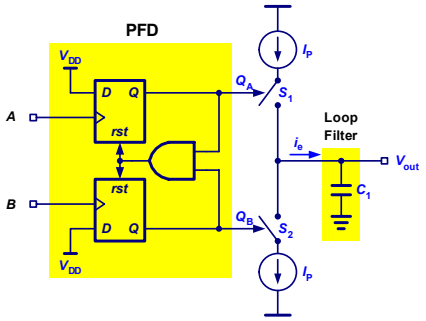
Charge-pump PLL

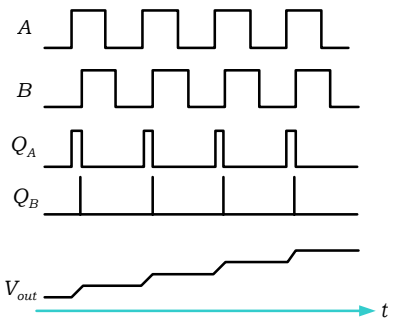


Why charge pump PLL ?

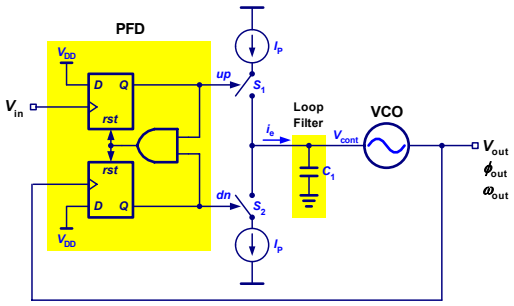
- **Advantages**
  - ***No active component for zero steady state phase error***
  - ***Large frequency and phase capture range***
  - ***Digital output (full CMOS swing)***
  - ***Simple and robust design***
  - ***Discrete time analysis***
- **Disadvantages**
  - ***Slow comparing with analog PLL***
  - ***May create dead zone problem***
  - ***Noisy***

PFD with charge pump





Simple charge-pump PLL (Type II PLL)



Operation

❶ When the loop is turned on, ω_{out} may be far from ω_{in}, and the PFD and the charge pump vary the control voltage such that ω_{out} approaches to ω_{in}.

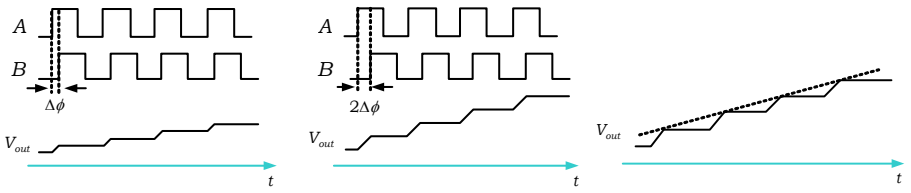
❷ When ω_{out} and ω_{in} are sufficiently close, the PFD operates as a phase detector, performing phase lock.

❸ The loop locks when the phase difference drops to *zero* and the charge pump remains relatively idle.

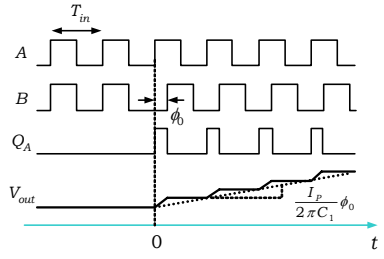
- If V_{cont} remains constant for a long time, the VCO frequency and phase begin to drift. The PFD then detects the phase difference, producing a corrective pulse on *up* and *dn* that adjusts the VCO frequency through the charge pump and the filter.
- Since phase comparison is performed in every cycle, the VCO phase and frequency cannot drift substantially.

- In locked condition, the gain of the PFD/CP combination is infinite, i.e., a nonzero (deterministic) difference between ϕ_{in} and ϕ_{out} leads to indefinite charge buildup on C_1. Therefore, the input phase error must be exactly *zero*.

Linearity of PFD/CP/LPF combination



***Step response*:**



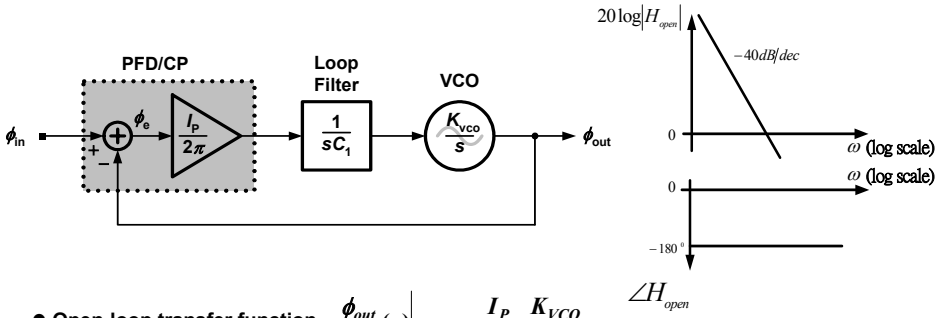
- The system is not linear in the strict sense. We approximate a discrete-time system by a continuous-time model.
- Approximated by a ramp, $\Delta\phi = \phi_0 u(t)$

$$V_{out}(t) = \frac{I_P}{2\pi C_1} t \cdot \phi_0 u(t)$$

⇨ transfer function $\frac{V_{out}}{\Delta\phi}(s) = \frac{I_P}{2\pi C_1} \cdot \frac{1}{s}$

- It contains a pole at the origin.

Linear model of simple charge-pump PLL



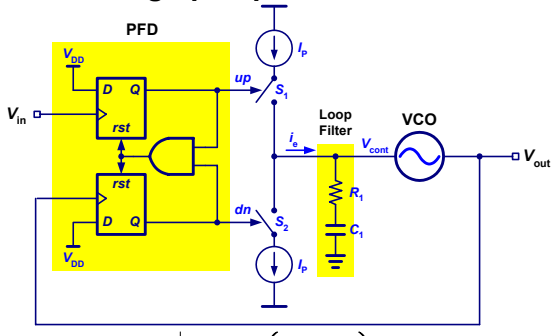
- **Open-loop transfer function** $\left.\frac{\phi_{out}}{\phi_{in}}(s)\right|_{open} = \frac{I_P}{2\pi C_1}\frac{K_{VCO}}{s^2}$

Since the loop gain has two poles at the origin, this topology is called a "type II" PLL.

- **Closed-loop transfer function** $H(s) = \dfrac{\frac{I_P K_{VCO}}{2\pi C_1}}{s^2 + \frac{I_P K_{VCO}}{2\pi C_1}}$

It contains two imaginary poles at $s_{1,2} = \pm j\sqrt{I_P K_{VCO}/(2\pi C_1)}$ **and is unstable.**

Addition of zero to charge-pump PLL

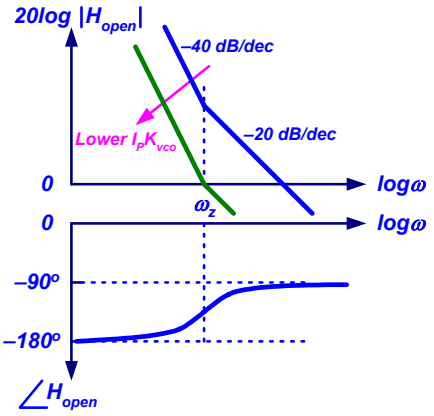


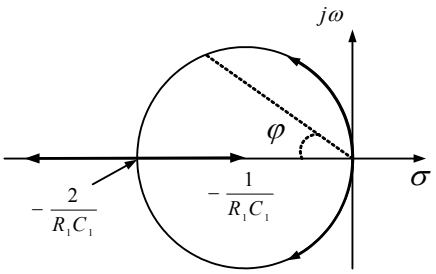
- **Open-loop transfer function** $\left.\frac{\phi_{out}}{\phi_{in}}(s)\right|_{open} = \frac{I_P}{2\pi}\left(R_1 + \frac{1}{C_1 s}\right)\frac{K_{VCO}}{s}$ ⇨ **a zero at** $s_z = -1/(R_1C_1)$.

- **Closed-loop transfer function** $H(s) = \dfrac{\frac{I_P K_{VCO}}{2\pi C_1}(R_1 C_1 s + 1)}{s^2 + \frac{I_P}{2\pi}K_{VCO}R_1 s + \frac{I_P}{2\pi C_1}K_{VCO}}$

⇨ $\omega_n = \sqrt{\frac{I_P K_{VCO}}{2\pi C_1}}$, $\zeta = \frac{R_1}{2}\sqrt{\frac{I_P C_1 K_{VCO}}{2\pi}}$ **and decay time constant** $\frac{1}{\zeta\omega_n} = \frac{4\pi}{R_1 I_1 K_{VCO}}$

Stability degradation of charge-pump PLL





Stability limit and overload limit

In fact, the elegant way to determine the stability limit in the charge pump PLL is to linearize a set of difference equations, to transform it into the z-domain, and to apply the stability criterion on it.

- Normalize PLL parameters:
  - ❶ the normalized loop gain $K_N = I_P R_1 K_{vco} T / 2\pi$
  - ❷ the normalized loop filter $\tau_{1N} = R_1 C_1 / T$
  - ❸ the normalized natural frequency $F_N = f_n / f_i = f_n T$

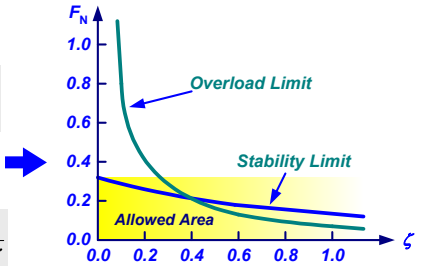
$$\Rightarrow \quad F_N = \frac{1}{2\pi}\sqrt{\frac{K_N}{\tau_{1N}}} \qquad \zeta = \frac{\sqrt{K_N \tau_{1N}}}{2}$$

Stability limit condition:

$$K_N < \frac{2}{1+\frac{1}{2\tau_{1N}}} \quad \Rightarrow \quad F_N < \frac{\sqrt{1+\zeta^2}-\zeta}{\pi}$$

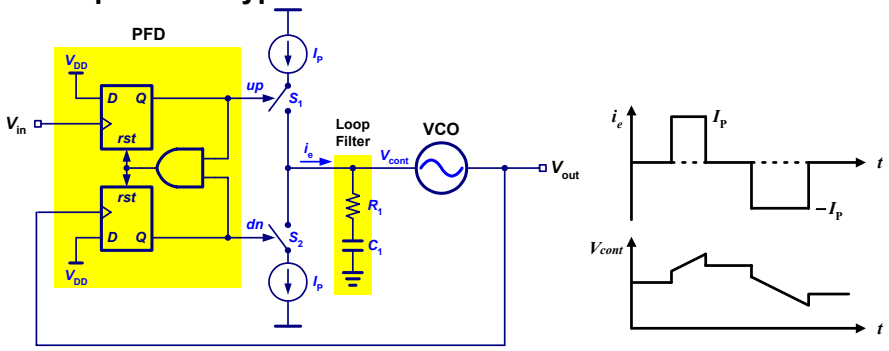
VCO overload limit:

$$V_{cont} = \frac{f_i}{K_{vco}} - I_P R_1 > 0 \quad \Rightarrow \quad K_N < 1 \quad \Rightarrow \quad F_N < \frac{1}{4\pi\zeta}$$



Gardner, IEEE Trans. on Comm., Nov. 1980. Paemel, IEEE Trans. on Comm., Jul. 1994

Compensated type II PLL



Critical drawback :

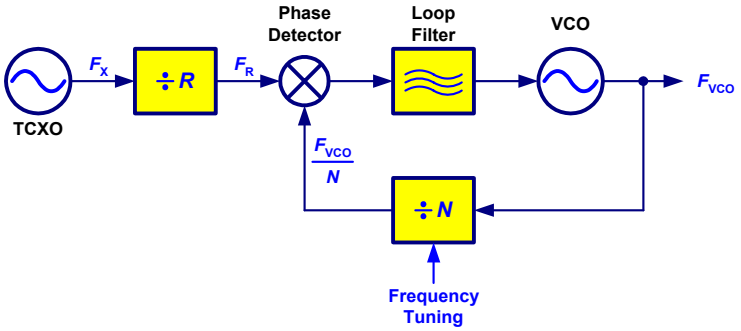
- **ince the charge pump drives the series combination of R_P and C_P, each time a current is injected into the loop filter, the control voltage experiences a large jump.**
- **In lock condition, the mismatches between I_1 and I_2 and charge injection and clock feedthrough of S_1 and S_2 introduce voltage jumps in V_{cont}.**

⇨ The resulting ripple severely disturbs the VCO, corrupting the output phase.

Design flow of 2nd-order PLLs

1. **Determine K_{VCO}.**
2. **Choose the natural frequency ω_n to be about or less then one-tenth of the input frequency.**
3. **Select I_p, to meet the reasonable trade-off between the value the filter components (i.e., chip area) and the pump current.**
4. **Set the damping factor ζ to be 0.707.**
5. **Calculate R_P and C_p.**

PLL frequency synthesizer using dividers



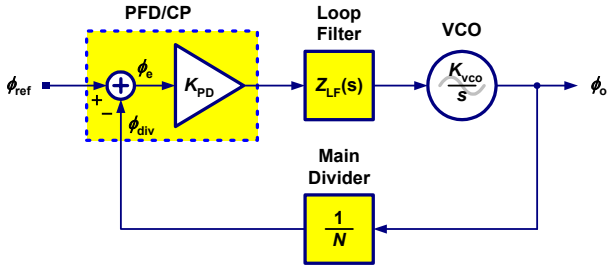
TCXO: Temperature Compensated Crystal Oscillator
VCO: Voltage Controlled Oscillator

In the locked state:

$F_{VCO} = N \times F_R,\ N \in \mathcal{N}$

$F_{VCO} / N = F_X / R = F_R$

Linear model of 3rd-order PLLs with 2nd-order loop filter



PLL phase transfer functions:

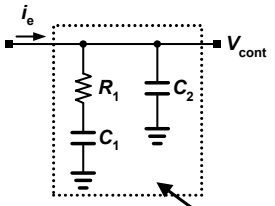
Forward-loop gain $G(s) = \dfrac{\theta_o}{\theta_e} = \dfrac{K_{PD} Z_{LF}(s) K_{vco}}{s}$

Reverse-loop gain $\beta(s) = \dfrac{\theta_{div}}{\theta_o} = \dfrac{1}{N}$

Open-loop gain $\beta(s)G(s) = \dfrac{\theta_{div}}{\theta_e} = \dfrac{K_{PD} Z_{LF}(s) K_{vco}}{Ns}$

Closed-loop gain $\dfrac{\theta_o}{\theta_{ref}} = \dfrac{G(s)}{1 + \beta(s)G(s)}$

- 2nd-order passive filter

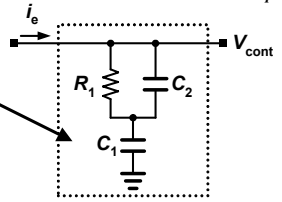


(Addition of C_2 to reduce ripple on the control line.)

$$Z_{LF}(s)=\frac{k}{s}\cdot\frac{1+s\tau_z}{1+s\tau_p}=\frac{k}{s}\cdot\frac{1+s\tau_z}{1+s\tau_z/b}$$

$$Z_{LF1}(s)=\frac{1+sR_1C_1}{s^2R_1C_1C_2+s(C_1+C_2)}=\frac{1+s\tau_z}{s(C_1+C_2)(1+s\tau_p)}$$

Parameters	Loop Filter 1	Loop Filter 2
τ_z	$R_1\,C_1$	$R_1\,(C_1+C_2)$
τ_p	$R_1\left(\frac{C_1C_2}{C_1+C_2}\right)$	$R_1\,C_2$
k	$\left(\frac{b-1}{b}\right)\cdot\frac{1}{C_1}$	$\frac{1}{C_1}$
$b=\frac{\tau_z}{\tau_p}$	$1+\frac{C_1}{C_2}$	$1+\frac{C_1}{C_2}$



$$Z_{LF2}(s)=\frac{1+sR_1(C_1+C_2)}{sC_1(1+sR_1C_2)}$$

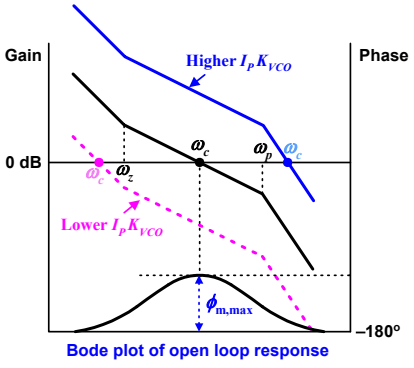
- Open-loop bandwidth ω_c and phase margin ϕ_m

Open-loop gain

$$\beta(s)G(s)=\frac{\theta_{div}}{\theta_e}=\frac{K_{PD}Z_{LF}(s)K_{vco}}{Ns}=\frac{I_P\cdot K_{vco}\cdot k}{2\pi\cdot N\cdot s^2}\cdot\frac{1+s\tau_z}{1+s\tau_p}$$

$$\Rightarrow\quad \beta(s)G(s)\big|_{s=j\omega}=-\frac{I_P\cdot K_{vco}\cdot k}{2\pi\cdot N\cdot \omega^2}\cdot\frac{1+j\omega\tau_z}{1+j\omega\tau_p}$$

$$\phi(\omega)=\tan^{-1}(\omega\cdot\tau_z)-\tan^{-1}(\omega\cdot\tau_p)+180^\circ$$



Bode plot of open loop response

$$\phi_{m,max}:\quad \frac{d\phi}{d\omega}=\frac{\tau_z}{1+(\omega\cdot\tau_z)^2}-\frac{\tau_p}{1+(\omega\cdot\tau_p)^2}=0$$

$$\Rightarrow\quad \omega_c=\frac{1}{\sqrt{\tau_z\cdot\tau_p}}$$

and $\phi_{m,\max}=\tan^{-1}\left(\frac{\tau_z-\tau_p}{2\sqrt{\tau_z\cdot\tau_p}}\right)=\tan^{-1}\left(\frac{b-1}{2\sqrt{b}}\right)$

- **If the loop bandwidth ω_c and the phase margin ϕ_m are specified, we have**

$$b = \frac{1}{\left(-\tan\phi_m + \frac{1}{\cos\phi_m}\right)^2} \quad \text{and} \quad \tau_z = \frac{\sqrt{b}}{\omega_c} \quad \tau_p = \frac{1}{\sqrt{b}\cdot\omega_c}$$

ϕ_m	b	sqrt(b)
20°	2.04	1.42
30°	3.00	1.73
40°	4.59	2.14
45°	5.82	2.41
50°	7.55	2.74
55°	10.06	3.17
60°	13.93	3.73
70°	32.16	5.67
80°	130.64	11.43

For loop filter 1:

$$\omega_c = \frac{I_P K_{vco}}{2\pi\cdot N} R_1 \frac{b-1}{b} = \frac{I_P K_{vco}}{2\pi\cdot N} R_1 \frac{C_1}{C_1+C_2}$$

$$R_1 = \frac{2\pi\cdot N\cdot\omega_c}{I_P\cdot K_{vco}}\frac{b}{b-1}$$

$$C_1 = \frac{\tau_z}{R_1} \quad \text{and} \quad C_2 = \frac{1}{R_1}\cdot\frac{\tau_z\tau_p}{\tau_z-\tau_p}$$

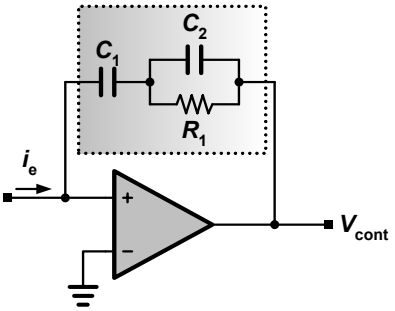
For loop filter 2:

$$\omega_c = \frac{I_P K_{vco}}{2\pi\cdot N} R_1 \frac{b}{b-1} = \frac{I_P K_{vco}}{2\pi\cdot N} R_1 \frac{C_1+C_2}{C_1}$$

$$R_1 = \frac{2\pi\cdot N\cdot\omega_c}{I_P\cdot K_{vco}}\frac{b-1}{b}$$

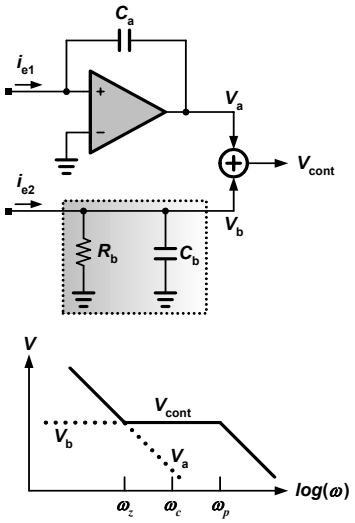
$$C_1 = \frac{\tau_z-\tau_p}{R_1} \quad \text{and} \quad C_2 = \frac{\tau_p}{R_1}$$

Active loop filter implementation



The active loop filter is often used when the charge-pump output can not directly provide the required voltage range for tuning of the VCO. Such voltages are incompatible with charge-pumps built in standard IC technologies, so that a (partly external) active loop filter is then used to isolate the charge-pump output from the VCO tuning input, and to generate the high tuning voltages.

Multi-path charge-pump filter



$$i_{e1} = I_{p1} \times \frac{\theta_e}{2\pi} \qquad i_{e2} = I_{p2} \times \frac{\theta_e}{2\pi}$$

The loop filter transfer function is

$$\frac{V_{cont}(s)}{\theta_e(s)} = K_{pd} Z_{LF}(s) = \frac{I_{p1}}{2\pi}\frac{1}{C_a} + \frac{I_{p1}}{2\pi}\left(R_b \| \frac{1}{sC_b}\right)$$

$$= \frac{I_{p1}}{2\pi \cdot sC_a} \cdot \frac{sC_b\left(C_b + C_a\frac{I_{p2}}{I_{p1}}\right)+1}{sR_bC_b+1}$$

$$\Rightarrow \quad \frac{1}{\omega_z} = R_b\left(C_b + C_a\frac{I_{p2}}{I_{p1}}\right) \approx R_bC_a\frac{I_{p2}}{I_{p1}}$$

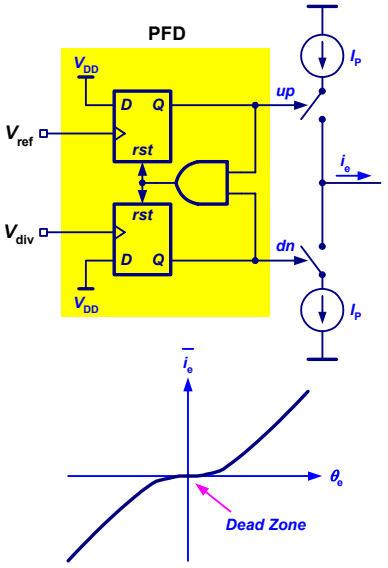
$$\frac{1}{\omega_p} = R_bC_b$$

$$\omega_c \approx \frac{I_{p1} \cdot K_{vco}}{2\pi \cdot N \cdot C_a \cdot \omega_z} = \frac{K_{vco}}{2\pi \cdot N} \cdot I_{p2} \cdot R_b$$

J. Craninckx, IEEE JSSC, Dec. 1998

Nonideal Effects in PLLs

PFD and charge-pump filter

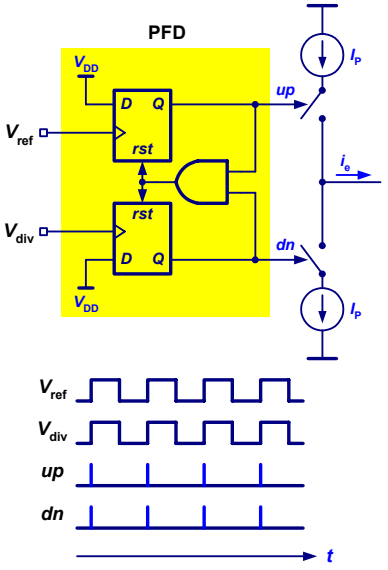


Owing to the finite risetime and falltime resulting from the capacitance seen at the nodes, the pulse may not find enough time to reach a logical high level, failing to turn on the charge pump switches.

- For $|\Delta\phi| < \phi_0$, the charge pump injects no current.
- The loop gain drops to zero and the output phase is not locked.
- The PFD/CP suffers from a dead zone equal to $\pm\phi_0$ around $\Delta\phi = 0$.

⇨ *Jitter resulting from the dead zone*

Reference spurs

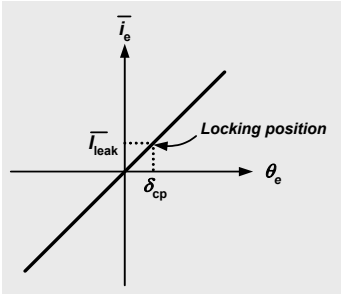


- Periodic disturbance of VCO control line due to charge pump activity:

$$i_e(t) = \underbrace{I_P\delta_{cp}}_{DC} + \underbrace{2I_P\delta_{cp}\sum_{n=1}^{\infty}\cos(2\pi n f_{ref}t)}_{Spectral\ components}$$

- Main effects which generate reference spurious breakthrough:
  - leakage current in the loop filter,
  - skew between *up* and *down* (*dn*) signals,
  - mismatch in the charge *up* and *down* current sources,
  - Charge sharing.

- Effect of leakage current



- Sources of leakage currents:
  - the capacitor of loop filter,
  - the input of VCO,
  - the charge-pump output,
  - the input biasing current of the op-amp, when active loop filter configuration is used.
- The duty cycle of the charge-pump output is

$$\overline{i_e} = I_P \delta_{cp} = I_{leak} \quad \Rightarrow \quad \delta_{cp} = \frac{I_{leak}}{I_P}$$

- The amplitude of charge-pump output:

$$i_e(t) = I_{leak} + 2I_{leak} \sum_{n=1}^{\infty} \cos(2\pi n f_{ref} t)$$

❶ The spectral component are twice the value of I_{leak}.

❷ Not dependent on the nominal charge-pump current I_P.

- Link the leakage current to the magnitude of the spurious components at the output of the VCO:

$$V_{ripple}(n \cdot f_{ref}) = 2I_{leak} \left| Z_{LF}(j2\pi n f_{ref}) \right|$$

- Phase deviation

$$\theta_P(n \cdot f_{ref}) = \frac{\Delta f(n \cdot f_{ref})}{n \cdot f_{ref}} = \frac{V_{ripple}(n \cdot f_{ref}) K_{vco}}{n \cdot f_{ref}} = \frac{2I_{leak} \left| Z_{LF}(j2\pi n f_{ref}) \right| K_{vco}}{n \cdot f_{ref}}$$

❶ Each of baseband modulation frequencies $n \cdot f_{ref}$ generates two RF spurious signals at offset frequencies $\pm n \cdot f_{ref}$ from the carrier f_{LO}.

❷ The amplitude of each spurious signal

$$A_{SP}(f_{LO} \pm n \cdot f_{ref}) = A_{LO} \frac{\theta_P(n \cdot f_{ref})}{2} = A_{LO} \frac{I_{leak} \left| Z_{LF}(j2\pi n f_{ref}) \right| K_{vco}}{n \cdot f_{ref}}$$

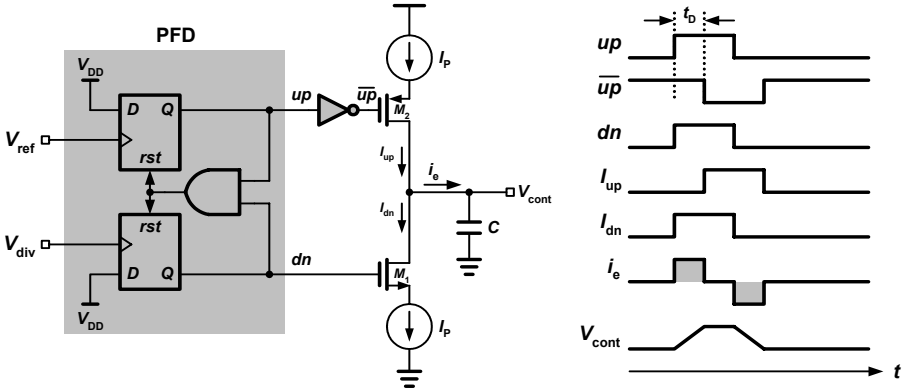
$$\Rightarrow \quad \frac{A_{SP}(f_{LO} \pm n \cdot f_{ref})}{A_{LO}} = \frac{I_{leak} \left| Z_{LF}(j2\pi n f_{ref}) \right| K_{vco}}{n \cdot f_{ref}}$$

$$\Rightarrow \quad \left[\frac{A_{SP}}{A_{LO}} \right]_{dBc} = 20\log \frac{\theta(n \cdot f_{ref})}{2} = 20\log \frac{I_{leak} \left| Z_{LF}(j2\pi n f_{ref}) \right| K_{vco}}{n \cdot f_{ref}} \ \text{[dBc]}$$

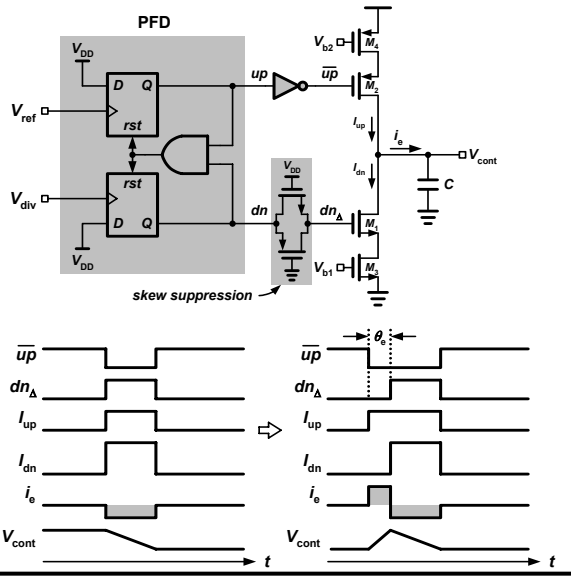
The relative amplitude of the spurious signal is *not* dependent on the value of loop bandwidth or on the nominal charge-pump current I_P.

Theoretically, if $I_{leak} = 0$ there are *no* reference spurs in the output.

- Effect of skew between *up* and *down* signals



- Effect of mismatch in the charge-pump current sources



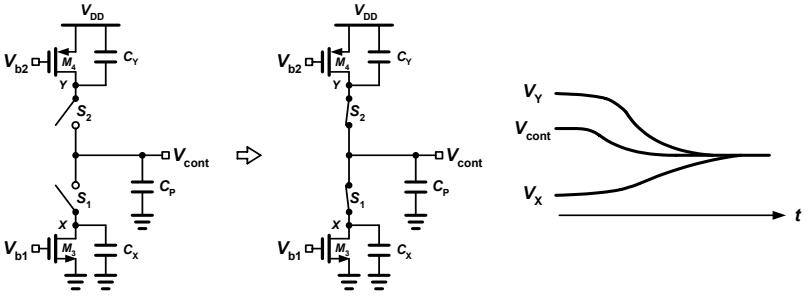
- Effect of mismatch in the charge-pump current sources

- For the loop to remain locked, the average value of V_{cont} must remain constant. The PLL therefore creates a phase error between the input and the output such that the net current injected by the charge pump in every cycle is zero.
  - ⇨ The control voltage still experiences a periodic ripple .
  - ⇨ Owing to the low output impedance of short-channel MOSFETs, the current mismatch *varies* with the output voltage.
  - ⇨ The clock feedthrough and charge injection mismatch between M_1 and M_2 further increases both the phase error and the ripple.
- The magnitude of the spectral components of the ripple voltage due to current-source mismatch can be found

$$V_{mismatch}(n \cdot f_{ref}) = I_{out}(n \cdot f_{ref}) \cdot \left| Z_{LF}(j2\pi n f_{ref}) \right|$$

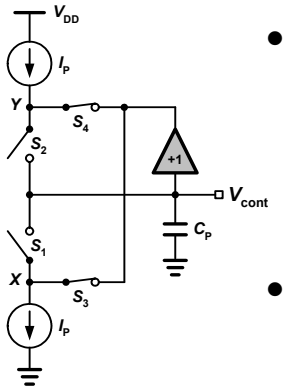
$$\Rightarrow \quad \left[\frac{A_{sp}(n \cdot f_{ref})}{A_{LO}} \right]_{dBc} = 20\log \frac{I_{out}(n \cdot f_{ref}) \left| Z_{LF}(j2\pi n f_{ref}) \right| K_{vco}}{2 \cdot n \cdot f_{ref}}$$

- Effect of charge sharing



- Charge sharing between C_P and capacitances at X and Y:
  - S_1 and S_2 are off, allowing M_3 to discharge X to ground and M_4 to charge Y to V_{DD}.
  - At the next phase comparison instant, both S_1 and S_2 turn on, V_X rises, V_Y falls, and $V_X \approx V_Y \approx V_{cont}$.
- If the phase error is zero and $I_{D3} = |I_{D3}|$, does V_{cont} remain constant after the switches turn on? Even if $C_X = C_Y$, the change in V_X is not equal to that in V_Y.

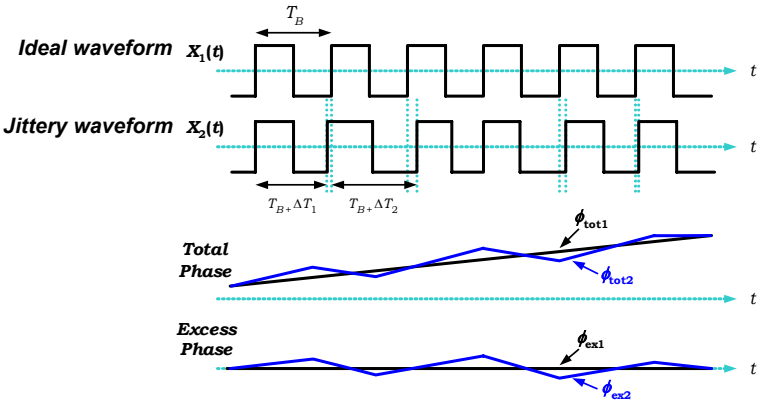
- Effect of charge sharing



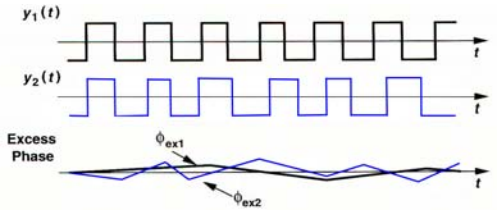
- Bootstrapping X and Y to minimize charge sharing:
  - When S_1 and S_2 turn off, S_3 and S_4 turn on, allowing the unity-gain amplifier to hold nodes X and Y at a potential equal to V_{cont}.
  - At the next phase comparison instant, S_1 and S_2 turn on, S_3 and S_4 turn off, and V_X and V_Y begin with a value equal to V_{cont}.
- The ideal is to "pin" V_X and V_Y to V_{cont} after phase comparison is finished. Thus, no charge sharing occurs between C_P and the capacitances at X and Y.

Jitter/Noise in PLLs

Jitter in PLLs



Jitter in PLLs (cont'd)

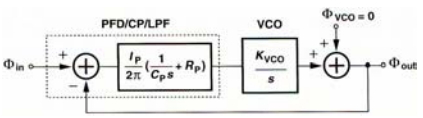


- Effect of input jitter

$$\frac{\phi_{out}}{\phi_{in}}(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

$$\frac{\phi_{out}}{\phi_{in}}(s) = \frac{\omega_n^2(1 + s\tau_z)}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

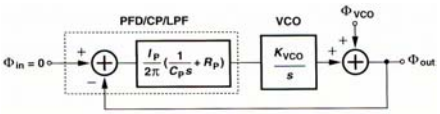
⇨ *Low-pass* characteristic. Slow jitter at the input propagates to the output unattenuated but fast jitter does not.



- Effect of VCO jitter

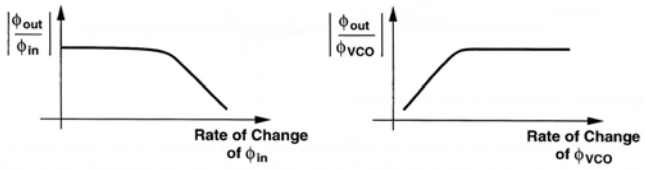
$$\frac{\phi_{out}}{\phi_{in}}(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

⇨ *High-pass* characteristic. Slow jitter components generated by the VCO are suppressed but fast jitter components are not.



Jitter in PLLs (cont'd)

Transfer functions of jitter from input and VCO to the output

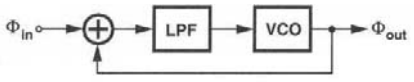


- Effect of VCO jitter:
  - If ϕ_{VCO} changes slowly (e.g., the oscillation period drifts with temperature), then the comparison with ϕ_{in} = 0 (i.e., a perfectly periodic signal) generates a slowly varying error that propagates through the LPF and adjusts the VCO frequency, thereby counteracting the change in ϕ_{VCO}.
  - If ϕ_{VCO} varies rapidly, (e.g., high-frequency noise modulates the oscillation period), then the error produced by the phase detector is heavily attenuated by the poles in the loop, failing to correct for the change.
- In summary, depending on the application and environment, one or both sources may be significant, requiring an optimum choice of the loop bandwidth.

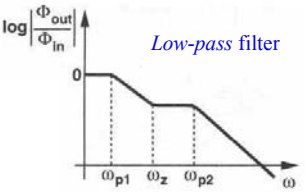
Noise in PLLs

- Phase noise $\phi_n(t) \Rightarrow x(t) = A\cos(\omega_c t + \phi_n(t))$
  If the input signal or the building blocks of a PLL exhibit noise, then the output signal will also suffer from noise.

- Phase noise at input



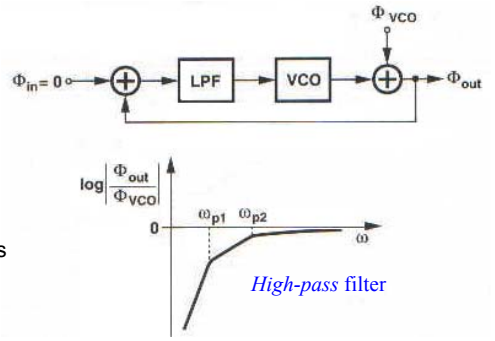
$$\frac{\phi_{out}}{\phi_{in}}(s) = \frac{\omega_n^2(1+s/\omega_z)}{s^2+2\zeta\omega_n s+\omega_n^2}$$



Noise in PLLs (cont'd)

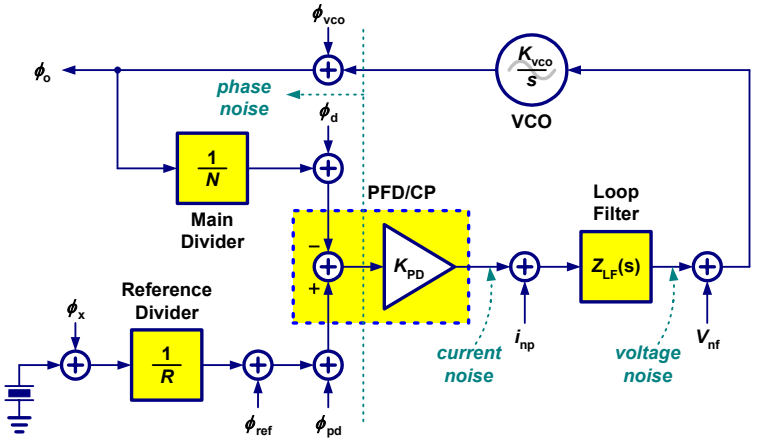
- Phase noise of VCO

$$\frac{\phi_{out}}{\phi_{VCO}}(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$



The VCO phase noise experiences a high-pass transfer function as it appears at the output of a PLL. Thus, increasing the bandwidth of the PLL can lower the contribution of the VCO phase noise.

Noise sources of the PLL

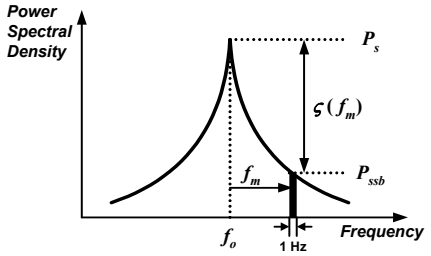


The rms phase noise power density of the loop's output signal is denoted $\phi_o(f_m)$.

The output phase noise power density: $\phi_o^2(f_m) = \phi_{oLP}^2(f_m) + \phi_{oHP}^2(f_m)$

Low-pass transfer function *High-pass transfer function*

- Phase noise



$$v(t) = V_s \sin\left(2\pi f_o t + \theta_n(t)\right)$$

The phase noise $\varsigma(f_m)$, usually in dBc, is the ratio of the single-sideband (SSB) power in a 1-Hz band width f_m Hz away from the carrier to the total signal power, i.e.,

$$\varsigma(f_m) \equiv \frac{P_s}{P_{ssb}}$$

Let $S_{\theta n}(f)$ be the power spectral density of $\theta_n(t)$ in frequency domain, it can be shown that $S_{\theta_n}(f_m) \approx 2\varsigma(f_m)$ and $\overline{\theta_n^2} = \int_0^\infty S_{\theta_n}(f)df$

- Phase noise originated from dividers, PFD/CP and crystal reference sources

- $\phi_d(f_m)$, $\phi_{ref}(f_m)$ and $\phi_{pd}(f_m)$ to $\phi_o(f_m)$: $H_{LP}(s) = N\frac{G(s)}{1+G(s)} = N \cdot H(s)$ (***Low pass***)

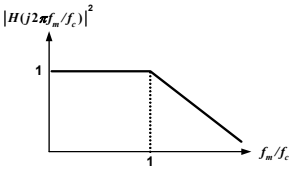
  with open-loop transfer function $G(s) = \frac{\theta_{Div}(s)}{\theta_{ref}(s)} = K_{pd}Z_{LF}(s)\frac{K_{vco}}{s}\frac{1}{N}$

  and closed-loop transfer function $H(s) = \frac{\phi_{Div}(s)}{\phi_{ref}(s)} = \frac{G(s)}{1+G(s)} = \frac{K_{pd}Z_{LF}(s)K_{vco}/N}{s + K_{pd}Z_{LF}(s)K_{vco}/N}$

  ⇨ $\phi_{oLP}^2(f_m) = N^2\left|H(j2\pi f_m)\right|^2\left(\phi_d^2(f_m) + \phi_{ref}^2(f_m) + \phi_{pd}^2(f_m) + \frac{i_{np}^2(f_m)}{K_{pd}^2} + \frac{\phi_x^2(f_m)}{R^2}\right)$

  where $\phi_{eq}^2(f_m) \equiv \phi_d^2(f_m) + \phi_{ref}^2(f_m) + \phi_{pd}^2(f_m) + \frac{i_{np}^2(f_m)}{K_{pd}^2} + \frac{\phi_x^2(f_m)}{R^2}$

  ⇨ The equivalent synthesizer phase noise floor at the input of the phase detector.

  ⇨ $\phi_{oLP}^2(f_m) = N^2\left|H(j2\pi f_m)\right|^2\phi_{eq}^2(f_m)$

- Phase noise due to loop filter and free-running VCO phase noise

- Oscillator: $$\phi_{vco}^2(f_m) \approx \frac{Fk_BT}{P_{rf}}\left[1+\left(\frac{f_{vco}}{2Q_l f_m}\right)^2\right]\left(1+\frac{f_k}{f_m}\right) \ \text{rad}^2/Hz$$

  where F is a noise factor, k_B = 1.37 × 10^{-23} J/K (Boltzmann constant),
  T is the absolute temperature, P_{rf} is the power of the oscillator signal,
  f_{vco} is the output frequency of the oscillator,
  Q_l is the loaded quality factor of the tuning circuit,
  f_m is the offset frequency from the frequency fvco, and
  f_k is the offset frequency which delimits the 9dB/octave dependency of the phase noise power density on the offset frequency (⇨ $\phi_{vco}^2 \propto 1/f_m^3$).

  Assume $f_k \approx 0$ and f_m is small, $$\phi_{vco}^2(f_m) \approx \frac{Fk_BT}{4P_{rf}}\frac{1}{Q_l^2}\frac{f_{vco}^2}{f_m^2} \ \text{rad}^2/Hz$$

  ⇨ –6dB/oct dependency on f_m.

  ⇨ $\phi_{vco}^2(f_m)$ as a function of the phase noise power density at an offset frequency f_r: $$\phi_{vco}^2(f_m) = \phi_{vco}^2(f_r)\frac{f_r^2}{f_m^2}$$

  ⇨ ***Exact function:*** $$\phi_{vco}^2(f_m) = \phi_{vco}^2(f_r)\frac{f_r^2}{f_m^2}\left(1+\frac{f_k}{f_m}\right)+\phi_{vco,nf}^2$$ ***VCO noise floor power density***

- Phase noise due to loop filter and free-running VCO phase noise

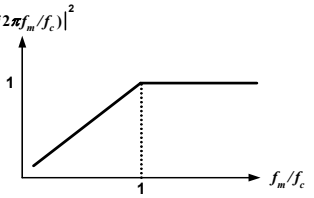
- Loop filter: Thermal noise voltage originated in the loop filter resistor causes unintended phase modulation of the VCO.

$$\phi_{lf}^2(f_m) = v_{nf}^2(f_m)\frac{K_{vco}^2}{f_m^2} \ \text{rad}^2/Hz$$

- Influence of the loop: The influence of the feedback loop on the free-running VCO phase noise power density $\phi_{vco}^2(f_m)$ and on the open-loop phase noise power density generated by the loop filter elements $\phi_{lf}^2(f_m)$ is expressed with the transfer function $T_{HP}(s)$,

$$T_{HP}(s) = \frac{1}{1+G(s)} \quad (\textbf{\textit{High pass}})$$

⇨ $$\phi_{oHP}^2(f_m) = |T_{HP}(j2\pi f_m)|^2\left(\phi_{vco}^2(f_m)+\phi_{lf}^2(f_m)\right)$$

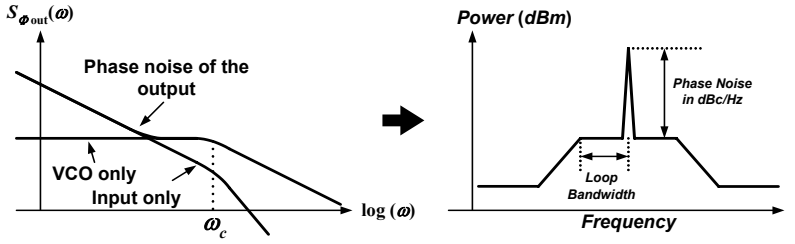


- Total phase noise at the output of the PLL

- Total phase noise noise power spectral density:

$$\phi_o^2(f_m) = N^2\phi_{eq}^2(f_m)\cdot\underbrace{|H(j2\pi f_m)|^2}_{(\textit{Low pass})} + \underbrace{\left(\phi_{vco}^2(f_m)+\phi_{If}^2(f_m)\right)\cdot|T_{HP}(j2\pi f_m)|^2}_{(\textit{High pass})} \quad \text{rad}^2/Hz$$

Typical phase noise spectral plot for PLL:



- General bandwidth requirements

- Low PLL System Jitter

  ⇨ Wide Loop Bandwidth

- Large Input Jitter Reduction

  ⇨ Narrow Loop Bandwidth

- Fast Locking

  ⇨ Wide Loop Bandwidth

- Phase Fluctuation Tracking

  ⇨ Adaptive Loop Bandwidth Control

- There are Trade-offs: No single good solution for All

Spectral purity & design of PLL loop filter

- Consideration:
  - Decrease I_P to acceptable level in order to decrease the power dissipation and to simplify the design of the charge-pump circuitry.
  - The impedance level of the loop filter should be maximized, for the chip-area of fully integrated loop filters to be minimized.

  Note: high impedance level ⇨ small C_1 and C_2, large R_1, and small I_P.
  ⇨ a higher noise contribution from the filter.

- Spurious reference breakthrough:

  ❶Effect of leakage currents

  $$\left|Z_{LF}(j2\pi f_{ref})\right| < \frac{n \cdot f_{ref}}{I_{leak} \cdot K_{vco}} 10^{\frac{Max.spurious}{20}}$$ (***the worst case situation***)

  ($f_c << f_{ref}$) $\left|Z_{LF}(j2\pi f_{ref})\right| \approx \frac{1}{2\pi f_{ref} C_2}$ ⇨ $C_{2,\min} = \frac{I_{leak} \cdot K_{vco}}{2\pi \cdot n \cdot f_{ref}^2} 10^{-\frac{Max.spurious}{20}}$

  ❷Effect of charge-pump current mismatch $C_{2,\min} = \frac{I_{out}(f_{ref}) \cdot K_{vco}}{4\pi \cdot n \cdot f_{ref}^2} 10^{-\frac{Max.spurious}{20}}$

- Phase noise contribution from the loop filter resistor

$$v_{nf}^2(f_m) = \left(\frac{b-1}{b}\right)^2 \cdot \frac{4k_B T R_1}{\left|1 + j2\pi f_m \tau_p\right|^2}$$

⇨ $\phi_{lf}^2(f_m) = v_{nf}^2(f_m) \frac{K_{vco}^2}{f_m^2} = \left(\frac{b-1}{b}\right)^2 \cdot \frac{4k_B T R_1}{\left|1 + j2\pi f_m \tau_p\right|^2} \frac{K_{vco}^2}{f_m^2}$

Define $\alpha_{lf}(f_m) \equiv \frac{\phi_{lf}^2(f_m)}{\phi_{vco}^2(f_m)} = \left(\frac{b-1}{b}\right)^2 \cdot \frac{4k_B T R_1 K_{vco}^2}{\phi_{vco}^2(f_r) f_r^2} \cdot \frac{1}{\left|1 + j2\pi f_m \tau_p\right|^2}$ where $\phi_{vco}^2(f_m) = \phi_{vco}^2(f_r) \frac{f_r^2}{f_m^2}$

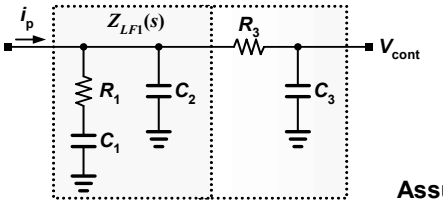
⇨ $\alpha_{lf}(f_m) = \alpha_{lf,dc} \cdot \frac{1}{\left|1 + j2\pi f_m \tau_p\right|^2}$ with $\alpha_{lf,dc} = \left(\frac{b-1}{b}\right)^2 \cdot \frac{4k_B T R_1 K_{vco}^2}{\phi_{vco}^2(f_r) f_r^2}$

Maximum value of R_1:

$$R_{1,\max} = \alpha_{lf,dc} \left(\frac{b}{b-1}\right)^2 \cdot \frac{\phi_{vco}^2(f_r) f_r^2}{4k_B T K_{vco}^2}$$

A smaller value than $R_{1,\max}$ for the loop filter resistor obviously leads to a smaller $\alpha_{lf,dc}$, which is always an acceptable situation from the point of view of phase noise performance.

More attenuation of unwanted spurs with the 3rd-order filter



$$Z_{LF1}(s)=\frac{1+s\tau_z}{s(C_1+C_2)(1+s\tau_p)}$$

$$Z_{LF}(s)=\frac{Z_{LF1}(s)\cdot\left(\frac{1}{sC_3}\right)}{Z_{LF1}(s)+R_3+\frac{1}{sC_3}}$$

Assume $C_2 \geq 10C_3$, we have

The added attenuation from the low-pass filter:

$$ATTEN = 20\log[(2\pi f_{ref}\tau_{p3})^2+1]$$

where $\tau_{p3}=R_3C_3$ (***low-pass pole***)

$$\Rightarrow \quad \tau_{p3}=\frac{\sqrt{10^{\frac{ATTEN}{20}}-1}}{2\pi f_{ref}}$$

$$\tau_z=\frac{1}{\omega_c^2\cdot(\tau_p+\tau_{p3})}$$

$$\omega_c=\frac{\tan\phi_m\cdot(\tau_p+\tau_{p3})}{(\tau_p+\tau_{p3})^2+\tau_p\tau_{p3}}\cdot\left(\sqrt{1+\frac{(\tau_p+\tau_{p3})^2+\tau_p\tau_{p3}}{(\tan\phi_m\cdot(\tau_p+\tau_{p3}))^2}}-1\right)$$

$$\Rightarrow \quad C_2=\frac{\tau_p}{\tau_z}\cdot\frac{K_{pd}\cdot K_{vco}}{\omega_c^2\cdot N}\cdot\left(\frac{(1+\omega_c^2\cdot\tau_z^2)}{(1+\omega_c^2\cdot\tau_p^2)(1+\omega_c^2\cdot\tau_{p3}^2)}\right)^{\frac{1}{2}}$$

$$C_1=C_2\cdot\left(\frac{\tau_z}{\tau_p}-1\right) \quad \text{and} \quad R_1=\frac{\tau_z}{C_1}$$

(***similar to the 2nd-order filter***)

- Derivation of ω_C

The impedance of the loop filter: $Z_{LF}(s)=\dfrac{Z_{LF1}(s)\cdot\left(\frac{1}{sC_3}\right)}{Z_{LF1}(s)+R_3+\frac{1}{sC_3}}$ and $Z_{LF1}(s)=\dfrac{1+s\tau_z}{s(C_1+C_2)(1+s\tau_p)}$

Knowing that $C_2 \geq 10C_3$ and $\tau_{p3} = R_3C_3$

Open-loop gain: $\beta(s)G(s)\big|_{s=j\omega}=-\dfrac{K_{PD}\cdot K_{vco}}{\omega^2\cdot C_1\cdot N}\cdot\dfrac{1+j\omega\tau_z}{1+j\omega\tau_p}\cdot\dfrac{\tau_p}{\tau_z}\cdot\dfrac{1}{1+j\omega\tau_{p3}}$

$$\phi(\omega)=\tan^{-1}(\omega\cdot\tau_z)-\tan^{-1}(\omega\cdot\tau_p)-\tan^{-1}(\omega\cdot\tau_{p3})+180^\circ \quad \text{... (A)}$$

Assume $\omega_z < \omega < \omega_p < \omega_{p3}$, we have

$\phi_{m,max}$: $\dfrac{d\phi}{d\omega}=\dfrac{\tau_z}{1+(\omega\cdot\tau_z)^2}-\dfrac{\tau_p}{1+(\omega\cdot\tau_p)^2}-\dfrac{\tau_{p3}}{1+(\omega\cdot\tau_{p3})^2}=0$

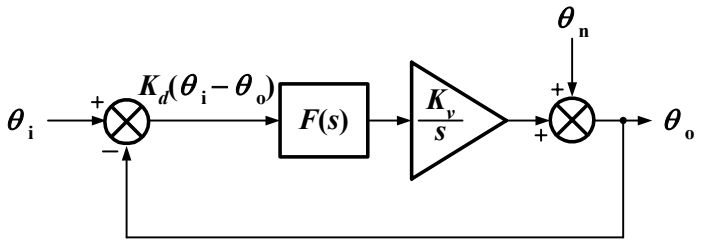
$$\Rightarrow \quad \frac{\tau_z}{(\omega\cdot\tau_z)^2}-\tau_p-\tau_{p3}\approx 0 \quad \Rightarrow \quad \tau_z=\frac{1}{\omega^2(\tau_p+\tau_{p3})} \quad \text{... (B)}$$

Substituting (B) into (A) gives $\tan\phi=\dfrac{-\omega\cdot(\tau_p+\tau_{p3})-\dfrac{\omega\cdot\tau_p\tau_{p3}}{\tau_p+\tau_{p3}}+\dfrac{1}{\omega\cdot(\tau_p+\tau_{p3})}}{2-\omega^2\cdot\tau_p\tau_{p3}}$

$$\Rightarrow \quad \omega^2+\omega\frac{2\tan\phi}{(\tau_p+\tau_{p3})^2+\tau_p\tau_{p3}}-\frac{1}{(\tau_p+\tau_{p3})^2+\tau_p\tau_{p3}}=0$$

Taking the negative root ⇨ $\omega_c=\dfrac{\tan\phi_m\cdot(\tau_p+\tau_{p3})}{(\tau_p+\tau_{p3})^2+\tau_p\tau_{p3}}\cdot\left(\sqrt{1+\dfrac{(\tau_p+\tau_{p3})^2+\tau_p\tau_{p3}}{(\tan\phi_m\cdot(\tau_p+\tau_{p3}))^2}}-1\right)$

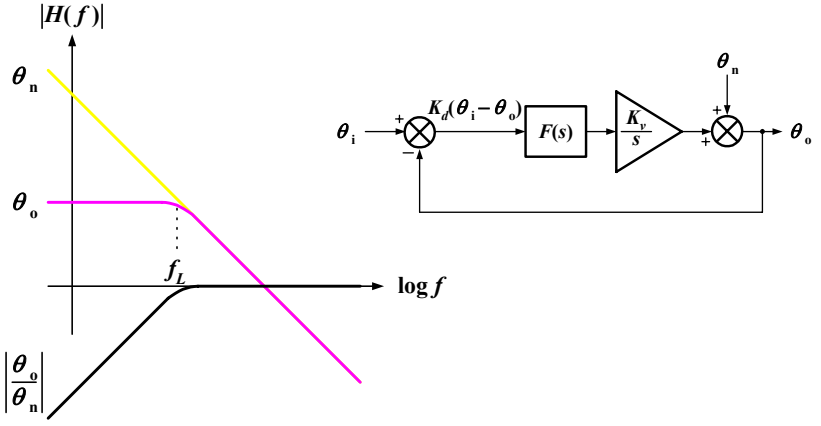
PLL block diagram



- **Noise transfer function:** $\frac{\theta_o}{\theta_n} = \frac{s}{s + 2\pi f_L}$

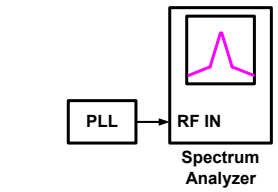
  where the loop bandwidth f_L is determined by K_d, K_v and $F(s)$.
- **θ_n can be represented by integrated white noise giving a 1 / f^2 power spectral density (psd).**

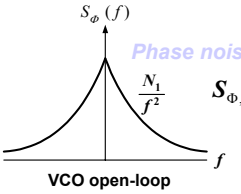
PLL output phase noise psd



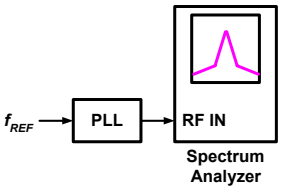
- **θ_n : open-loop phase noise psd (integrated white noise)**
- **θ_o : closed-loop phase noise psd (lowpass due to shaping by loop)**

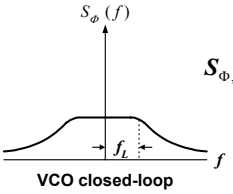
Measured phase noise: frequency domain





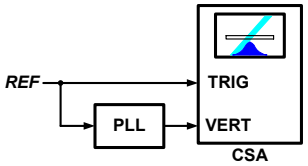
$$S_{\Phi,OL}(f) = \frac{N_1}{f^2} = \frac{K^2 f_0^2}{f^2}$$

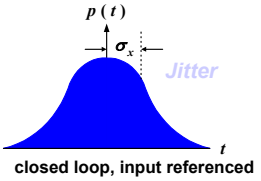




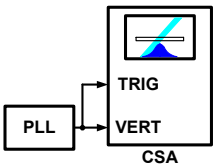
$$S_{\Phi,CL}(f) = \frac{\frac{N_1}{f_L^2}}{1+\left(\frac{f}{f_L}\right)^2} = \frac{K^2\left(\frac{f_0}{f_L}\right)^2}{1+\left(\frac{f}{f_L}\right)^2}$$

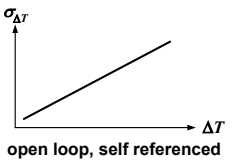
Measured phase noise: time domain



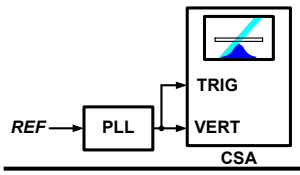


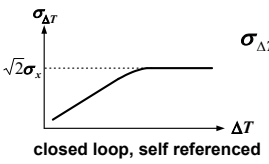
$$\sigma_x = \frac{1}{f_0}\sqrt{\frac{N_1}{4\pi f_L}} = K\sqrt{\frac{1}{4\pi f_L}}$$





$$\sigma_{\Delta T,OL} = K\sqrt{\Delta T}$$





$$\sigma_{\Delta T,CL} = \sqrt{2}\sigma_x\sqrt{1-\exp(-2\pi f_L \Delta T)}$$

Design example

- A VCO with center frequency of f_0 = 622 MHz and phase noise –106 dBc at a 1-MHz offset is to be used in a PLL. Assuming the VCO is the dominant source of jitter, what is the required loop bandwidth f_L to realize a jitter of σ_x = 10 ps rms?

  ⌦ Determine N_1:

  Phase noise @ f_{os} = 10 log (N_1/f_{os}^2)

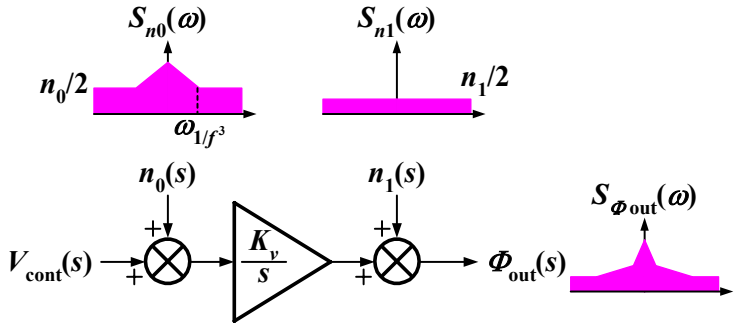
  – 106 dBc = 10 log (N_1/(1MHz)^2) ⇨ $N_1 = 25.1$ Hz

  ⌦ Find f_L:

  Jitter $\sigma_x = \frac{1}{f_0}\sqrt{\frac{N_1}{4\pi f_L}}$

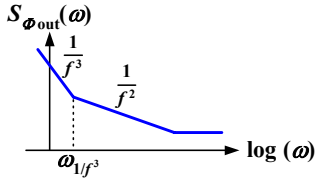
  ⇨ f_L = 51.6 kHz

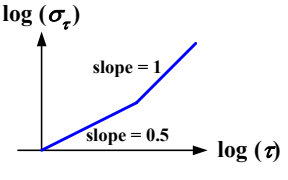
Equivalent model for the phase noise of a VCO



- **VCO acts as an ideal integrator.**
- **The input source, $n_0(s)$, has white and 1/f noise portions that will generate the 1/f^2 and 1/f^3 regions in the output spectrum. The output source, $n_1(s)$, models the noise floor.**

Typical phase noise and timing jitter of a free running VCO





- **Output power spectrum**

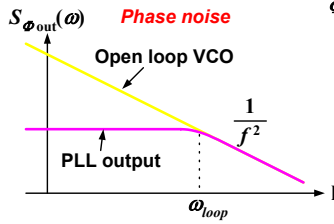
$$S_{\Phi_{out}}(\omega) = \left|\frac{K_V}{j\omega}\right|^2 S_n(\omega) + \frac{N_1}{2} = \frac{K_V^2 N_0}{2\omega^2}\left(1 + \frac{\omega_{1/f^3}}{\omega}\right) + \frac{N_1}{2}$$

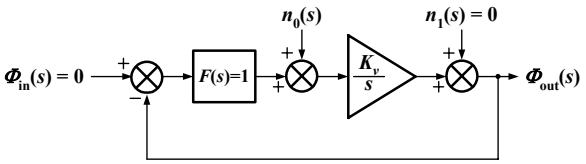
where $N_{0,1}/2$ are the double-sideband power spectral densities of the input and output white noise sources, $n_{0,1}(s)$, and ω_1/f^3 is the $1/f$ noise corner of the input behavior noise source, $n_0(s)$, that is equal to the $1/f^3$ noise corner of the VCO.

- **In the time domain, the uncertainties in the transition times accumulate continuously, increasing the timing jitter of the oscillator.**
  - ⊠ **Uncorrelated part: $\sigma_\tau = \kappa\sqrt{\tau}$ where σ_τ is the rms jitter τ seconds after the reference, and κ is the proportionality constant.**
  - ⊠ **Correlated part: the magnitudes add directly resulting in an additional region with a slope of one.**

Phase noise and jitter in 1st order loops

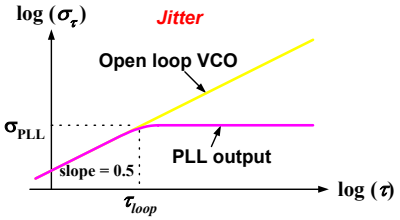
- **Assuming a noiseless input and assuming the VCO noise is dominated by its $1/f^2$ noise**





⊠ **Phase noise**

$$\frac{\Phi_{out}(s)}{n_0(s)} = \frac{K_V}{K_D K_V + s} \Rightarrow S_{\Phi_{out}}(\omega) = \frac{N_0}{2}\frac{K_V^2}{(K_D K_V)^2 + \omega^2}$$



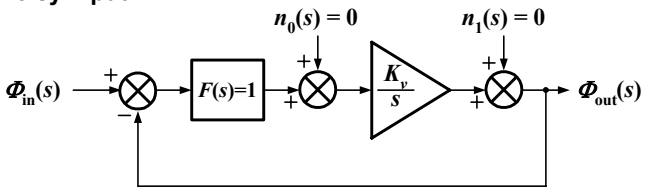
⊠ **Timing jitter**

$$\sigma_\tau^2 = \frac{NK_V^2}{2\omega_0^2}\cdot\frac{1}{\omega_{loop}}\cdot\left(1 - e^{-\omega_{loop}\cdot\tau}\right) \approx \frac{NK_V^2}{2\omega_0^2}\cdot\tau \quad \text{for } \tau << \tau_{loop}.$$

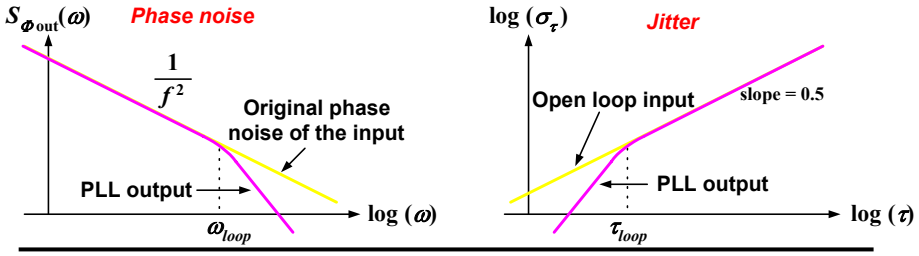
(Khinchin theorem)

Phase noise and jitter in 1st order loops

- **Ideal VCO and noisy input**

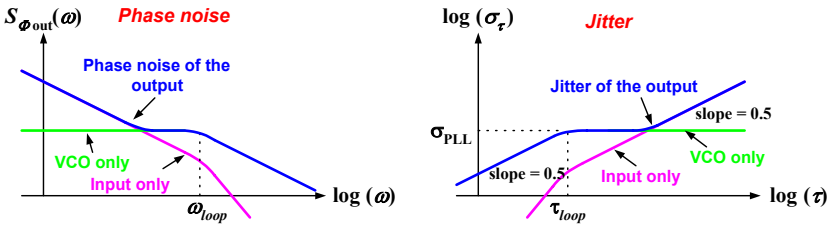


$$\frac{\Phi_{out}(s)}{\Phi_{in}(s)} = \frac{K_D K_V}{K_D K_V + s} = \frac{1}{1 + s/\omega_{loop}} \quad \Rightarrow S_{\Phi_{out}}(\omega) = \frac{\alpha}{\omega^2}\frac{\omega_{loop}^2}{\omega_{loop}^2 + \omega^2} \text{ if } S_{\Phi_{in}}(\omega) = \frac{\alpha}{\omega^2}$$

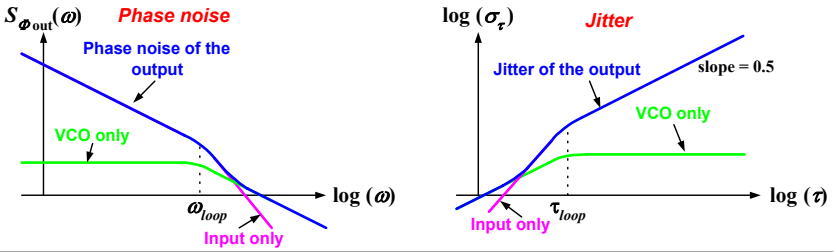


Phase noise and jitter in 1st order loops

- **PLL with large VCO noise (e.g. clock generators, frequency synthesizers)**

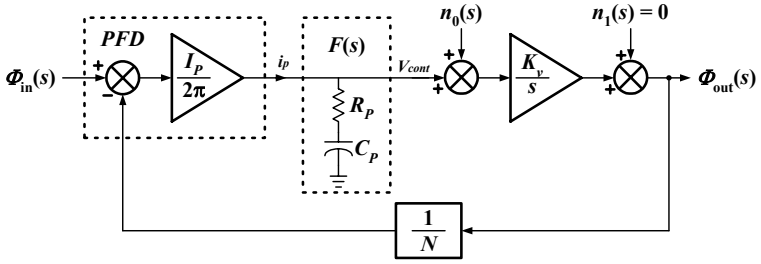


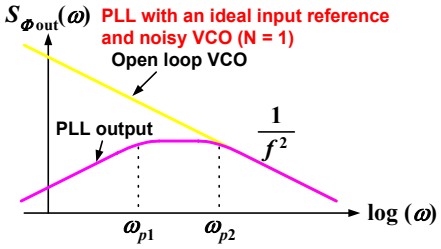
- **PLL with large input reference noise (e.g. clock recovery)**

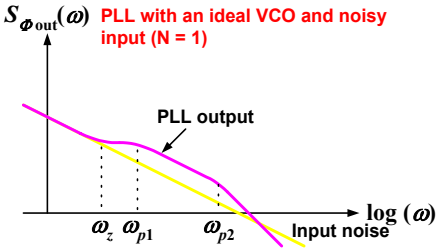


Phase noise in higher-order loops

- **Charge-pump PLL**

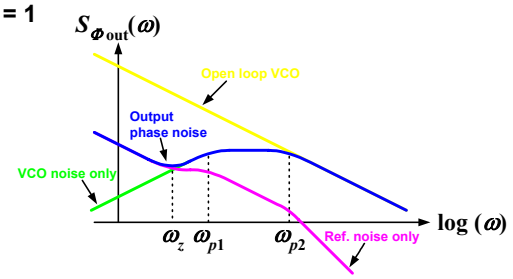




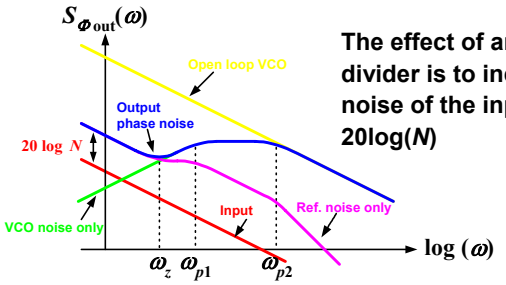


Phase noise in higher-order loops

- **PLL with *N* = 1**



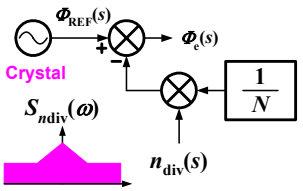
- **PLL with *N***

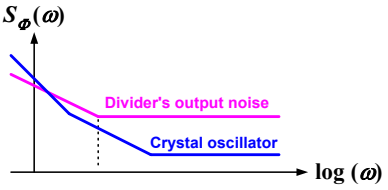


The effect of an *ideal* frequency divider is to increase the phase noise of the input by a factor of 20log(*N*)

Noise contribution of the frequency divider

- **Equivalent model for frequency divider noise**

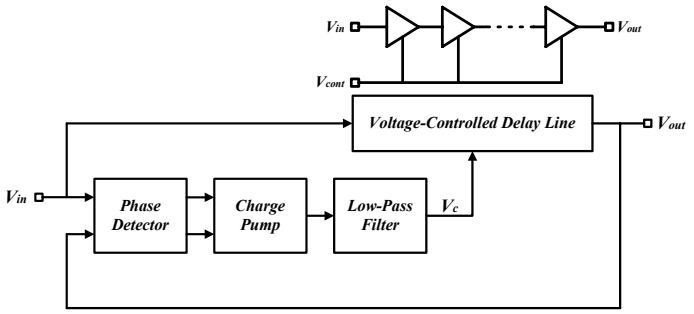




- **The divider's noise usually appears as directly at the input of the PD and experiences the same transfer function as the noise on the input terminal.**
- **Digital dividers usually have a large white noise floor at their output. If the divider is implemented using active devices with large 1/*f* noise, it may even swamp the noise of the reference completely.**
- **Due to the resonant nature, analog regenerative and injection-locked dividers are generally less noisy than the digital synchronous and asynchronous counterparts.**

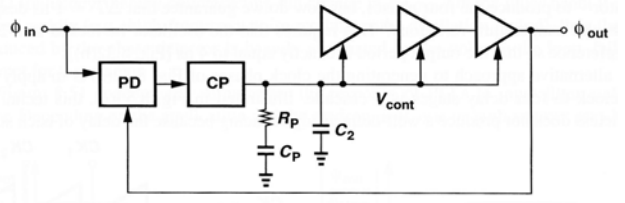
Applications of PLLs

Delay-locked loops



- **Delay line much less noisy than VCOs.**
- **First-order system (for first-order LPF), thus very stable.**
- **But input and output frequencies must be equal.**

Transfer function of DLL



Transfer function of PD/CP/LPF

$$\frac{V_{cont}}{\Delta\phi}(s) = \frac{I_P}{2\pi}\left[\left(R_P + \frac{1}{C_P s}\right)\middle\|\frac{1}{C_2 s}\right] = \frac{I_P}{2\pi}\frac{R_P C_P s + 1}{(R_P C_P C_2 s + C_P + C_2)s}$$

Close-loop transfer function

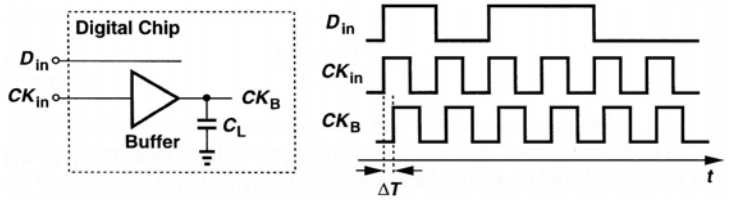
$$\frac{\phi_{out}}{\phi_{in}}(s)\bigg|_{\text{closed}} = \frac{\frac{I_P K_{VCDL}}{2\pi}(R_P C_P s + 1)}{R_P C_P C_2 s^2 + \left[C_P + C_2 + \frac{I_P K_{VCDL} R_P C_P}{2\pi}\right]s + \frac{I_P K_{VCDL}}{2\pi}}$$

Discussion

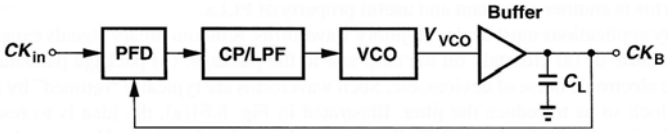
- The closed-loop transfer can be used to determine how ϕ_{out} settles if ϕ_{in} experiences a change. ⇨ ω_n, ζ
- In practice R_P may not be need because the loop contains only one pole at the origin.

Skew reduction

- Skew between data and buffered clock

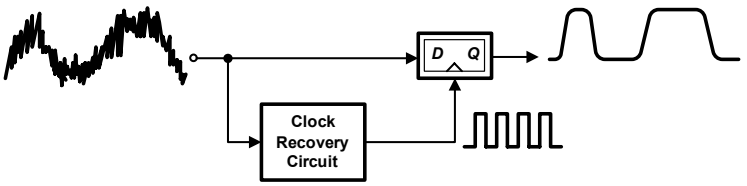


- Use of a PLL to eliminate skew



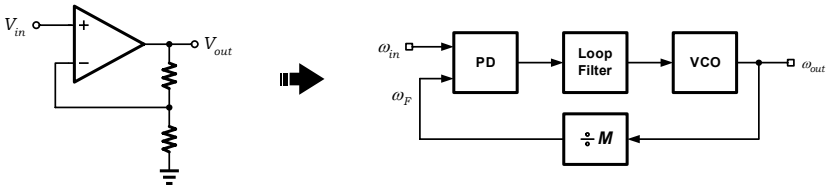
Data Recovery (Jitter reduction)

- Retiming data with D flipflop driven by a low-noise clock



  - Random binary signals experience jitter because
    - crosstalk on the chip and in the package,
    - package parasitics,
    - additive electronic noise of devices, etc.
  - The idea is to resample the midpoint of each bit by a D flipflop that is driven by a low-noise clock.
  - Clock recovery circuit (CRC): The CRC produces the clock from the data. Employing phase locking with a relatively narrow loop bandwidth, the CRC minimizes the effect of the input jitter on the recovered clock.

Frequency multiplication

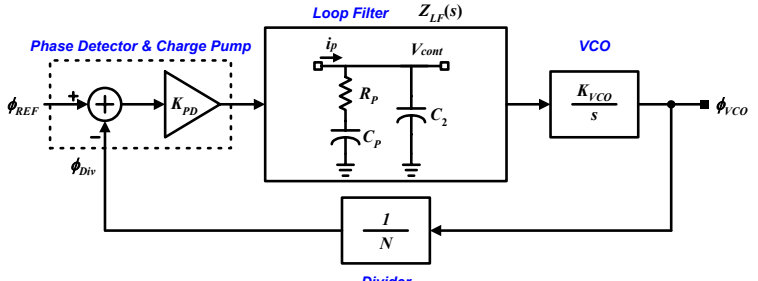


- When the loop is locked, $\omega_F = \omega_{in}$, and hence $\omega_{out} = M \cdot \omega_{in}$. The divide ratio of M is called the "modulus."
- Frequency multiplication also amplifies the input phase noise. For example, the magnitude of phase noise components within the −3dB bandwidth of the PLL is multiplied by a factor of approximately M.

Phase-Locked Loops

Behavior Simulation

Linear model of 3rd-order PLLs



Loop filter: $Z_{LF}(s) = \dfrac{1 + s\tau_z}{s(C_P + C_2)(1 + s\tau_p)}$ with $\tau_z = R_P \cdot C_P$ and $\tau_p = R_P \cdot (C_P^{-1} + C_2^{-1})^{-1}$.

Open-loop transfer function: $GH(s) = \dfrac{I_P \cdot K_{VCO}}{2\pi \cdot N} \cdot \dfrac{1 + s\tau_Z}{s^2(C_P + C_2) \cdot (1 + s\tau_P)}$

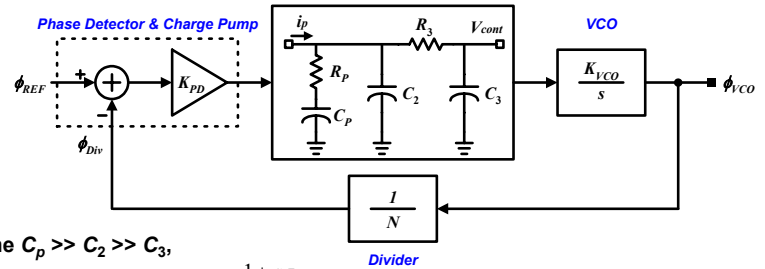
⇨ **Crossover frequency** $\omega_C \approx \dfrac{I_P \cdot R_P \cdot K_{VCO}}{2\pi \cdot N} \cdot \dfrac{C_P}{C_P + C_2}$

Gain margin $GH(s)\big|_{s=j\omega} = -\dfrac{I_P K_{VCO}}{2\pi \cdot N} \cdot \dfrac{(1 + j\omega\tau_Z)}{\omega^2(C_P + C_2) \cdot (1 + j\omega\tau_P)}$

Phase margin $\phi(\omega) = 180^\circ + \tan^{-1}(\omega\tau_Z) - \tan^{-1}(\omega\tau_P)$

Linear model of 4rd-order PLLs

$Z_{LF}(s) = \dfrac{sR_1C_1 + 1}{s^3R_1R_3C_1C_2C_3 + s^2[R_1C_1(C_2 + C_3) + R_3(C_1 + C_2)C_3] + s(C_1 + C_2 + C_3)}$



Assume C_p >> C_2 >> C_3,

Loop filter: $Z_{LF}(s) \approx \dfrac{1 + s\tau_Z}{sC_P(1 + s\tau_{P1}) \cdot (1 + s\tau_{P2})}$ with $\tau_z = R_P \cdot C_P$, $\tau_{P1} = R_1C_2$ and $\tau_{P2} = R_3C_3$.

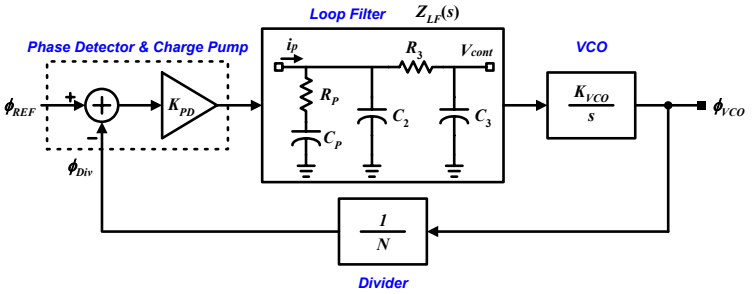
Open-loop transfer function: $GH(s) \approx \dfrac{I_P \cdot K_{VCO}}{2\pi \cdot N} \cdot \dfrac{1 + s\tau_Z}{s^2C_P \cdot (1 + s\tau_{P1}) \cdot (1 + s\tau_{P2})}$

⇨ **Crossover frequency** $\omega_C \approx \dfrac{I_P \cdot R_P \cdot K_{VCO}}{2\pi \cdot N}$

Gain margin $GH(s)\big|_{s=j\omega} \approx -\dfrac{I_P K_{VCO}}{2\pi \cdot N} \cdot \dfrac{(1 + j\omega\tau_Z)}{\omega^2 C_P \cdot (1 + j\omega\tau_{P1}) \cdot (1 + j\omega\tau_{P2})}$

Phase margin $\phi(\omega) \approx 180^\circ + \tan^{-1}(\omega\tau_Z) - \tan^{-1}(\omega\tau_{P1}) - \tan^{-1}(\omega\tau_{P2})$

Linear model of 4rd-order PLLs



Design the extra pole ω_{p2} on the top of ω_{p1} by taking $\tau_{p2} = \tau_{p1}$.

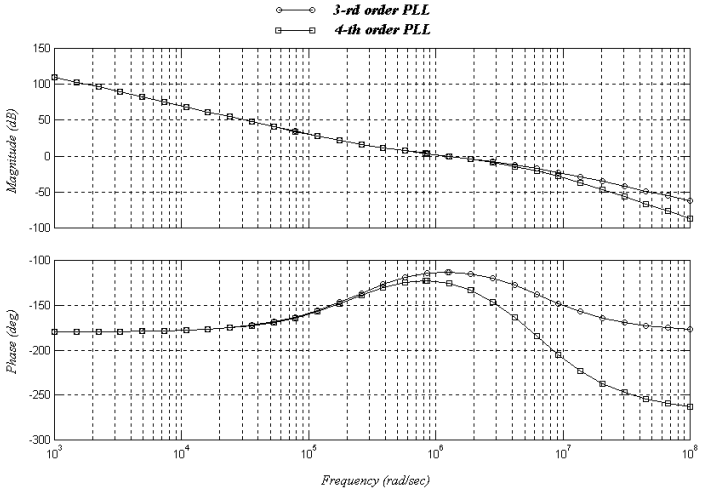
⇨ **$\tau_{p2} = R_3 \cdot C_3 = (\lambda R_3) \cdot (C_3 / \lambda)$ with $\lambda > 10$.**

⇨ **Crossover frequency** $\omega_C \approx \dfrac{I_P \cdot R_P \cdot K_{VCO}}{2\pi \cdot N}$

Gain margin $GH(s)\big|_{s=j\omega} \approx -\dfrac{I_P K_{VCO}}{2\pi \cdot N} \cdot \dfrac{(1+j\omega\tau_Z)}{\omega^2 C_P \cdot (1+j\omega\tau_{P1})^2}$

Phase margin $\phi(\omega) \approx 180^\circ + \tan^{-1}(\omega\tau_Z) - 2\tan^{-1}(\omega\tau_{P1})$

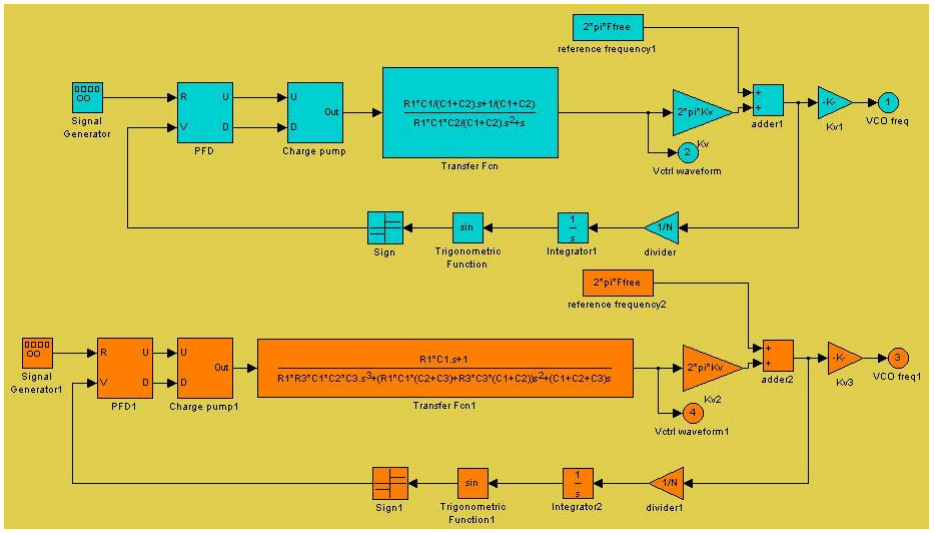
Bode diagram of 3rd-order and 4rd-order PLLs



Choose $\omega_C = 2\pi \times 200$ Krad/s and $\gamma = 5$

⇨ $N = 50$, $K_v = 50$ MHz/V, $I_P = 100$ μA, $R_1 = 13.4$ KΩ, $C_1 = 237$ pF, $C_2 = 16$ pF, and $\lambda = 12$.

Simulink behavior simulation of 3rd-order and 4rd-order PLLs



Transient of 3rd-order and 4rd-order PLLs

f_{REF} = 20 MHz
f_{VCO}: 900 → 1000 MHz