A 1-V 9.8-ENOB 100-kS/s Single-Ended SAR ADC With Symmetrical DAC Switching Technique for Neural Signal Acquisition

Chao Yuan[1], Kian Ann Ng[1,2], Yong Ping Xu[2], Shih-Cheng Yen[1,2] and Nitish V. Thakor[1,2]
[1]Singapore Institute for Neurotechnology (SiNAPSE), National University of Singapore, Singapore
[2]Dept. of Electrical and Computer Engineering, National University of Singapore, Singapore
Email: yuan000042@gmail.com, ngkianann@nus.edu.sg

***Abstract*—This paper reports a high-performance low-power and area-efficient single-ended SAR ADC for neural signal acquisition. The proposed 10-bit ADC features a novel symmetrical DAC switching technique that resolves the signal-dependent comparator offset voltage problem in conventional single-ended SAR ADCs, and improves the ADC's ENOB. Combined with an existing LSB single-sided switching method, the proposed switching scheme reduces DAC switching energy by 92% and capacitor array area by 50%. Besides, the proposed ADC also eliminates the need for any power consuming V_{cm} generation circuit, making it more suitable for low-power System-on-Chip (SoC) integration. The 10-bit prototype ADC is fabricated in a standard 0.18-μm CMOS technology. Operating at 1.0 V power supply and 100 kS/s, the proposed ADC achieves 58.83 dB SNDR and 63.6 dB SFDR for a 49.06 kHz input signal. The maximum ENOB is 9.8-bit for low frequency input signal; and the minimum ENOB is 9.48-bit at the Nyquist input frequency. The average power consumption is 1.72 μW and the figure-of-merit (FoM) is 24.1 fJ/conversion-step.**

I. Introduction

Accurately sampling and recording neural signals is one of the key factors in neural prosthesis development. A typical nerve signal acquisition chain consists of multi-channel neural amplifiers, analog multiplexers and an analog-to-digital converter (ADC) [1], among which the ADC is one of the most critical and power consuming components. For such an application, a single-ended SAR ADC is usually adopted for its low power and small area compared with its differential counterpart.

Fig. 1 shows three commonly used SAR ADC architectures. The conventional single-ended SAR ADC consists of one set of binary-weighted capacitor array. The bottom-plates of each capacitor are switched to V_{ref} or ground during conversion. The ADC structure in Fig. 1(a) requires a dedicated sampling capacitor C_s, thus consuming additional silicon area. In addition, the comparator must be implemented by a pre-amplifier with a dynamic latch in order to alleviate the signal-dependent offset voltage in the dynamic comparator, which consumes additional static current. Lastly, a rail-to-rail comparator is needed if the input signal range is extended to supply rail, as in [1] [2]. This inevitably increases ADC power consumption. Fig. 1(b) shows the improved structure that resolves the dynamic comparator offset issue. However, a common-mode voltage, V_{cm}, is required since the DAC top-plate samples this voltage and the positive input terminal of the comparator is connected to V_{cm} all the time. This third reference voltage (V_{cm}) must be generated on chip by either a resistor divider or a bandgap reference with an analog buffer [3]–[5], which significantly increases system power consumption. In addition, for both (a) and (b), most of the ADC power is consumed in the DAC capacitor array because the conventional switching scheme is energy-inefficient [6]. A widely used low-power DAC structure with a bridging capacitor, as shown in Fig. 1(c), can significantly reduce DAC power consumption and is applicable to both (a) and (b). However, it does not resolve the comparator offset problem and still requires the V_{cm} generation circuits. Furthermore, the bridging capacitor introduces parasitic capacitance, which degrades ADC linearity, and requires complex calibration algorithms.

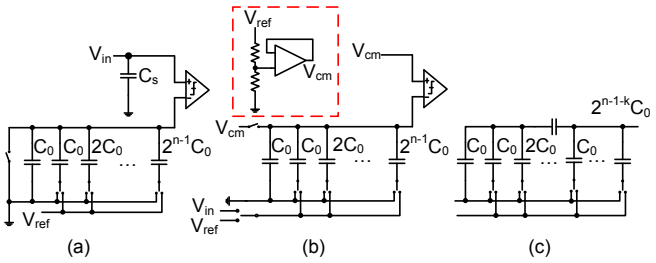

Fig. 1. Conventional single-ended SAR ADC architectures

In this paper, a 10-bit single-ended SAR ADC for multi-channel neural signal acquisition is proposed to address the comparator offset issue and reduce DAC power consumption. The proposed symmetrical DAC switching technique is realized by sampled passive single-end-to-differential conversion and bottom-plate charge-averaging. The rest of this paper is organized as follows. Section II describes the architecture of the proposed ADC and design concept of the proposed switching scheme. Section III presents the measurement results and comparison with the state-of-the-art. Conclusion is drawn in section IV.

II. ADC Architecture

The architecture of the proposed SAR ADC is shown in Fig. 2. The ADC consists of two identical binary-weighted capacitor arrays. Each capacitor array has $2^{n-2}C_0$ capacitors for n-bit ADC, where C_0 is the unit capacitor. Therefore, the total capacitance of the n-bit ADC is $2^{n-1}C_0$, which is 50% less compared to a conventional SAR ADC. A distinctive feature of the proposed ADC is that the DACN-side capacitor array is separated into two by a switch S_{TN}, which is implemented by a minimum-sized NMOS with bootstrapped gate voltage to

978-1-4673-7191-9/15/$31.00 ©2015 IEEE

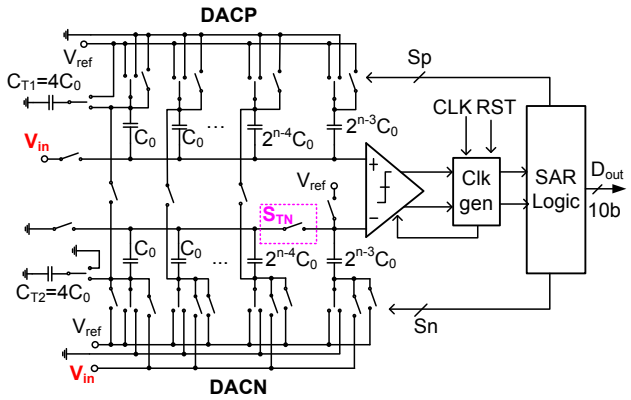

Fig. 2. Proposed SAR ADC architecture

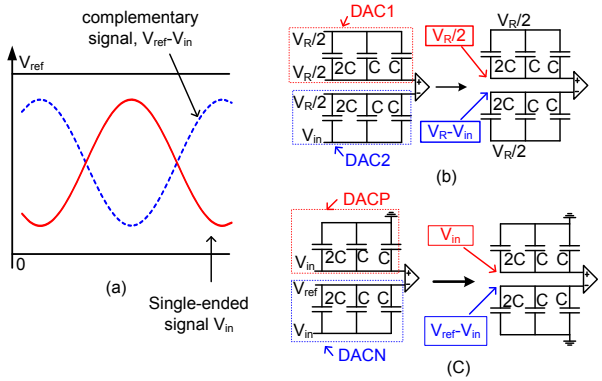

Fig. 3. (a) A continuous-time single-ended signal and its complementary signal, (b) the sampling phase and MSB conversion phase of ADC in [7], and (c) the proposed sampled passive single-ended-to-differential conversion.

reduce its source and drain parasitic capacitances. This allows the DACN-side array to sample different voltage levels on the top-plates. Capacitors C_{T1} and C_{T2} are used for the LSB single-sided switching as demonstrated in [4].

A similar capacitor array structure employed in a single-ended ADC is also reported in [7]. However, operation of the proposed design is completely different from that of [7]. In [7], the input voltage is only sampled on one side of the array whereas the proposed design samples input voltage on both capacitor arrays, that is, the top-plate of DACP and bottom-plates of DACN. The DAC switching in [7] is single-sided and the other DAC array remains un-switched during conversion. This makes the design in [7] vulnerable to signal-dependent comparator offset voltage. In the proposed ADC, except for the MSB conversion step, both capacitor arrays are switched simultaneously and symmetrical switching is achieved. As described in the later part of the Section, with the proposed switching technique, the third voltage reference V_{cm} is not needed. In our design, V_{ref} is chosen to be V_{DD}.

A. Sampled Passive Single-ended-to-differential Conversion

Fig. 3 illustrates the concept of sampled passive single-ended-to-differential conversion proposed in this work, which is inspired from [7]. A single-ended signal, V_{in} and its complementary signal, $V_{ref} - V_{in}$ are shown in Fig. 3(a). For continuous-time signal, this is usually accomplished by using a fully differential amplifier, which consumes a large amount of power.

Fig. 3 (b) shows the sampling phase and MSB-conversion phase of ADC in [7]. The top-plate voltage of DAC2 after sampling phase is $V_R - V_{in}$, which equals to the desired complementary signal. For the proposed ADC after sampling phase, the top-plate voltages of DACP and DACN are V_{in}, and $V_{ref} - V_{in}$, respectively. In this way, the sampled input and its complementary signals are obtained. The details of the conversion are described in Section II(b). It is observed that the comparator input signal swing of the proposed ADC is twice of that of the ADC in [7] as well as the conventional ones. Doubling the comparator input voltage swing improves ADC SNR for the same comparator noise characteristics.

B. Symmetrical DAC Switching Procedures

The switching sequence of the proposed ADC is depicted in Fig. 4. The quantitative switching energy consumption E in each switching phase and the digital output bit b_i are also indicated in the figure. Fig. 4 (a) and (b) show the actual implementation of the sampled passive single-ended-to-differential conversion. After this phase, the MSB b_0 is determined and the MSB capacitor can be switched to their corresponding voltage levels, as shown in phase (c). In the following phase, the rest of the capacitors are switched for bottom-plate charge-averaging. This is slightly different from [3] and [4] since all the capacitors in [3] and [4] are connected for charge-averaging, which makes the two DAC arrays completely floating. This could result in a situation that the bottom-plate voltage level drifts far away from the desired $V_{ref}/2$, causing DACP and DACN top-plate voltage moving beyond supply rail. In the proposed switching scheme, such a problem is eliminated since the MSB capacitors $(2C)$ are connected to known voltage levels, providing reference voltage for the DAC arrays and forcing the bottom-plate voltage of the rest capacitors close to $V_{ref}/2$.

The DAC output waveforms of conventional and the proposed SAR ADCs are depicted in Fig. 5. The conventional single-

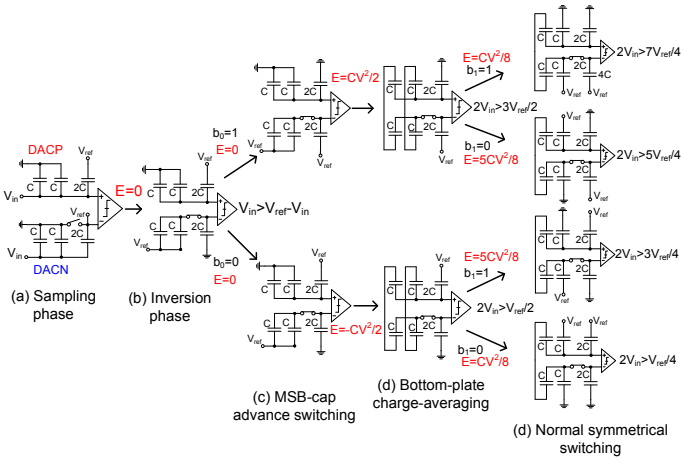

Fig. 4. The switching sequence of the proposed ADC for 4-bit case. The last bit conversion is using LSB single-sided switching technique discussed in [4] and not shown in this graph.

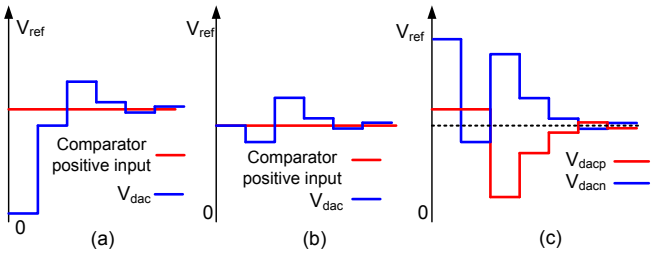

Fig. 5. DAC output waveforms of (a) (b) conventional and (c) the proposed single-ended SAR ADC.

ended SAR ADC has only one capacitor array. Hence, the comparator positive input terminal voltage is fixed during a conversion cycle. As shown in Fig. 5 (c), the proposed SAR ADC has symmetrical DAC switching, making the proposed ADC insensitive to dynamic comparator offset voltage. The DAC waveform of [7] is similar to Fig. 5(b) but it converges to two predefined values, $V_{ref}/2$ and ground, where a dedicated $V_{ref}/2$ is needed. In the proposed ADC, the third voltage level, indicated by the dotted line in (c), is inexplicitly generated by bottom-plate charge averaging.

C. Switching Energy

A comparison of DAC switching energy in the conventional, charge-recycle [6] and the proposed single-ended ADCs, is shown in Fig. 6. Other switching techniques discussed in [3]–[5] are designed for fully-differential SAR ADCs and cannot be directly translated into a single-ended design. Therefore they are not included in the comparison. The average switching energy of the proposed switching scheme is $58.08CV^2$, which is about 92% and 87.5% less than the conventional and charge recycle single-ended SAR ADCs, respectively. The energy saving comes from three aspects. Firstly, during the MSB conversion, the proposed design does not consume any energy as compared to the conventional and charge-recycle switching schemes, which consume the most switching energy during this phase. Secondly, the switching of capacitors for the remaining conversion steps is from a virtual voltage level, V_{cm} to V_{ref} or to ground. The voltage difference is only around $V_{ref}/2$, which is half of that in the conventional and charge-recycle SAR ADCs. Thirdly, the total DAC capacitance is reduced by half by using the LSB switching technique proposed in [4]. Hence, the switching energy is reduced significantly since E is proportional to CV^2. Although the proposed design requires extra clock cycles and additional digital circuit, low-power operation is still achieved because DAC power reduction overweighes the digital overhead.

It is noted that the switching energy curve for the proposed ADC is divided into two parts with similar shape at the middle code, 512. This is evident from the transition from (c) to (d) in Fig. 4. For input level higher than $V_{ref}/2$, the switching energy is $0.5CV_{ref}^2$. For input lower than $V_{ref}/2$, the switching energy drawn from V_{ref} during this transition is $-0.5CV_{ref}^2$. The difference for the 4-bit example is CV_{ref}^2. For 10-bit case, the difference is $64CV_{ref}^2$ and this can be verified in Fig. 6. The negative switching energy implies DAC capacitor array dumps charge into the reference voltage and it comes from the energy stored in the capacitors in previous phase.

III. Measurement Results

The 10-bit ADC was fabricated in a 1P6M 0.18-μm CMOS technology. Fig. 7 shows the chip microphotograph. The ADC core area is 360 μm $\times$ 380 μm. The unit capacitor measures 4 μm $\times$ 4 μm, and has a value 34 fF, which is determined by the matching requirement for 10-bit accuracy. The total DAC capacitance is about 18 pF.

Fig. 8 shows the measured DNL and INL at 1V supply voltage. The DNL deteriorates to -0.5 LSB at midcode, 512. This is due to the charge-sharing caused by top-plate parasitic capacitance C_p at the DACN-side during the inversion phase. The absolute DNL at micode is approximately given by $(C_p/C_0)\,LSB$. In our design, the top-plate parasitic capacitance is about 15 fF obtained from parasitic extraction, which leads to the 0.5 LSB DNL. The DNL for other codes is confined within +/- 0.15 LSB. The INL is within -0.42/+0.45 LSB.

Fig. 9 shows the 8192-point FFT plot of the ADC ouput spectrum for input frequencies at 10.78 kHz (neural signal recording

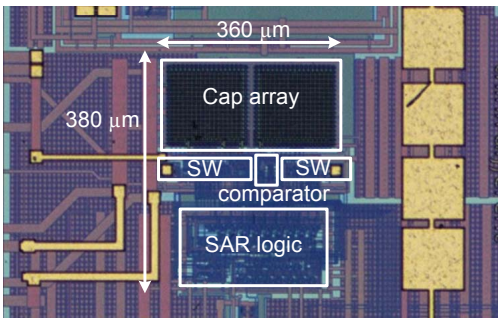

Fig. 7. Chip microphotograph

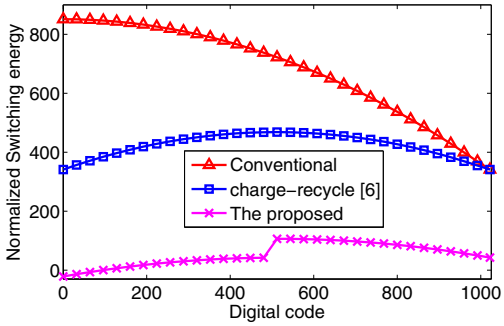

Fig. 6. Comparison of DAC switching energy

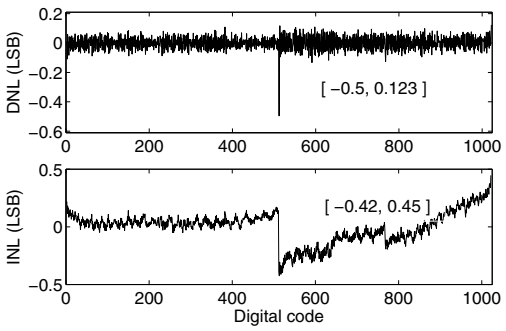

Fig. 8. Measured linearity at 1.0 V and 100 kS/s

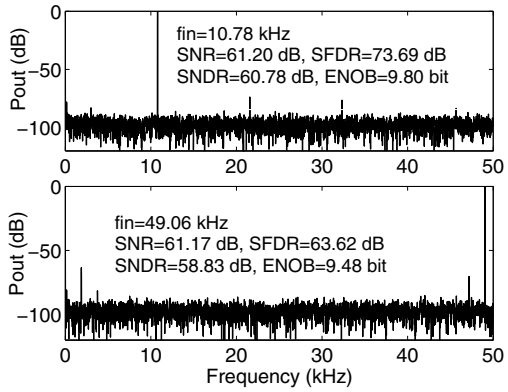

Fig. 9. Measured output spectrum at 1.0 V supply and 100 kS/s.

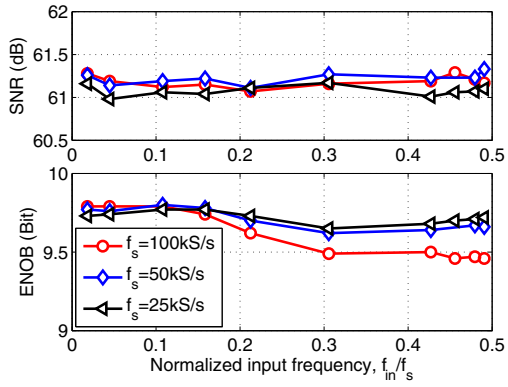

Fig. 10. Measured SNR and ENOB at different sampling rates under 1.0 V supply voltage.

bandwidth is usually 8-10 kHz) and 49.06 kHz, respectively. The ENOB is 9.8-bit for low-frequency input and 9.48-bit at Nyquist input frequency.

The ADC is also characterized at other sampling rates. Fig. 10 shows the measured SNR and ENOB versus input signal frequency at different sampling rates. The SNR is approximately 61 dB and is consistent for different sampling rates. The slight deterioration of ADC ENOB at higher input signal frequency is attributed to the on-resistance change of the bootstrapped sampling switches, which causes harmonic distortion.

The measured power consumption of the ADC at 1.0V supply and 100 kS/s is 1.72 μW. The analog circuit including capacitor array and the dynamic comparator consumes 0.7 μW and the digital circuit consumes 1.02 μW. The resulting FoM at 100 kS/s equals to 24.1fJ/conversion-step, by taking ENOB of 9.48-bit at Nyquist input frequency.

Compared to existing state-of-the-art single-ended ADCs with similar operating speed and in the same technology node, this design achieves the best ENOB. A detailed comparison of key performance parameters is summarized in Table I. It is worthwhile to note that the input voltage swing for designs [1] [2] [7] is twice of the reference voltage, which means these designs would require either on-chip [1] or off-chip [2] [7] generation for the third reference voltage. The FoM of these designs should be worse than the reported if the power consumption of $V_{ref}/2$ generation circuit and buffer is included. The ADC in [8] has an on-chip V_{cm} generation circuit. However, this design requires

TABLE I
COMPARISON WITH STATE-OF-THE ART

	[1]	[2]	[7]	[8]	**This work**
Technology	0.18μm	0.18μm	0.18μm	0.13μm	0.18μm
Arachitecture	SAR	SAR	SAR	SAR	SAR
Topology	All are single-ended designs				
Power Supply (V)	0.45	0.9	1.1	0.8	1.0
V_{ref} (V)	0.45	0.9	0.6	0.8	1.0
Input Swing (V)	0.9	1.8	1.2	0.8	1.0
$V_{ref}/2$ Buffer	on-chip	off-chip	off-chip	on-chip	**Not needed**
Resolution	9	9	8	10	10
fs (kS/s)	200	100	2	1000	100
ENOB (bit)	8.27	8.02	7.4	8.8	**9.48**
Power (μW)	1.35	1.33	0.027	12.2	**1.72**
Area (mm^2)	–	0.151	0.06	0.056	0.118
FoM (fJ/c-s)	22	51.3	79.9	27	**24.1**

off-chip biasing circuit and manual calibration. For the proposed design, FoM is superior to most of other single-ended designs in literature.

IV. CONCLUSION

In this paper, an ultra low-power 10-bit single-ended SAR ADC for neural signal acquisition is presented. By employing a novel symmetrical DAC switching technique, the proposed single-ended ADC not only overcomes existing issues such as signal-dependent comparator offset voltage, but also reduced DAC power consumption. In addition, this ADC is self-contained and does not require explicit third reference voltage generation circuit, making it more power efficient. Operating at 1.0V supply and 100 kS/s, the proposed ADC achieves ENOB as high as 9.8-bit for low input frequency and 9.48-bit at Nyquist input frequency.

ACKNOWLEDGMENT

This work was supported by National Research Foundation (NRF), Singapore under grant NRF-CRP10-2012-01. The authors would like to thank the staff at Institute of Microelectronics (IME), A*Star, Singapore and SiNAPSE for chip layout and chip testing support, respectively.

REFERENCES

[1] D. Han, Y. Zheng, R. Rajkumar, G. H. Dawe and M. Je, "A 0.45 V 100-channel neural-recording IC with sub-μW/channel consumption in 0.18 μm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2013, pp. 290-291.

[2] H. Tang, Z. C. Sun, K. W. Chew and L. Siek, "A 1.33 μW 8.02-ENOB 100 kS/s Successive Approximation ADC With Supply Reduction Technique for Implantable Retinal Prosthesis," *IEEE Trans. Biomed. Circuits Syst.*, Vol. 8, No. 6, pp. 844-856, Dec. 2014.

[3] Y. F. Chen, S. Tsukamoto and T. Kuroda, "A 9b 100MS/s 1.46mW SAR ADC in 65nm CMOS," in *Proc. IEEE Asian Solid-State Circuits Conf.*, 2009, pp. 145-148.

[4] X. L. Zhu, Y. F. Chen, S. Tsukamoto and T. Kuroda, "A 9-bit 100MS/s Tri-level Charge-Redistribution SAR ADC with asymmetric CDAC Array," in *Proc. IEEE Int. Symp. VLSI Design, Automation, and Test*, 2012, pp. 1-4.

[5] Y. Zhu, C. H. Chan, U. F. Chio, S. W. Sin, S. P. U, R. P. Martins and F. Maloberti, "A 10-bit 100-MS/s Reference-Free SAR ADC in 90nm CMOS," *IEEE J. Solid-State Circuits*, Vol. 45, No. 6, pp. 1111-1121, Jun. 2010.

[6] B. P. Ginsburg and A. P. Chandrakasan, "An energy-efficient charge recycling approach for a SAR converter with capacitive DAC," in *Proc. IEEE Int. Symp. Circuits Syst.*,2005, pp. 184-187.

[7] W. B. Hu, Y. T. Liu, T. Nguyen, D. C. Lie and B. P. Ginsburg, "An 8-bit Single-Ended Ultra-Low-Power SAR ADC with a Novel DAC Switching Method and a Counter-Based Digital Control Circuit," *IEEE Trans. Circuits Syst. I, Reg. Papers*, Vol. 60, No. 7, pp. 1726-1739, Jul. 2013.

[8] Y. H. Tao and Y. Lian, "A 0.8-V, 1-MS/s, 10-bit SAR ADC for Multi-Channel Neural Recording," *IEEE Trans. Circuits Syst. I, Reg. Papers*, Vol. 62, No. 2, pp. 366-375, Feb. 2015.