Dithered Timing Spread Spectrum Clock Generation for Reduction of Electromagnetic Radiated Emission from High-speed Digital System

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Abstract

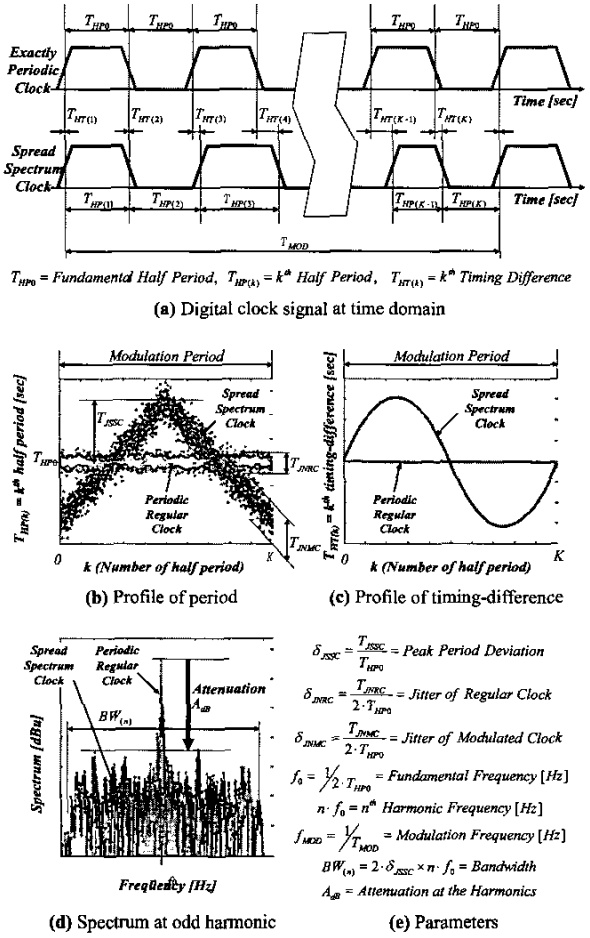
In the modern digital systems, the most amount of the radiation from the system is caused by the high-speed digital clock signal. As a method to reduce the electromagnetic radiation from the system clock, the spread spectrum clock technique that modulates the system clock frequency had been introduced. The conventional spread spectrum clock is realized by controlling the period or the frequency using a phase locked loop. Because of the inherent jitter of the phase locked loop, the attenuation of the spectrum decreased and the realization is very difficult at the higher clock frequency near the GHz. In this paper, we propose a dithered timing spread spectrum clock. The proposed dithered timing spread spectrum clock is realized by controlling the transition timing-difference using a delayer. The proposed dithered timing spread spectrum clock has more effective suppression of the electromagnetic radiation from the high-speed digital system than the conventional spread spectrum clock.

Keywords

Spread Spectrum Clock, Dithered Timing, and EMI Reduction.

INTRODUCTION

Since the digital clock is the periodic and the highest frequency signal in the digital system, all of its energy is concentrated on narrow frequency band consisting of the fundamental frequency and its harmonics. In general, the most critical interconnection lines are those carrying the system clock because they are the primary sources of the electromagnetic radiation and interference. In the modern digital systems, the most amount of the radiation from the system is caused by the high-speed digital clock signal [4]. As a method to reduce the radiation from the system clock, the spread spectrum clock (SSC) technique that modulates the system clock frequency had been introduced [1], [2]. Recently, this technique that was adopted by some commercial electronic products such as personal computer has shown good performance on the suppression of the electromagnetic radiation and interference [3], [5].



(a) Digital clock signal at time domain

(b) Profile of period (c) Profile of timing-difference

(d) Spectrum at odd harmonic (e) Parameters

Figure 1. Parameters for the periodic regular clock and the spread spectrum clock (SSC) with triangular modulation profile

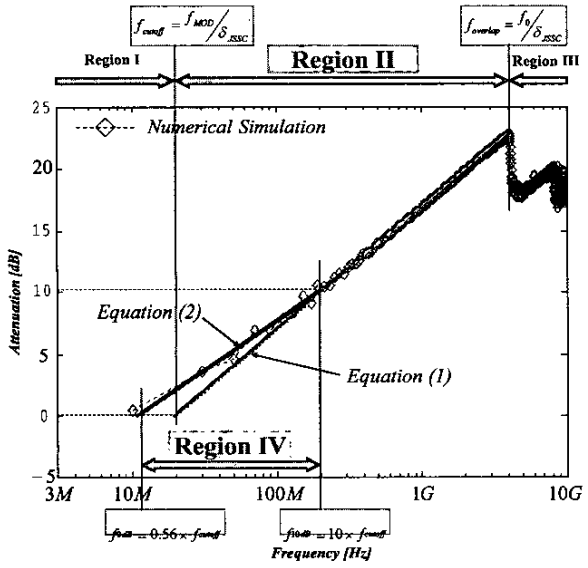
The SSC has voltage waveform at time domain as Figure 1(a). There are various modulation profiles for the SSC technique such as random pulses, sinusoidal, triangular, and SSCG modulation profiles [1], [2], [3]. We are interested in the triangular modulation profile. The modulation profile of the period or the frequency is

triangular as shown in Figure 1(b) [7] [9]. The half period is represented by $T_{HP(k)}$ as shown in Figure 1(b). Simultaneously, we can easily find the transition timing-difference, $T_{HT(k)}$, between the exactly periodic clock and the SSC as shown in Figure 1(c). The suppression of the maximum spectrum at the n^{th} harmonic is represented in Figure 1(d). Some important parameters such as attenuation A_{dB}, fundamental frequency f_0 of periodic regular clock, modulation frequency f_{MOD} of SSC, peak period or frequency deviation (modulation rate) δ_{JSSC} of SSC, unintentional jitter δ_{JNRC} of regular clock, unintentional jitter δ_{JNMC} of SSC, and n^{th} harmonic frequency $n \cdot f_0$ can be defined as shown in Figure 1(e).

The attenuation at considerable harmonics is depicted at Figure 2. It can be divided into three regions denoted as I, II, and III by the cutoff f_{cutoff} and the overlap $f_{overlap}$ frequencies. In the Region I, the attenuation is always 0 dB. We cannot suppress the radiation even using the SSC technique in this region. The region III represents the attenuation where the spread spectra are overlapped between adjacent odd harmonics. The harmonics in the Region III are beyond our consideration in this paper [6].

We are interested in the linear region between the cutoff and the overlap frequencies categorized as Region II. For the clock without considering its unintentional inherent jitter, the attenuation formula is represented by *(1)* in Figure 2. In the Region II, the attenuation is directly proportional to the peak period deviation and the harmonic frequency and inversely proportional to the modulation frequency. If the harmonic frequency or the peak period deviation becomes double, the attenuation increases 3 dB. However, if the modulation frequency becomes double, the attenuation decreases 3 dB. At the same harmonic frequency, though the fundamental frequency is different, the attenuation is identical.

The error of the proposed formula *(1)* in Figure 2 is less than 2 dB if the attenuation is smaller than 10 dB. For more accurate formula, we define Region IV between f_{0dB} and f_{10dB} where attenuations are 0 dB and 10 dB, respectively. In this Region IV, the formula *(1)* is changed to the formula *(2)* in Figure 2. With this formula *(2)*, the error can be expected less than 1dB.



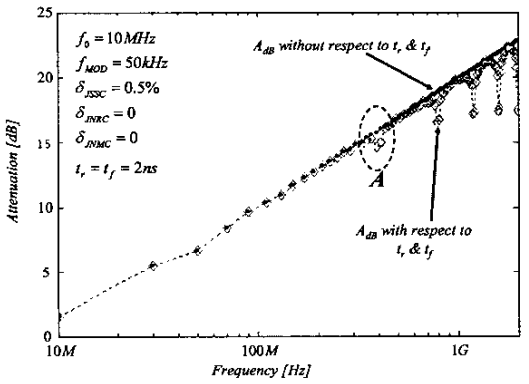
In the Region II

$$A_{dB} = 10 \cdot \log_{10}\left(\frac{\delta_{JSSC} \cdot n \cdot f_0}{f_{MOD}}\right) \qquad (1)$$

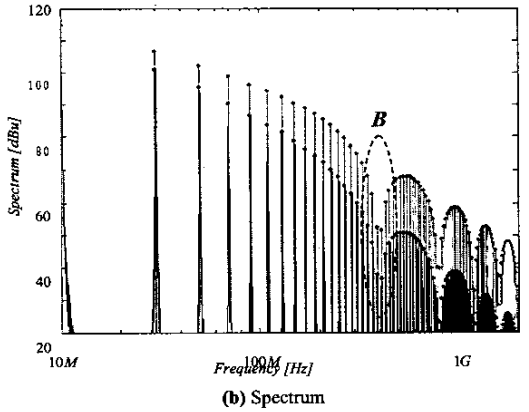
In the Region IV

$$A_{dB} = 8 \cdot \log_{10}\left(\frac{\delta_{JSSC} \cdot n \cdot f_0}{f_{MOD}}\right) + 2 \qquad (2)$$

Figure 2. Attenuation formulas for the ideal SSC with triangular modulation profile [6]



(a) A_{dB}: Attenuation



(b) Spectrum

Figure 3. Attenuation for the SSC with triangular modulation profile with respect to rising and falling time

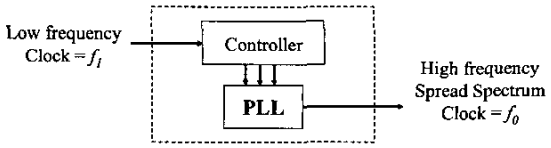
The conventional digital clock has the rising and the falling time about 10 % of its period. In Figure 3(a), the attenuation decreased abruptly in the frequency range marked A, because of area marked B in Figure 3(b). In that frequency range, however, we have no interest in the attenuation. Because the rising and the falling time has no relation to the period, the attenuation shows little difference between with and without the considerations of the rising and the falling time as shown in Figure 3(a). Therefore, for the calculation of the attenuation, the rising and the falling time can be excluded.

We consider the unintentional jitters of the periodic regular clock and the SSC. If the SSC has the unintentional jitter, the attenuation decreased as shown in reference [6]. The decrement of the attenuation is the function of the size and the distribution profile of the unintentional jitter. The decrement of the attenuation caused by the unintentional jitter of the regular clock can be ignored below the frequency of 10 GHz, because the unintentional jitter of the regular clock using the commercial crystal oscillator is less than about 0.001%. However, because the unintentional jitter of the SSC is up to several %, the decrement of the attenuation cannot be ignored. Therefore we consider the unintentional jitter of the SSC only. In most digital system, the unintentional jitter that decreases the attenuation of the maximum spectrum for the SSC is an unavoidable problem.

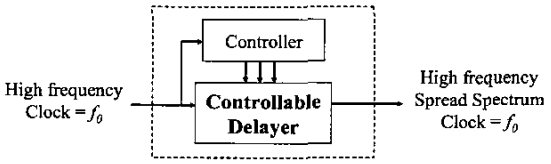
In this paper, we propose a dithered timing spread spectrum clock (DT-SSC) generation technique. For the realization of the SSC, as we mentioned before, we can control the transition timing-difference as well as the period or the frequency as shown in Figure 1(b) and 1(c). The conventional SSC generator using a phase locked loop (PLL) controls the period $T_{HP(k)}$ or the frequency [7], [9]. However, the proposed DT-SSC generator controls the transition timing-difference $T_{HT(k)}$. Two techniques are theoretically identical if we ignore the unintentional jitter. However, two techniques have some difference in the consideration of the unintentional jitter. The proposed DT-SSC has more effective suppression than the conventional SSC using the PLL.

DITHERED TIMING SPREAD SPECTRUM CLOCK

Nowadays, most of SSC generators use the PLL for modulation. The conventional SSC generator has the lower frequency periodic clock input terminal and the higher frequency SSC output terminal as shown in Figure 4(a). In the conventional SSC generator using the PLL, the period is dithered. However, the proposed DT-SSC generator needs the periodic clock input terminal and the SSC output terminal with the same fundamental frequency as shown in Figure 4(b). In the proposed DT-SSC generator using the controllable delayer, the transition timing is controlled. For the higher frequency clock input, for example, the crystal oscillator can be needed. The unintentional jitter of this input clock should be as small as possible.



(a) Conventional spread spectrum clock (Dithered PERIOD Scheme)



(b) Proposed spread spectrum clock (Dithered TIMING Scheme)

Figure 4. The conventional SSC generator using the PLL and the proposed DT-SSCG using the delayer

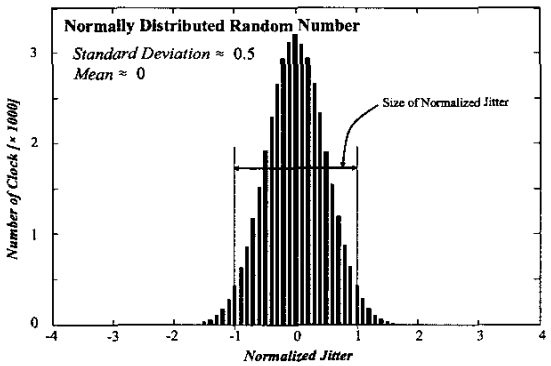


Figure 5. Normalized Jitter Distribution

There are 2 unintentional jitters for the conventional SSC in Figure 4(a). One is the inherent jitter of the input clock and the other is the inherent jitter of the PLL. The former jitter can be ignored by using the crystal oscillator as we mentioned earlier. The inherent jitter of the conventional PLL is about 10 ps (±5 ps) or more. If the fundamental frequency is 1 GHz, the ±5 ps jitter is ±0.5 % of its period. If we intend to realize the SSC with the triangular modulation profile of the ±0.5 % peak period deviation, the intentional jitter to realize the SSC is below about ±5 ps. Because the unintentional jitter of the PLL is not much smaller than the intentional jitter to realize the SSC, the realization of the SSC cannot be easy. Similarly, there are 2 unintentional jitters for the proposed DT-SSC in Figure 4(b). One is the inherent jitter of input clock and the other is the inherent delay jitter of the controllable delayer. The former jitter can be ignored by using the crystal oscillator as we mentioned earlier. Because the unintentional delay jitter of the controllable delayer is much smaller than the period 1 ns, the realization of the proposed DT-SSC is easy. In this paper, the normally distributed random numbers of which mean and standard deviation are 0 and 0.5, respectively, are adopted for the normalized jitter noise distribution as shown in Figure 5.

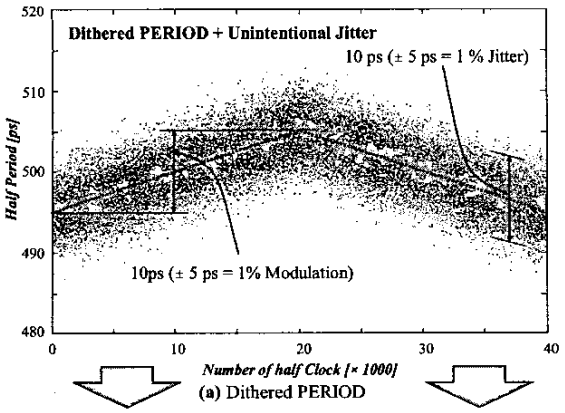


Figure 6. The conventional SSC with the triangular modulation profile (Dithered PERIOD Scheme)

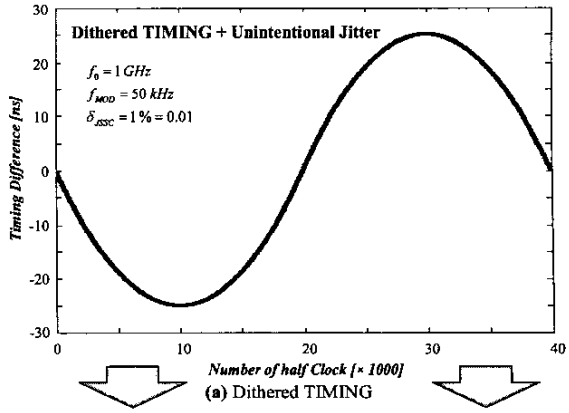


Figure 7. The proposed DT-SSC with the triangular modulation profile (Dithered TIMING Scheme)

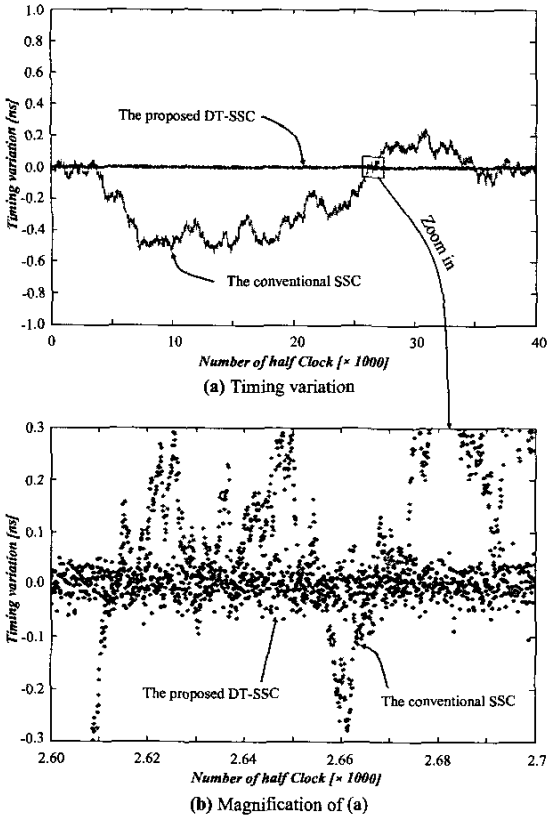
For the comparison of the conventional SSC and the proposed DT-SSC, the signal waveform was generated, and the spectrum profile was calculated by using the Fast-Fourier-Transform (FFT) algorithm. The amount of the suppressed spectrum was calculated at the fundamental and the odd harmonics because a duty cycle is about 50 %. The dithered half period and the dithered timing-difference of the SSC with the triangular modulation profile are represented as shown in Figure 1. The half period is the interval between adjacent transition times of the SSC. The timing-difference is the interval between the n^{th} transition times of the exactly periodic clock and the SSC.

For example, we suppose that the fundamental clock frequency is 1 GHz, the modulation frequency is 50 kHz, and the peak period deviation is ±1 %. The dithered period and the dithered timing-difference for the conventional SSC and for the proposed DT-SSC are represented in Figure 6 and 7, respectively.

For the conventional SSC, the intentional jitter for the SSC and unintentional inherent jitter of the PLL are added to the exact period as shown in Figure 6(a). Consequently, the timing-difference is determined as shown in Figure 6(b). The unintentional inherent jitter of the PLL is ±10 ps that are the ±1 % of 1ns period.

For the proposed DT-SSC, the intentional jitter for the SSC and unintentional delay jitter of the controllable delayer are added to the exact timing as shown in Figure 7(a). Consequently, the period is determined as shown in Figure 7(b). The unintentional propagation delay jitter of the controllable delayer is ±10 ps that are the ±1 % of 1 ns period. The resulted unintentional jitter of the half period is about 14 ps that are the 1.4 % of 1 ns period as shown in Figure 7(b). The resulted unintentional jitter of the period in the proposed DT-SSC is higher than that in the conventional SSC if the jitter of the PLL and the jitter of the controllable delayer are same.

The timing variation between SSCs with and without the unintentional jitter is shown as Figure 8. In other words, Figure 8 shows the difference between the transition times of the ideal SSC without any unintentional jitter and the conventional or proposed SSC with the unintentional jitter. The timing variation of the conventional SSC is about several hundred ps and cannot predict the waveform as shown in Figure 8(a). The timing variation of the proposed DT-SSC is about several ten ps. The timing variation of the proposed DT-SSC is much smaller than that of the conventional SSC.



(a) Timing variation

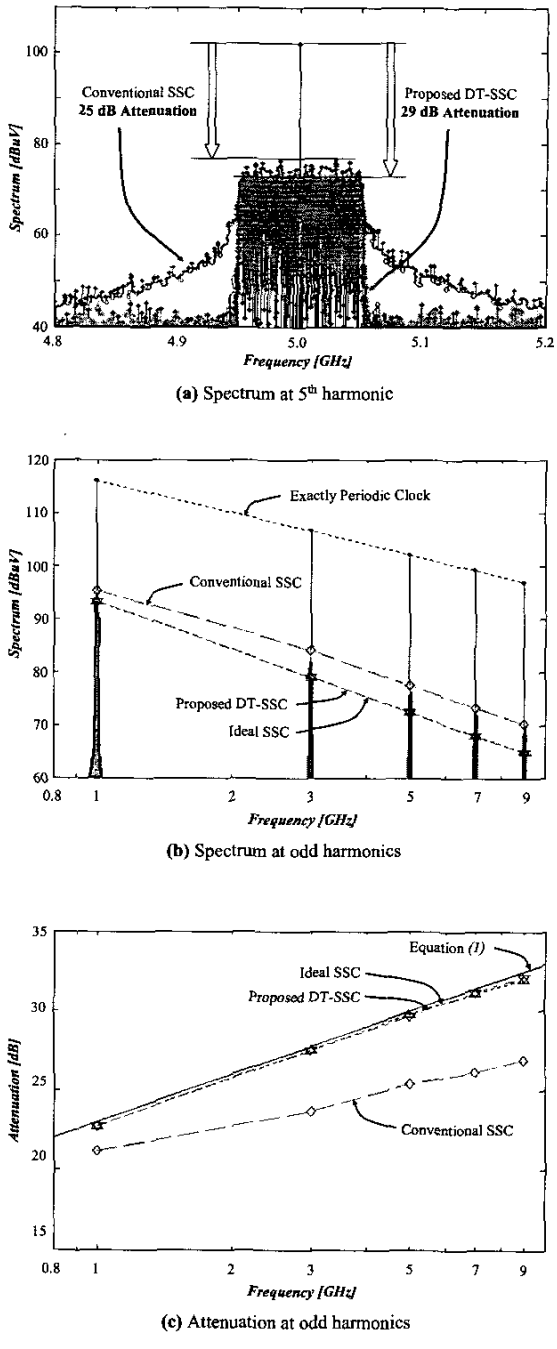
(b) Magnification of (a)

Figure 8. The timing variation between the SSCs with without the unintentional jitter

ATTENUATION OF PROPOSED DT-SSCG

As the modulation profiles for the conventional SSC and the proposed DT-SSC are determined by Figure 6 and 7, the spectrum and the attenuation are represented as Figure 9. At the 5th harmonic of 5 GHz, the maximum spectrum can be reduced about 25 dB by the conventional SSC and can be reduced about 29 dB by the proposed DT-SSC. The proposed DT-SSC has the additional 4 dB compared to the conventional SSC as shown in Figure 9(a). Even though the resulted unintentional jitter of the period in the proposed DT-SSC is higher than that in the conventional SSC, the attenuation of the maximum spectrum using the proposed DT-SSC is higher than that using the conventional SSC. The attenuation calculated by using the formula *(1)* is 30 dB and is similar to the attenuation using the proposed DT-SSC.

As shown in figure 9(b), the spectra for the exactly periodic regular clock, for the ideal SSC without the unintentional jitter, for the conventional SSC with the inherent jitter of the PLL, and for the proposed DT-SSC with the propagation delay jitter, are represented. The spectrum was found at the fundamental and the odd harmonics because a duty cycle is about 50 %. The attenuation of the maximum spectrum at odd harmonics as shown in Figure 9(c) can be derived from Figure 9(b).



(a) Spectrum at 5th harmonic

(b) Spectrum at odd harmonics

(c) Attenuation at odd harmonics

Figure 9. The Spectrum and the Attenuation for the ideal SSC without the unintentional jitter, for the conventional SSC with the unintentional inherent jitter of the PLL, and for the proposed DT-SSC with the unintentional propagation delay jitter of the controllable delayer

The proposed DT-SSC has more effective suppression of the electromagnetic radiation than the conventional SSC. Even though the proposed DT-SSC has the unintentional propagation delay jitter ±1.0 % of the period, the attenuation of the proposed DT-SSC is similar to that of the ideal SSC without unintentional jitter. Resultantly, if the unintentional jitter is same, the proposed DT-SSC using the controllable delayer has more attenuation than the conventional SSC using the PLL.

CONCLUSION

We proposed the dithered timing spread spectrum clock (DT-SSC) for the suppression of the electromagnetic radiation from the high-speed digital system. The proposed dithered timing spread spectrum clock (DT-SSC) has more effective suppression than the conventional spread spectrum clock (SSC).

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