A 16/32 Gb/s Dual-Mode NRZ/PAM4 SerDes in 65nm CMOS

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***Abstract* —A dual-mode NRZ/PAM4 SerDes seamlessly supports both modulations with a 1-FIR- and 2-IIR-tap DFE receiver and a 4/2-tap FFE transmitter in NRZ/PAM4 modes, respectively. A source-series-terminated (SST) transmitter employs lookup-table (LUT) control of a 31-segment output DAC to implement FFE equalization in NRZ and PAM4 modes with 1.2Vpp output swing and utilizes low-overhead analog impedance control. Optimization of the quarter-rate transmitter serializer is achieved with a tri-state inverter-based mux with dynamic pre-driver gates. The quarter-rate DFE receiver achieves efficient equalization with 1-FIR tap for the large first post-cursor ISI and 2-IIR taps for long-tail ISI cancellation. Fabricated in GP 65-nm CMOS, the transceiver occupies 0.074 mm^2 area and achieves power efficiencies of 10.9 and 5.5 mW/Gbps with 16Gb/s NRZ and 32Gb/s PAM4 data, respectively.**

***Index Terms*—decision feedback equalizer, dual-mode serial link, feed-forward equalizer, impedance tuning, NRZ, PAM4.**

I. Introduction

PAM4 modulation offers the potential to support ever-increasing serial I/O bandwidth density demands due to its lower Nyquist frequency loss, improved spectral efficiency, and lower clock speeds. While dedicated PAM4 transceivers have been developed [1, 2], the majority of serial I/O standards use simple binary NRZ modulation. This motivates the development of dual-mode transceivers which can seamlessly support both NRZ and PAM4 modulation.

This work presents a dual-mode NRZ/PAM4 serial I/O SerDes datapath which can be configured to work in both modes with minimal hardware overhead. In order to achieve high-resolution equalization and level generation in the high-swing voltage-mode source-synchronous-terminated (SST) transmitter, a 31-segment output DAC is controlled by a lookup-table to enable a 4-tap and 2-tap FFE in NRZ and PAM4 mode, respectively. This segmented DAC approach to generate the multiple output levels required by the modulation and equalization eliminates any full-rate tap-select muxes in the output segments [3] which can limit the maximum achievable data rate. Reduced output stage area is achieved with a new low-overhead analog impedance control scheme which obviates additional impedance control segments [4], while the quarter-rate transmitter's serializer bandwidth is improved with a tri-state inverter-based mux with dynamic pre-driver gates. The quarter-rate DFE receiver achieves efficient equalization with 1-FIR tap for the large first post-cursor ISI and 2-IIR taps for long-tail ISI cancellation [5].

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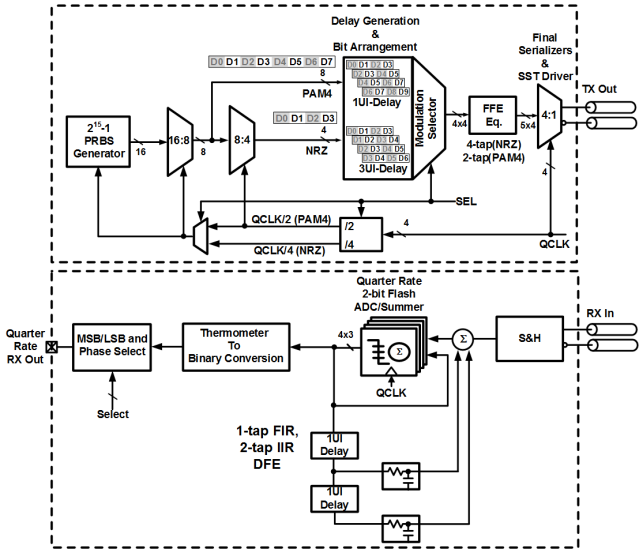

Fig. 1. Proposed dual-mode transceiver architecture.

II. Transceiver Architecture

Fig. 1 shows the proposed dual-mode transceiver block diagram. At the transmitter side, a modulation mode signal selects either a 1/16th or 1/8th symbol-rate clock to control the 16-bit wide pattern generator and initial serialization stages in NRZ and PAM4 mode, respectively, to generate four sets of four-bit patterns which address the LUT equalizer. This allows the realization of a 4-tap FFE in NRZ mode, with a main cursor and up to three pre/post cursor taps, and a 2-tap FFE in PAM4 mode, with a main cursor and either one pre/post cursor tap for the MSB and LSB bits. A 16x5 LUT provides for 5-bit resolution in the output stage level generation, eliminates any full-rate tap-select muxes in the output segments [3], and also allows for potential non-linear equalization. After a retiming stage, a final quarter-rate 4:1 stage serializes the 5-bit resolution LUT output to full rate to drive the 31-segment high-swing source-series-terminated output stage.

The 3-tap DFE receiver, which is described in detailed PAM4 operation in [5], also employs a quarter-rate

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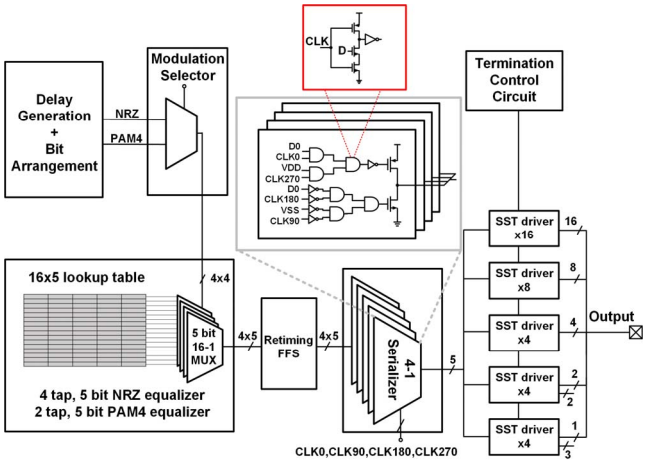

Fig. 2. Proposed transmitter architecture.

architecture. Each data slice consists of three comparators whose thresholds are either set to all zero or to levels corresponding to a 2-bit flash ADC for NRZ and PAM4 mode, respectively. The 3 output bits per slice, which are all the same value for NRZ and thermometer-code for PAM4, control both the DFE's FIR tap to cancel the first post-cursor ISI and 2 IIR taps for long-tail ISI cancellation.

III. Transmitter Circuits

Fig. 2 shows a detailed block diagram of the transmitter from the modulation selection block to the chip output. The final 4:1 serializer is one of the most critical blocks in a quarter-rate transmitter, as it must maintain enough bandwidth to support the full-rate output. This transmitter extends the tri-state inverter-based mux design proposed in [6] to perform 4:1 serialization and further improves power efficiency by utilizing dynamic NAND pre-drivers (Fig. 2). Due to the minimal transistor stacking, simulations indicate that it can achieve the same level of deterministic jitter with a 40% power reduction relative to a conventional pass-gate mux design.

A straight-forward technique to control the output impedance of a high-swing voltage-mode driver involves implementing redundant segments that can be digitally activated to match the channel impedance [4]. However, the presence of these redundant stages results in increased output stage area and power. Instead, this design proposes pseudo-analog control to compensate for large statistical variations in driver output impedance. Fig. 3 shows a schematic of the voltage-mode SST driver segments which supports a 1.2Vpp output swing. Here the main MP and MN switch transistors and Rterm resistors are sized to always yield greater than 50• output impedance over corners, and two analog-controlled paths are added for impedance

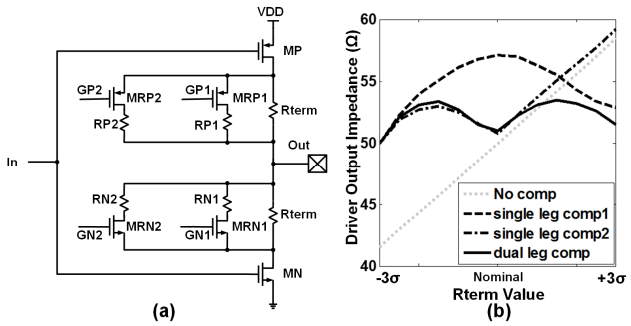

Fig. 3. (a) SST driver segment. (b) Simulated termination compensation vs corners.

tuning via the GP/N gate voltages. While conceivably only one additional analog-controlled path is necessary, if a low-impedance path is added to yield near 50• under a +3 case, this results in a low-overdrive under a nominal impedance corner and a large deviation (single leg comp1). Conversely, if a high-impedance path is added to yield near 50• under a nominal case, this results in insufficient voltage range to maintain proper impedance under a +3 case (single leg comp2). Thus, both analog-controlled low-impedance path1 and high impedance path2 are added which are replica-biased by the FSM-controlled termination control circuitry shown in Fig. 4.

For corners with low output resistance, the termination tuning circuitry operates with the lower-impedance path 1 in the feedback loops to set analog voltages GP1/GN1 to yield a 50• match, while the higher-impedance path is

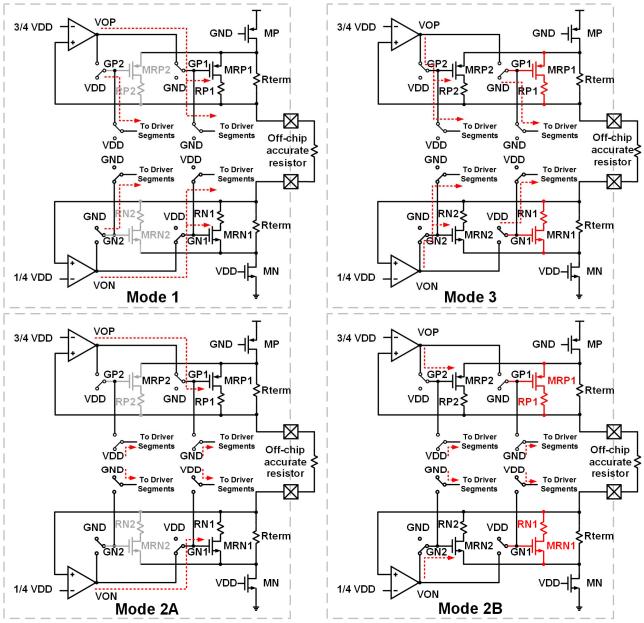

Fig. 4. Termination control circuitry in different operating modes.

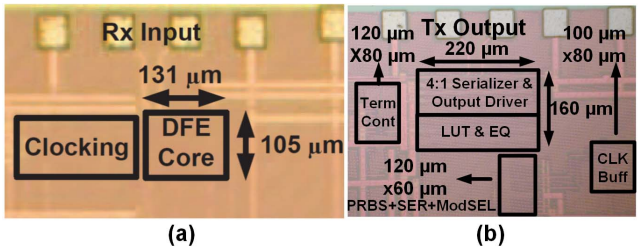

Fig. 5. (a) RX chip micrograph, (b) TX chip micrograph.

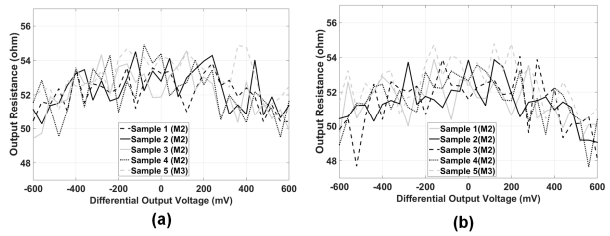

Fig. 6. Measured impedance vs output voltage level for (a) positive output pin and (b) negative output pin.

disabled (mode 1). In the case of high output resistance, path 1 is fully on and the higher-impedance path 2 is in the feedback loops to set analog voltages GP2/GN2 to yield a 50Ω match (mode 3). For corners with close-to-nominal output resistance, path 1 is simply set fully on and path 2 is disabled (mode 2A/B). Monitoring of GN1 and GN2 controls the transitions between different modes, with a transition from mode 1 to 2 if GN1 is close to VDD and a transition from mode 3 to 2 if GN2 is close to GND. Overlap is designed between modes 1/2 and 2/3, with an additional state in mode 2, to prevent dither in the main transmitter control.

IV. Experimental Results

Fig. 5 shows the chip micrographs of the dual-mode transceiver, which was fabricated in a GP 65nm CMOS process. The total area of the TX and RX is 0.06mm^2 and 0.014mm^2, respectively.

Fig. 6 shows measurement results for the output impedance control circuitry for 5 different TX chips. The impedance control loop ensures that the output stage maintains near a 50Ω output impedance over the entire 1.2Vpp range for both nominal samples (1-4) which operate in mode 2 and the high-impedance variation sample 5 which operates in the analog-controlled mode 3. Link BER measurements were performed using the three channels whose frequency responses are shown in Fig. 7. Fig. 8(a, b) shows that by optimizing the 4-tap TX equalizer in NRZ mode, a previously closed 16Gb/s eye is opened at the end of the highest-loss channel 3. Utilizing the 2-tap TX equalizer in PAM4 mode allows for significant

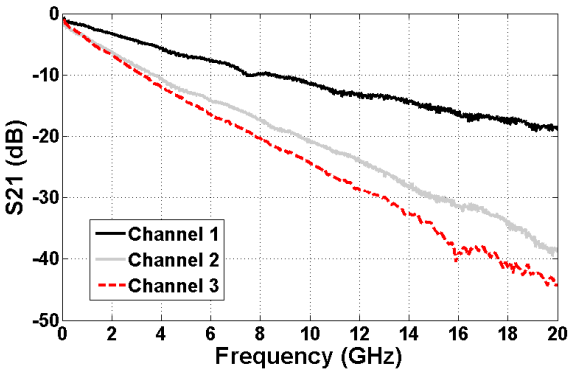

Fig. 7. Measured channel responses.

improvement in the channel output eyes at 25Gb/s over the moderate-loss channel 2 (Fig. 8(c,d)) and at 32Gb/s over the low-loss channel 1 (Fig. 8(e,f)). As depicted in the BER bathtub curves of Fig. 9, a timing margin near 0.16UI is achieved at a BER=10^{-12} with joint optimization of TX and RX equalization for 16Gb/s NRZ operation over channel 3. Higher data rates are possible when operating in PAM4 mode, with 25Gb/s achieved with 0.08UI timing margin over channel 2 and 32Gb/s achieved with 0.1UI timing margin over channel 1.

Table I summarizes the multi-mode transceiver performance and compares this work against other dedicated PAM4 and NRZ designs. Relative to the PAM4

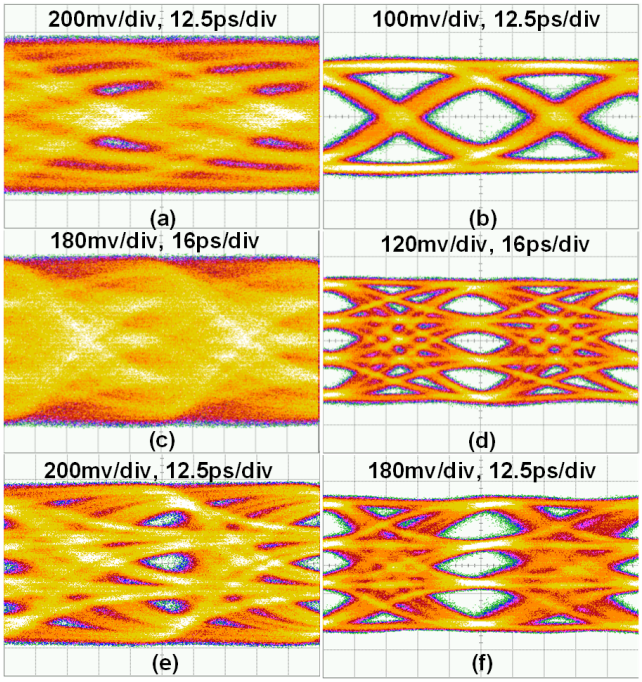

Fig. 8. 16Gb/s NRZ over Ch. 3 (a) eye-diagram w/o TX EQ and (b) w/ TX EQ, 25Gb/s PAM4 over Ch. 2 (c) eye-diagram w/o TX EQ and (d) w/ TX EQ, 32Gb/s PAM4 over Ch. 1 e) eye-diagram w/o TX EQ and (f) w/ TX EQ.

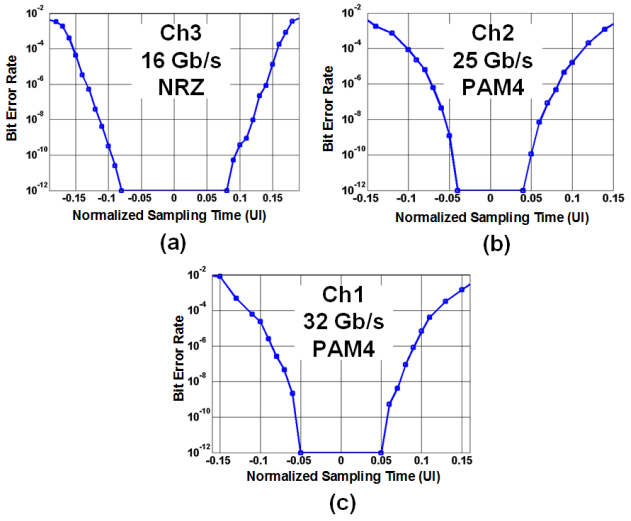

Fig. 9. Measured bathtub curves: (a) 16Gb/s NRZ over Ch. 3, (b) 25Gb/s PAM4 over Ch. 2, and (c) 32Gb/s PAM4 over Ch. 1.

designs of [1] and [2], the presented transceiver's additional equalization functionality allow for compensation of higher channel loss. Superior power efficiency and maximum data rate is also achieved in 32Gb/s PAM4 operation relative to the 28nm design operating at 28Gb/s NRZ [3] and superior power efficiency in NRZ operation relative to the 16Gb/s 40nm design [7].

TABLE I: PERFORMANCE SUMMARY

References	This Work			[1]	[2]	[3]	[7]
Data Rate (Gb/s)	32	25	16	20	56	28	16
Equalization	2-tap FFE + 3-tap DFE	2-tap FFE + 3-tap DFE	4-tap FFE + 3-tap DFE	3-tap FFE	3-tap FFE + 1-tap DFE	CTLE + 5-tap FFE + 14-tap DFE	CTLE + 3-tap FFE + 14-tap DFE
Modulation	PAM4	PAM4	NRZ	PAM4	PAM4	NRZ	NRZ
Total Loss @ Nyquist (dB)	9.6	14.2	20.5	5	2	40 for 25.78Gb/s	34
Eye Width (UI) BER	10% 10^{-12}	8% 10^{-12}	16% 10^{-12}	- 10^{-12}	- 10^{-12}	23% 10^{-12}	- 10^{-15}
Supply (V)	1.2 TX, 1 RX			1.8	1.2	1, 1.25 TX drv.	1/1.5 TX, 0.9 RX
Power (mW) (mW/Gbps)	176.3 5.5	151.1 6	173.7 10.8	408 20.4	475 8.5	295* 10.5	235* 14.7
Area (mm^2)	0.074			0.43	2.74	0.62	2.15
Technology	65-nm			90-nm	65-nm TX, 40-nm RX	28-nm	40-nm

*Clock generation and CDR power included

VII. CONCLUSION

This paper presented a 16/32 Gb/s SerDes which can seamlessly support both NRZ and PAM4 operation modes. High-resolution equalization and level generation in the high-swing voltage-mode source-synchronous-terminated (SST) transmitter is achieved with a 31-segment output DAC controlled by a lookup-table to enable a 4-tap and 2-tap FFE in NRZ and PAM4 modes, respectively. Power efficiency is improved in the transmitter with an optimized quarter-rate serializer and a new low-overhead analog impedance control scheme is employed in the output stage to obviate additional impedance control segments. At the receive side, efficient decision-feedback equalization is achieved with 1-FIR tap for the large first post-cursor ISI and 2-IIR taps for long-tail ISI cancellation. The equalization and modulation flexibility provided by the proposed architecture, achieved with minimal hardware overhead, makes it an excellent single design solution for systems required to support multiple channel conditions and variable data rates.

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