A 0.8–1.2 V 10–50 MS/s 13-bit Subranging Pipelined-SAR ADC Using a Temperature-Insensitive Time-Based Amplifier

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***Abstract*— This paper presents an energy-efficient 13-bit 10–50 MS/s subranging pipelined-successive approximation register (SAR) analog-to-digital converter (ADC) with power supply scaling. In the presented ADC, an SAR-assisted subranging floating capacitive DAC switching algorithm reduces switching energy along with enhanced linearity and speed in the first-stage SAR ADC. A following temperature-insensitive time-based residue amplifier realizes open-loop residual amplification without background calibration, while maintaining the benefits of dynamic operation and noise filtering. Furthermore, asynchronous SAR control logic employs a pre-window technique to accelerate SAR logic operations. The prototype ADC was fabricated in a 130-nm CMOS process with an active area of 0.22 mm^2. With a 1.2-V power supply and a Nyquist frequency input, the ADC consumes 1.32 mW at 50 MS/s and achieves signal-to-noise and distortion ratio and spurious-free dynamic range of 69.1 and 80.7 dB, respectively. The operating speed is scalable from 10 to 50 MS/s with a scalable power supply range of 0.8–1.2 V. Walden FoMs of 4–11.3 fJ/conversion-step are achieved.**

***Index Terms*— Analog-to-digital converter (ADC), dynamic amplifier, open-loop amplifier, pipelined-successive approximation register (SAR), residue amplifier, SAR, subranging, switched capacitor (SC), switching scheme, temperature insensitive.**

I. Introduction

FOR low-to-moderate resolution data conversion, a successive approximation register (SAR) analog-to-digital converter (ADC) [1]–[3] benefits from dynamic operation and no need for high-gain amplifiers as the feature size of CMOS technology scales down, thereby resulting in the best energy efficiency. However, the energy efficiency of an SAR ADC is degraded in high-resolution and high-speed [4]–[7] design because of a strict noise requirement for comparator design and an inherent serial conversion process. To overcome the problem, a pipeline technique [8], [9] can play a continuing role for high-speed and high-resolution conversion.

For high-speed and high-resolution applications, a pipelined-SAR ADC [10]–[18] is a promising architecture which combines two moderate-resolution SAR ADCs with an inter-stage residue amplifier. Compared with a conventional pipeline ADC, this architecture allows a higher first-stage resolution to improve linearity while it avoids a front-end sample-and-hold amplifier. This is because signal sampling, SAR operations, and residue holding are made on the same capacitive DAC (CDAC) array. Compared with a conventional high-resolution SAR ADC, a stage redundancy of the pipelined-SAR ADC significantly relaxes a comparator noise requirement and the pipelined operation breaks the speed bottleneck of a conventional SAR ADC. Furthermore, noise and linearity requirements of the second stage can be mitigated dramatically as well because of inter-stage gain.

While the pipelined-SAR architecture features the aforementioned benefits, it encounters a few design challenges. First, it still requires a high-gain high-speed amplifier to enable precise large inter-stage gain after a large number of bits are resolved in the first stage. A conventional telescopic operational transconductance amplifier (OTA)-based switched-capacitor (SC) residue amplifier [10]–[12] is power hungry and technology scaling-unfriendly with limited output swing and long settling time. As an alternative, a ring-amplifier-based SC residue amplifier [15] has the advantage of energy-efficient slew-based charging as well as a nearly rail-to-rail output swing. However, it has an inherent stability issue due to its ring operation and requires high threshold voltage devices additionally to accomplish high gain. A dynamic amplifier [16]–[20] is also attractive to a pipelined-SAR ADC because it operates as a time-domain integrator with the benefit of noise filtering [16] and an inherent dynamic feature. However, its open-loop nature makes it sensitive to process, supply voltage, and temperature (PVT). Therefore, background calibration [16], [18] is essential to achieve accurate inter-stage gain. Second, the linearity requirement of the first-stage CDAC must satisfy that of the whole ADC regardless of the resolution of the first-stage SAR ADC because DAC errors are reflected into residual voltage and cannot be corrected by digital error correction. Digital calibration [13], [16] can be used to

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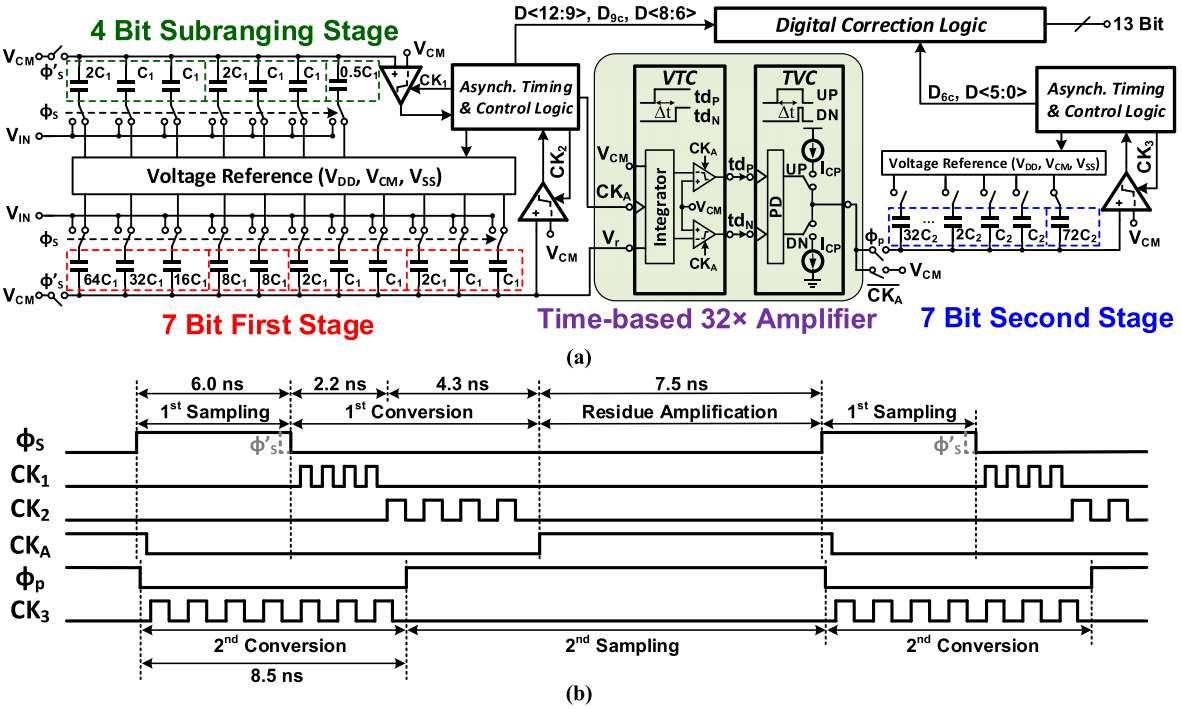

Fig. 1. (a) Block diagram and (b) timing diagram of the subranging pipelined-SAR ADC at 50 MS/s. (Actual implementation is fully differential.)

eliminate a mismatch error but increases design complexity. In this regard, high linearity switching algorithms [15], [21] are attractive because they usually accomplish both low switching energy and high linearity simultaneously.

In this work, we explore a 13-bit subranging pipelined-SAR ADC with a temperature-insensitive time-based residue amplifier. First, this work improves the accuracy and energy efficiency of the CDAC in the first-stage SAR ADC through the SAR-assisted subranging floating capacitor switching algorithm. Second, a 32× technology scaling-friendly time-based residue amplifier is presented to overcome the issues of PVT variation and small inter-stage gain in conventional dynamic amplifier through time information. Third, this paper also presents a pre-window technique adopted by the asynchronous SAR control logic to accelerate SAR logic operation. With the techniques presented above, the prototype ADC achieves Walden FoMs of 4–11.3 fJ/conversion-step with a Nyquist frequency input at 10–50 MS/s in a scalable power supply voltage range of 0.8–1.2 V.

This paper is organized as follows. Section II presents the architecture of the prototype ADC. Section III shows how the SAR-assisted subranging floating capacitor switching improves both linearity and switching energy. Section IV illustrates the principle and implementation of the temperature-insensitive time-based residue amplifier. Section V discusses the pre-window-based asynchronous SAR logic. Section VI presents the measurement results. Finally, conclusions are drawn in Section VII.

II. ADC Architecture

The overall ADC architecture is described in Fig. 1(a). Each 7-bit first-stage and second-stage SAR ADC is connected by a 32× time-based residue amplifier with one inter-stage redundancy bit. In the 7-bit first-stage SAR ADC, the first four most significant bits (MSBs) are resolved by a subranging stage [1], which is a 4-bit SAR ADC. One redundancy bit is inserted between the subranging stage and the first stage to cover the mismatch between them. The subranging architecture in [1] sets the capacitors in the first stage after the subranging stage completely finishes bit decisions, which slows down the comparison cycling loop of the total SAR ADC. However, the subranging floating capacitor architecture in this paper (detailed in Section III-C) sets the partial floating capacitors in the first-stage SAR ADC immediately after the corresponding decision bit from the subranging stage is acquired. Moreover, compared with the big and small DAC architectures [14]–[16], the subranging operation in our work has lower comparator energy consumption because the first four bits are acquired by a low-resolution comparator while maintaining the benefits of high energy efficiency, high linearity, and a fast SAR bit cycling loop. Bottom plate input sampling is adopted in the subranging stage and the first stage to avoid the gain error caused by parasitic capacitance on the top plate of CDAC and comparator input, and at the same time, it enhances the accuracy of sampling process.

The 32× time-based residue amplifier shown in Fig. 1(a) consists of a dynamic integrator-based voltage-to-time converter (VTC) and a charge pump-based time-to-voltage converter (TVC). The residue voltage stored in the first-stage CDAC is converted to time difference Δt by a dynamic integrator [19] and a zero-crossing detector (ZCD). The time difference is restored to voltage information by a phase detector (PD) and a charge pump [23]. The gain sensitivity to temperature and supply voltage variations is compensated by a time-based two-step conversion, which will be discussed in

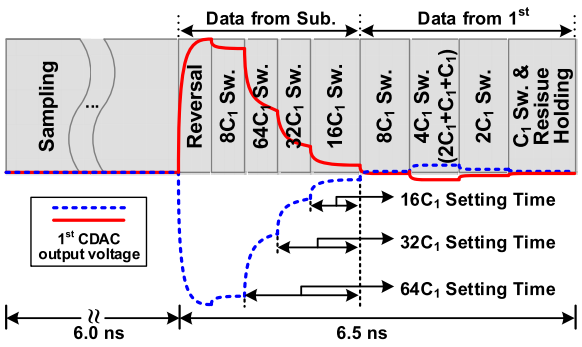

Fig. 2. First-stage CDAC output voltage during sampling, subranging, and first-stage conversion at 50 MS/s.

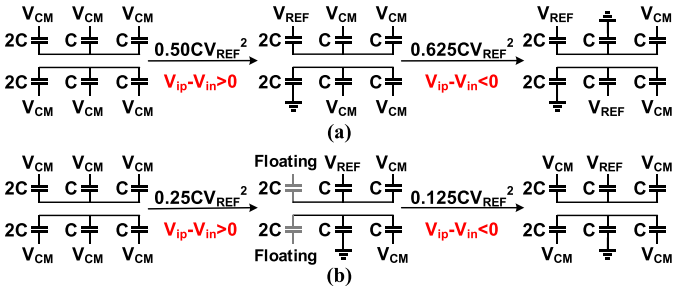

Fig. 3. (a) V_{CM}-based switching and (b) partial floating capacitor switching energy consumption for a 3-bit CDAC ($V_{REF} = 2\ V_{CM}$). (V_{ip} and V_{in} are the output voltages of CDAC.)

Section IV. The output current of the charge pump is integrated on the top plate of the 7-bit second-stage SAR ADC's CDAC to minimize parasitic capacitor charging. Half-full scale range design [13] is adopted in the second-stage SAR ADC to relax the gain of the residue amplifier from 64× to 32× for linearity considerations.

Fig. 1(b) shows the timing diagram of the overall ADC. The ADC requires a 30% duty cycle external clock ϕ_S for sampling, and all the other comparison clocks and control signals are asynchronously generated on chip. For example, when the pipelined-SAR ADC works at 50 MS/s with a 1.2-V power supply, the first-stage SAR ADC spends 6 ns for input sampling and 6.5 ns for the subranging-stage operation (2.2 ns) and first-stage CDAC setup. The remaining 7.5 ns is used for residual amplification and the system margin. The second-stage SAR ADC spends 8.5 ns for data conversion. Fig. 2 shows the differential output voltage of CDAC in the first stage. The settling time of the first three capacitors in the first stage is significantly relaxed because of the subranging operation. The detailed switching procedure is addressed in Section III-C.

III. SAR-Assisted Subranging Floating Capacitor Switching Technique in the First Stage

An energy-efficient and highly linear CDAC is essential in high-resolution and low-power pipelined-SAR ADC design. This section explains how the subranging floating capacitor switching technique improves linearity and reduces switching energy in the first-stage SAR ADC.

A. Review of Energy Saving of the Partial Floating Capacitor Switching Technique

The partial floating capacitor switching technique in [24] reduces switching energy consumption by interchanging the switching order of the largest capacitor with the second largest one. Fig. 3 shows an example of 3-bit CDAC switching energy consumptions of the V_{CM}-based switching technique [25], [26] and the partial floating capacitor switching technique. To illustrate an energy saving at each decision step, the decision steps of the first two bits "10" are considered here. In comparison with the V_{CM}-based switching technique, the partial floating capacitor switching technique can save switching energy through two approaches. First, the largest capacitor is made floating when the second bit is determined. This avoids additional charging to the largest capacitor and leads to a 50% energy savings in comparison with the V_{CM}-based switching technique (from 0.50 to 0.25 CV_{REF}^2 in Fig. 3). Second, when the first bit decision is different from the second bit decision, the floating capacitors are reconnected to V_{CM}, and this results in an 80% reduction of switching energy in comparison with the V_{CM}-based switching (from 0.625 to 0.125 CV_{REF}^2 in Fig. 3).

B. Linearity Analysis of the Partial Floating Capacitor Switching Technique

In this section, we address the integral nonlinearity (INL) characteristic of the partial floating technique and the effect of parasitic capacitors on the linearity of the CDAC. The partial floating technique reduces INL error (not mentioned in [24]) because V_{CM} is utilized as a reconstruction reference to the MSB capacitor between 1/4 and 3/4 V_{FS}. As explained in [25] and [26], the worst case INL for an N-bit V_{CM}-based switching CDAC is expected to occur at the mid-scale code, and its value is

$$\sigma[\mathrm{INL_{max}}]_{V_{CM-based}} = \sqrt{2^{N-2}}\frac{\sigma_0}{C_0}\mathrm{LSB} \tag{1}$$

where σ_0 is the standard deviation of the unit capacitor C_0. For the partial floating capacitor array, the worst case INL occurs at 1/4 and 3/4 V_{FS}, which is

$$\sigma[\mathrm{INL_{max}}]_{\mathrm{Partial-floating}} = \frac{\sqrt{3}}{2}\sqrt{2^{N-2}}\frac{\sigma_0}{C_0}\mathrm{LSB}. \tag{2}$$

This value is the same as the INL error at 1/4 and 3/4 V_{FS} of the V_{CM}-based switching because they have the same switching sequence from 0 to 1/4 V_{FS} and from 3/4 to V_{FS}. So, the partial floating technique relaxes the matching requirement between the unit capacitors by a factor of $2/\sqrt{3}$ in comparison with the V_{CM}-based switching.

However, the top and bottom plates' parasitic capacitance deteriorates the performance of the partial floating-based SAR ADC. Depending on whether the largest capacitor is floating or not, the weight of parasitic capacitance to the CDAC varies, and this generates a non-binary scaled voltage step during bit cycling. Fig. 4 models how large the top and bottom plates' parasitic capacitance affects the signal-to-noise and distortion ratio (SNDR) of a 13-bit pipelined-SAR ADC with

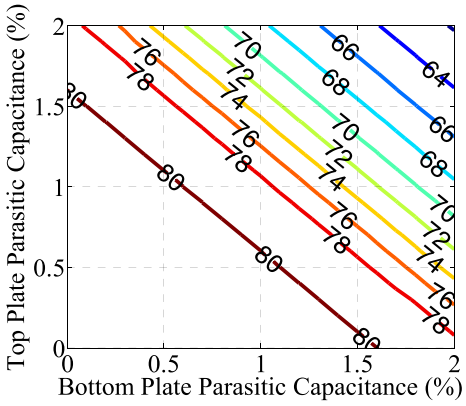

Fig. 4. SNDR degradation of a 13-bit pipelined-SAR ADC with a 7-bit partial floating-based first-stage SAR ADC, owing to capacitor array's top and bottom parasitic capacitance.

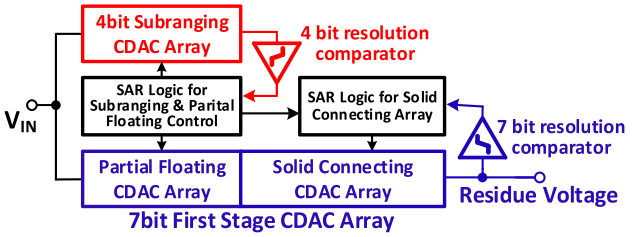

Fig. 5. SAR-assisted subranging floating operation in the 7-bit first-stage SAR ADC.

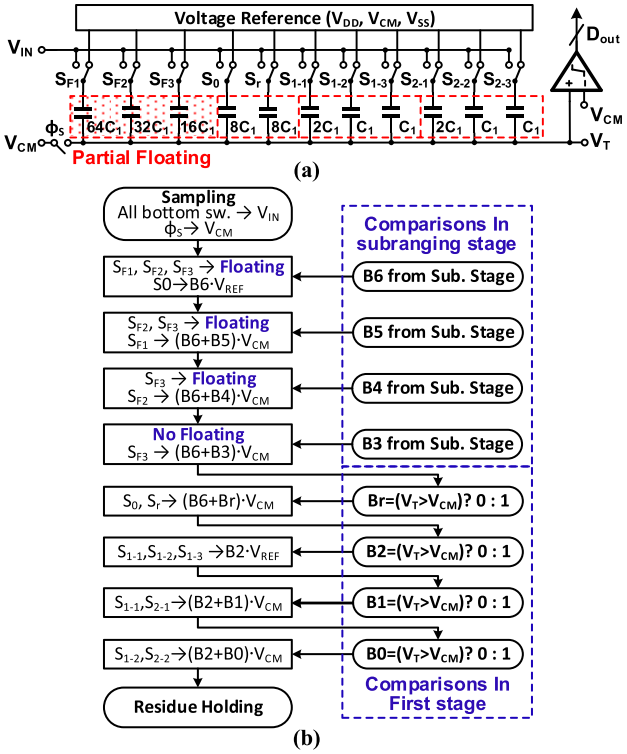

Fig. 6. (a) Capacitor array of the first-stage 7-bit SAR ADC with SAR-assisted subranging floating technique. (b) Its switching algorithm. (Actual implementation is fully differential.)

a 7-bit partial floating-based first-stage SAR ADC. Through MATLAB modeling, 2% top and bottom plates' parasitic capacitance decreases the effective number of bits (ENOB) of the 13-bit ADC to around 10 bit. Therefore, the partial floating capacitor switching technique is not suitable for high-resolution ADCs, and the SAR-assisted subranging floating capacitor switching technique is presented in our work to solve the aforementioned issues.

C. SAR-Assisted Subranging Floating Capacitor Switching Technique

From the energy saving approaches in Section III-A, more switching energy can be saved when more capacitors are used by the partial floating technique. However, this results in more decision errors because more non-binary scaled voltage steps appear. In Fig. 5, in order to skip the decision errors from the floating capacitors, a 4-bit subranging CDAC, which samples the input signal simultaneously with the first-stage CDAC, is employed to resolve the first four bits. With the help of these four bits, the first-stage CDAC array resolves the remaining four bits (one redundancy bit is included) and generates residue voltage to be transferred to a residue amplifier. Fig. 6(a) shows the capacitor array details of the first-stage 7-bit SAR ADC with the subranging floating technique. The first three largest capacitors ($64C_1$, $32C_1$, and $16C_1$) use the partial floating technique to save switching energy and reduce INL error. Fig. 6(b) shows the switching algorithm of the first-stage CDAC. After sampling, the first three capacitors are made floating, and are set by the data

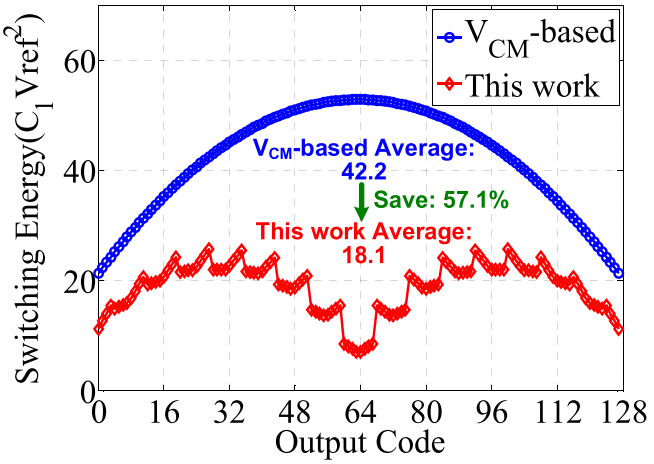

Fig. 7. Seven-bit first-stage switching energy comparison versus output code.

stream from the subranging stage one by one. After all the capacitors are solidly connected, the comparator in the first stage reaches the redundancy bit to set $8C_1$. Then, $4C_1$ is split into $2C_1$, C_1 and C_1 like a split capacitor array in [27] to further improve CDAC linearity. Splitting capacitors like this enable to employ the same control logic structure that the partial floating and redundancy capacitors employ.

Fig. 7 shows theoretical 7-bit CDAC switching energy of the SAR-assisted subranging floating capacitor switching. This switching energy includes energy consumption of both the first-stage CDAC and the subranging CDAC with the same unit capacitance. As compared with the V_{CM}-based switching,

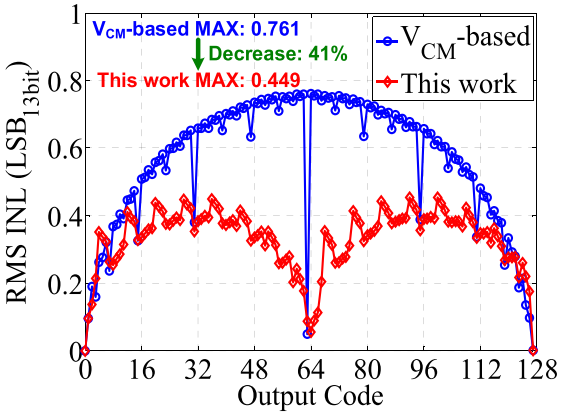

Fig. 8. Seven-bit first-stage linearity comparison due to CDAC mismatch.

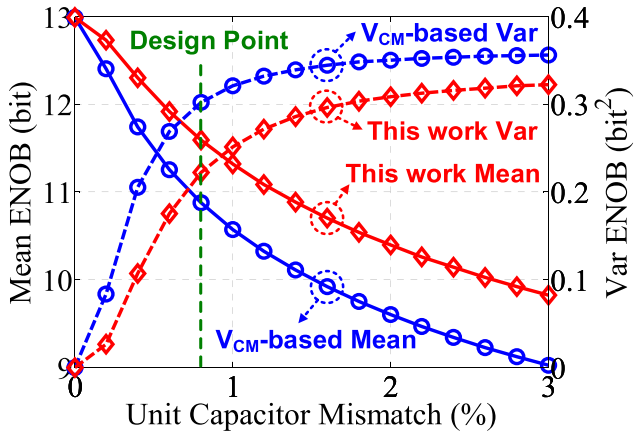

Fig. 9. ENOB improvement by SAR-assisted subranging floating capacitor switching technique.

the subranging floating technique consumes 57.1% less switching energy on average. Since the three largest capacitors are partially floating in the subranging floating technique, smaller INL error can be achieved when V_{CM} is used as the reconstruction reference voltage. Fig. 8 shows behavioral 5000 Monte Carlo rms INL simulation results under the assumption of 0.3% one sigma unit capacitor mismatch in the subranging and the first-stage CDAC. The simulation shows that the maximum rms INL of the subranging floating technique is 41% lower than that of the V_{CM}-based switching technique. In Fig. 9, 5000 Monte Carlo simulations in MATLAB show ENOB improvement as a result of the subranging floating technique. Here, the other blocks are assumed to be ideal. The horizontal axis denotes a standard deviation of the unit capacitor percent mismatch in the subranging stage and the first stage. For a 1% mismatch, the subranging floating capacitor switching technique improves the mean value of ENOB by 0.8 bit in comparison with the V_{CM}-based switching scheme.

IV. Temperature-Insensitive Time-Based Residue Amplifier

A. Review of Conventional Inter-Stage Residue Amplifiers

In a pipelined-SAR ADC with an M-bit first-stage, the inter-stage residue amplifier needs a gain of 2^{M-1} to finish the residual amplification while there is no extra input swing attenuation in the second-stage SAR ADC [10]. An OTA-based feedback amplifier [10]–[12] achieves an accurate inter-stage gain through the ratio of capacitance. However, it is not friendly to technology scaling due to low intrinsic gain. Moreover, with certain setting time, a smaller feedback factor β ($\approx 2^{1-M}$) for a higher inter-stage gain requires the OTA to have larger transconductance for the same settling error, which translates to increase in static power consumption [10]. On the other hand, an inter-stage gain less than 2^{M-1} increases the total sampling capacitance of the second-stage SAR ADC due to the extra capacitors for the input swing attenuation, and in turn increases the load capacitance of the OTA [12].

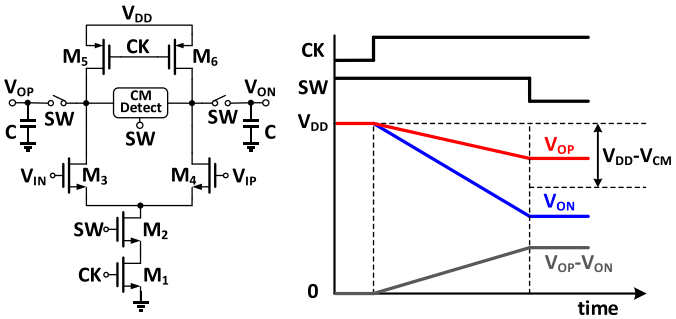

Fig. 10. (a) Circuit diagram and (b) timing diagram of a conventional dynamic amplifier.

A conventional dynamic amplifier is attractive to a pipelined-SAR ADC because of its zero static power and noise filtering features [16]–[20]. Fig. 10 shows the circuit and timing diagrams of a single-stage dynamic amplifier [19]. The voltage amplification is done by the clock-controlled charging and discharging operations to the load capacitors. The dynamic amplifier exhibits a transfer function of an integrator, and provides the best separation of a sampled-data input signal and thermal noise [16]. The gain of the single-stage dynamic amplifier is given by [19]

$$\text{Gain}_{\text{Dynamic-Amplifier}} = \frac{g_m}{I_d} \cdot (V_{\text{DD}} - V_{\text{CM}}) \tag{3}$$

where g_m/I_d is the ratio of the transconductance and drain current of the input transistors (M_3 and M_4). From (3), the dynamic amplifier faces two critical challenges when it is used as a residue amplifier: one is that its gain is sensitive to PVT variations, and another is that the gain is limited to a small value inherently due to the limitations of supply voltage and g_m/I_d [16]. A temperature-insensitive time-based residue amplifier is introduced in the following to solve the above challenges, while maintaining the merits of the conventional dynamic amplifier.

B. Operating Principle of the Time-Based Residue Amplifier

The presented residue amplifier finishes its residue transfer through time-domain information as shown in Fig. 11. The residue voltage stored in the first-stage SAR ADC is converted to time difference by a VTC which consists of a dynamic integrator for noise filtering [16] and a ZCD for time-delay generation. The time difference is converted to the output

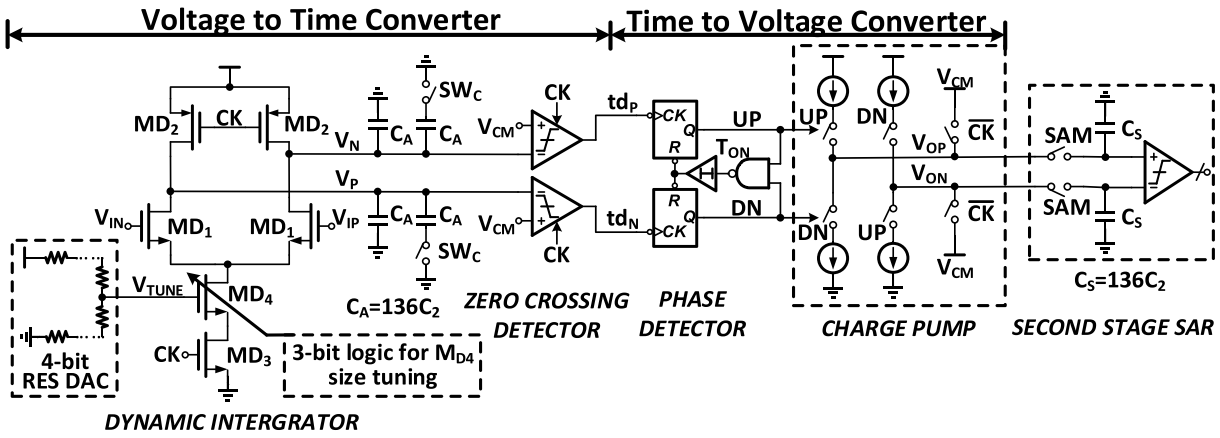

Fig. 11. Temperature-insensitive time-based residue amplifier.

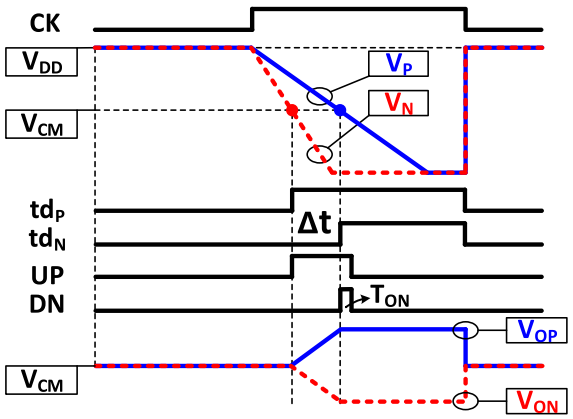

Fig. 12. Timing diagram of the time-based residue amplifier.

voltage of the residue amplifier by a TVC which consists of a PD and a charge pump [23]. The ZCD in Fig. 11 contains a dynamic pre-amplifier and a dynamic inverter for power efficient full dynamic operation. The load capacitors of the dynamic amplifier use capacitor arrays which have the same capacitance and structure as those of the sampling capacitor arrays in the second-stage SAR ADC. This eliminates the inter-stage gain's dependence on the capacitance (C_A and C_S). The 4-bit resistor DAC for V_{TUNE}, the 3-bit logic for MD_4 transistor size tuning, and the SW_C switches at the output of the dynamic integrator are used for initial settings for different power supply modes and process corner correction. Fig. 12 shows the timing diagram of the time-based residue amplifier. When CK is low, the output node voltage (V_N and V_P) of the dynamic integrator is reset to V_{DD} and the output node voltage (V_{ON} and V_{OP}) of the charge pump is reset to common-mode voltage V_{CM}. At the rising edge of CK, V_N and V_P start to be discharged at different rates based on the input residue voltage and the output of the ZCD (td_P and td_N), which becomes high after V_N and V_P cross V_{CM}, respectively. Control signals of the charge pump (UP and DN) are generated by the PD, and T_{ON} is used for dead zone elimination. According to UP and DN signals, the charge pump injects current into the CDAC in the second-stage SAR ADC, and it develops the output voltage of the residue amplifier. The residue amplification is done through the above discharging and charging operations, which is reminiscent of a dual-slope ADC [28]. The ZCD's offset voltage and the input transistor's (MD1) offset voltage in Fig. 11 can be translated to the equivalent input offset voltage of the residue amplifier. If the total input offset voltage of the residue amplifier is less than the inter-stage redundancy voltage range (8.82 mV), the performance of the ADC is not affected. The offset voltage of the ZCD in this work is attenuated by the dynamic integrator gain, whereas that of the ZCD in a ZCD-based ADC [29] is not. The effect of signal-dependent delay of the ZCD is also minimized because of a similar discharging slope across the small input range of the dynamic integrator in Fig. 11.

Fig. 13 shows the schematic of the charge pump in the residue amplifier [23]. Replica branches ($\overline{\mathrm{UP}}$ and $\overline{\mathrm{DN}}$ switches) are used for current stabilization when both UP and DN are low. A mismatch between PMOS and NMOS current will cause the output common-mode voltage of the charge pump to change. However, this is not critical because the V_{CM}-based switching is adopted in the second-stage SAR ADC. Furthermore, the mismatch between UP current sources (two transistors of MC4 in Fig. 13) leads to different voltage gains when the input voltage polarity of the residue amplifier is different. According to the simulations, the ENOB of the ADC is higher than 11.5 bit with a mismatch of 30% between the UP current sources, which is easy to satisfy.

The gain of the time-based residue amplifier is determined by the gain of VTC and TVC, which are controlled by V_{TUNE} in Fig. 11 and the resistor R in Fig. 13, respectively. The gain of the time-based residue amplifier is given by

$$\mathrm{Gain}_{\mathrm{Time-based-Amplifier}} = 2 \cdot I_{\mathrm{CP}} \cdot \frac{g_{m,\mathrm{MD1}}}{I_{\mathrm{MD1}}^2} \cdot (V_{\mathrm{DD}} - V_{\mathrm{CM}}) \tag{4}$$

where $g_{m,\mathrm{MD1}}$ and I_{MD1} are the transconductance and drain current of MD1 in Fig. 11, respectively, and I_{CP} is the drain current of MC1 in Fig. 13. Compared with (3) and (4), the time-based residue amplifier is easy to achieve 32× gain. Furthermore, the total transfer time of the time-based residue amplifier has a relation with the sampling capacitance C_S in the second stage. Hence, the time-based residue amplifier

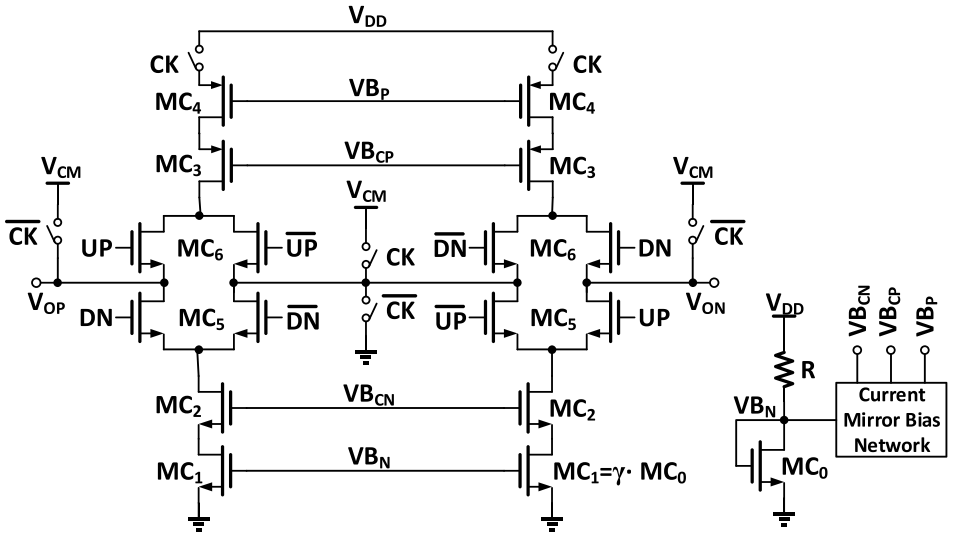

Fig. 13. Schematic of the charge pump in the residue amplifier.

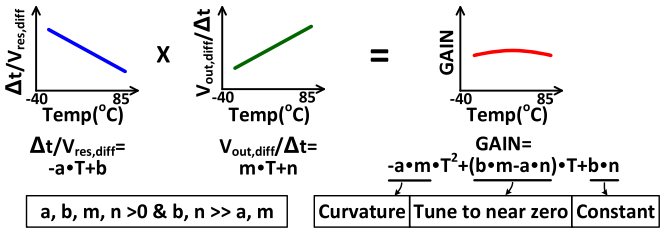

Fig. 14. Temperature compensation concept.

is technology scaling-friendly in terms of speed because the metal-oxide-metal (MOM) capacitor C_S is also technology scaling-friendly.

C. Temperature Compensation in the Time-Based Residue Amplifier

The temperature compensation is done by a VTC with a negative temperature coefficient (TC) and a TVC with a positive TC. For simplicity, we model the negative TC and positive TC with a linear equation in Fig. 14. The detailed derivation procedure of the TC of the VTC and TVC is given in the Appendix. Through equations (6), (10), (11), and (13) in the Appendix, all the coefficients in Fig. 14 can be obtained. From (10), the negative TC of VTC increases as V_{TUNE} increases (because $V_{\mathrm{OV,MD1}}$ increases) in Fig. 11. From (13), the positive TC of TVC decreases as R increases in Fig. 13. Therefore, the temperature compensation can be done by tuning V_{TUNE} in Fig. 11 and R in Fig. 13. Fig. 15 shows the simulation results of the conversion factors of the VTC and the TVC at a 1.2-V power supply and the typical-typical (TT) corner. When the temperature varies from −40 °C to 85 °C, the gain of the residue amplifier changes only 0.6% from 33.1× to 33.3× (bigger than 32× to compensate the top plate's parasitic capacitance in the first-stage CDAC).

From (14) and (15) in the Appendix, the time-based residue amplifier can also tolerate some degree of supply voltage variation in the same principle shown in Fig. 14 through a negative voltage coefficient (VC) in (14) and a positive

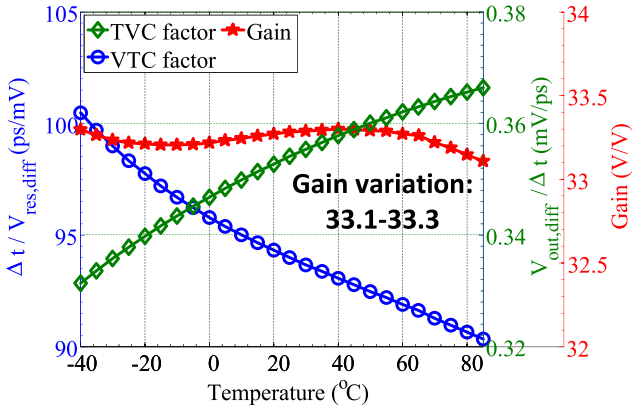

Fig. 15. Simulation result of the temperature compensation process.

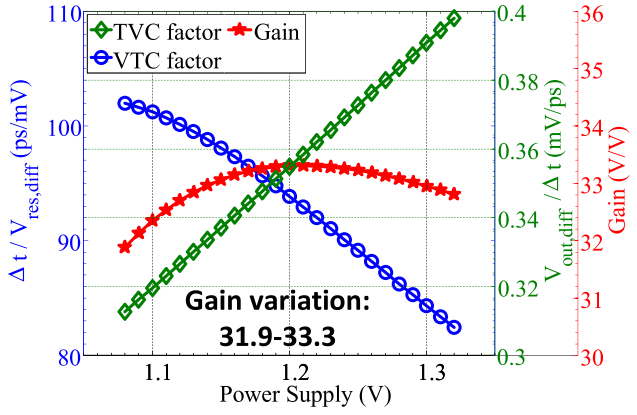

Fig. 16. Simulation result of the residue amplifier gain versus power supply voltage variation.

VC in (15). Fig. 16 shows the simulation result of the residue amplifier gain versus power supply voltage variation (1.2 V is nominal supply voltage) at the TT corner. With ±10% power supply voltage variation, gain of the residue amplifier changes 4.2% from 31.9× to 33.3×.

Equations (10) and (13)–(15) in the Appendix show that TC and VC of the VTC have the same trends as those of

TABLE I
RESIDUE AMPLIFIER GAIN VARIATIONS WITH PVT VARIATIONS (−40 °C TO 85 °C)

Corners	SS	SF	TT	FS	FF
1.32 V Supply	31.7-32.9	31.7-33.0	32.0-33.1	32.5-33.6	32.5-33.5
1.20 V Supply	33.1-33.3	33.1-33.3	33.1-33.3	33.1-33.3	33.1-33.3
1.08 V Supply	32.1-32.7	32.2-32.7	31.7-31.9	31.5-31.7	31.5-31.7

TABLE II
NOISE BREAKDOWN OF THE PIPELINED-SAR ADC

Total Noise [V^2]	Quantization Noise [V^2]	Sampling Noise [V^2]	Residue Amp. Noise [V^2]	2nd Comparator Noise [V^2]
1.11e-8	6.35e-9	2.60e-9	2.03e-9	0.12e-9

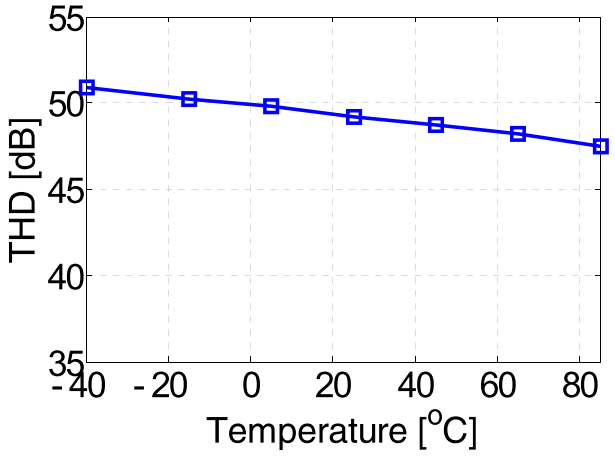

Fig. 17. Simulated THD of the residue amplifier versus temperature.

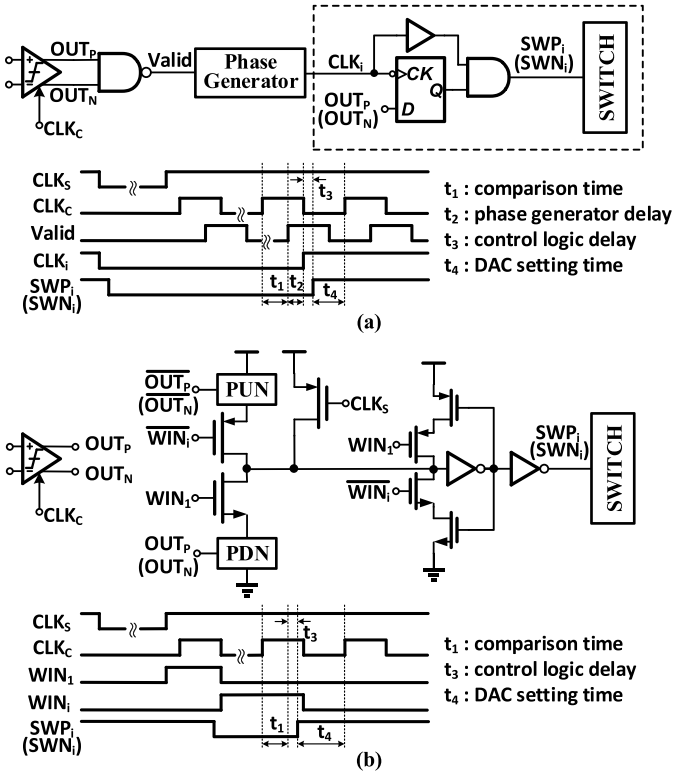

Fig. 18. (a) Conventional SAR logic. (b) Subranging stage's pre-window SAR logic.

the TVC, respectively. Moreover, they are governed by the same design variables, and can be tuned by V_{TUNE} and R. The design point of the residue amplifier in this paper is determined mainly by temperature compensation, while power supply sensitivity is reasonably minimized. Table I summarizes the simulation results of the gain variations of the residue amplifier at different process corners and different power supplies when the temperature varies from −40 °C to 85 °C. Different trimming block settings are used for different process corners to cover the process variations.

D. Noise and Linearity of the Time-Based Residue Amplifier

According to the noise analysis in the Appendix, the input-referred noise of the presented time-based residue amplifier in Fig. 11 is given by

$$\overline{v_{i,\mathrm{noise}}^2} = \frac{4kT\gamma}{C_A} \cdot \frac{I_{\mathrm{MD1}}}{g_{m,\mathrm{MD1}}(V_{\mathrm{DD}} - V_{\mathrm{CM}})}. \tag{5}$$

The noise in (5) is the same with the noise of a conventional dynamic amplifier [16], so the presented time-based residue amplifier is also a low-noise solution due to the noise filtering feature. Table II shows the simulated noise breakdown of the pipelined-SAR ADC. The time-based residue amplifier causes only 18% of the total noise power of the ADC.

Fig. 17 shows the simulated total harmonic distortion (THD) of the residue amplifier versus temperature under 1.2-V power supply and TT corner. The input signal of the residue amplifier is an 11-MHz stair-case sinusoidal signal with a voltage swing of 17.65 $\mathrm{mV_{pp,diff}}$ (maximum residue voltage swing), and it is generated by an ideal DAC clocked at 50 MHz. From Fig. 17, the linearity of the time-based residue amplifier is sufficient to resolve the seven bits in the second stage.

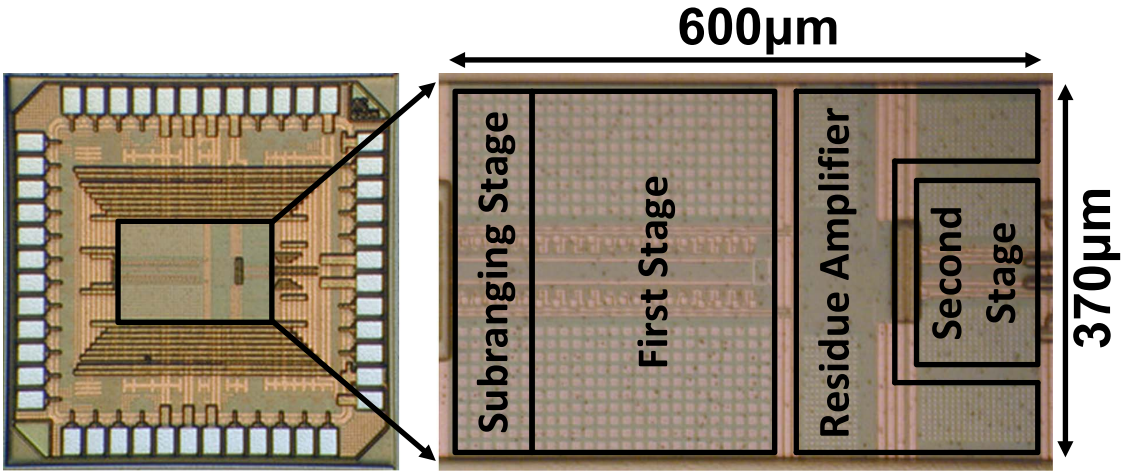

Fig. 19. Die microphotograph of pipelined-SAR ADC.

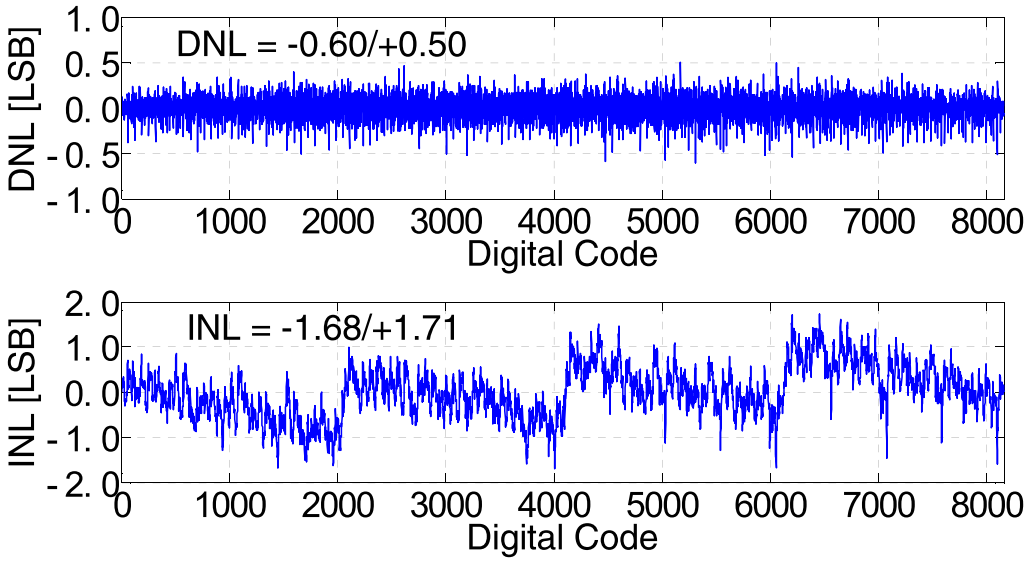

Fig. 20. Measured DNL and INL errors.

V. Pre-Window Asynchronous Control Logic

In high-resolution SAR ADC design, a large CDAC for a strict matching requirement makes a DAC settling time longer. Moreover, the comparison results always suffer further delays in order to set the control logic for a CDAC as shown in Fig. 18(a) [30]. Therefore, a DAC settling time requirement is getting harder to achieve in high-speed high-resolution SAR ADC design. Fig. 18 shows the comparison between conventional SAR logic [30] and the presented pre-window-based SAR logic. Fig. 18(b) shows an example of the pre-window technique used in the subranging stage. In a similar way, it can apply to the first stage and the second stage as well. In the pre-window-based SAR logic, a window (WIN_i) is enabled for the comparator output before it is clocked. With assistance from WIN_i, comparison results are used by the corresponding switched control blocks without extra delay. In Fig. 18, the pre-window-based SAR logic saves the delay time of the phase generator t_2, which is usually considerable in high-resolution SAR ADC because the delay cells are always inserted into the asynchronous loop in order to relax the CDAC set up time. The pre-window signal, WIN_i is generated through a true single phase clocked D-type flip flop-based shift register chain.

VI. Measurement Results

The prototype pipelined-SAR ADC was fabricated in an 1P8M 130-nm CMOS process. A die photograph is shown in Fig. 19. The active area of the ADC is 0.22 mm^2, and most of the active area is occupied by the CDAC in both the first stage and second stage. The unit capacitance of the first-stage SAR ADC is 22 fF. Moreover, both the CDAC of the second-stage SAR ADC and the load capacitor of the dynamic integrator in the residue amplifier use the same unit capacitance 1.8 fF. All of the unit capacitor is a custom-designed encapsulated MOM capacitor [30]. The designed pipelined-SAR ADC has three operation modes supporting different power supply voltages (1.2, 1, and 0.8 V) with different maximum conversion speeds (50, 30, and 10 MS/s, respectively). As there is no integrated reference buffer, V_{DD} and GND are used as the high and low reference voltages, respectively, to simplify the measurement. Large on-chip bypass capacitors are used to stabilize the reference

TABLE III
PIPELINED-ADC PERFORMANCE SUMMARY

Resolution	13 bits		
Technology	130 nm 1P8M CMOS		
Active Area	0.22 mm^2		
DNL	− 0.60/+0.50 LSB		
INL	− 1.68/+1.71 LSB		
Power Supply	1.2 V	1.0 V	0.8 V
Sampling Rate	50 MS/s	30 MS/s	10 MS/s
Input Range	2.26 $V_{p\text{-}p,diff}$	1.88 $V_{p\text{-}p,diff}$	1.51 $V_{p\text{-}p,diff}$
SNDR @ 2.05 MHz input	71.6 dB	71.4 dB	71.5 dB
SFDR @ 2.05 MHz input	84.6 dB	81.9 dB	82.0 dB
SNDR @ Nyquist input	69.1 dB	71.0 dB	71.2 dB
SFDR @ Nyquist input	80.7 dB	80.0 dB	81.5 dB
Total Power	1.32 mW	0.56 mW	0.12 mW
FoM @ 2.05 MHz input	8.5 fJ/conv. step	6.1 fJ/conv. step	3.9 fJ/conv. step
FoM @ Nyquist input	11.3 fJ/conv. step	6.4 fJ/conv. step	4.0 fJ/conv. step

voltages. Foreground calibration is used for the temperature compensation setting of the open-loop residue amplifier in different operation modes with a dc input signal of V_{CM}. The calibration flow is as follows: First, configuring the residue amplifier in Fig. 11 with the default settings which are from simulations; then changing the current of the charge pump by adjusting the resistor R in Fig. 13 to make the output code of the ADC 4096 (mid-scale code of a 13-bit ADC) under 25 °C. Second, putting the measured ADC under −40 °C and 85 °C, and capturing its output code simultaneously; if the output code is within a range of [4094–4098], the calibration is done; if not, changing V_{TUNE} in Fig. 11 and R in Fig. 13 according to the temperature compensation analysis in Section IV-C to make the output code of the ADC in the range of [4094–4098] under −40 °C and 85 °C.

Fig. 20 shows the measured differential nonlinearity (DNL) and INL errors under 50 MS/s conversion rate. The DNL is within −0.60/+0.50 LSB and the INL is within −1.68/+1.71 LSB with assistance from the highly linear SAR-assisted subranging floating capacitor switching scheme and a large CDAC array used in the first-stage SAR ADC. Fig. 21 shows the measured fast Fourier transform (FFT) spectrums at different modes with Nyquist frequency input signals. The ADC achieves 69.1-dB spurious-free dynamic range (SNDR) and 80.7-dB SFDR at 50 MS/s under 1.2-V power supply, 71-dB SNDR and 80-dB SFDR at 30 MS/s under 1-V power supply, and 71.2-dB SNDR and 81.5-dB SFDR at 10 MS/s under 0.8-V power supply. The designed pipelined-SAR ADC has a very low-noise floor thanks to the noise filtering benefit from the residue amplifier. Fig. 22 summarizes the measured SNDR and SFDR versus input frequencies at different operation modes. The performance drops in the high input frequencies

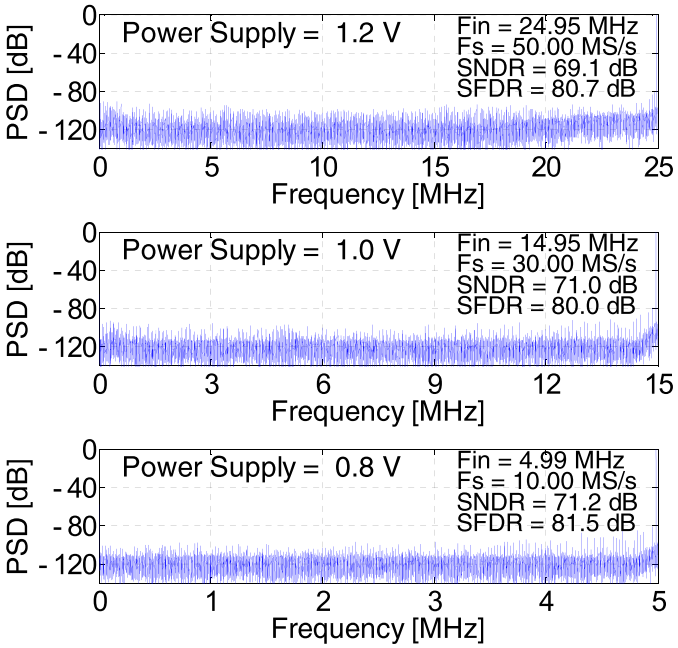

Fig. 21. Measured FFT from 66536 data output with Nyquist input signals at 1.2-, 1-, and 0.8-V power supplies.

due to sampling bandwidth limitation by the resistance in ADC test input paths, including the sampling switches, the ESD protection resistors, and the routing resistors.

The robustness of the presented pipelined-SAR ADC against temperature and power supply variation is also measured in Figs. 23 and 24. Since the sampling performance of ADC is strongly related with its ambient temperature and power supply voltage, the measurements in Figs. 23 and 24 were performed at low conversion rates to evaluate the residue

TABLE IV
COMPARISON WITH STATE-OF-THE-ART PIPELINED-SAR ADC DESIGNS

	This Work			[10] VLSI 2010	[11] ISSCC 2012	[16] ISSCC 2014	[18] VLSI 2014	[15] ISSCC 2015
Technology	130 nm			65 nm	130 nm	28 nm	28 nm	65 nm
Resolution [bits]	13			12	14	14	14	13
Active Area [mm^2]	0.22			0.16	0.24	0.137	0.35	0.054
Interleaving	No			No	No	2X	2X	No
DNL [LSB]	0.60			0.75	0.89	-	-	0.58
INL [LSB]	1.71			1.50	3.52	-	-	0.96
Residue Amplifier Structure	Open-loop Time-based			Closed-loop Telescopic		Open-loop Dynamic		Closed-loop Ring
Residue Amplifier PVT-Stabilized	Yes			Yes		Digital Calibration		Yes
Power Supply [V]	1.2	1.0	0.8	1.3	1.2	1.0	0.9	1.2
ADC FS [$V_{p\text{-}p,diff}$]	2.26	1.88	1.51	2.0	2.0	1.4	-	2.4
Sampling Rate [MS/s]	50	30	10	50	30	80	200	50
SNDR @ Nyq. [dB]	69.1	71.0	71.2	64.4	70.4	66.0	65.0	70.9
SFDR @ Nyq. [dB]	80.7	80.0	81.5	75.0	79.6	74.0	-	84.6
Total Power [mW]	1.32	0.56	0.12	3.5	2.54	1.5	2.3	1.0
FoM @ Nyq. [fJ/conv.step]	11.3	6.4	4.0	51.8	31.3	11.5	7.9	6.9

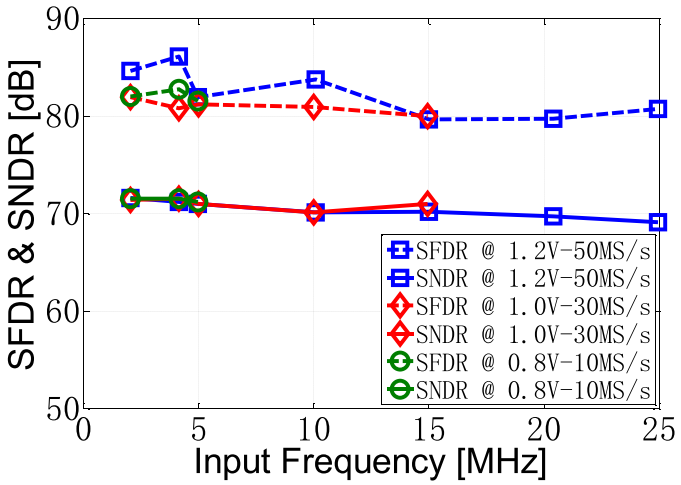

Fig. 22. Measured SFDR and SNDR versus input frequency at different power supply voltages and sampling rates.

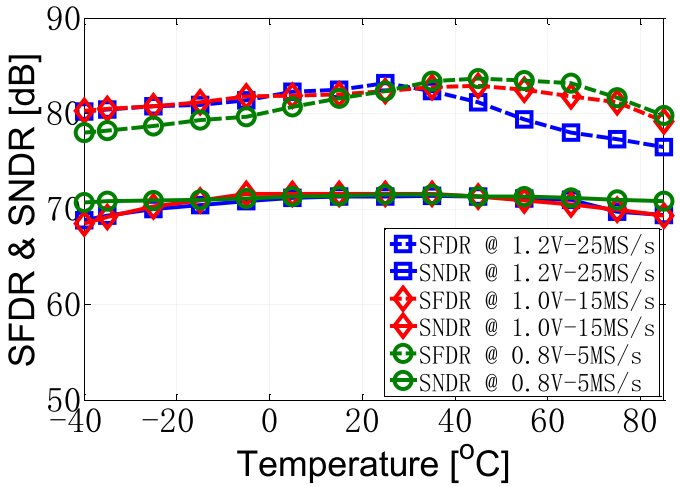

Fig. 23. Measured SFDR and SNDR versus temperature of ADC with 2.05-MHz input signals.

amplifier gain variation versus ambient temperature and power supply voltage by minimizing the performance deterioration from sampling. The ADC has a higher than 68.5-dB measured SNDR and a higher than 76.5-dB measured SFDR over a −40 °C to 85 °C temperature range at all operating modes in Fig. 23. If temperature ranges from −25 °C to 65 °C, SNDR is higher than 70.1 dB, and SFDR is higher than 78.2 dB at all operating modes. This verifies that the temperature compensation presented in Section IV is valid. More than 66-dB measured SNDR and more than 80.9-dB measured SFDR can be obtained within ±10% power supply variation of the whole pipelined-SAR ADC at all operating modes in Fig. 24. If measured within ±5% power supply variation, SNDR is higher than 68.9 dB, and SFDR is higher than 81.4 dB at all operating modes. Fig. 25 shows the power consumption breakdown of the presented pipelined-SAR ADC at 1.2-V power supply and 50-MS/s conversion rate with a Nyquist frequency input. The total measured power is

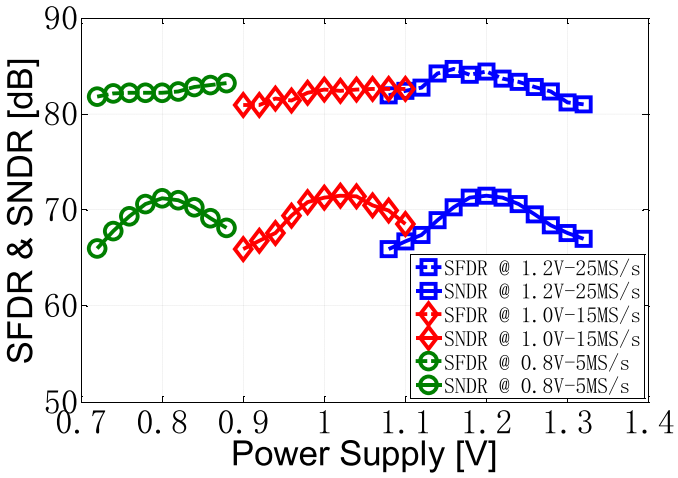

Fig. 24. Measured SFDR and SNDR versus ±10% power supply variation of ADC with 2.05-MHz input signals.

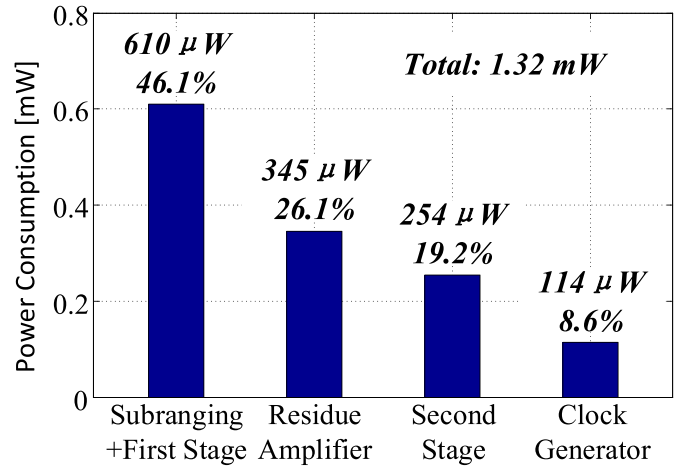

Fig. 25. Pipelined-SAR ADC power consumption breakdown (1.2-V power supply and 50 MS/s).

1.32 mW. Only 26.1% of the total power is consumed by the time-based residue amplifier, and this is much smaller than that of a closed-loop residue amplifier design [10]–[12]. The other power consumption percentages include 46.1% for the subranging and first stage, 19.2% for the second stage, and 8.6% for the clock generator.

Table III summarizes the performance of the pipelined-SAR ADC at different operating modes. The full-scale differential input signal range is 16/17 of $2 \times V_{\mathrm{DD}}$ due to the redundancy capacitor in the first stage. The performance of the pipelined-SAR ADC keeps similar at down-scaled power supply voltages, even leading to better FoMs at 0.8- and 1-V power supply. The Walden FoM with 2.05-MHz input signal is from 3.9 to 8.5 fJ/conversion-step, and 4 to 11.3 fJ/conversion-step with a Nyquist frequency input. Table IV shows a comparison between the prototype ADC and other pipelined-SAR ADCs. To our best knowledge, among the pipelined-SAR ADC with an open-loop residue amplifier, this work is the only one that achieves high gain and background calibration-free operation simultaneously under ambient temperature and power supply variation. This work also shows an attractive power supply scaling feature with competitive energy efficiency, even though it is implemented in a relatively old technology. With a 0.8-V power supply and a 10-MS/s conversion rate, the 4-fJ/conversion-step is the best reported FoM to date for an ADC with more than 70-dB measured SNDR and more than 10-MS/s conversion rate.

VII. Conclusion

This paper introduces a subranging pipelined-SAR ADC employing a new CDAC switching algorithm and a new residue amplifier. The presented SAR-assisted subranging floating capacitor switching algorithm reduces the CDAC switching energy and improves its linearity by utilizing a subranging stage which also breaks the speed bottleneck in the first-stage SAR ADC. The presented temperature-insensitive time-based residue amplifier solves the PVT variation issue in the open-loop residue amplifier. This time-based residue amplifier also shows power supply voltage scalability. The pre-window asynchronous control logic is used to extend the settling time of the CDAC array. With the aforementioned three techniques, the prototype ADC achieves 69.1-dB SNDR and 80.7-dB SFDR for a Nyquist frequency input sampled at 50 MS/s and consumes 1.32 mW. With a power supply range of 0.8–1.2 V and 10–50 MS/s conversion rate, this ADC achieves Walden FoMs from 4 to 11.3 fJ/conversion-step.

Appendix

A. Temperature Compensation Analysis of the Time-Based Residue Amplifier

The conversion factor of the VTC in Figs. 11 and 12 is given by

$$F_{\mathrm{VTC}} = \frac{\Delta t}{V_{\mathrm{res,diff}}} \cong \frac{g_{m,\mathrm{MD1}}}{I_{\mathrm{MD1}}^2} \cdot \left(V_{\mathrm{DD}} - V_{\mathrm{CM}}\right) \cdot C_A = \frac{2 \cdot \left(V_{\mathrm{DD}} - V_{\mathrm{CM}}\right) \cdot C_A}{K_{\mathrm{MD1}} \cdot V_{\mathrm{OV,MD1}}^3} \quad (6)$$

where $K_{\mathrm{MD1}} = 1/2 \times \mu_n \times C_{\mathrm{ox}} \times (W/L)_{\mathrm{MD1}}$. $V_{\mathrm{OV,MD1}}$ is the overdrive voltage of MD_1. C_A is the output capacitance of dynamic integrator. (Assume, the SW_C switch is OFF in Fig. 11.) The TC of (6) is given by

$$\frac{\partial F_{\mathrm{VTC}}}{\partial T} = -\frac{2 \cdot \left(V_{\mathrm{DD}} - V_{\mathrm{CM}}\right) \cdot C_A}{K_{\mathrm{MD1}} \cdot V_{\mathrm{OV,MD1}}^3} \cdot \left(\frac{1}{K_{\mathrm{MD1}}} \cdot \frac{\partial K_{\mathrm{MD1}}}{\partial T} + \frac{3}{V_{\mathrm{OV,MD1}}} \cdot \frac{\partial V_{\mathrm{OV,MD1}}}{\partial T}\right). \quad (7)$$

MD_1 is biased in the saturation region, and MD_4 is in the triode region in Fig. 11. The current passing MD_4 is given by

$$2 \cdot K_{\mathrm{MD1}} \cdot V_{\mathrm{OV,MD1}}^2 = K_{\mathrm{MD4}} \cdot \left(V_{\mathrm{OV,MD4}} - \frac{1}{2} \cdot V_{\mathrm{DS,MD4}}\right) \cdot V_{\mathrm{DS,MD4}} \quad (8)$$

where $K_{\mathrm{MD4}} = \mu_n \times C_{\mathrm{ox}} \times (W/L)_{\mathrm{MD4}}$. $V_{\mathrm{OV,MD4}}$ and $V_{\mathrm{DS,MD4}}$ are the overdrive voltage and drain-to-source voltage of MD_4, respectively. Taking a derivative to (8) with respect to temperature to get the TC of $V_{\mathrm{OV,MD1}}$, the result is

$$\frac{\partial V_{\mathrm{OV,MD1}}}{\partial T} = -\frac{\alpha \cdot V_{\mathrm{OV,MD4}}}{\alpha \cdot \left(V_{\mathrm{OV,MD4}} - V_{\mathrm{DS,MD4}}\right) + 4 \cdot V_{\mathrm{OV,MD1}}} \cdot \frac{\partial V_{\mathrm{TH,MD1}}}{\partial T} = \beta \cdot \frac{\partial V_{\mathrm{TH,MD1}}}{\partial T} \quad (9)$$

where α is K_{MD4}/K_{MD1}, which is temperature insensitive, and $V_{TH,MD1}$ is the threshold voltage of MD_1 with negative TC [31]. The resulting β is negative. When deriving (9), body effect of MD_1 is neglected. Therefore, the TC of the conversion factor of the VTC is given by

$$\frac{\partial F_{VTC}}{\partial T} = -\frac{2\cdot (V_{DD}-V_{CM})\cdot C_A}{K_{MD1}\cdot V_{OV,MD1}^3} \cdot\left(\frac{1}{K_{MD1}}\cdot\frac{\partial K_{MD1}}{\partial T}+\frac{3\beta}{V_{OV,MD1}}\cdot\frac{\partial V_{TH,MD1}}{\partial T}\right). \tag{10}$$

MD_1 in Fig. 11 is biased with $V_{OV,MD1}$ smaller than 100 mV to make the TC of $V_{TH,MD1}$ dominant in (10). Therefore, F_{VTC} has a negative TC.

On the other hand, the conversion factor of the TVC in Figs. 11 and 13 is given by

$$F_{TVC} = \frac{V_{out,diff}}{\Delta t} = \frac{2\cdot I_{CP}}{C_s} = \frac{2\cdot K_{MC1}\cdot {V_{OV,MC1}}^2}{C_s} = \frac{2\cdot K_{MC1}}{C_s}\cdot\left(V_{DD}-\frac{I_{CP}}{\gamma}\cdot R - V_{TH,MC1}\right)^2 \tag{11}$$

where $K_{MC1} = 1/2\times\mu_n\times C_{ox}\times(W/L)_{MC1}$. I_{CP} is the drain current of MC_1. γ is the current mirror factor between MC_1 and MC_0. $V_{TH,MC1}$ and $V_{OV,MC1}$ are the threshold voltage and the overdrive voltage of MC_1, respectively. C_S is the total sampling capacitance in the second-stage SAR ADC. The TC of (11) is given by

$$\frac{\partial F_{TVC}}{\partial T} = \frac{-\frac{\gamma}{R}\cdot\frac{2}{C_s}}{\frac{\gamma\cdot V_{OV,MC1}}{2\cdot I_{CP}\cdot R}+1}\cdot\left(\frac{\partial V_{TH,MC1}}{\partial T}-\frac{V_{OV,MC1}}{2\cdot K_{MC1}}\cdot\frac{\partial K_{MC1}}{\partial T}\right). \tag{12}$$

As $I_{CP}\times R = \gamma\times(V_{DD}-V_{GS,MC1})$, where $V_{GS,MC1}$ is the gate-to-source voltage of MC_1. Therefore, the TC of conversion factor of the TVC is simplified as

$$\frac{\partial F_{TVC}}{\partial T} \cong -\frac{2\cdot\gamma}{R\cdot C_s}\cdot\left(\frac{\partial V_{TH,MC1}}{\partial T}-\frac{V_{OV,MC1}}{2\cdot K_{MC1}}\cdot\frac{\partial K_{MC1}}{\partial T}\right) \tag{13}$$

where MC_1 is biased with $V_{OV,MC1}$, which is about 120 mV to make the TC of $V_{TH,MC1}$ (negative TC [31]) dominant in (13). Here, thermal variation of R is ignored. Therefore, F_{TVC} has a positive TC.

Similarly, using the same derivation procedure of the temperature variation analysis, (14) and (15) show the supply VC of VTC and TVC, respectively

$$\frac{\partial F_{VTC}}{\partial V_{DD}} = \frac{C_A}{K_{MD1}\cdot V_{OV,MD1}^3}\cdot\left(1-\frac{3\cdot\delta\cdot V_{DD}}{V_{OV,MD1}}\cdot\frac{\partial V_{TUNE}}{\partial V_{DD}}\right) \tag{14}$$

$$\frac{\partial F_{TVC}}{\partial V_{DD}} = \frac{4}{C_s}\cdot\frac{V_{DD}-V_{TH,MC1}-\frac{I_{CP}\cdot R}{\gamma}}{\frac{1}{K_{MC1}}+\frac{2R}{\gamma}\cdot\left(V_{DD}-V_{TH,MC1}-\frac{I_{CP}\cdot R}{\gamma}\right)} = \frac{4}{C_s}\cdot\frac{V_{OV,MC1}}{\frac{1}{K_{MC1}}+\frac{2R}{\gamma}\cdot V_{OV,MC1}} \tag{15}$$

where $\delta = \beta\times(V_{DS,MD4}/V_{OV,MD4})$, β is the factor in (9). When deriving (14), we assume $V_{DD} = 2\times V_{CM}$. Under the same bias conditions, (14) and (15) have a negative VC and a positive VC, respectively.

B. Noise Analysis of the Time-Based Residue Amplifier

The noise of the time-based residue amplifier consists of noise from the VTC and TVC. For the stochastic zero-crossing delay variables td_P and td_N in Figs. 11 and 12, their delay difference variance due to circuit noise is given by

$$\sigma^2_{td_P-td_N} = \sigma^2_{td_P}+\sigma^2_{td_N}-2\mathrm{cov}[td_P, td_N]. \tag{16}$$

Since td_P and td_N are correlated due to the same noise sources, their covariance cov[td_P, td_N] is complex. For simplicity, the worst case output noise power of the VTC is given by

$$\left(\sigma^2_{td_P-td_N}\right)_{worst} = (\sigma_{td_P}+\sigma_{td_N})^2. \tag{17}$$

The zero-crossing delay variance is affected by three terms which are windowed integrals of thermal noise, initial integrated thermal noise (KT/C), and noise from a ZCD [32]. The jitter derivation for an inverter-based ring oscillator in [32] is still applicable to our noise analysis. According to [32], the time delay variance is given by

$$\sigma^2_{td_P} = \frac{td_{P0}}{2I^2_{MD1,P}}\cdot S_{iP,noise}+\frac{KTC_A}{I^2_{MD1,P}}+\frac{C_A^2\overline{v^2_{i,noise-ZCD}}}{I^2_{MD1,P}} \tag{18}$$

$$\sigma^2_{td_N} = \frac{td_{N0}}{2I^2_{MD1,N}}\cdot S_{iN,noise}+\frac{KTC_A}{I^2_{MD1,N}}+\frac{C_A^2\overline{v^2_{i,noise-ZCD}}}{I^2_{MD1,N}} \tag{19}$$

$$S_{iP,noise} = S_{iN,noise} = 2kT\gamma g_{m,MD1}+kTg_{ds0,MD4} \tag{20}$$

$$td_{P0} = \frac{C_A(V_{DD}-V_{CM})}{I_{MD1,P}} \tag{21}$$

$$td_{N0} = \frac{C_A(V_{DD}-V_{CM})}{I_{MD1,N}} \tag{22}$$

where $S_{iP,noise}$ and $S_{iN,noise}$ are noise power spectral densities due to MD1 and MD4 at V_P and V_N in Fig. 11 before zero-crossing occurs, respectively. The last two terms of (18) and (19) are much smaller than the first term, and the second term of (20) is significantly smaller than the first term. Because of a small input voltage (the difference between $I_{MD1,P}$ and $I_{MD1,N}$ is small), the input-referred noise of the time-based residue amplifier due to the VTC in the worst case is given by

$$\overline{v^2_{i,noise-VTC}} = \frac{(\sigma_{td_P}+\sigma_{td_N})^2}{F^2_{VTC}} \cong \frac{4kT\gamma}{C_A}\cdot\frac{I_{MD1}}{g_{m,MD1}(V_{DD}-V_{CM})}. \tag{23}$$

The output noise of the TVC is given by [23]

$$\overline{v^2_{o,noise-TVC}} = \frac{4kT\gamma}{2C_A^2}\cdot\ (g_{m,MC1}+g_{m,MC4})\cdot T_{ON} \tag{24}$$

where T_{ON} is the time used for dead zone elimination in Fig. 12. According to (6) and (24), the input-referred noise

of the time-based residue amplifier due to the TVC is given by

$$\overline{v_{i,\text{noise}-\text{TVC}}^2} = \overline{v_{i,\text{noise}-\text{VTC}}^2} \cdot \frac{I_{\text{MD1}}^3 \cdot T_{\text{ON}} \cdot \ (g_{m,\text{MC1}} + g_{m,\text{MC4}})}{8 \cdot I_{\text{CP}}^2 \cdot C_A \cdot \ (V_{\text{DD}} - V_{\text{CM}}) \cdot g_{m,\text{MD1}}}. \quad (25)$$

Since T_{ON} is much less than the integration time (td_P and td_N) of the dynamic integrator, the noise in (25) is much less than the noise in (23). Therefore, the input-referred noise of the time-based residue amplifier in Fig. 11 is dominated by the noise from the VTC.

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