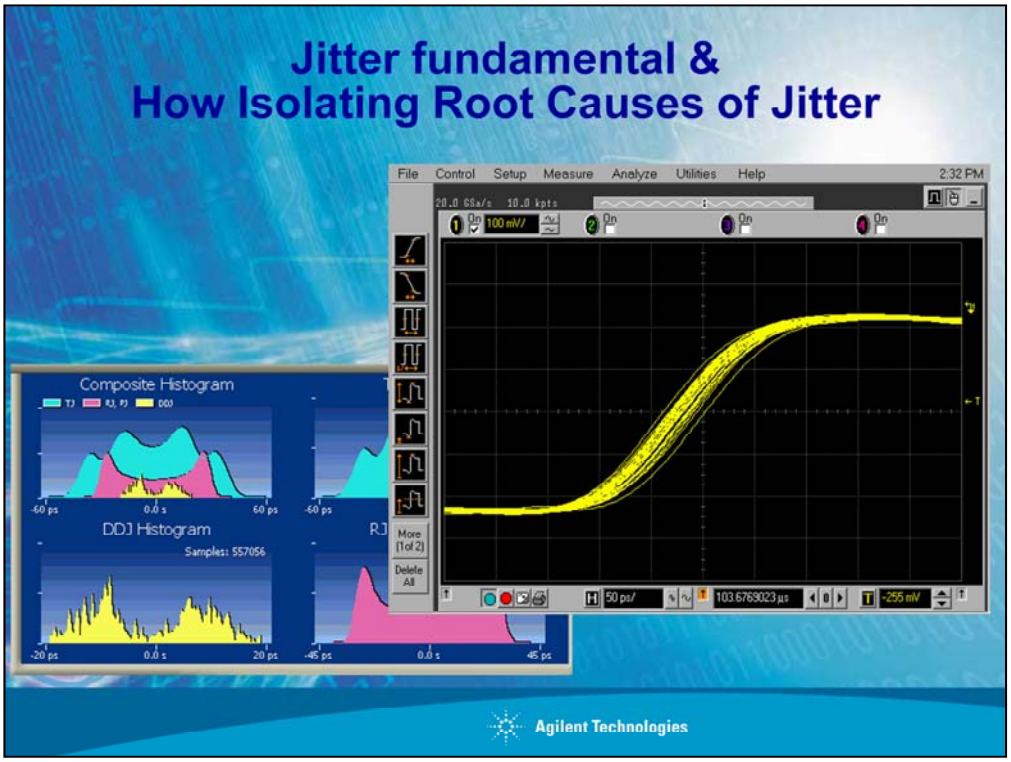

Isolating Root Causes of Jitter

High-speed serial data links have been around for a while in the data storage and communications worlds, primarily for box-to-box communications. Examples include SONET and FibreChannel. Now those techniques and high data rates are migrating inside PCs, servers, and embedded systems; examples include PCI-Express, SATA, RapidIO, and HyperTransport.

As data rates go up, jitter becomes more critical and the jitter budget becomes tighter. Some instruments, such as Bit Error Ratio Testers (BERT) are optimized for determining the total amount of jitter and eye-opening for your high-speed digital system and can be used to test for compliance based on industry standards. But when jitter measurements do not meet a particular minimum standard, or if jitter measurement results are "too close for comfort", then measuring the amount of component or system jitter is just half of the jitter test equation. Determining the root-cause of jitter is the other half of the equation. During this seminar we will share with you some "tips & tricks" on using real-time oscilloscopes with jitter analysis to separate and time-correlate specific deterministic jitter components to help identify sources of systematic timing errors.

Agenda

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- What is BER?
- What is Jitter?
- What is an Eye Diagram?
- Why Separate Jitter?
- Total Jitter Components
- Receiver Jitter tolerance

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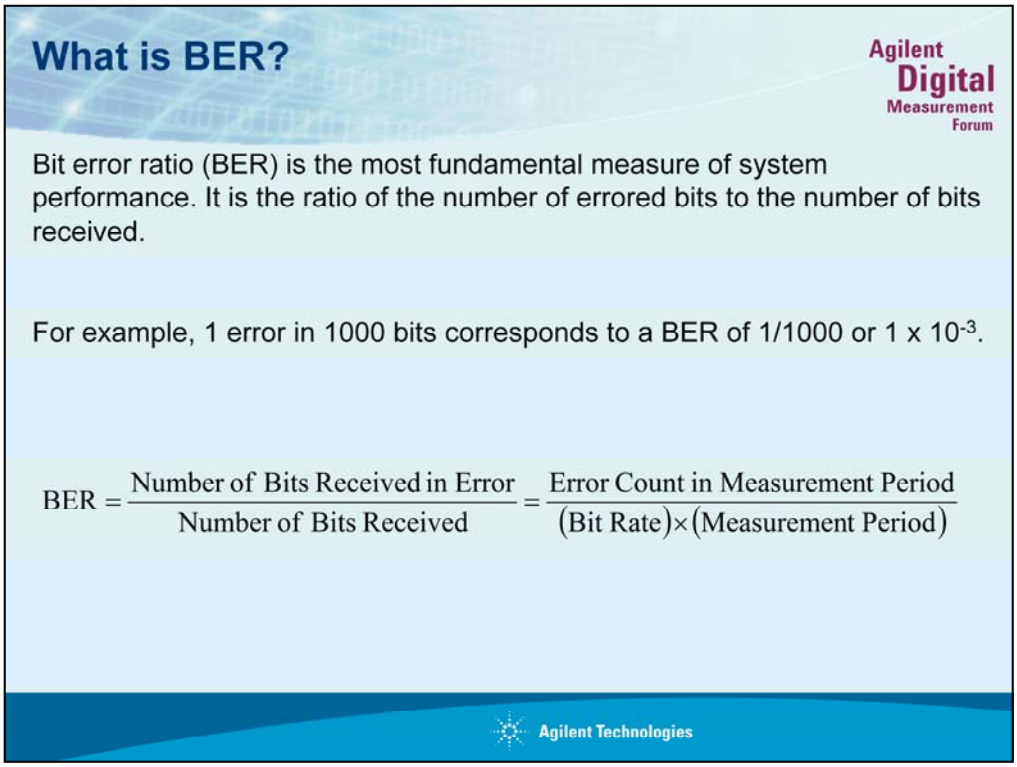
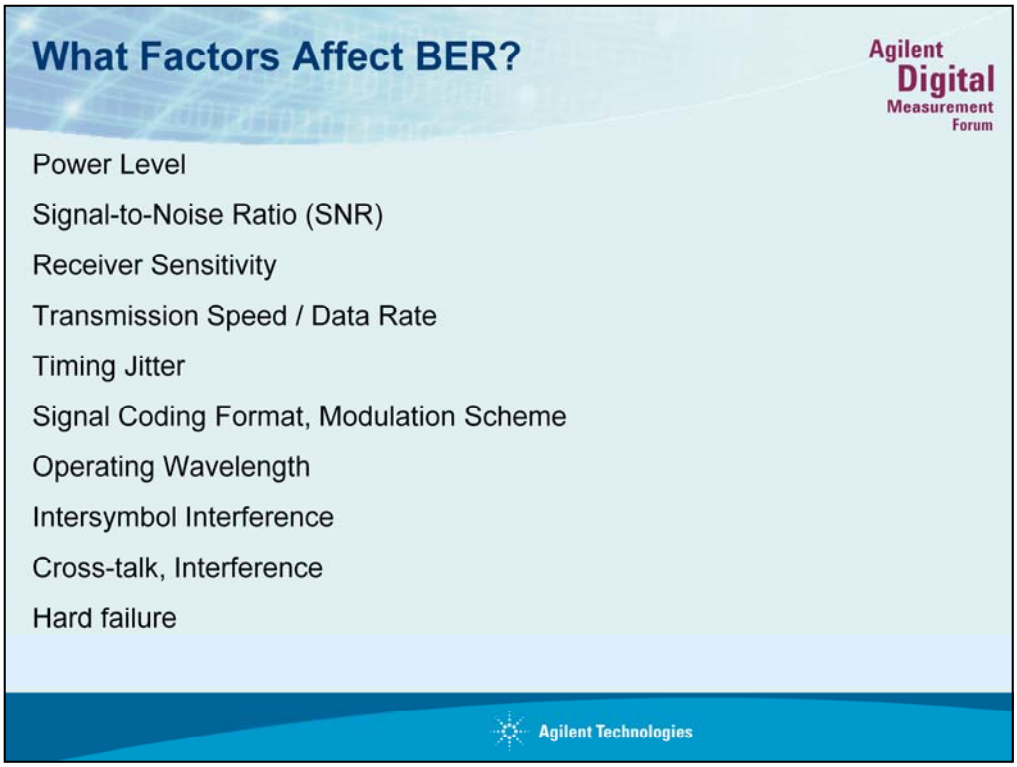


When transmitting digital information – it all comes down to bits. Bits are binary digits - something that represents a 1 or a 0. Bits are transmitted, go through networks and systems and different devices, and bits are received. Sometimes the bits don't arrive in the same way that they were sent. All 1's don't arrive as 1's, all 0's don't arrive as 0's. These are called bit errors. The industry standard way of measuring bit errors is the bit error ratio, or BER.

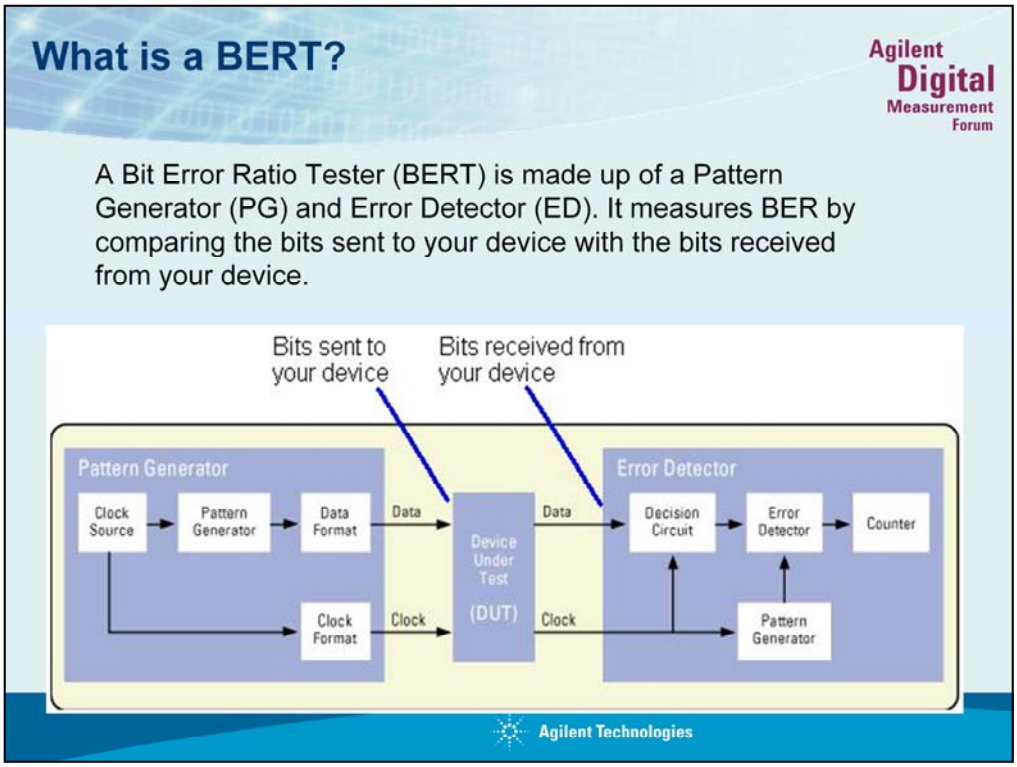
Note that the term "bit error rate" is often used interchangeably with "bit error ratio." Bit error ***rate*** is technically inaccurate. Bit error ***ratio*** will be used throughout this course.

A BER measurement allows you to prove that your device meets performance specifications. An example of a good BER is 1×10^{-12}. A bad BER may be 1×10^{-2}. What is considered good or bad depends on your application.



When transmitting digital information, a number of factors can affect BER.

Given this broad range of factors, you can probably see the benefit of having an instrument that can be used to analyze bit errors and help isolate the cause.



We will consider the main components and functions of a BERT. But first, a quick overview.

The device under test will be specific to your application. For example, it may be a transmitter/receiver pair, a MUX/DEMUX pair, or an amplifier.

A repeating pattern of bits is sent from the PG data output to your device at a certain bit rate (or frequency), and in a specific electrical format. At the same time, the expected data output pattern of your device is internally generated in the ED - this provides a reference by which to compare the output pattern of your device.

A clock signal from the PG clock output may also be sent to your device in a specific electrical format.

The ED receives the data output pattern of your device, and also requires a frequency reference (from the clock signal of your device or the PG). The incoming bits from the data pattern are sampled in “decision” circuitry and synchronized with the internal reference pattern. Each bit from the incoming pattern is compared with the reference and a BER measurement is made.

Verify BER 1e-12

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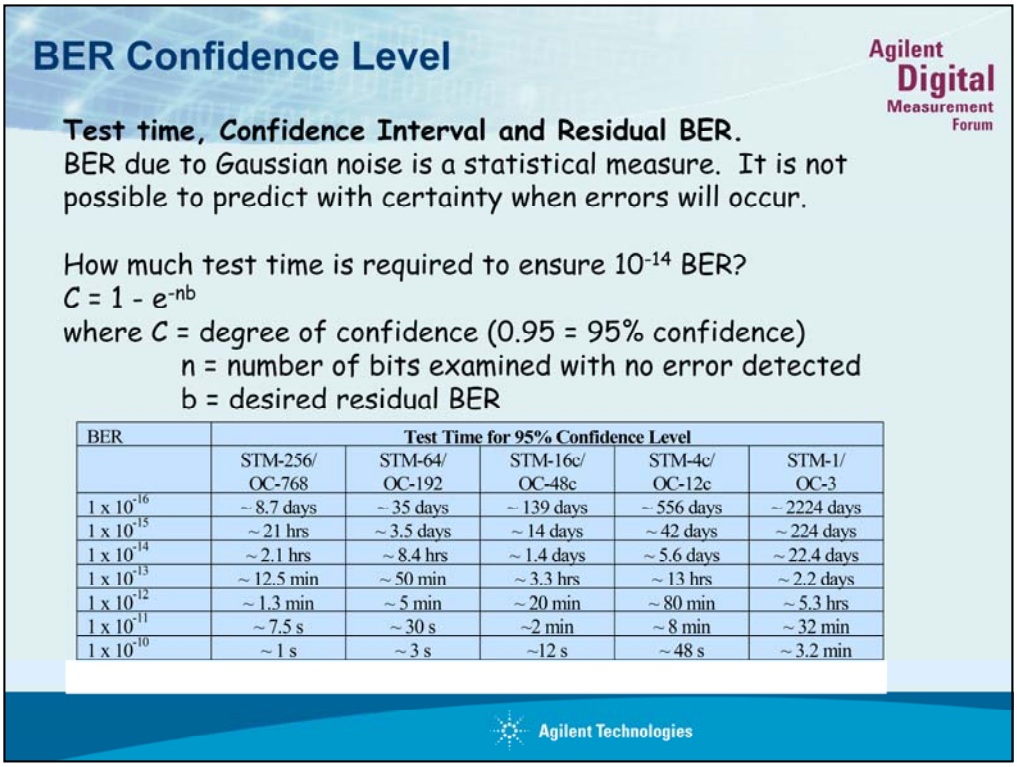
Test 1e12 bits with no error?

Test 3x 1e12 bits with no error?

BER Testing is a matter of statistic!

The number of bits tested correspond to a confidence level:

- Test 3x 1e12 bits with no error corresponds to a confidence level of 95%



BER	Test Time for 95% Confidence Level				
	STM-256/ OC-768	STM-64/ OC-192	STM-16c/ OC-48c	STM-4c/ OC-12c	STM-1/ OC-3
1×10^{-16}	~ 8.7 days	~ 35 days	~ 139 days	~ 556 days	~ 2224 days
1×10^{-15}	~ 21 hrs	~ 3.5 days	~ 14 days	~ 42 days	~ 224 days
1×10^{-14}	~ 2.1 hrs	~ 8.4 hrs	~ 1.4 days	~ 5.6 days	~ 22.4 days
1×10^{-13}	~ 12.5 min	~ 50 min	~ 3.3 hrs	~ 13 hrs	~ 2.2 days
1×10^{-12}	~ 1.3 min	~ 5 min	~ 20 min	~ 80 min	~ 5.3 hrs
1×10^{-11}	~ 7.5 s	~ 30 s	~2 min	~ 8 min	~ 32 min
1×10^{-10}	~ 1 s	~ 3 s	~12 s	~ 48 s	~ 3.2 min

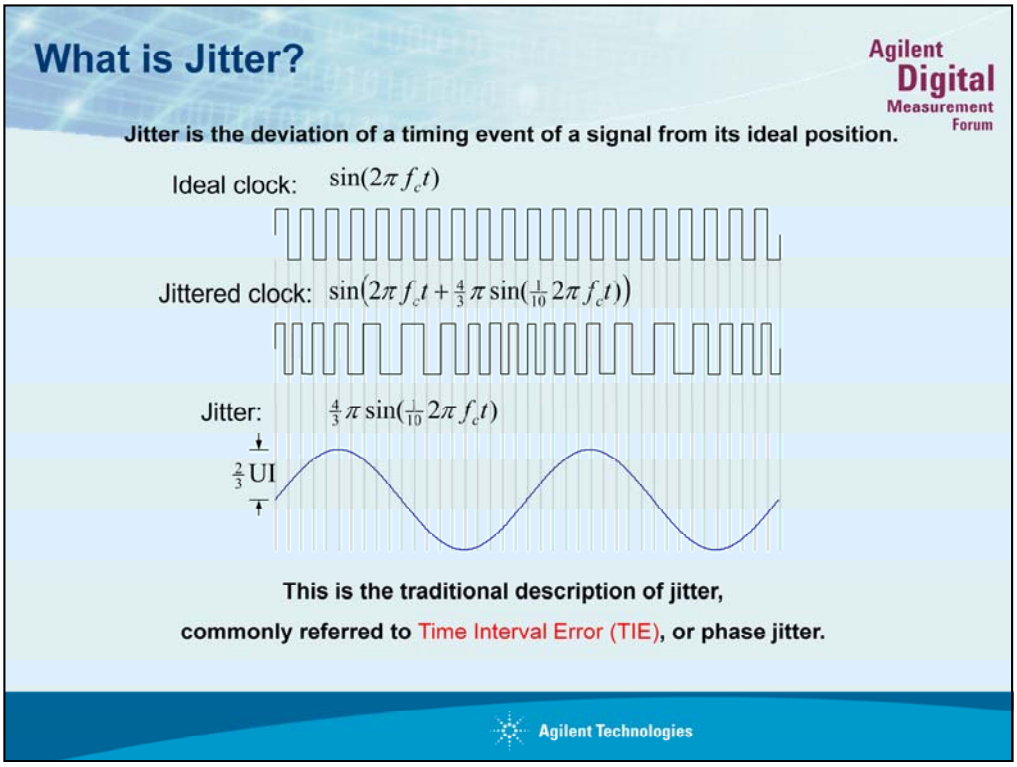
Confidence Level is the likelihood — expressed as a percentage — that the results of a test are real and repeatable, and not just random. The idea is based on the concept of the "normal distribution curve," which shows that variation in almost any data (such as the heights of all fourth-graders, or the amount of rainfall in January) tends to be clustered around an average value, with relatively few individual measurements at the extremes.

So if your confidence level is, say, 92%, that means, according to probability theory, there's a 92% chance that you'd see similar results in a repeat of the test. (It does not mean you'd receive the same numbers, or that the difference between would be the same. It only means that the number in the first test would be likely to the number in the second as well — unless, of course, some significant other factors have changed.)

A confidence level of 50% would mean the difference is truly random, with only a 50-50 chance that you'd see the same results in a repeat of the test. Even at 75% the odds are not good — there's a one in four chance that your results are meaningless. Some statisticians consider 90% to be the minimum confidence level for statistically significant results, and that's reportedly the standard used in many election polls. Others insist on a minimum of 95% to be considered significant. And in medical research, for obvious reasons, there's a strong preference for even higher levels of confidence.

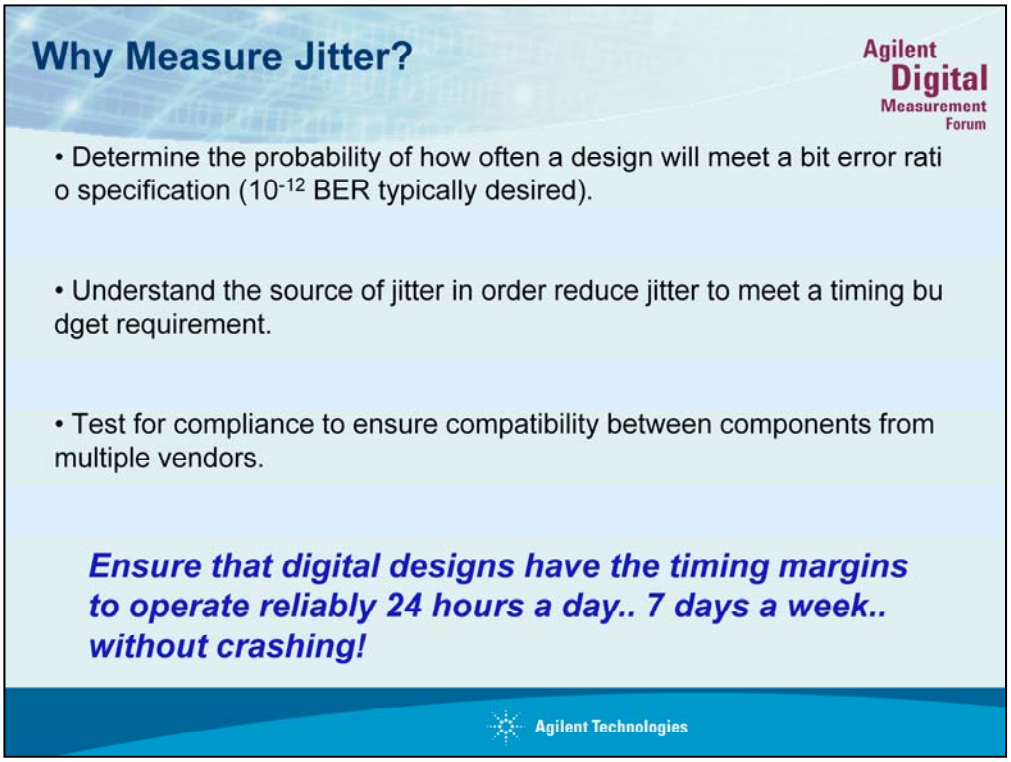
It's important to remember that we're talking about probabilities, and there's no magic number that guarantees your results will be repeatable. While it's always best to have a confidence level of 95% or higher, you shouldn't ignore results in the 80% to 90% range. Those results may indicate trends and provide clues about how to improve your mailings; at the very least, they're worth re-testing, preferably in larger quantities. (In any test, a larger sample size will generally give more reliable results.)

Finally, a few words of caution: These confidence levels are only valid when you're comparing test panels that can be thought of as a single event. Don't try to adapt them to a situation that changes over time (such as your total number of active donors), or use it to compare appeals that mailed at different times (there are far too many uncontrolled variables in that case). You'll also notice that the formula allows you to use test panels of different sizes — but if you do, make sure your merge/purge house is extremely careful about producing statistically equivalent lists of names.



What is Jitter?

Jitter is the deviation of a timing event of a signal from its ideal position. In this particular example we are showing a jittered clock with sinusoidal modulation. By measuring/comparing each edge of the clock relative to an ideal fixed-frequency clock, jitter analysis can then plot the results to view the sinusoidal modulation. This "plot" is usually called a jitter "trend" waveform. Besides measuring clock jitter, measuring jitter on serial data signals with embedded clocks is also very important in today's high-speed digital systems.



Why Measure Jitter?

For today's high-speed digital systems it is extremely important to determine the probability of bit errors. A typical specification that is usually desired is 10^{-12} BER. There is a direct relationship between BER and total jitter.

Another important reason to measure jitter is to debug and find sources of jitter so that they can be reduced in order to meet a timing budget requirement. A Bit Error Ratio Tester (BERT) will provide a very good measure of total eye-opening and BER, but it does not provide any indication as to the source of various jitter components.

Testing for jitter is also a compliance requirement for many bus standards to not only ensure that a product meets a minimum specification, but also ensure compatibility between multiple vendors components.

The bottom line is, testing for jitter can help ensure that your products operate reliability all the time.

Why do we Care about Jitter?

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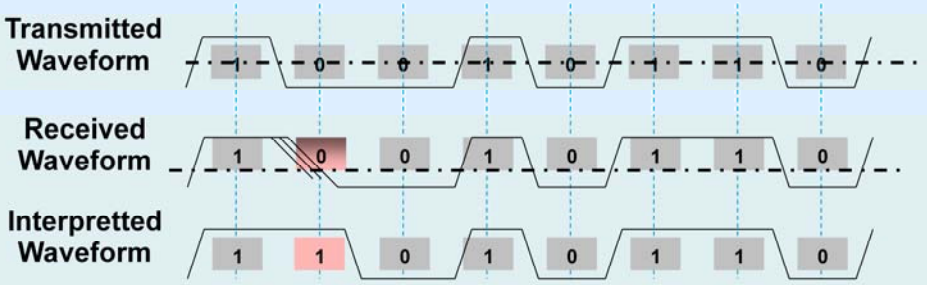
- It Causes Transmitted Bit Errors!



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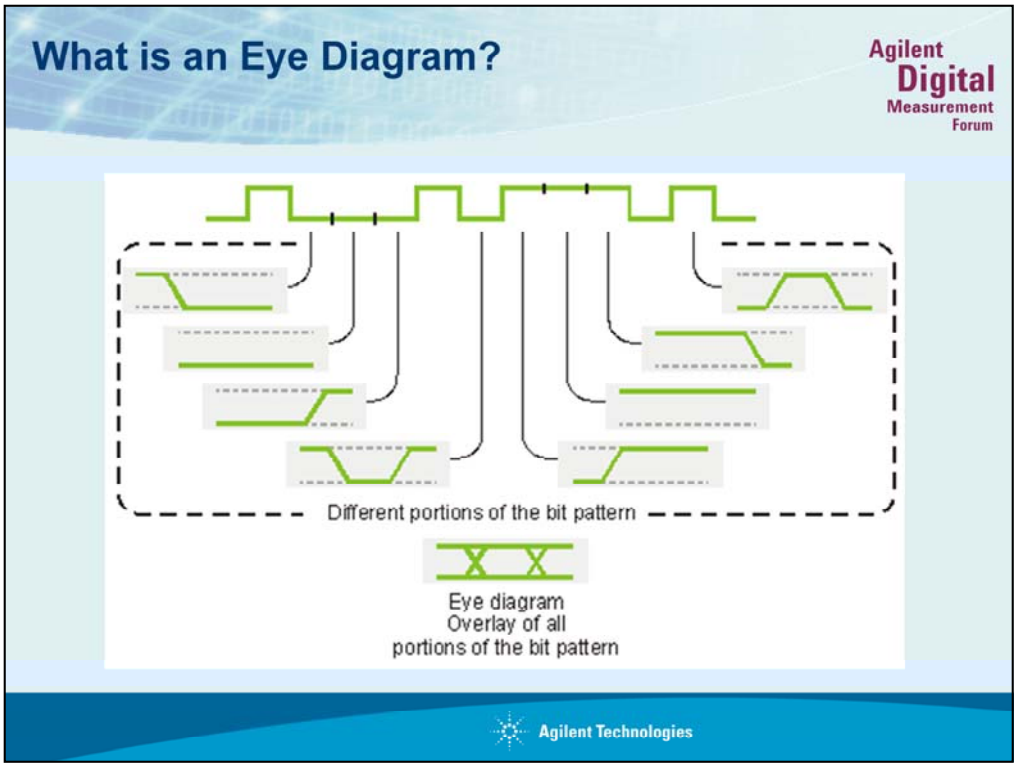

As we consider the next components and functions of a BERT, you will see graphic representations of eye diagrams. Therefore, it's important to review what an eye diagram is.

An eye diagram is a common measurement made with a DCA or an oscilloscope. This diagram provides a way to view all possible one-to-zero combinations of a pattern by overlapping them on the display of a high-speed oscilloscope. It is typically produced from triggering the oscilloscope with a synchronous clock signal.

When the oscilloscope is triggered by a clock signal, data patterns will not be observed. Instead, if persistence is set high enough, an "eye" will be observed. The eye is bounded by overlaid logic 1 and 0 voltages, top and bottom, and multiple 0 to 1 and 1 to 0 transitions, left and right.

A Fundamental View of Jitter

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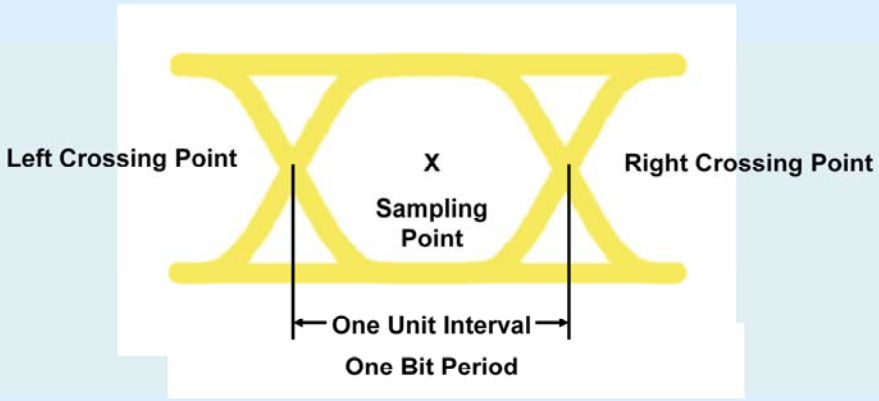
The Eye Diagram



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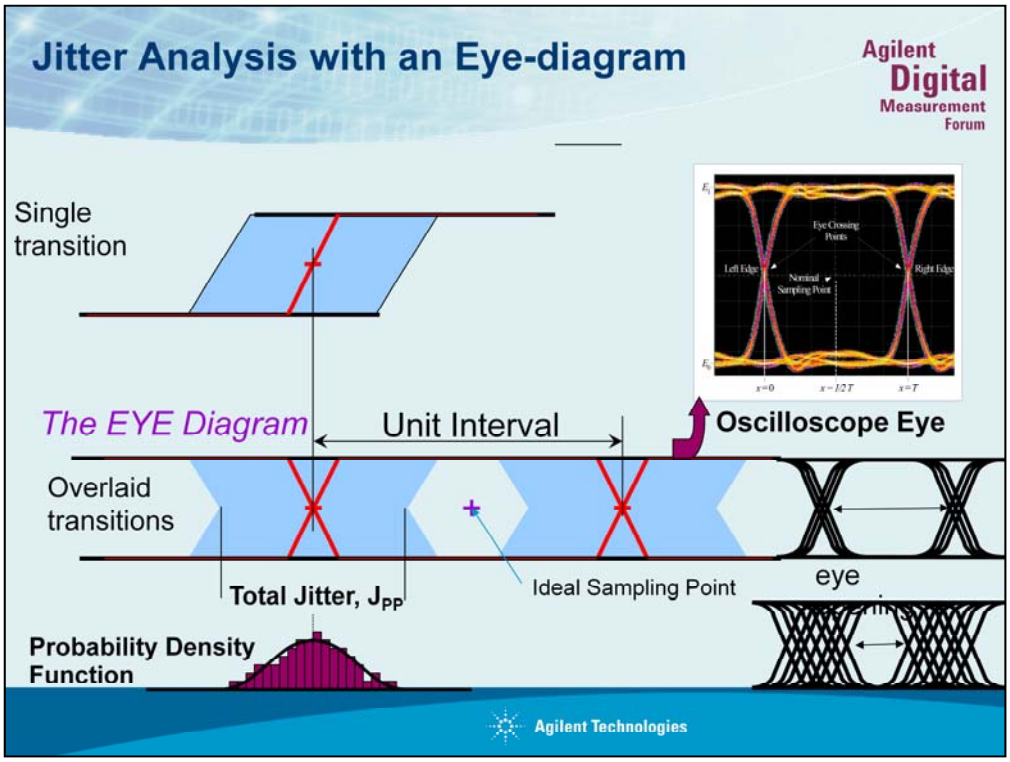


Again we do the slide build thing…

We start with a pictorial of the rising edge… and we show a blue area denoting some sort of probabilistic cloud of edges. But the rising edges arent the only story so lets include falling edges as well. When we do get this idealized eye where we have two crossing points where the red x's are and the clouds about them. If the shaded region isn't too big we will have a space where no trajectory goes and the center of this will be where the idealized sampling point is for lowest possible error.

We note that as before the extremes about a crossing point (at a specific threshold hopefully related to the receiver circuit) is the Jitter peak to peak.

If we kept track of every edge's advance and delay value and binned them and counted the number in each bin we would build a histogram as depicted here. The histogram is a very important view of jitter.

Finally, a real world eye is shown which is very open, but you will note has some over shoot to it.

•Jitter is the primary factor of Bit Error

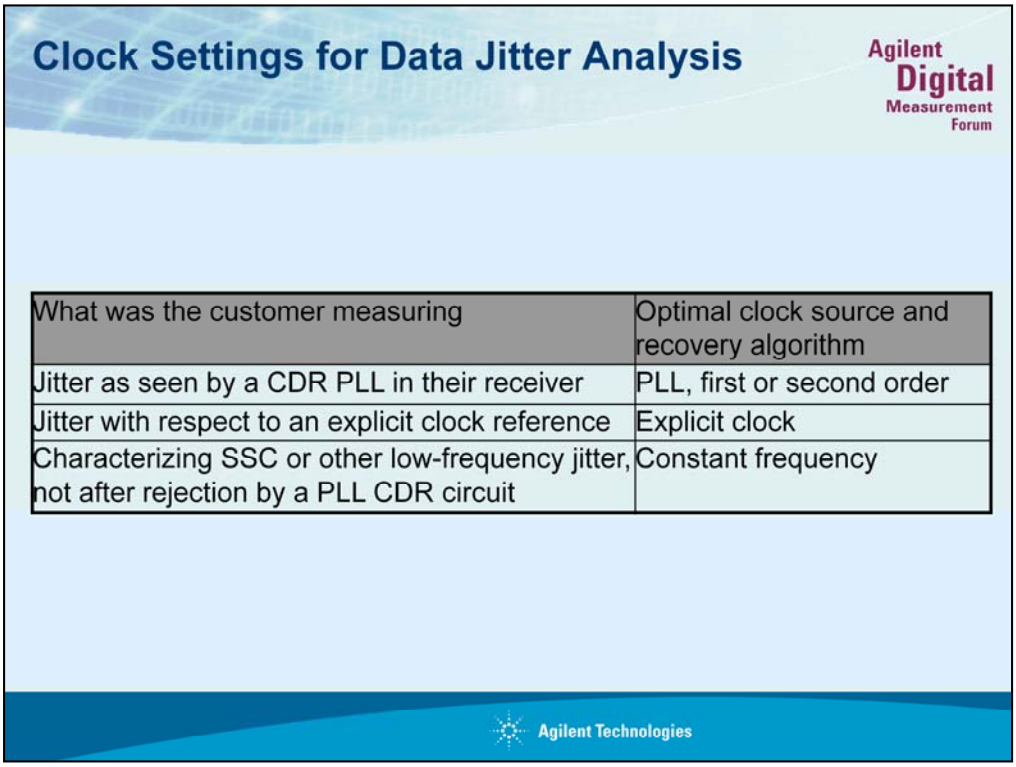
•Jitter decreases valid bit period (eye opening)

•Data Rates Getting Faster and bit period shorter

•The Same amount of Jitter Causing a

5% decrease of eye-opening@500Mb/s

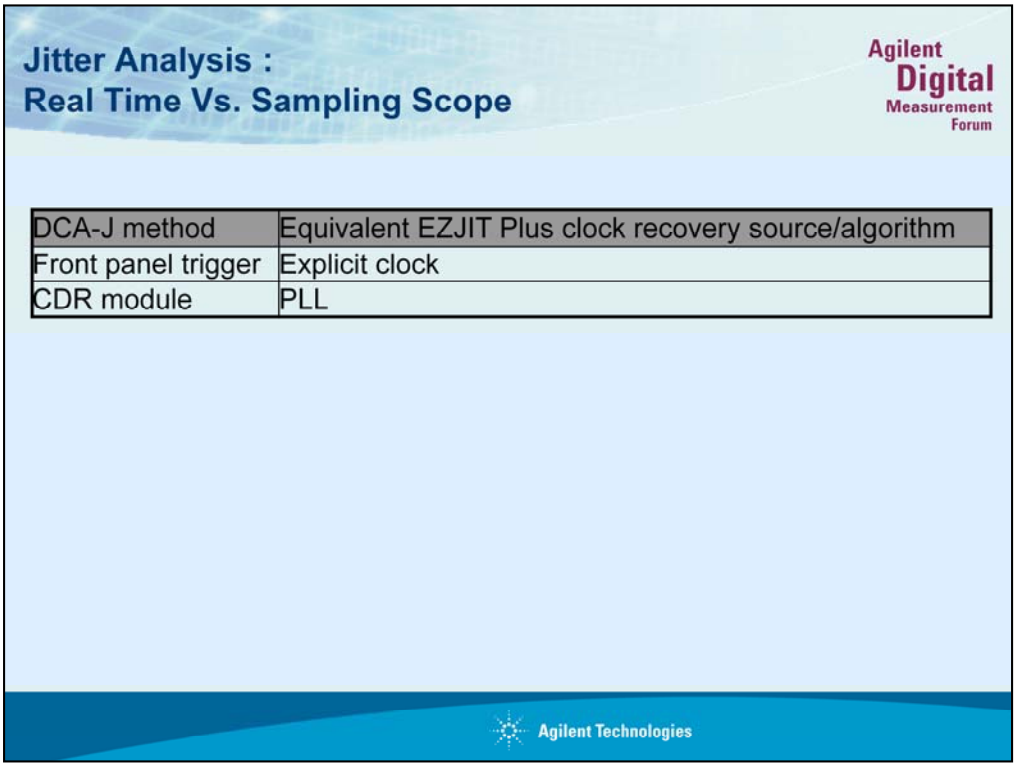
50% decrease of eye-opning@5Gb/s



The clock reference depends on what you were trying to measure. Most serial data is interpreted by a clock and data recovery PLL in the customer's system, so using a PLL recovery algorithm that mimics as closely as possible the specs of the customer's CDR PLL will in most cases yield the most meaningful answer.

If the system under test uses an explicit clock as the reference, then the explicit clock choice is most appropriate.

If the customer needs to characterize, for example, SSC, which would be rejected by the PLL CDR in their receiver, they will want to use the constant frequency clock recovery algorithm.



Oftentime the question is phrased as “I measured jitter with the DCA-J and with EZJIT Plus and the numbers weren’t the same.” The most common cause is that the clock reference is different. DCA-J doesn’t have en equivalent to EZJIT Plus’s “Constant Frequency“ algorithm. If the clock reference on the DCA-J is a signal applied to the front panel trigger, the equivalent technique in EZJIT Plus is “Explicit Clock.” If using a CDR module in the DCA-J to derive the clock reference from the data signal, use the PLL clock recovery in EZJIT Plus and set its corner frequency to the same as the CDR module in the DCA-J.

Demonstrating the differences in clock recovery sources and algorithms with easily available signal sources is not easy. In my experimentation, the jitter measured using either an 81134A or SerialBERT (and I assume 81141A) is quite low (close to the scope’s measurement floor capability), and you don’t see much difference when changing clock recovery source or algorithm. But in real customers’ systems, you may see a difference. In that case you can explain the differences by understanding this material.

Why Separate Jitter?

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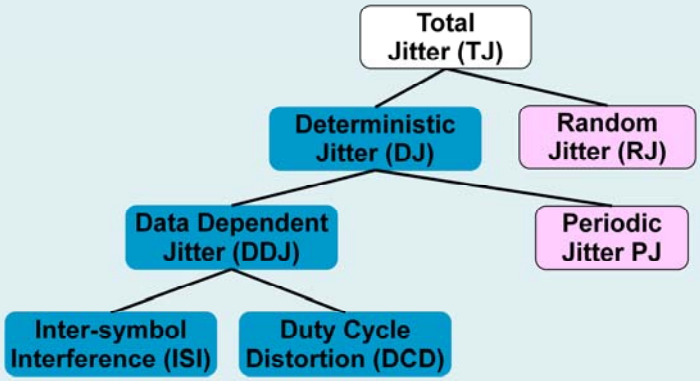
Mechanism to enable fast estimates of Total Jitter (TJ) at low BER

Tool to support budgeting of jitter in new and evolving designs

Diagnostic tool for troubleshooting jitter



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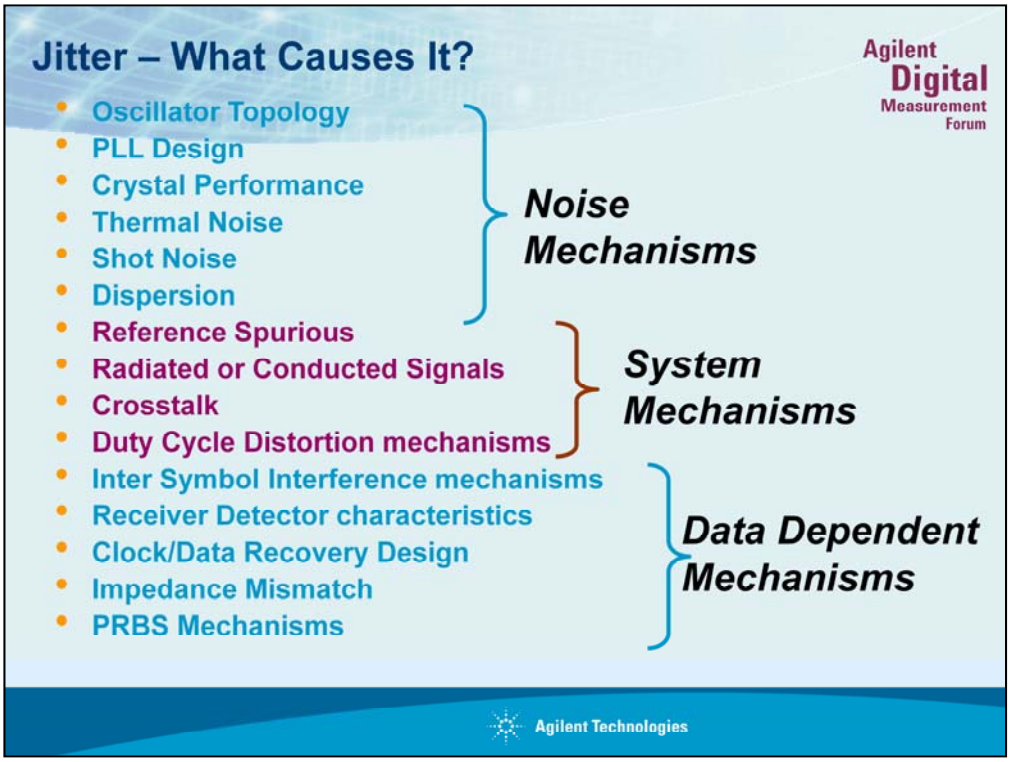
Jitter – What Causes It?
Agilent
Digital
Measurement
Forum
Oscillator Topology
PLL Design
Crystal Performance
Thermal Noise
Shot Noise
Dispersion
Noise Mechanisms
Reference Spurious
Radiated or Conducted Signals
Crosstalk
Duty Cycle Distortion mechanisms
System Mechanisms
Inter Symbol Interference mechanisms
Receiver Detector characteristics
Clock/Data Recovery Design
Impedance Mismatch
PRBS Mechanisms
Data Dependent Mechanisms
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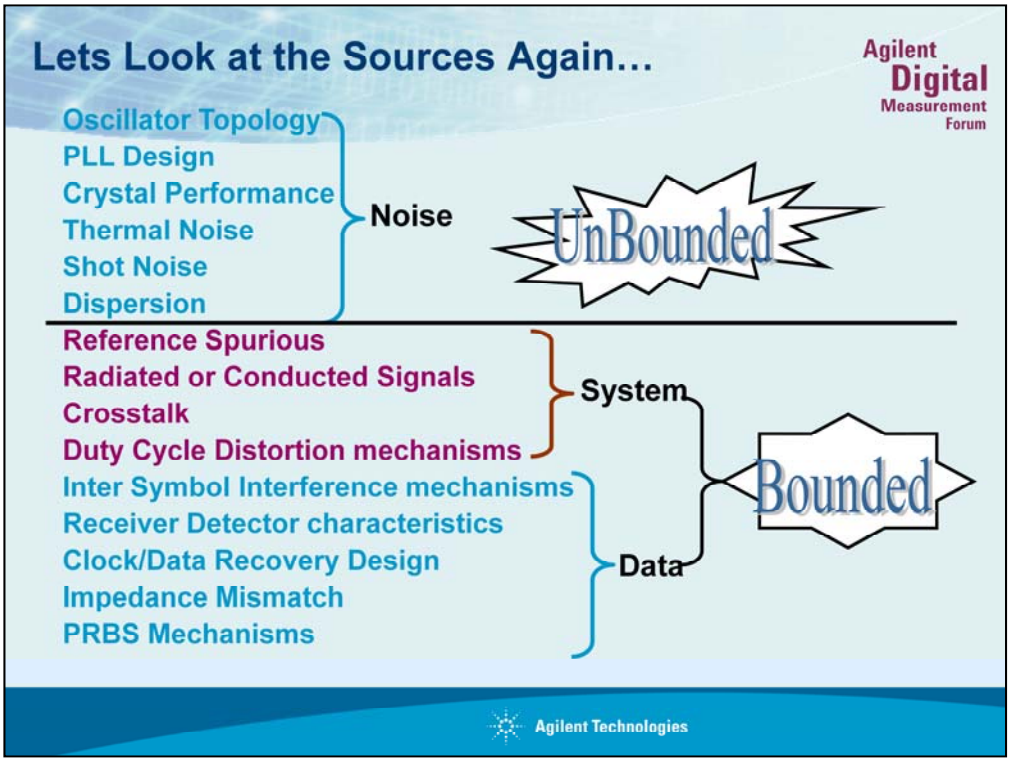
Lets Look at the Sources Again…
Agilent
Digital
Measurement
Forum
Oscillator Topology
PLL Design
Crystal Performance
Thermal Noise
Shot Noise
Dispersion
Noise
UnBounded
Reference Spurious
Radiated or Conducted Signals
Crosstalk
Duty Cycle Distortion mechanisms
System
Inter Symbol Interference mechanisms
Receiver Detector characteristics
Clock/Data Recovery Design
Impedance Mismatch
PRBS Mechanisms
Data
Bounded
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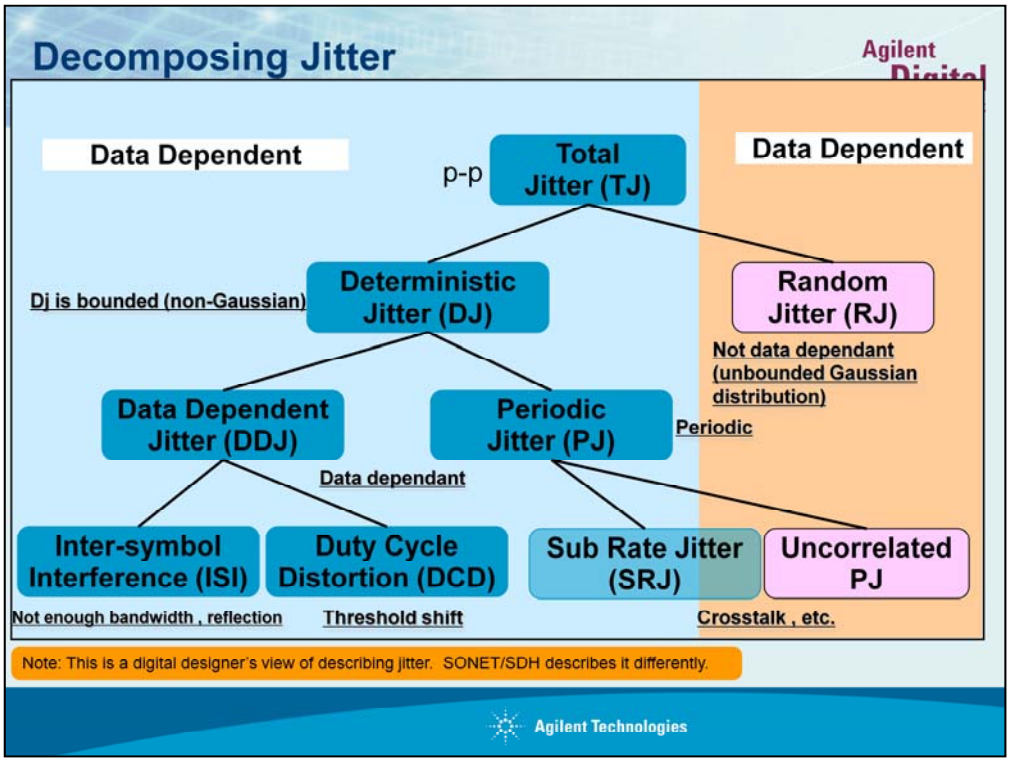
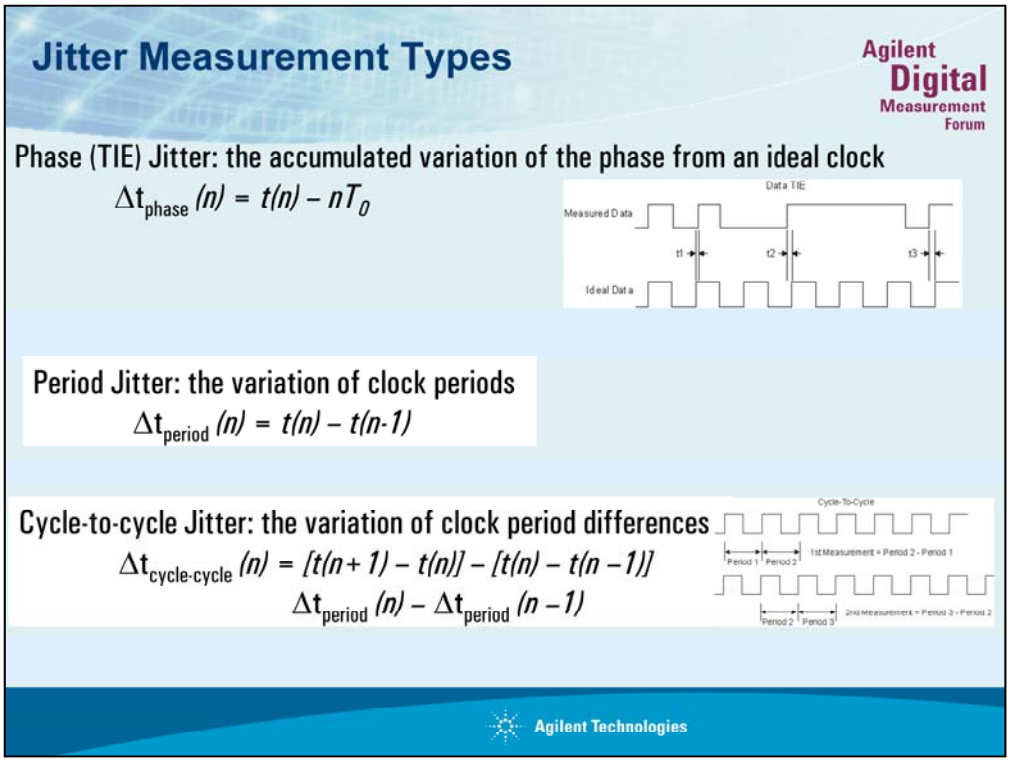


Let's familiarize ourselves with the components of jitter. As we said, Total Jitter is composed of Random jitter (which is unbounded) and Deterministic Jitter (which is bounded or systematic). It's specified as peak-to-peak, similar to DJ but since RJ is Gaussian, it's measured as RMS and extrapolated to peak-to-peak.

DJ can be broken down into Periodic Jitter, Data Dependent Jitter, and Bounded Uncorrelated Jitter. PJ is sinusoidal, DDJ is due to data smearing, and Uncorrelated is due to Crosstalk.

Your jitter measurement will likely provide insight into which component is your biggest source of error. In the eye diagram in slide 9, you can see 2 distinct bands in the trailing edge and 3 distinct bands in the rising edge. This signal seems to have a strong DJ component.



A recent interaction with a customer revealed that they had a component with a jitter specification from a third party but the two parties could not agree on the result. It turns the part was specified as total jitter but no indication was made on how this was measured. There really is no good assumption to make as many default to TIE while others are interest in period jitter or cycle to cycle. It is a good idea to understand the methodology customers are using. When specific standards are brought up there should be no ambiguity. SATA: Cycle to Cycle; FibreChannel: TIE; etc.

There are two ways to find the Serial Data TIE: Automatic mode or Manual mode. In the Automatic mode, Infiniium determines the ideal data rate by searching your waveform for the narrowest pulse. The data rate is calculated and used as the ideal data rate. In the Manual mode, you enter the value for the ideal data rate.

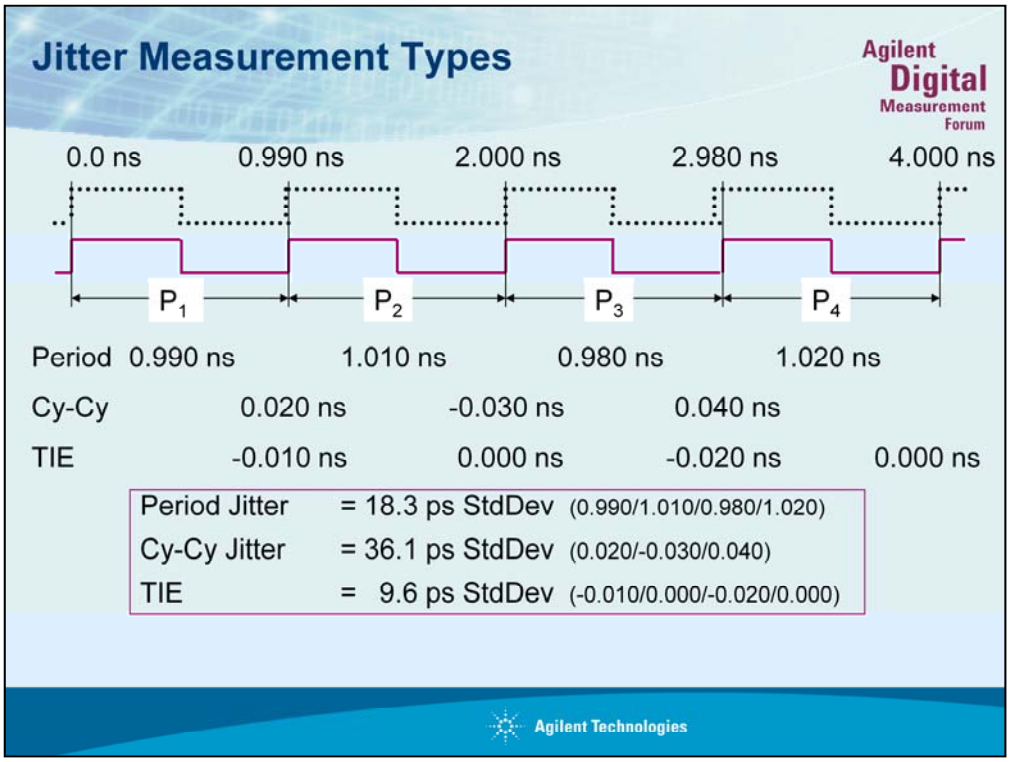
Once the ideal data rate is determined, all of the data intervals are measured with respect to the ideal data rate and the error statistics are computed. The following figure shows how Data TIE is measured on rising edges of the data.

There are two ways to find the Clock TIE: Automatic mode and Manual Mode. In the Automatic mode, Infiniium determines the ideal clock frequency by measuring the frequency of all the cycles in your waveform and taking the average of all the measurements. In the Manual mode, you enter the value for the ideal clock frequency.

Once the ideal clock frequency is determined, all of the cycles of your waveform are compared to the ideal clock frequency and the error statistics are computed. The following figure shows how the Clock TIE is measured on rising edges of the clock

The period measurement is defined as the time between the middle threshold crossings of two consecutive, like-polarity edges.

The cycle-to-cycle jitter measurement measures the period of the first cycle of the waveform and subtracts it from the period of the second cycle of the waveform for the first measurement result. Then, the second cycle of the waveform is measured and subtracted from the third cycle period for the second measurement result. This operation continues until all of the cycles of the waveform have been measured. The following figure shows two cycle-to-cycle measurements ; All of the measurement results are used to compute the statistics. The statistics are the values accumulated over all of the trigger cycles that have occurred.



This example points out the difference between the various methods. For period jitter, the average value is the nominal period and std deviation is the jitter sigma. For the cycle to cycle, the average value indicates long term period error and should be about 0 for short term jitter and longish records. Time Interval Error is the difference from an extracted (or explicit) clock on a cycle to cycle basis…low frequency variations will be followed according to a PLL formula that the receiver circuits will implement.

Characteristics of the Causes of Jitter

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- **Causes of Jitter are categorized Two Ways:**
  - **Those where the phase deviation achieves a Max and a Min value over an identifiable time interval..**

And….

- **Those that don't!!**

$$P(\sin(2\pi f_d t + \varphi(t)))$$

$$P(\sin(2\pi f_d t + \varphi_B(t) + \varphi_{UB}(t)))$$

$\varphi_B(t)$ is composed of functions that have Bounded phase deviations because their max amplitudes don't change

$\varphi_{UB}(t)$ is composed of functions that have UnBounded phase deviations because their max amplitudes do change. The functions are characterized by their statistics

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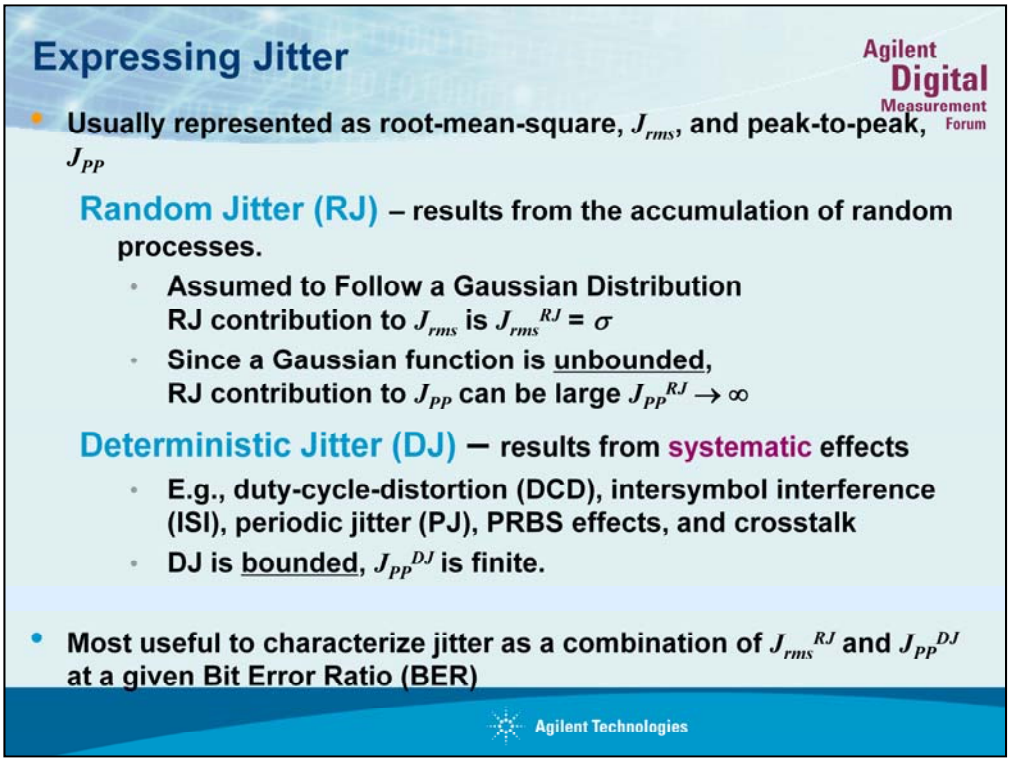
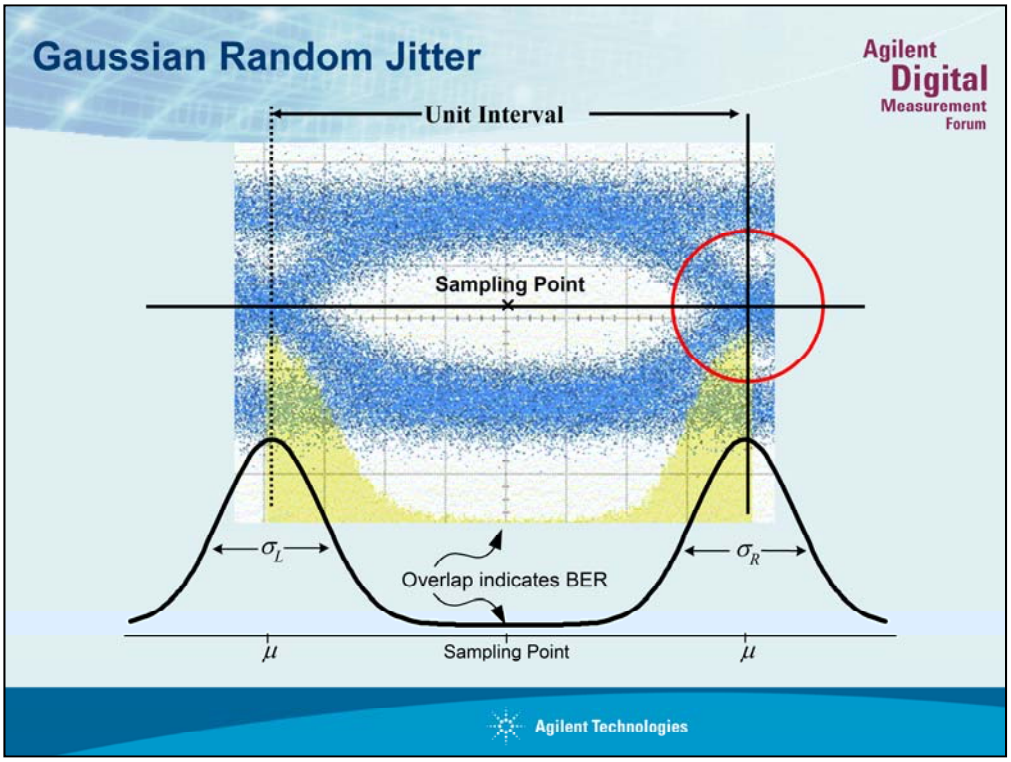


Test patterns induce data dependent jitter



There is random and there is gaussian random---

This is linear view of histogram and is hard to differentiate the effects at the bottom. In Log mode can see tail effects clearly. If sigmas aren't equal then we don't have true random---if these are significantly different we might be talking about deterministic type PRBS effects.

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Designing to a Jitter and BER Budget

- Since J_{PP}^{RJ} is unbounded, it can be *defined* by the BER that would result if there were *only* RJ. This is where the tails of the right and left distributions overlap (at the Sampling point):

  For a BER = 10^{-12} → $J_{PP}^{RJ} = 14\times\sigma$ … *7 for each tail*

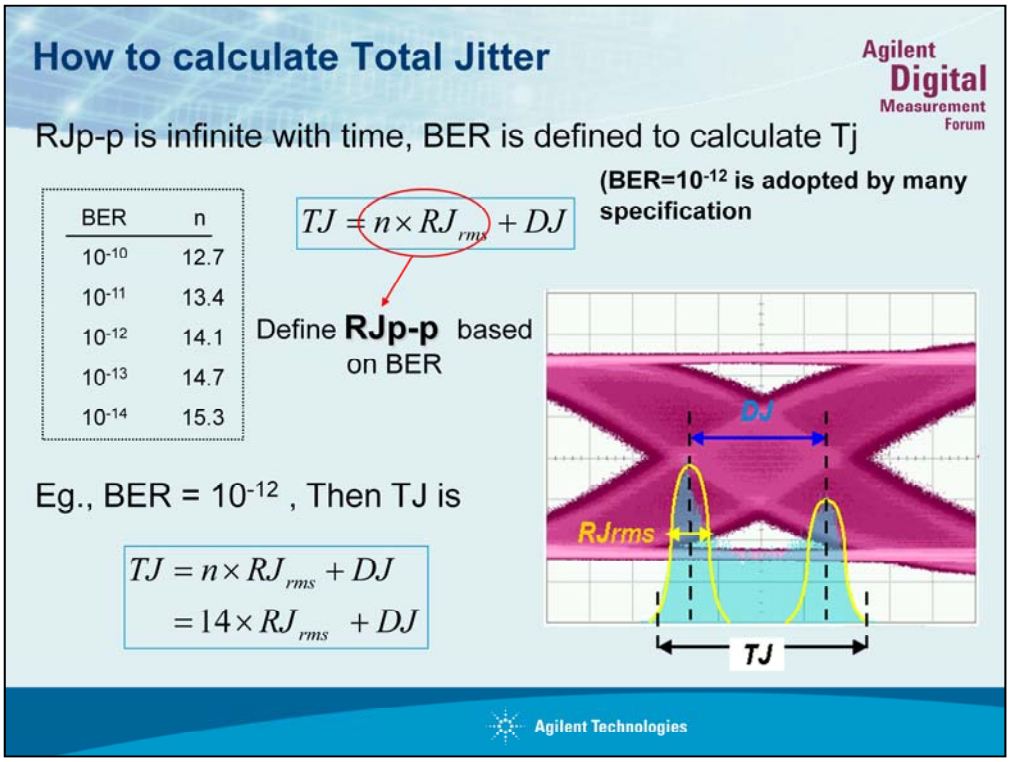
  Then $J_{PP}^{RJ} \equiv n\times\sigma$ so that $J_{PP}^{RJ} = nxJ_{rms}^{RJ}$

- The Total Jitter (TJ), J^{TJ}, for a given BER is then

$$J^{TJ} = n\times J_{rms}^{RJ} + J_{PP}^{DJ}$$
$$= 14\times\sigma + J_{PP}^{DJ}$$

which can be compared to a given jitter + BER budget

J_{PP}, is useful for isolating rare error causing events.

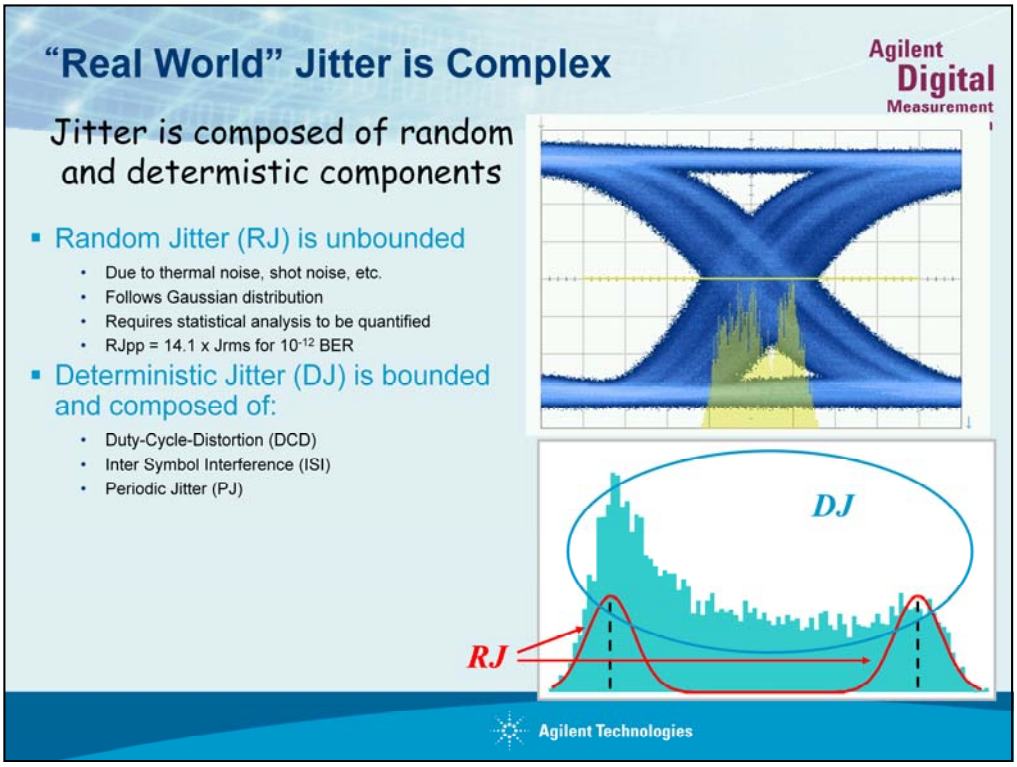


Jitter is due to both random and deterministic mechanisms. In that there are random elements to the jitter, the jitter is then theoretically unbounded. That is, if one were willing to wait long enough, the jitter magnitude could reach any value.

Since jitter is considered to be a source of bit errors, and a bus is expected to operate at an error performance level of better than say 1E-12, it would be important to characterize the probability that the jitter will consume a significant portion of the horizontal eye opening margin.

Thus a simple “peak-to-peak” assessment of the jitter magnitude is considered inappropriate.

The above graphs show the jitter histogram of the crossing point of a transmitter eye-diagram and a typical model of the jitter. The random jitter results in the tails of the histogram and should be equivalent on either side. The deterministic jitter components cause the spread between the fitted gaussian curves. Thus it is possible to extract both the random and deterministic components of jitter form the histogram. It is difficult to derive the random “tails” to a 10 E-12 precision.



"Real World" Jitter is Complex

Jitter is complex and is composed of both random and deterministic jitter components. The traditional way to measure jitter is with an eye-diagram using repetitive acquisitions. And using a histogram, you can view the probability distribution function (PDF) of the composite jitter. However, it is practically impossible to see the extreme/worst-case excursions of jitter with an eye-diagram using an oscilloscope.

The random jitter (RJ) component, which is usually measured in terms of an RMS value, is theoretically Gaussian in distribution and is unbounded. This means that timing errors due to random jitter can be theoretically infinite if you wait long enough (infinity) for it to happen. However for practical measurement purposes, you can compute a worst-case peak-to-peak random component based on a bit error ratio (BER). Most people today use a BER of 10^{-12} which translates into a peak-to-peak random jitter of 14.1 x RJ_{rms}.

The other major component of jitter is Deterministic Jitter (DJ). DJ is bounded, measured as a peak-to-peak value, and consists of sub-components including Duty Cycle Distortion (DCD), Inter-Symbol Interference (ISI), and Periodic Jitter (PJ). We will be taking a closer look at these individual deterministic jitter components later in this seminar.

Random and Deterministic Jitter

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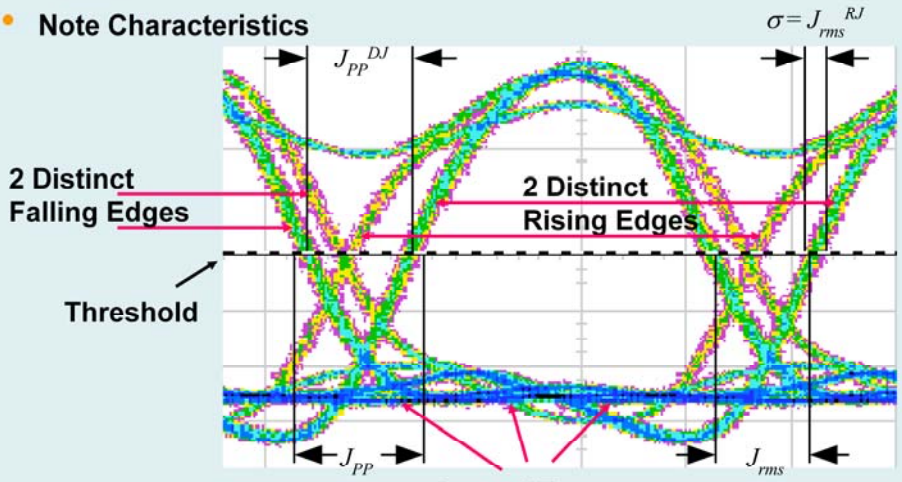
- Waveform Observation
- Pattern
- Note Characteristics



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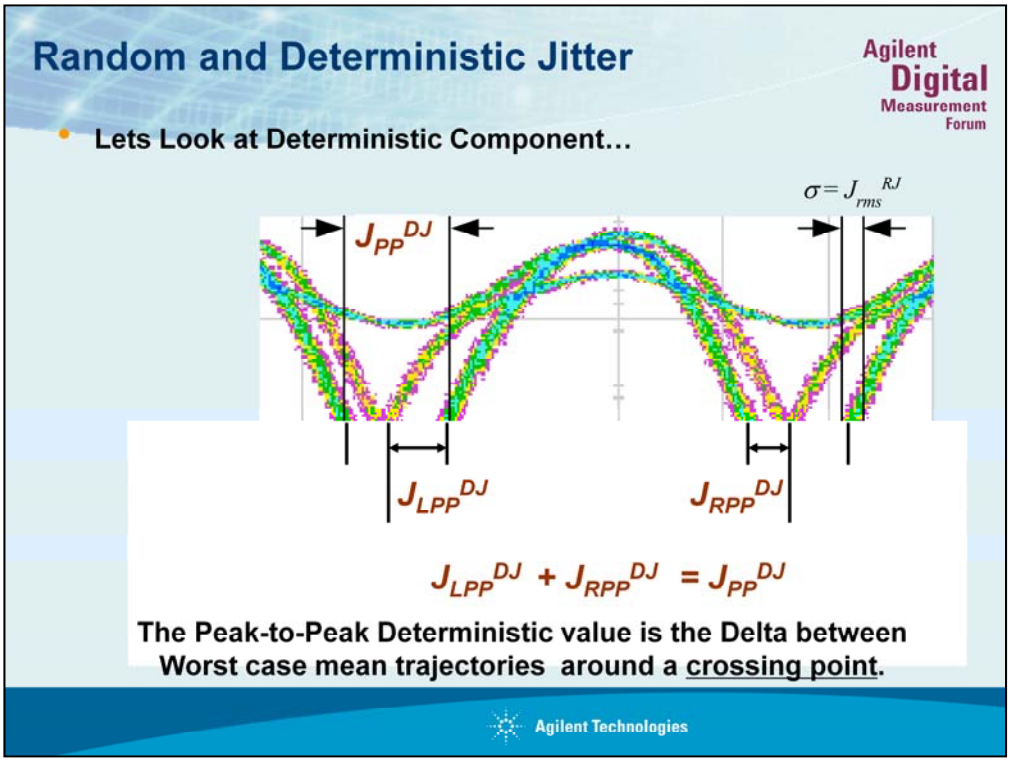
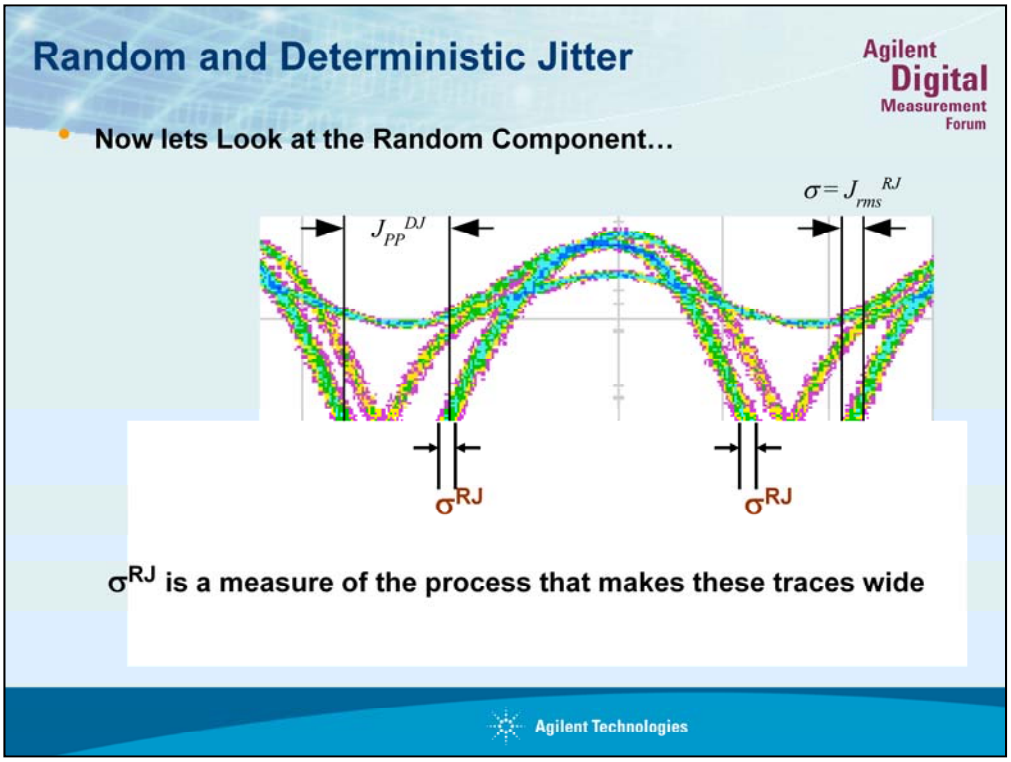
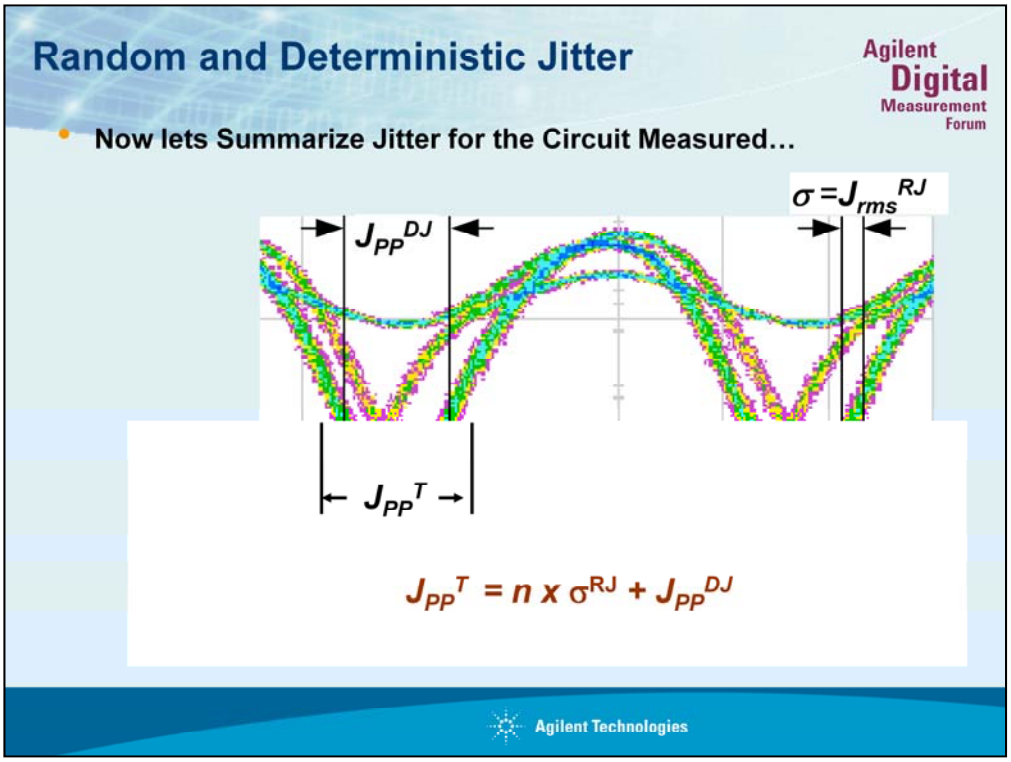


Make note that it is not the difference between the two rising edges but the worst case between a determined crossing point and a rising signal.

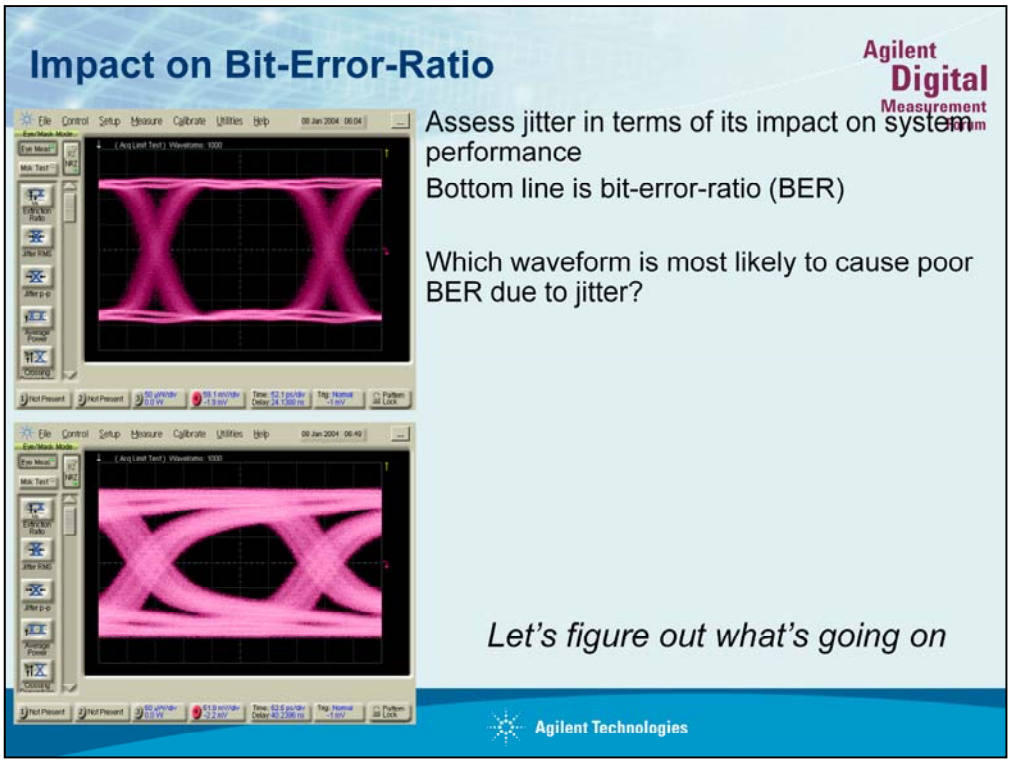
Also for convenience I have used both crossing points---it applies to either



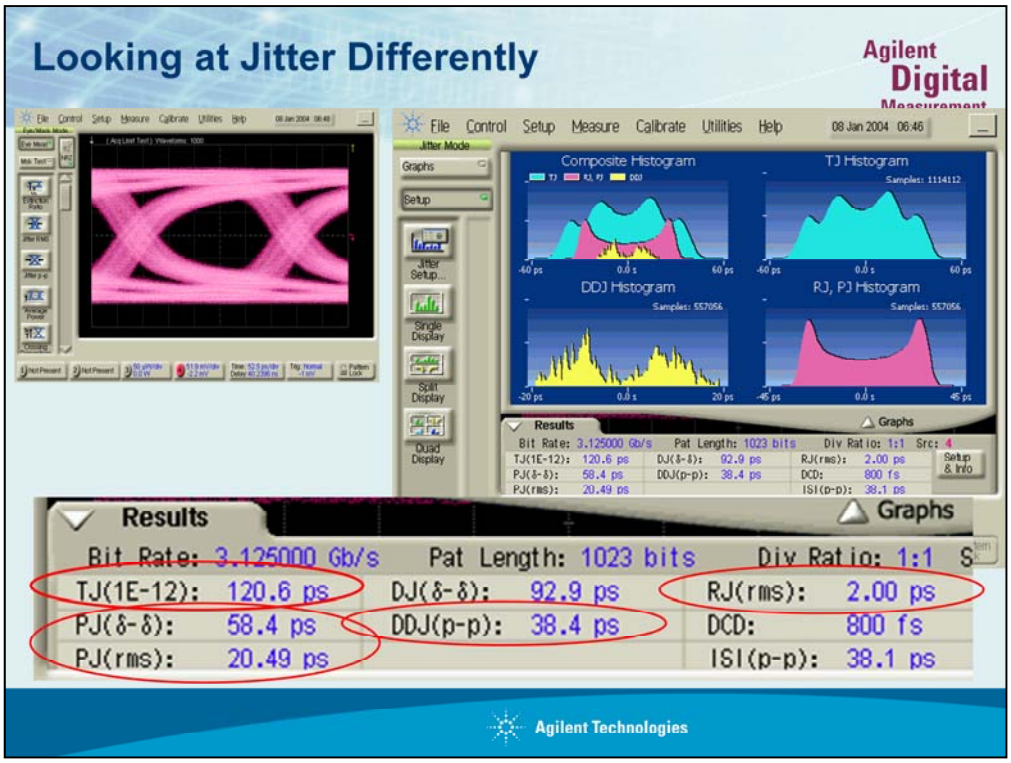
Note the Deterministic bias and need to add process spread



Caution is if long PRBS pattern then mis-estimation of sigma can occur. Can look random….



Why do all this work to separate jitter?


Looking at Jitter Differently
Agilent
Digital
File Control Setup Measure Calibrate Utilities Help
08 Jan 2004 06:46
Jitter Mode
Graphs
Setup
Jitter Setup...
Single Display
Split Display
Quad Display
Composite Histogram
TJ Histogram
DDJ Histogram
RJ, PJ Histogram
Samples: 1114112
Samples: 557056
Results
Graphs
Bit Rate: 3.125000 Gb/s
Pat Length: 1023 bits
Div Ratio: 1:1
TJ(1E-12): 120.6 ps
DJ(δ-δ): 92.9 ps
RJ(rms): 2.00 ps
PJ(δ-δ): 58.4 ps
DDJ(p-p): 38.4 ps
DCD: 800 fs
PJ(rms): 20.49 ps
ISI(p-p): 38.1 ps
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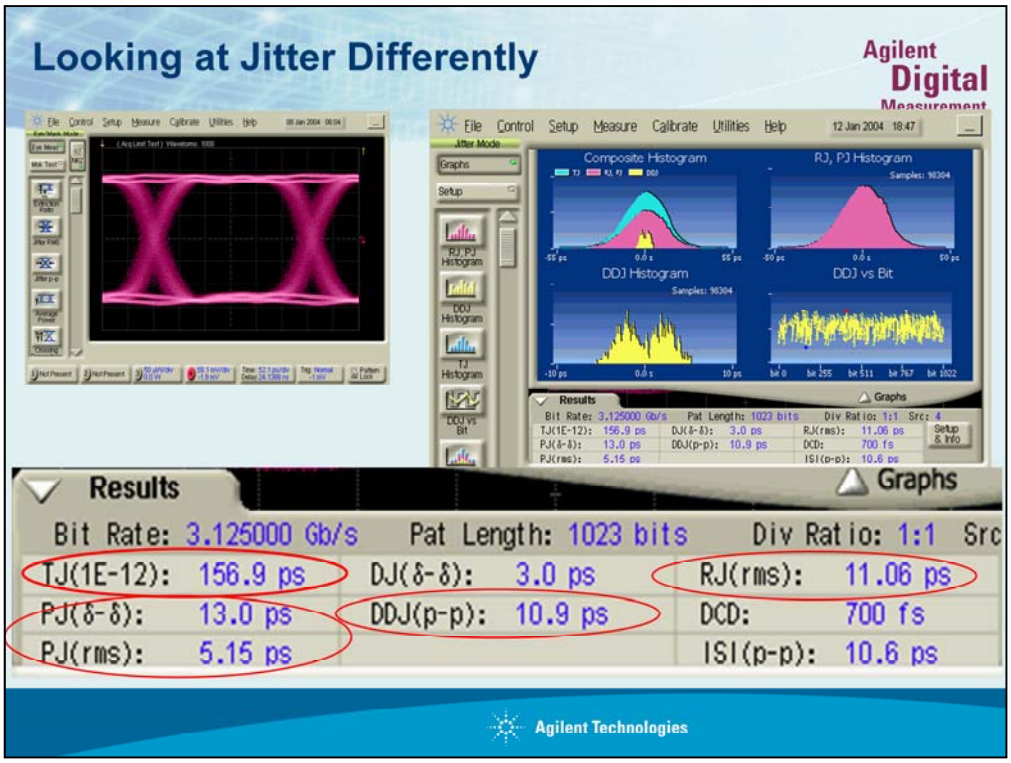
Looking at Jitter Differently
Agilent
Digital
Composite Histogram
RJ, PJ Histogram
DDJ Histogram
DDJ vs Bit
Results
Graphs
Bit Rate: 3.125000 Gb/s
Pat Length: 1023 bits
Div Ratio: 1:1
Src
TJ(1E-12): 156.9 ps
DJ(δ-δ): 3.0 ps
RJ(rms): 11.06 ps
PJ(δ-δ): 13.0 ps
DDJ(p-p): 10.9 ps
DCD: 700 fs
PJ(rms): 5.15 ps
ISI(p-p): 10.6 ps
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The Bathtub Plot

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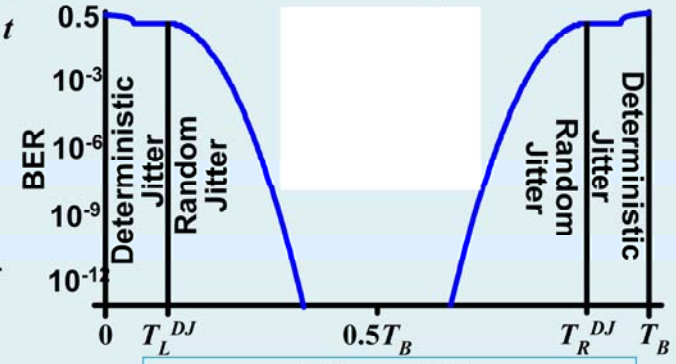
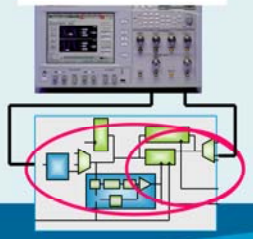
1. Bit Error Rate versus Sampling Point Location
2. Step the sampling point from the center to the crossing points.
3. Measure BER vs. t



Bit Error Rate Tester



$$T_L^{DJ} < t < T_R^{DJ}$$

$$\mathrm{BER}_{RJ}(t) = N_L \,\mathrm{erfc}\left(\frac{t - T_L^{DJ}}{\sqrt{2}\sigma_L}\right) + N_R \,\mathrm{erfc}\left(\frac{t - T_R^{DJ}}{\sqrt{2}\sigma_R}\right)$$

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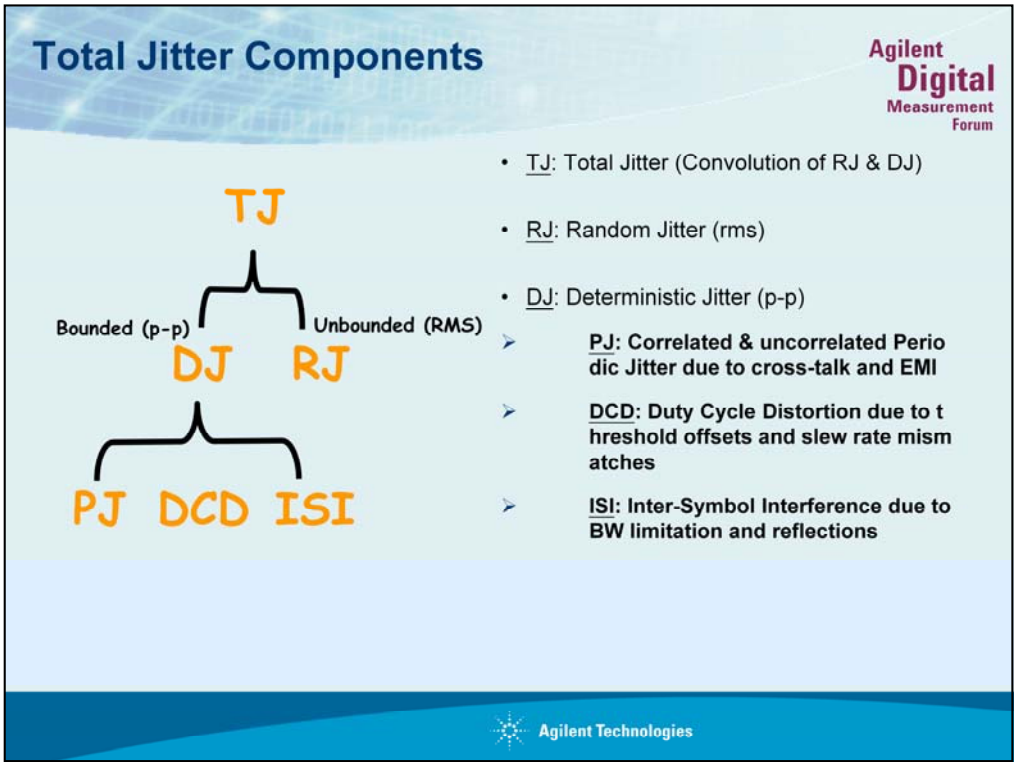


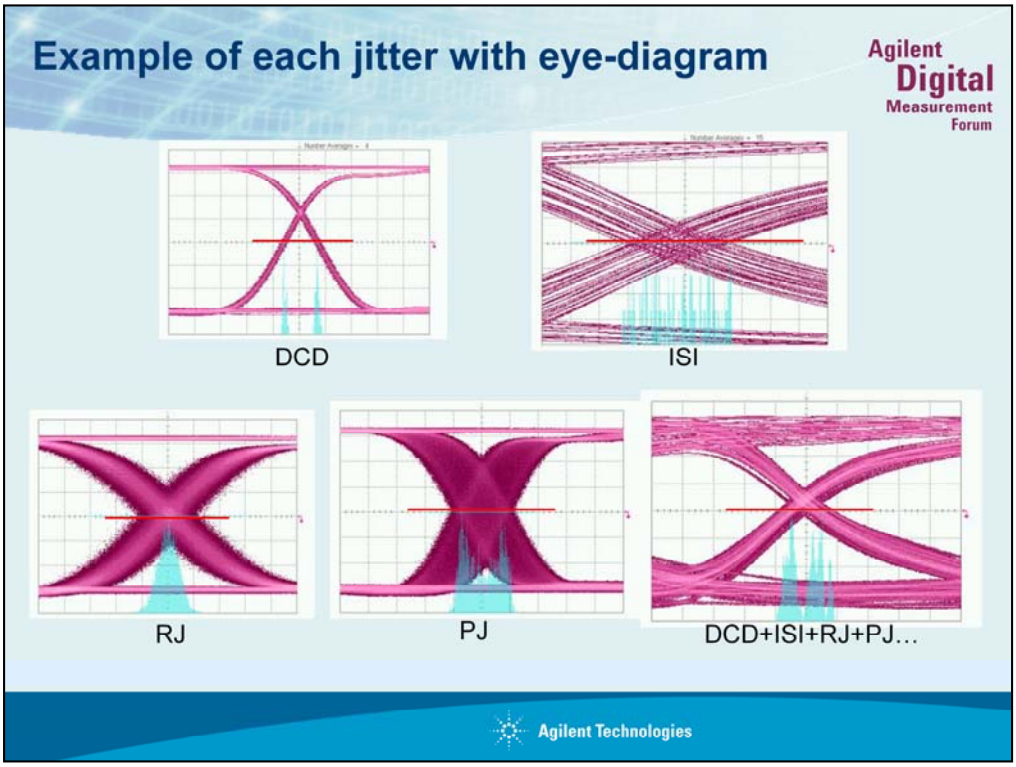
Total Jitter Components

Total jitter in a system is the convolution of Random Jitter (RJ) and Deterministic Jitter (DJ). Random Jitter follows a Gaussian distribution as a first approximation. Theoretically, the RJ component is unbounded based on a true Gaussian distribution. "Unbounded" simply means that the peak-to-peak value of RJ is unlimited. With continuous measurements of random jitter, the peak-to-peak excursions will increase infinitely… given infinite test time. Because of this unbounded characteristic, random jitter is usually stated in terms of an rms value, which is the same as one standard deviation (1σ). However, a peak-to-peak value can be extrapolated relative to a particular bit error ratio (BER) standard. The most common BER used to predict peak-to-peak random jitter is 10^{-12}. For example, for a desired BER of 10^{-12}, $RJ_{p-p} = 14.1 \times RJ_{rms}$.

Deterministic Jitter (DJ) is bounded and is always measured in terms of a peak-to-peak value. It is usually caused by some systematic problem within your system, and is even sometimes called "systematic jitter". DJ can be further broken down into a Periodic Jitter (PJ) component, a Duty Cycle Distortion (DCD) component, and Inter-Symbol Interference (ISI).

Periodic Jitter (PJ) can be either correlated or uncorrelated. In other words, this jitter component may be synchronous to the data signal, and/or may be totally uncorrelated/asynchronous relative to the data signal. For example, a switching power supply within a system may couple into the data signal with the switching frequency having no timing relationship to the data or clock signal. Jitter caused by this condition would be termed uncorrelated periodic jitter. Alternatively, a parallel lane of synchronous serial data may couple into an adjacent lane of serial data. This would be a case of correlated periodic jitter.

Both the DCD and ISI components are always time-correlated to the data signal, and are sometimes called data dependent jitter (DDJ). The jitter or timing errors from these two components are always directly related to the clock or data pattern. A real-time scope can often be the only tool that can track down these types of jitter.



Example of each jitter with eye diagram

RJ is caused by thermal and noise effects. These effects are statistical by nature. So the Random Jitter (RJ) is unbounded and is modeled by a probability density function and is quantified by the rms value of the density function. In most cases the Gaussian distribution is used for the characterization of Random

Jitter. In this case the rms value equals the ‘s’ (sigma) of the Gaussian distribution. There is a fixed relation between ‘s’ (sigma) and the number of events. While a range of 6 sigma already defines a high number of events (99.7%), this is a small number for BER. Typically a BER is required to be as low as 10-12, this needs a range of 14.1 sigma to be included for the total jitter budget

- Duty Cycle Distortion (DCD), which is caused by voltage offsets between differential inputs and differences between transition times within a system. note double delta… but it is not the same as double delta caused by square wave jitter

- Inter-Symbol Interference (ISI), which is caused by the different symbols (long and short bit cycles). note the many trajectories…. The striation is a dead ringer

This can also be explained from Bandwidth limitations which occur from AC coupling (low frequency cut-off) or from high frequency roll-off. However, this is from filters with nonlinear phase characteristic

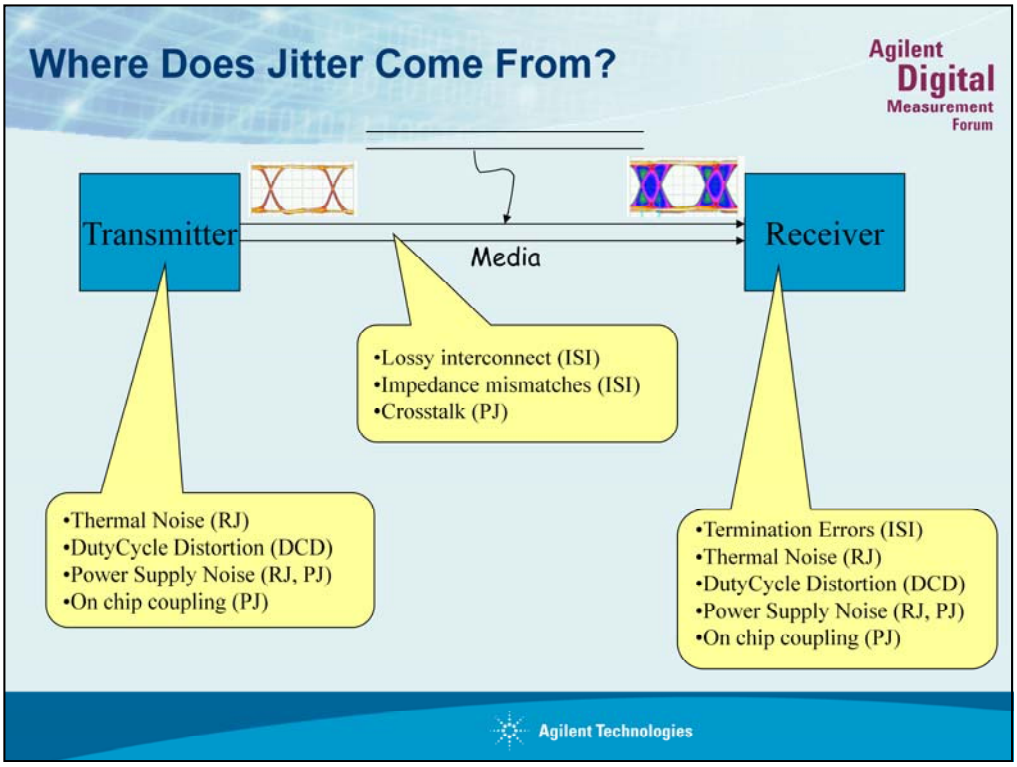
only. Linear filters, such as Bessel filters, do not cause jitter.

DCD and ISI jitter are a function of the pattern. The jitter appears when changing the pattern from a clock-like pattern to real data. PRBS type patterns are good for testing as they contain many variants of frequency component.

Periodic Jitter (PJ), which displaces the timing of rising and falling edges with a periodic pattern (or as the origin of this type of jitter is sinusoidal modulation, it is also called SJ). The above figure shows Sinusoidal (note the u-shaped distribution)

Striation AND High crossing point =>ISI and DCD

In the next layer the Data Dependent Jitter can be separated into:



Where Does Jitter Come From?

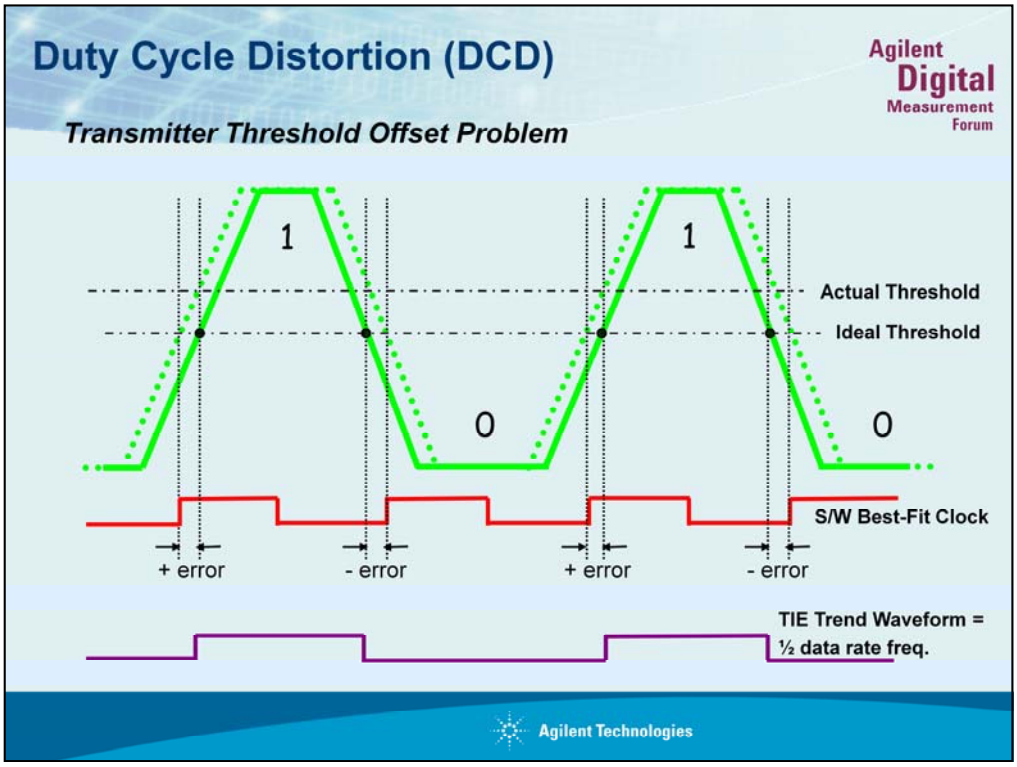
Sources of jitter can be broken down into three primary contributors consisting of the transmitter, the physical media, and the receiver. Your perspective of transmitters and receivers will depend upon your measurement reference point.

Random jitter (Gaussian) can usually be tracked down as a "source" or transmitter problem. Random jitter can often be the most difficult jitter component to track down.. primarily because it is not correlated the data signal. Duty cycle distortion (DCD) is another jitter component that is usually considered a transmitter source problem.

Periodic jitter (PJ), which can be either uncorrelated or correlated, can be viewed as either being generated by a transmitter circuit, or PJ can be coupled into the transmission line. Whether this source of jitter is correlated or uncorrelated, it is ultimately synchronous to something. Therefore, if you are able to trigger on various suspect sources, you may be able to eventually track down the source.

Inter-symbol Interference (ISI) jitter is usually a key component of jitter in high-speed data signals. The primary culprits of ISI jitter include limited bandwidth of the transmitter, limited bandwidth of the data media (transmission line), as well termination problems at the receiver side or impedance discontinuities within the physical media.

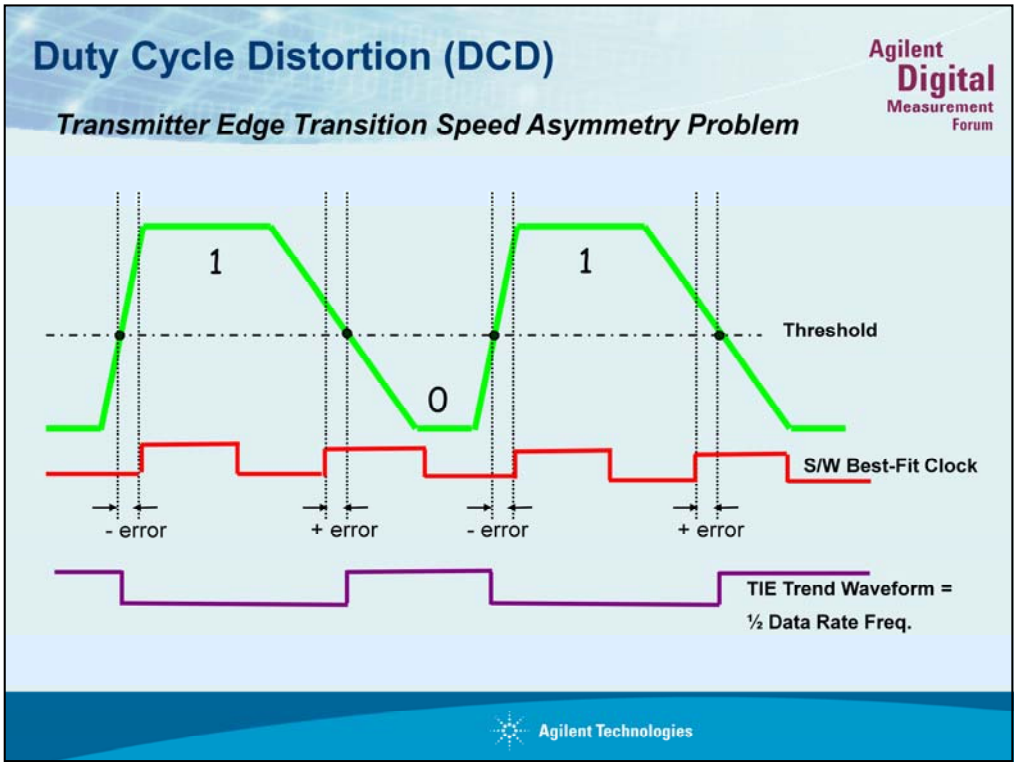
Let's now take a closer look at some of these individual jitter components and how they theoretically look and are revealed with jitter analysis.



Duty Cycle Distortion (DCD)

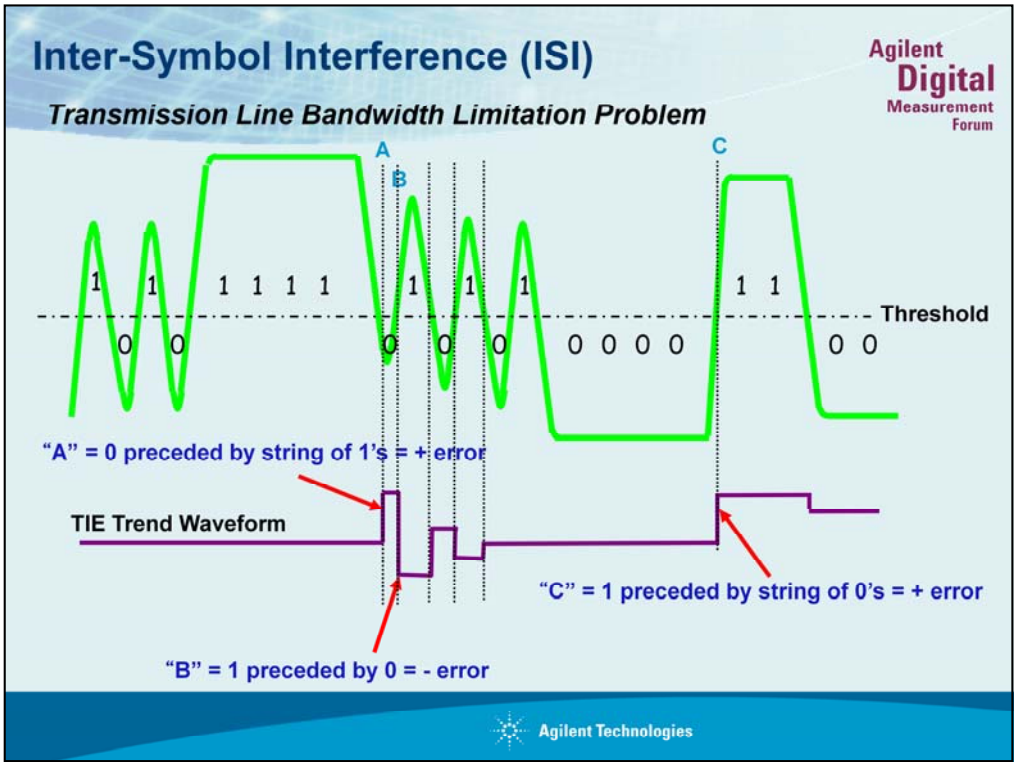
There are two primary causes of DCD jitter which are usually generated within a transmitter. If the data input to a transmitter is theoretically perfect, but if the transmitter sampling threshold is offset from its ideal level, then the output of transmitter will have duty cycle distortion as a function of the slew rate of the data signal. The waveform represented by the dashed green line shows the ideal output of the transmitter with an accurate threshold level at 50%, whereas the solid green waveform represents a distorted output of a transmitter due to a positive shift in the threshold level.

The resultant TIA trend waveform will possess a fundamental frequency equal to ½ the data rate. The polarity of the TIE trend waveform will depend upon whether the threshold shift is positive or negative. With a significant amount of DCD, this component of frequency (1/2 the data rate) can also be viewed on the jitter spectrum view. With no other sources of jitter in the system, the peak-to-peak amplitude of DCD jitter will be constant across the entire data signal. Unfortunately, other sources such as ISI almost always exist making it sometimes difficult to isolate the DCD component. One technique to test for DCD is to stimulate your system/components with a repeating 1-0-1-0… data pattern. This technique will eliminate inter-symbol interference (ISI) jitter and make viewing the DCD within the spectrum display much easier.



Duty Cycle Distortion (DCD)

Another cause of duty cycle distortion can be a mismatch/asymmetry in rising and falling edge speeds. This will result in distortions of duty cycle of the signal as shown in this slide. The polarity/phase of the resultant "trend" waveform will depend upon the asymmetry of the slew rates in rising and falling edges of the signal. With a slower falling edge, the TIE trend waveform will be out-of-phase with the input signal as shown in this graphic. If the rising edge is slower than the falling edge, then the TIE trend waveform will be in-phase with the input signal.



Inter-Symbol Interference (ISI)

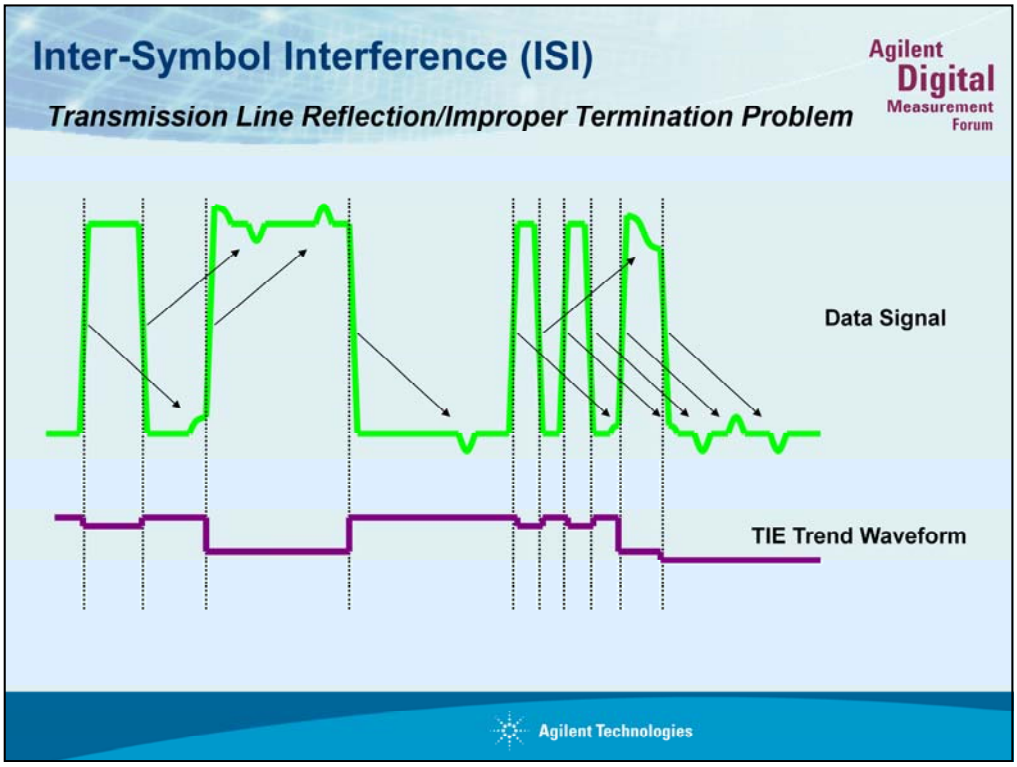
Inter-symbol interference (ISI) jitter is usually a major component of Deterministic Jitter (DJ) for high-speed signals. Causes of this type of timing errors are primarily transmission-line bandwidth limitations and improper termination/impedance discontinuities. Signal transition speeds and levels of signals can effect the timing of data bits that occur later in time.

With a bandwidth limitation problem, signal edge transition speeds of a serial data signal will result in what appears to be modulated peak amplitudes. This is due to slew rate limitations of the signal. Long strings of "1's" or "0's" will eventually reach full high and low steady-state levels, whereas an individual "1" or "0" bit may be never reach full high or level levels before transitioning back to the opposite polarity state because of signal slew rate (bandwidth) limitations.

If the signal reaches a steady-state high level, then the signal will generate a positive timing error when transitioning to a "0" as illustrated at point "A". It requires more time to transition from a full "1" level to the specified threshold level as opposed to transitioning from a partial "1" level". The TIE trend waveform will show a positive peak at this point. Point "C" illustrates another positive timing error point where a long series of "0's" transitions to a "1". Again, the TIE trend waveform will show another positive peak of timing error at this point.

If the signal is defined as a "0" for just a single data bit, and then transitions back to a "1", it will have less distance to travel to reach the specified threshold level, and hence will generate a negative timing error as illustrated at point "B".

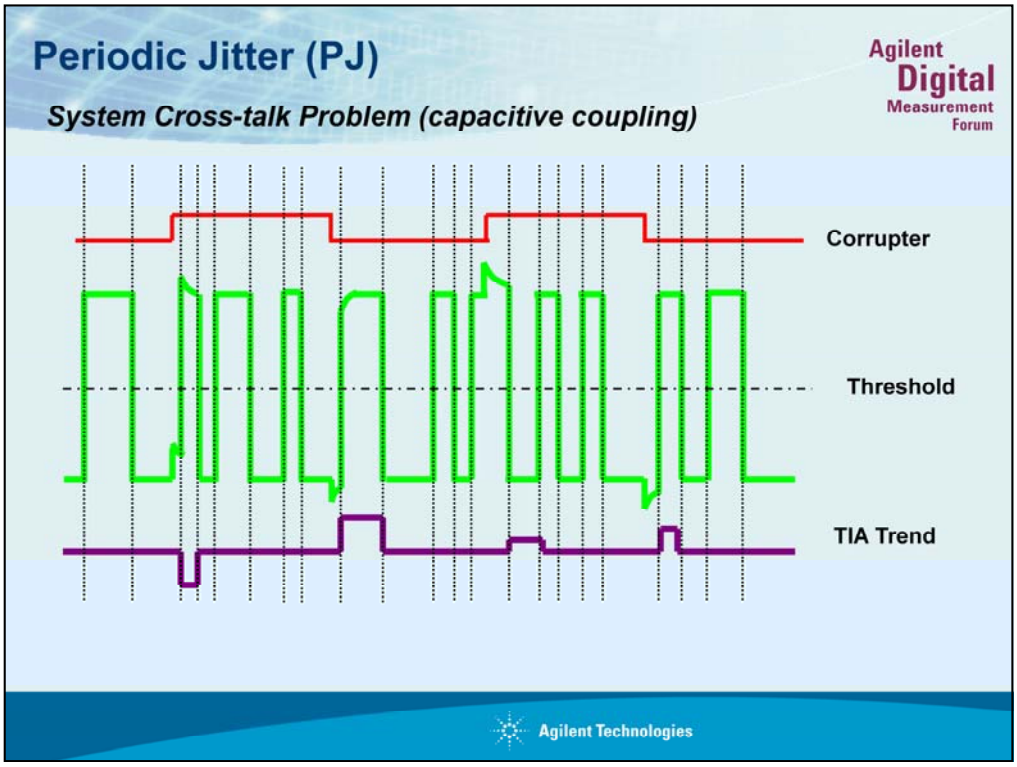
If it is possible to eliminate other jitter components including RJ, then the shape of the TIE trend waveform will have a unique "signature" based on the serial data pattern. We will discuss some measurement techniques to achieve this situation later in this seminar.



Inter-Symbol Interference (ISI)

Another contributor to ISI jitter can be due to reflections. This particular cause of ISI jitter can be very difficult to interpret. With high-speed data, a signal reflection due to termination problems from one bit may not show up on the data signal until a few bits later in the transmission. In this graphic, each of the arrows shows which bit of data caused a reflection distortion on a later data bit. The physical distance between the impedance discontinuity in the media causing the reflection to the measurement point will determine the amount delay between the data bit and the distortion. And this time/distance will be fixed. If the reflection/signal distortion occurs at or near a data transition edge, then a timing error (jitter) will be the result.

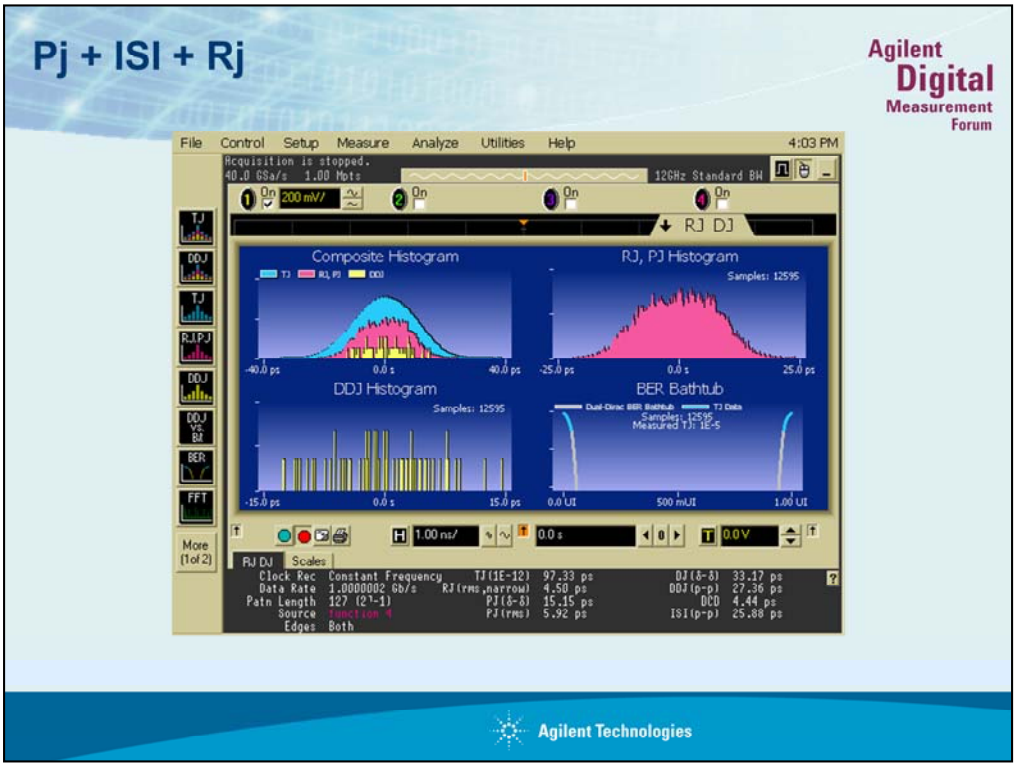
As with bandwidth limitation problems, reflections will in effect modulate the amplitude of the data signal. And if the "high" and "low" levels of the signal are modulated, then the signal transition time errors will vary due to longer or shorter transition times from initial levels to the threshold level. This will directly result in timing errors or jitter. The slew rate of the signal, and hence the bandwidth of the transmission line will have a direct effect on the magnitude of timing errors due to reflections.



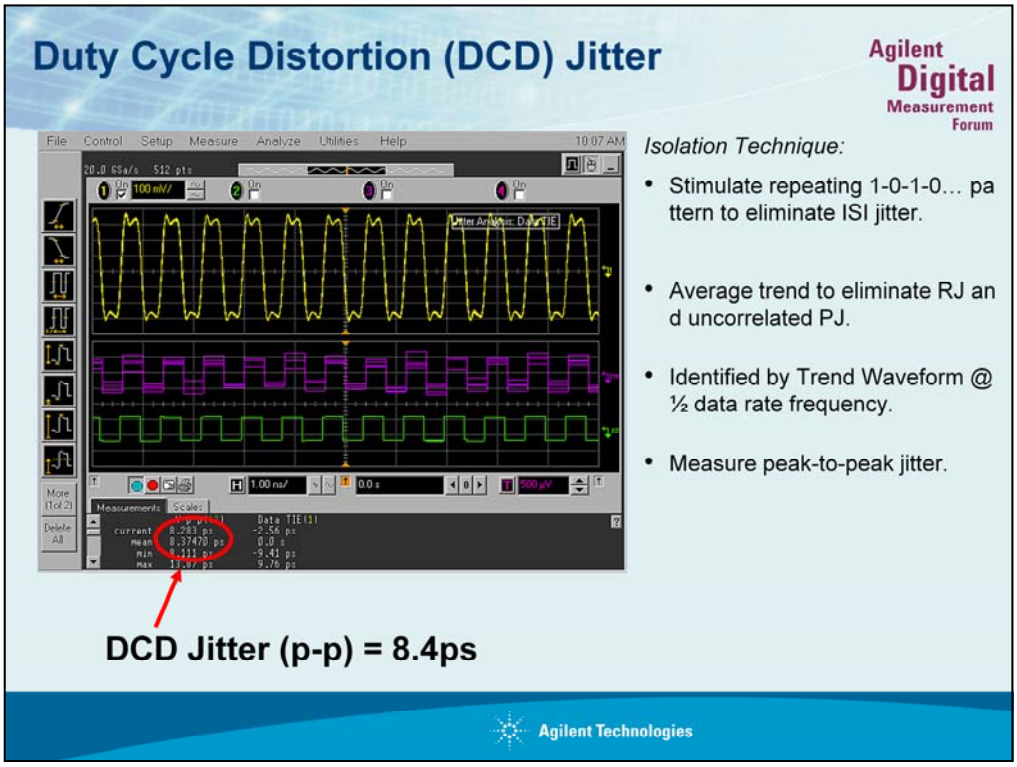
Periodic Jitter (PJ)

Periodic Jitter (PJ) is usually the result of another signal coupling into the data signal. The "currupter" signal may be correlated or uncorrelated to the data signal. In this slide we show an example of an uncorrelated signal capacitively coupling into the serial data signal under test. If the coupling occurs near a data edge, then the initial amplitude of the pulse just prior to the transition will shift in amplitude, thereby causing a timing error when transitioning to the next threshold level crossing. Assuming that edge speeds are not infinitely fast, then the shift in initial amplitude along with the limited slew rate of the signal will result in a timing error.

This particular error component (PJ) will sometimes show up as a particular frequency component on the jitter "spectrum" display if it is uncorrelated to the data signal. Depending upon the RC time constant, it may be difficult to see and could be "buried" in the base-band noise of the spectrum (FFT) display. Another technique to view this frequency component of coupling is to set up an FFT math function on the data signal. If this periodic jitter (PJ) component was resistively coupled, as opposed to capacitively coupled, it would more clearly be displayed on both the jitter spectrum display and the signal FFT display.



Function 4 now includes Pj, R, and ISI. Compare Pj to the previous 2 measurements. Compare ISI and Rj to slide 16.



Duty Cycle Distortion (DCD) Jitter

The best way to isolate DCD jitter is to stimulate the input of a transmitter circuit with a repeating 1-0-1-0… pattern. Using this simple repeating serial pattern, most of the ISI will be eliminated. Next, set up the oscilloscope to perform jitter analysis of time interval error (TIE) on both the rising and falling edges relative to a best-fit software generated clock. The primary "view" to measure the DCD is the jitter "trend" waveform. At this point, the trend waveform (purple trace) will show a combination of DCD plus random jitter (RJ).

Using the scope's waveform math functions, select to average the jitter trend waveform. With a synchronous trigger, averaging the jitter trend waveform will eliminate both random jitter (RJ) as well as any uncorrelated periodic jitter (PJ). The resultant averaged jitter trend waveform (green trace) will consist almost entirely of duty cycle distortion (DCD). You can then select to automatically measure the peak-to-peak jitter of the jitter trend waveform. The polarity of the jitter waveform relative to the data signal will depend upon shifts in transmitter threshold levels and/or asymmetry in edge speeds. With proper isolation testing techniques as outlined here, the peak-to-peak amplitude of the TIE trend waveform will show up as a constant level of error across the entire signal.

If the peak-to-peak amplitude of duty cycle distortion is excessive, you could then characterize edge speeds and pulse widths of the transmitter output signal using the parametric capabilities of the real-time jitter analysis.

You can also view this component of jitter using the jitter spectrum view. The frequency of this component will be ½ the signal data rate.

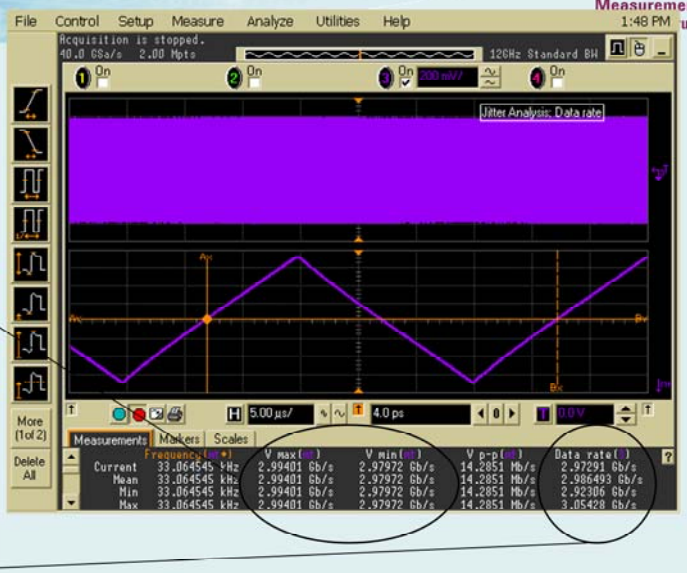
SSC – SATA

Agilent Digital Measurement

Standard Vmax and Vmin measurement quickly measure the Max and Min Data Rate when applied to the filtered measurement trend, per the SATA II specification.

One setup, precise results and statistical trends over many acquisitions.

Observe the unfiltered raw data rate using the standard Data Rate measurement for worst-case conditions on the transmitter.



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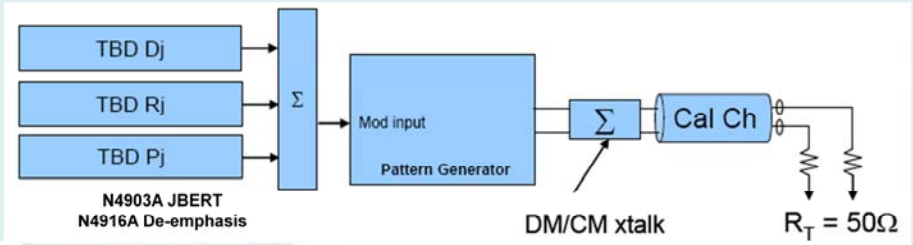
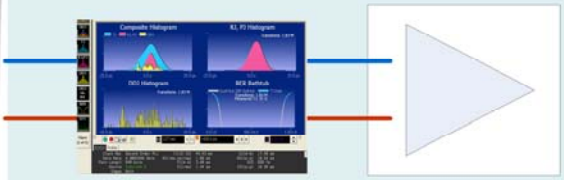
Rx Test Solution for USB3.0 SuperSpeed - Receiver Jitter tolerance

Agilent Digital Measurement Forum





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Normative Receiver Tolerance Compliance Test Requirements

Agilent Digital Measurement Forum

Table 6-19. Input Jitter Requirements for Rx Tolerance Testing

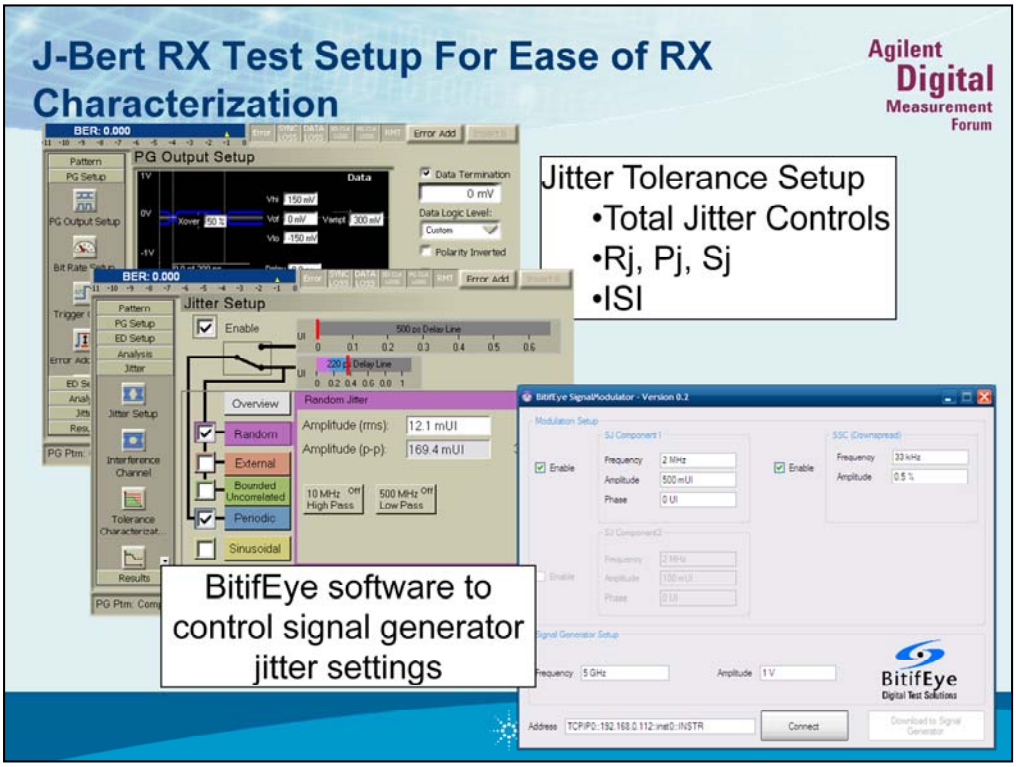
Symbol	Parameter	Value	Units	Notes
f1	Tolerance corner	4.9	MHz	
J_{Rj}	Random Jitter	0.0121	UI rms	1
$J_{Rj\_p\text{-}p}$	Random Jitter peak- peak at 10^{-12}	0.17	UI p-p	1,4
J_{Pj_500kHZ}	Sinusoidal Jitter	2	UI p-p	1,2,3
J_{Pj_1Mhz}	Sinusoidal Jitter	1	UI p-p	1,2,3
J_{Pj_2MHz}	Sinusoidal Jitter	0.5	UI p-p	1,2,3
J_{Pj_f1}	Sinusoidal Jitter	0.2	UI p-p	1,2,3
J_{Pj_50MHz}	Sinusoidal Jitter	0.2	UI p-p	1,2,3
V_full_swing	Transition bit differential voltage swing	0.75	V p-p	1
V_EQ_level	Non transition bit voltage (equalization)	-3	dB	1

Notes:

1. All parameters measured at TP1. The test point is shown in Figure 6-18.
2. Due to time limitations at compliance testing, only a subset of frequencies can be tested. However, the Rx is required to tolerate Pj at all frequencies between the compliance test points.
3. During the Rx tolerance test, SSC is generated by test equipment and present at all times. Each J_{Pj} source is then added and tested to the specification limit one at a time.
4. Random jitter is also present during the Rx tolerance test, though it is not shown in Figure 6-19.

J-Bert RX Test Setup For Ease of RX Characterization

Agilent Digital Measurement Forum



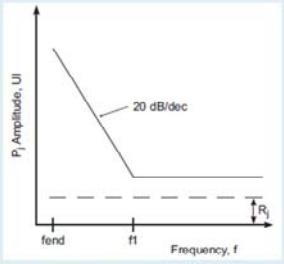
SuperSpeed Receiver Tests

CTS 0.5 Test Descriptions and Requirements

Agilent Digital Measurement Forum

Normative Receiver Tolerance Compliance Test

- TD.1.3: Loopback BERT Test
- TD.1.4: Receiver Jitter Tolerance Test



Jitter Tolerance Curve

Symbol	Parameter	Value	Units
f1	Tolerance corner	4.9	MHz
J_{Rj}	Random Jitter	0.0121	UI rms
J_{Rj_p-p}	Random Jitter peak- peak at 10^{-12}	0.17	UI p-p
J_{Pj_500kHz}	Sinusoidal Jitter	2	UI p-p
J_{Pj_1MHz}	Sinusoidal Jitter	1	UI p-p
J_{Pj_2MHz}	Sinusoidal Jitter	0.5	UI p-p
J_{Pj_f1}	Sinusoidal Jitter	0.2	UI p-p
J_{Pj_50MHz}	Sinusoidal Jitter	0.2	UI p-p
V_full_swing	Transition bit differential voltage swing	0.75	V p-p
V_EQ_level	Non transition bit voltage (equalization)	-3	dB

Jitter Requirements

- Periodic (sinusoidal) jitter frequencies 500 KHZ – 50 MHz

Additional requirements

- Polling Loopback substate
- 5,000 ppm SSC

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In the past, USB receiver tests were only informative. The Compliance Test Specification 0.5 now lists two mandatory receiver tests, the Loopback BERT and Receiver Jitter Tolerance Tests.

A jitter tolerance limit curve is given within the 500 KHz to 50 MHz jitter range. SSC is required.