Microelectronics Journal 44 (2013) 185–189

Contents lists available at SciVerse ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

A 30-V transmitter front-end IC for ultrasound medical imaging applications

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ARTICLE INFO

Article history:
Received 29 June 2012
Received in revised form
7 January 2013
Accepted 9 January 2013
Available online 4 February 2013

Keywords:
Ultrasound
High-voltage front-end
Output driver
Level-shifter

ABSTRACT

A transmitter front-end IC for ultrasound medical imaging applications is implemented using 30-V 0.18-μm Bipolar/CMOS/DMOS process. The proposed ultrasound transmitter front-end, consisting of voltage level-shifters and an output driver, achieves high integration and maintains good reliability while generating a 33 ns output pulse signal in order to drive a large capacitive load, which represents the equivalent capacitance of the capacitive micromachined ultrasound transducer device. The proposed high-frequency transmitter achieves a delay of less than 20 ns at 30 Vp–p output voltage while successfully driving a capacitive load of 44 pF and consumes an area of 0.34 mm^2.

1. Introduction

During the last decade, ultrasound medical imaging systems utilizing capacitive micromachined ultrasound transducer (CMUT) has received much attention [1] from the medical imaging community due to its safe characteristic to the human body in comparison to other imaging modalities, its ease of fabrication using CMOS compatible process techniques, superior frequency characteristics, and integration capability with the interface integrated circuits (IC) in comparison to its piezoelectric counterpart [2] which has dominated as the ultrasound transducer choice in the past.

In order to generate a large acoustic pressure from the transducer surface during transmission, the CMUT device is usually biased at a high DC voltage and driven with a high voltage (HV) pulse signal. Using a high operating frequency and utilizing multiple elements in the 2-dimensional transducer array improves the image resolution, image depth, sensitivity, and signal-to-noise ratio (SNR) of the overall system. Each transducer element must be closely coupled to its dedicated interface analog front-end IC in order to minimize the effect of parasitic components which degrades the sensitivity of the transducer [3,4]. To satisfy these requirements, a highly-integrated transmitter is needed to drive the transducer with a narrow HV pulse to generate a large acoustic signal in the transmit path. In addition, high robustness must be guaranteed so that device reliability issues such as oxide or junction breakdown do not occur during operation.

In this paper, we demonstrate a single-channel highly integrated high-frequency transmitter front-end for ultrasound medical imaging applications using 30-V 0.18-μm Bipolar/CMOS/DMOS process. The implemented front-end IC consists of two voltage level-shifters and an output driver capable of driving a large capacitive load up to 30 Vp–p with a pulse width of 33 ns. The design methodology of the front-end is described in detail, while discussing the reliability issues of using HV circuits with regular supply voltage circuits in a single IC. Section 2 discusses the overall architecture of the ultrasound transceiver interface IC while Section 3 describes the circuit design details. Section 4 shows the experimental results followed by the conclusions in Section 5.

2. System architecture

The block diagram of a general ultrasound transceiver interface IC is illustrated in Fig. 1. The transducer elements interface with the multi-channel analog front-end, which consist of HV pulsers, low-noise preamplifiers, and HV switches to protect the low-voltage (LV) circuits for isolation. For the transmitter side, the HV pulsers are driven by LV trigger pulses generated by the digital signal processor (DSP) with controlled delays for beamforming [5]. For the receiver chain, time-to-gain compensation amplifiers (TGC) [6] follow the preamplifiers to control the receiver gain according to the depth of the received echo signal. The analog-to-digital converters (ADC) follow the TGC to digitize the signals and further signal processing is performed by the DSP. Finally, the

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http://dx.doi.org/10.1016/j.mejo.2013.01.009

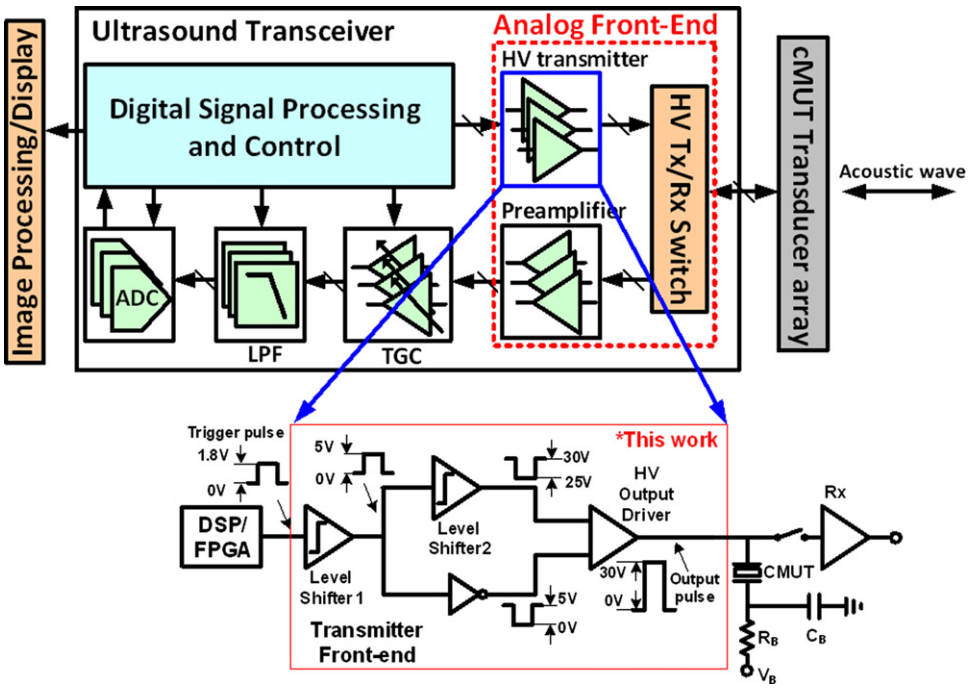

Fig. 1. Overall block diagram of the ultrasound imaging system (top) and the block diagram of HV transmitter front-end IC (bottom).

targeted ultrasound image is constructed from the pulse-echo-signal information.

The bottom part of Fig. 1 shows the simplified overall block diagram of the transmitter front-end. The purpose of the transmitter is to generate a pulse signal to excite the capacitive transducer load so that sufficient pressure can be generated from the transducer to propagate through the acoustic medium to reach the targeted distance for imaging. The pulse width, period, and the required amount of generated acoustic pressure which relates to the maximum voltage of the output pulse signal are decided in the system level depending on the specific medical imaging application as well as the device characteristics of the following transducer. This high-voltage signal generation in the transmitter should be done without compromising the reliability of the operating transistors in the circuit. In this work, double-diffused MOS (DMOS) transistors are utilized for the output driver and parts in the level-shifter in order to sustain up to 30 V of drain-to-source voltage. As the DMOS devices consume much die area in comparison to CMOS devices with larger parasitic capacitance and high dynamic power, nominal CMOS transistors are utilized as much as possible in the design for higher integration purpose while maintaining the robustness during its operation. The external DSP generated 1.8 Vp–p trigger signals are applied to the first voltage level-shifter and it is converted to swing between 0 and 5 V at the output. Then the resulting 5 Vp–p signal is divided into two different paths. The upper path contains a second level-shifter which converts the signal to swing between 25 V and 30 V. This is used to drive the gate of PDMOS transistor of the output driver. The lower path, on the other hand, goes through inverter-based buffers to drive the gate of NDMOS transistor of the output driver. The output driver is followed by the CMUT element where the CMUT is driven with a 30 Vp–p pulse.

The other terminal of the CMUT device is connected to a DC bias voltage through a large bias resistor R_B, and a bypass AC capacitor C_B, for biasing the CMUT near the pull-in voltage for high transmit efficiency. The output driver and CMUT interface is also connected to the receiver analog front-end, which consists of a HV isolation switch and a low-noise preamplifier. Some of the transmitted pressure signal is reflected back due to the difference in the acoustic impedance between tissue layers [4], and is received by the CMUT. This returning wave causes a certain change in the CMUT capacitance, which results in the generation of current. This converted weak electrical signal is amplified by the preamplifier so that it can be processed ultimately in the following stages for image construction. This work includes the HV transmitter part of the overall ultrasound analog transceiver front-end.

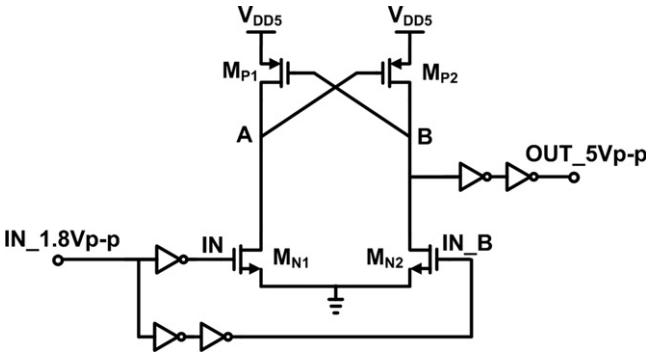

Fig. 2. Schematic of 1.8-to-5V level-shifter.

3. Circuit design

3.1. 1.8-to-5 V level-shifter

The schematic diagram of 1.8-to-5 V level-shifter is shown in Fig. 2. The circuit consists of cross-coupled PMOS transistors and two NMOS transistors driven by two complementary input signals noted as IN and INB. When the input voltages IN and INB are low and high, then M_{N1} and M_{N2} are OFF and ON, respectively. Then M_{N2} pulls down node B and M_{P1} is turned

ON, which will pull up node A. This will turn OFF M_{P2} and OUT_5 Vp–p will pull down to GND. On the other hand, when the input voltages IN and INB are high and low, then M_{N1} and M_{N2} are ON and OFF, respectively. Then M_{N1} pulls down node A and M_{P2} is turned ON, which will pull up node B resulting in OUT_5 Vp–p to be at 5 V.

3.2. 5-to-25 V level-shifter and 30 V output driver

The schematic of the proposed second level-shifter and output driver stage is shown in Fig. 3. As the DMOS transistors can only sustain 5 V gate-to-source voltage, a second level-shifter is needed to produce a pulse that swings between 25 V and 30 V to drive the PDMOS of the output driver. In order to prevent junction breakdown of the regular MOS transistors during high voltage operation, DMOS transistors are used in both the level-shifter and output driver so that reliability in the circuit operation is maintained [7]. However, the disadvantage of these DMOS transistors is the added process cost, increased layout size and parasitic capacitance. In addition, the device on-resistance of these transistors is larger than regular CMOS transistors and the sizing has to be sufficiently large in order to drive the following CMUT element to a high voltage at megahertz frequencies. Therefore, for the proposed work, standard CMOS transistors are used wherever possible in order to minimize the overall area of the transmitter front-end.

The output driver stage consists of DMOS transistors M_{HVP1} and M_{HVN1}, in which the gates are driven by two signals created from the low/mid-voltage triggering logic. The gate of M_{HVN1} is controlled by Pulse_trig3, which swings between ground and 5 V. On the other hand, the control signal at node B driving the gate of M_{HVP1} needs a level shift to operate between V_{DD30} (30 V) and V_{DD30}-5 V, which is made possible by the transistors $M_{HVN2,3}$ and

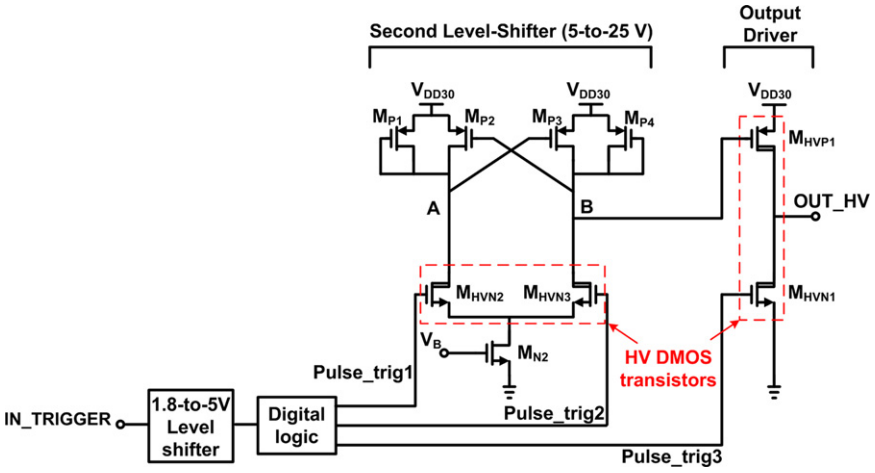

Fig. 3. Schematic of 5-to-25V level-shifter and HV output driver.

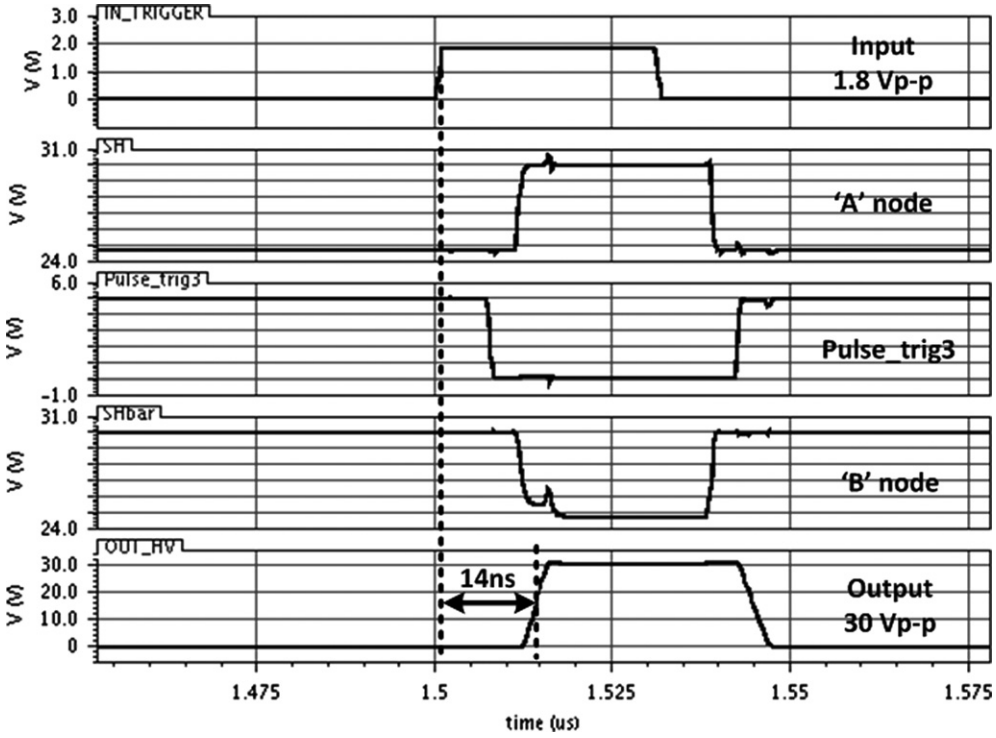

Fig. 4. Transient simulation plot of input trigger signal versus output high voltage pulse.

$M_{P1\text{-}5}$. 5 Vp–p trigger signals go through a digital logic block consisting of delay cells to create non-overlapping trigger signals Pulse_trig1 and Pulse_trig2. Pulse_trig1 is used to control the unipolar HV pulse applied across the transducer element, while Pulse_trig2 is inverted version of Pulse_trig1 which is used to completely turn OFF M_{HVP1} during the pulse repetition time. These two signals are used to drive the gate of M_{HVN2} and M_{HVN3}, which will have the A and B nodes to swing between 25 and 30 V due to the diode connected transistors M_{P1} and M_{P4} connected in parallel to the M_{P2} and M_{P3} transistors. The signal at B node will then switch M_{HVP1} ON and OFF to apply the 30 V to the output which excites the CMUT. Pulse_trig3 is a pulse-width delayed version of Pulse_trig1. These three pulses are generated from the input trigger source signal to prevent M_{HVP1} and M_{HVN1} of the output driver from turning on at the same time during the signal transition of the input pulse. This way, a large dynamic current flow between the supply and ground is avoided.

As the pulser has to drive a large transducer capacitance in short pulse duration, the correct sizing of the output driver stage transistors is critical. The sizes cannot be designed too large as the parasitic capacitances associated with the transistors M_{HVP1} and M_{HVN1} as well as the interconnect lines can be significant. Those large capacitances can reduce the output signal amplitude and degrade the element sensitivity. In addition, the amount of dynamic current flow inside the chip should be considered. Therefore, the sizes of M_{HVP1} and M_{HVN1} are optimized through careful simulation so that the generated pulse can have a steep rise and fall times to better excite on the ultrasound transducer elements while minimizing the high dynamic current through the driver transistors.

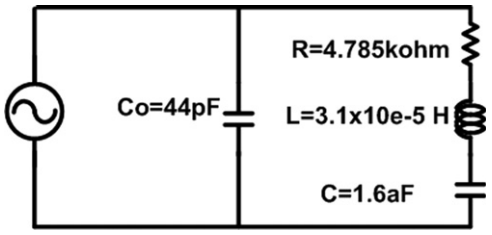

Fig. 5. Equivalent electrical model of the CMUT.

Fig. 4 shows the transient simulation plot using Cadence in which a 28.5 ns pulse width input trigger signal at 1.8 V is applied to the first level-shifter input and the output of the driver is monitored. The 30 Vp–p output pulse is generated after a small delay. All the internal nodes meet the process limits for all simulation corners. The load condition at the output driver in this simulation is an equivalent electrical CMUT model shown in Fig. 5, mainly consisting of a large parallel capacitor and a resistor [3].

A special attention is given in the layout stage to isolate the HV operating circuits and the regular voltage parts. Also, multiple wide top metal paths stacked from metal-1 to metal-6 layers are used to route the HV supply, HV ground, and output nodes from the core to the pads to minimize the parasitic resistance and support high dynamic current through this path.

4. Measurement results

The HV ultrasound transmitter is fabricated in Global Foundry 0.18-μm Bipolar/CMOS/DMOS (BCD) process which supports up to 30 V of drain-to-source/drain-to-bulk voltage and 5 V gate-to-source voltage for DMOS devices. The chip, shown in Fig. 6, consists of the proposed transmitter front-end IC with wide metal routing paths to the bonding pads in order to support large

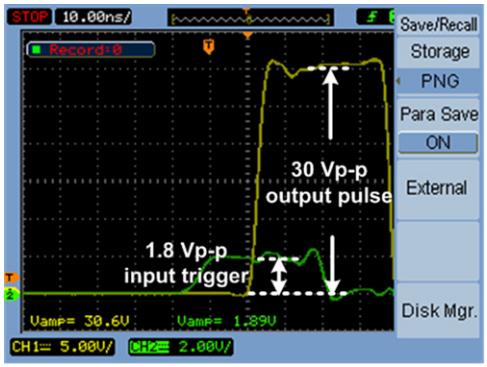

Fig. 7. Measured input trigger pulse versus HV output pulse.

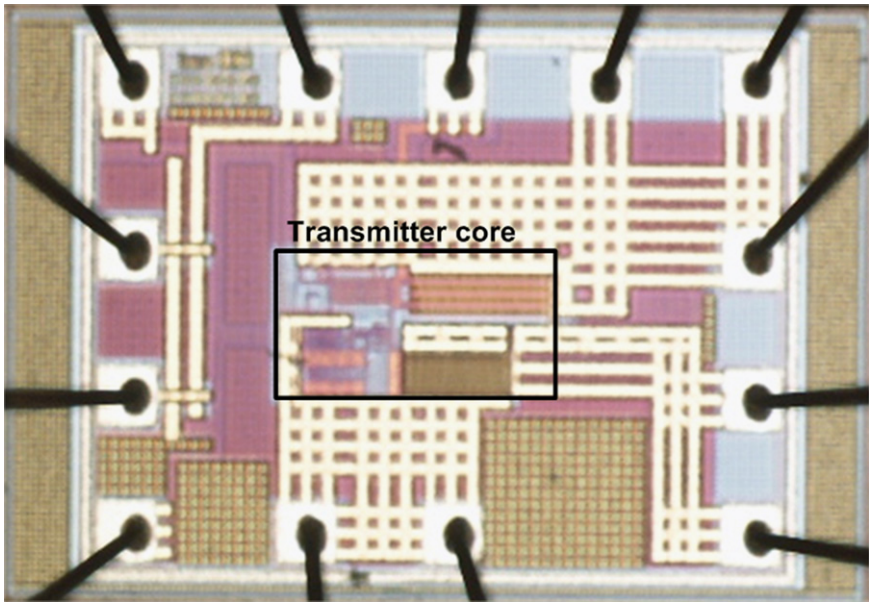

Fig. 6. Chip microphotograph of the transmitter IC.

Table 1
Performance summary of implemented transmitter front-end IC.

Parameter	This work	[7]
Blocks	Two voltage level-shifters +HV output driver	DC–DC, level-shifter, HV output driver
Transmitter input/Max. output pulse voltage	1.8 Vp–p/30 Vp–p unipolar pulse	5 Vp–p/59 Vp–p unipolar pulse
Transmitter current consumption	30 mA dynamic/28 mA static	200 mA dynamic
Transmitter input trigger pulse width	33 ns	5 MHz operation freq.
Input-–output delay	<20 ns	—
Rise/Fall time	<5 ns	69/58 ns
Output loading capacitance	40 pF	20 pF
Chip area	0.34^2	4.25 mm^2
Process technology	30-V 0.18 μm BCDlite	0.8 μm CMOS/DMOS

dynamic current during ON–OFF transitions. The active chip area of the proposed transmitter is 480 μm $\times$ 700 μm. Fig. 7 shows the measured capture of the 1.8 Vp–p input trigger pulse versus 30 Vp–p output pulse signal with a pulse width of 33 ns driving a 40 pF capacitive load at the output, with over 12 pF capacitance of the measurement probes. The output signal rise and fall times are measured to be less than 5 ns, while the input-output delay time is less than 20 ns. The external input trigger signal is provided by an arbitrary waveform generator.

Table 1 summarizes the performance details of the implemented transmitter front-end IC and compares with previous work.

5. Conclusions

A 30-V ultrasound transmitter IC for medical imaging applications is implemented using 0.18-μm BCD process. The transmitter front-end, which includes the proposed output driver and level-shifter, achieves up to 30 Vp–p output pulse signal while driving a large output capacitance with robust reliability while utilizing both CMOS and DMOS transistors for high integration and high reliability. A successful demonstration is done using the proposed ultrasound transmitter IC for high-voltage pulse generation.

Acknowledgement

This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science, and Technology (grant number 2012R1A1A1040958).

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