SpectreRF Workshop

Mixer Design Using SpectreRF

MMSIM 12.1

September 2012

Contents

Mixer Design Using SpectreRF

Note: The procedures described in this workshop are deliberately broad and generic. Your specific design might require procedures that are slightly different from those described here.

Purpose

This workshop describes how to use SpectreRF in the Virtuoso Analog Design Environment to measure parameters that are important in verifying mixers.

Audience

Users of SpectreRF in the Virtuoso Analog Design Environment.

Overview

This application note describes a basic set of the most useful measurements for mixers.

Introduction to Mixers

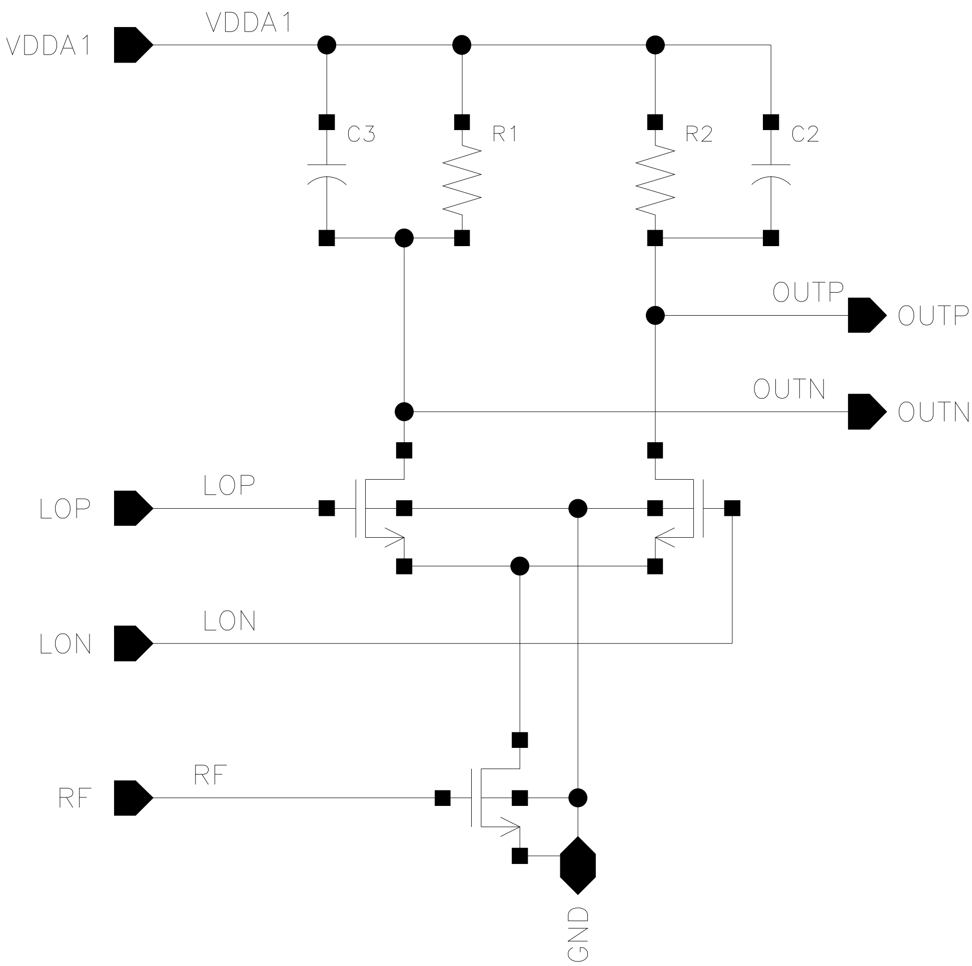
Mixers are key components in both receivers and transmitters. Mixers translate signals from one frequency band to another. The output of the mixer consists of multiple images of the mixer's input signal where each image is shifted up or down by multiples of the local oscillator (LO) frequency. The most important mixer output signals are usually the signals translated up and down by LO frequency.

In an ideal situation, the mixer is an exact replica of the input signal. In reality, mixer output is distorted by non-linearity in the mixer. In addition, the mixer components and a non-ideal LO signal add noise to the output. Leakage effects caused by bad mixer designs also complicate the design of the complete system.

Noise performance and the rejection of out-of-band interferers affect the sensitivity of receivers. Linearity affects transmitter performance, where error-free output signals are important.

The Design Example: A Differential Input Mixer

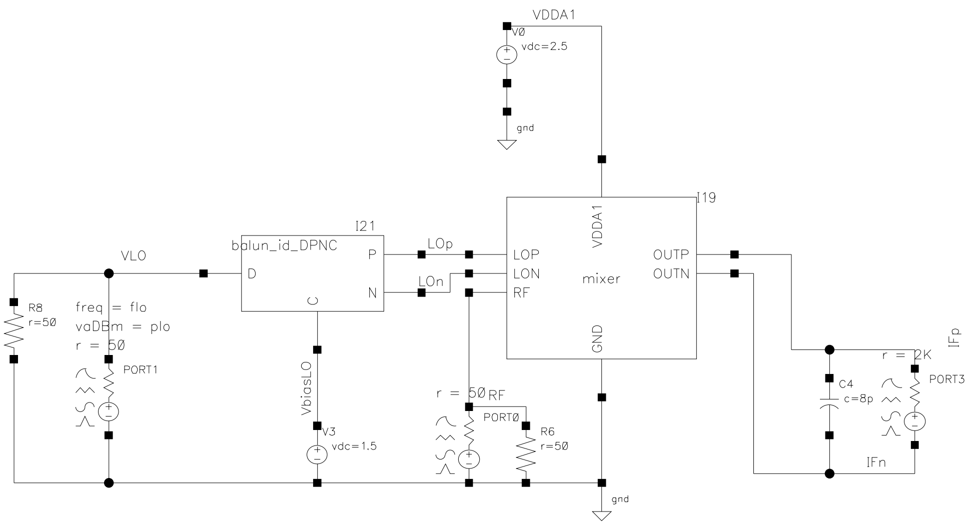
The mixer measurements described in this workshop are calculated using SpectreRF in the Analog Design Environment. The design investigated is the mixer shown below.



The example circuit, a single balanced differential down-converting mixer, runs with a local oscillator at f(LO) = 5 GHz. The range of interest is the baseband output noise from 1 kHz to 10 MHz. The RF signal frequency used for the simulation is around 5001 MHz.

Testbench

In this workshop, you use the mixer measurements testbench shown below to measure typical mixer characteristics. You use a PORT component and match impedance for each of the inputs and the output.



- To supply a LO input to the mixer, the testbench uses a port (PORT1) with a matching resistor and transfers the single-ended signal into the differential with an ideal balun.
- To represent the RF input to the mixer, the testbench uses a port (PORT0) that is matched to the mixer input.
- To use the differential output for measurements, the testbench matches the output port (PORT3) to the output impedance of the mixer.

Simulate the resulting testbench as follows

- Set the LO bias voltage to 1.5 V and set the mixer supply to 2.5 V.
- Set the LO port to a sinusoidal source for all the measurements described in this workshop.
- Set the RF port to either a dc or a sinusoidal source, depending on the requirements of each measurement. The RF port has a dc bias of 0.5 V.
- For both LO and RF ports, the amplitude and frequency of the signal are parameterized as plo, prf, and frf. You usually specify the amplitude in dBm. In addition, for the RF port, specify the small signal parameter PAC Magnitude. Use pacmag or pacdbm, depending on the units you prefer.
- Set the Output port to *dc* with no bias.

Example Measurements Using SpectreRF

The Mixer measurements described in the following labs are calculated using SpectreRF in the Analog Design Environment.

Begin your examination of the flow by bringing up the Cadence Design Framework II (DFII) environment for a full view of the reference design:

To prepare to run the workshop:

Action: 0-1 Move into the **./rfworkshop** directory.

Action: 0-2 Start the tool **virtuoso&**.

Action: 0-3 In the CIW window, select **Tools — Library Manager**.

Lab 1: Voltage Conversion Gain Versus LO Signal Power (Swept hb with hbac)

A mixer's frequency converting action is characterized by conversion gain or loss. The voltage conversion gain is the ratio of the RMS voltages of the IF and RF signals. The power conversion gain is the ratio of the power delivered to the load and the available RF input power.

When the mixer's input impedance and load impedance are both equal to the source impedance, the power and voltage conversion gains, in decibels, are the same. Note that when you load a mixer with a high impedance filter, this condition is not satisfied.

You can calculate the voltage conversion gain in two ways:

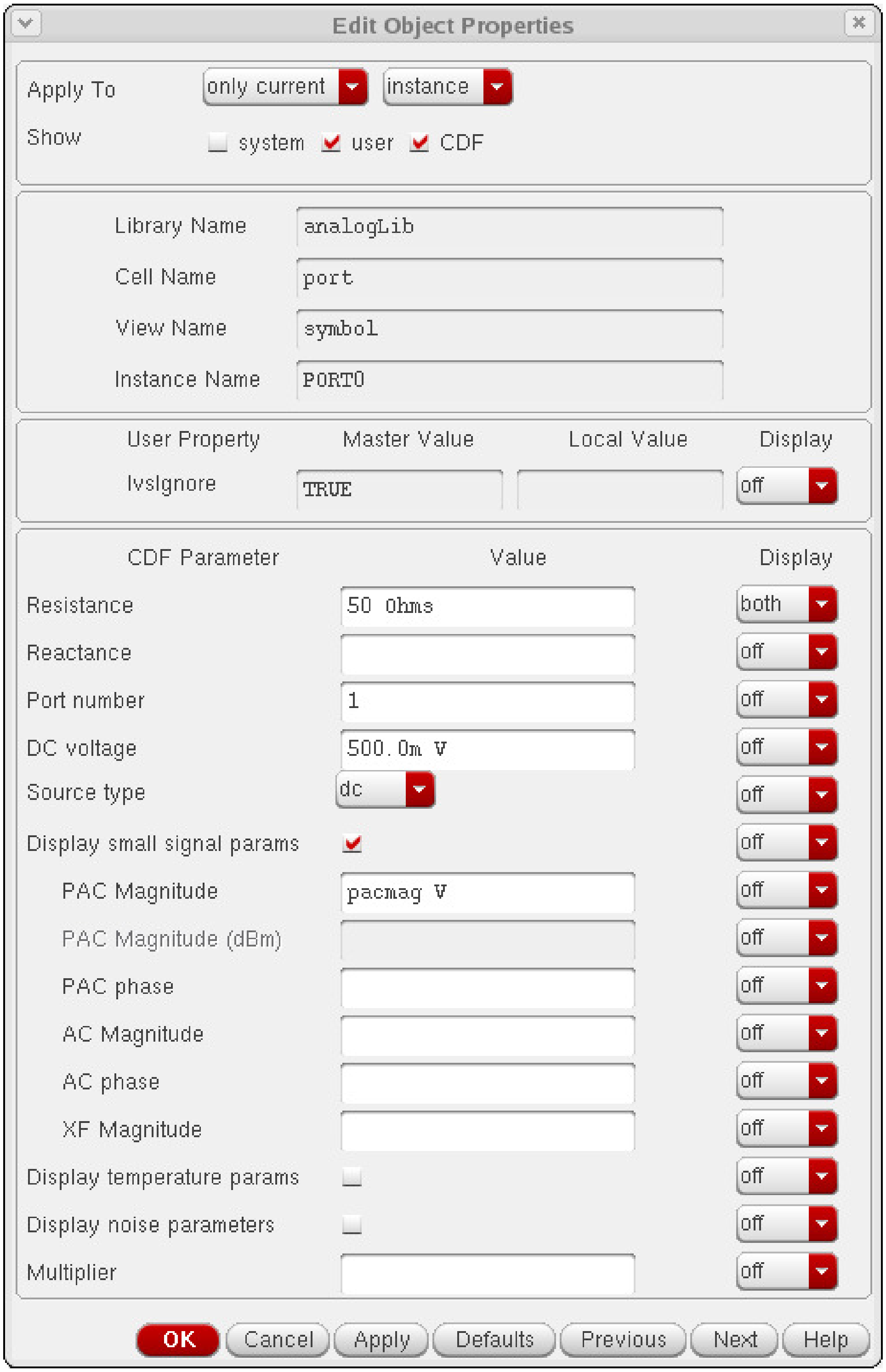
- Using a small-signal analysis, like PSS/hb with PAC/hbac or PXF. The PSS/hb with PAC/hbac or PXF analyses supply the small-signal gain information. You can use either PAC/hbac or PXF analysis to compute the voltage gain.
- Using a two-tone large-signal QPSS/hb analysis, which is more time-consuming. The power convergence gain, in general, requires that you run the two-tone large-signal QPSS/hb analysis.

This example measures the variation of conversion gain with the power of the LO signal.

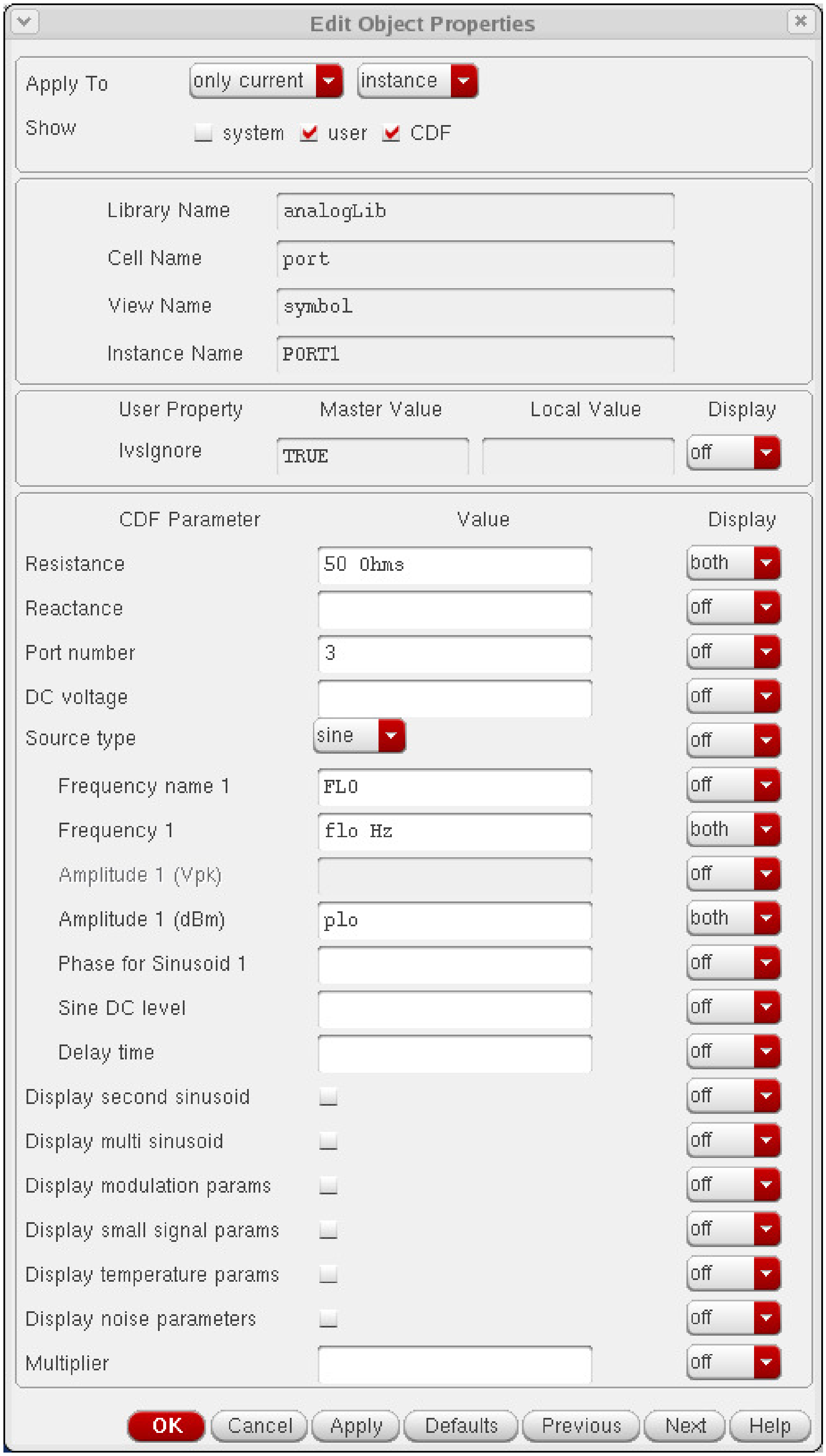
Action 1-1: In the Library Manager window, open the *schematic* view of the *mixer_testbench* design in the library *RFworkshop.*

Action 1-2: Use the mouse to select the `PORT0` source. Then, in the Virtuoso Schematic Editor, select **Edit — Properties — Objects.**

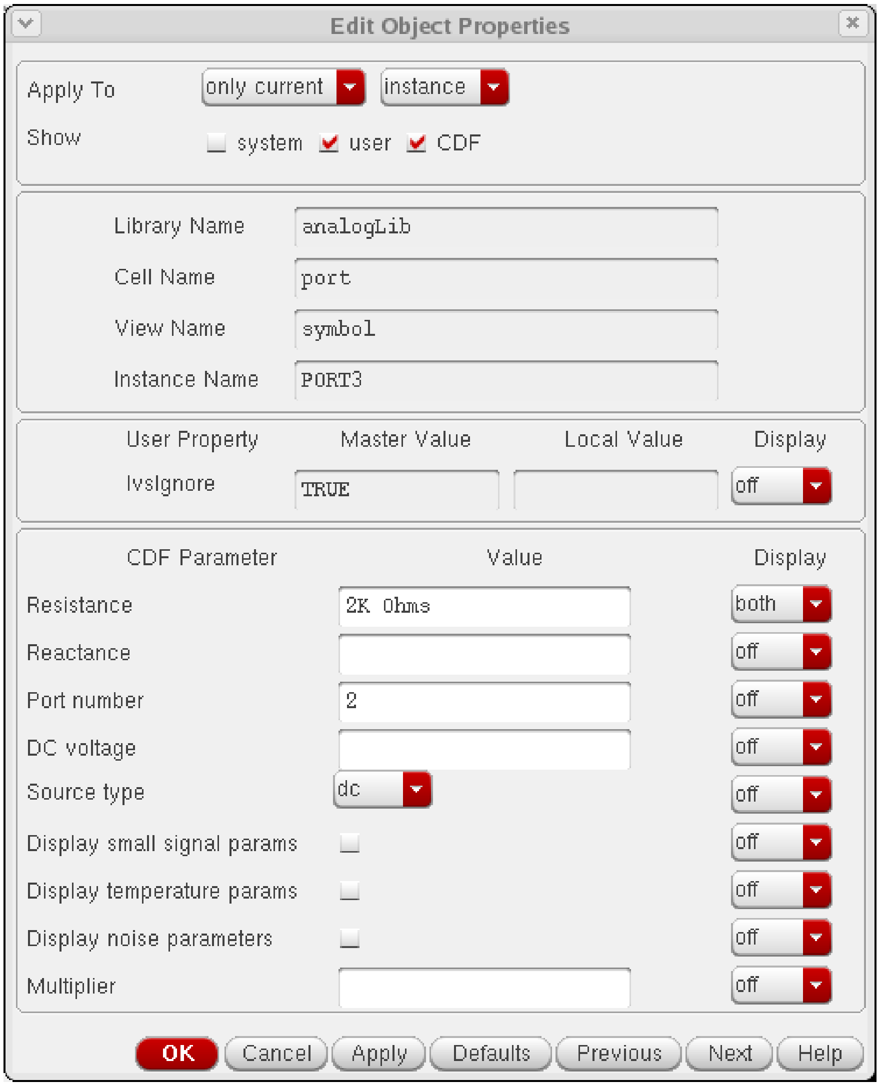
The Edit Object Properties window for the port cell appears.



Action 1-3: Click *OK* on the Edit Object Properties window to close it. Select PORT1 and show the object properties:


Edit Object Properties
Apply To
only current
instance
Show
system
user
CDF
Library Name
analogLib
Cell Name
port
View Name
symbol
Instance Name
PORT1
User Property
Master Value
Local Value
Display
lvsIgnore
TRUE
off
CDF Parameter
Value
Display
Resistance
50 Ohms
both
Reactance
off
Port number
3
off
DC voltage
off
Source type
sine
off
Frequency name 1
FLO
off
Frequency 1
flo Hz
both
Amplitude 1 (Vpk)
off
Amplitude 1 (dBm)
plo
both
Phase for Sinusoid 1
off
Sine DC level
off
Delay time
off
Display second sinusoid
off
Display multi sinusoid
off
Display modulation params
off
Display small signal params
off
Display temperature params
off
Display noise parameters
off
Multiplier
off
OK
Cancel
Apply
Defaults
Previous
Next
Help

Action 1-4: Make sure the *Source type* for `PORT3` is set to *dc*.



Action 1-5: Check and save the schematic.

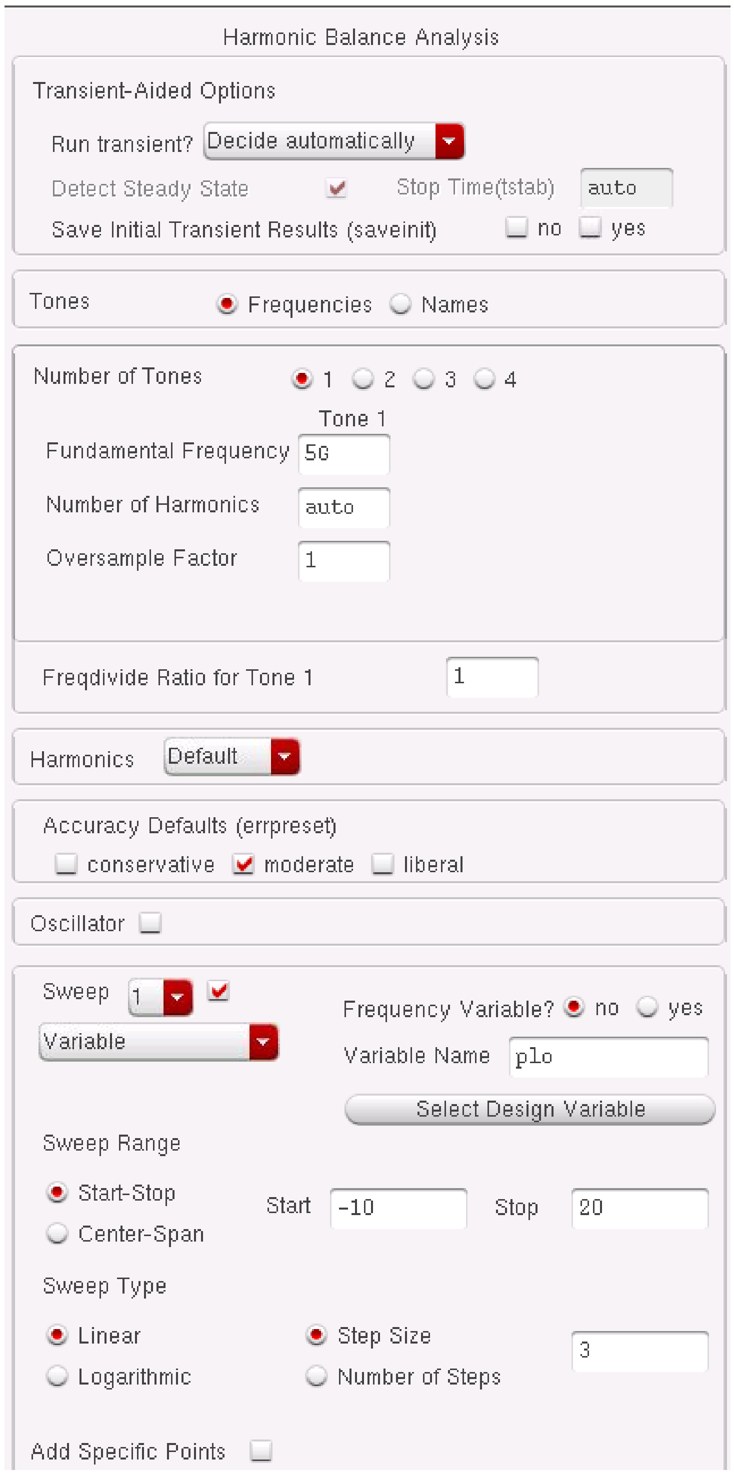
Action 1-6: From the *Mixer_testbench* schematic, choose **Launch — ADE L**.

The Virtuoso Analog Design Environment window appears.

Action 1-7: You can choose **Session — Load State**, select **Cellview** in **Load State Option** and load state "**Lab1_VCGvsLO_hbac**" and skip to Action 1-12 or …

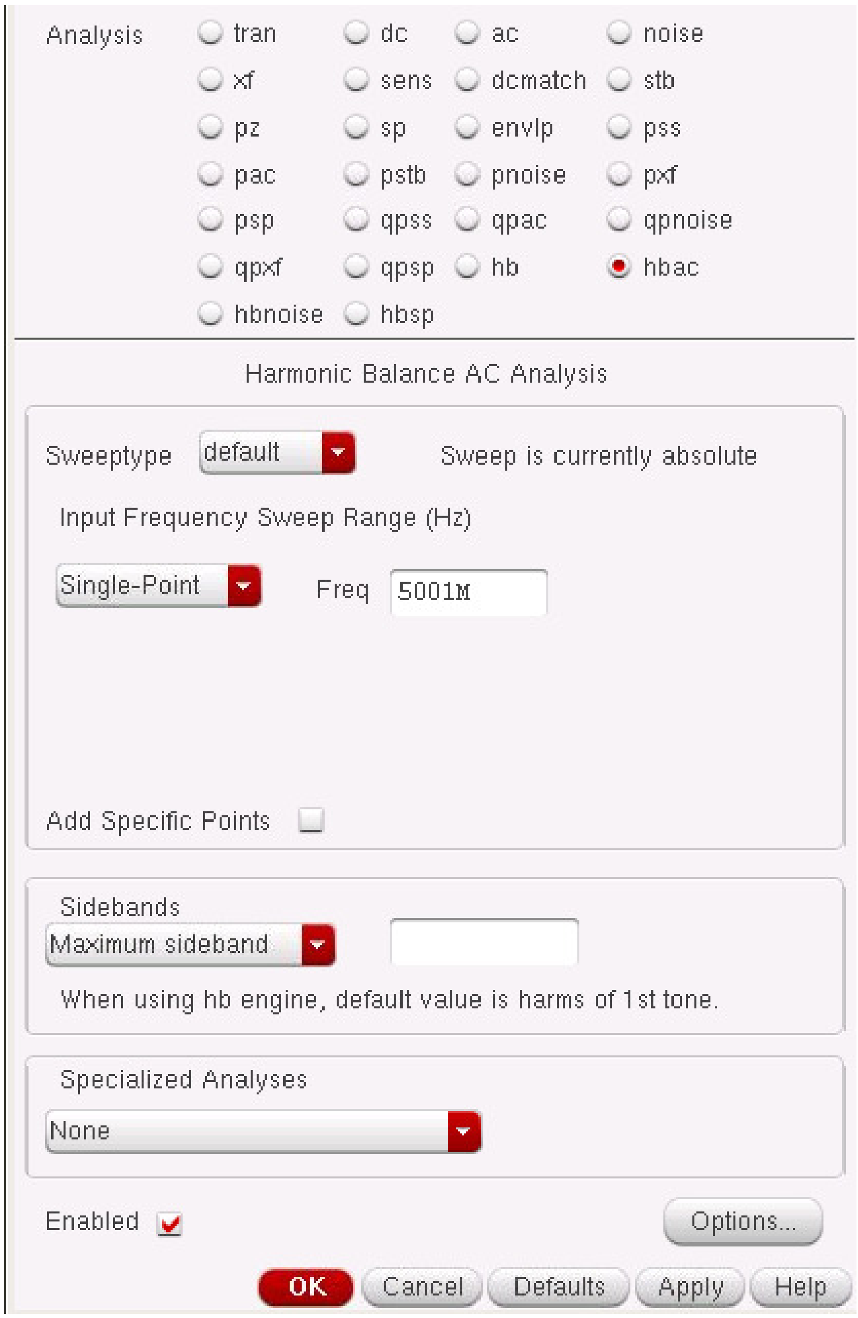
Action 1-8: In the Virtuoso Analog Design Environment window, choose **Analyses — Choose**.

Action 1-9: In the Choosing Analyses window, select the *hb* button in the *Analysis* field of the window. Set the fundamental frequency parameter, flo = 5 GHz. Set *errpreset* = *moderate*. Click *Sweep* and enter plo as the *Variable Name* parameter to sweep LO power. Click *Sweep Range* and set *Start* = -10 dBm and *Stop* = 20 dBm. This sweeps LO power from a small value to a value above the expected gain saturation. The form looks like this.



Note: The new hb analysis in MMSIM12.1 determines the length of tstab and number of harmonics automatically. All you need to do here is to set fundamental frequency and the sweep.

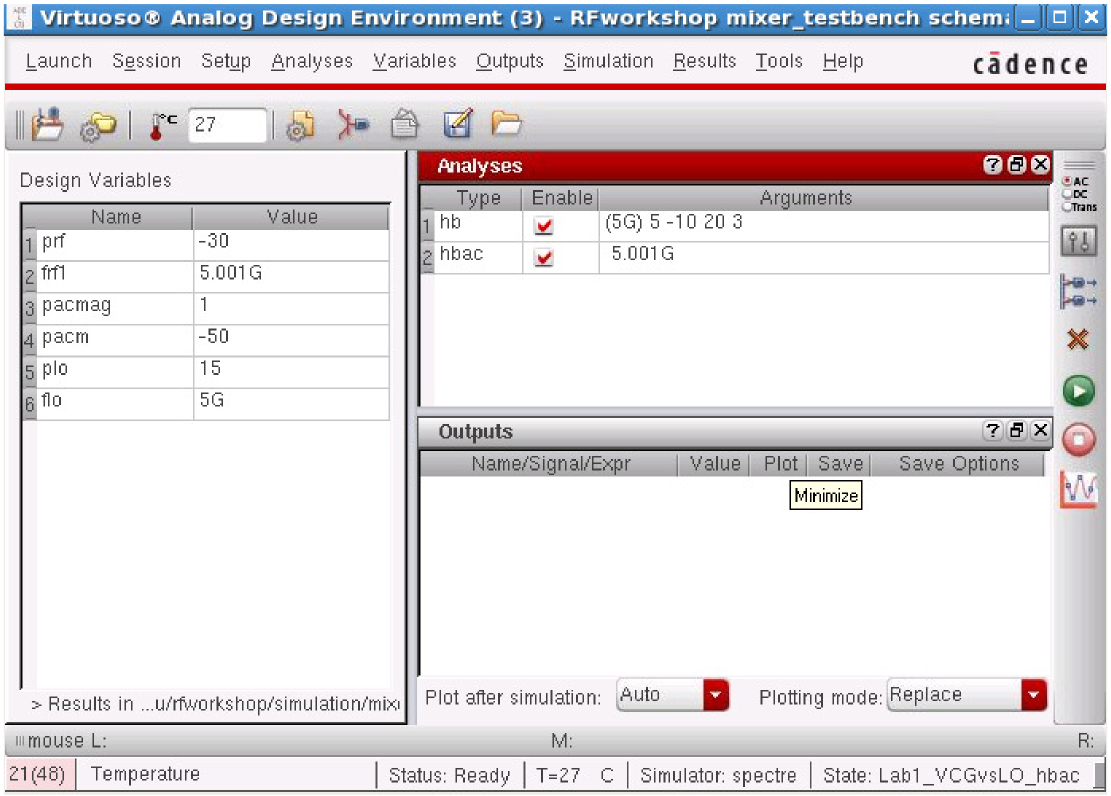
Action 1-10: In the Choosing Analyses window, select the *hbac* button in the *Analysis* field of the window. Set the fixed input frequency point to the RF signal frequency, 5001 MHz. Leave *Maximum sideband* blank so that the default value, which is the number of harms in hb, will be used..



Action 1-11: Make sure the *Enabled* button is on. In the Choosing Analyses window,

click *OK*.

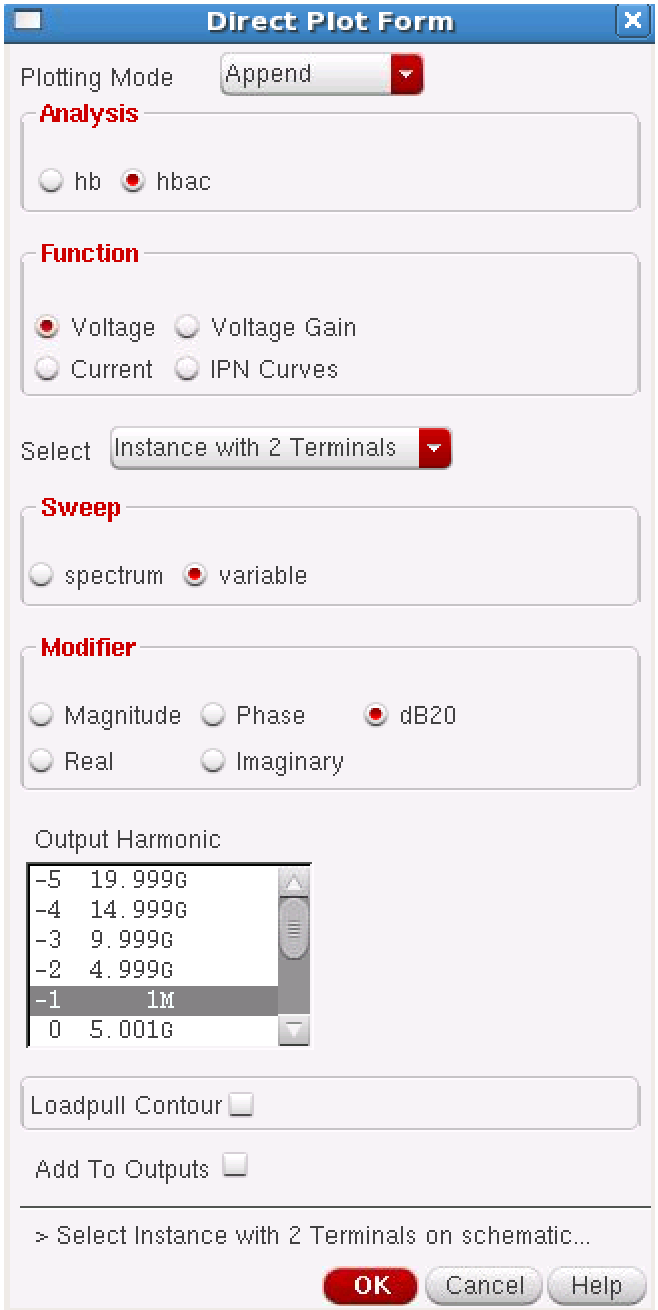
The Virtuoso Analog Design Environment window looks like this.



Action 1-12: In the Virtuoso Analog Design Environment window, choose **Simulation — Netlist and Run** or click the **Netlist and Run** icon to start the simulation.

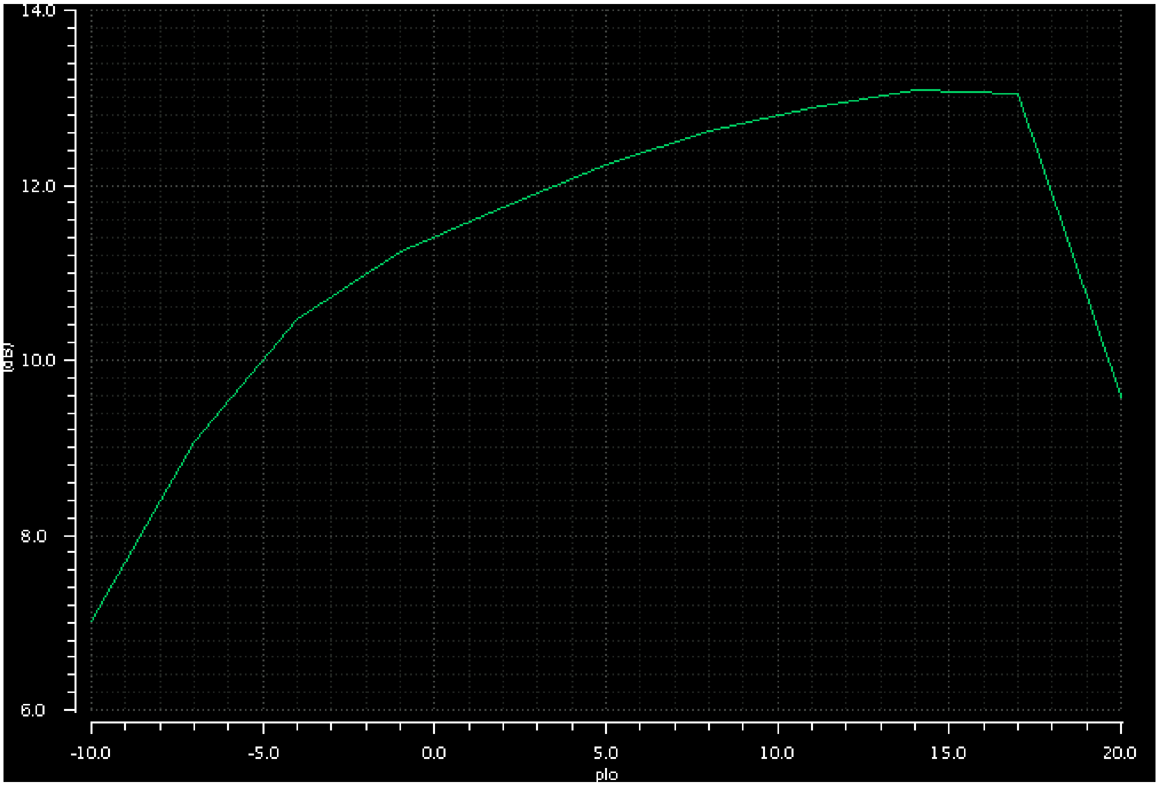
Action 1-13: After the simulation completes, in the Virtuoso Analog Design Environment window, choose **Results — Direct Plot — Main Form**.

Action 1-14: In the Direct Plot Form, select the *hbac* button, and configure the form as follows:



Action 1-15: Select `port3` on the schematic.

You get the following waveform:



The PAC analysis computes gain directly only when you set the pacmag parameter to 1 V. Otherwise, take a ratio of the output and input. The maximum conversion gain value is reached somewhere around 15 dBm. Use this value for the plo parameter in the following measurements.

Action 1-16: After viewing the waveforms, click *Cancel* in the Direct Plot Form. Close the waveform window.

Lab 2: Voltage Conversion Gain Versus RF Frequency (hb and Swept hbac)

This lab measures how conversion gain varies with the frequency of the stimuli.

Action 2-1: If it is not already open, open the *schematic* view of the *mixer_testbench* design in the library *RFworkshop.*

Action 2-2: Set port as you did in Lab 1.

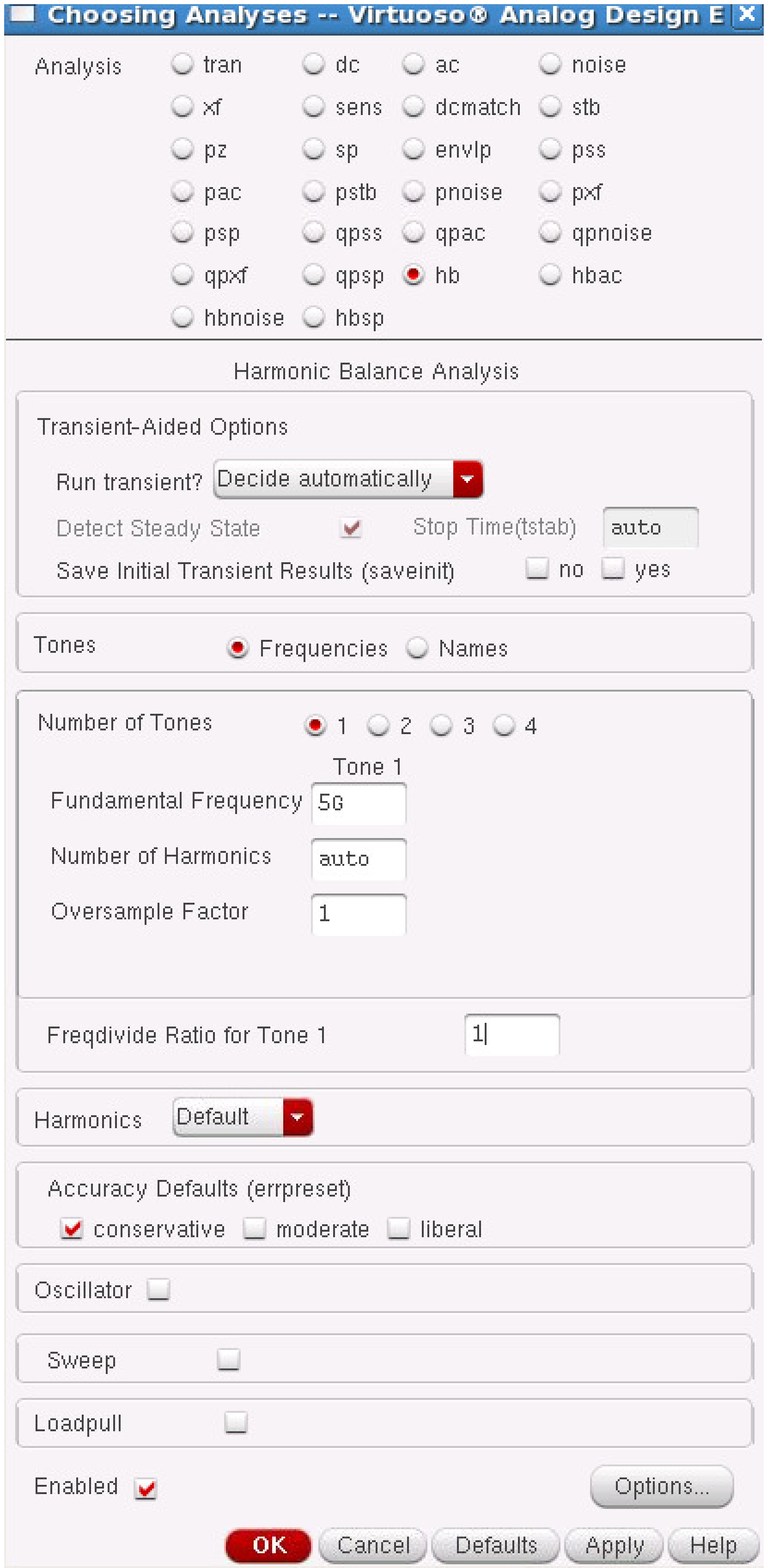
Action 2-3: From the *Mixer_testbench* schematic, choose **Launch — ADE L.**

The Virtuoso Analog Design Environment window appears.

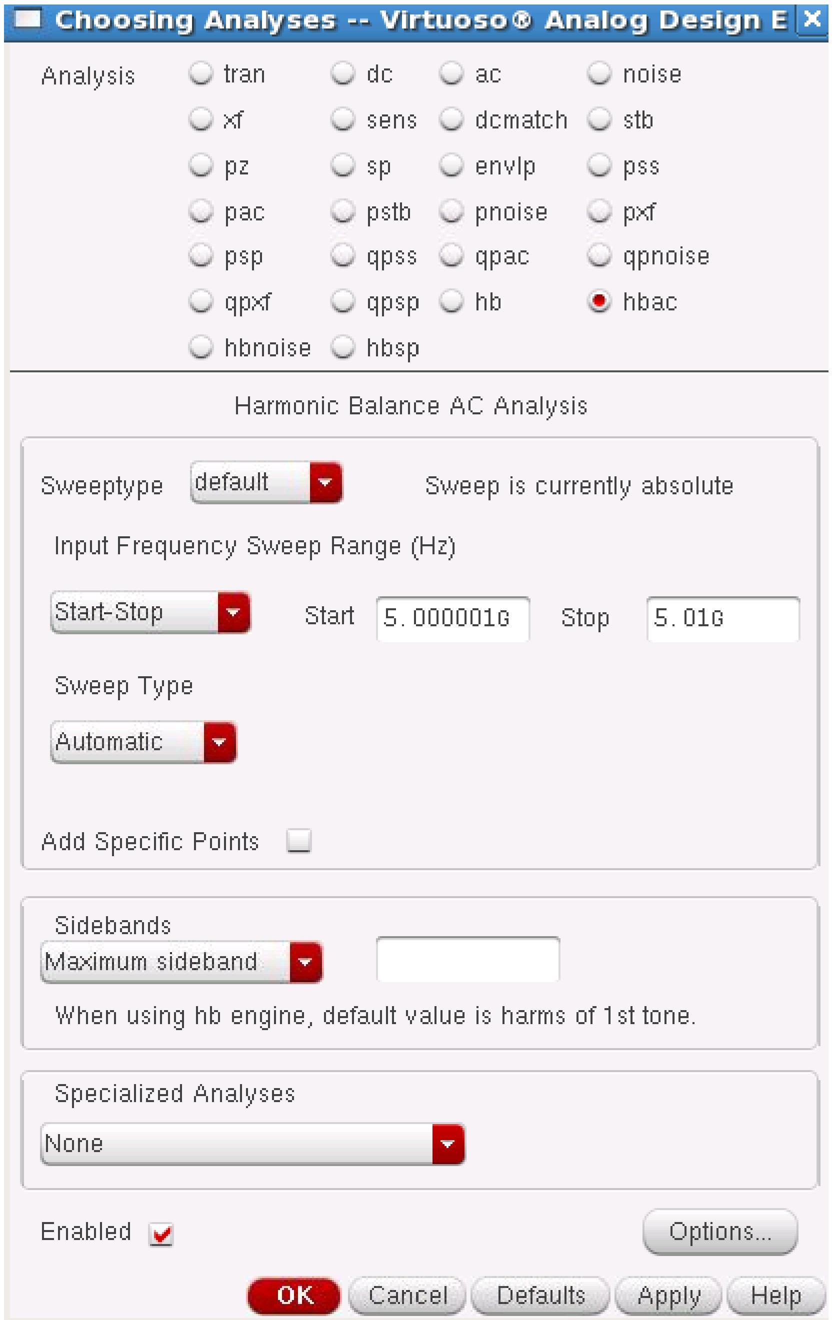
Action 2-4: You can choose **Session — Load State**, select **Cellview** in **Load State Option** and load state "**Lab2_VCGvsRF_hbac**" and skip to Action 2-9 or …

Action 2-5: In the Virtuoso Analog Design Environment window, choose **Analyses — Choose**.

Action 2-6: In the Choosing Analyses window, select the *hb* button in the *Analysis* field of the window and set the form as follows:

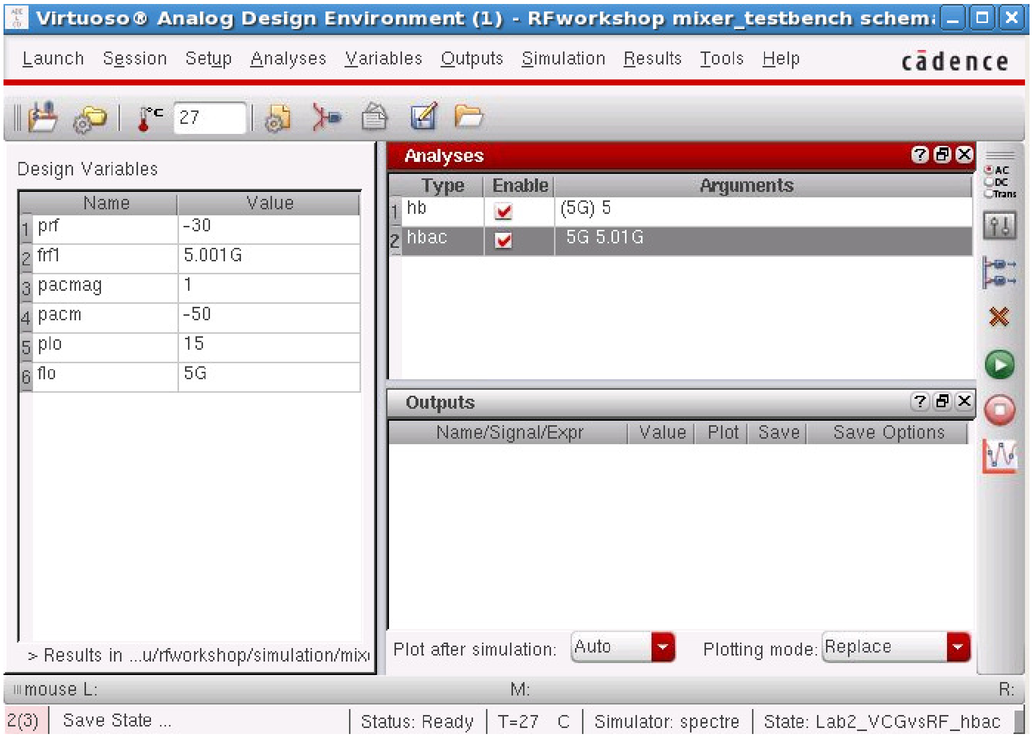

Choosing Analyses -- Virtuoso® Analog Design E
Analysis
tran
dc
ac
noise
xf
sens
dcmatch
stb
pz
sp
envlp
pss
pac
pstb
pnoise
pxf
psp
qpss
qpac
qpnoise
qpxf
qpsp
hb
hbac
hbnoise
hbsp
Harmonic Balance Analysis
Transient-Aided Options
Run transient?
Decide automatically
Detect Steady State
Stop Time(tstab)
auto
Save Initial Transient Results (saveinit)
no
yes
Tones
Frequencies
Names
Number of Tones
1
2
3
4
Tone 1
Fundamental Frequency
5G
Number of Harmonics
auto
Oversample Factor
1
Freqdivide Ratio for Tone 1
1
Harmonics
Default
Accuracy Defaults (errpreset)
conservative
moderate
liberal
Oscillator
Sweep
Loadpull
Enabled
Options...
OK
Cancel
Defaults
Apply
Help

Action 2-7: In the Choosing Analyses window, select the *hbac* button in the *Analysis* field of the window. Set the RF input frequency to sweep from 5 G + 1 kHz to 5 G + 10 MHz. The form looks like this:



Action 2-8: Make sure the *Enabled* button is on. In the Choosing Analyses window, click *OK*.

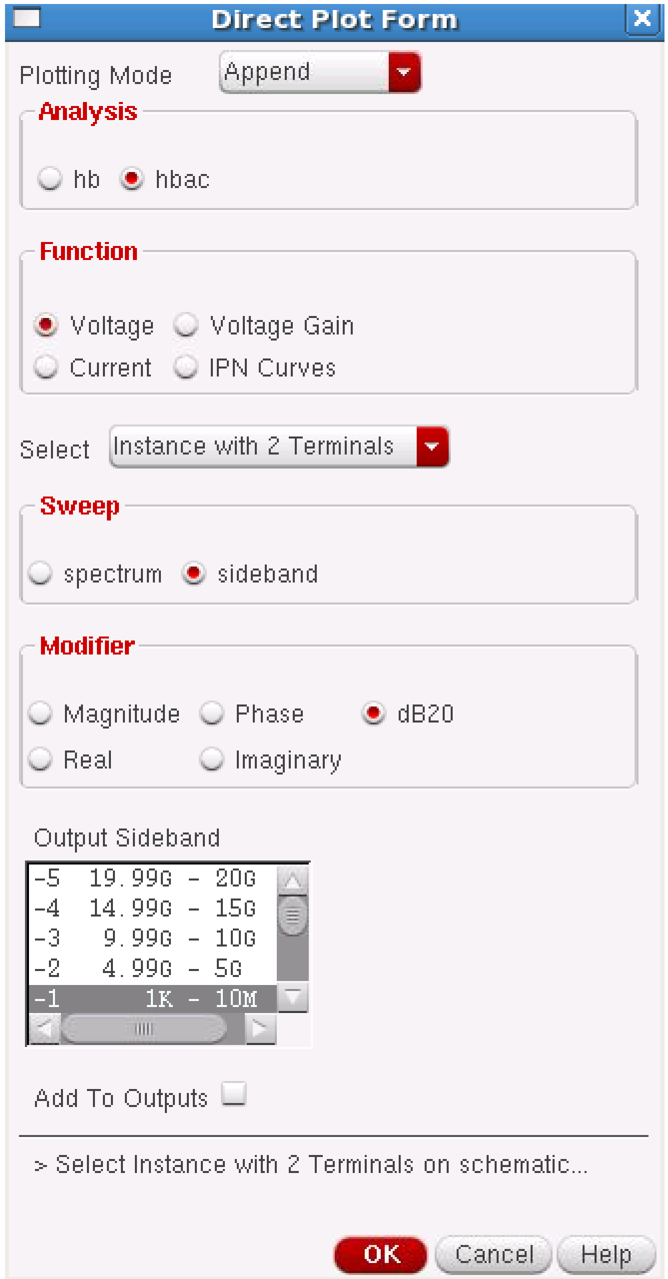
The Virtuoso Analog Design Environment window looks like this.



Action 2-9: In the Virtuoso Analog Design Environment window, choose **Simulation — Netlist and Run** or click the **Netlist and Run** icon to start the simulation.

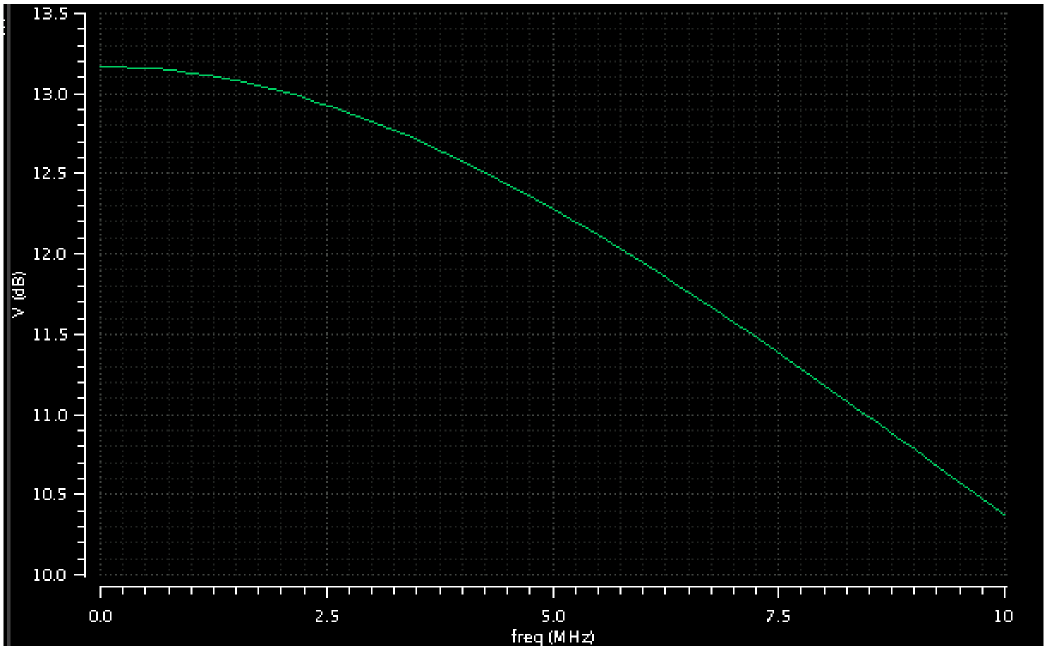
Action 2-10: After the simulation completes, in the Virtuoso Analog Design Environment window, choose **Results — Direct Plot — Main Form**.

Action 2-11: In the Direct Plot Form, select the *hbac* button, and configure the form as follows:



Action 2-12: Select `port3` on the schematic.

The waveform window appears:



Because the sweep type in the analysis is linear by default, uniform frequency points display along the X-axis in the above plot. For a large frequency range, set the sweep type to logarithmic.

The same PAC analysis generates results you can use to measure RF to LO isolation. The results are also used in the measurements that follow.

Action 2-13: Close the waveform window and click *Cancel* in the Direct Plot Form.

Lab 3: Voltage Conversion Gain Versus RF Frequency (hb and Swept hbnoise)

This example uses PXF analysis to measure the small-signal voltage conversion gain.

Action 3-1: If it is not already open, open the *schematic* view of the *mixer_testbench* design in the library *RFWorkshop*.

Action 3-2: Set the ports as you did in Lab1.

Action 3-3: From the *Mixer_testbench* schematic, choose **Launch — ADE L**.

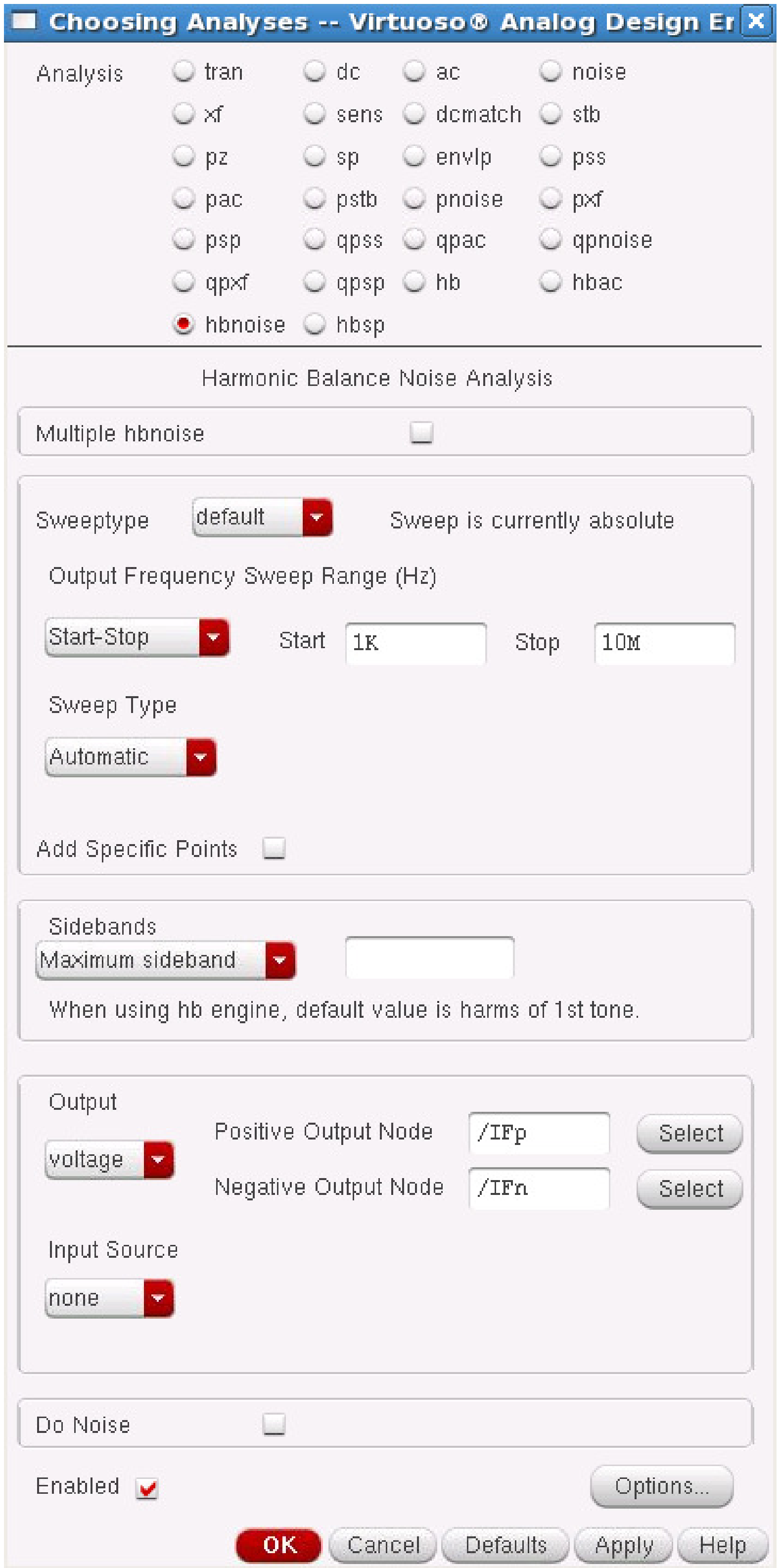
The Virtuoso Analog Design Environment window appears.

Action 3-4: You can choose **Session — Load State**, select **Cellview** in **Load State Option** and load state “**Lab3_VCGvsRF_hbnoise**” and skip to Action 3-9 or …

Action 3-5: In the Virtuoso Analog Design Environment window, choose **Analyses — Choose**.

Action 3-6: In the Choosing Analyses window, select the *hb* button in the *Analysis* field of the window. Set the form as in Action 2-6.

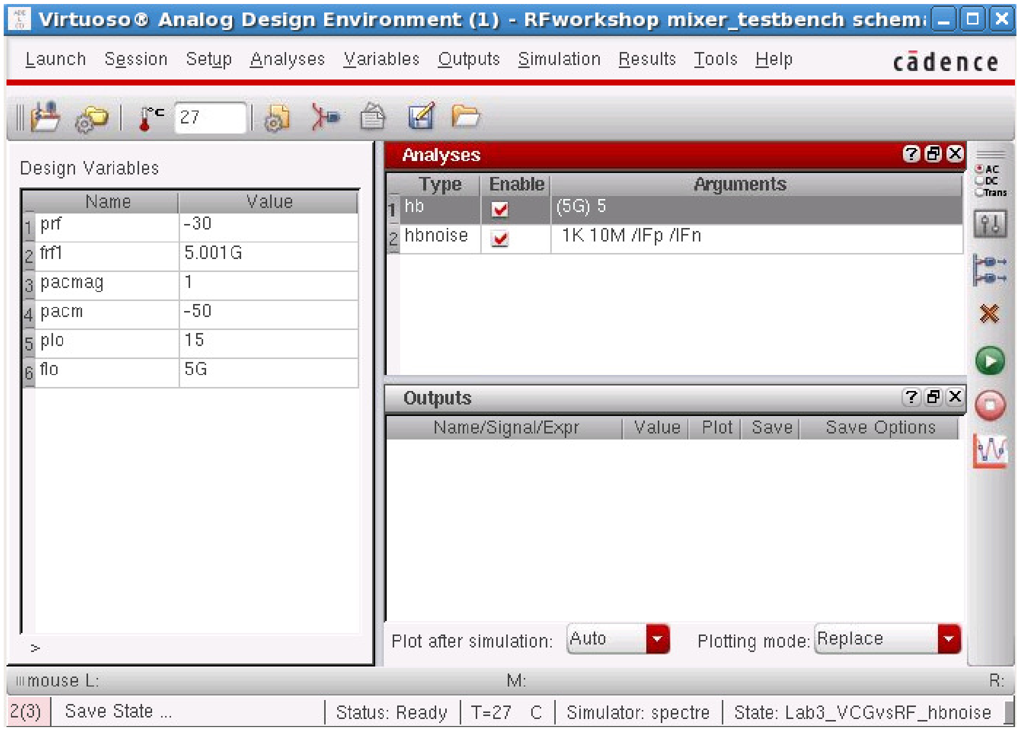
Action 3-7: In the Choosing Analyses window, select the *hbnoise* button in the *Analysis* field of the window. Sweep the output frequency from 1 kHz to 10 MHz. The form looks like this.



Note: When turning off the *Do Noise* button, the hbnoise analysis is actually the hbxf analysis.

Action 3-8: Make sure the *Enabled* button is on. In the Choosing Analyses window, click *OK*.

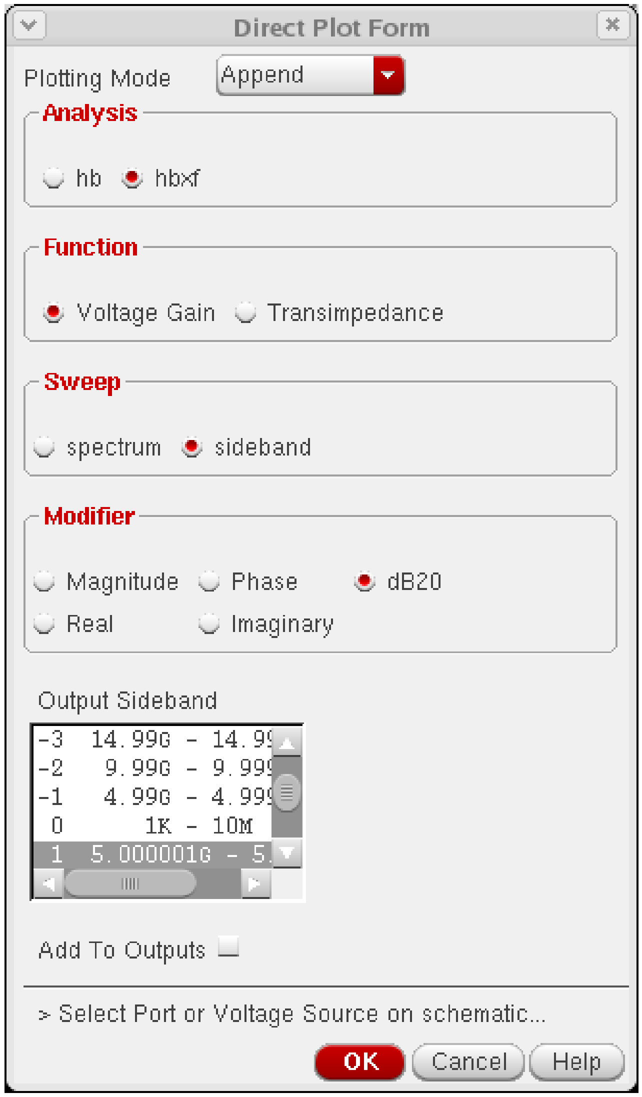
The Virtuoso Analog Design Environment window looks like this.



Action 3-9: In the Virtuoso Analog Design Environment window, choose **Simulation — Netlist and Run** or click the **Netlist and Run** icon to start the simulation.

Action 3-10: After the simulation completes, in the Virtuoso Analog Design Environment window, choose **Results — Direct Plot — Main Form**.

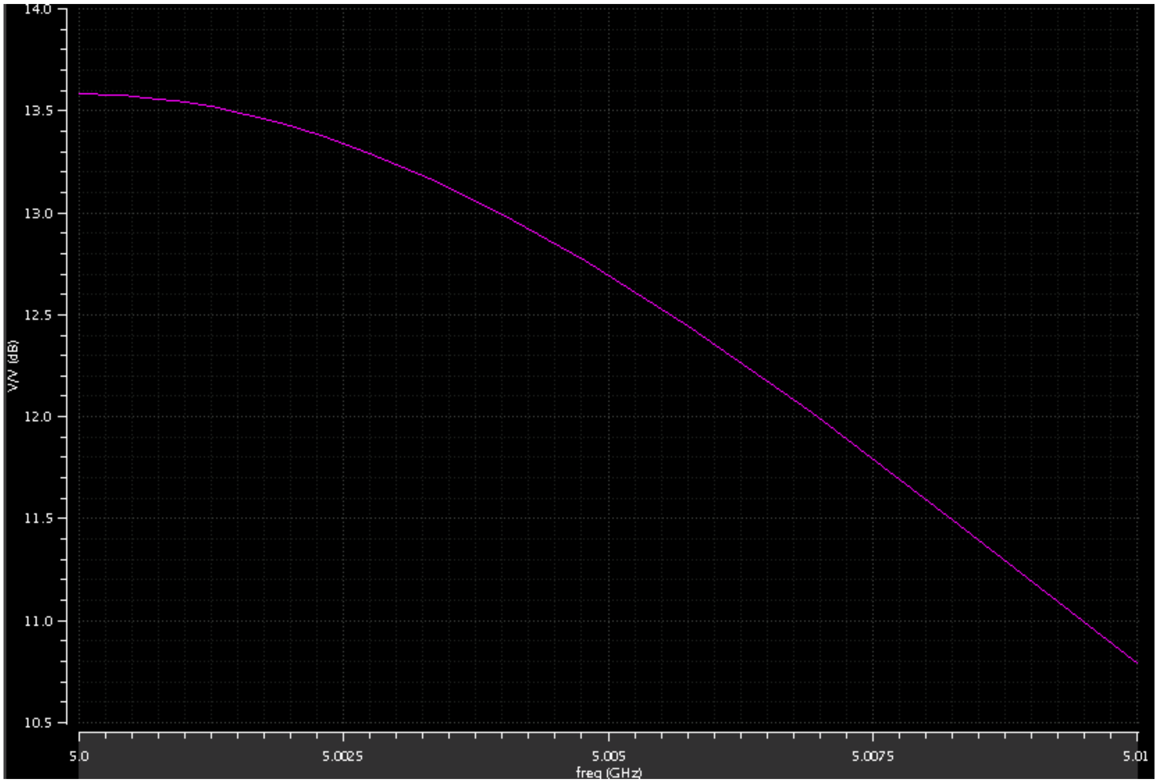
Action 3-11: In the Direct Plot Form, select the *hbxf* button and configure the form as follows:



Action 3-12: Select input `port0` on the schematic.

The waveform window appears:

18



Action 3-13: After viewing the waveforms, click *Cancel* in the Direct Plot Form.

Another way to measure small-signal gain is to use the PSS and PSP/PXF analyses to get the gain and noise parameters with one simulation. For more information, refer to the SpectreRF user guide Appendix L (using psp and pnoise analysis).

You can also set up an appropriate QPSS analysis to measure large-signal gain. Set LO as a large tone on the Plo port. Use a sinusoidal voltage source for the Prf port. This analysis models the signal at a particular frequency going through the mixer. In the Direct Plot Form for QPSS, the Voltage and Power Gain provide all the needed information.

Lab 4: Power Conversion Gain Versus RF Frequency (hb with Two Tones)

You can measure the Power Conversion Gain and Power Dissipation for an unmatched source and load using an hb analysis with two tones. If the effect of the RF tone is small, you might use an hb analysis with one tone instead, as mentioned in previous sections.

Action 4-1: If it is not already open, open the *schematic* view of the *mixer_testbench* design in the library *RFworkshop*

Action 4-2: From the *Mixer_testbench* schematic, choose **Launch — ADE L**.

The Virtuoso Analog Design Environment window appears.

Action 4-3: Use the mouse to select the `PORT0` source. Then, in the Virtuoso Schematic Editor, select **Edit — Properties — Objects**. The Edit Object Properties window for the port cell appears. Make sure the properties are set as follows:

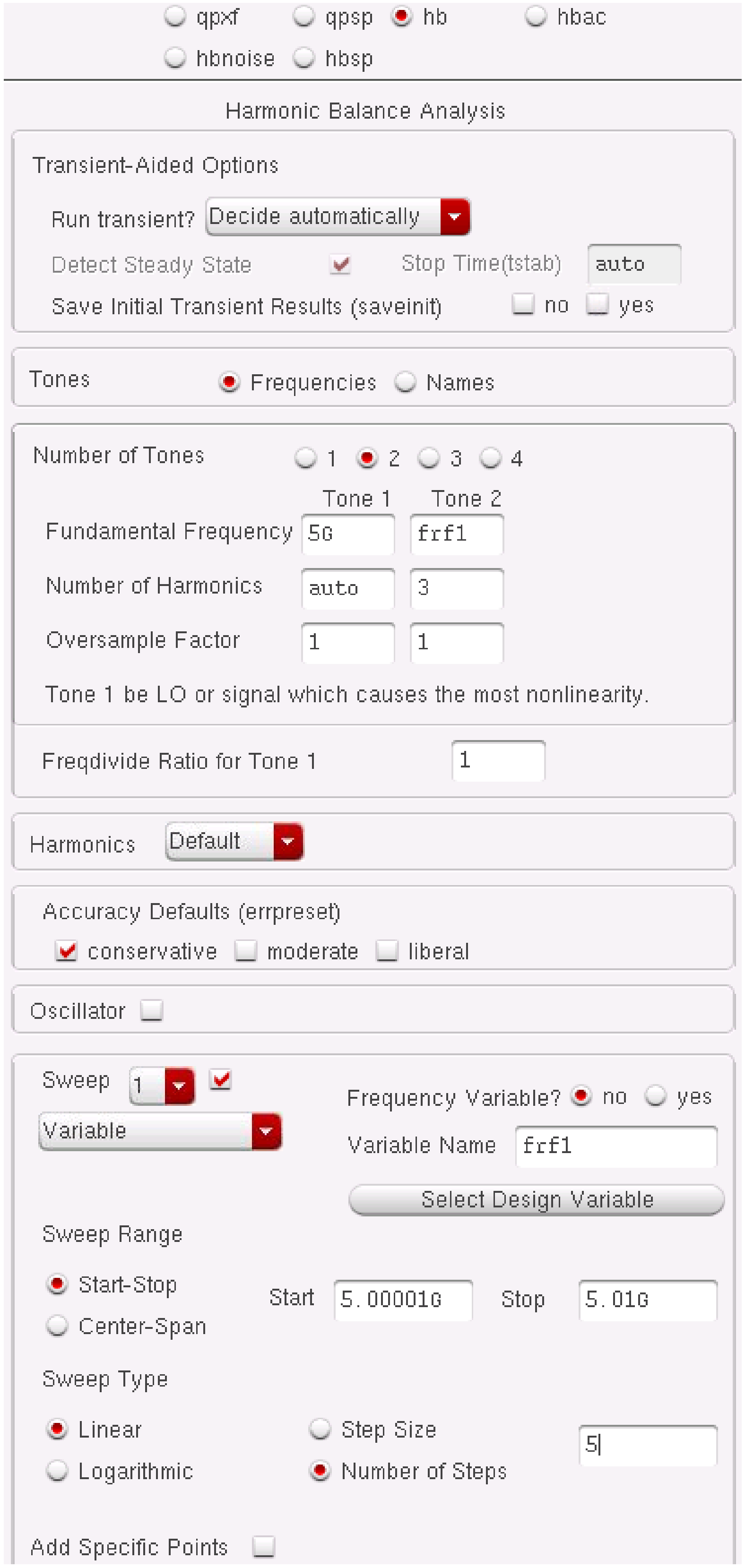
Parameter	Value
Resistance	50 ohm
Port Number	1
DC voltage	500 mV
Source type	*sine*
Frequency name 1	RF1
Frequency 1	frf1
Amplitude 1 (dBm)	prf

Action 4-4: Check and save the schematic.

Action 4-5: You can choose **Session — Load State**, select **Cellview** in **Load State Option** and load state "**Lab4_PCG_hb2**" and skip to Action 4-12 or …

Action 4-6: In the Virtuoso Analog Design Environment window, choose **Analyses — Choose**.

Action 4-7: In the Choosing Analyses window, select the *hb* button in the *Analysis* field of the window. Set the form as follow:


qpxf
qpsp
hb
hbac
hbnoise
hbsp
Harmonic Balance Analysis
Transient-Aided Options
Run transient?
Decide automatically
Detect Steady State
Stop Time(tstab)
auto
Save Initial Transient Results (saveinit)
no
yes
Tones
Frequencies
Names
Number of Tones
1
2
3
4
Tone 1
Tone 2
Fundamental Frequency
5G
frf1
Number of Harmonics
auto
3
Oversample Factor
1
1
Tone 1 be LO or signal which causes the most nonlinearity.
Freqdivide Ratio for Tone 1
1
Harmonics
Default
Accuracy Defaults (errpreset)
conservative
moderate
liberal
Oscillator
Sweep
1
Frequency Variable?
no
yes
Variable
Variable Name
frf1
Select Design Variable
Sweep Range
Start-Stop
Start
5.00001G
Stop
5.01G
Center-Span
Sweep Type
Linear
Step Size
5
Logarithmic
Number of Steps
Add Specific Points

Action 4-8: Make sure the *Enabled* button is on. In the Choosing Analyses window, click *OK*.

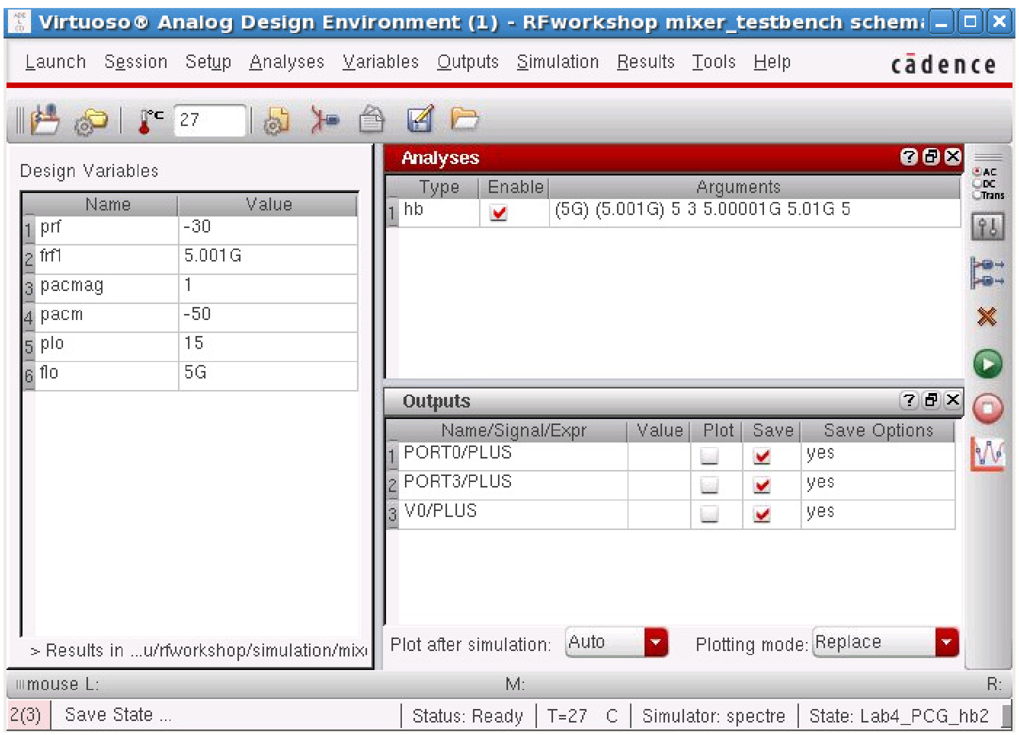
Action 4-9: In the Virtuoso Analog Design Environment window, choose **Outputs — To Be Saved — Select on Schematic**.

Action 4-10: In the schematic, select the positive terminals of `port0`, `port3`, and `V0`.

After you select them, the terminals are circled in the schematic window, indicating that you are saving the currents at these nodes.

Action 4-11: With your cursor in the schematic window, press **Esc** to end the selections.

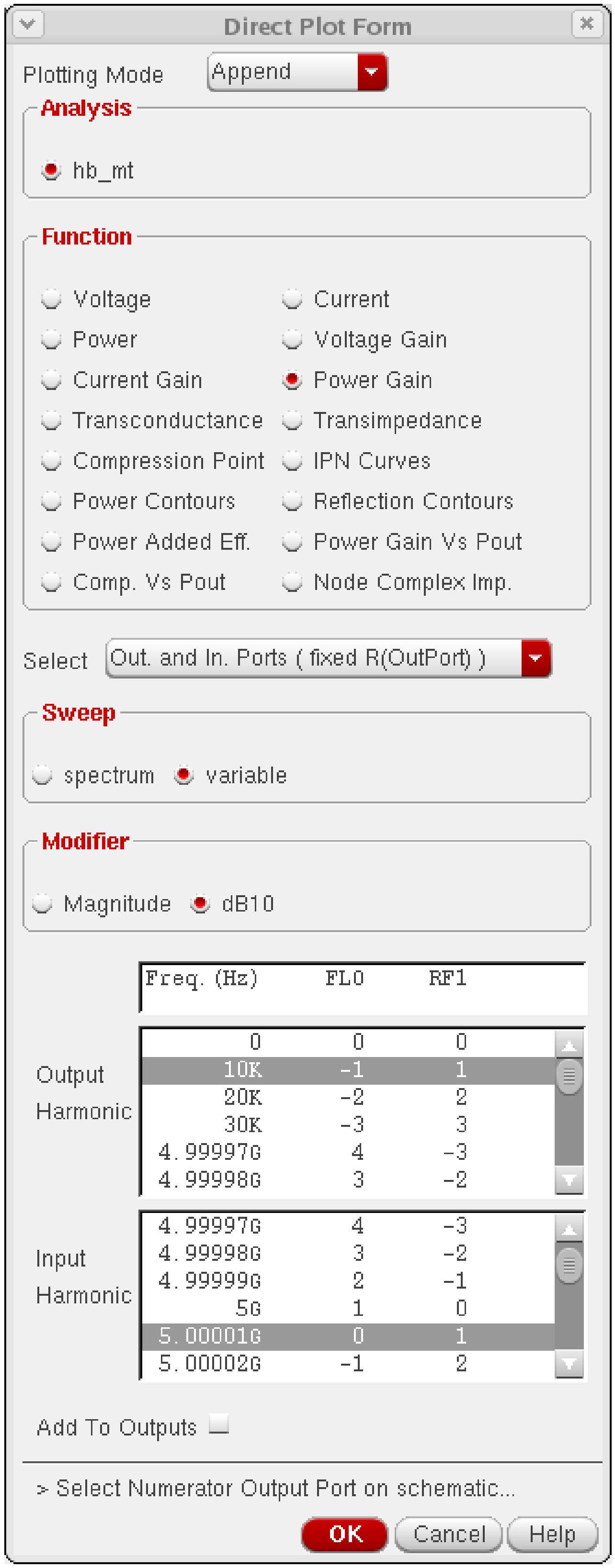
The Virtuoso Analog Design Environment window looks like this.



Action 4-12: In the Virtuoso Analog Design Environment window, choose **Simulation — Netlist and Run** or click the **Netlist and Run** icon to start the simulation.

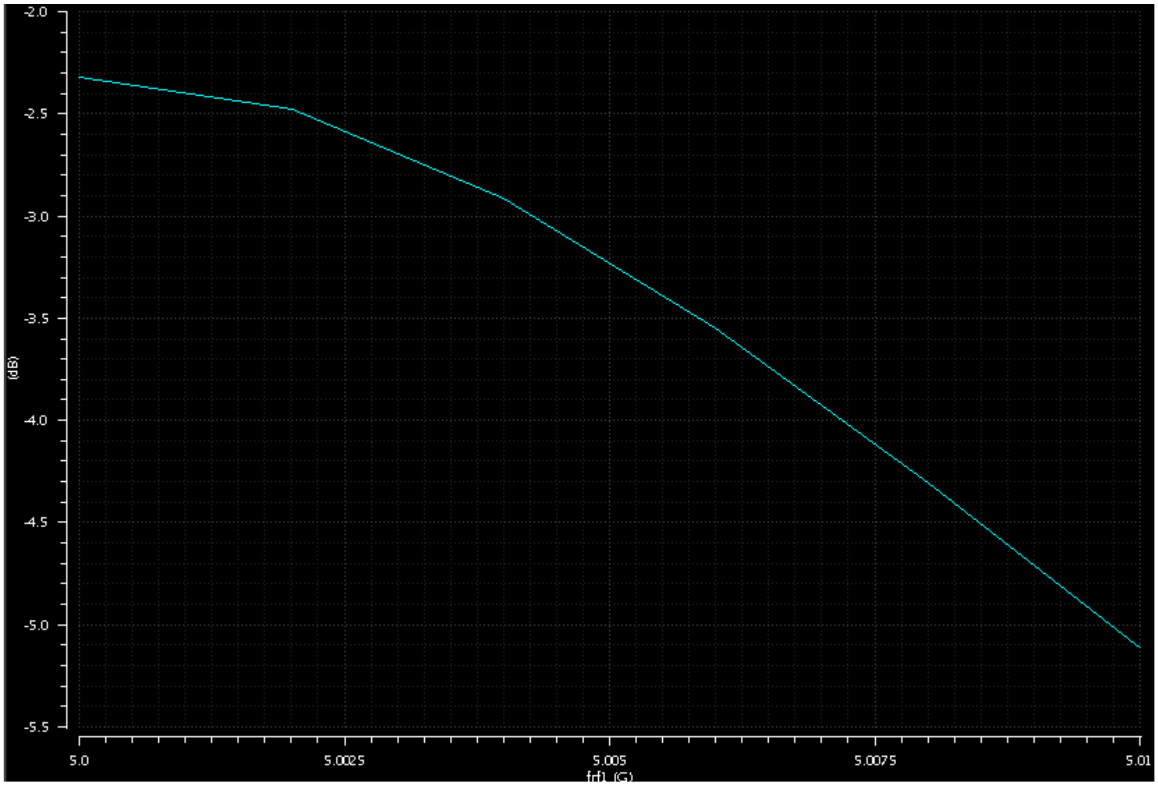
Action 4-13: After the simulation completes, in the Virtuoso Analog Design Environment window, choose **Results — Direct Plot — Main Form**.

Action 4-14: In the Direct Plot Form, select the *hb_mt* button, and configure the form as follows:


Direct Plot Form
Plotting Mode
Append
Analysis
hb_mt
Function
Voltage
Current
Power
Voltage Gain
Current Gain
Power Gain
Transconductance
Transimpedance
Compression Point
IPN Curves
Power Contours
Reflection Contours
Power Added Eff.
Power Gain Vs Pout
Comp. Vs Pout
Node Complex Imp.
Select
Out. and In. Ports (fixed R(OutPort))
Sweep
spectrum
variable
Modifier
Magnitude
dB10
Freq. (Hz) FLO RF1
Output Harmonic
0 0 0
10K -1 1
20K -2 2
30K -3 3
4.99997G 4 -3
4.99998G 3 -2
Input Harmonic
4.99997G 4 -3
4.99998G 3 -2
4.99999G 2 -1
5G 1 0
5.00001G 0 1
5.00002G -1 2
Add To Outputs
> Select Numerator Output Port on schematic...
OK
Cancel
Help

Action 4-15: Select the top terminal of `port3` and the top terminal of `port0` on the schematic.

The waveform window appears.



Action 4-16: Close the waveform window. Click *Cancel* in the Direct Plot Form.

Lab 5: Periodic S-Parameters (hb and hbsp)

The receiver amplifies the small input signals to the point where they can be processed by the baseband section. You develop a gain budget where every stage in the receiver is assigned the gain it is expected to provide. Therefore, the signal gain or loss provided by the mixer must be known.

There are various ways of characterizing gain and all are derived from the mixer's S-parameters. As such, it must be easy to calculate the various S-parameters of the circuit and apply the various gain metrics.

Action 5-1: If it is not already open, open the *schematic* view of the *mixer_testbench* design in the library *RFworkshop*.

Action 5-2: Use the mouse to select the `PORT0` source. Then in the Virtuoso Schematic Editor select **Edit — Properties — Objects**. The Edit Object Properties window for the port cell appears. Change the *Source type* to *dc*. Blank out all the Second Sinusoid fields before setting the *Source type* to *dc*.

Parameter	Value
Resistance	50 ohm
Port Number	1
DC voltage	500 mV
Source type	*dc*
PAC Magnitude	(blank)

For small-signal analysis, it is often sufficient to treat the RF input as a small signal (for example, by setting the *Source type* to *dc*). However, sometimes it is important to analyze additional noise folding terms induced by the RF input (larger signal interferer). In those cases, the RF source is a large signal and the *Source type* is *sine*.

Action 5-3: Set **lo** port to *sine* type and output port to *dc* type.

Action 5-4: Check and save the schematic.

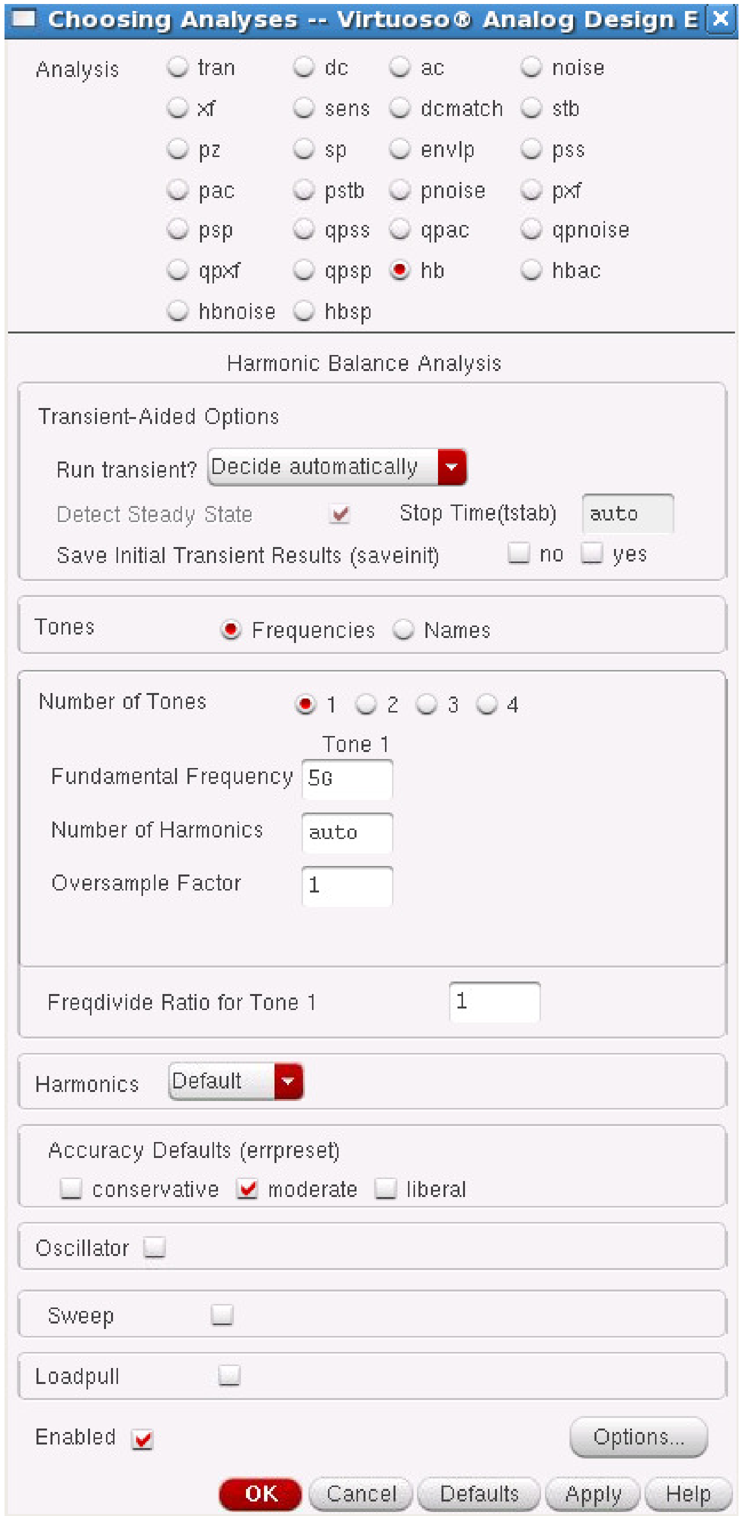
Action 5-5: From the *Mixer_testbench* schematic, choose **Tools — Analog Environment.**

The Virtuoso Analog Design Environment window appears.

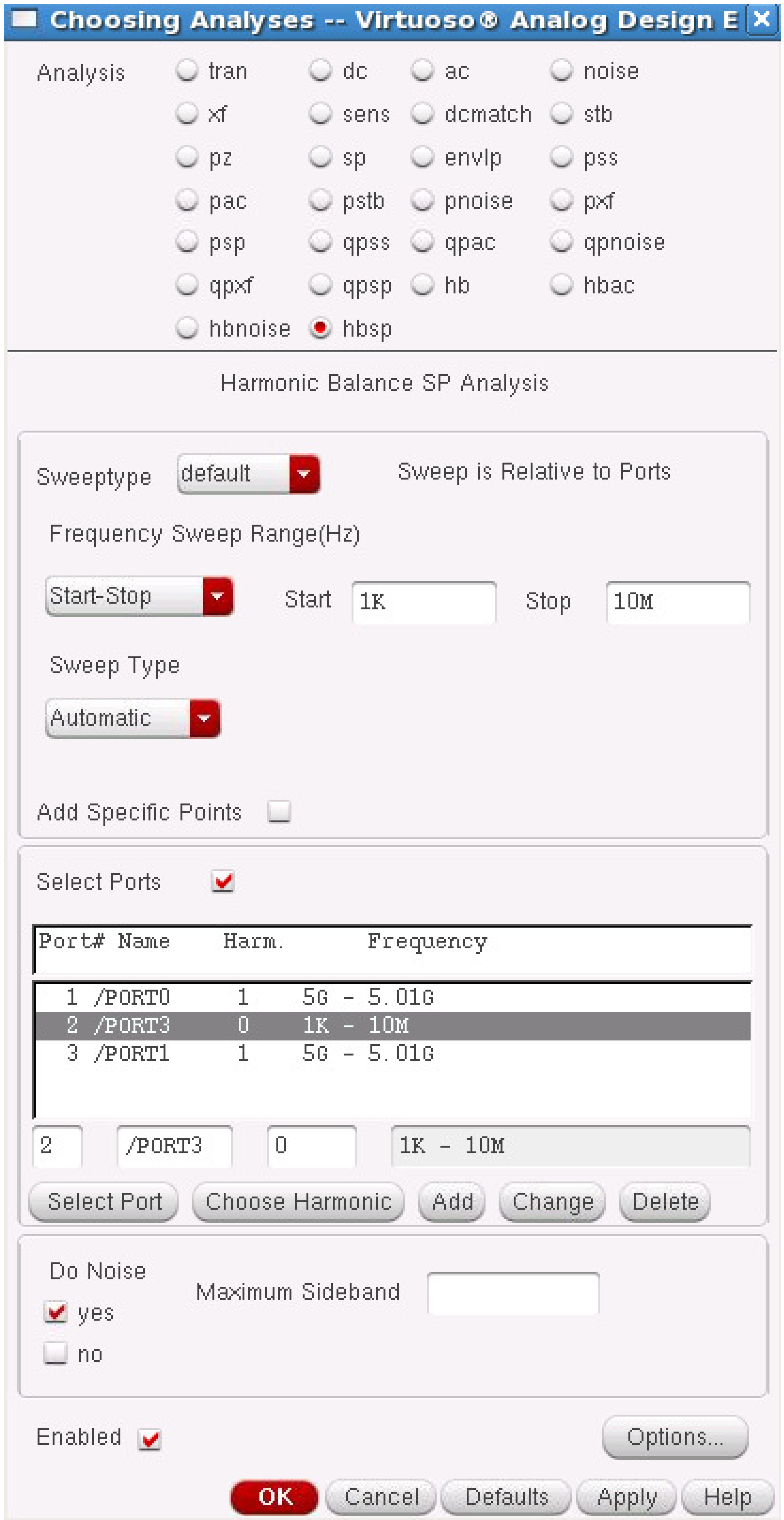
Action 5-6: You can choose **Session — Load State**, select **Cellview** in **Load State Option** and load state "**Lab5_SParameter_hbsp**" and skip to Action 5-11 or …

Action 5-7: In the Virtuoso Analog Design Environment window, choose **Analyses — Choose**.

Action 5-8: In the Choosing Analyses window, select the *hb* button in the *Analysis* field of the window. Set the form as follows:

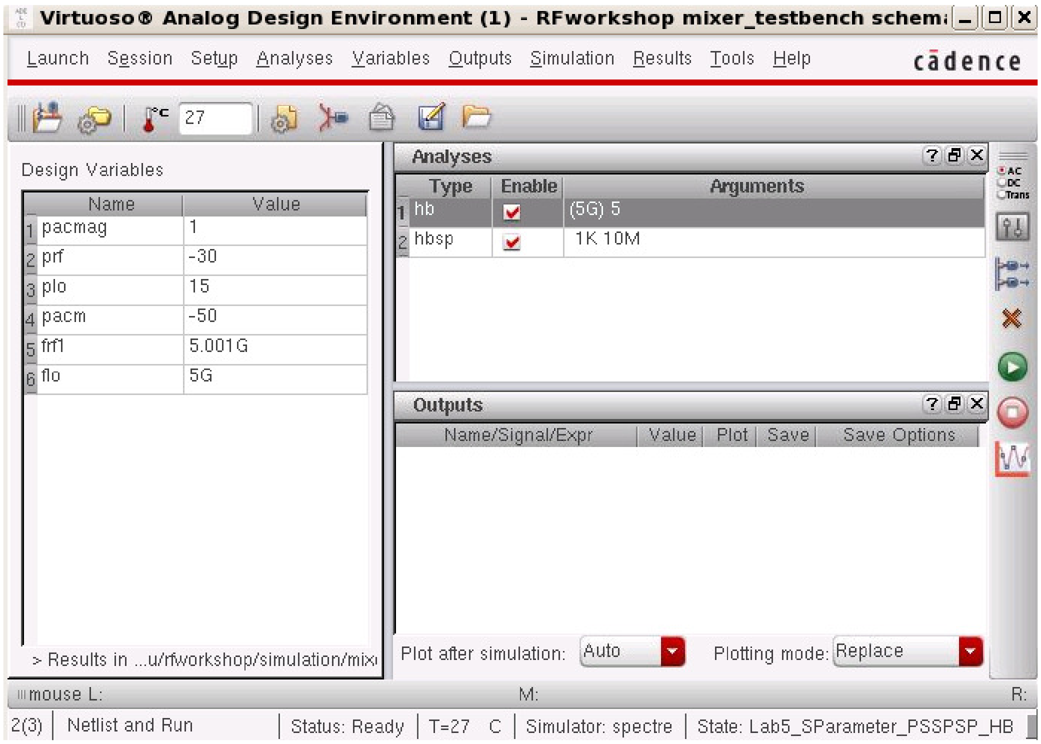


Action 5-9: In the Choosing Analyses window, select the *hbsp* button in the *Analysis* field of the window and set the form as follows:



Action 5-10: Make sure the *Enabled* button is on. In the Choosing Analyses window, click *OK*.

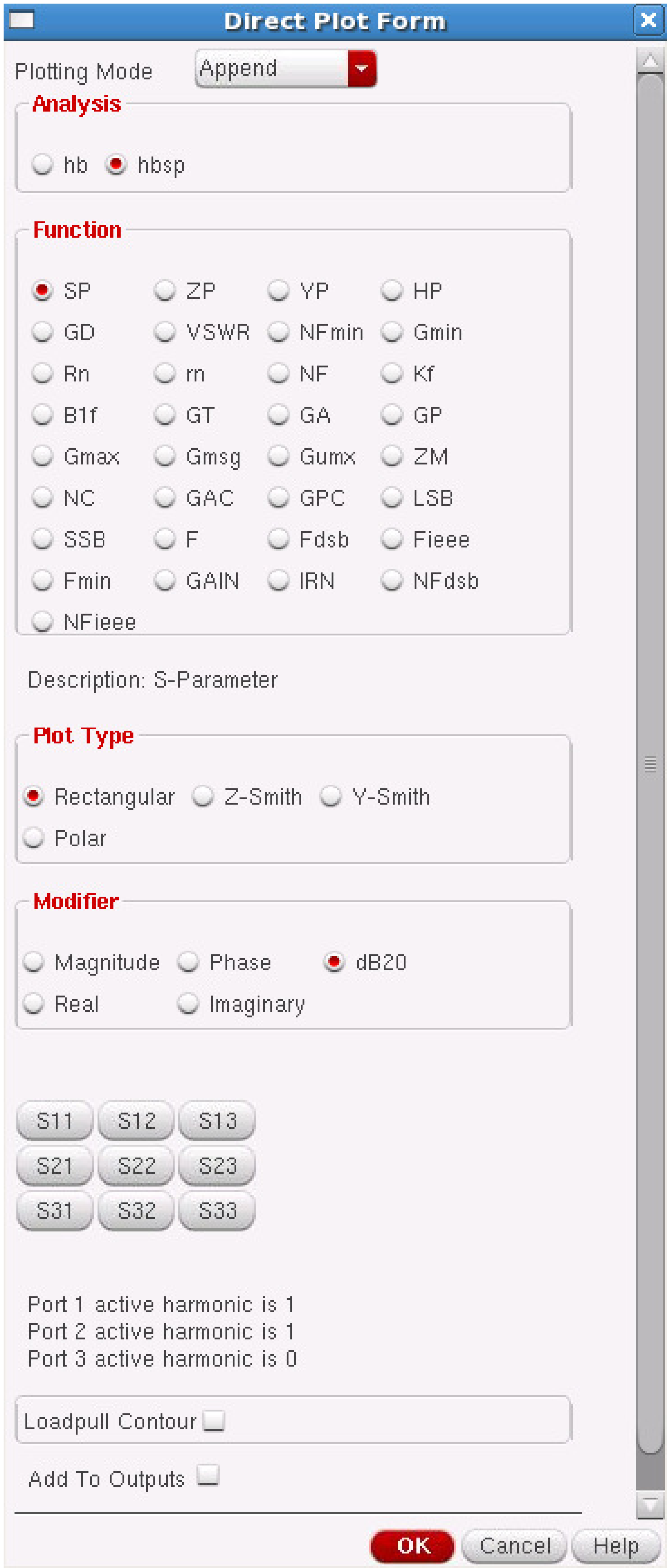
The Virtuoso Analog Design Environment window looks like this.



Action 5-11: In the Virtuoso Analog Design Environment window, choose **Simulation — Netlist and Run** or click the **Netlist and Run** icon to start the simulation.

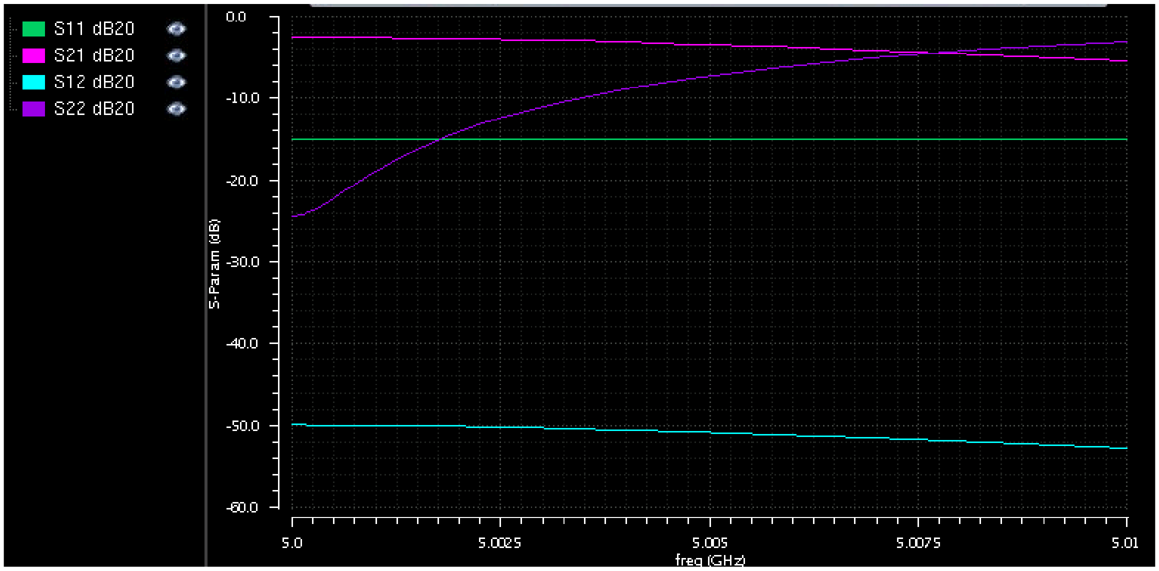
Action 5-12: After the simulation completes, in the Virtuoso Analog Design Environment window, choose **Results — Direct Plot — Main Form**.

Action 5-13: In the Direct Plot Form, select the *hbsp* button and configure the form as follows:


Direct Plot Form
Plotting Mode Append
Analysis
hb hbsp
Function
SP ZP YP HP
GD VSWR NFmin Gmin
Rn rn NF Kf
B1f GT GA GP
Gmax Gmsg Gumx ZM
NC GAC GPC LSB
SSB F Fdsb Fieee
Fmin GAIN IRN NFdsb
NFieee
Description: S-Parameter
Plot Type
Rectangular Z-Smith Y-Smith
Polar
Modifier
Magnitude Phase dB20
Real Imaginary
S11 S12 S13
S21 S22 S23
S31 S32 S33
Port 1 active harmonic is 1
Port 2 active harmonic is 1
Port 3 active harmonic is 0
Loadpull Contour
Add To Outputs
OK Cancel Help

Action 5-14: In the Direct Plot Form, click S11, S21, S12, and S22.

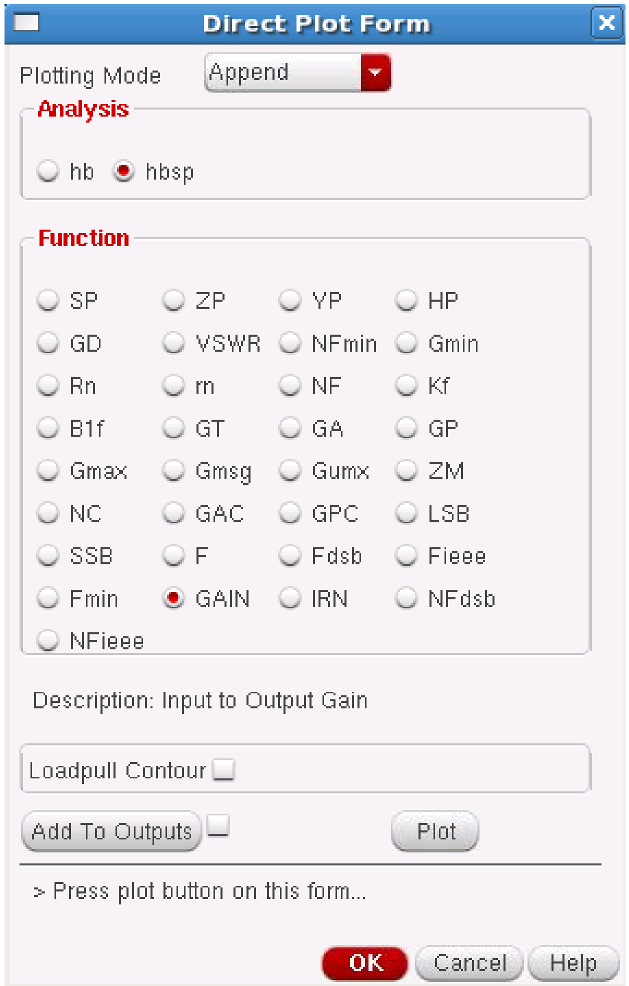
The waveform window appears:



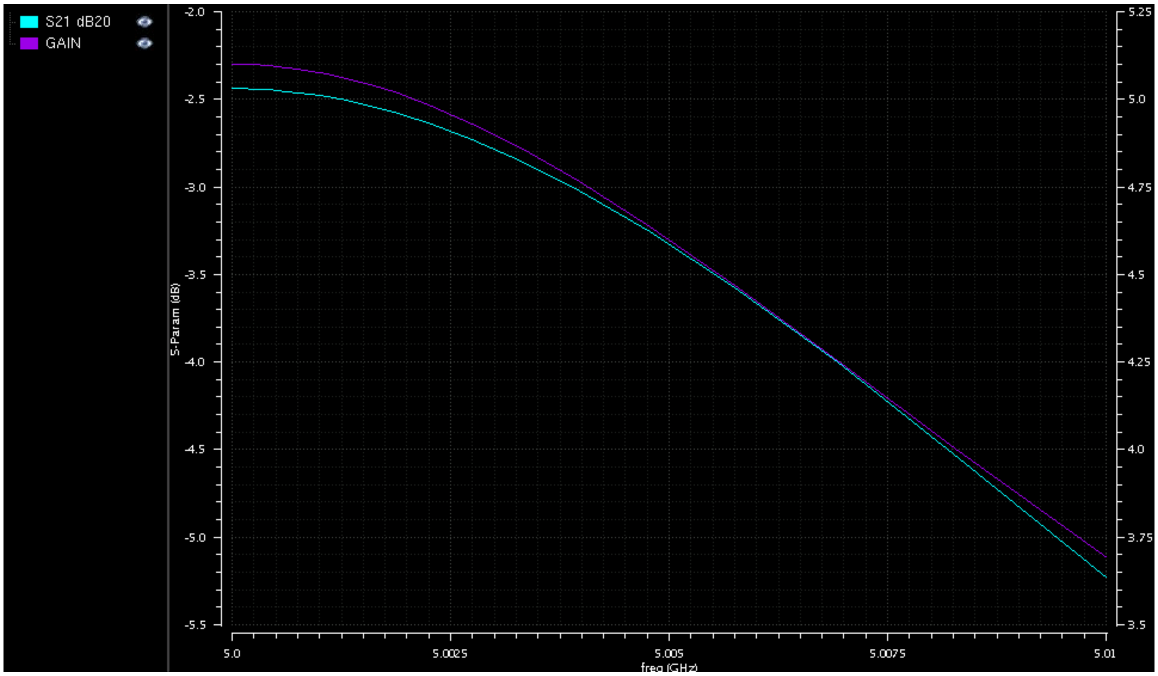
Action 5-15: Close the waveform window.

Action 5-16: In the Direct Plot Form, choose the *sp* function, set the *Plot Type* to *Rectangular* and *Modifier* to *dB20*. Plot S21.

Action 5-17: In the Direct Plot Form, choose *GAIN*.



Action 5-18: Click *Plot*. The waveform window appears with the following plot:



Action 5-19: Close the waveform window. Click *Cancel* in the Direct Plot Form.

hbsp GAIN differs from the hbsp S21 gain and the Pnoise gain because hbsp GAIN is independent of input match (determined by the impedance of the RF port). hbsp S21 and Pnoise gains vary depending on the input match. hbsp GAIN is the voltage gain from the internal port voltage source to the output. For more information, see the SpectreRF user guide Appendix L (using psp and pnoise analysis).

Lab 6: Noise, Noise Summary and Noise Separation (hb and hbnoise)

Because the noise from the mixer is moderated by the LNA's gain, it places a limit on how small a signal can be resolved. The sensitivity of the receiver is then adversely affected. Noise is measured using the noise figure (NF), which is a measure of how much noise the mixer adds to the signal relative to the noise that is already present in the signal. An NF of 0 dB is ideal, meaning that the mixer adds no noise. An NF of 3 dB implies that the mixer adds an amount of noise equal to that already present in the signal. For a mixer alone, an NF of 15 dB is typical.

Running the hb and hbnoise analyses produces all the needed information, including the total output noise and the noise figure.

Action 6-1: If it is not already open, open the *schematic* view of the *mixer_testbench* design in the library *RFworkshop*.

Action 6-2: Select the `PORT0` source and set the *Source type* to *dc*. Select `PORT3` and set the *Source type* to *dc*. Set `PORT1` and set the *Source type* to *sine*.

Action 6-3: Check and save the schematic.

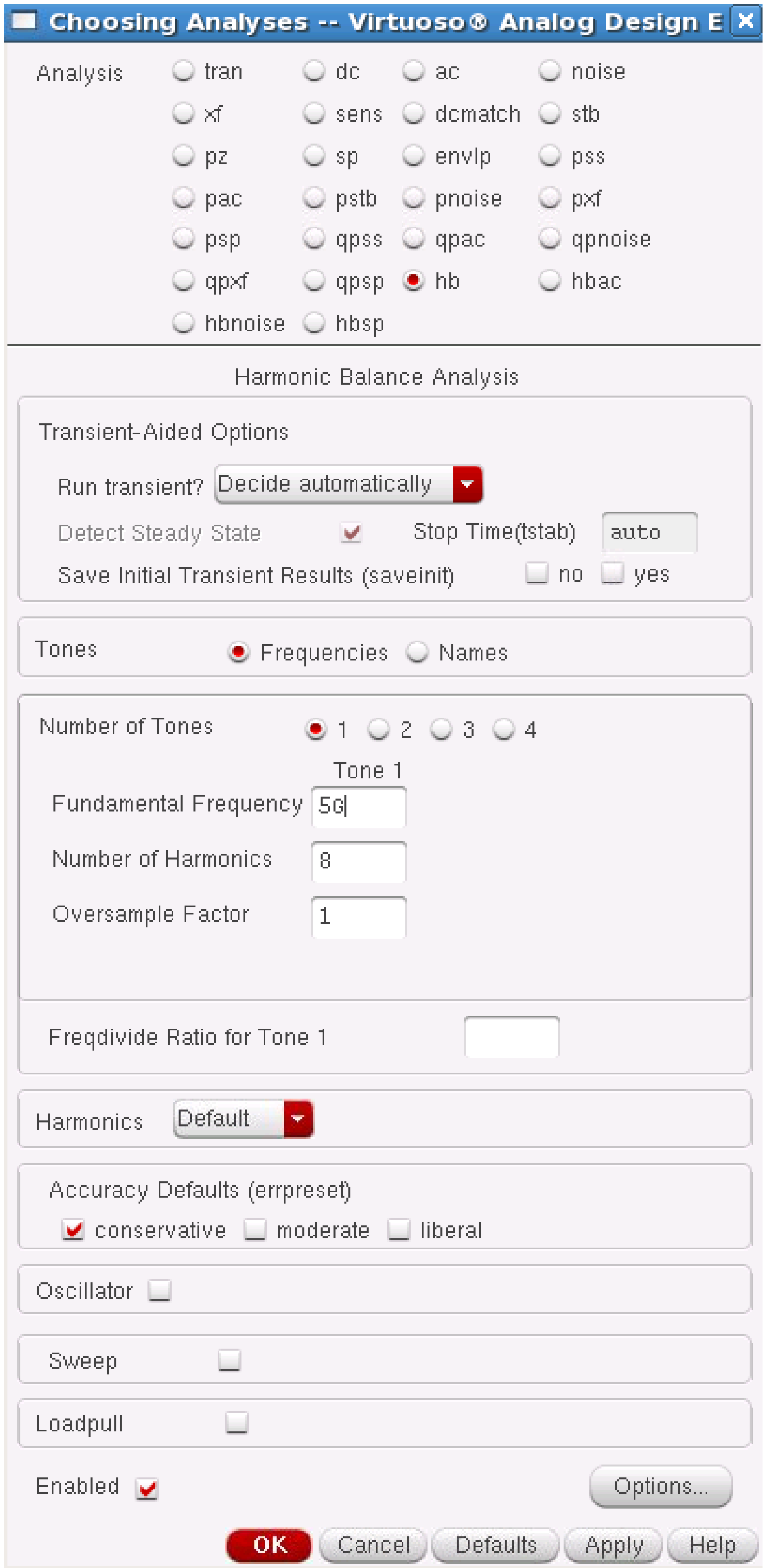
Action 6-4: From the *Mixer_testbench* schematic, choose **Launch — ADE L.**

The Virtuoso Analog Design Environment window appears.

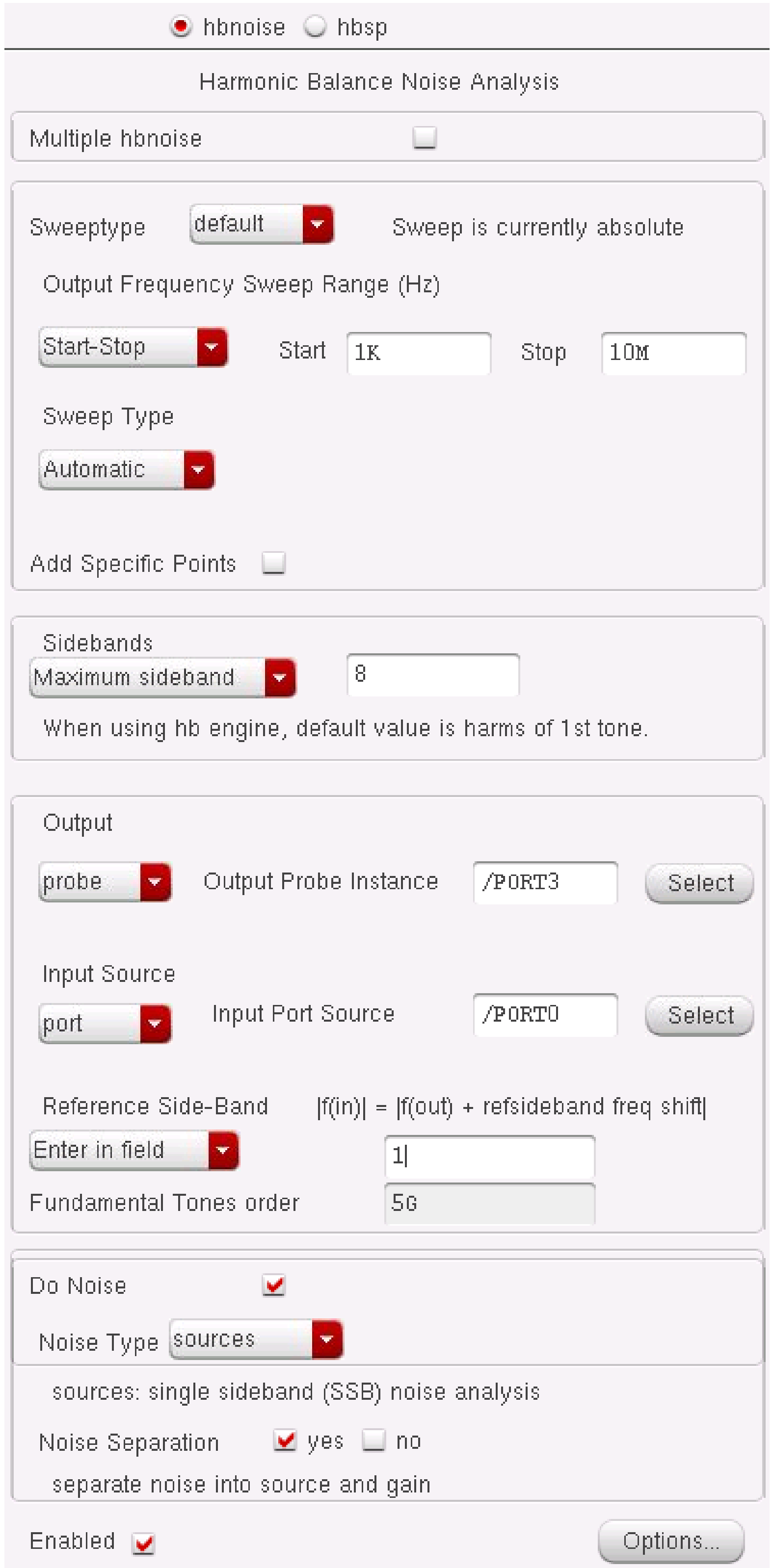
Action 6-5: You can choose **Session — Load State**, select **Cellview** in **Load State Option** and load state "**Lab6_hbnoise**" and skip to Action 6-10 or …

Action 6-6: In the Virtuoso Analog Design Environment window, choose **Analyses — Choose**.

Action 6-7: In the Choosing Analyses window, select the *hb* button in the *Analysis* field of the window and set the form as follow:



Action 6-8: In the Choosing Analyses window, select the *hbnoise* button in the *Analysis* field of the window and set up the form as follows:

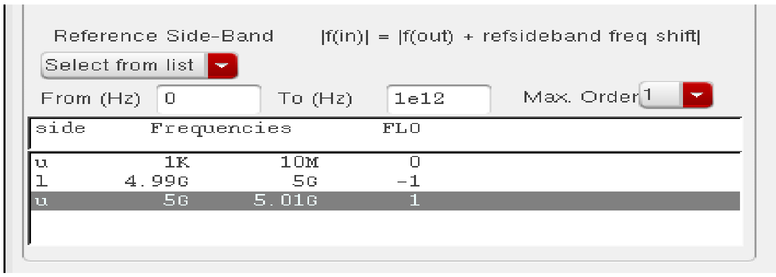


Note: You must specify the load as an output or probe. The load can be a resistor or a port. All noise from the source is included in the denominator of the noise factor fraction, including excess noise, so do not specify excess noise on the input port. (Excess noise is specified with the *noisefile* or *noisevec* option.)

The refsideband can be determined by the following expression

|Fin| = |Fout + refsideband x Flo|

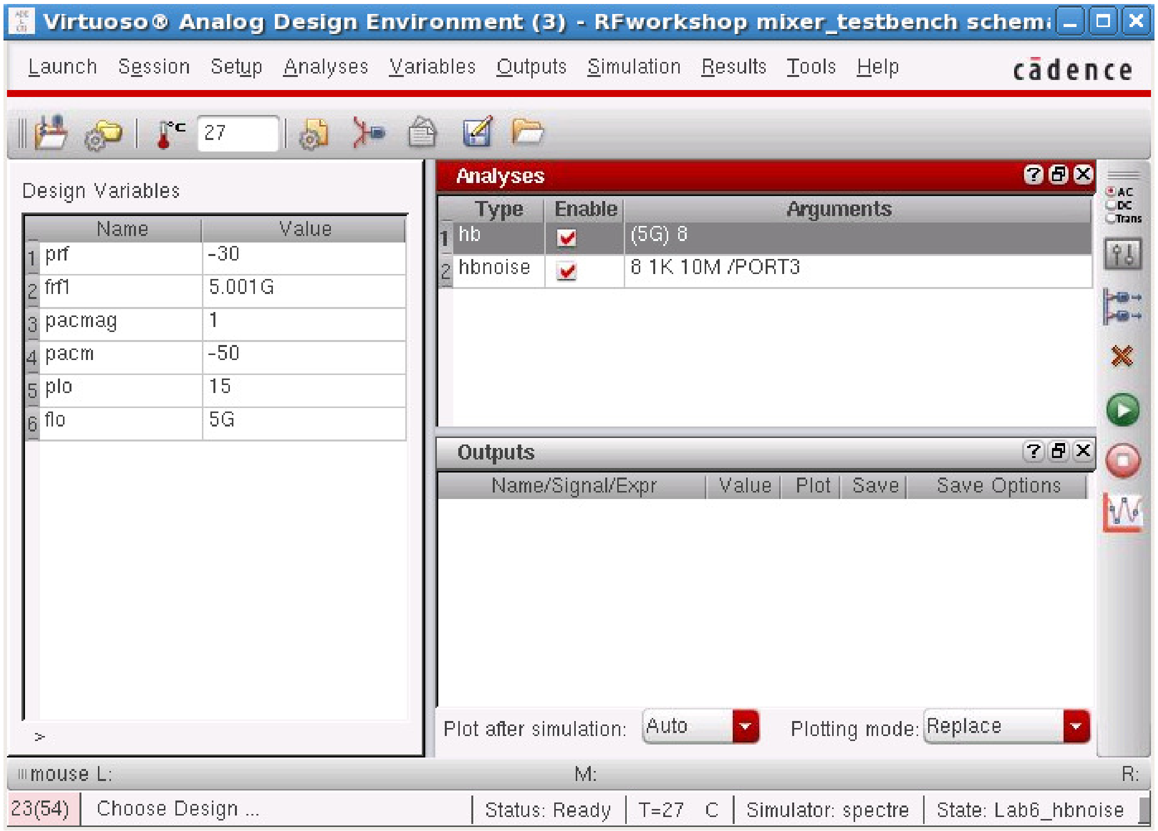
Or the user can use the *Select from list* option to select the corresponding input frequency range.



Also note that *Noise Separation* is set to *yes*. When the Pnoise simulation runs, the Pnoise separation feature is included during the simulation and the corresponding results are saved. This allows the user to get more information on how noise source and transfer function of each noise source contribute to the output noise.

If the design contains the multiple stages, the user can use multiple hbnoise on this form to calculate the noise at different points in the circuit.

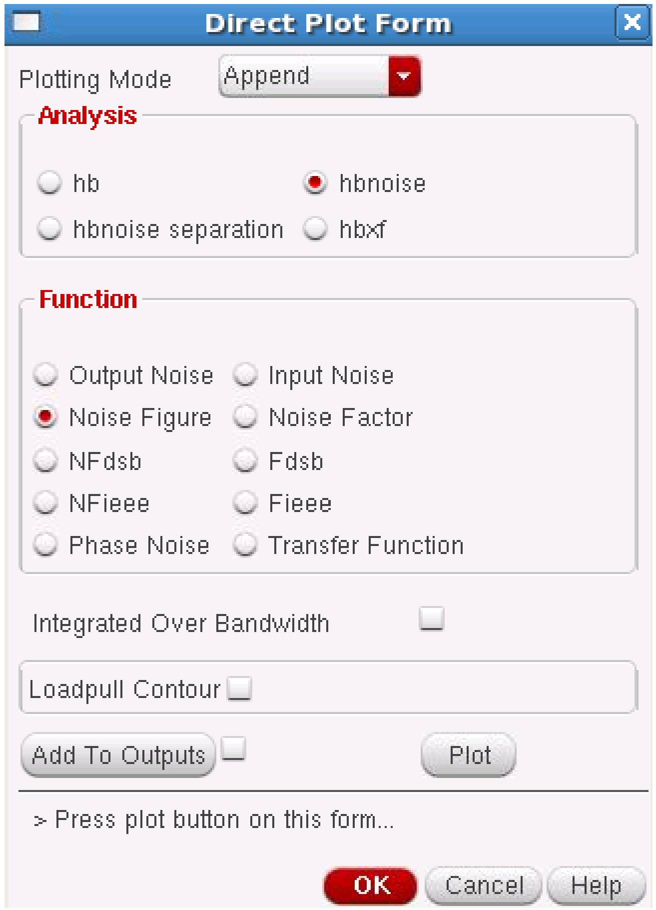
Action 6-9: Make sure the *Enabled* button is on. In the Choosing Analyses window, click *OK*. The Virtuoso Analog Design Environment window looks like this.



Action 6-10: In the Virtuoso Analog Design Environment window, choose **Simulation — Netlist and Run** or click the **Netlist and Run** icon to start the simulation.

Action 6-11: In the Virtuoso Analog Design Environment window, choose **Results — Direct Plot — Main Form**.

Action 6-12: In the Direct Plot Form, select the *hbnoise* button, and configure the form as follows:

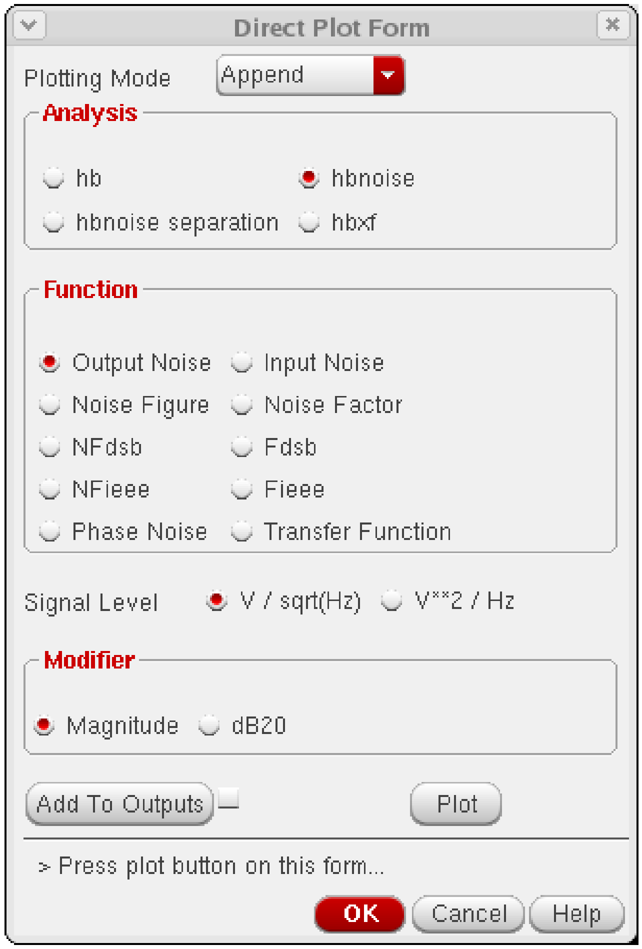


Action 6-13: Click **Plot**.

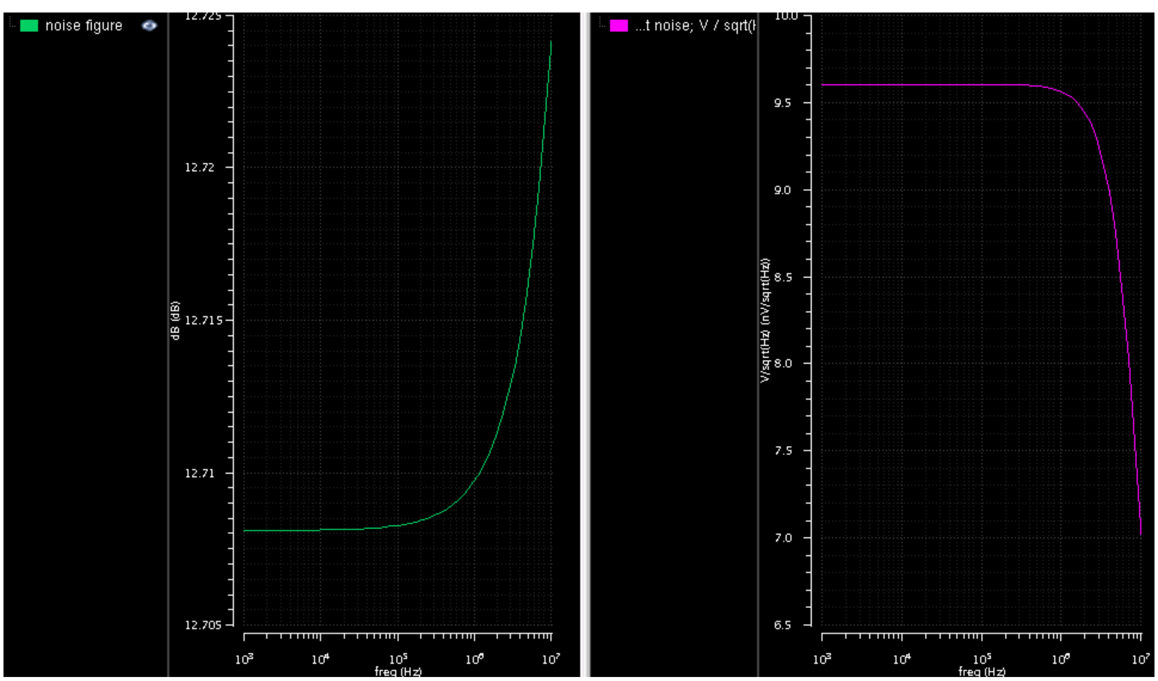
The waveform window appears.

Action 6-14: In the Direct Plot Form window, click **New Subwindow**.

Action 6-15: Set the *Function* to *Output Noise* and configure the rest of the form as follow:



Action 6-16: Click *Plot*. The waveform window appears.



Action 6-17: After viewing the waveforms, click *Cancel* in the Direct Plot Form.

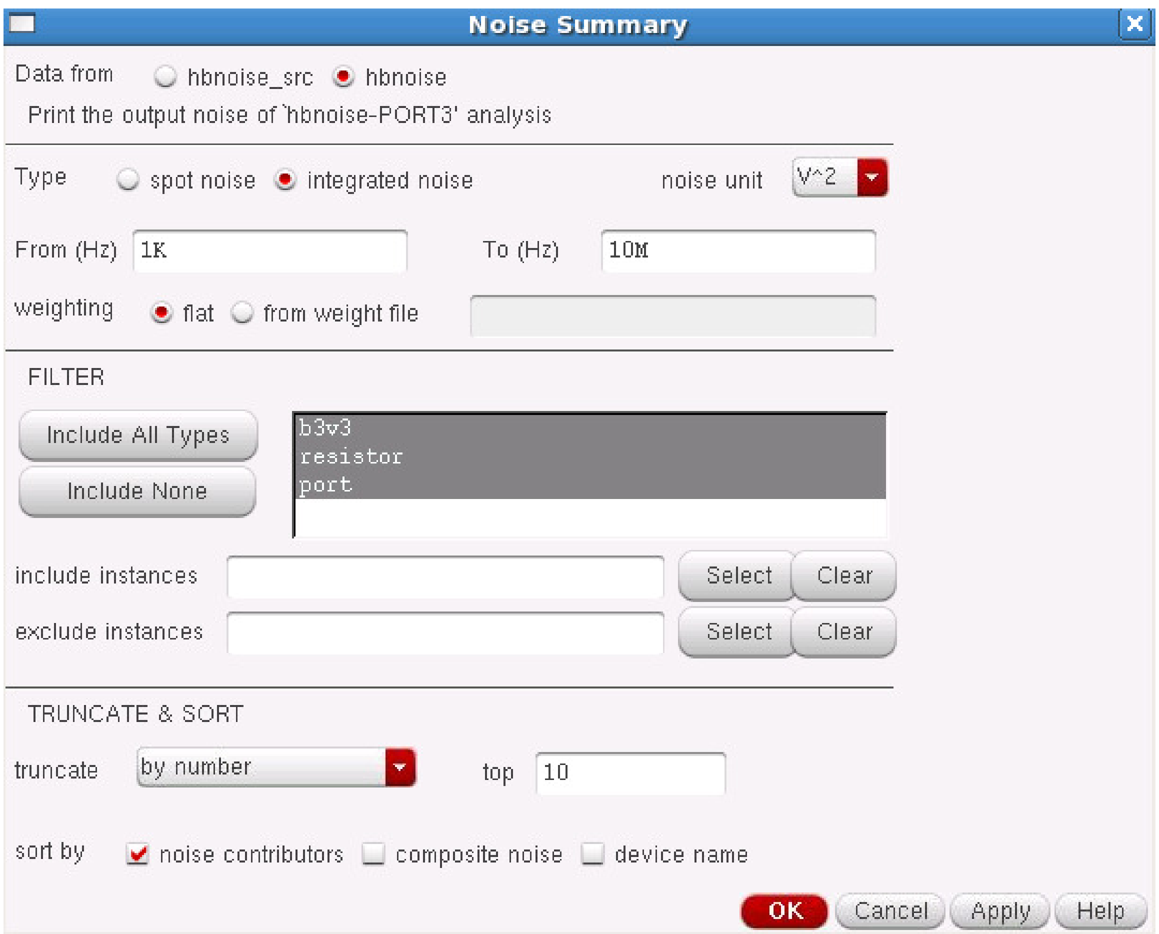
It is valuable to know the main contributors of noise in a system, after the noise performance of the circuit is calculated. This information is readily available from a Pnoise simulation.

Action 6-18: In the Virtuoso Analog Design Environment window, choose **Results — Print — Noise Summary**.

The Noise Summary form appears.

Action 6-19: Fill in the form as shown here.

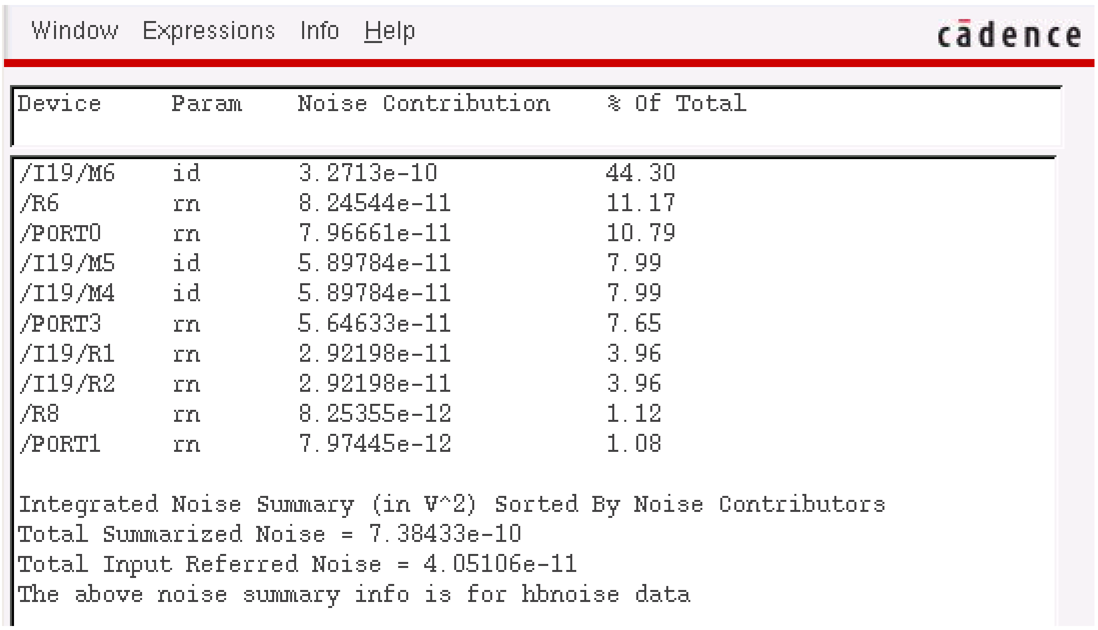
Note: The Noise Summary form includes both a *hbnoise* and a *hbnoise_src* choice. The *hbnoise_src* form and the fill, filter, and truncate methods are the same as those used in the *hbnoise* form.



Action 6-20: Click the *Include All Types* button in the FILTER section.

Action 6-21: Click *OK* in the Noise Summary form.

The Results Display Window appears.



Window Expressions Info Help

Device	Param	Noise Contribution	% Of Total
/I19/M6	id	3.2713e-10	44.30
/R6	rn	8.24544e-11	11.17
/PORT0	rn	7.96661e-11	10.79
/I19/M5	id	5.89784e-11	7.99
/I19/M4	id	5.89784e-11	7.99
/PORT3	rn	5.64633e-11	7.65
/I19/R1	rn	2.92198e-11	3.96
/I19/R2	rn	2.92198e-11	3.96
/R8	rn	8.25355e-12	1.12
/PORT1	rn	7.97445e-12	1.08

Integrated Noise Summary (in V^2) Sorted By Noise Contributors
Total Summarized Noise = 7.38433e-10
Total Input Referred Noise = 4.05106e-11
The above noise summary info is for hbnoise data

Action 6-22: After viewing the results, choose **Window — Close** to close the window.

You can use SpectreRF to quickly locate the noise sources that cause the most noise to the output. The basic flow is:

[1] Direct Plot Form

[2] Pnoise/Qpnoise/hbnoise Separation

[3] Sideband Output

Here you decide which sidebands contribute more output noise.

[4] Instance Output

Here you decide which instances contribute more output noise to the selected sideband.

[5] Source Output

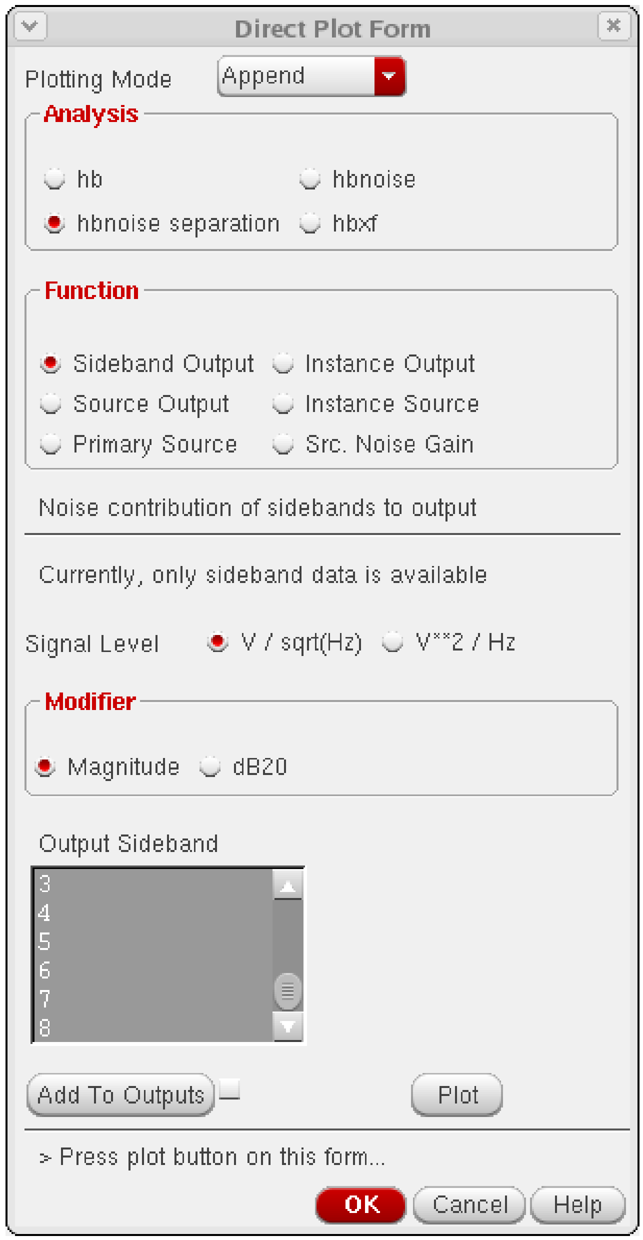
Here you decide which primary sources contribute more output noise to the filtered and truncated instances.

[6] Instance Source/Primary Source/Src. Noise gain

Here you determine which primary noise sources or gains have more effect on the output noise.

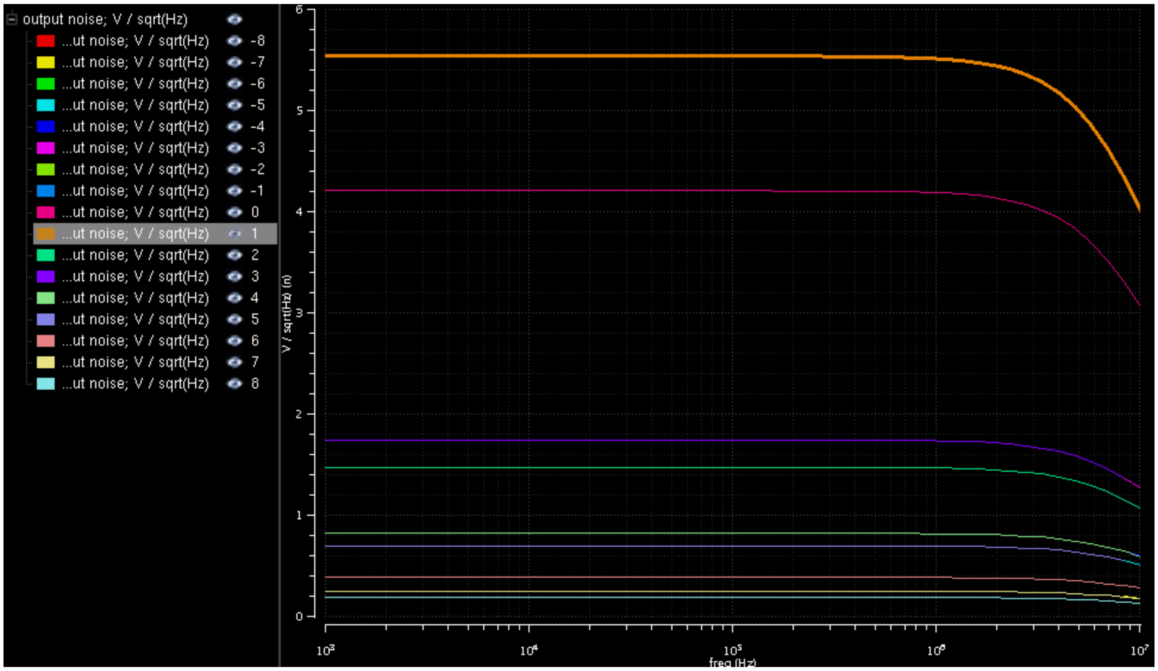
The steps of this flow are illustrated in the following actions.

Action 6-23: In the Direct Plot Form, select **hbnoise separation**, choose **Sideband Output**, and select the sidebands (from -8 to 8).



Action 6-24: Click **Plot**.

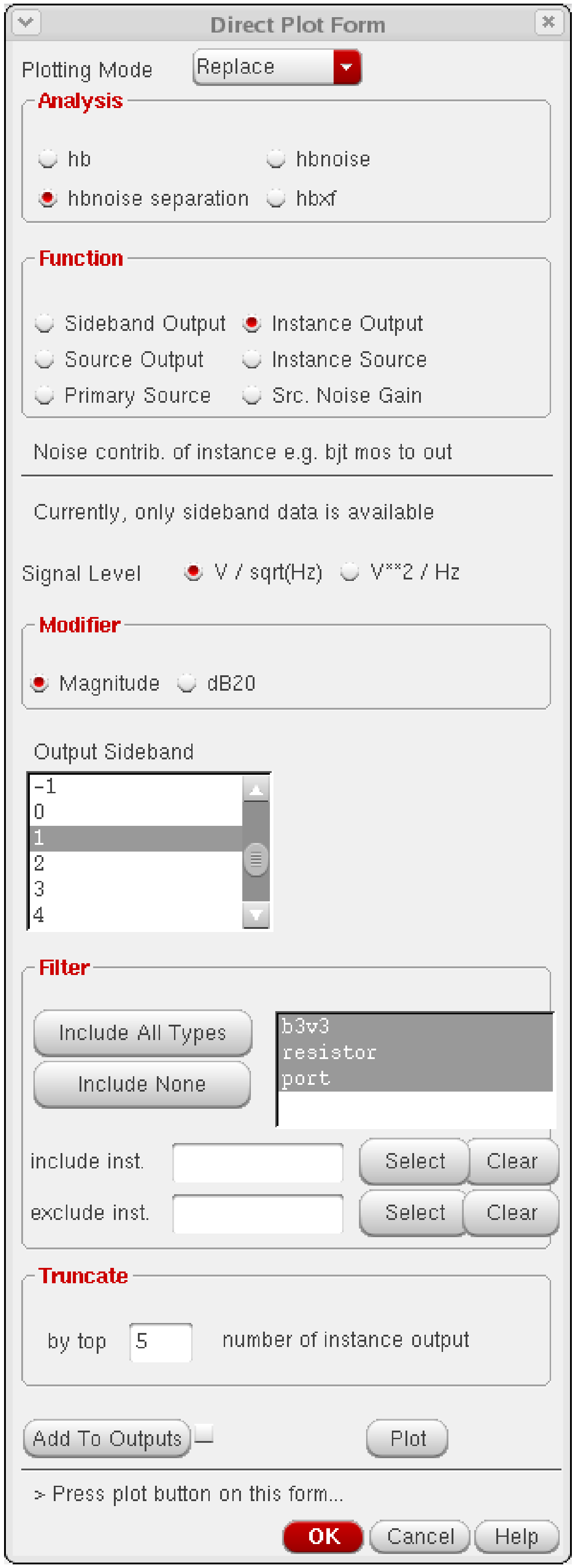
The waveform window appears with results as shown below:



Click the plus sign to the left of the label output noise in the upper left part of the waveform window.

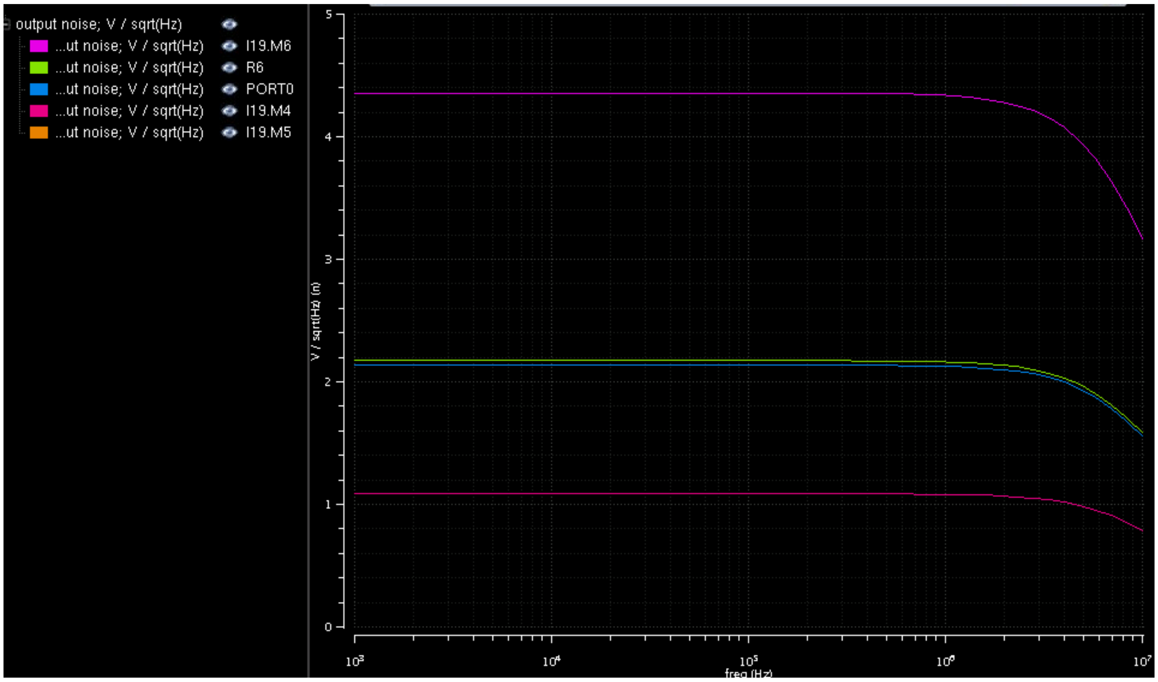
Select he highest amplitude curve. Note that the sidebband number reads 1.

Action 6-25: In the Direct Plot Form, set the *Plotting Mode* to *Replace*. Choose *Instance Output***.** Set *Output Sideband* as 1. Click *Include All Types*, and set *by top* to 5, then click Plot.


Direct Plot Form
Plotting Mode
Replace
Analysis
hb
hbnoise
hbnoise separation
hbxf
Function
Sideband Output
Instance Output
Source Output
Instance Source
Primary Source
Src. Noise Gain
Noise contrib. of instance e.g. bjt mos to out
Currently, only sideband data is available
Signal Level
V / sqrt(Hz)
V**2 / Hz
Modifier
Magnitude
dB20
Output Sideband
-1
0
1
2
3
4
Filter
Include All Types
Include None
b3v3
resistor
port
include inst.
exclude inst.
Select
Clear
Select
Clear
Truncate
by top
5
number of instance output
Add To Outputs
Plot
> Press plot button on this form...
OK
Cancel
Help

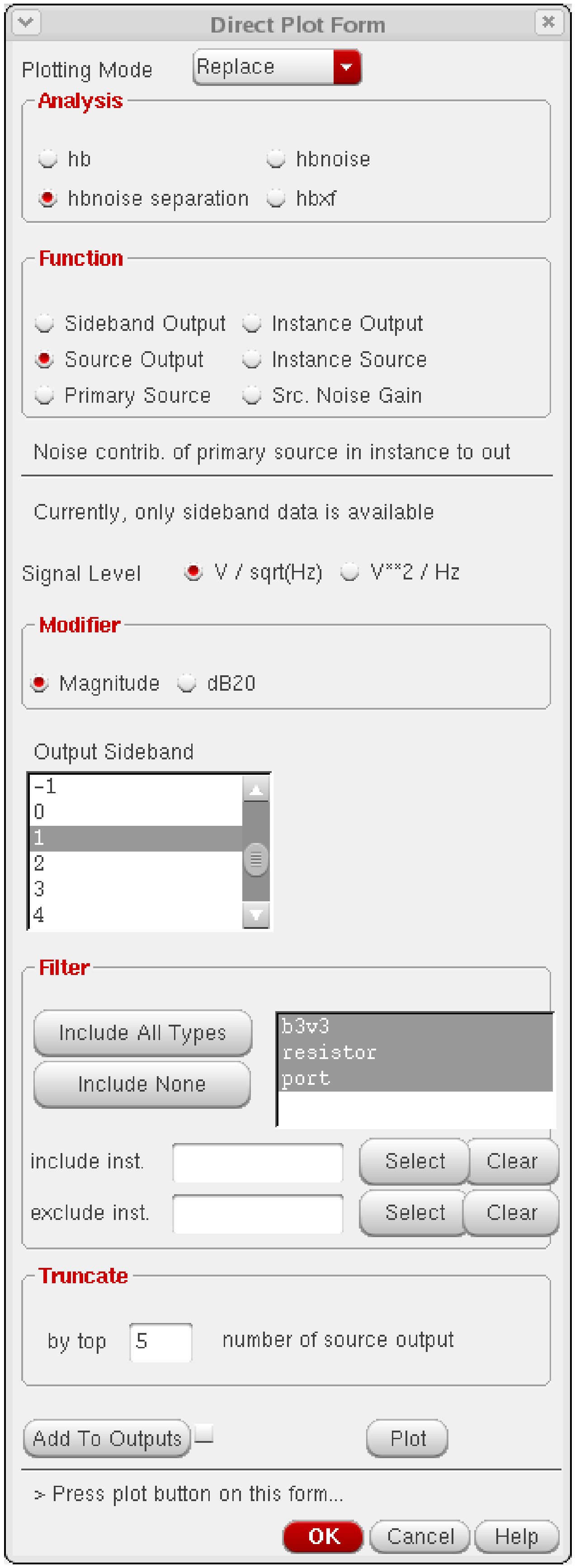
Action 6-26: Click **Plot**.

The result is shown below:



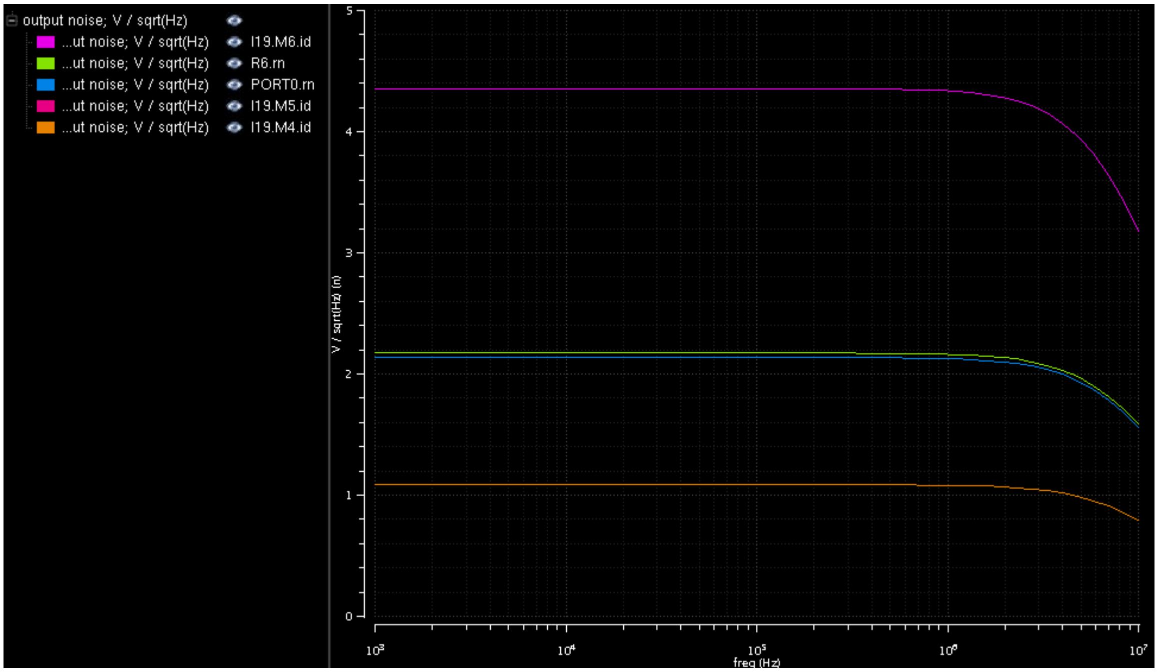
In this example, “I19.M6” contributes more output noise than the other instances.

Action 6-27: In the Direct Plot Form, set *Plotting Mode* to *Replace*. Choose *Source Output*. Set *Output Sideband* to 1, select *Include All Types*, and set *by top* to 5.


Direct Plot Form
Plotting Mode
Replace
Analysis
hb
hbnoise
hbnoise separation
hbxf
Function
Sideband Output
Instance Output
Source Output
Instance Source
Primary Source
Src. Noise Gain
Noise contrib. of primary source in instance to out
Currently, only sideband data is available
Signal Level
V / sqrt(Hz)
V**2 / Hz
Modifier
Magnitude
dB20
Output Sideband
-1
0
1
2
3
4
Filter
Include All Types
Include None
b3v3
resistor
port
include inst.
Select
Clear
exclude inst.
Select
Clear
Truncate
by top
5
number of source output
Add To Outputs
Plot
> Press plot button on this form...
OK
Cancel
Help

Action 6-28: Click **Plot**.

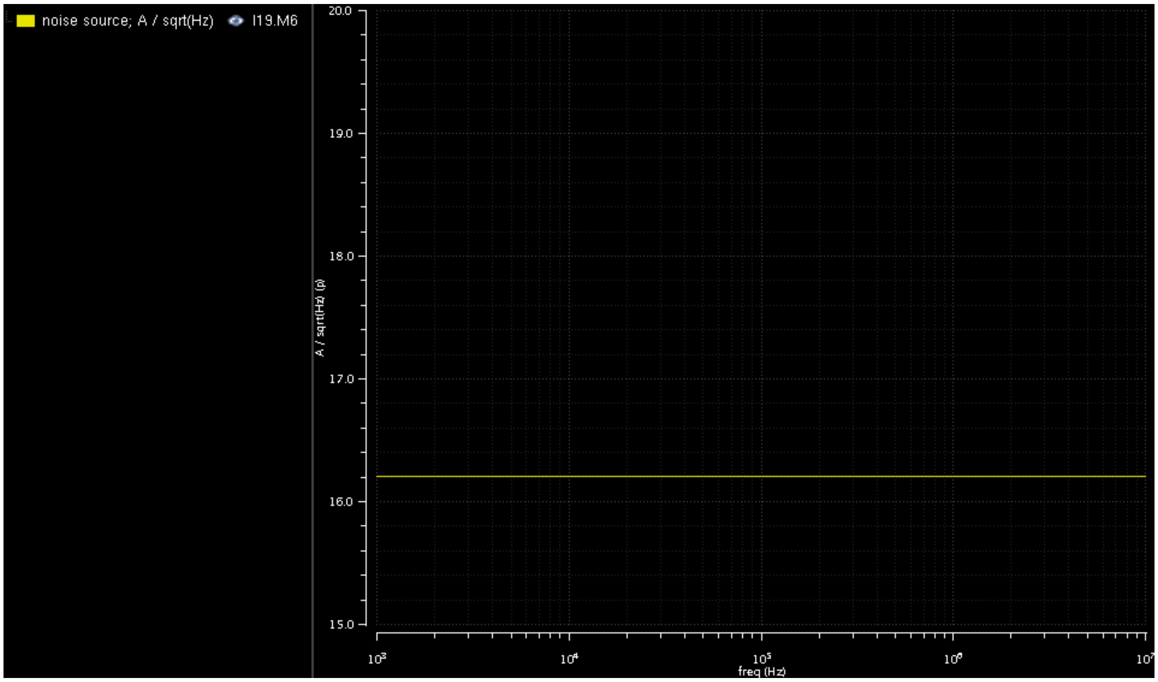
The result is shown below:



This plot shows that the thermal noise from the channel of I19.M6 is the largest noise contributor, followed by the thermal noise of the resistor R6. Note that the list order of the instances in this plot is different from that of **instance output**.

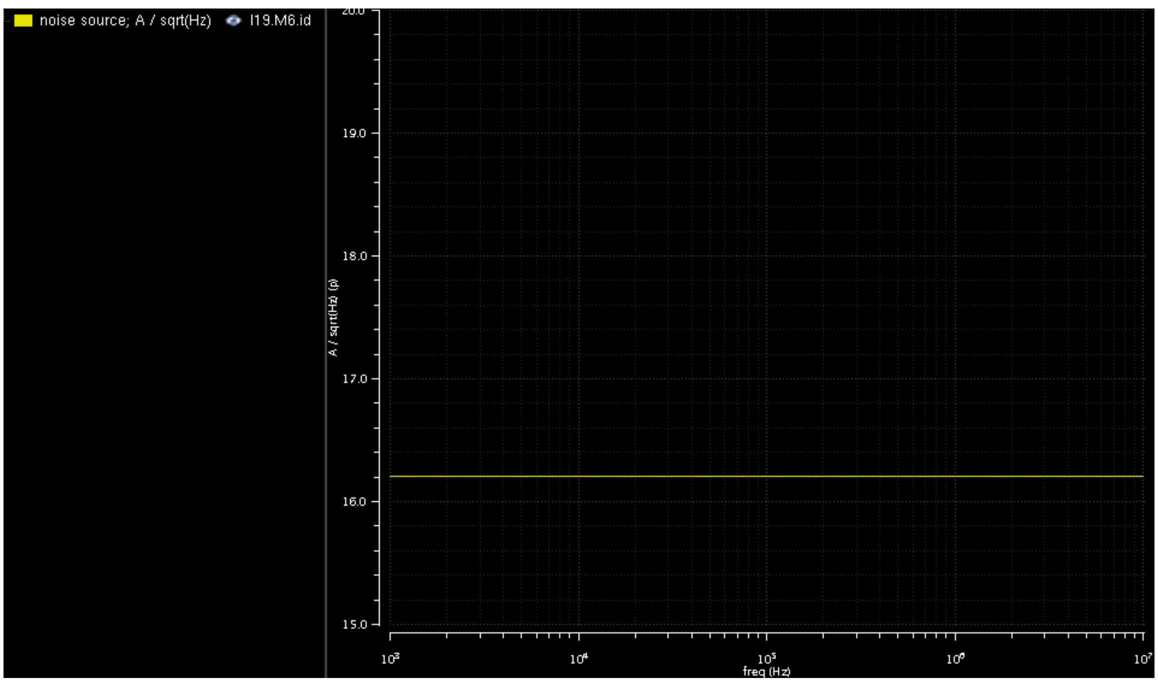
Action 6-29: In the Direct Plot Form, choose *Instance Source*. Set *by top* to 1**.** Click *Plot* to plot the noise source measurement of instance “I19.M6”.

The result is shown below:



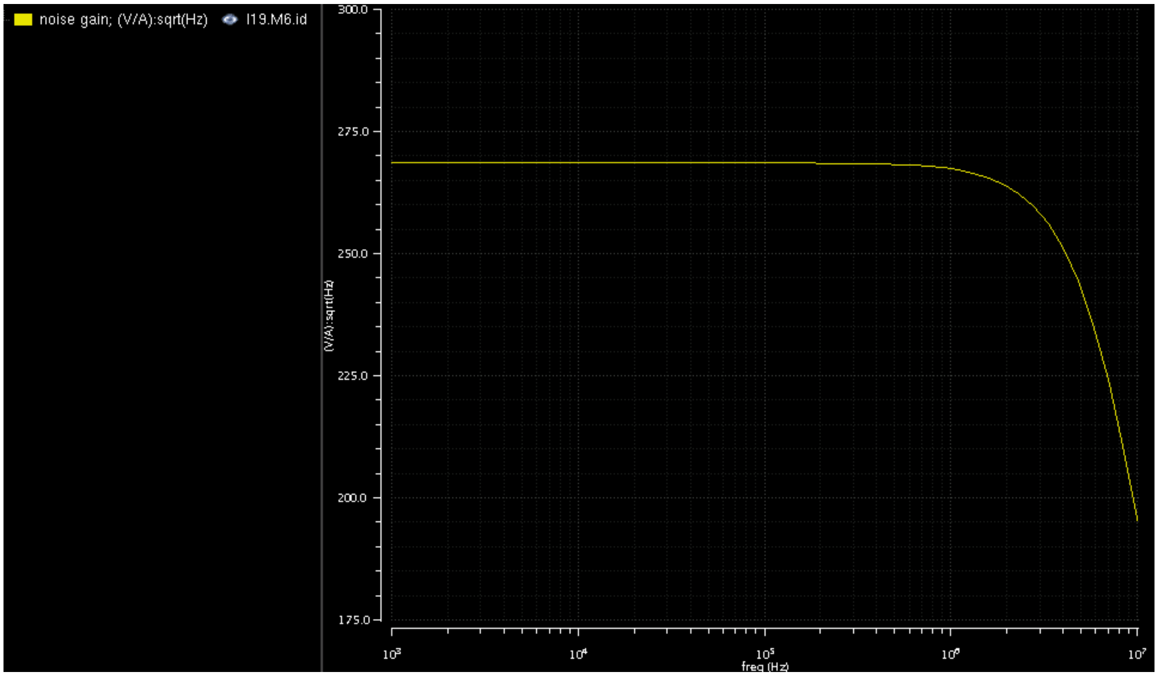
Action 6-30: In the Direct Plot Form, choose *Primary Source*. Set *by top* to 1. Click *Plot* to plot the noise source measurement of primary source in instance "I19.M6".

The result is shown below:



Action 6-31: In the Direct Plot Form, choose *Src. Noise Gain*. Set *by top* to 1. Click *Plot* to plot the noise gain from primary source in instance to output.

The result is shown below:



So to improve the noise performance of this circuit, decreasing the output noise of “I19.M6”is an effective solution. There are two approaches: one is decreasing the magnitude of noise source “I19.M6” by adjusting the device geometric size; the other is decreasing the transfer function of “I19.M6”by adjusting the circuit architecture.

Lab 7: Port-to-Port Isolation among RF, IF and LO Ports (hb and Swept hbac)

The isolation required between a mixer's ports depends on the circuit and the architecture of the product. Isolation is critical for the mixer to function properly.

You can combine PAC and PXF analyses to produce transfer functions from different ports to each other. One suggested configuration is to set up a PAC analysis with a nonzero pacmag parameter at the signal input (the RF port) and to set up a PXF analysis with the IF port as the output probe. This example uses pacmag = 1 for simplicity.

Action 7-1: If it is not already open, open the *schematic* view of the *mixer_testbench* design in the library *RFworkshop.*

Action 7-2: Use the mouse to select the `PORT0` source. Then, in the Virtuoso Schematic Editor, select **Edit — Properties — Objects**. The Edit Object Properties window for the port cell appears. Change the port properties as follows:

Parameter	**Value**
Resistance	50 ohm
Port Number	1
DC voltage	500 mV
Source type	*dc*
PAC Magnitude	*pacmag*

Action 7-3: Click *OK* on the Edit Object Properties window to close it.

Action 7-4: Set the *Source type* of `PORT1` to *sine*, and the *Source type* of `PORT3` to *dc*.

Action 7-5: Check and save the schematic.

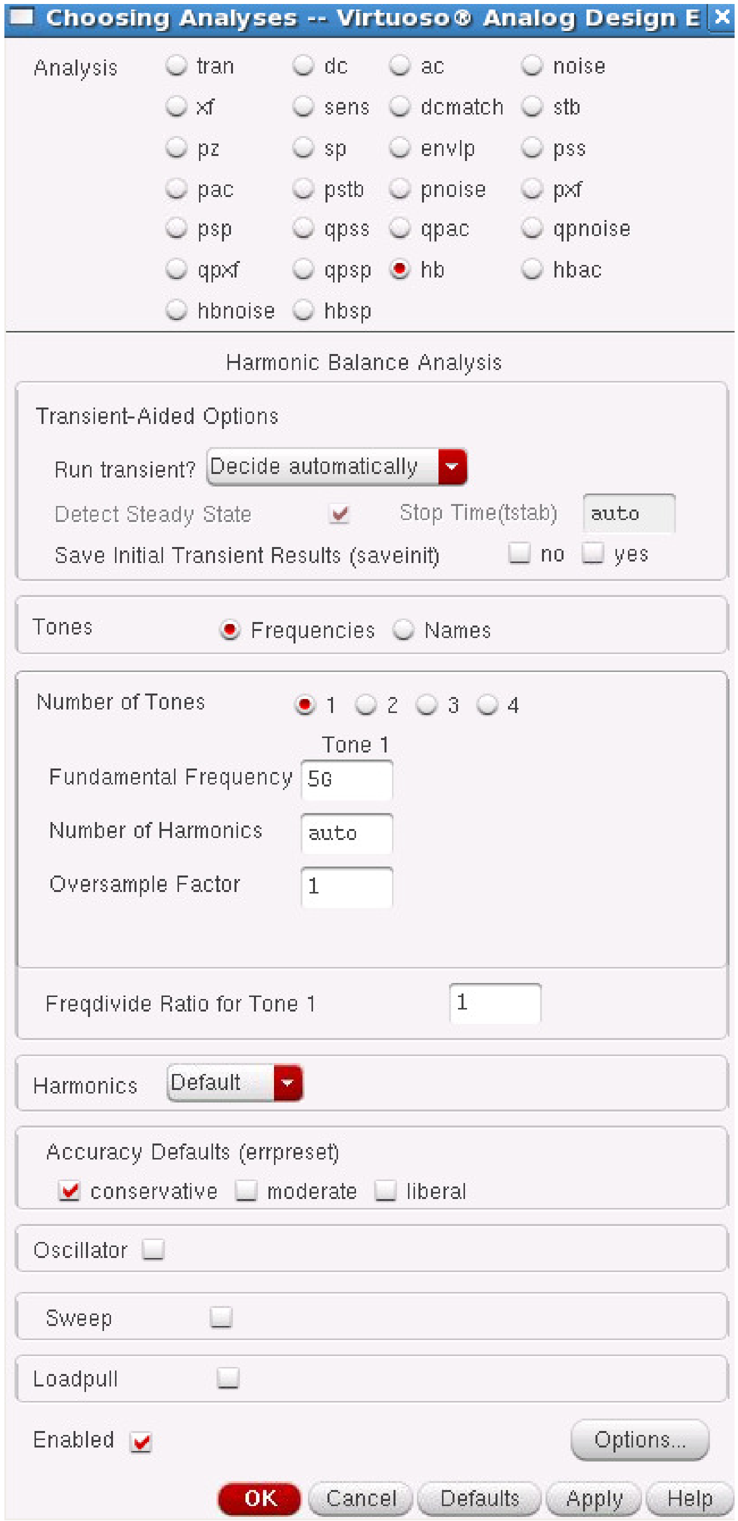
Action 7-6: From the *Mixer_testbench* schematic, choose **Launch — ADE L**.

The Virtuoso Analog Design Environment window appears.

Action 7-7: You can choose **Session — Load State**, select **Cellview** in **Load State Option** and load state “**Lab7_Isolation_hbac**” and skip to Action 7-14 or …

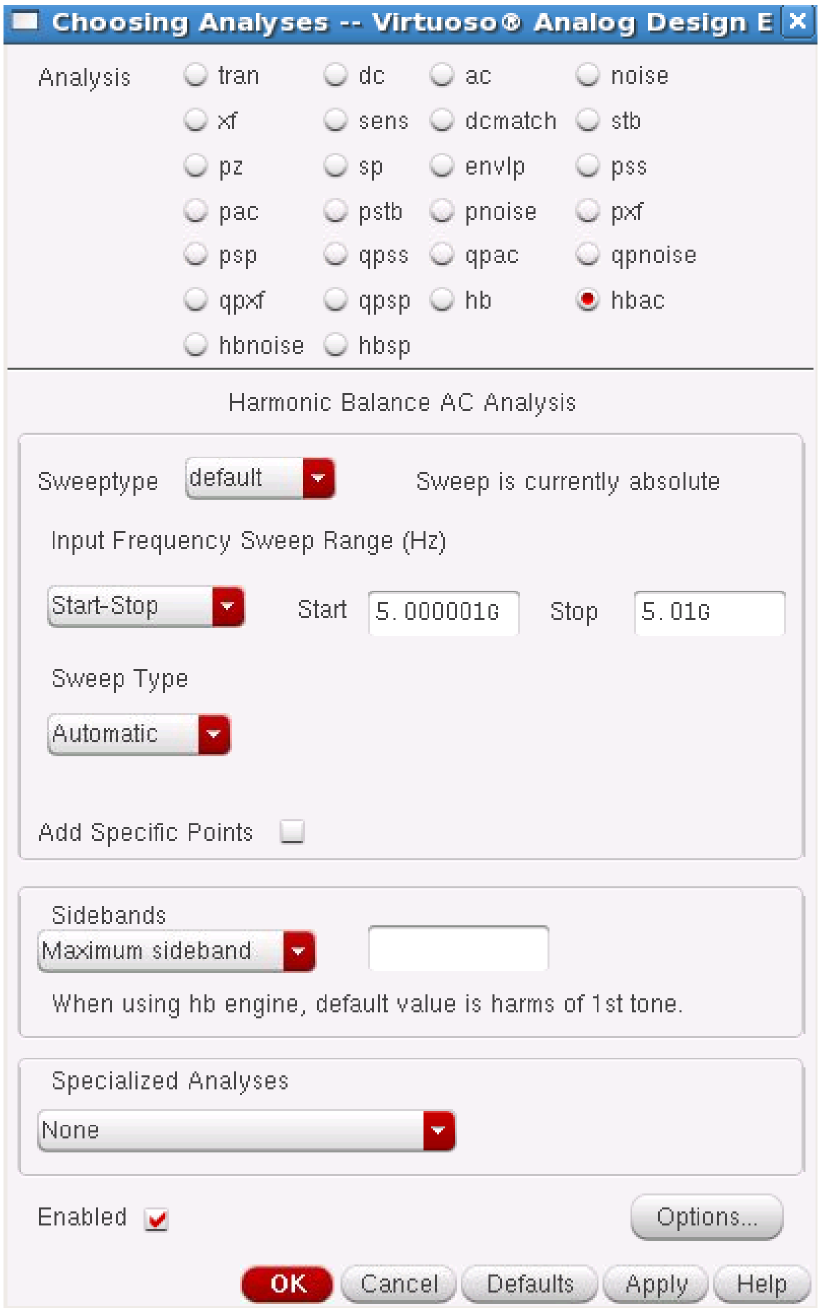
Action 7-8: In the Virtuoso Analog Design Environment window, choose **Analyses — Choose**.

Action 7-9: In the Choosing Analyses window, select the *hb* button in the *Analysis* field of the window. Set up the form as follows:



hb simulation is set up here to check the LO feedthrough. LO feedthrough is a large-signal effect and should not be measured using a small-signal analysis such as PXF. If you have a small RF conversion product and a large signal (LO) also, the large signal swamps the small-signal (RF) conversion product. Because there is no 1dB/dB relationship between the LO and IF, you will get an incorrect answer. It is therefore not recommended to use PXF to perform this measurement.

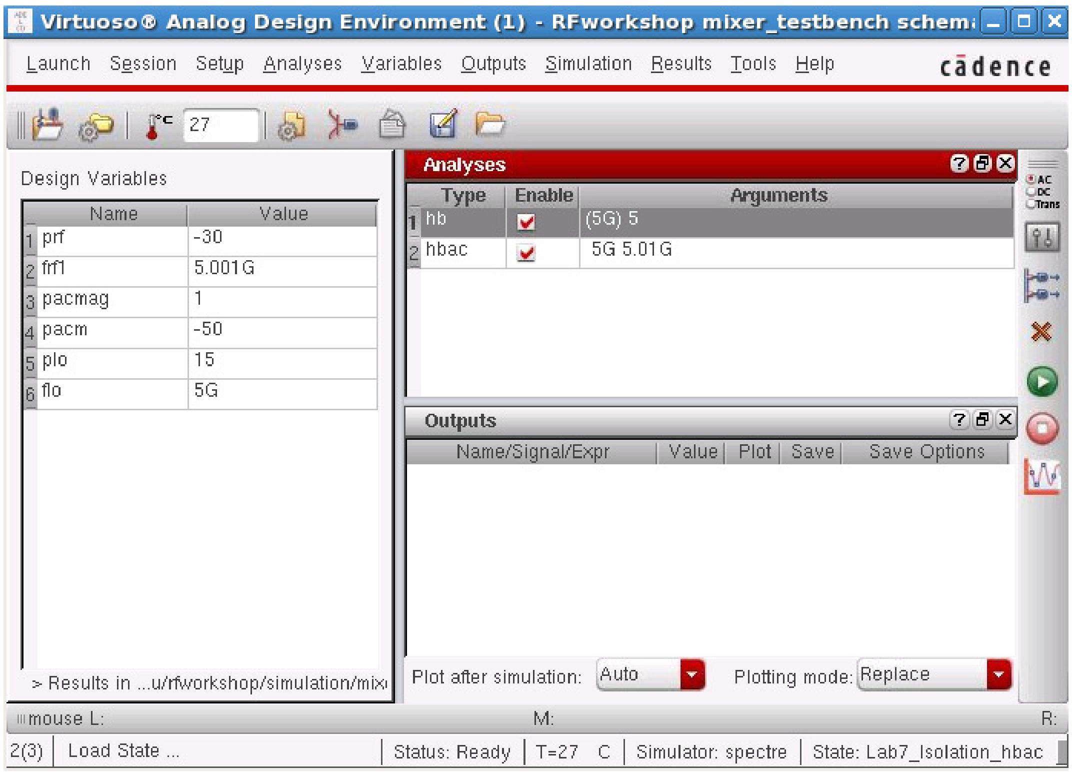
Action 7-10: In the Choosing Analyses window, select the *hbac* button in the *Analysis* field of the window. Set up the form as follows:



Action 7-11: Make sure the *Enabled* button is on. In the Choosing Analyses window, click *OK*.

PAC simulation is set up here to check the RF feed through.

The Virtuoso Analog Design Environment window looks like this.



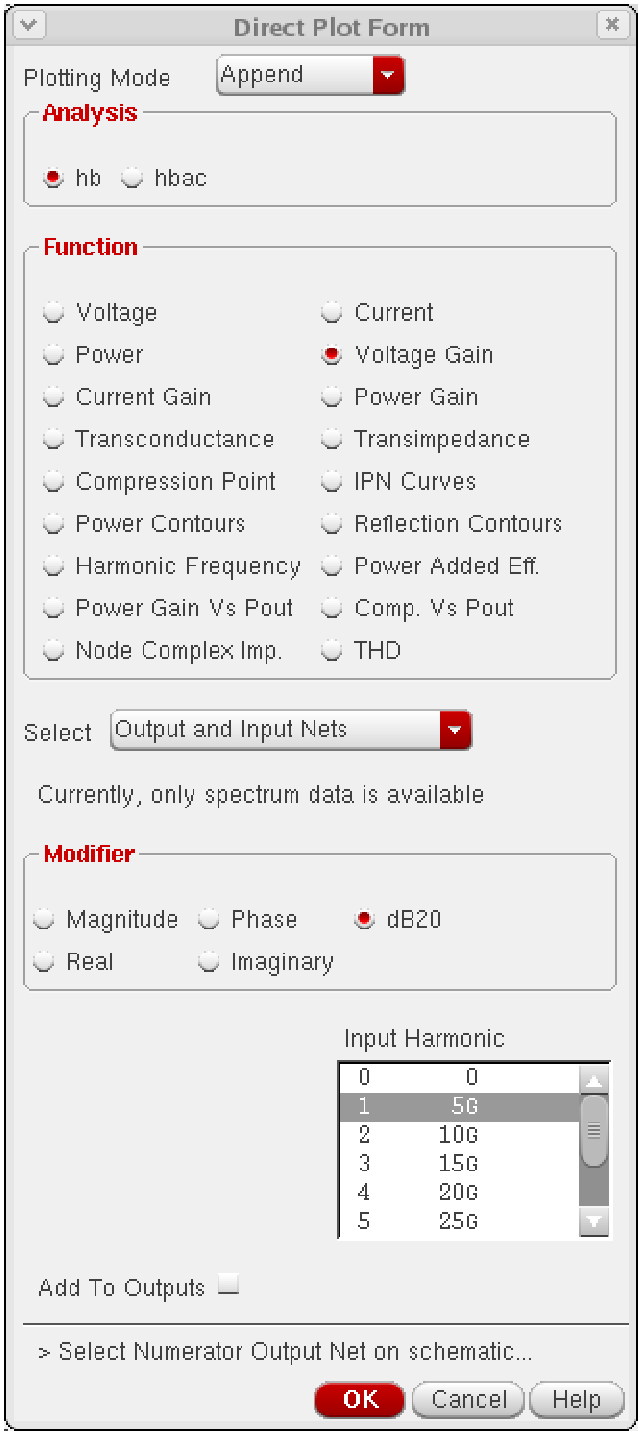
Action 7-12: In the Virtuoso Analog Design Environment, choose **Simulation — Netlist and Run** or click the **Netlist and Run** icon to start the simulation.

After the simulation runs, use the Direct Plot feature to plot the results.

To avoid desensitizing the stage following the mixer with high-level LO signal feedthrough to the output, measure LO-to-IF isolation. Use the results of the PSS analysis with the LO port as input and IF port as output to measure the level of isolation.

Action 7-13: In the Virtuoso Analog Design Environment window, choose **Results — Direct Plot — Main Form**.

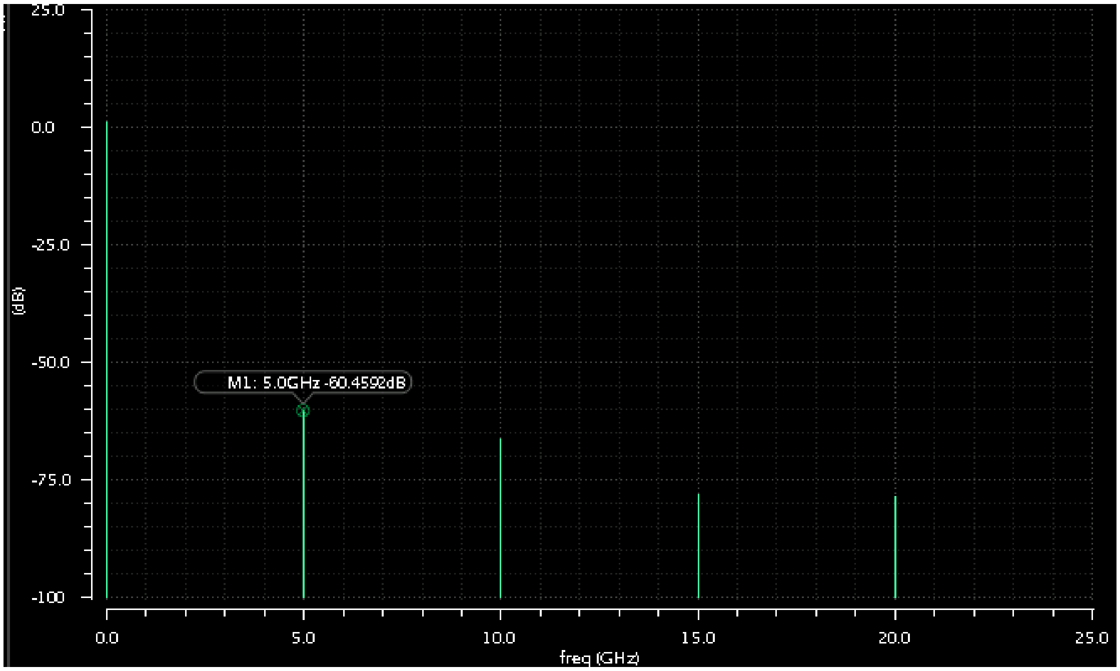
Action 7-14: In the Direct Plot Form, select the *hb* button, and configure the form as follows:



Action 7-15: In the schematic, select the net IFp as the output and net VLO as input.

Action 7-16: In the waveform window, choose **Marker — Place — Trace Marker** to place a marker at the first harmonic 5 GHz.

The following waveform shows the LO to IF feedthrough:



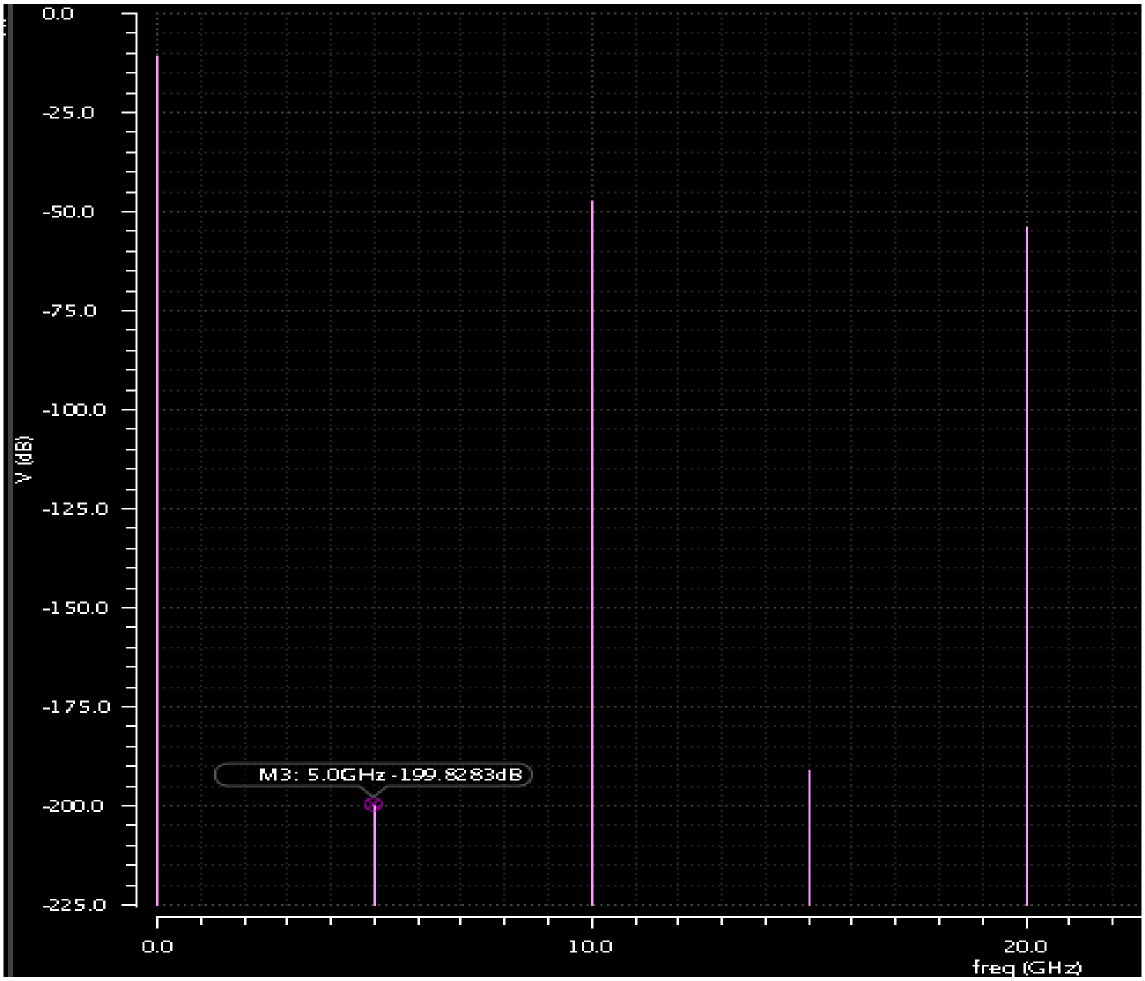
LO-to-RF feedthrough affects the functionality of LNAs and antennas and the self-mixing causes the dc offset. Use the results of the PSS analysis with the LO port as input and the RF port as output to measure the LO-to-RF feedthrough.

Action 7-17: In the Direct Plot Form, change the Plotting Mode to *Replace*.

Action 7-18: In the schematic, select the net RF as the output and net VLO as input.

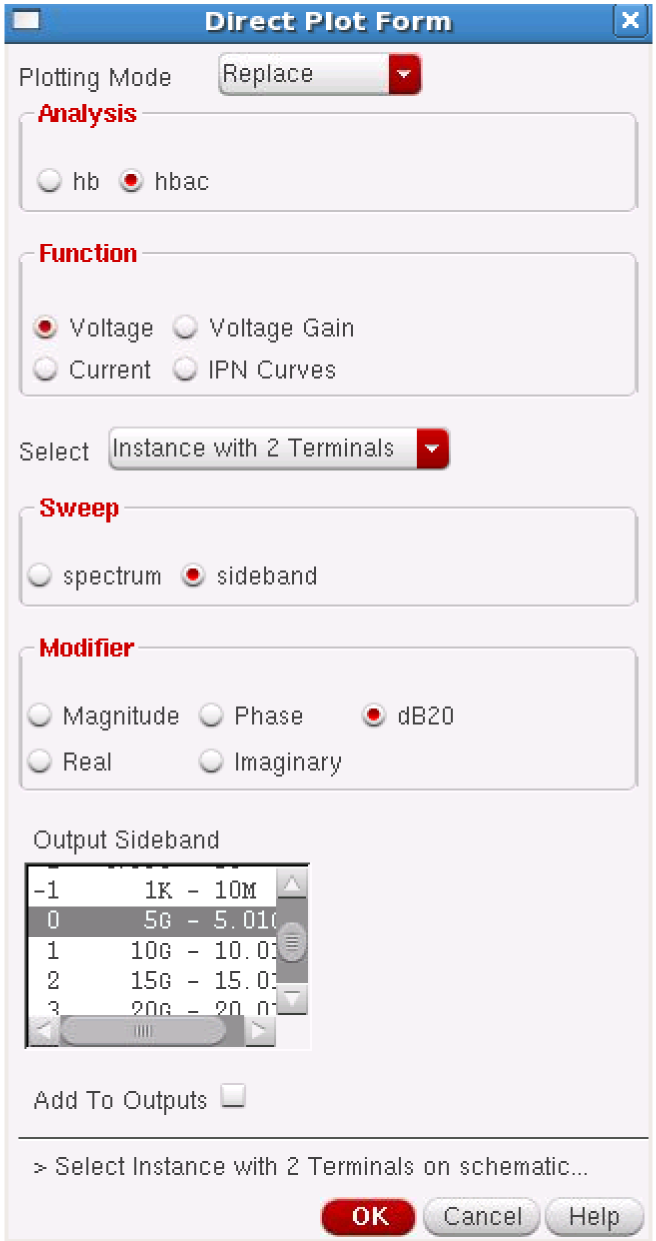
Action 7-19: In the waveform window, select **Marker — Place — Trace Marker** to place a marker at the first harmonic 5 GHz.

The following waveform shows the LO to RF feedthrough:



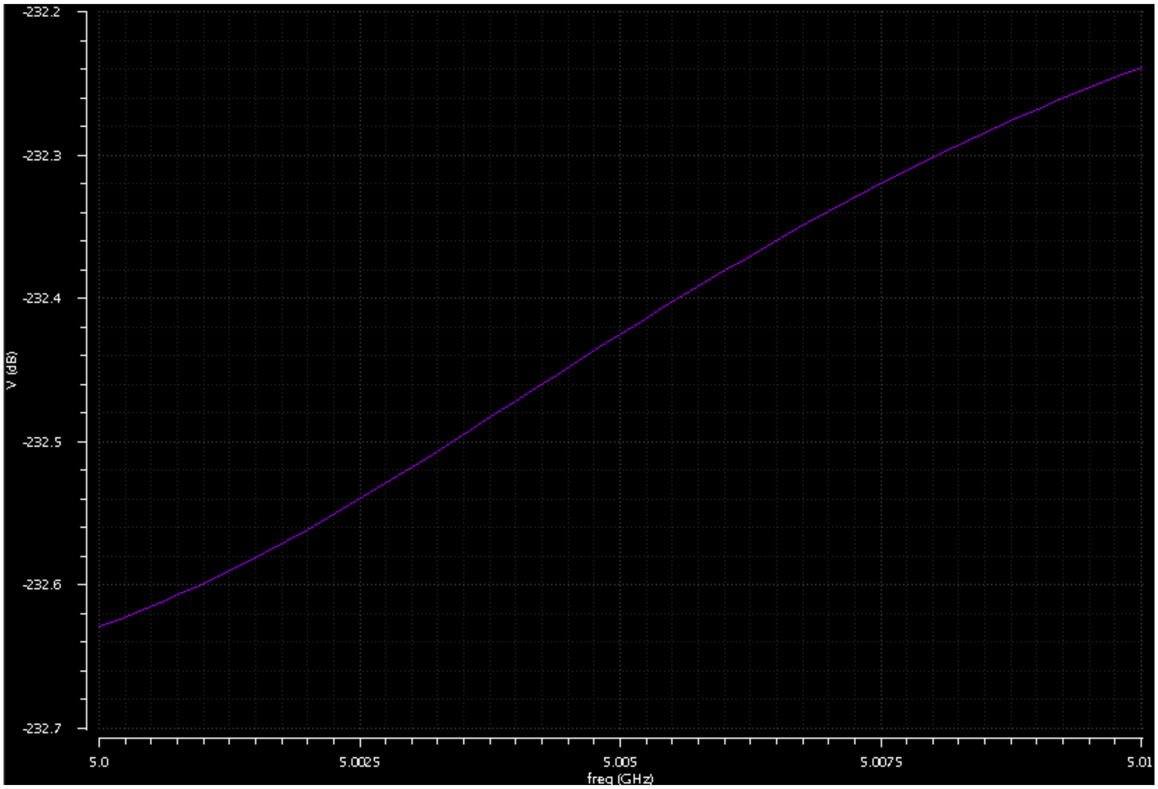
RF-to-LO feedthrough affects the local oscillator by letting strong interferers at the input pass through to the LO. Measure RF-to-LO feedthrough using the PAC analysis results.

Action 7-20: In the Direct Plot Form, select the *hbac* button, and configure the form as follows:



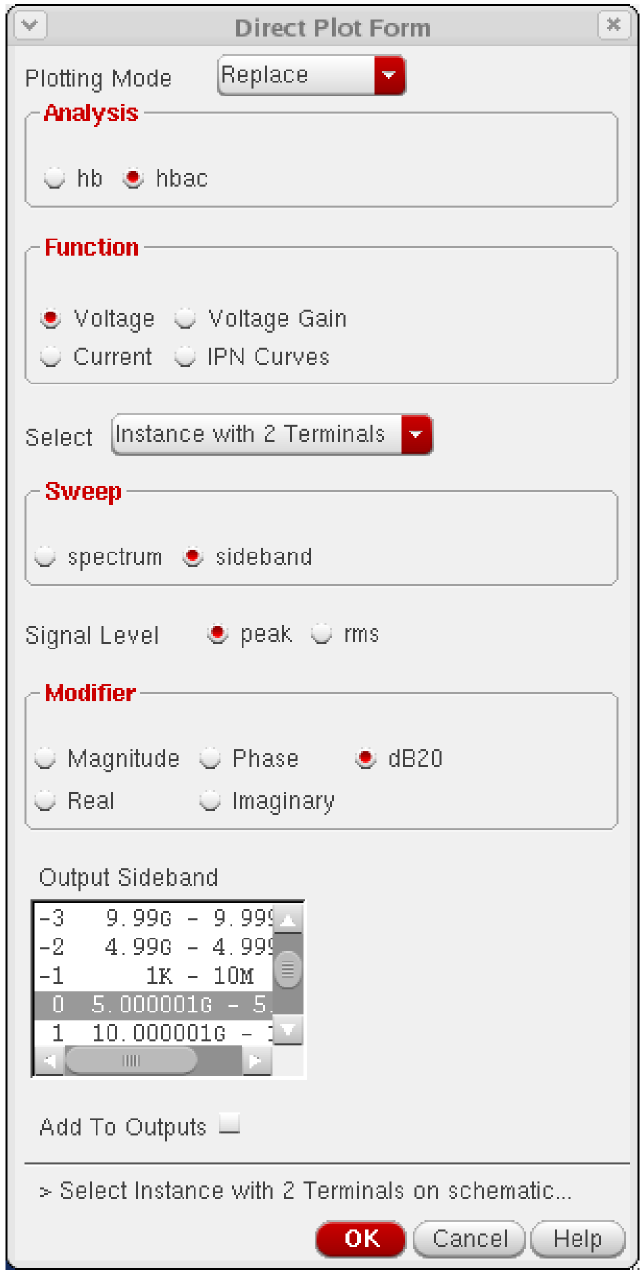
Action 7-21: Select 0 in *Output Sideband* to represent the RF signal and click `PORT1` to select the LO port as the output instance.

The following waveform shows the RF to LO feedthrough:



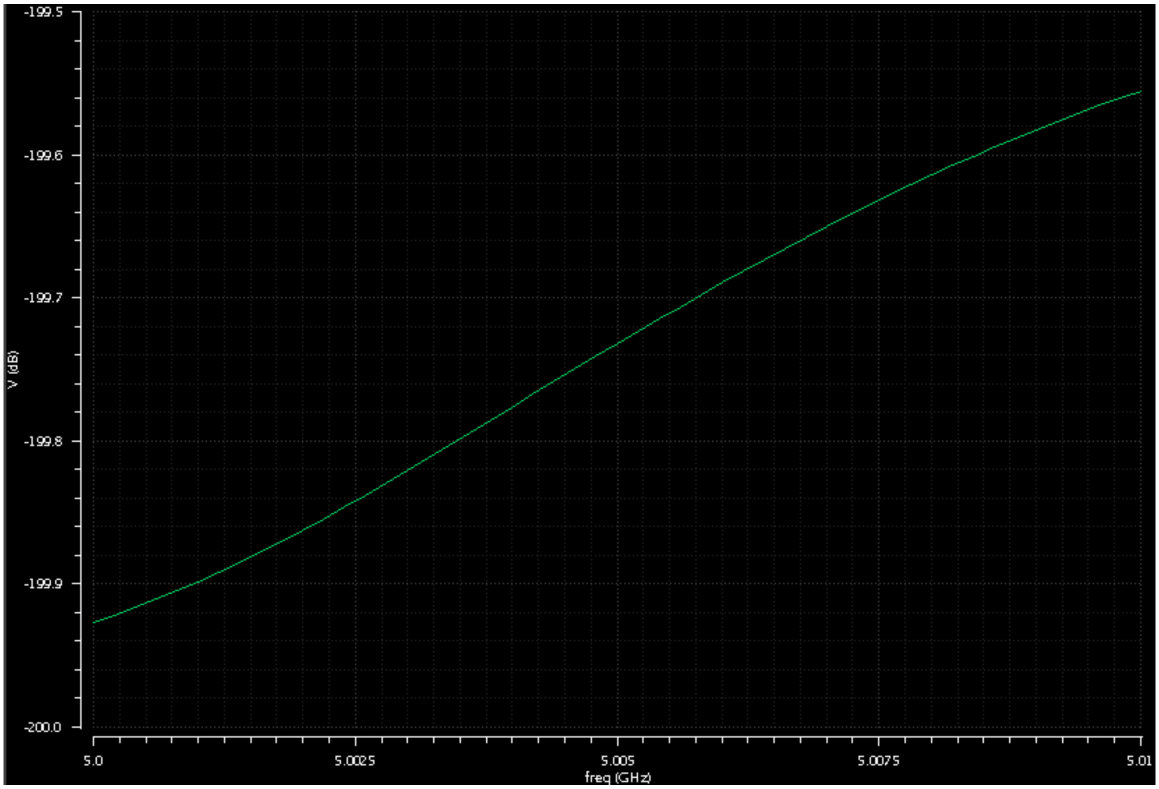
RF-to-IF feedthrough might create an even-order distortion problem for homodyne receivers. Measure RF-to-IF feedthrough using the hbac analysis results with two simple changes.

Action 7-22: In the Direct Plot Form, select the *hbac* button and configure the form as follows:



Action 7-23: Select 0 in *Output Harmonic* and select the IF output `PORT3`.

The following waveform shows the RF to IF feedthrough:



Action 7-24: Click *Cancel* in the Direct Plot Form. Close the waveform window.

Lab 8: Mixer Performance with a Blocking Signal (hb, hbac, and hbnoise)

Large interfering signals are called blockers. Blocking signals reduce the mixer's gain and deteriorate the mixer's noise performance. As such, you need to measure the gain and noise of a mixer in the presence of a blocking signal. Many communication standards include blocking requirements for both mobile and base stations. The requirements use several in-band and multiple out-of-band blocking signals.

Because a mixer has both signal and LO inputs, you should use the multi-tone large signal hb analysis for these measurements. Follow the hb analysis with hbac and hbnoise analyses to measure gain and NF variations versus the level of the interfering signal. In the hb analysis, model the blocker as a moderate tone.

Action 8-1: If it is not already open, open the *schematic* view of the *mixer_testbench* design in the library *RFworkshop.*

Action 8-2: From the *Mixer_testbench* schematic, choose **Tools — Analog Environment**.

The Virtuoso Analog Design Environment window appears.

Action 8-3: Select the `PORT0` source. Use the **Edit — Properties — Objects** command to ensure that the port properties are set as described below:

Parameter	Value
Resistance	50 ohm
Port Number	1
DC voltage	500 mV
Source type	*sine*
Frequency name 1	RF1
Frequency 1	5.003G
Amplitude 1 (dBm)	prf
PAC magnitude (dBm)	-30

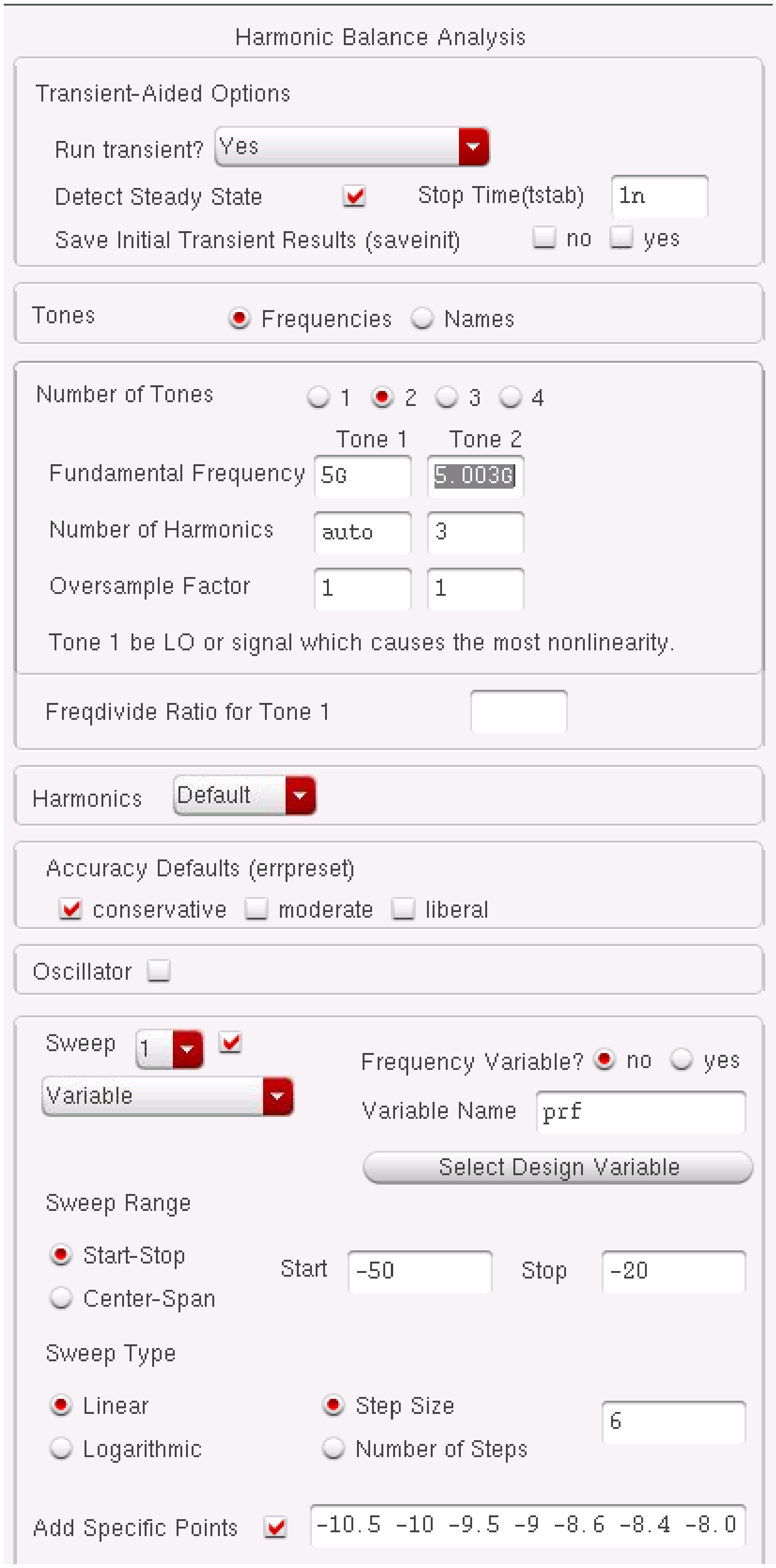
Action 8-4: Make sure the *Source type* of `PORT1` is set to *sine* and the *Source type* of `PORT3` is set to *dc*.

Action 8-5: Check and save the schematic.

Action 8-6: You can choose **Session — Load State**, select **Cellview** in **Load State Option** and load state "**Lab8_Blocker_hbachbnoise**" and skip to Action 8-14 or …

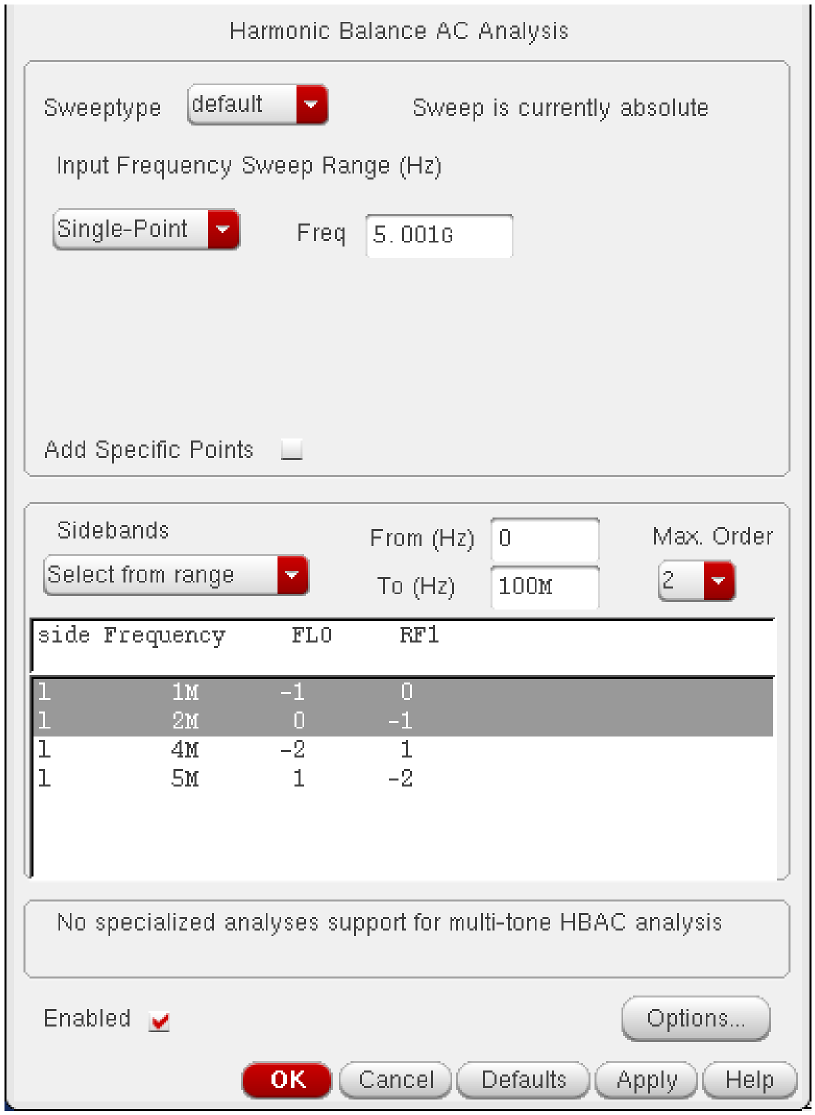
Action 8-7: In the Virtuoso Analog Design Environment window, choose **Analyses — Choose**.

Action 8-8: In the Choosing Analyses window, select the *hb* button in the *Analysis* field of the window. Represent the blocking signal by setting the moderate tone frequency fblocker = 5.003 GHz. Represent a small-signal RF input by setting a fixed value for the pacm parameter. For example, in this example pacm = -30 dB. In the hb analysis, sweep the parameter prf from -50 dB to -8 dB. The form looks like this.


Harmonic Balance Analysis
Transient-Aided Options
Run transient? Yes
Detect Steady State
Stop Time(tstab) 1n
Save Initial Transient Results (saveinit) no yes
Tones Frequencies Names
Number of Tones 1 2 3 4
Tone 1 Tone 2
Fundamental Frequency 5G 5.003G
Number of Harmonics auto 3
Oversample Factor 1 1
Tone 1 be LO or signal which causes the most nonlinearity.
Freqdivide Ratio for Tone 1
Harmonics Default
Accuracy Defaults (errpreset)
conservative moderate liberal
Oscillator
Sweep 1
Variable
Frequency Variable? no yes
Variable Name prf
Select Design Variable
Sweep Range
Start-Stop
Center-Span
Start -50
Stop -20
Sweep Type
Linear
Logarithmic
Step Size
Number of Steps
6
Add Specific Points -10.5 -10 -9.5 -9 -8.6 -8.4 -8.0

Action 8-9: Make sure the *Enabled* button is on. In the Choosing Analyses window, click *Apply*.

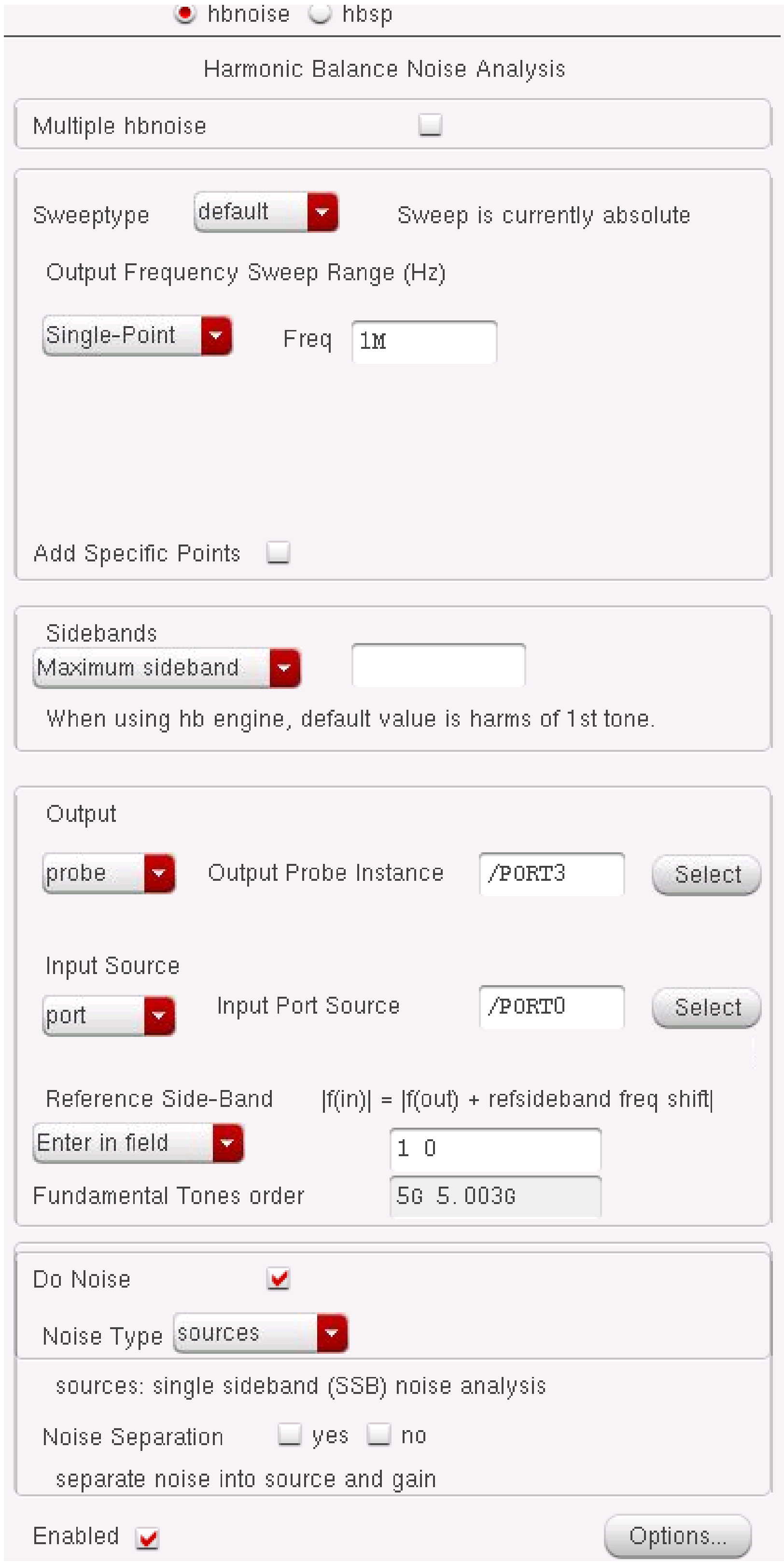
Action 8-10: In the Choosing Analyses window, select the *hbac* button in the *Analysis* field of the window. Set the input frequency = 5.001 GHz and set *Sweeptype* = absolute. The form looks like this.



Action 8-11: Make sure the *Enabled* button is on. In the Choosing Analyses window, click *Apply*.

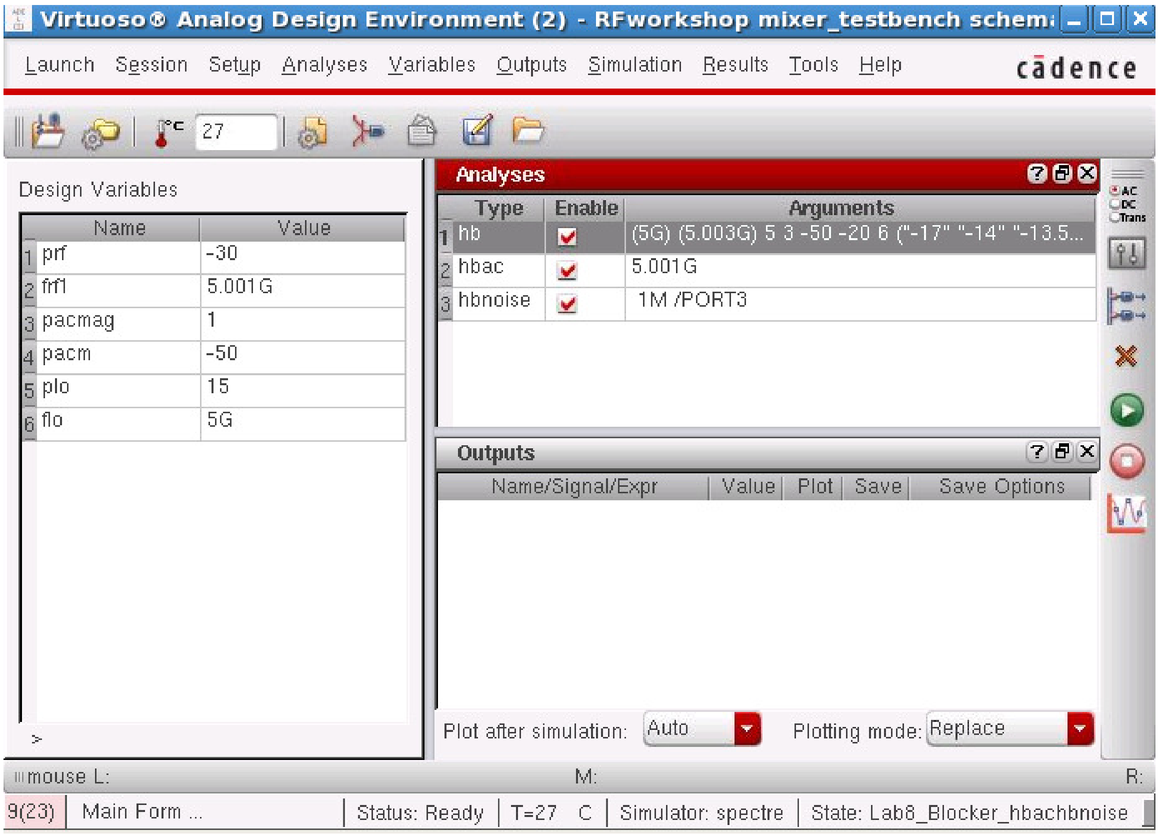
Action 8-12: In the Choosing Analyses window, select the *hbnoise* button in the *Analysis* field of the window.
Use a 1 MHz frequency point and *Maximum clock order* = 10. Set Output *probe* as `PORT3` and *Input Source* as `PORT0`. Use the *Reference side-*

band as (1 0) to represent a downconverted RF signal relative to the IF output signal, 1 MHz + 1 * f (LO) = f (RF). The form looks like this.



Action 8-13: Make sure the *Enabled* button is on. In the Choosing Analyses window, click *OK*.

The Virtuoso Analog Design Environment window looks like:

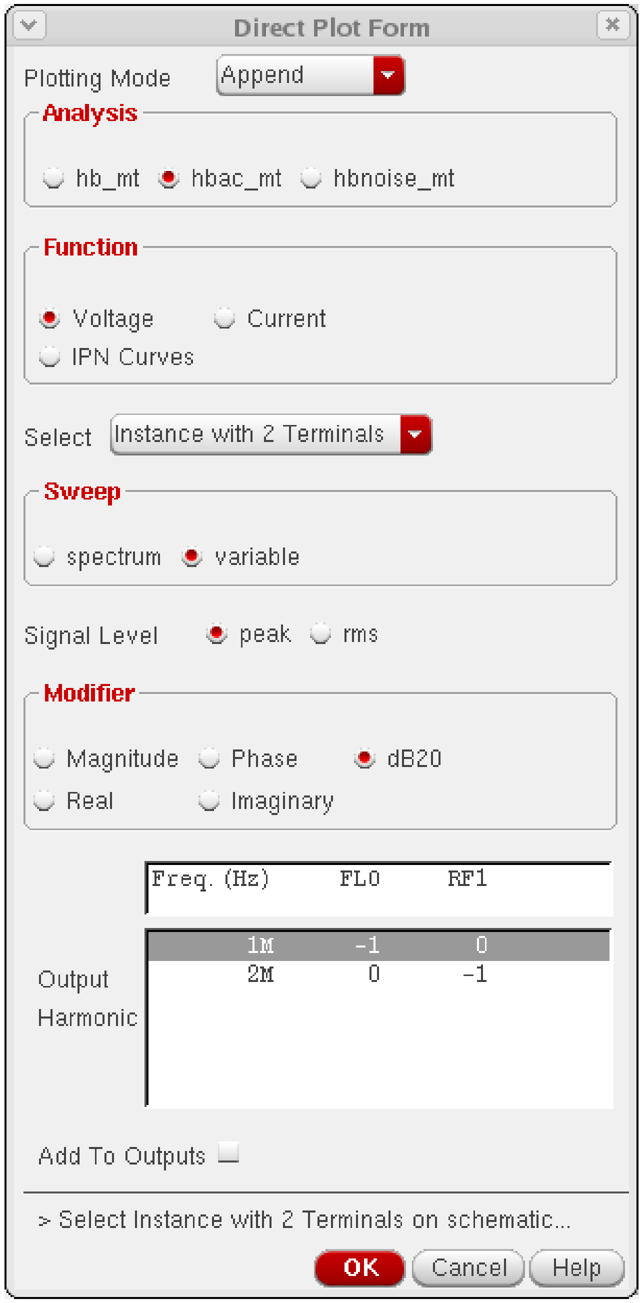


Action 8-14: In the Virtuoso Analog Design Environment, choose **Simulation — Netlist and Run** or click the **Netlist and Run** icon to start the simulation.

When the simulation ends, you can check how the blocking signal affects the performance of the Mixer.

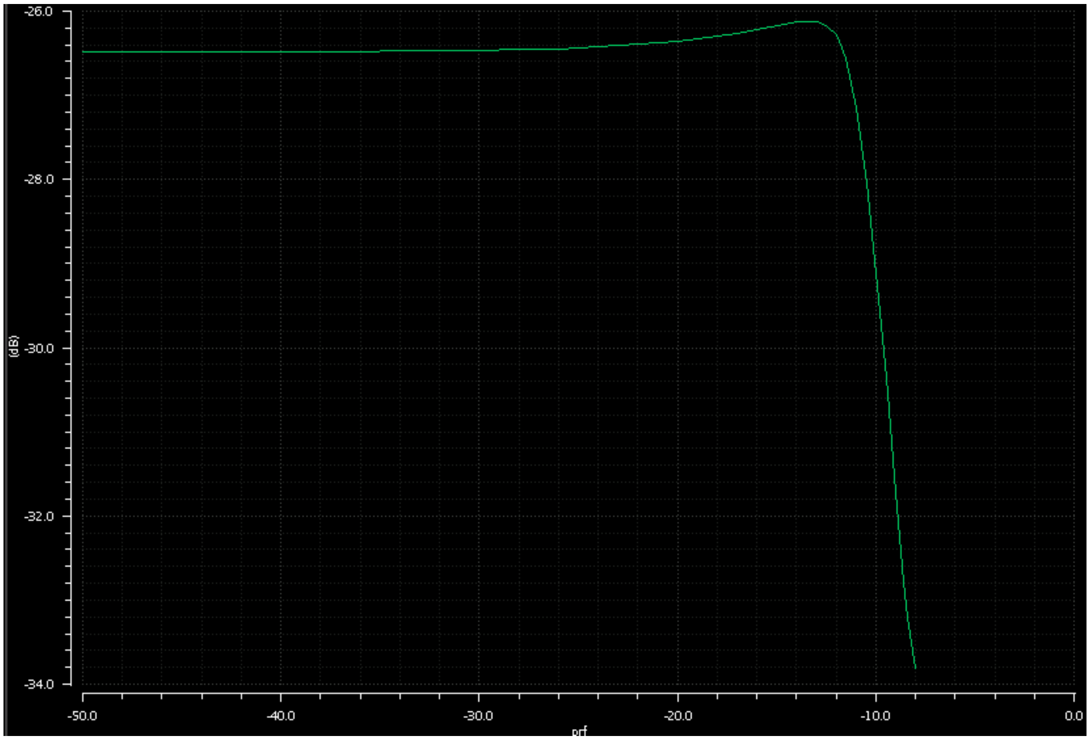
Action 8-15: In the Virtuoso Analog Design Environment window, choose **Results — Direct Plot — Main Form**.

Action 8-16: In the Direct Plot Form, select the *hbac_mt* button, and configure the form as follows:



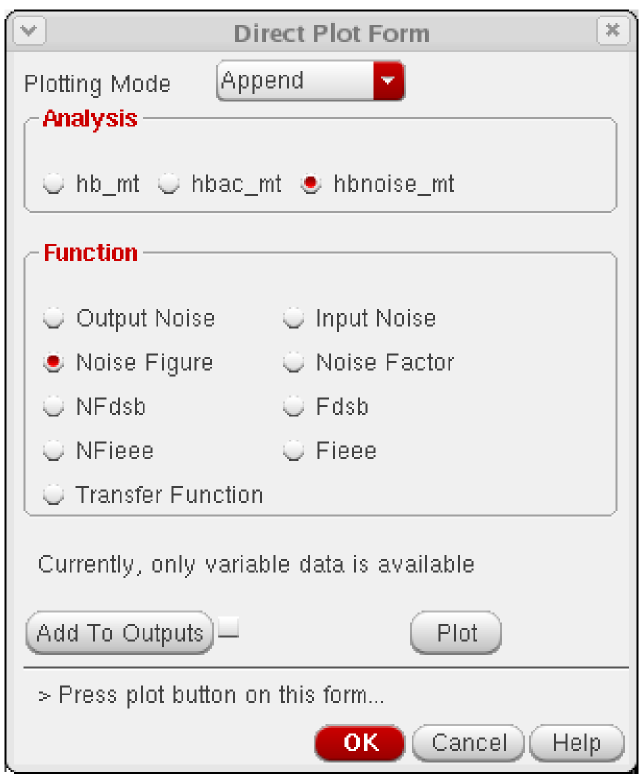
Action 8-17: Select `PORT3`.

The waveform window appears, showing the blocker effect on the voltage gain.



Action 8-18: Close the waveform window.

Action 8-19: In the Direct Plot Form, select the *hbnoise_mt* button, and configure the form as follows:

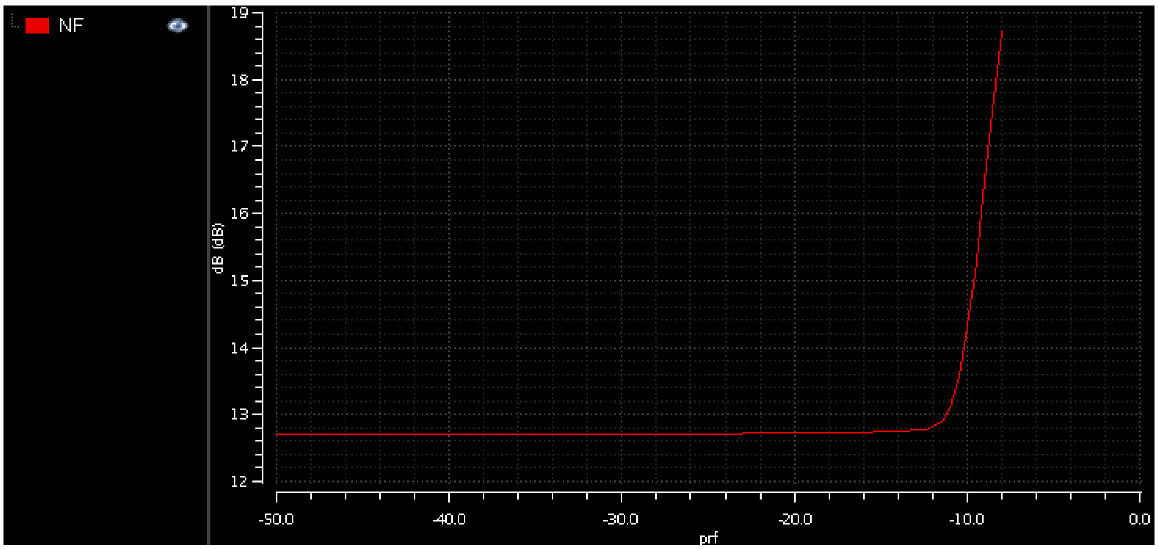


Action 8-20: Click *Plot*.

The waveform window appears.

Action 8-21: Right-click the X axis, move to Swap Freq Axis, left-click it. In the new window, note that prf is already selected. Type 1M in the X axis value field, select OK.

The waveform window appears, showing the blocker effect on the noise figure:



Action 8-22: Close the waveform window. Click *Cancel* in the Direct Plot Form.

Intermodulation Distortion and Intercept Points

Mixer distortion limits the sensitivity of a receiver if there is a large interfering signal present that is within the bandwidth of the RF input filter (a characteristic known as selectivity). There are two aspects of distortion that are of concern:

- Compression
- Intermodulation Distortion

The 1 dB compression point (CP1) is the point where the output power of the fundamental crosses the line that represents the output power extrapolated from small-signal conditions minus 1 dB. The 3rd order intercept point (IP3) is the point where the third-order term as extrapolated from small-signal conditions crosses the extrapolated power of the fundamental.

The third order intermodulation distortion occurs when signals at frequencies f_1 and f_2 mix together to form the response at $2f_1 - f_2$ and $2f_2 - f_1$. If f_1 and f_2 are close enough in frequency, then the intermodulation products $2f_1 - f_2$ and $2f_2 - f_1$ are in-band and interfere with the reception of the input signal. (When choosing f_1 and f_2, perform a PAC analysis to determine the bandwidth of the circuit, and place them in the middle of the bandwidth, close enough in frequency so that their intermodulation terms are well within the bandwidth.) Distortion of the output signal occurs because several of the odd-order intermodulation tones fall within the bandwidth of the circuit.

Intermodulation distortion is typically measured in the form of an intercept point. You determine the 3rd order intercept point (IP3) by plotting the power of the fundamental and the 3rd order intermodulation product versus the input power. Both input and output power should be plotted in some form of dB. Extrapolate both curves from a low power level and identify where they cross—that is the intercept point. To make this determination and to be comfortable with the accuracy of the results, you must have a broad region where both curves follow their asymptotic behavior. When in the asymptotic region, the slope of an nth order distortion product has a slope of n. Thus, when measuring IP3, the fundamental power curve is extrapolated from where the curve has a slope of 1 over a broad region. The 3rd order intermodulation product is extrapolated from a point where its curve has a slope of 3 over a broad region.

Previous versions of SpectreRF use either qpss (or hb)-based or qpac (or hbac)-based methods to calculate IP3 in a system that contains a mixer and LO. In the qpss (or hb)-based method, three-tone qpss/hb analysis with LO, RF1 and RF2 frequencies ω_{LO}, ω_{RF1} and ω_{RF2} is run at a given RF power level. IM3 of harmonic $2\omega_{RF1}-\omega_{RF2}-\omega_{LO}$ is obtained from the solution. Assuming RF power is low enough and IM3 is dominated by leading order V_{RF}^3 terms, $log(V_{IM3})$ is expected to be a linear function of $log(V_{RF})$ with a slope of 3. IP3 is then extrapolated from V_{IM3}. Here V_{IM3} and V_{RF} are amplitudes of the IM3 and RF signals, respectively. This method requires very high accuracy to accommodate the large dynamic range between the RF and LO signals because they are mixed in the same solution vector. For a large circuit, this method also relies on speed and convergence of multi- tone qpss (or hb).

In the qpac (or hbac)-based method, a two-tone qpss/hb analysis at frequencies ω_{RF1} and ω_{LO} is run first. Then RF2 input is included as a small signal by qpac/hbac analysis to calculate IM3 at $2\omega_{RF1}-\omega_{RF2}-\omega_{LO}$. As in the qpss-based (or hb) method, this method also has to cover the dynamic range between RF1 and LO and depends on convergence of two-tone qpss/hb.

Compared to the qpss (or hb)-based approach, the qpac (or hbac) approach reduces computation from three-tone qpss (or hb) to two-tone qpss (or hb) plus a qpac/hbac by applying first order perturbation to RF2 signal. The amount of computation can be further reduced if we treat both RF signals as perturbation to the steady-state operating point at LO frequency with zero RF input. In this way, leading order intermodulation between RF1 and RF2 in IM3 can be computed directly from third order perturbation.

Starting in the MMSIM60 USR2 release, SpectreRF provides a perturbative approach to solve weakly nonlinear circuits. This approach does not require explicit high order derivatives from the device model. All equations are formulated in the form of RF harmonics. They can be implemented in both time and frequency domains.

For nonlinear system, the circuit equation can be expressed as:

$$L \cdot v + F_{NL}(v) = \varepsilon \cdot s$$

Here the first term is the linear part, the second one is the nonlinear part, and s is the RF input source. Parameter ε is introduced to keep track of the order of the perturbation expansion. Under weakly nonlinear condition, the nonlinear part is small compared to the linear part, so the above equation can be solved by using the Born approximation iteratively:

$$u^{(n)} = v^{(1)} - L^{-1} \cdot F_{NL}\left(u^{(n-1)}\right)$$

where $u^{(n)}$ is the approximation of v and is accurate to the order or $O(\varepsilon^n)$.

Because the evaluation of F_{NL} takes full nonlinear device evaluation of F and its first derivative, no higher order derivative is needed. This allows the simulator to carry out higher order perturbations without modifications to the current device models. Also, the dynamic range of perturbation calculations covers only RF signals, giving the perturbative method advantages in terms of accuracy.

Lab 9: IP3 Calculation (Swept hb and hbac)

Action 9-1: If it is not already open, open the *schematic* view of the *mixer_testbench* design in the library *RFworkshop.*

Action 9-2: Select the `PORT0` source. Use the **Edit — Properties — Objects** command to ensure that the port properties are set as described below:

Parameter	**Value**
Resistance	50 ohm
Port Number	1
DC voltage	500 mV
Source type	*sine*
Frequency name 1	RF1
Frequency 1	frf
Amplitude 1 (dBm)	prf
PAC magnitude (dBm)	prf

Action 9-3: Click *OK* on the Edit Object Properties window to close.

Action 9-4: Check and save the schematic.

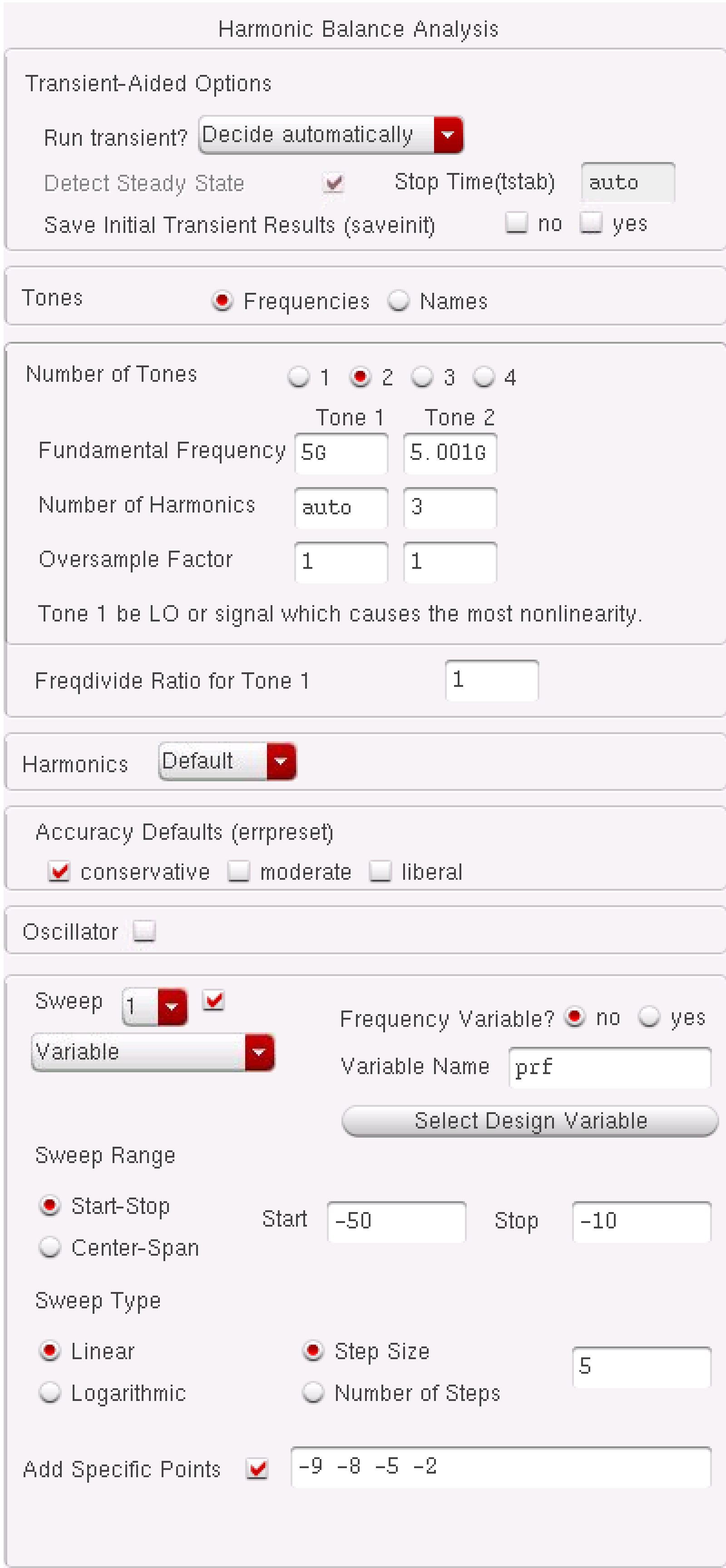
Action 9-5: From the *Mixer_testbench* schematic, choose **Launch — ADE L**.

The Virtuoso Analog Design Environment window appears.

Action 9-6: You can choose **Session — Load State**, select **Cellview** in **Load State Option** and load state "**Lab9_IP3_hbac**" and skip to Action 9-12 or …

Action 9-7: In the Virtuoso Analog Design Environment window, choose **Analyses — Choose.**

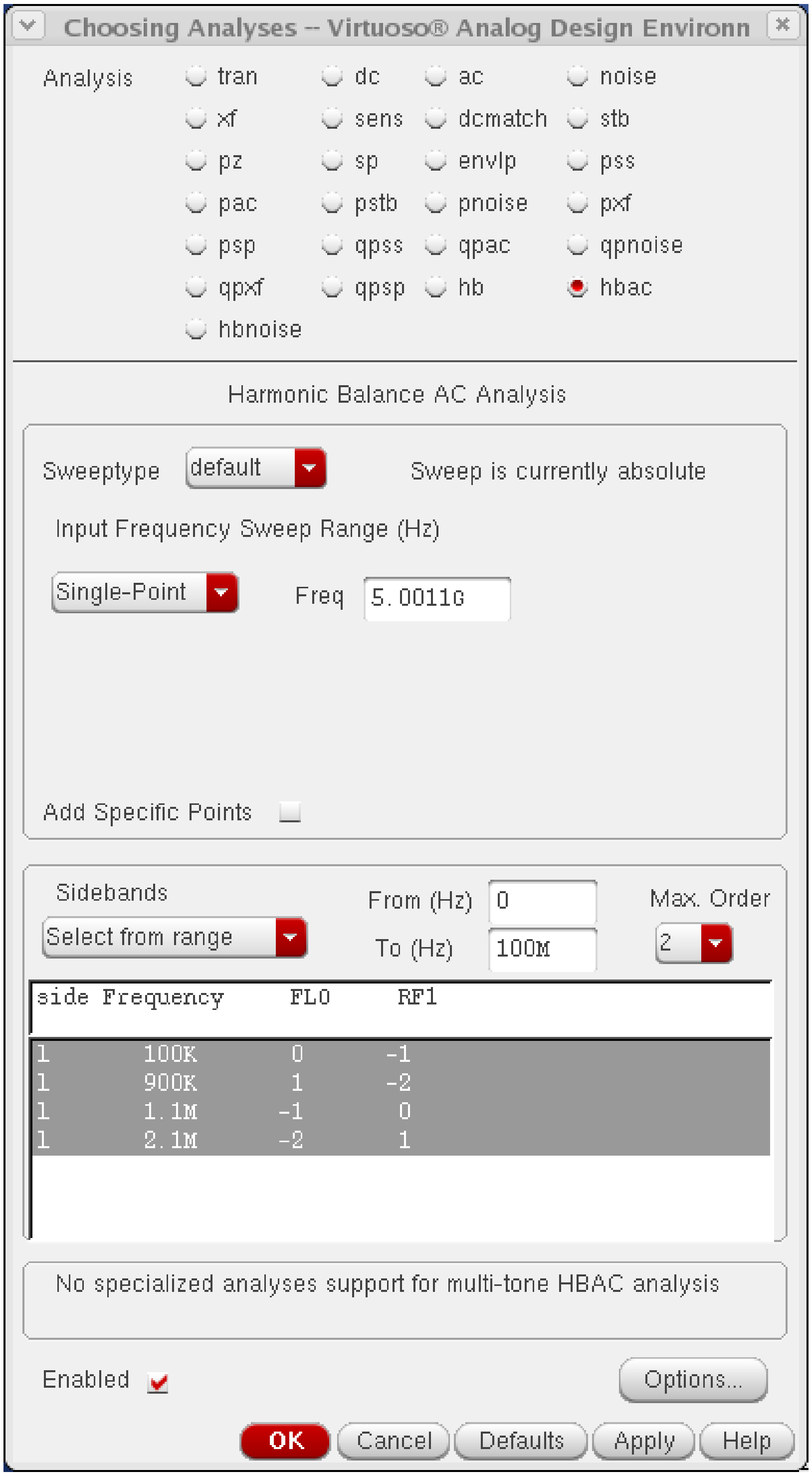
Action 9-8: In the Choosing Analyses window, select the *hb* button in the *Analysis* field of the window and set the form as follows:


Harmonic Balance Analysis
Transient-Aided Options
Run transient? Decide automatically
Detect Steady State
Stop Time(tstab) auto
Save Initial Transient Results (saveinit) no yes
Tones Frequencies Names
Number of Tones 1 2 3 4
Tone 1 Tone 2
Fundamental Frequency 5G 5.001G
Number of Harmonics auto 3
Oversample Factor 1 1
Tone 1 be LO or signal which causes the most nonlinearity.
Freqdivide Ratio for Tone 1 1
Harmonics Default
Accuracy Defaults (errpreset)
conservative moderate liberal
Oscillator
Sweep 1
Variable
Frequency Variable? no yes
Variable Name prf
Select Design Variable
Sweep Range
Start-Stop
Center-Span
Start -50 Stop -10
Sweep Type
Linear
Logarithmic
Step Size
Number of Steps
5
Add Specific Points -9 -8 -5 -2

Action 9-9: Make sure the *Enabled* button is on. In the Choosing Analyses window, click *Apply*.

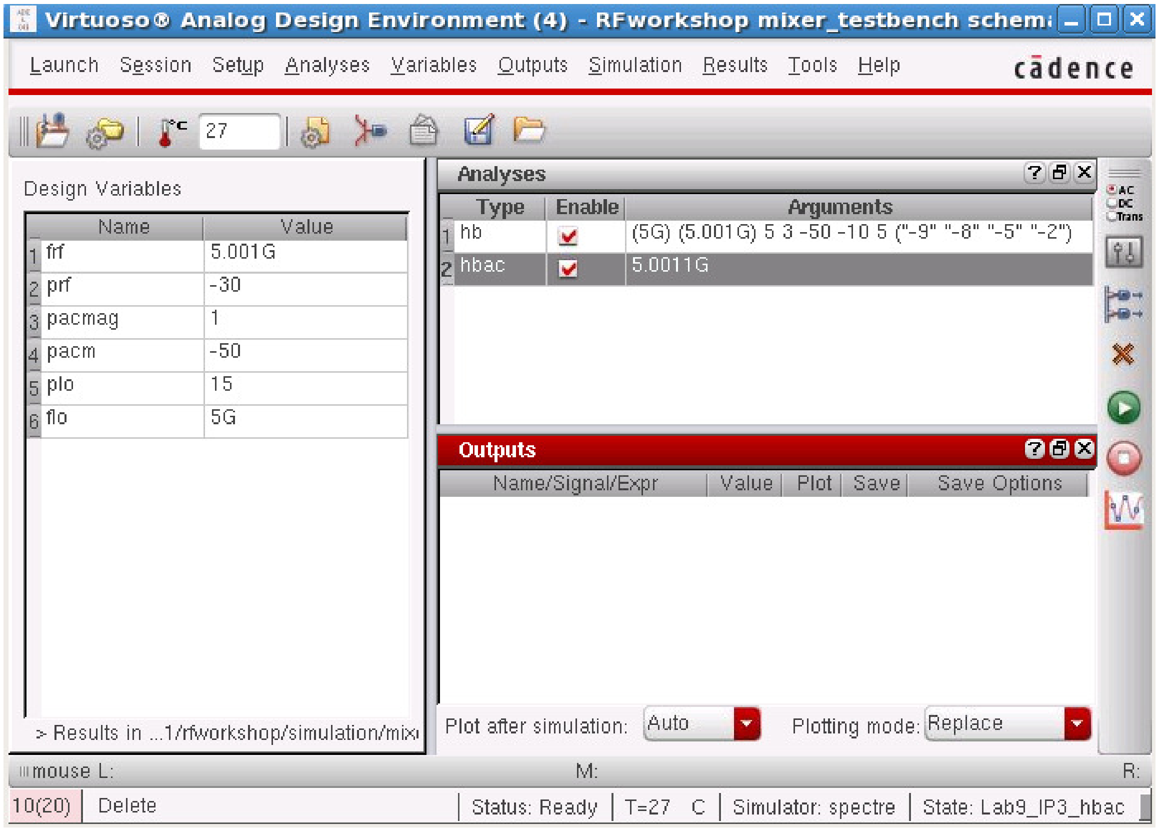
Action 9-10: In the Choosing Analyses window, select the *hbac* button in the ***Analysis*** field of the window. Set the frequency of the small signal very close to f(RF), for example 5.0011 GHz. In the *Select from range* option of the *Sidebands* section, highlight the harmonics of interest. Limit the harmonics to second order in the large tone (Set *Clock Order* = 2), from 0 Hz to 100 MHz.

The form looks like this.



Action 9-11: Make sure the *Enabled* button is on. In the Choosing Analyses window, click *OK*.

The Virtuoso Analog Design Environment window looks like this.

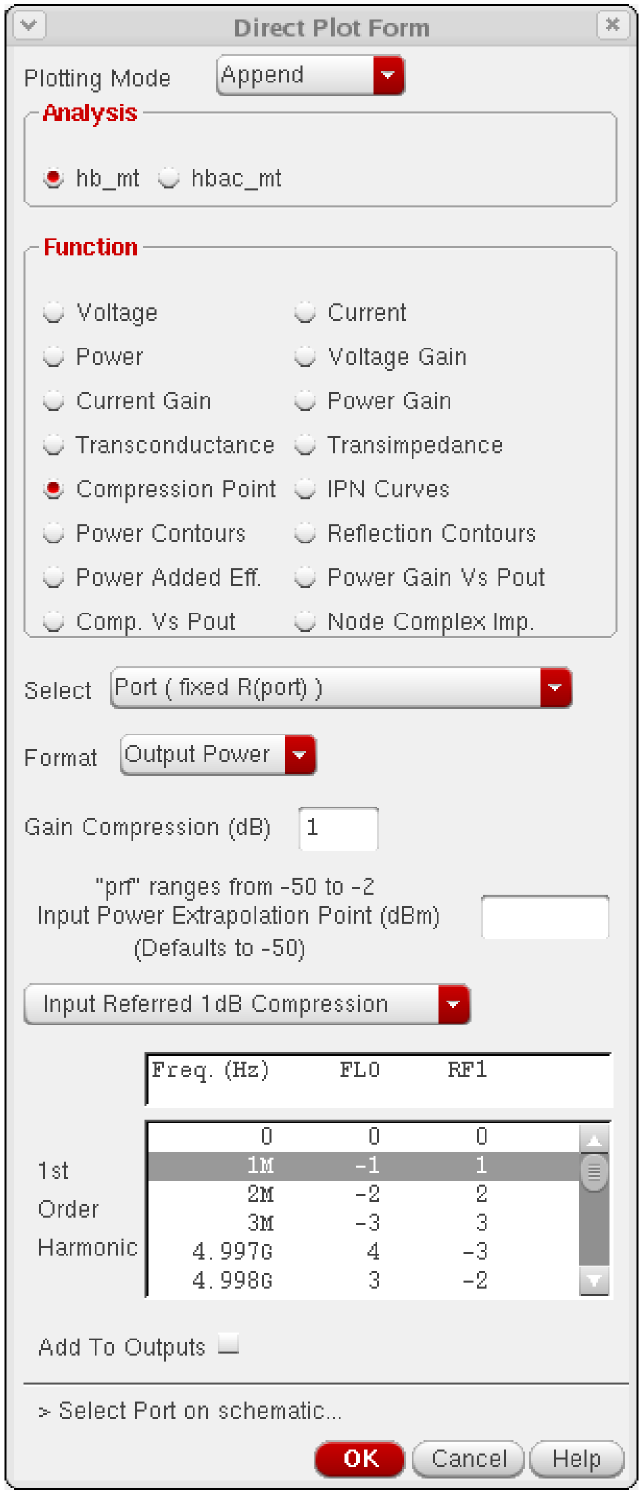


Action 9-12: In the Virtuoso Analog Design Environment window, choose **Simulation — Netlist and Run** or click the **Netlist and Run** icon to start the simulation.

When the simulation completes, use the Direct Plot feature to view the results.

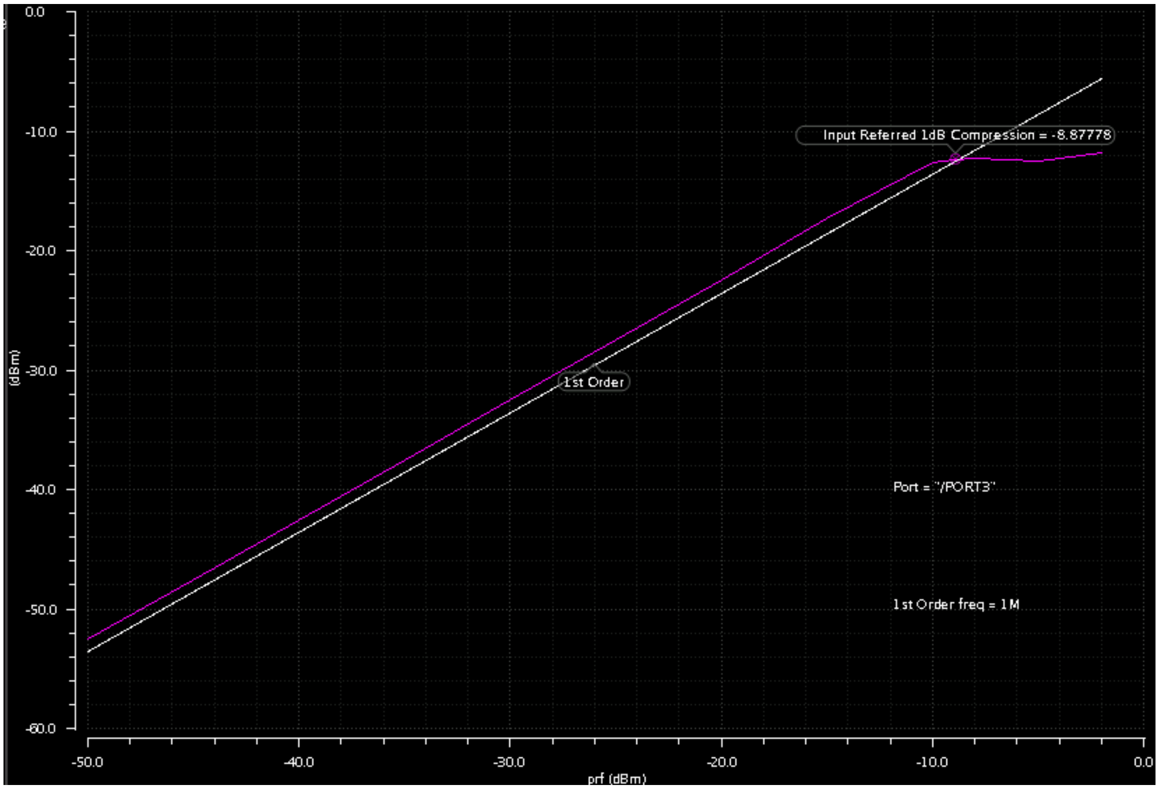
Action 9-13: In the Virtuoso Analog Design Environment window, choose **Results — Direct Plot — Main Form**.

Action 9-14: To plot the 1 dB compression point, click *hb_mt* analysis in the Direct Plot Form. Select *Compression Point*. Select a point in the linear region for an extrapolation or leave it blank to use the default value. The output harmonic is (-1 1) or 1 MHz.



Action 9-15: Select output `Port3` on schematic.

You see the value of the P1dB value as shown below:

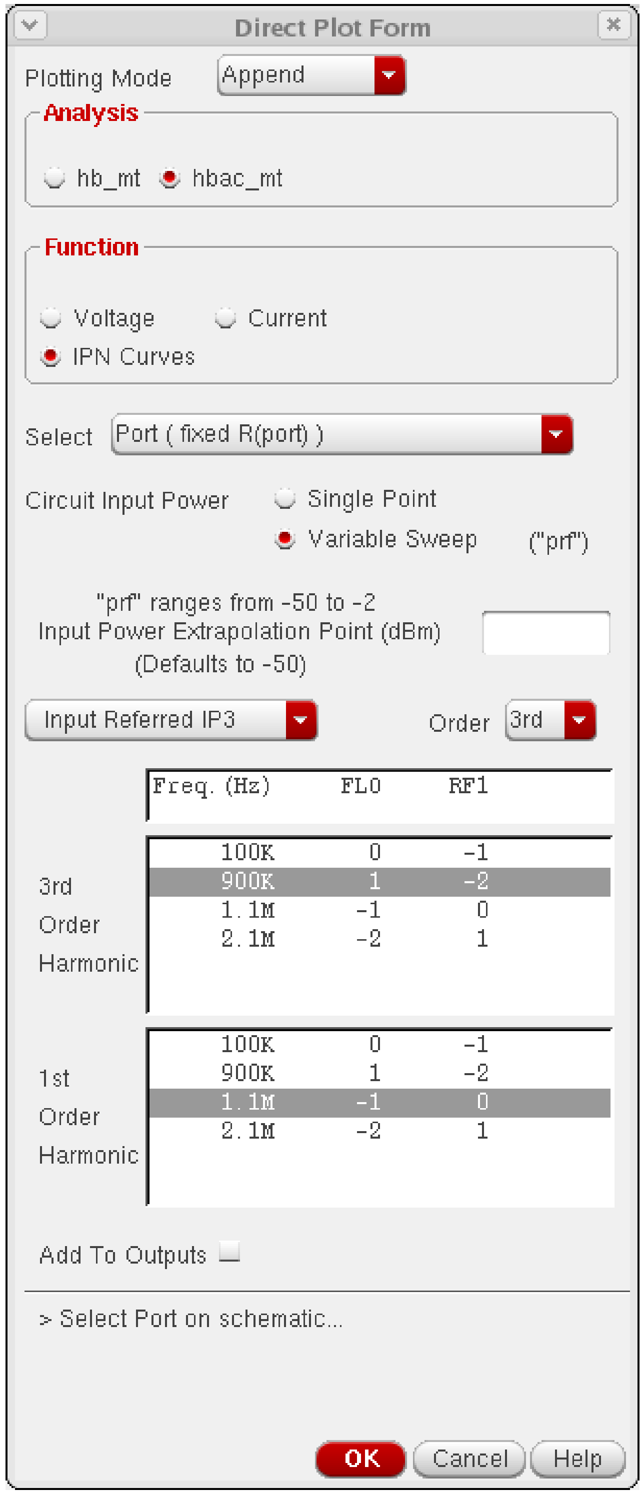


Action 9-16: Close the waveform window.

Action 9-17: To plot IP3, select *hbac_mt* analysis in the Direct Plot Form, select the *IPN Curves* button, select *Variable Sweep*. If the first extrapolation point you select is not in the linear range of the IM1 and IM3 curves, you might want to reset the extrapolation point later. To plot the third order input referred intercept point, set the first order harmonic to (-1 0) or 1.1 MHz, and the third order harmonic to (1 -2), or 0.9 MHz. Because the mixer is down-converting to the baseband, the first harmonic is calculated as:

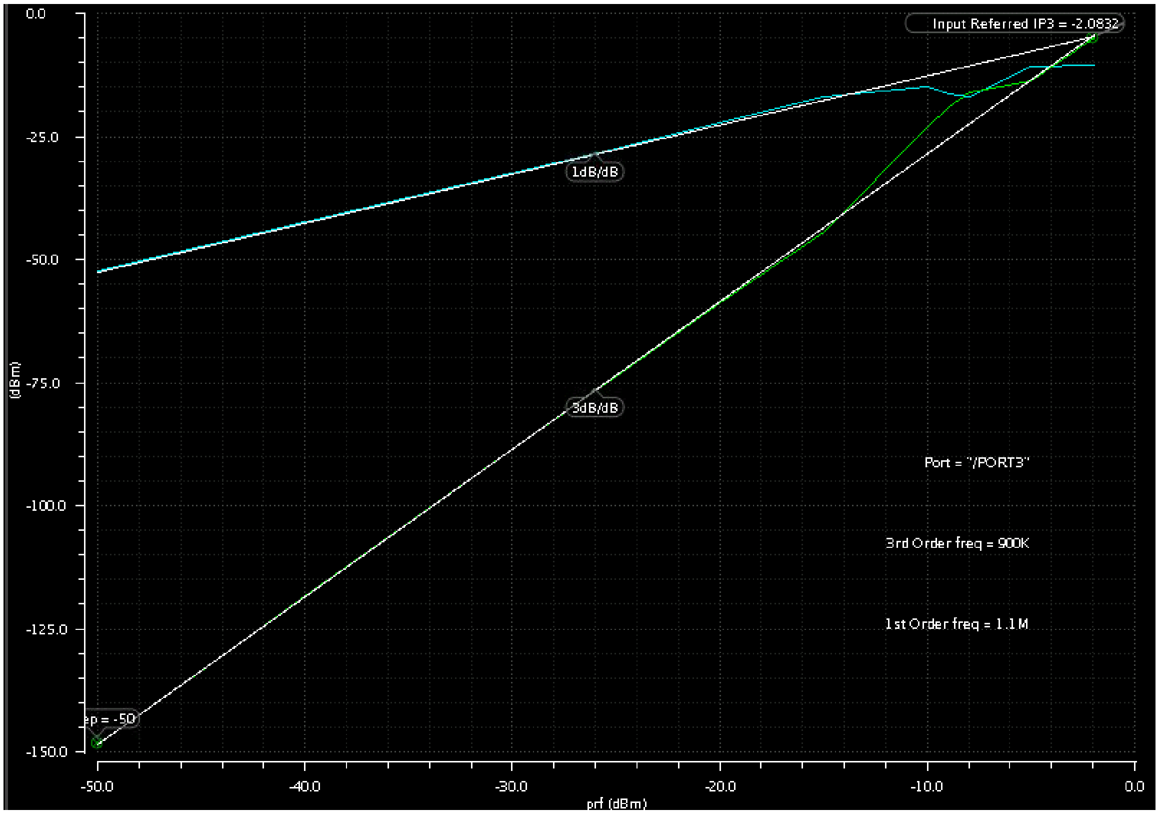
f(small signal) - f(LO) = 5.0011GHz - 5GHz = 1.1MHz

The third harmonic is at 0.9 MHz or -0.9 MHz depending on the *freqaxis* you selected in the Direct Plot Form. The form looks like this.



Action 9-18: Select output `Port3` on the schematic.

The third order input referred intercept point is calculated and curves of harmonics versus prf are presented as shown below:



Action 9-19: After viewing the waveforms, click *Cancel* in the Direct Plot Form.

For more accurate results, you might want to set *errpreset* = *conservative* when setting up the hb analysis. Initially, when you do not know the exact location of the linear region for IM3 and IM1, you may use *errpreset* = *moderate* to get a better understanding of your design. When the linear region is known, defining a single point simulation with *errpreset* = *conservative* is typically more accurate and less time-consuming.

Lab 10: IP3 Calculation (hb with Three Tones)

Another way to calculate IP3 is to apply the LO and two moderate RF input tones in a single hb analyses. That approach is illustrated in this lab.

Action 10-1: If it is not already open, open the *schematic* view of the *mixer_testbench* design in the library *RFWorkshop*.

Action 10-2: Select the `PORT0` source. Use the **Edit — Properties — Objects** command to ensure that the port properties are set as described below:

Parameter	Value
Resistance	50 ohm
Port Number	1
DC voltage	500 mV
Source type	*sine*
Frequency name 1	RF1
Frequency 1	frf
Amplitude 1 (dBm)	prf
Frequency name 2	RF2
Frequency 2	frf+0.1M
Amplitude 2 (dBm)	prf

Action 10-3: Click *OK* on the Edit Object Properties window to close.

Action 10-4: Check and save the schematic.

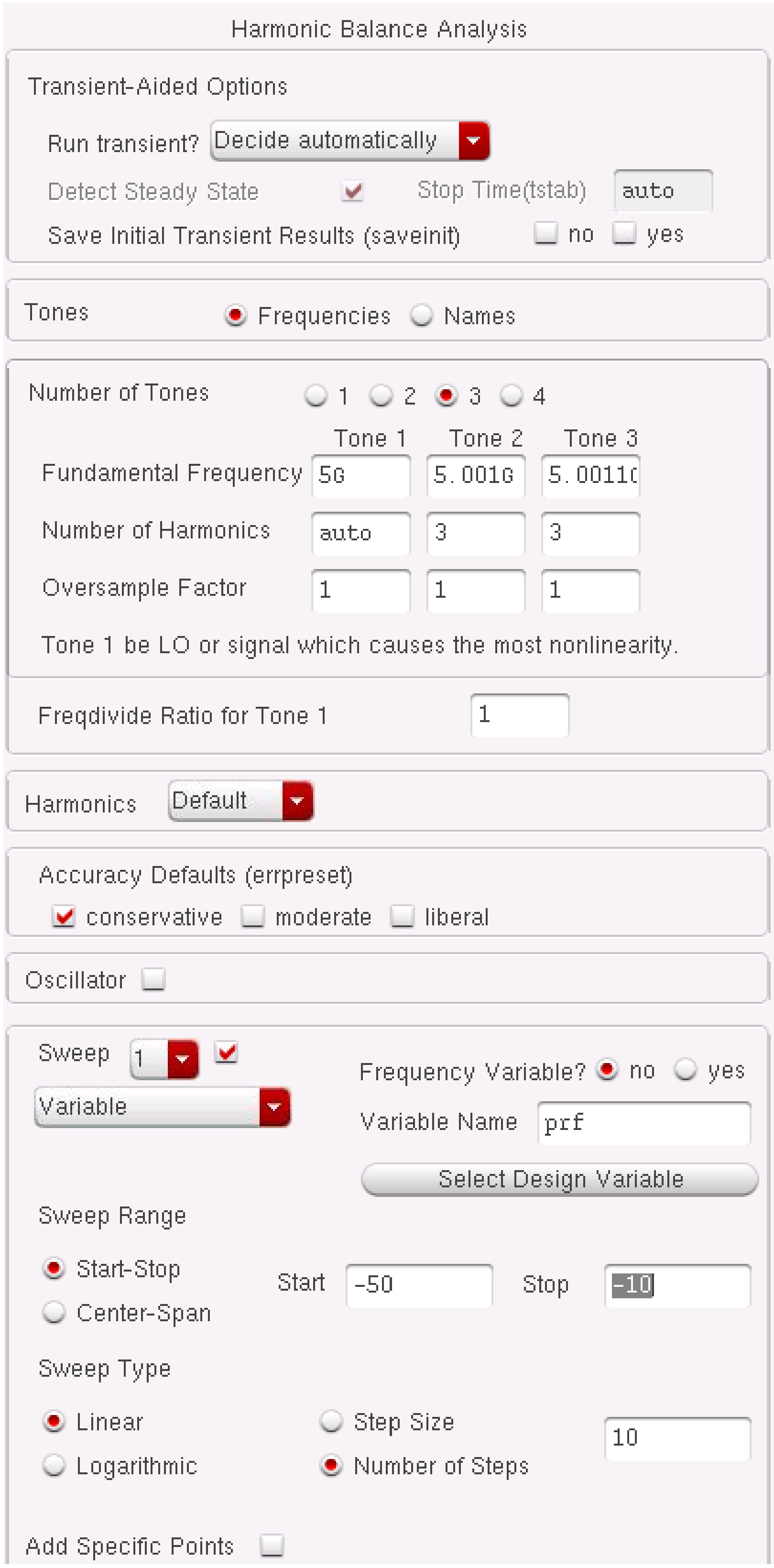
Action 10-5: From the *Mixer_testbench* schematic, choose **Launch — ADE L**.

The Virtuoso Analog Design Environment window appears.

Action 10-6: You can choose **Session — Load State**, select **Cellview** in **Load State Option** and load state "**Lab10_IP3_hb3**" and skip to Action 10-10 or …

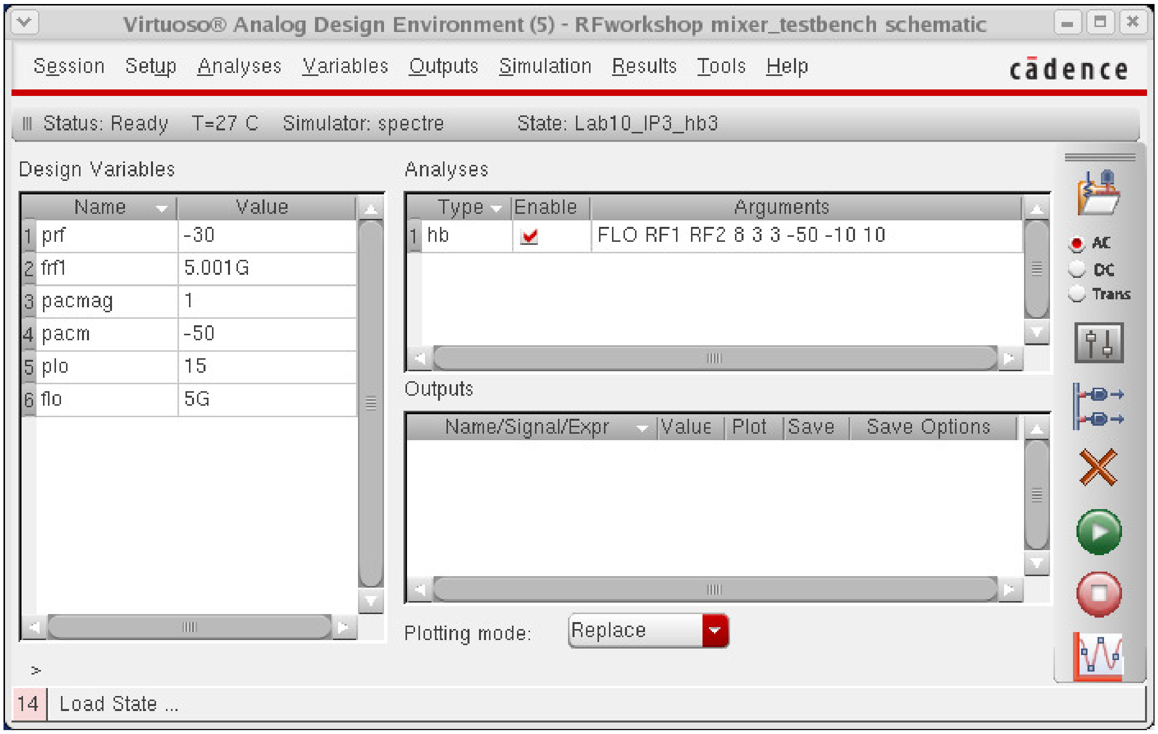
Action 10-7: In the Virtuoso Analog Design Environment window, choose **Analyses — Choose**.

Action 10-8: In the Choosing Analyses window, select the *hb* button in the *Analysis* field of the window and set the form as follows:


Harmonic Balance Analysis
Transient-Aided Options
Run transient? Decide automatically
Detect Steady State
Stop Time(tstab) auto
Save Initial Transient Results (saveinit) no yes
Tones Frequencies Names
Number of Tones 1 2 3 4
Tone 1 Tone 2 Tone 3
Fundamental Frequency 5G 5.001G 5.0011
Number of Harmonics auto 3 3
Oversample Factor 1 1 1
Tone 1 be LO or signal which causes the most nonlinearity.
Freqdivide Ratio for Tone 1 1
Harmonics Default
Accuracy Defaults (errpreset)
conservative moderate liberal
Oscillator
Sweep 1
Variable
Frequency Variable? no yes
Variable Name prf
Select Design Variable
Sweep Range
Start-Stop
Center-Span
Start -50
Stop -10
Sweep Type
Linear
Logarithmic
Step Size
Number of Steps
10
Add Specific Points

Action 10-9: Make sure the *Enabled* button is on. In the Choosing Analyses window, click *OK*.

The Virtuoso Analog Design Environment window looks like this.

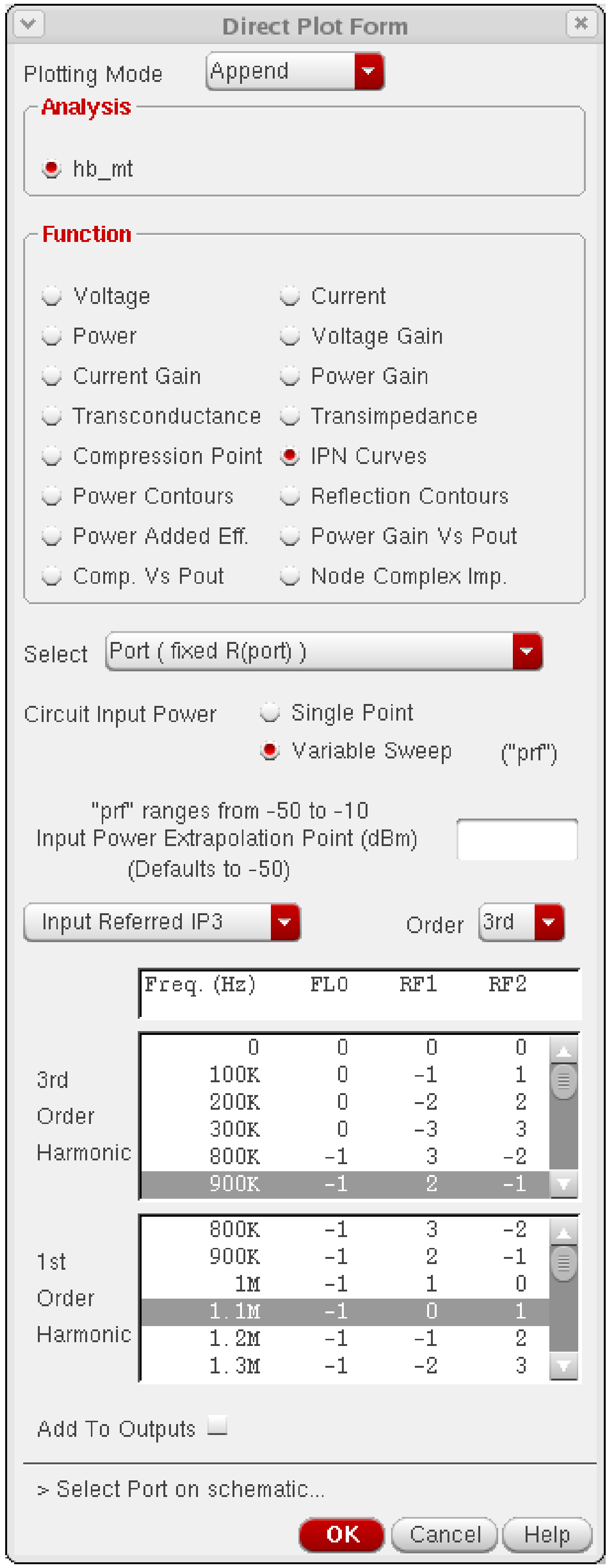


Action 10-10: In the Virtuoso Analog Design Environment window, choose **Simulation — Netlist and Run** or click the **Netlist and Run** icon to start the simulation.

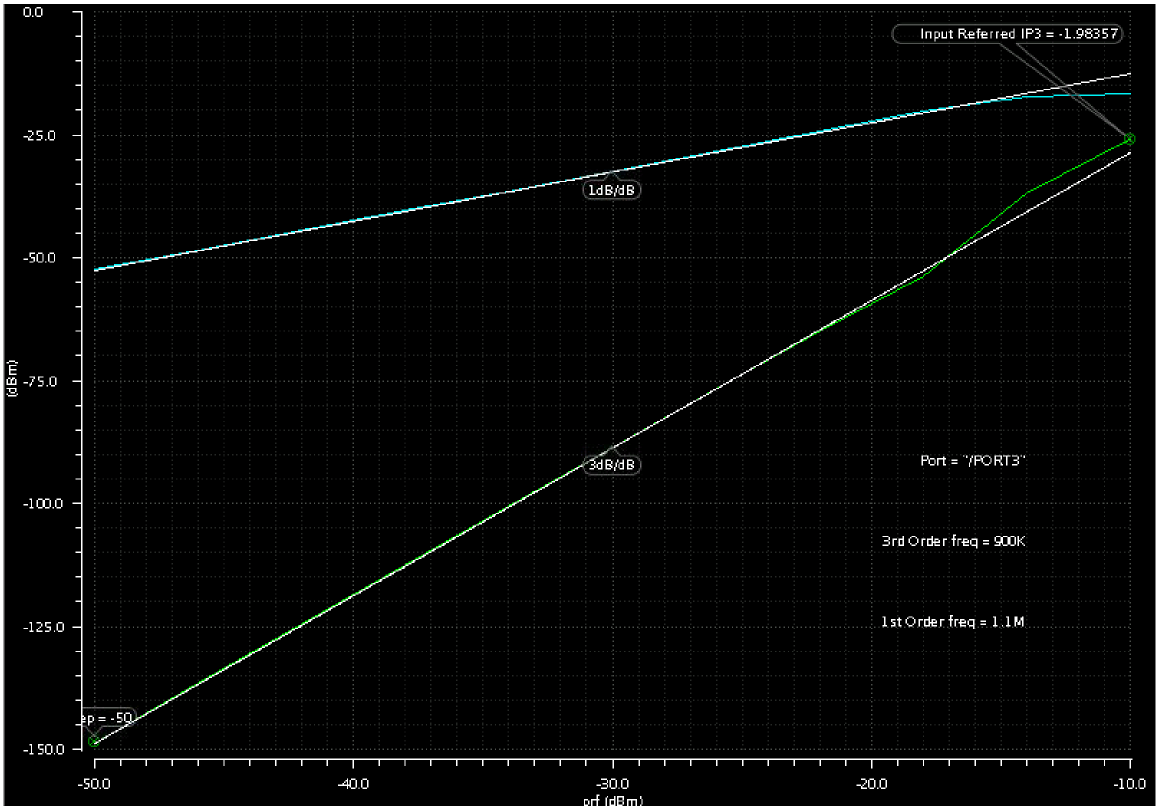
After the simulations finish, plot the IP3 and compare it with the results from Lab 9 (hb plus hbac simulations).

Action 10-11: In the Virtuoso Analog Design Environment window, choose **Results — Direct Plot — Main Form**.

Action 10-12: In the Direct Plot Form, select the *hb_mt* button, and configure the form as follows:


Direct Plot Form
Plotting Mode
Append
Analysis
hb_mt
Function
Voltage
Current
Power
Voltage Gain
Current Gain
Power Gain
Transconductance
Transimpedance
Compression Point
IPN Curves
Power Contours
Reflection Contours
Power Added Eff.
Power Gain Vs Pout
Comp. Vs Pout
Node Complex Imp.
Select
Port (fixed R(port))
Circuit Input Power
Single Point
Variable Sweep
("prf")
"prf" ranges from -50 to -10
Input Power Extrapolation Point (dBm)
(Defaults to -50)
Input Referred IP3
Order
3rd
Freq. (Hz) FLO RF1 RF2
3rd Order Harmonic
0 0 0 0
100K 0 -1 1
200K 0 -2 2
300K 0 -3 3
800K -1 3 -2
900K -1 2 -1
1st Order Harmonic
800K -1 3 -2
900K -1 2 -1
1M -1 1 0
1.1M -1 0 1
1.2M -1 -1 2
1.3M -1 -2 3
Add To Outputs
> Select Port on schematic...
OK
Cancel
Help

Action 10-13: Select output `Port3` on schematic. The IP3 calculation results looks like this.



Action 10-14: After viewing the waveforms, click *Cancel* in the Direct Plot Form.

Lab 11: Rapid IP3 (hbac)

Rapid Ip2/Ip3 based on perturbation technology extends both shooting and flexible balance. Rapid IM (IP2, IP3) calculations are an order of magnitude faster than using flexible balance or shooting alone.

Action 11-1: If it is not already open, open the *schematic* view of the *mixer_testbench* design in the library *RFworkshop*.

Action 11-2: From the *Mixer_testbench* schematic, choose **Launch — ADE L**.

The Virtuoso Analog Design Environment window appears.

Action 11-3: Select the `PORT0` source. Use the **Edit — Properties — Objects** command to ensure that the port properties are set as described below:

Parameter	Value
Resistance	50 ohm
Port Number	1
DC voltage	500 mV
Source type	*dc*
PAC magnitude (dBm)	pacm

Action 11-4: Click *OK* on the Edit Object Properties window to close it.

Action 11-5: Check and save the schematic.

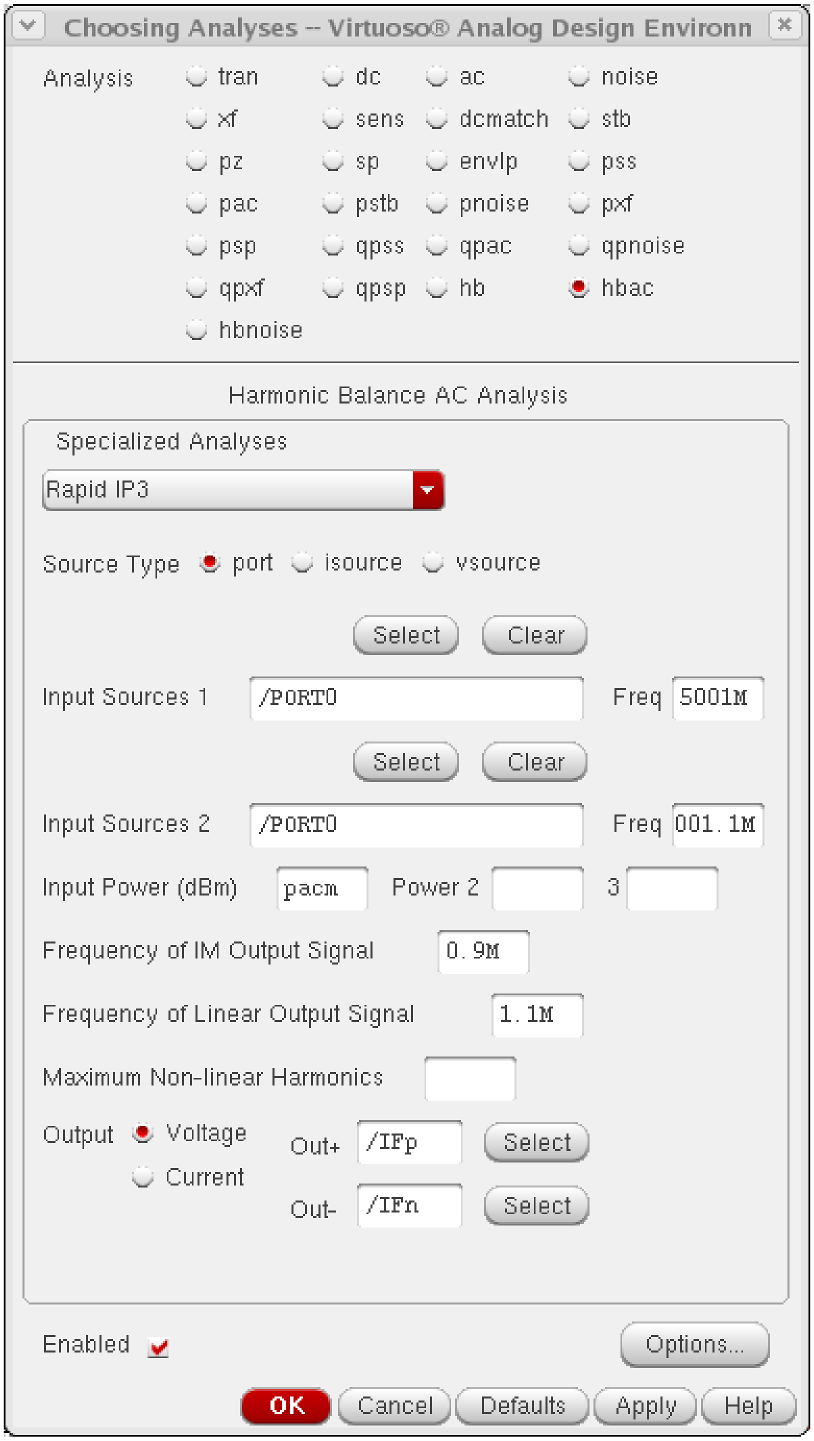
Action 11-6: You can choose **Session — Load State**, select **Cellview** in **Load State Option** and load state "**Lab11_Rapid_IP3_hbac**" and skip to Action 11-11 or …

Action 11-7: In the Virtuoso Analog Design Environment window, choose **Analyses — Choose**.

Action 11-8: In the Choosing Analyses window, select the *hb* button in the *Analysis* field of the window and set the form as shown in Action 2-6.

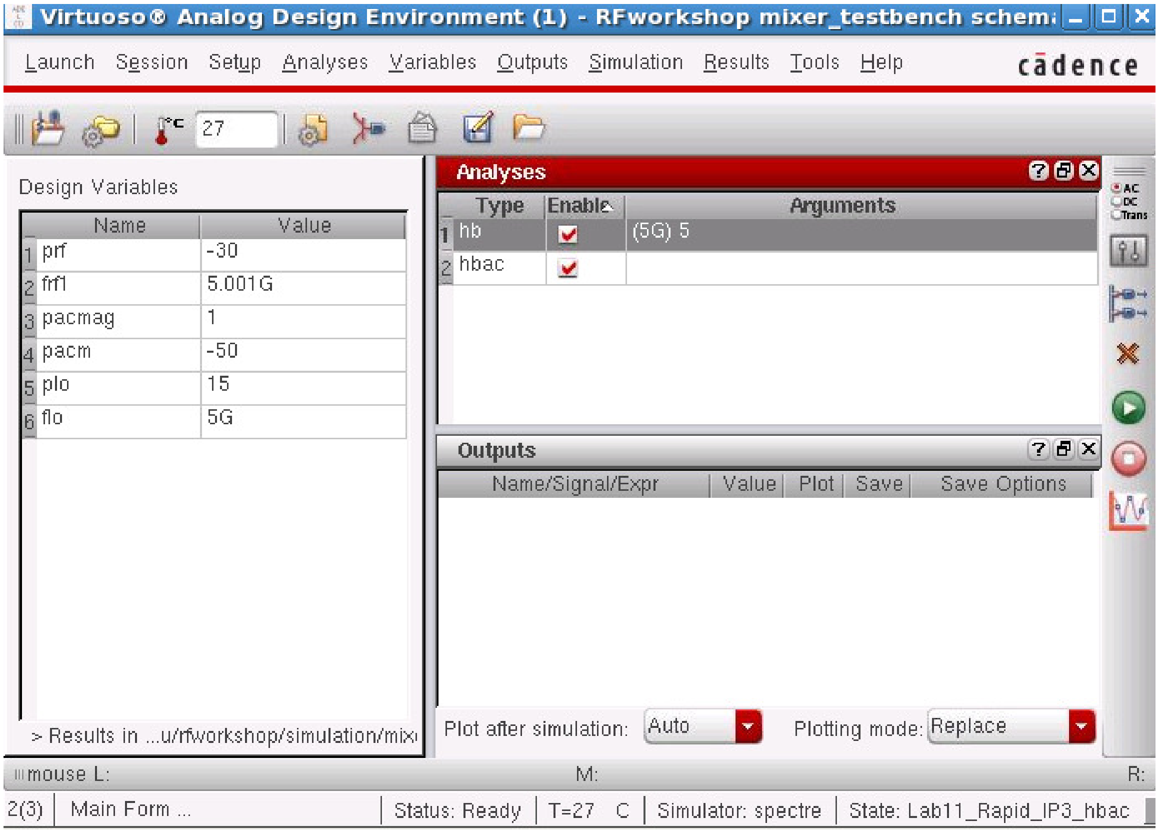
Action 11-9: In the Choosing Analyses window, select the *hbac* button in the *Analysis* field of the window. Choose *Rapid IP3* as *Specialized Analyses*. Set the *Input Sources 1* to `/PORT0` by selecting `PORT0` on the schematic. Press ESC to terminate the selection process.

Set the *Freq* of source 1 to 5001M and *Freq* of Source 2 to 5001.1M. Set the *Frequency of IM Output Signal* as 0.9M and the *Frequency of Linear Output Signal* as 1.1M. The form looks like this.



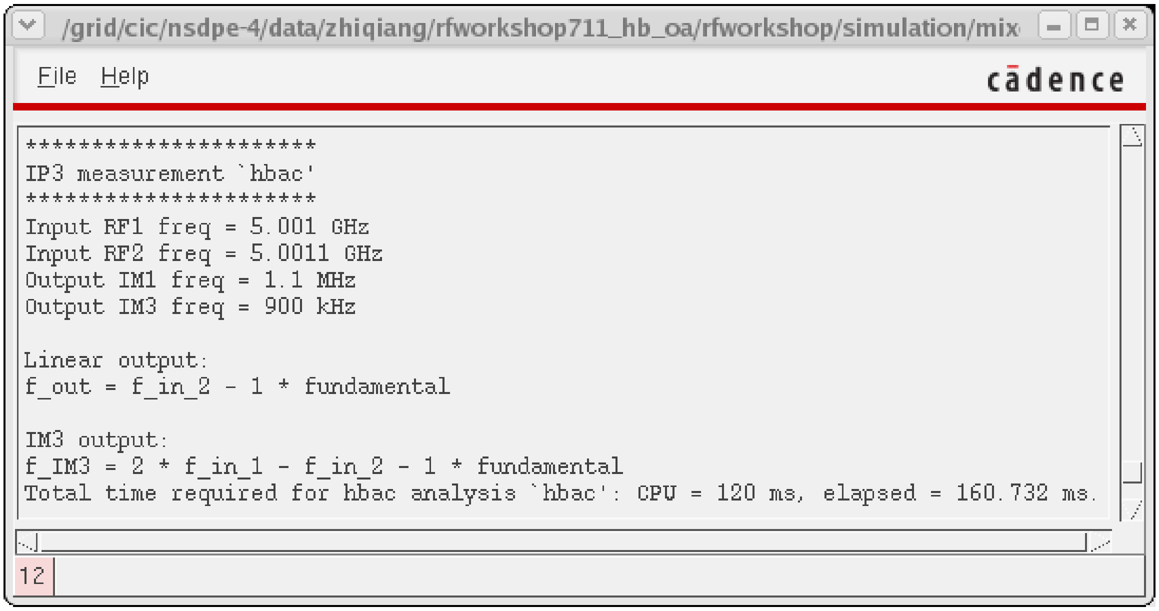
Action 11-10: Make sure the *Enabled* button is on. In the Choosing Analyses window, click *OK*.

The Virtuoso Analog Design Environment window looks like this.

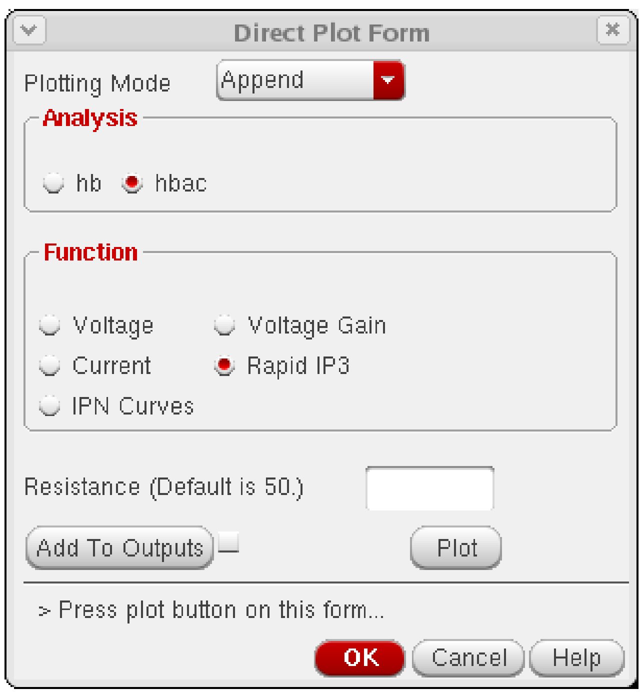


Action 11-11: In the Virtuoso Analog Design Environment window, choose **Simulation — Netlist and Run** or click the **Netlist and Run** icon to start the simulation.

As the simulation progresses, messages similar to the following appear in the simulation output log window:

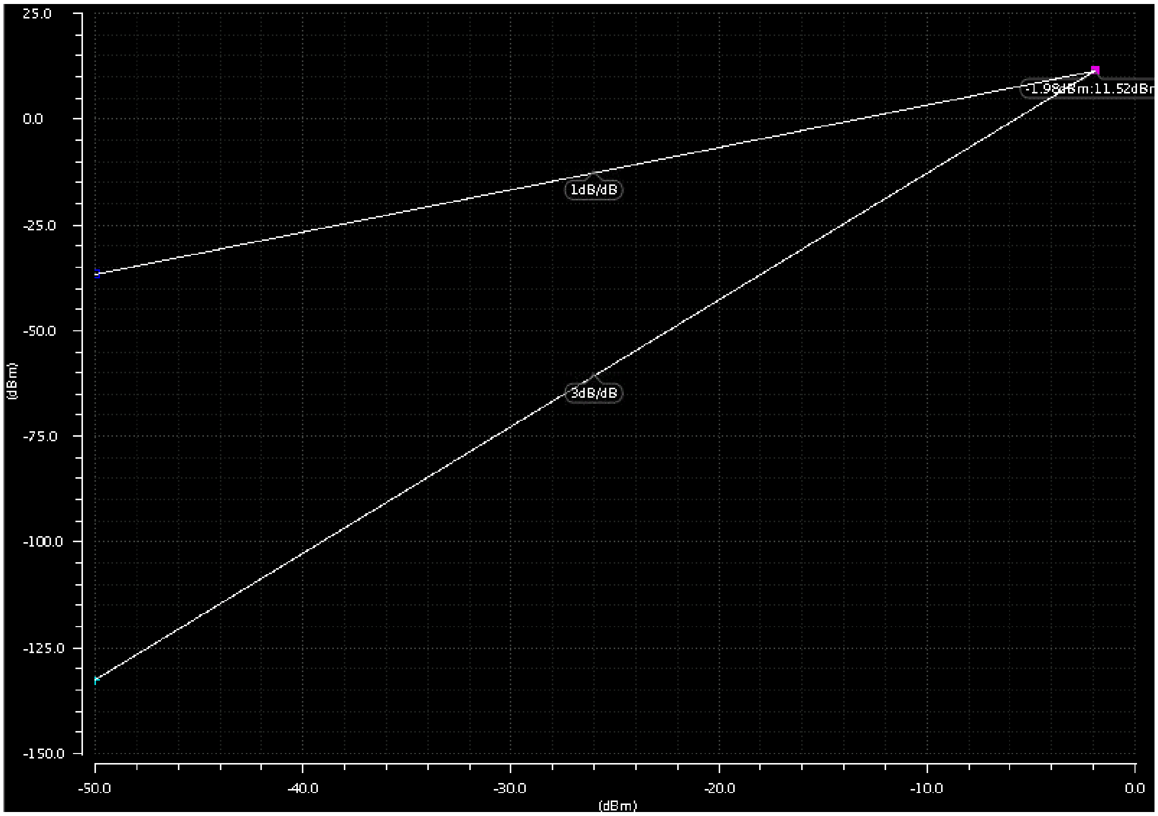


Action 11-12: In the Direct Plot form select the *hbac* button, and choose *Rapid IP3*. The form looks like this.



Action 11-13: Click *Plot*.

The calculated IP3 appears in the waveform window:



Action 11-14: Close the waveform window and click *Cancel* on the Direct Plot Form.

Lab 12: Compression Distortion Summary (hbac)

Action 12-1: If it is not already open, open the *schematic* view of the *mixer_testbench* design in the library *RFworkshop*.

Action 12-2: Select PORT0. Use the **Edit — Properties — Objects** command to ensure that the port properties are set as described below:

Parameter	Value
Resistance	50 ohm
Port Number	1
DC voltage	500 mV
Source type	*dc*
PAC Magnitude (dBm)	pacm

Action 12-3: Click *OK* on the Edit Object Properties window to close it.

Action 12-4: Check and save the schematic.

Action 12-5: From the *Mixer_testbench* schematic, choose **Launch — ADE L**.

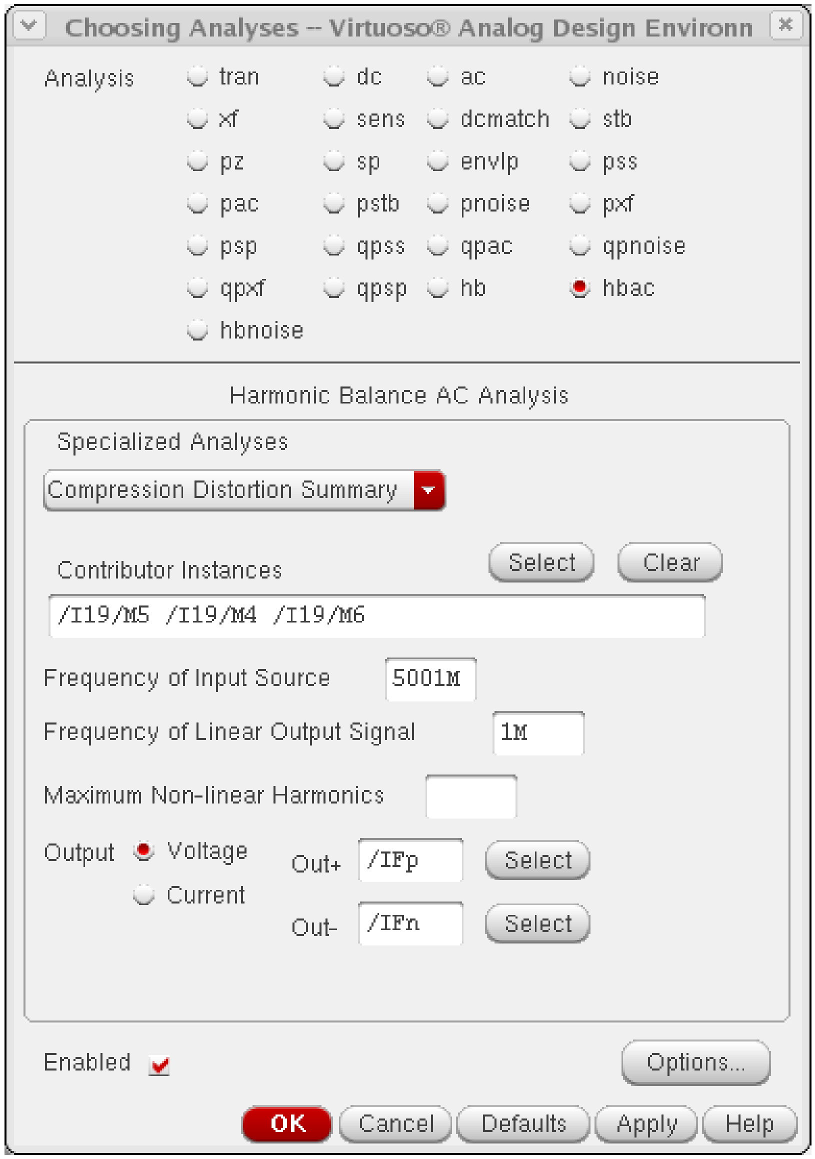
The Virtuoso Analog Design Environment window appears.

Action 12-6: You can choose **Session — Load State**, select **Cellview** in **Load State Option** and load state "**Lab12_CompDistorSmry_hbac**" and skip to Action 12-11 or …

Action 12-7: In the Virtuoso Analog Design Environment window, choose **Analyses — Choose**.

Action 12-8: In the Choosing Analyses window, select the *hb* button in the *Analysis* field of the window and set the form as shown in Action 2-6.

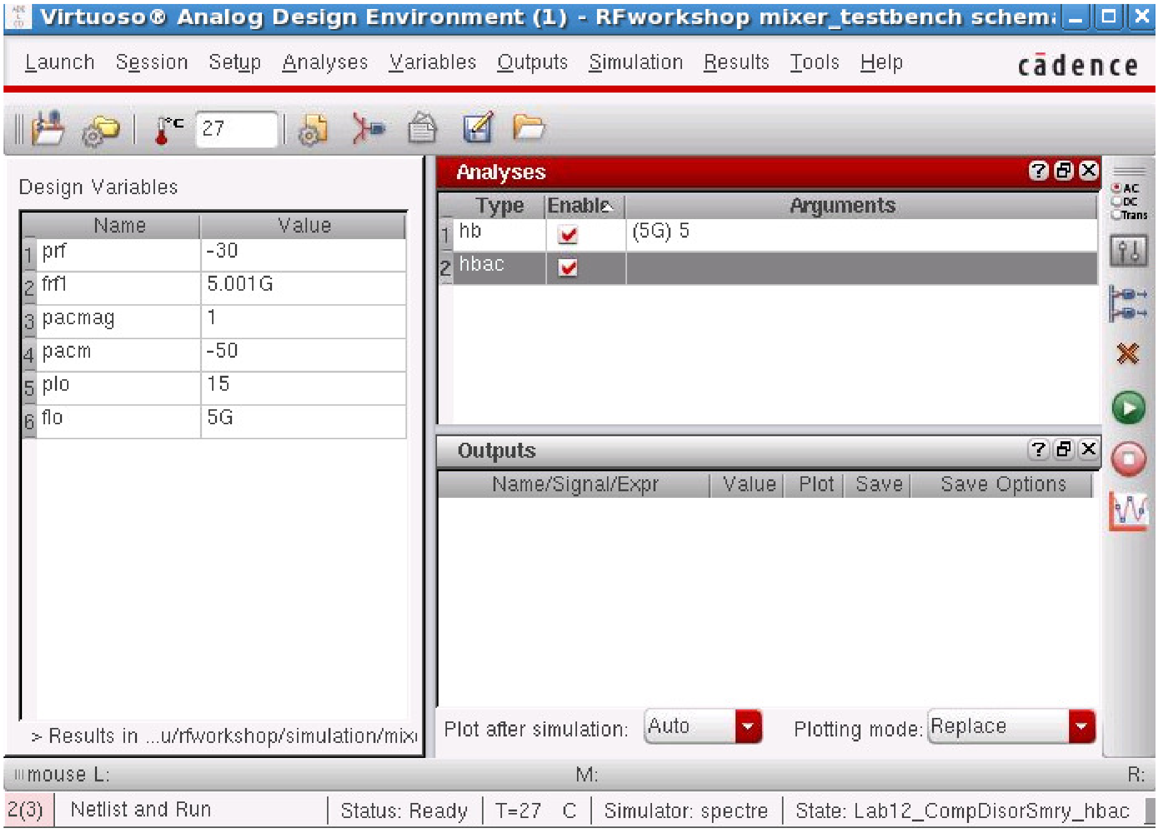
Action 12-9: In the Choosing Analyses window, select the *hbac* button in the *Analysis* field of the window and set the form as follows:



In the above form, the Maximum Non-linear Harmonics is not specified, so the default value 4 is used.

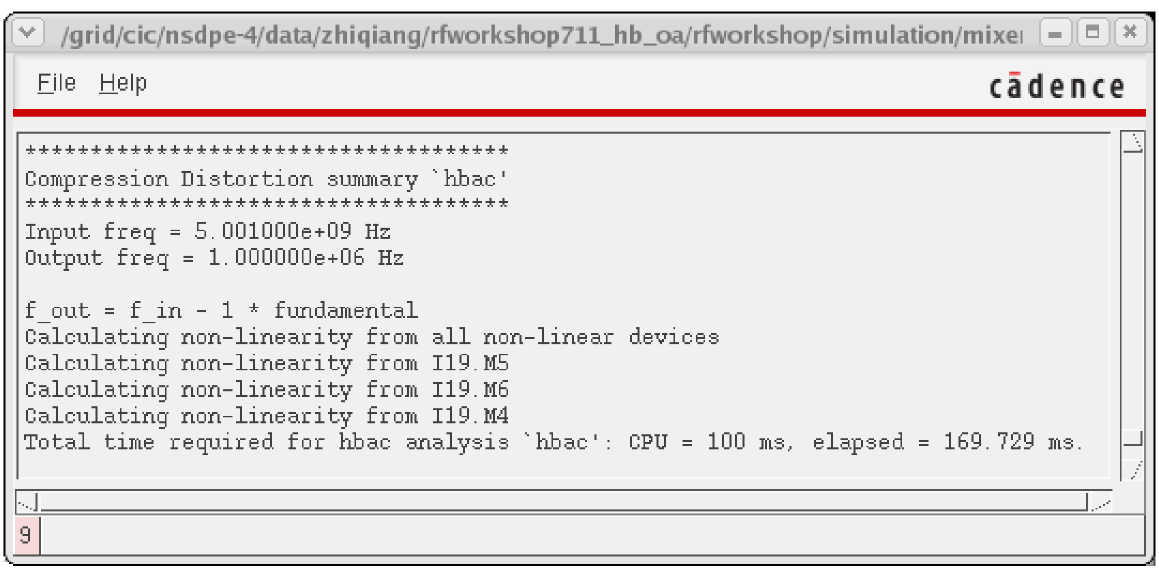
Action 12-10: Make sure the *Enabled* button is on. In the Choosing Analyses window, click *OK*.

The Virtuoso Analog Design Environment window looks like this.



Action 12-11: In the Virtuoso Analog Design Environment, choose **Simulation — Netlist and Run** or click the **Netlist and Run** icon to start the simulation.

As the simulation progresses, messages similar to the following appear in the simulation output log window:



Action 12-12: After the simulation completes, go to the Virtuoso Analog Design Environment window and choose **Results — Print — HBAC Distortion Summary.**

The Results Display Window appears:

```
HBAC Compression Distortion Summary

Results in          hbac_distortion

                                        Nonlinear Mag at 1st 2nd & 3rd harm of linear freq (V)
Instance            Distortion(dB)      freq=1e+06          freq=2e+06          freq=3e+06
Total               -1.50316m           845.416n            19.9714n            19.3822p
I19.M6              -1.24837m           687.571n            10.2466n            5.48893p
I19.M5              -139.588u           111.644n            5.09329n            7.9658p
I19.M4              -139.588u           111.644n            5.09329n            7.9658p
```

Action 12-13: After viewing the results, close it by choosing **Window — Close**.

Lab 13: Rapid IP2 (hbac)

Action 13-1: If it is not already open, open the *schematic* view of the *mixer_testbench* design in the library *Rfworkshop.*

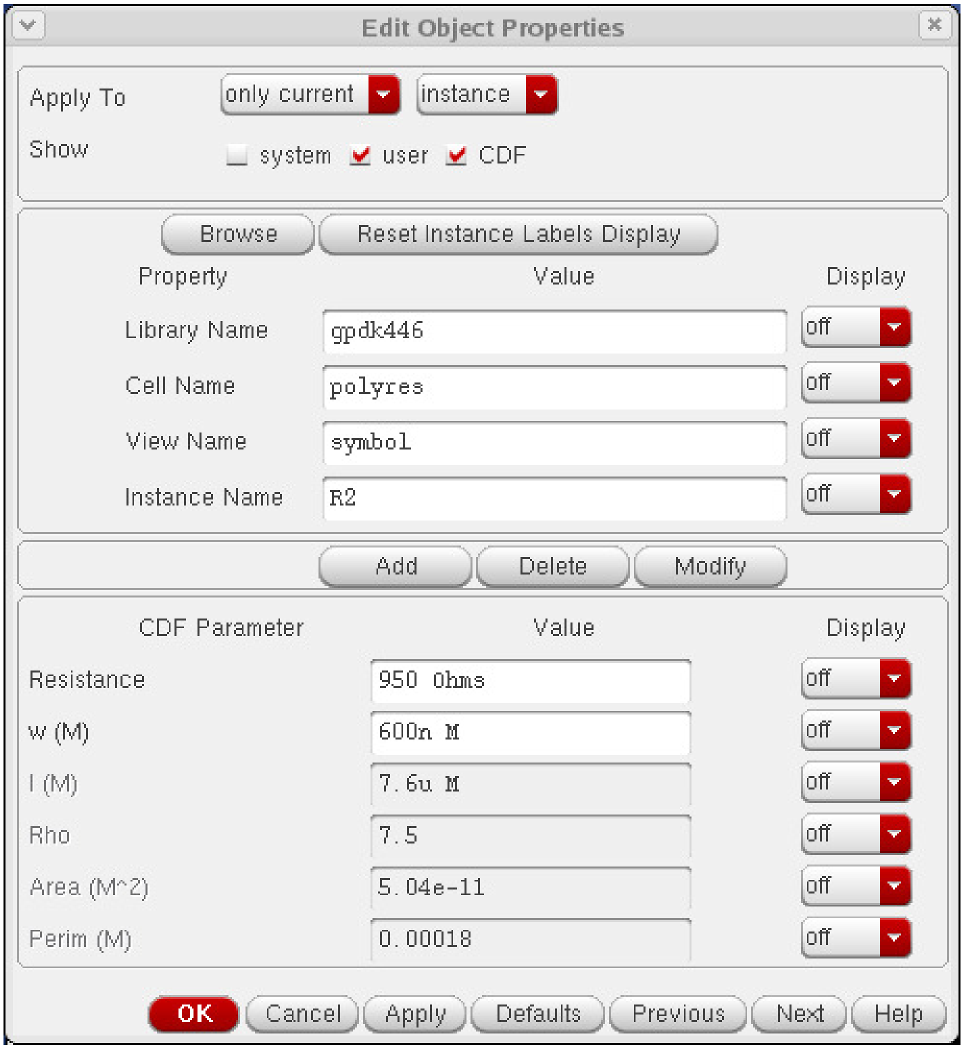
Action 13-2: Use the mouse to select the `PORT0` source. Then in the Virtuoso Schematic Editor select **Edit — Properties — Objects.**

The Edit Object Properties window for the port cell appears. Set the *Source type* to *dc*.

Parameter	**Value**
Resistance	50 ohm
Port Number	1
DC voltage	500 mV
Source type	*dc*

Action 13-3: Click *OK* on the Edit Object Properties window to close it.

Action 13-4: Use the mouse to select the `mixer` cell. Then in the Virtuoso Schematic Editor select **Edit — Hierarchy — Descend Edit…,** click *OK* on the Descend window, and change the *Resistance* parameter of the R2 instance from 1K to 950**.** Check and save the schematic.



The IP2 of a double balanced /symmetric mixer will tend towards infinity if the device mismatch in the commutating mixer core is not included. Mismatch is typically the primary mechanism by which the IM2 products appear in the baseband mixer output. Another possible source can be the RF-LO leakage. In this lab, we manually introduced a mismatch in the mixer load circuitry. In practice, the user should run monte carlo simulation to get IP2 value or derive the device matching information from the process/technology documentation.

Action 13-5: From the *Mixer_testbench* schematic, choose **Launch — ADE L**.

The Virtuoso Analog Design Environment window appears.

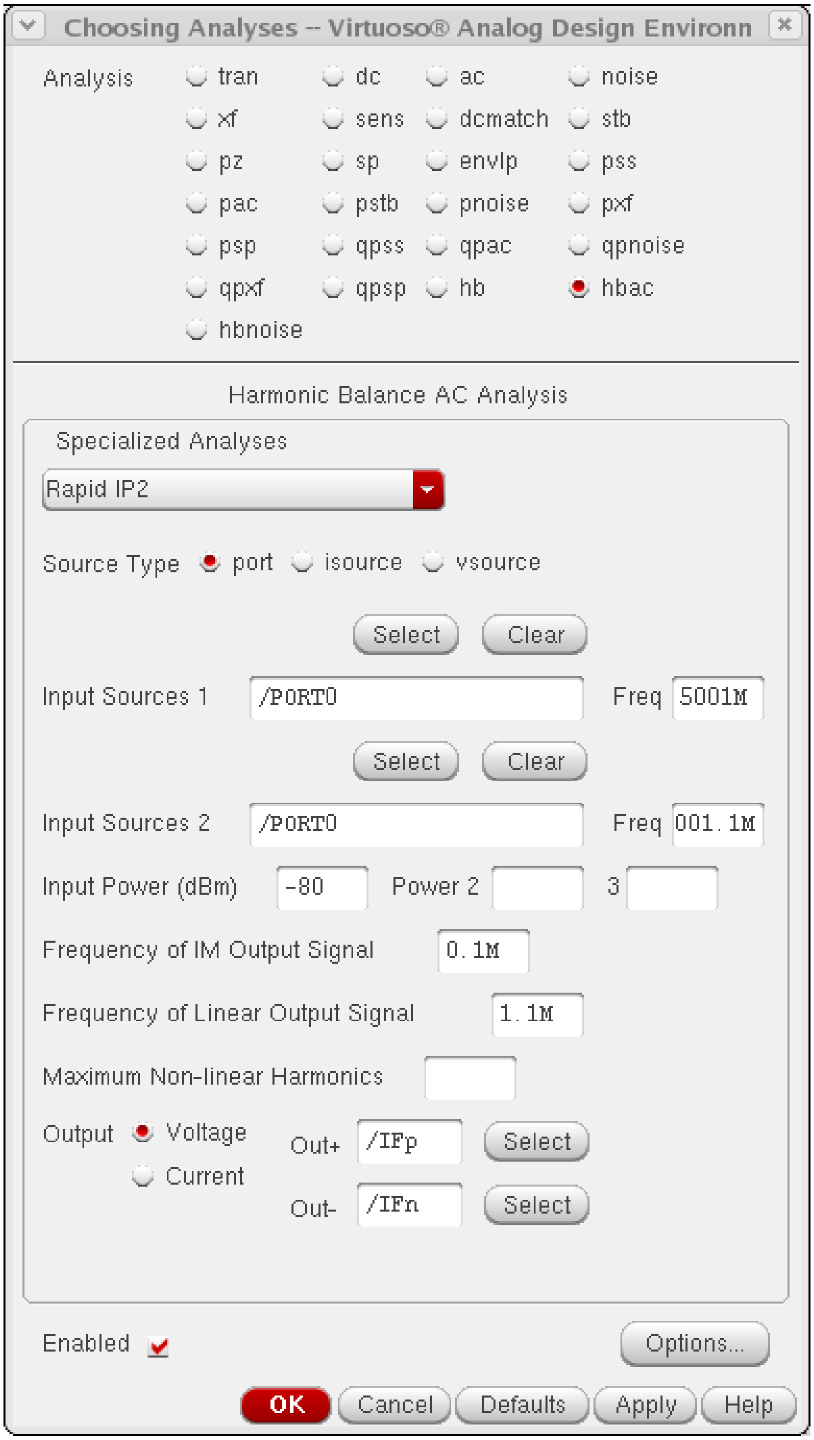
Action 13-6: You can choose **Session — Load State**, select **Cellview** in **Load State Option** and load state "**Lab13_Rapid_IP2_hbac**" and skip to Action 13-12 or …

Action 13-7: In the Virtuoso Analog Design Environment window, choose **Analyses — Choose**.

Action 13-8: In the Choosing Analyses window, select the *hb* button in the *Analysis* field of the window and set the form as shown in Action 2-6.

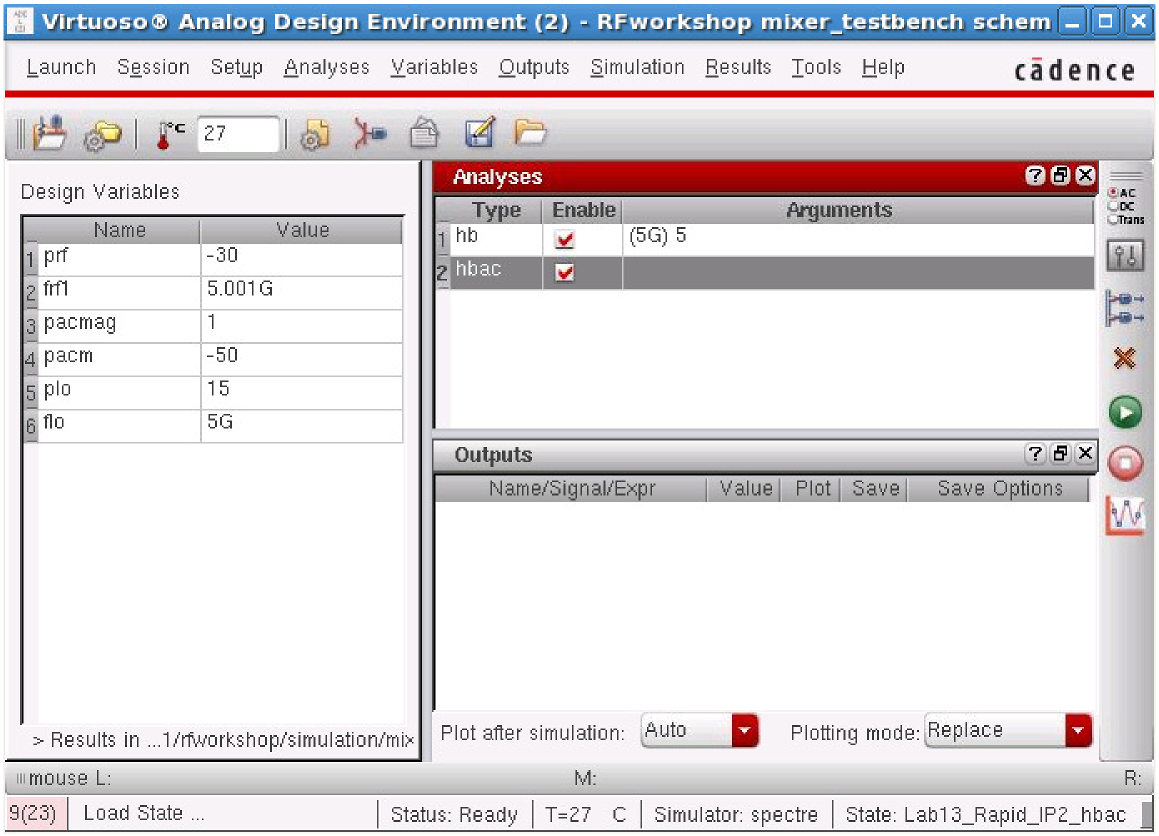
Action 13-9: Make sure the *Enabled* button is on. In the Choosing Analyses window, click *Apply*.

Action 13-10: In the Choosing Analyses window, select the *hbac* button in the *Analysis* field of the window. In the *Specialized Analyses* field, choose *Rapid IP2*. Set *Input Sources 1* to `/PORT0` by selecting `PORT0` on the schematic. Press the ESC key to terminate the selection process.
Set the *Freq* of source 1 to 5001M and *Freq* of Source 2 to 5001.1M. Set the *Frequency of IM Output Signal* as 0.1M and the *Frequency of Linear Output Signal* as 1.1M. The form looks like this.



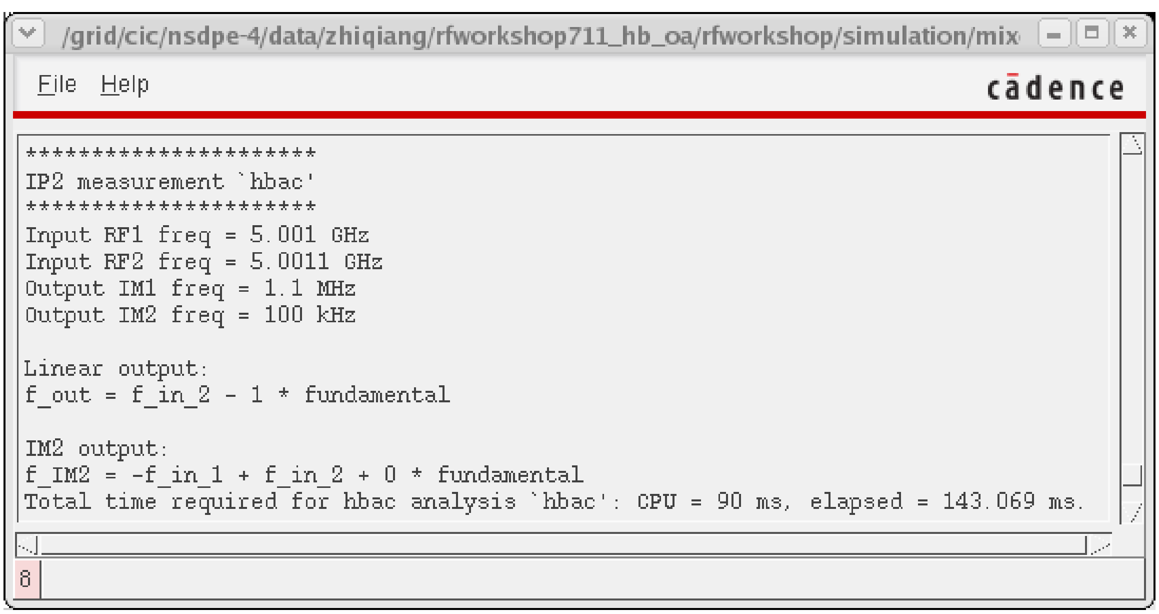
Action 13-11: Make sure the *Enabled* button is on. In the Choosing Analyses window, click *OK*.

The Virtuoso Analog Design Environment window looks like this.



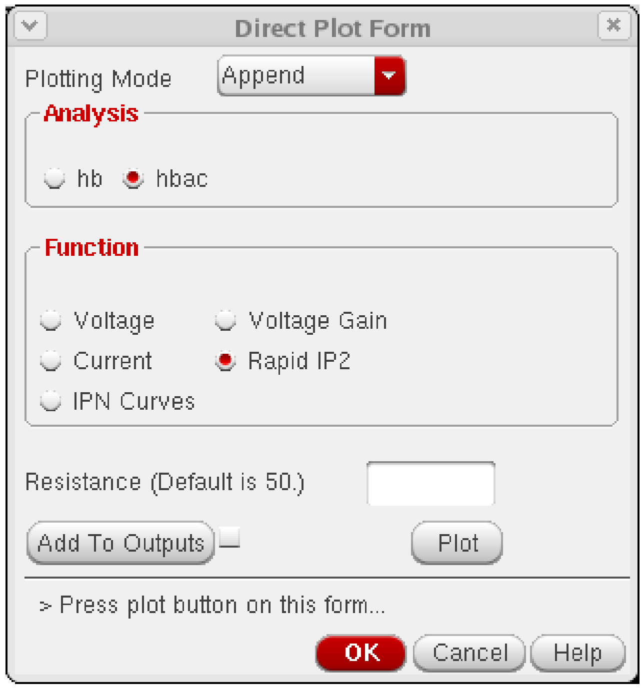
Action 13-12: In the Virtuoso Analog Design Environment window, choose **Simulation — Netlist and Run** or click the **Netlist and Run** icon to start the simulation.

As the simulation progresses, messages similar to the following appear in the simulation output log window:

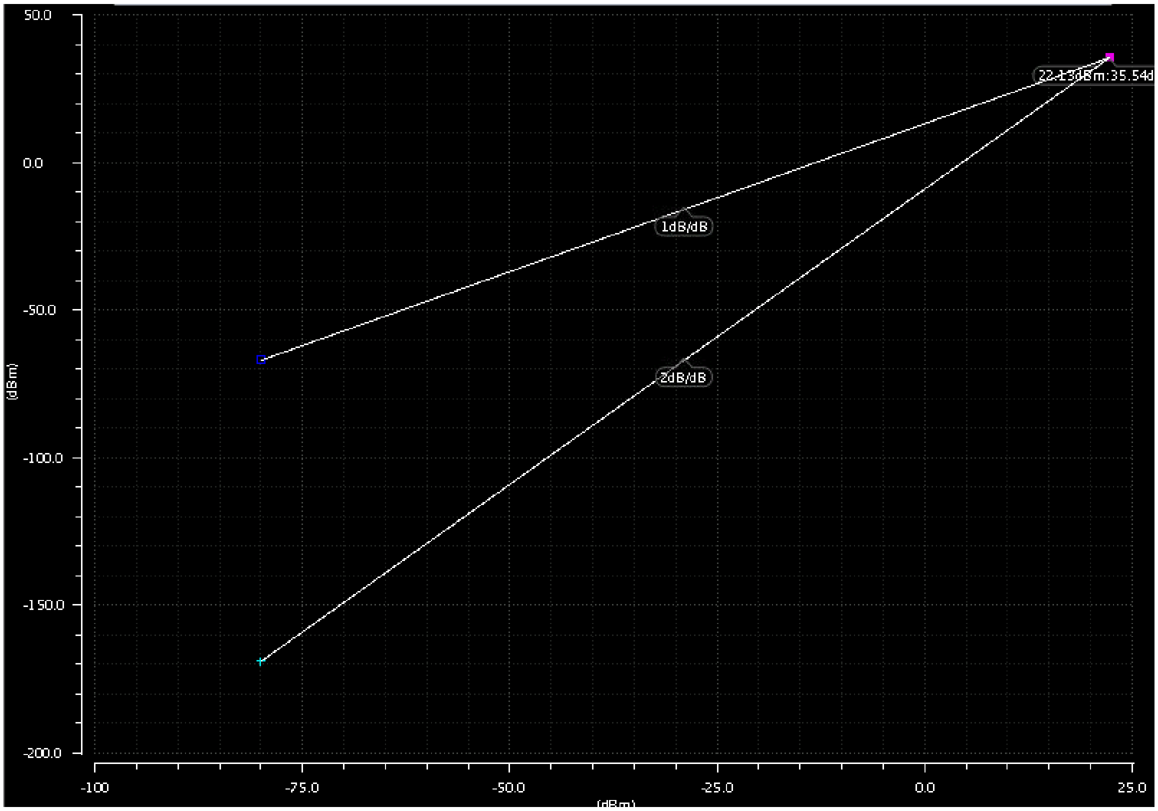


Action 13-13: In the Virtuoso Analog Design Environment window, choose **Results — Direct Plot — Main Form**.

Action 13-14: In the Direct Plot Form, select the *hbac* button in analysis field and choose *Rapid IP2* in the *Function* field.



Action 13-15: Click *Plot*.



Action 13-16: Close the waveforms window and click *Cancel* in the Direct Plot Form.

Action 13-16: Use the mouse to select the `mixer` cell. Then in the Virtuoso Schematic Editor select **Edit — Hierarchy — Descend Edit…,** click *OK* on the Descend window, and change the *Resistance* parameter of the R2 instance from 950 to 1K**.** Check and save the schematic.

Lab 14: IM2 Distortion Summary (hbac)

Action 14-1: If it is not already open, open the *schematic* view of the *mixer_testbench* design in the library *Rfworkshop.*

Action 14-2: Make sure the *Source type* of `PORT0` is *dc*.

Parameter	**Value**
Resistance	50 ohm
Port Number	1
DC voltage	500 mV
Source Type	*dc*

Action 14-3: Check and save the schematic.

Action 14-4: From the *Mixer_testbench* schematic, choose **Launch — ADE L**.

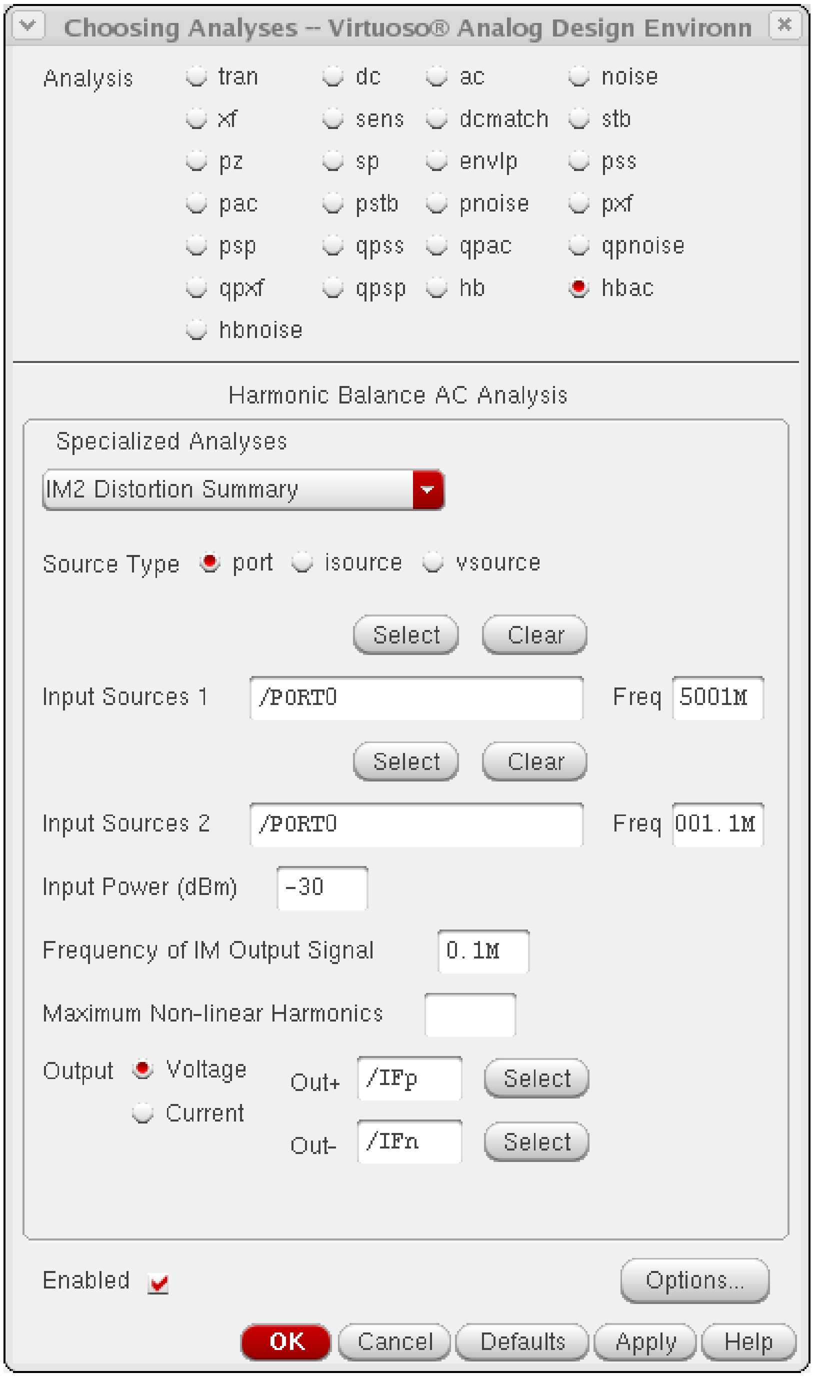
The Virtuoso Analog Design Environment window appears.

Action 14-5: You can choose **Session — Load State**, select **Cellview** in **Load State Option** and load state "**Lab14_IM2DistorSmary_hbac**" and skip to Action 14-10 or …

Action 14-6: In the Virtuoso Analog Design Environment window, choose **Analyses — Choose**.

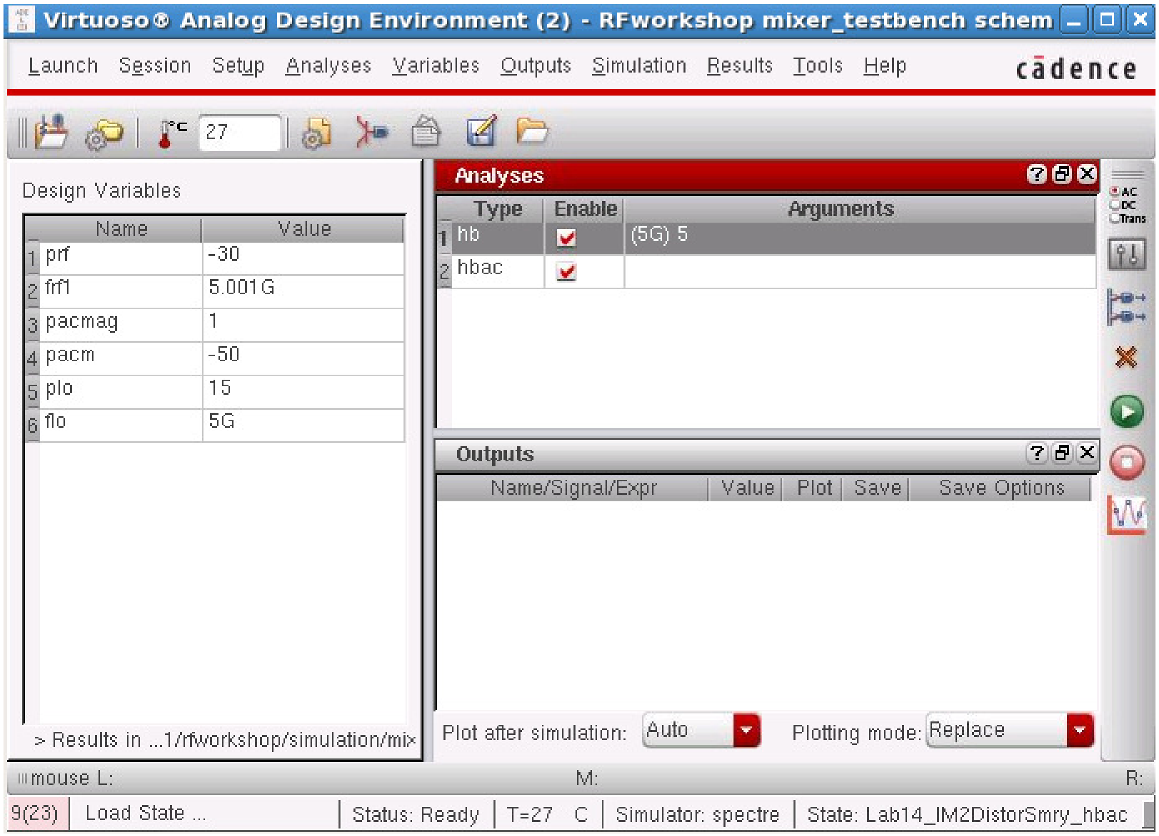
Action 14-7: In the Choosing Analyses window, select the *hb* button in the *Analysis* field of the window and set the form as you did in the Rapid IP2 simulation.

Action 14-8: In the Choosing Analyses window, select the *hbac* button in the *Analysis* field of the window. In the *Specialized Analyses* field, choose *IM2 Distortion Summary*. Set *Input Sources 1* to `/PORT0` by selecting `PORT0` on the schematic. Press the ESC key to terminate the selection process. Set the *Freq* of source 1 to 5001M and *Freq* of Source 2 to 5001.1M. Set the *Frequency of IM Output Signal* as 0.1M. The form looks like this.



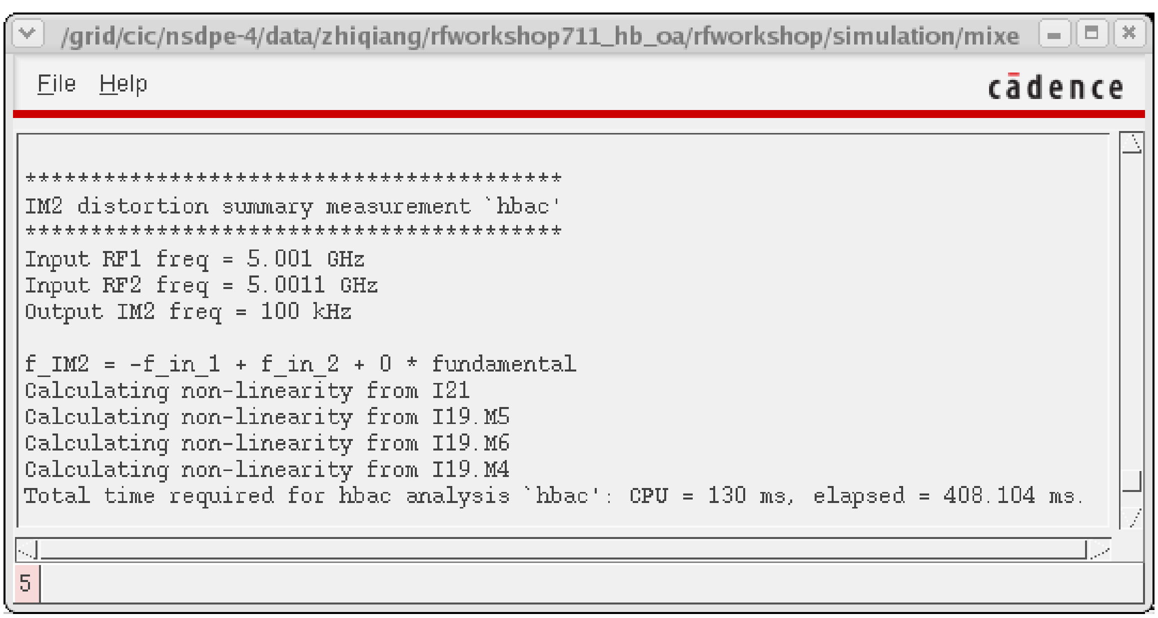
Action 14-9: Make sure the *Enabled* button is on. In the Choosing Analyses window, click *OK*.

The Virtuoso Analog Design Environment window looks like this.



Action 14-10: In the Virtuoso Analog Design Environment window, choose **Simulation — Netlist and Run** or click the **Netlist and Run** icon to start the simulation.

As the simulation progresses, messages similar to the following appear in the simulation output log window:



Action 14-11: In the Virtuoso Analog Design Environment window, choose **Results — Print — HBAC Distortion Summary.**

The Results Display Window shows the PAC IM2 Distortion Summary.

```
HBAC IM2 Distortion Summary

Results in        hbac_im2distortion

Instance          Distortion(V)[Magnitude Complex]
Total             21.7622p    complex(21.7595p, 344.067f)
/I19/M5           386.286u    complex(-386.27u, -3.46419u)
/I19/M4           386.286u    complex(386.27u, 3.46419u)
/I19/M6           57.7075p    complex(57.7038p, 650.691f)
/I21              50.1114a    complex(50.0249a, -2.94262a)
```

The distortion is listed in dB for each instance. Due to the very low RF input power, the distortion is very small.

Action 14-12: After viewing the distortion summary report, close it by choosing **Window — Close**.

Conclusion

This workshop illustrates how to use SpectreRF to simulate a mixer and to extract design parameters such as IP3, 1dB compression point, or port-to-port isolation. Various techniques using hb, hbac, hbnoise, hbsp, PSS, Pnoise, PAC, and QPSS analyses are demonstrated. SpectreRF Flexible Balance and Time domain algorithms are demonstrated and their accuracies are compared.

References

[1] "The Designer's Guide to Spice & Spectre", Kenneth S. Kundert, Kluwer Academic Publishers, 1995.

[2] "Microwave Transistor Amplifiers", Guillermo Gonzalez, Prentice Hall, 1984.

[3] "RF Microelectronics", Behzad Razavi. Prentice Hall, NJ, 1998.

[4] "The Design of CMOS Radio Frequency Integrated Circuits", Thomas H. Lee. Cambridge University Press, 1998.