Noise Analysis in Switched-Capacitor Circuits

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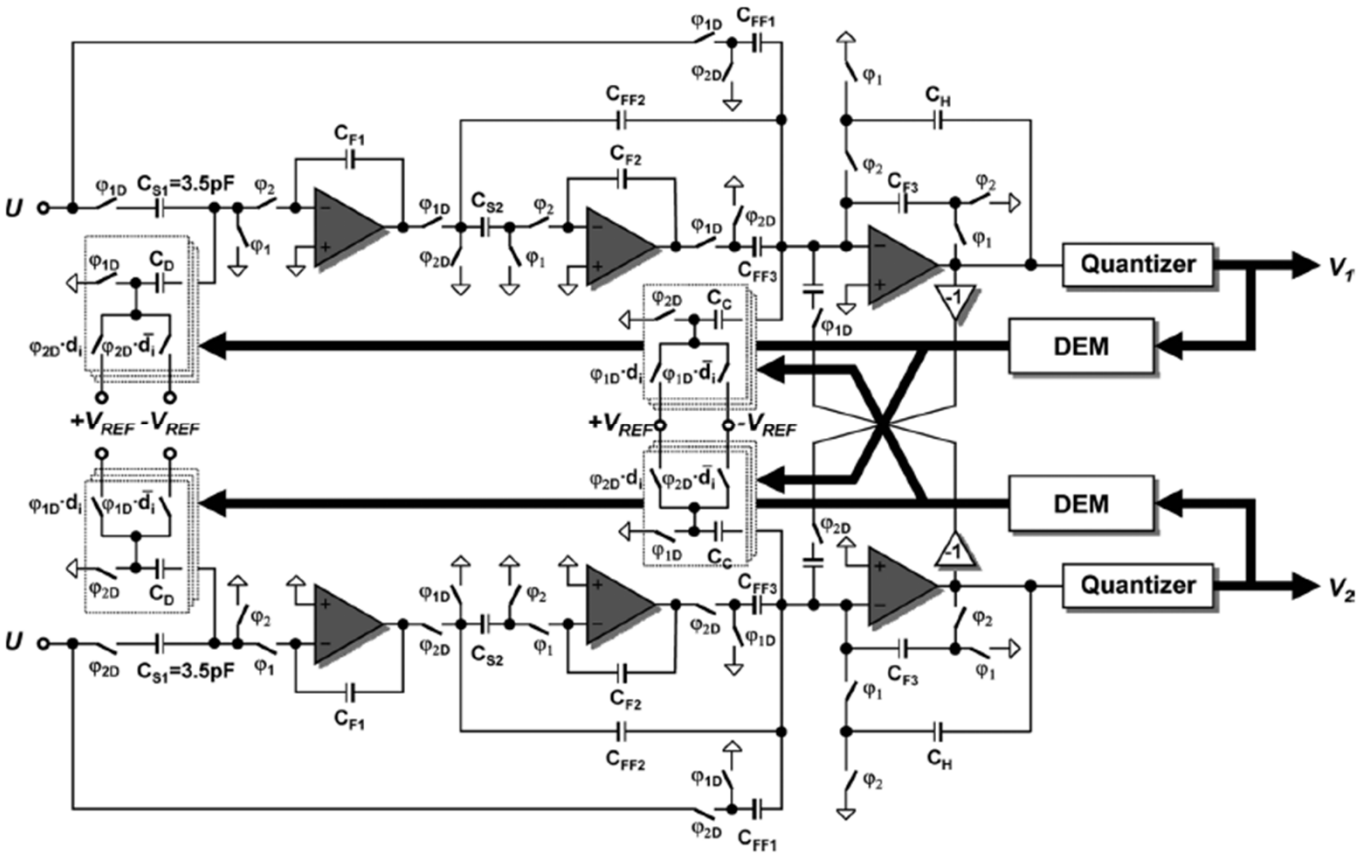
Abstract

Switched-capacitor (SC) circuits are ubiquitous in CMOS mixed-signal ICs. The most fundamental performance limitation in these circuits stems from the thermal noise introduced by MOSFET switches and active amplifier circuitry. This tutorial reviews hand analysis techniques that allow the designer to predict the noise performance of switched-capacitor circuits at various levels of complexity. The material presented in this course focuses on practical examples ranging from basic passive and active track-and-hold circuits, integrators and SC delta-sigma modulators. Simulation examples are included to complement and verify the theoretical treatment.

Outline

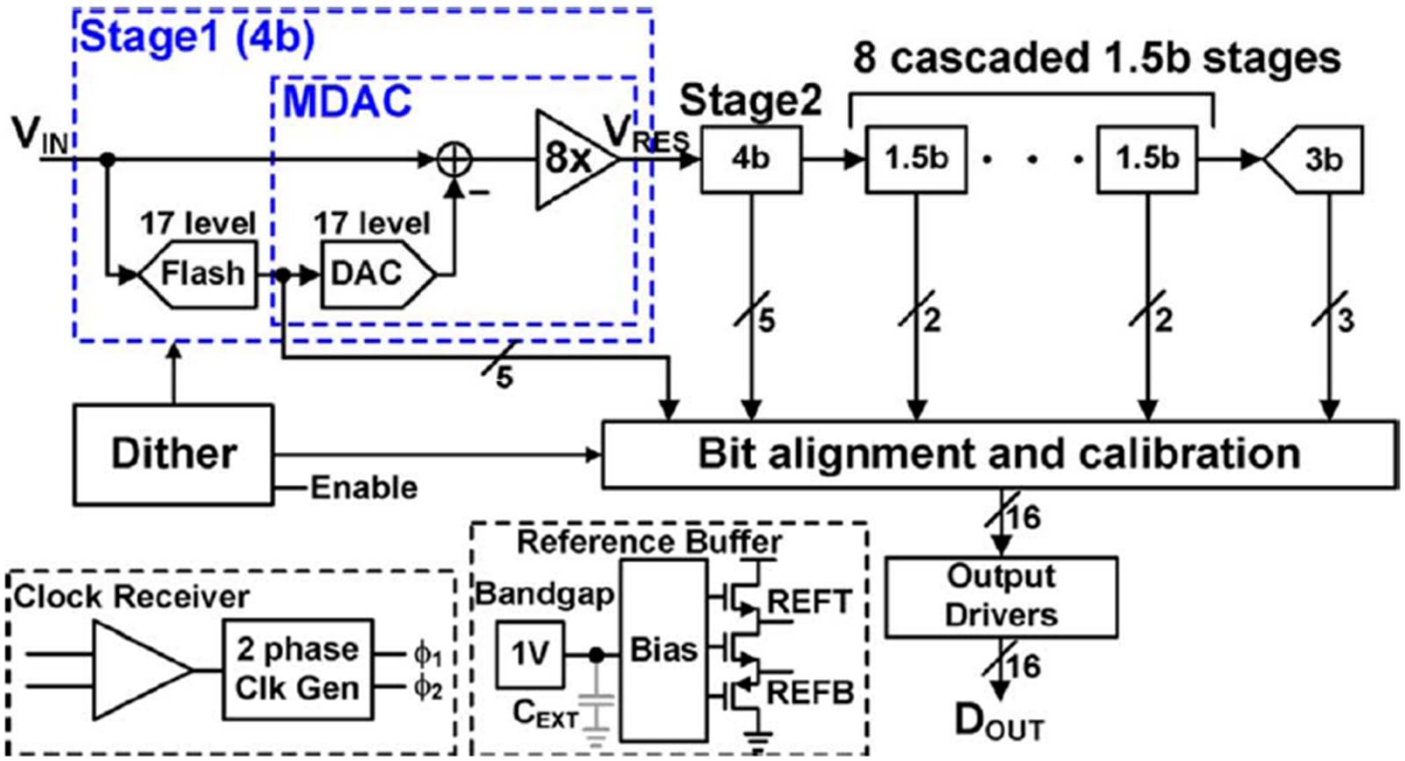
- Motivation and Overview
- Preliminaries
- Circuit Examples
  - Elementary track-and-hold circuit
  - Charge redistribution stage
  - Delta-sigma modulator

Example: Delta-Sigma Modulator



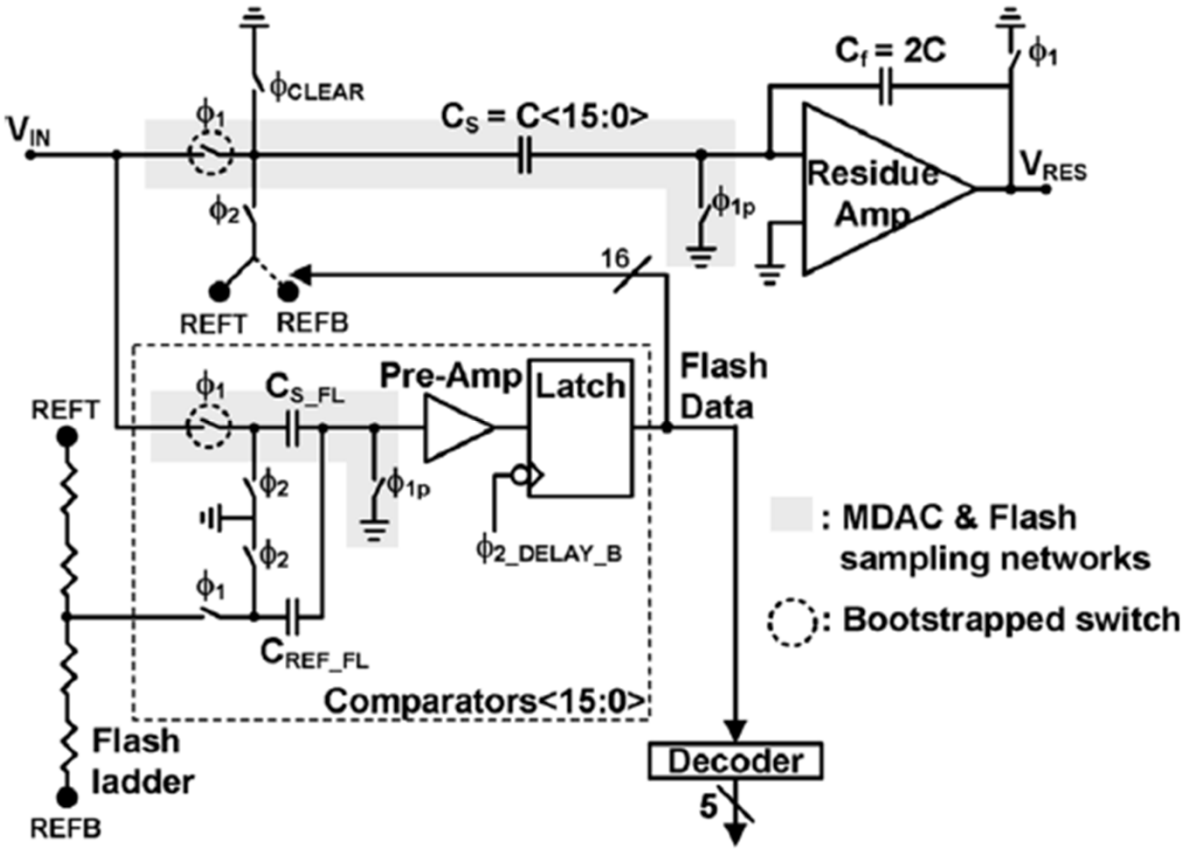
Kyehyung Lee, Jeongseok Chae, M. Aniya, K. Hamashita, K. Takasuka, S. Takeuchi, and G.C. Temes, "A Noise-Coupled Time-Interleaved Delta-Sigma ADC With 4.2 MHz Bandwidth, 98 dB THD, and 79 dB SNDR," IEEE J. Solid-State Circuits, vol.43, no.12, pp. 2601-2612, Dec. 2008.

Example: Pipeline ADC



S. Devarajan, L. Singer, D. Kelly, S. Decker, A. Kamath, P. Wilkins, "A 16-bit, 125 MS/s, 385 mW, 78.7 dB SNR CMOS Pipeline ADC," IEEE J. Solid-State Circuits, vol. 44, no. 12, pp. 3305-3313, Dec. 2009.

Example: Pipeline ADC



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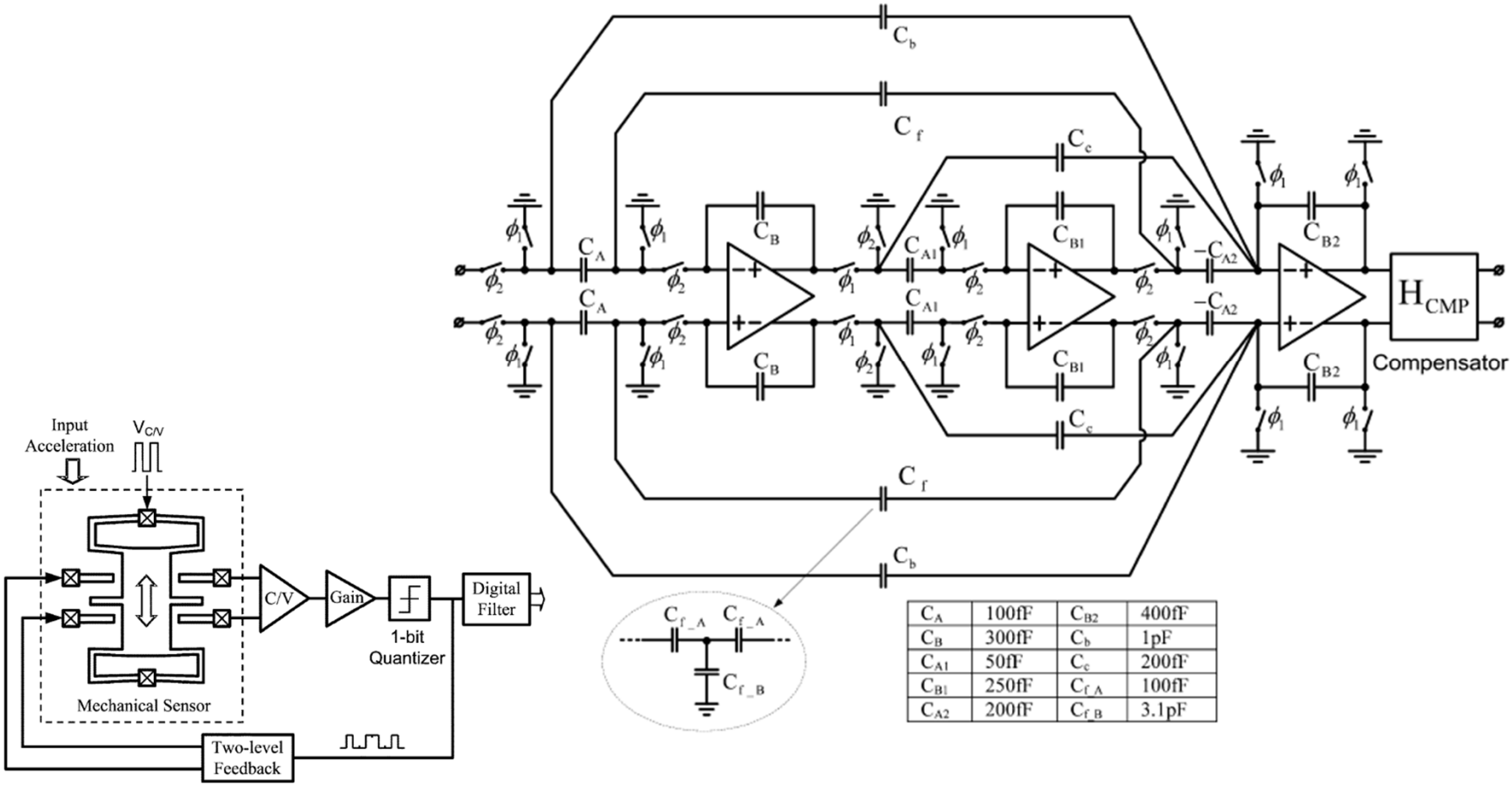
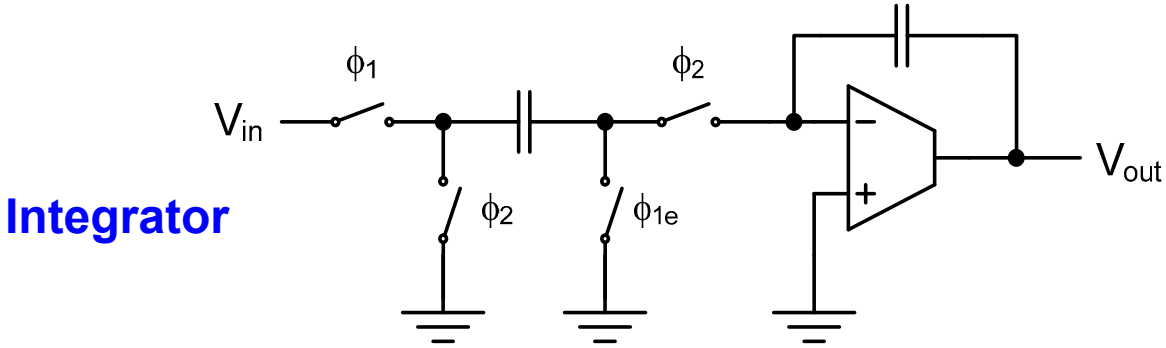
Example: Sensor Interface

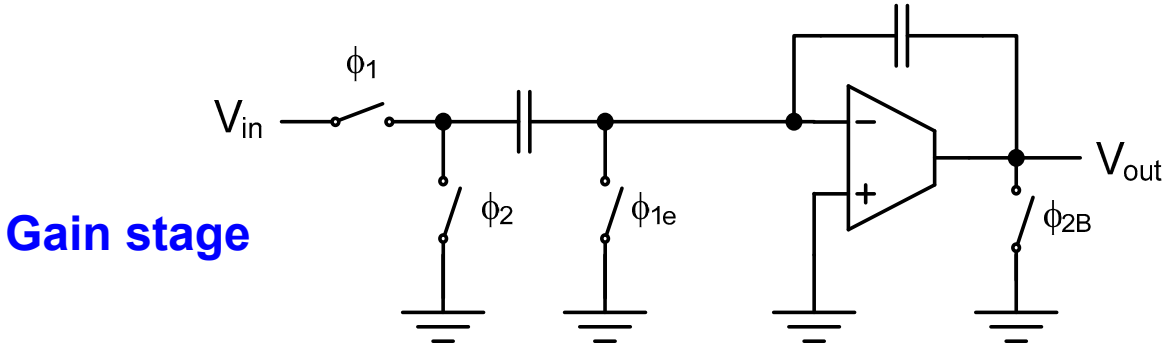


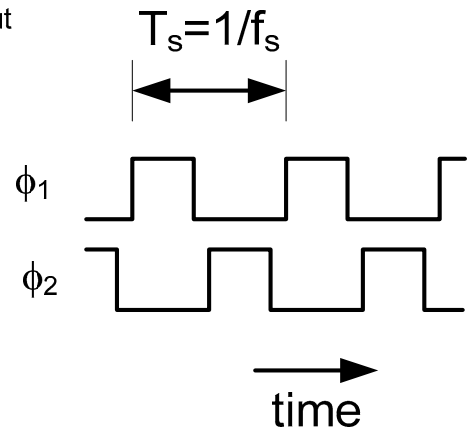
C_A	100fF	C_{B2}	400fF
C_B	300fF	C_b	1pF
C_{A1}	50fF	C_e	200fF
C_{B1}	250fF	C_{f_A}	100fF
C_{A2}	200fF	C_{f_B}	3.1pF

V.P. Petkov, B.E. Boser, "A fourth-order ΣΔ interface for micromachined inertial sensors," IEEE J. Solid-State Circuits, vol. 40, no. 8, pp. 1602-1609, Aug. 2005.

Charge Redistribution Stages

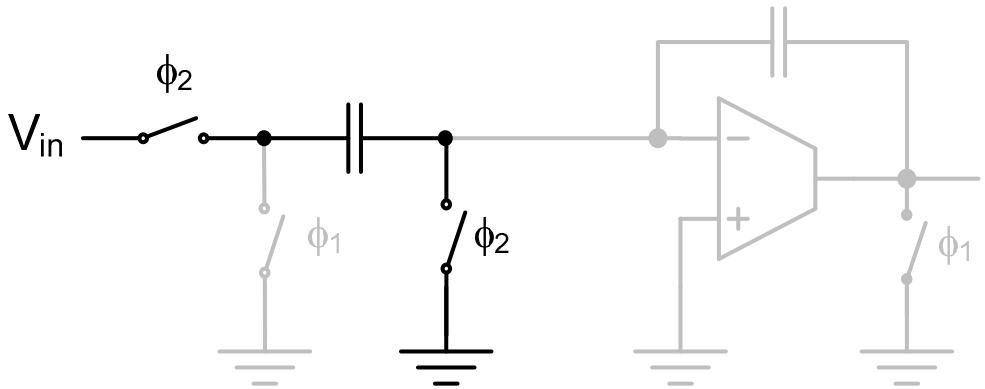


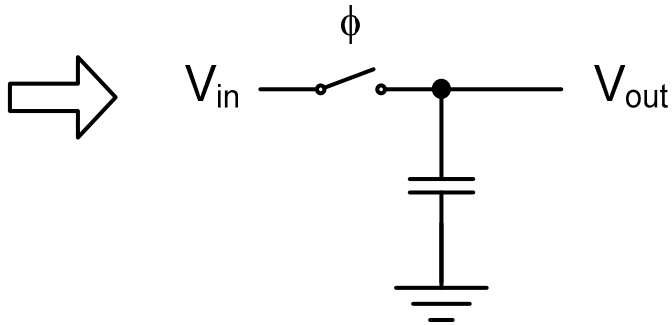




Non-overlapping clock signals

Elementary T/H Circuit





Elementary Track and Hold Circuit

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- Circuit Examples
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  - Charge redistribution stage
  - Delta-sigma modulator

Types of Noise

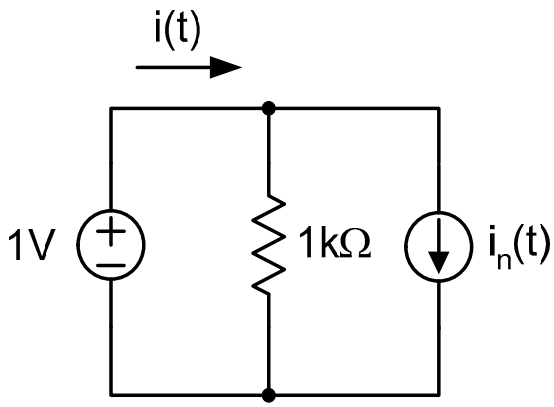
- "Man made noise”
  - Supply coupling
  - Substrate coupling
- "Electronic noise"
  - Technology related
    - Flicker noise caused by lattice defects
  - Fundamental
    - Thermal noise caused by random motion of carriers
    - Focus of this short course

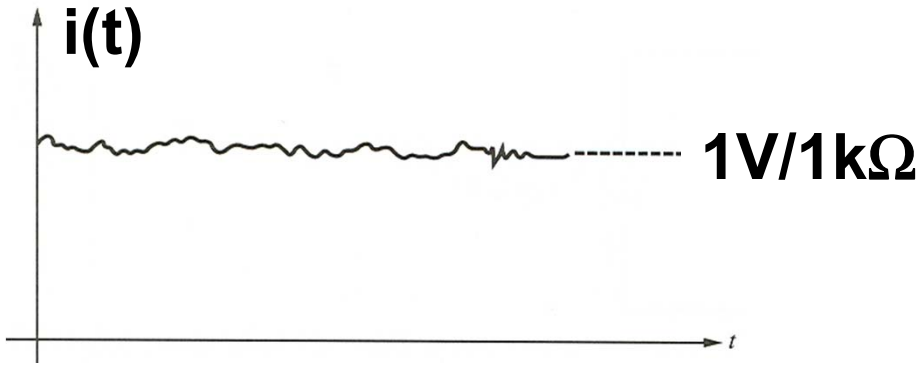
Significance of Thermal Noise

- **The "fidelity" of electronic systems is often determined by their SNR**
  - **Examples: Audio systems, wireless transceivers, sensor interfaces**
- **Electronic noise directly trades with power dissipation and speed**
- **Electronic noise is a major concern in modern technologies with reduced V_{DD}**

$$\mathrm{SNR} \propto \frac{V_{signal}^2}{V_{noise}^2} \propto \frac{(\alpha V_{DD})^2}{V_{noise}^2}$$

Physical Resistor

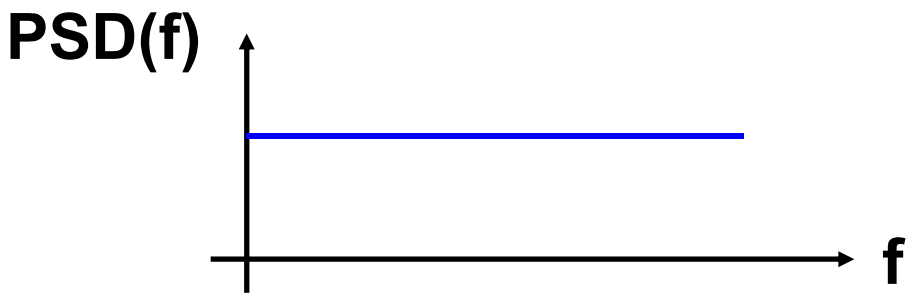




- **"Thermal Noise" or "Johnson Noise"**
  - **J. B. Johnson, "Thermal Agitation of Electricity in Conductors," Phys. Rev., pp. 97-109, July 1928**
- **Can model random current component using a noise current source $i_n(t)$**

Statistical Model

- The power spectral density (PSD) indicates how the power of a signal is spread across frequency
- For thermal noise, the power is spread uniformly up to very high frequencies (about 10% drop at 2 THz)



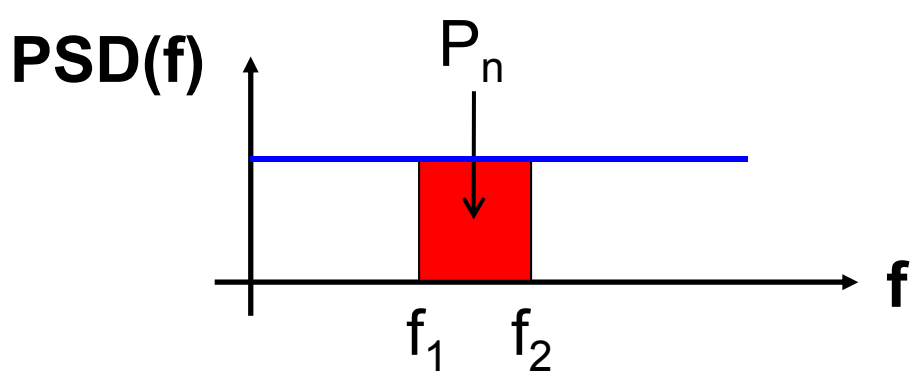
Thermal Noise Power

- **Nyquist showed that**

$$\mathrm{PSD}(f) = 4kT$$

- **The total average noise power of a resistor in a certain frequency band is therefore**

$$P_n = \int_{f_1}^{f_2} 4kT \cdot df = 4kT \cdot (f_2 - f_1) = 4kT \cdot \Delta f$$



Equivalent Noise Generators

- **We can model the noise using an equivalent voltage or current generator**

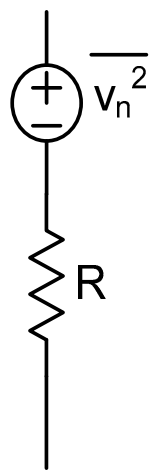
$$\overline{v_n^2} = P_n \cdot R = 4kT \cdot R \cdot \Delta f$$

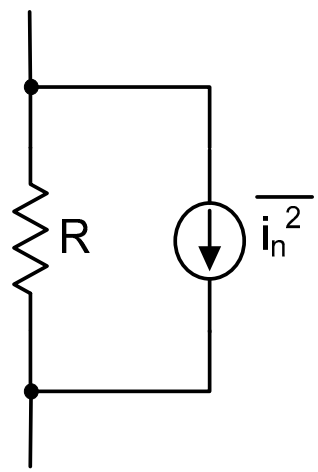
$$\overline{i_n^2} = \frac{P_n}{R} = 4kT \cdot \frac{1}{R} \cdot \Delta f$$

For R = 1kΩ:

$$\frac{\overline{v_n^2}}{\Delta f} = 16 \cdot 10^{-18} \frac{V^2}{Hz}$$

$$\sqrt{\frac{\overline{v_n^2}}{\Delta f}} = \frac{4nV}{\sqrt{Hz}}$$





For R = 1kΩ:

$$\frac{\overline{i_n^2}}{\Delta f} = 16 \cdot 10^{-24} \frac{A^2}{Hz}$$

$$\sqrt{\frac{\overline{i_n^2}}{\Delta f}} = \frac{4pA}{\sqrt{Hz}}$$

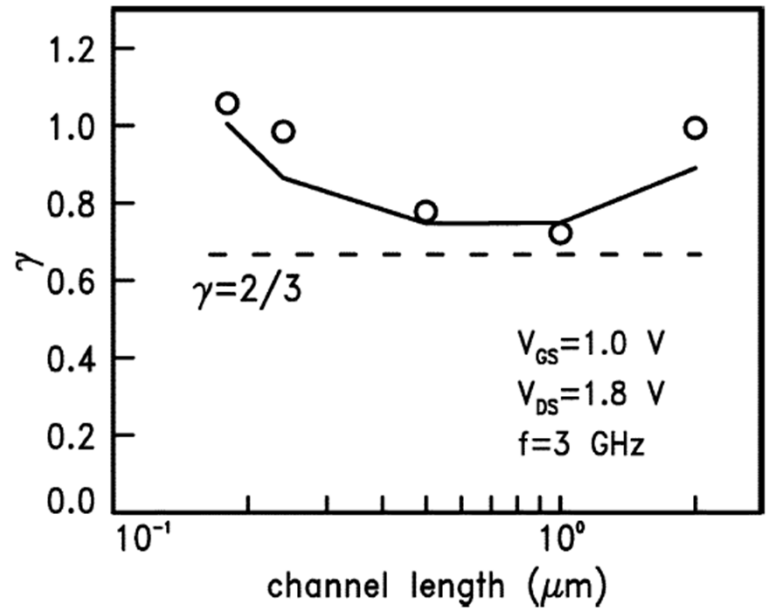
MOSFET Thermal Noise

- **The noise of a MOSFET operating in the triode region is approximately equal to that of a resistor**
- **In the saturation region, the thermal noise can be modeled using a drain current source with power spectral density**

$$\overline{i_d^2} = 4kT \cdot \gamma \cdot g_m \cdot \Delta f$$

- **For an ideal MOSFET, we have $\gamma = 2/3$**

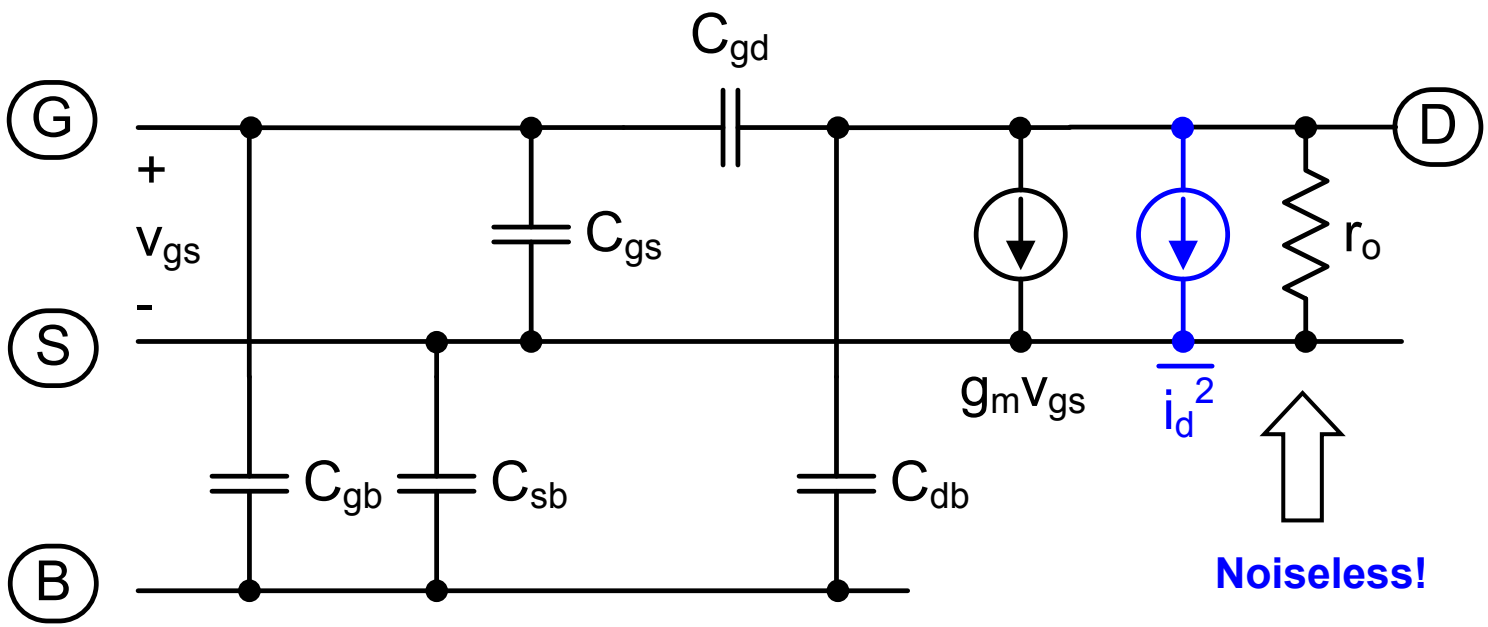
γ Parameter for Short Channels



[Scholten]

- **In moderate inversion, $\gamma \cong 1 \ldots 1.5$**
  - **A. J. Scholten et al., "Noise modeling for RF CMOS circuit simulation," IEEE Trans. Electron Dev., pp. 618-632, Mar. 2003.**
  - **R. P. Jindal, "Compact Noise Models for MOSFETs," IEEE Trans. Electron Devices, pp. 2051-2061, Sep. 2006.**

MOSFET Model in Saturation



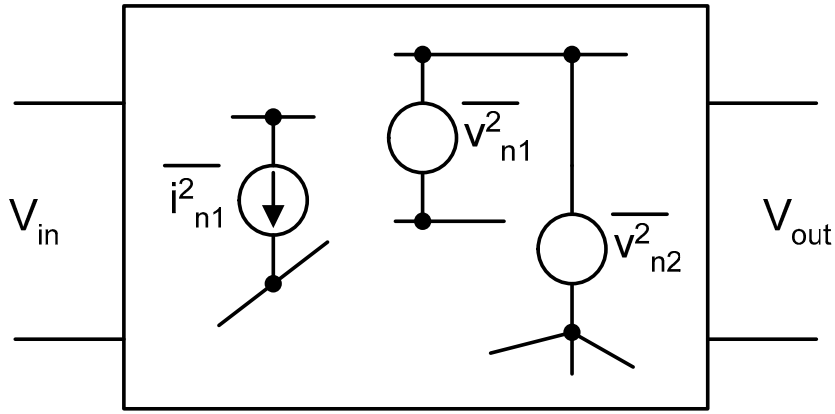
Noiseless!

Merely a modeling resistor that lets us account for finite dI_D/dV_{DS}

$$\frac{\overline{i_d^2}}{\Delta f} = 4kT \cdot \gamma \cdot g_m + \cancel{\frac{K_f}{C_{ox}} \frac{g_m^2}{W \cdot L} \frac{1}{f}}$$

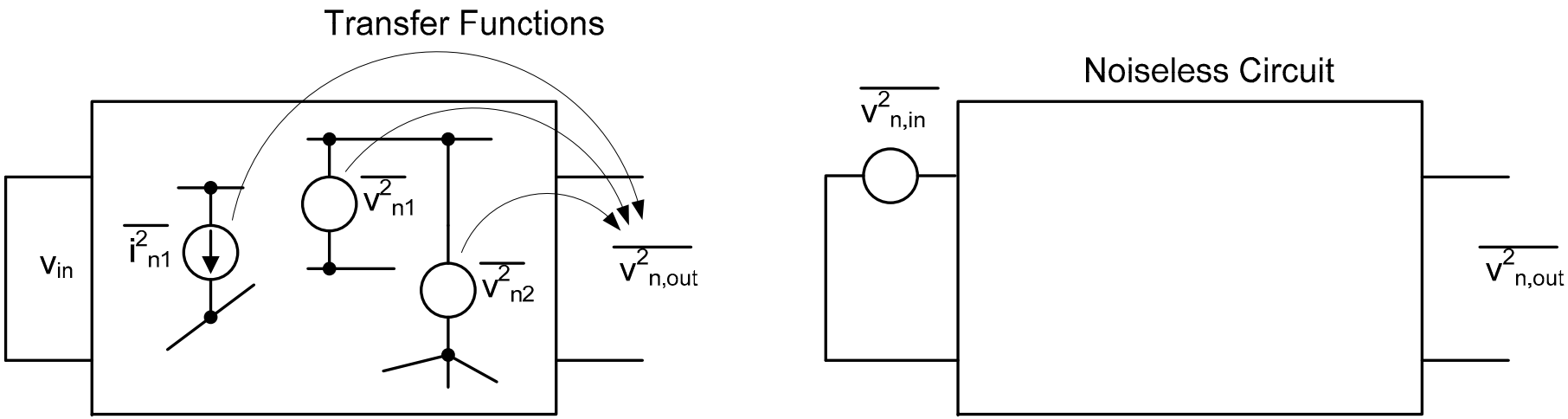
We'll ignore flicker noise in this short course

Noise in Circuits



- **Most circuits have more than one relevant noise source**
- **In order to quantify the net effect of all noise sources, refer the noise sources to a single "interesting" port of the circuit**
  - **Usually the output or input**

Output and Input Referred Noise



$$v_{out} = H \cdot v_{in} \quad \Rightarrow \quad \overline{v^2_{n,in}} = \frac{\overline{v^2_{n,out}}}{|H|^2}$$

- **H can be a continuous time or discrete time transfer function**

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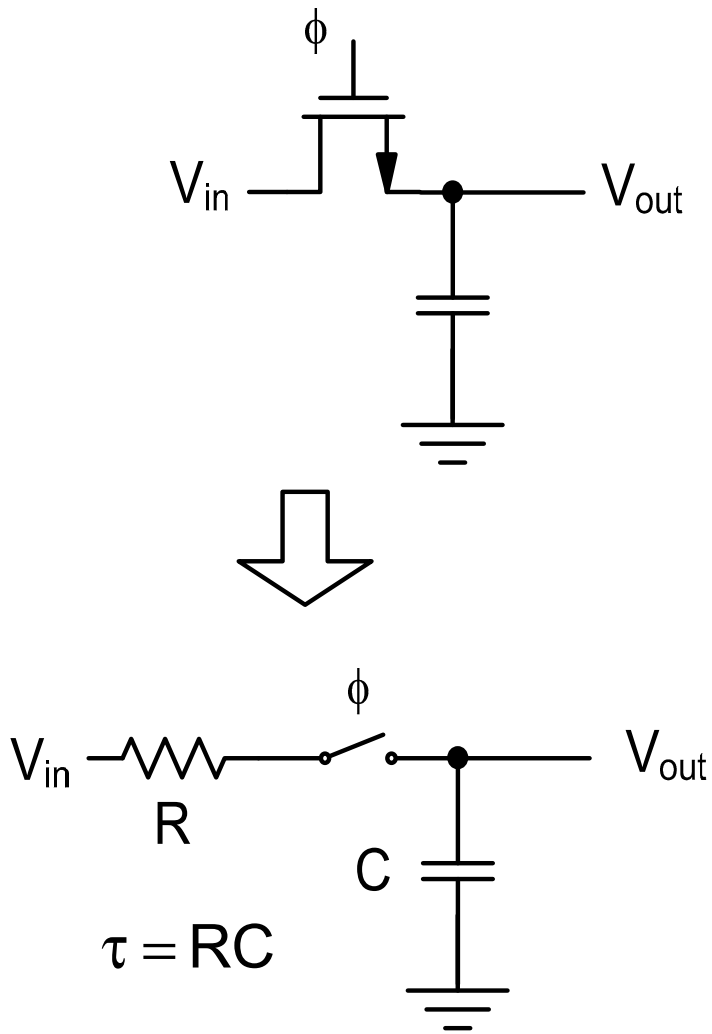
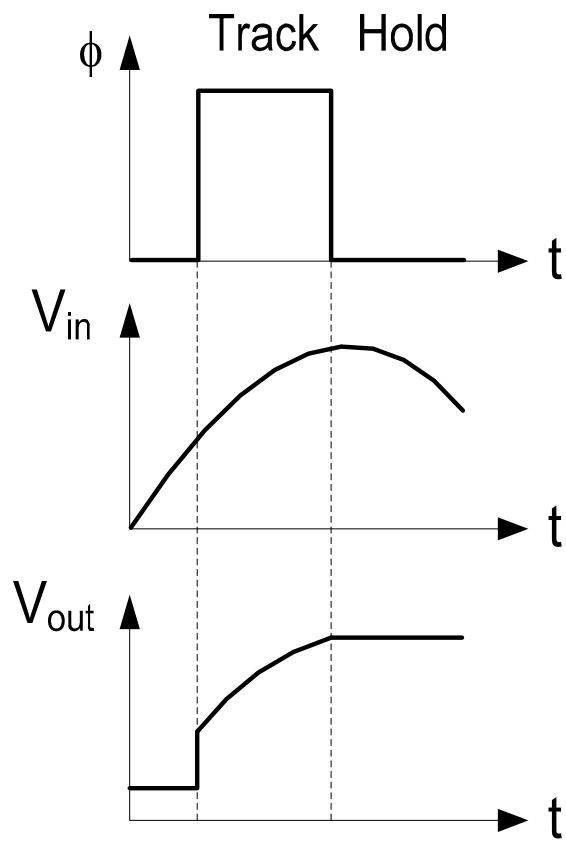
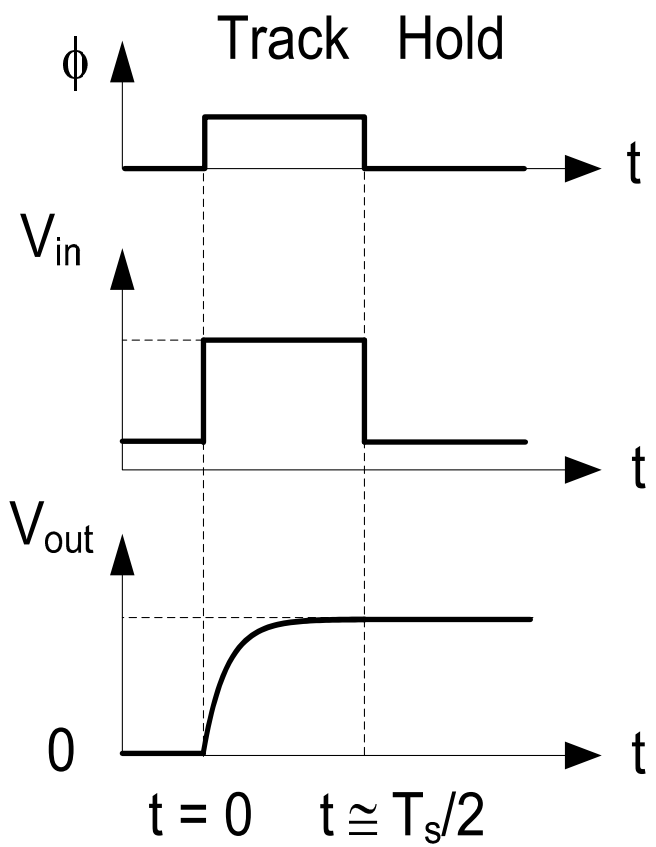
  - **Charge redistribution stage**
  - **Delta-sigma modulator**

Elementary T/H Model





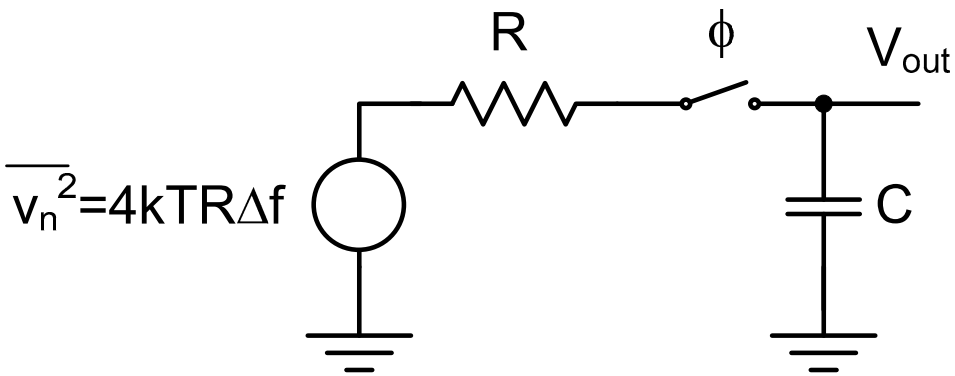
Step Response

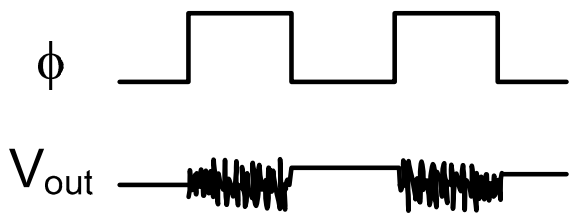


Settling Error at $t = T_s/2$	Required $N = (T_s/2) / \tau$
1%	4.6
0.1%	6.9
0.01%	9.2

- **Circuit is typically designed to settle for N > 5…10 time constants**

T/H Noise Analysis

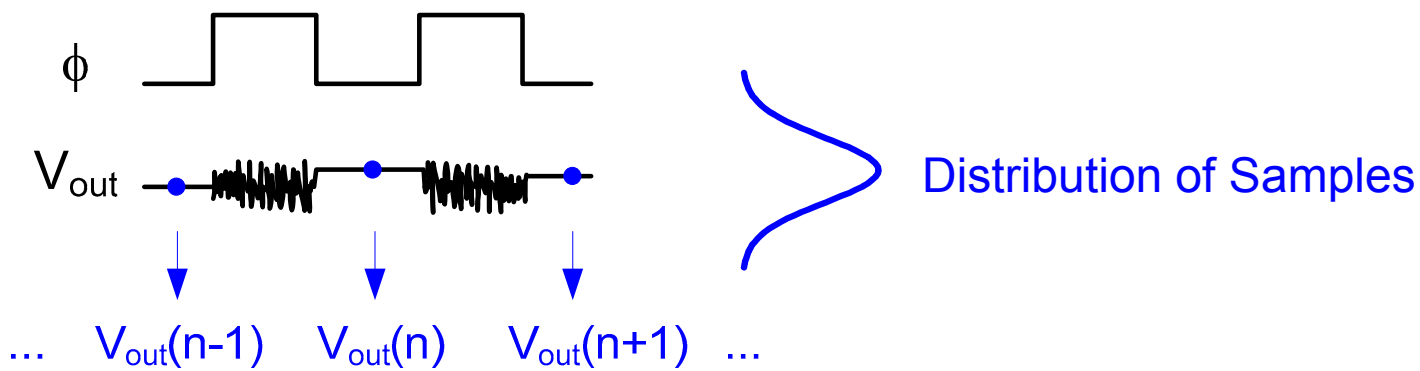




- **Question: What is the noise at the output?**
- **Can't really answer this question without being more specific…**

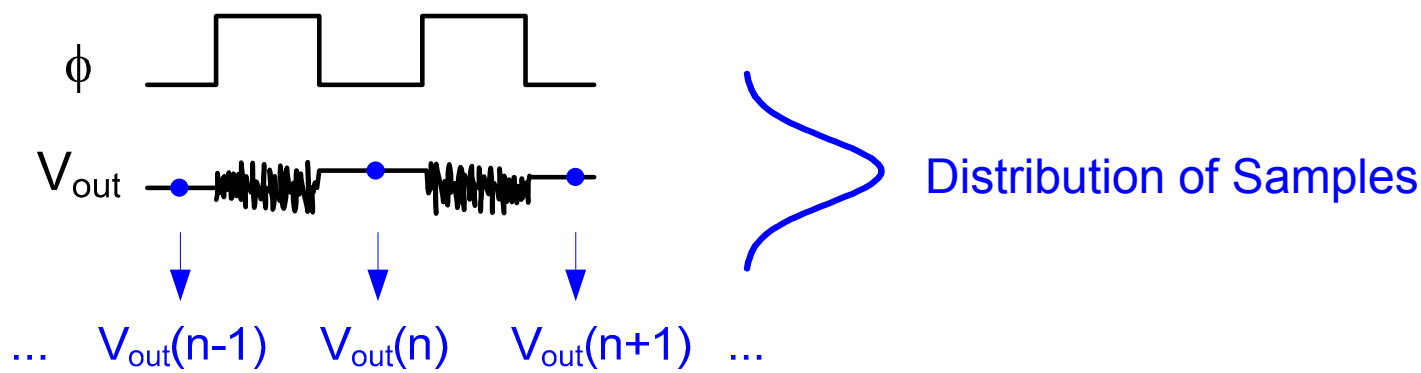
T/H Noise Analysis

- Two possible ways to look at the noise
  - Noise in the continuous time output waveform
  - Discrete time, i.e. “frozen” noise values
- In SC circuits, we think about the signal in terms of discrete time samples, hence we should do the same for noise



T/H Noise Analysis

- **A discrete time noise sequence has two important properties**
  - **The variance of the samples**
  - **The spectrum of the sequence**
    - **Noise samples are uncorrelated → white spectrum**
    - **Samples are correlated → colored spectrum**



T/H Noise Analysis

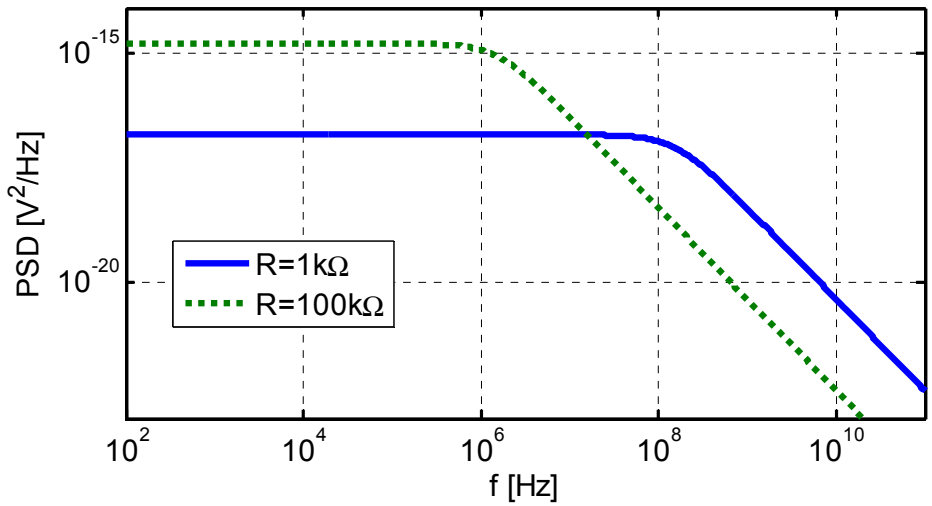
- **The variance of the samples is equal to the noise PSD integrated over all frequencies (Parseval)**

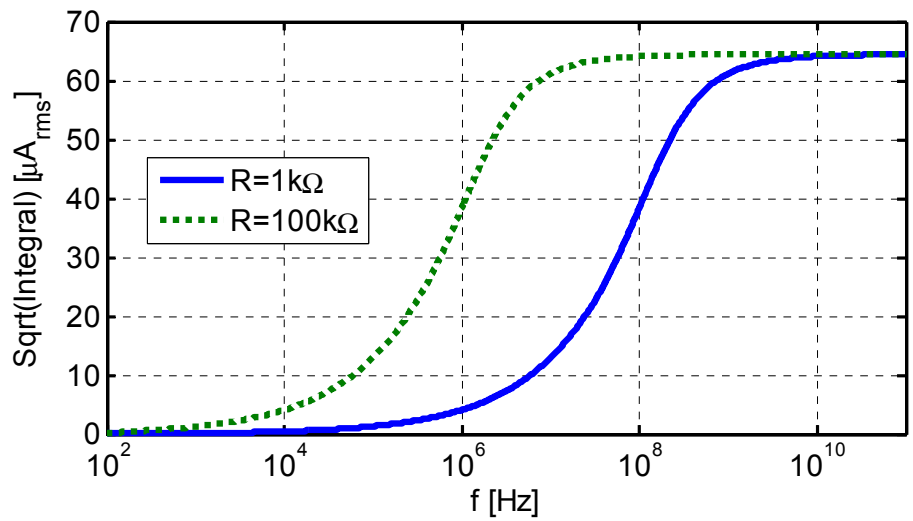
$$\mathrm{var}\left[V_{out}(n)\right] = \overline{v_{out,tot}^2} = \int_0^\infty 4kTR \cdot \left| \frac{1}{1 + j2\pi f \cdot RC} \right|^2 df = 4kTR \cdot \frac{1}{4RC}$$

$$\boxed{\overline{v_{out,tot}^2} = \frac{kT}{C}}$$

Effect of Varying R

- Increasing R increases the noise PSD, but decreases the bandwidth
  - R drops out
- For C=1pF the total integrated noise is ~64μVrms
- Integral converges for f > 10x RC bandwidth





Alternative Derivation

- **The equipartition theorem says that each degree of freedom of a physical system in thermal equilibrium holds an average energy of kT/2**
- **In our system, the degree of freedom is the energy stored on the capacitor**

$$\overline{\frac{1}{2}Cv_{out}^{2}} = \frac{1}{2}kT$$

$$\overline{v_{out}^{2}} = \frac{kT}{C}$$

Does kT/C Noise Matter?

- **Let's look at the SNR of the elementary T/H circuit with a 1V sinusoid applied**

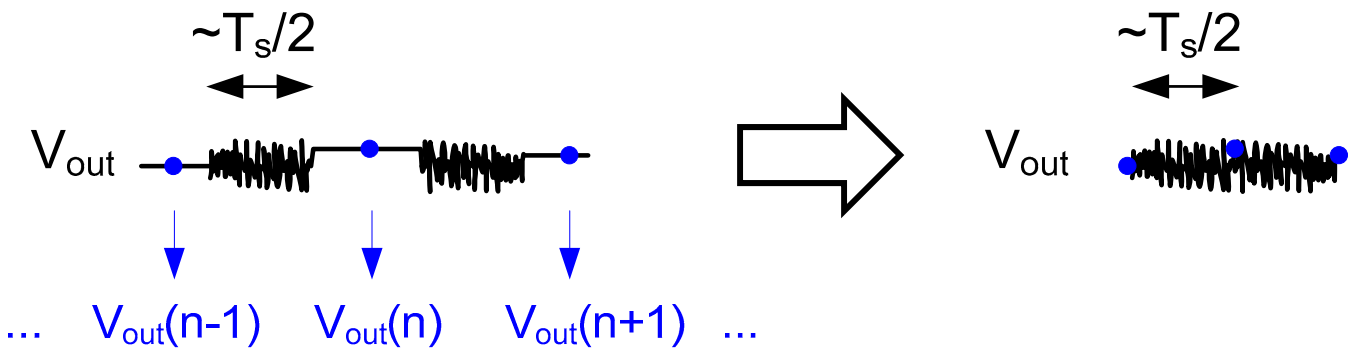
SNR [dB]	C [pF]
20	0.00000083
40	0.000083
60	0.0083
80	0.83
100	83
120	8300
140	830000

Required C is smaller than physically realizable

Designer will be concerned about thermal noise; component sizes often set by SNR

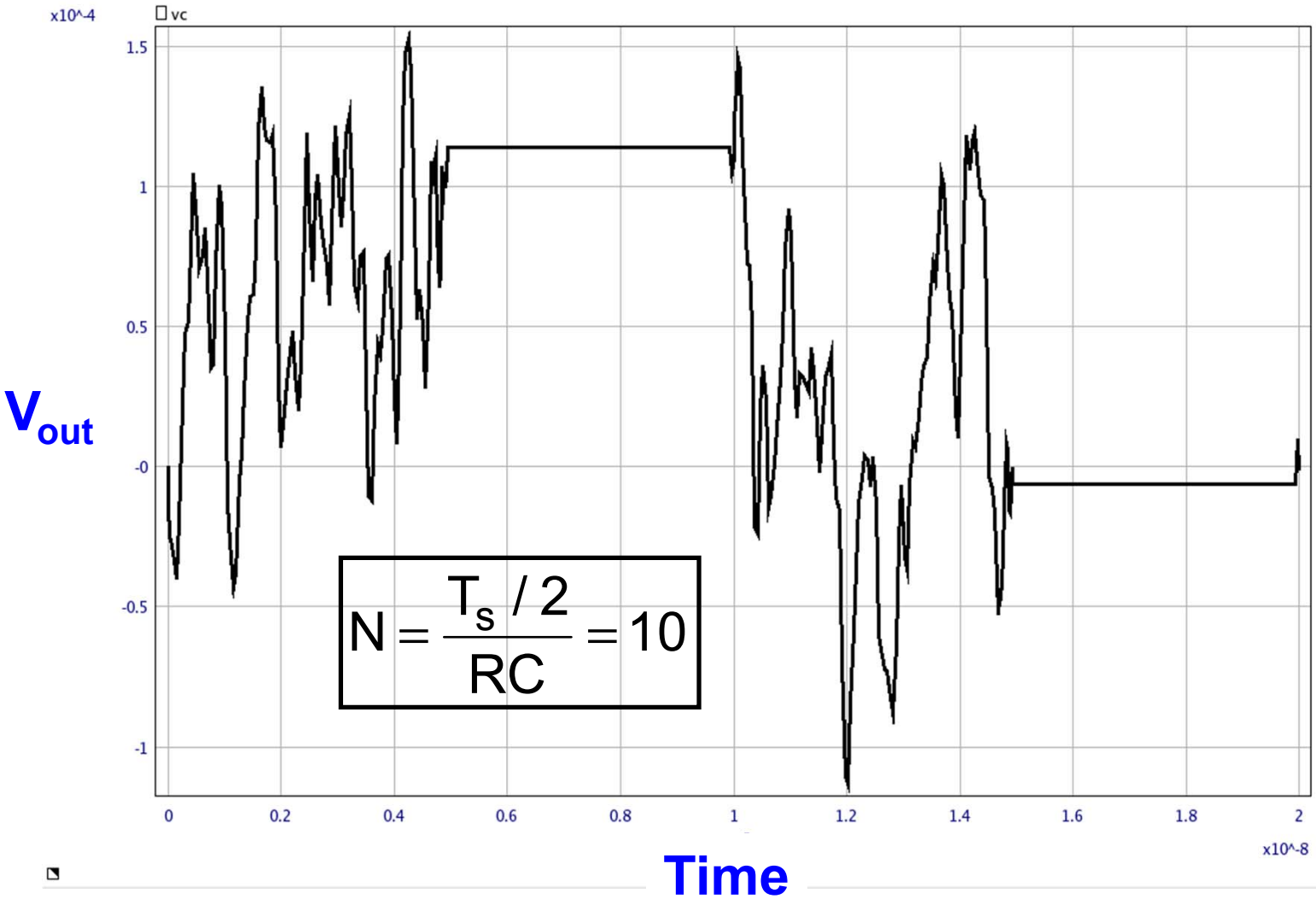
Difficult battle with thermal noise, often resort to oversampling or external components

Spectrum of Noise Samples



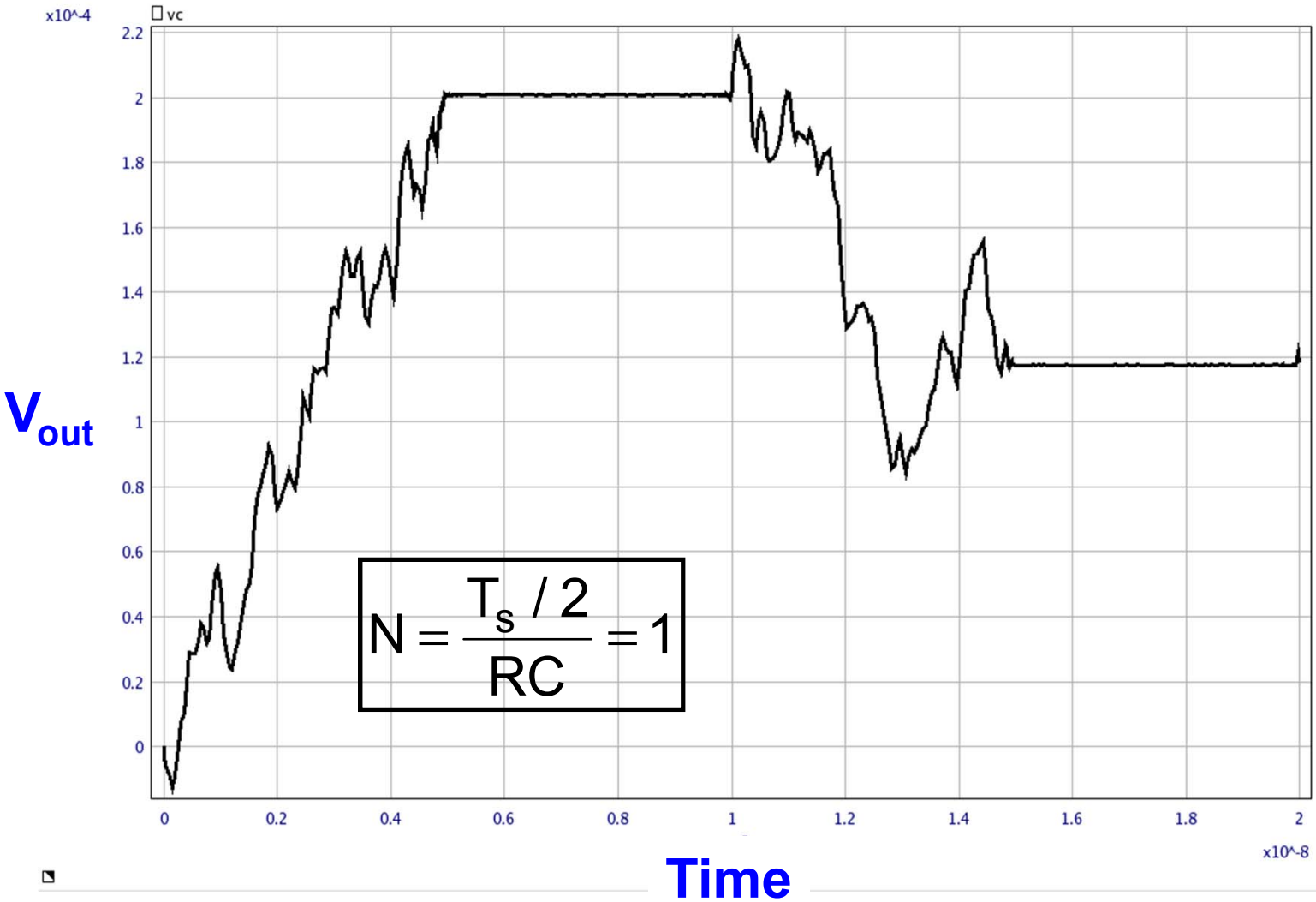
- **The noise samples are instantaneous values (~T_s/2 apart) of the track mode noise process**
- **Intuition**
  - **If the τ = RC is small relative to T_s/2 the samples should show little correlation → white spectrum**
  - **For large RC → significant correlation, colored spectrum**

Transient Noise Simulation



$$N = \frac{T_s / 2}{RC} = 10$$

Transient Noise Simulation



$$N = \frac{T_s / 2}{RC} = 1$$

Calculating the Spectrum

- Spectrum follows from Fourier transform of the noise process' autocorrelation function (Wiener-Khinchin)
- The derivation in the following slides consists of two steps
  - Calculate autocorrelation function of noise at the output of the RC filter
  - Calculate the spectrum by taking the discrete time Fourier transform of the autocorrelation function

Analysis

Autocorrelation of resistor noise (white)

$$R_{xx}(\tilde{\tau}) = \delta(0) \cdot 2kTR$$

Impulse response of RC filter

$$h(t) = \frac{1}{\tau} e^{-t/\tau}$$

Autocorrelation of filtered noise

$$R_{yy}(\tilde{\tau}) = R_{xx}(\tilde{\tau}) * h(\tilde{\tau}) * h(-\tilde{\tau})$$

$$R_{yy}(\tilde{\tau}) = \frac{kT}{C} e^{-|\tilde{\tau}|/\tau}$$

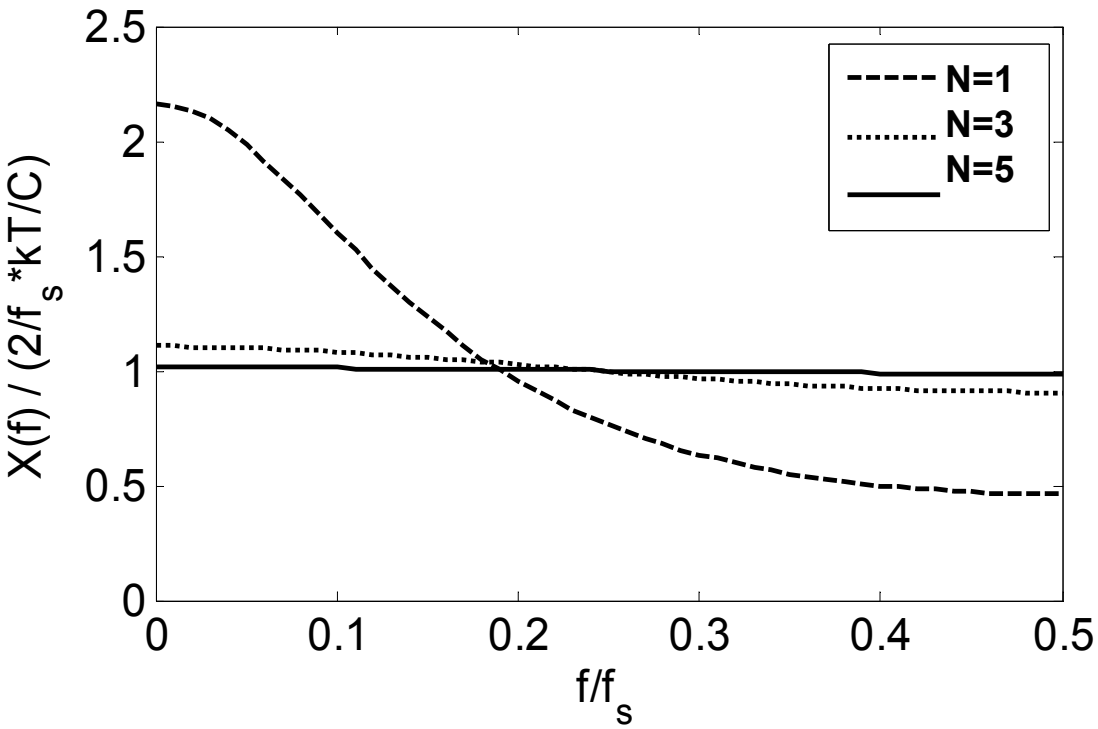
$$R_{yy}(n) = \frac{kT}{C} e^{-\frac{|n \cdot 0.5 T_s|}{\tau}} = \frac{kT}{C} e^{-|n \cdot N|}$$

Covariance of samples separated by n clock cycles

Analysis

$$X(\omega) = \sum_{-\infty}^{\infty} R_{yy}(n) e^{j\omega \cdot nT_s}$$

$$X(f) = \frac{2}{f_s}\frac{kT}{C}\frac{1-e^{-2N}}{1-2e^{-N}\cos\left(2\pi\frac{f}{f_s}\right)+e^{-2N}}$$



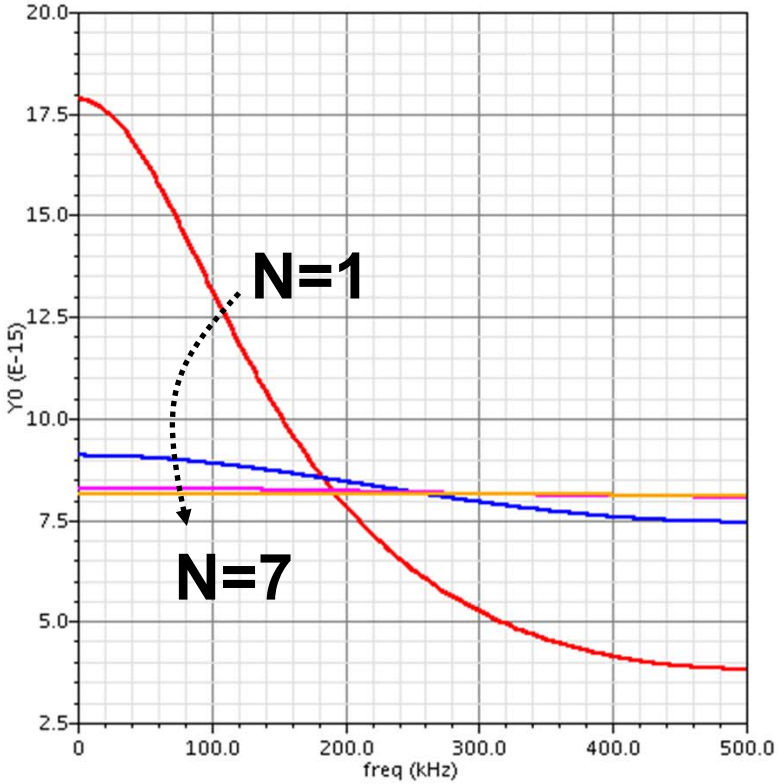
Spectrum is essentially "white" for N > 3

$$\text{PSD} \cong \frac{2}{f_s}\frac{kT}{C}$$

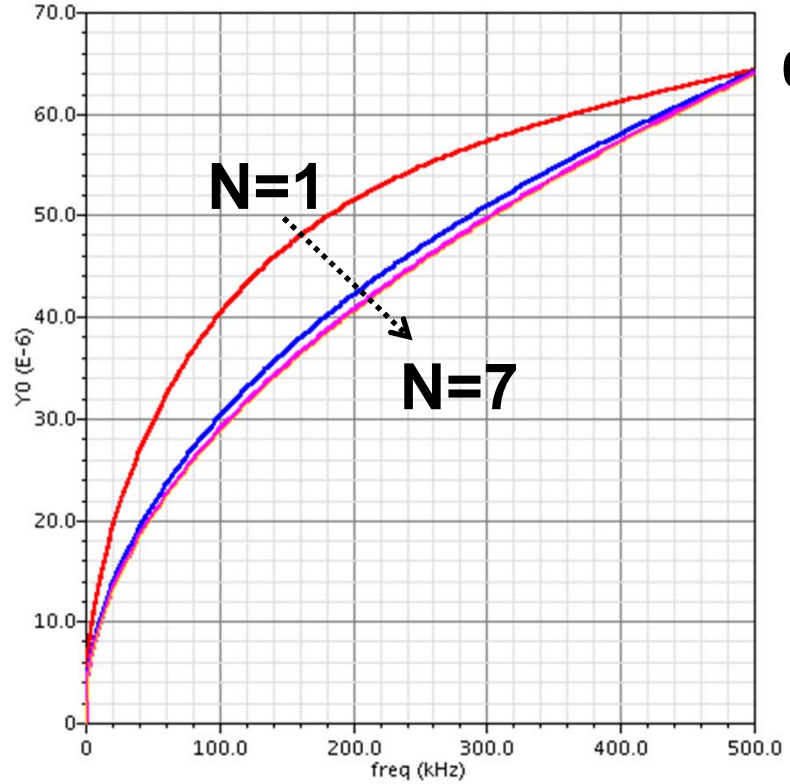
PNOISE Simulation (More Later)

C=1pF

Noise PSD



Noise Integral

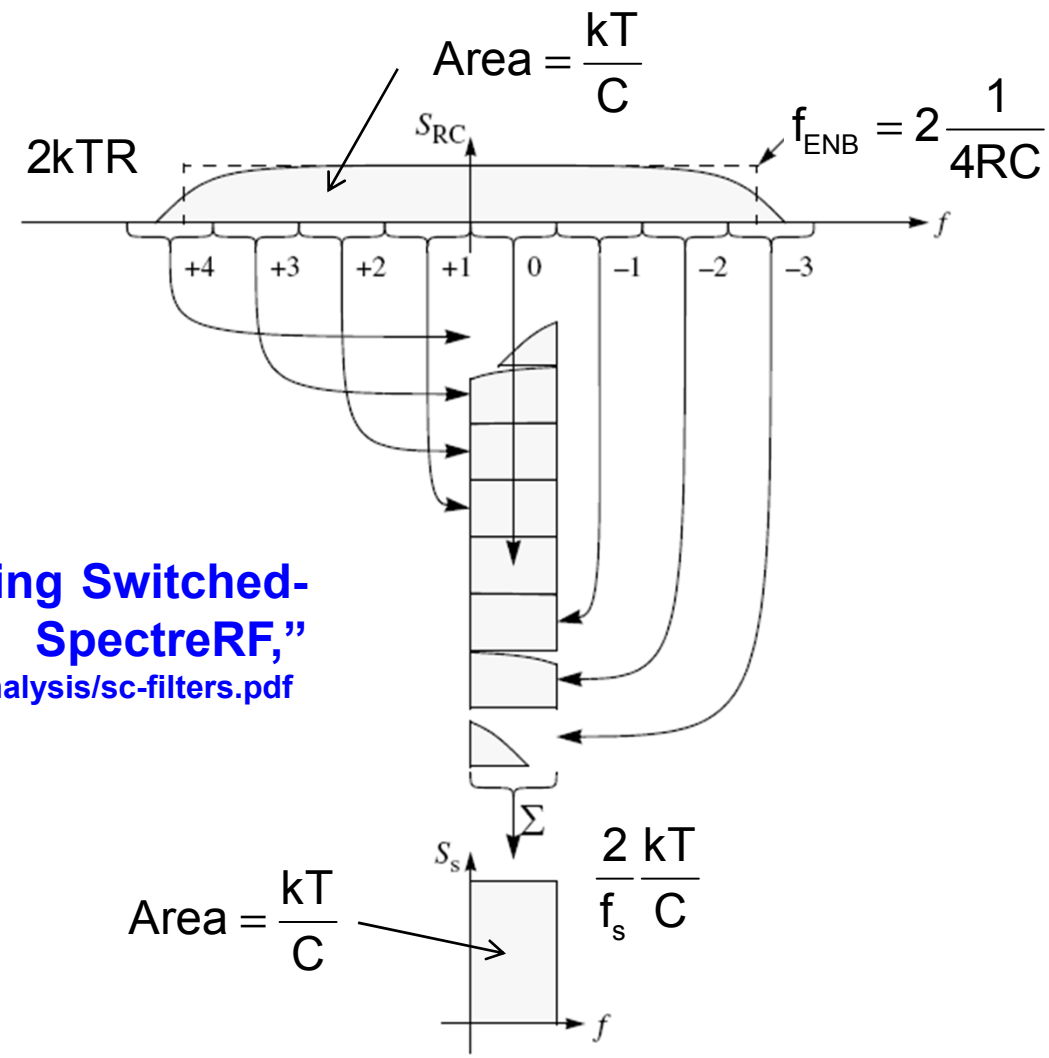


64μVrms

Noise Aliasing Interpretation

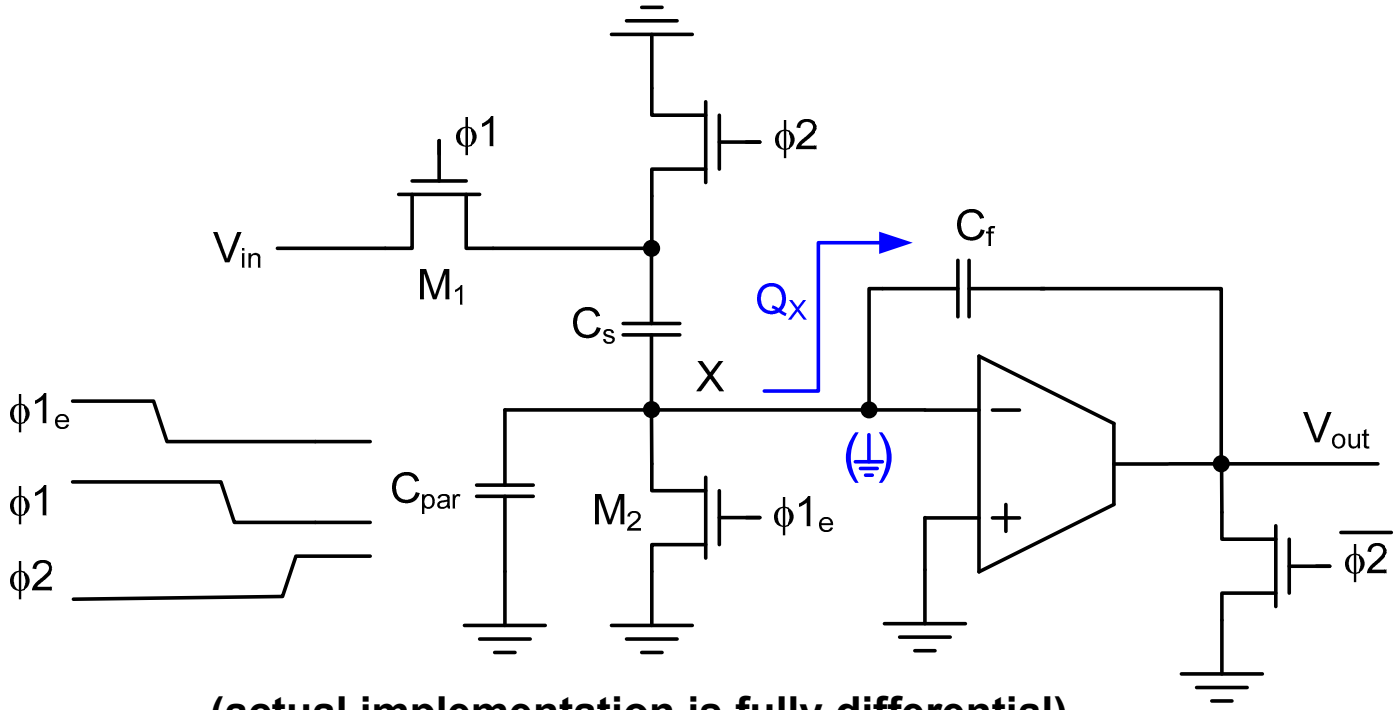
- **Noise PSD of the samples** $$PSD_S = \frac{2}{f_s}\frac{kT}{C}$$
- **Noise PSD of the resistor** $$PSD_R = 4kTR$$
- **Ratio of the PSDs** $$\frac{PSD_S}{PSD_R} = \frac{1}{2f_s}\frac{1}{RC} = \frac{T_s/2}{\tau} = N$$
- **The increase in the noise PSD is due to aliasing of noise across all frequencies into the band from 0…f_s/2**

Noise Aliasing Interpretation



Ken Kundert, "Simulating Switched-Capacitor Filters with SpectreRF,"
http://www.designers-guide.org/Analysis/sc-filters.pdf

Charge-Redistribution T/H



(actual implementation is fully differential)

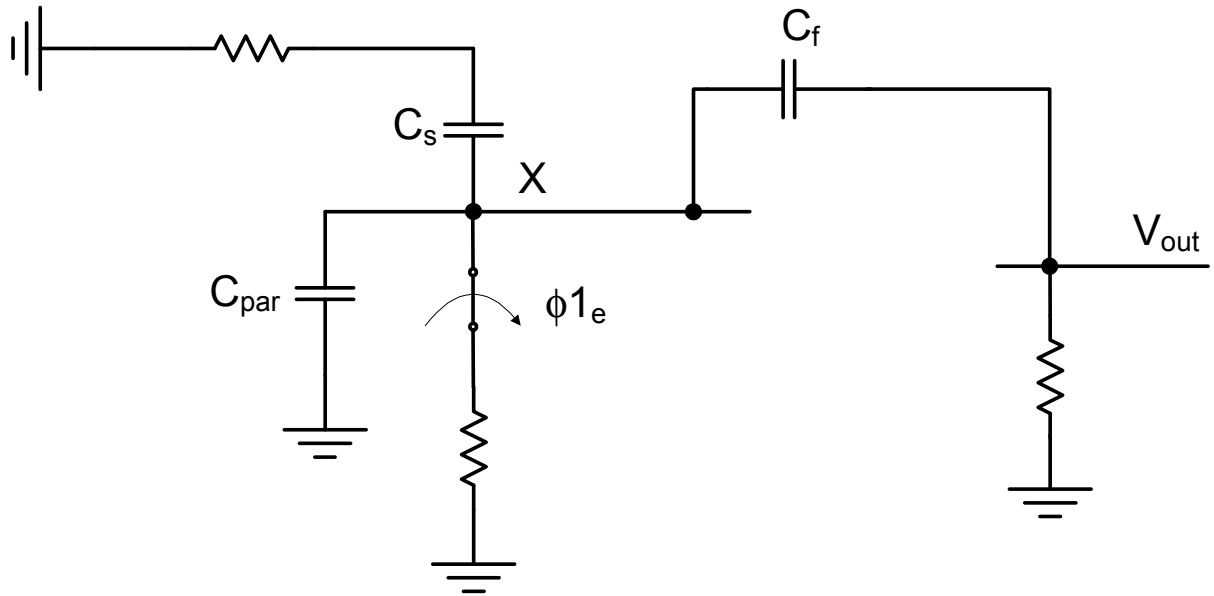
- **When ϕ_{1e} goes low, the signal charge (Q_x) is acquired at node X**
- **During ϕ2, this charge is redistributed onto C_f**

Charge Conservation Analysis

- **During ϕ_1** $$Q_{X1} = -C_s V_{in}$$
- **During ϕ_2** $$Q_{X2} = -C_f V_{out}$$
- **Charge Conservation** $$Q_{X1} = Q_{x2}$$ $$-C_s V_{in} = -C_f V_{out}$$

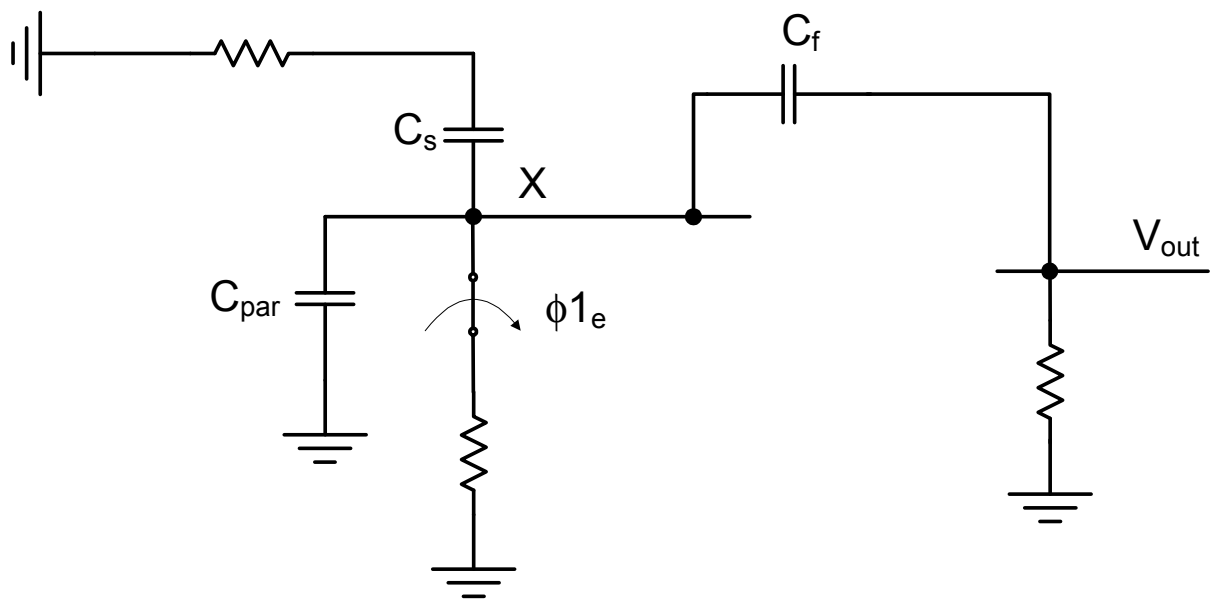
$$\boxed{\therefore V_{out} = \frac{C_s}{C_f} V_{in}}$$

Noise Analysis During $\phi 1$



- **Need to find the total noise <u>charge</u> at node X after the ϕ1e switch has turned off**
- **Tedious to calculate using piece-by-piece integration of all three noise sources**

Equipartition to the Rescue



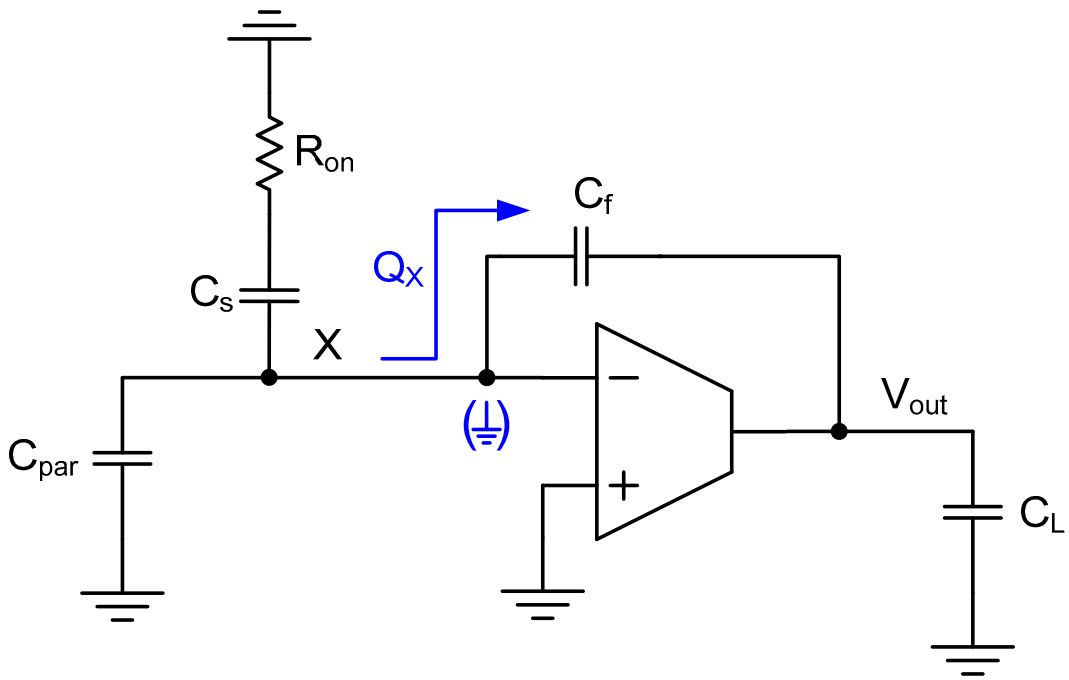
$$\frac{1}{2}\frac{q_x^2}{C_{eff}} = \frac{1}{2}\frac{q_x^2}{C_s + C_f + C_{par}}$$

$$\overline{\frac{1}{2}\frac{q_x^2}{C_s + C_f + C_{par}}} = \frac{1}{2}kT$$

$$\overline{q_x^2} = kT\left(C_s + C_f + C_{par}\right)$$

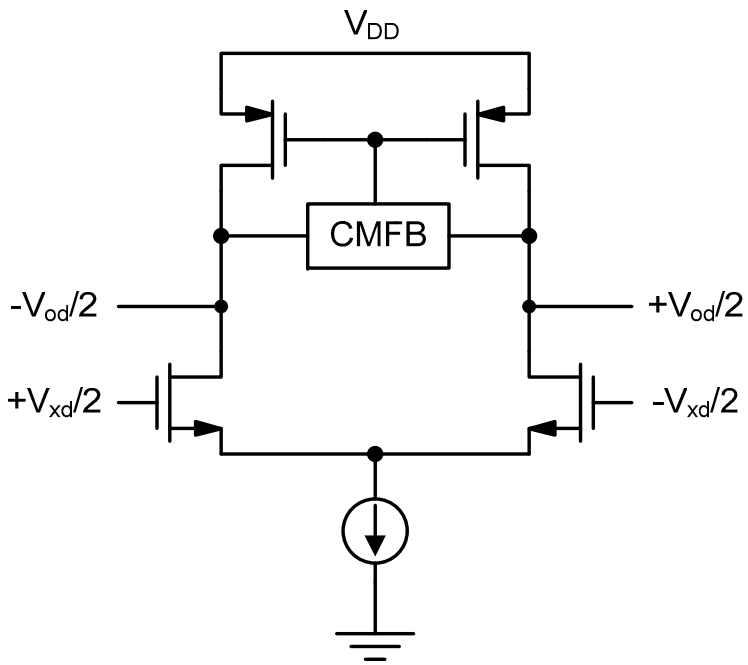
C_{par} can deteriorate noise performance!

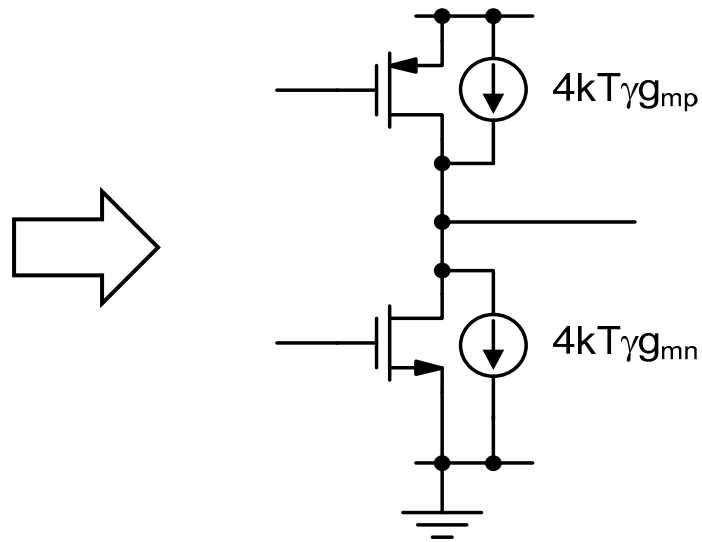
Noise Analysis During $\phi 2$

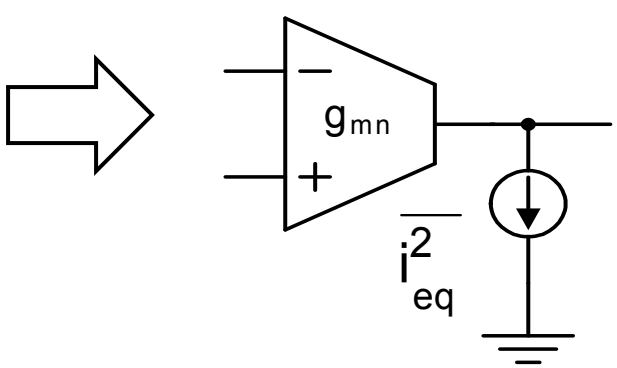


- **Signal and noise charge acquired during $\phi 1$ is redistributed onto C_f**
- **Additional noise from R_{on} and OTA is added**

Single Stage OTA Model



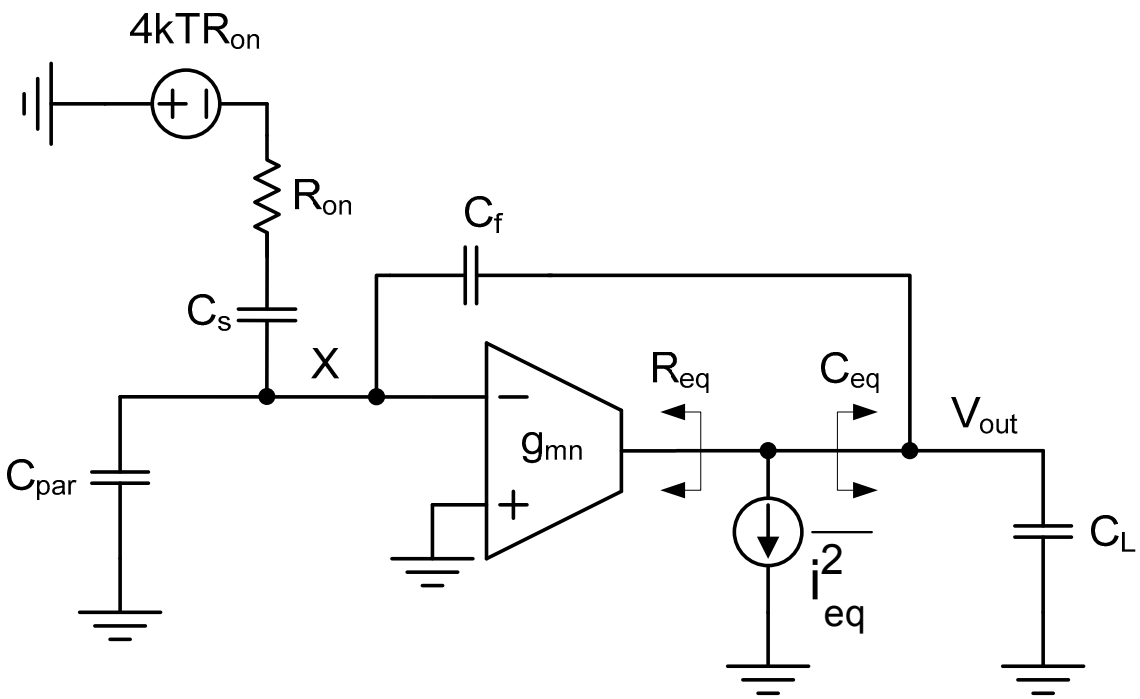




$$\overline{i^2_{eq}} = 4kT\gamma g_{mn} + 4kT\gamma g_{mp}$$

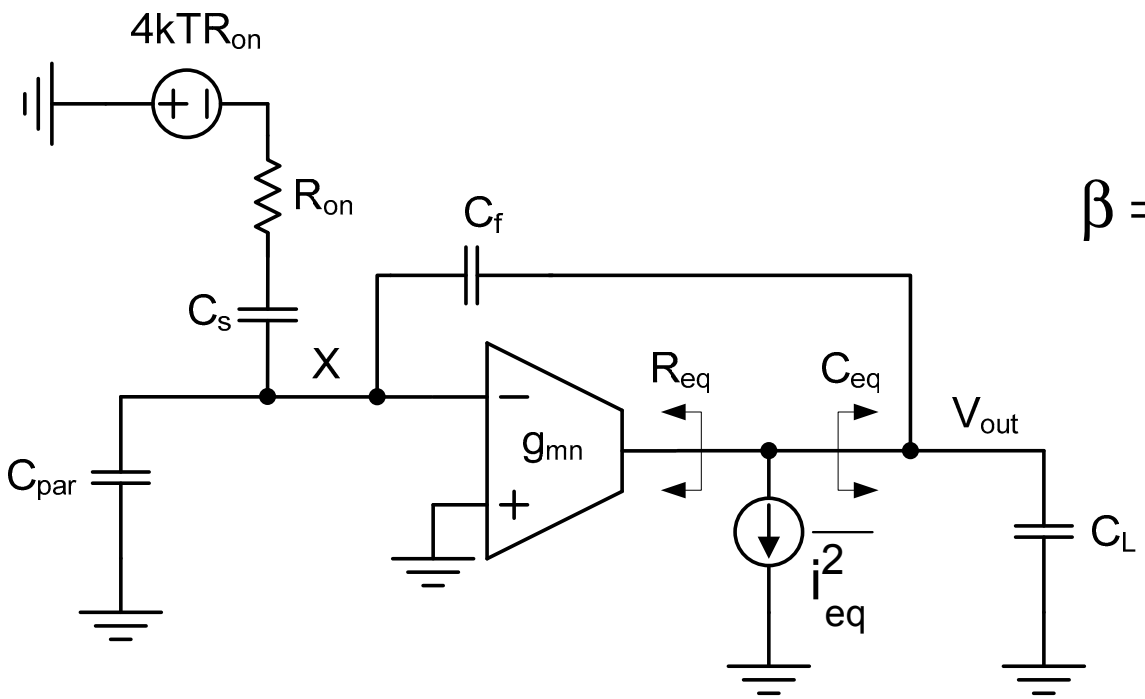
$$\overline{i^2_{eq}} = 4kT\gamma g_{mn}\left(1 + \frac{g_{mp}}{g_{mn}}\right) = 4kT\gamma g_{mn}\alpha$$

Noise Analysis During ϕ2



- **Simplifying assumption: R_{on} has negligible effect on the circuit's frequency response**
  - **Typically true in a practical design; it would be wasteful to let the switch (rather than the OTA) limit the bandwidth**

OTA Time Constant

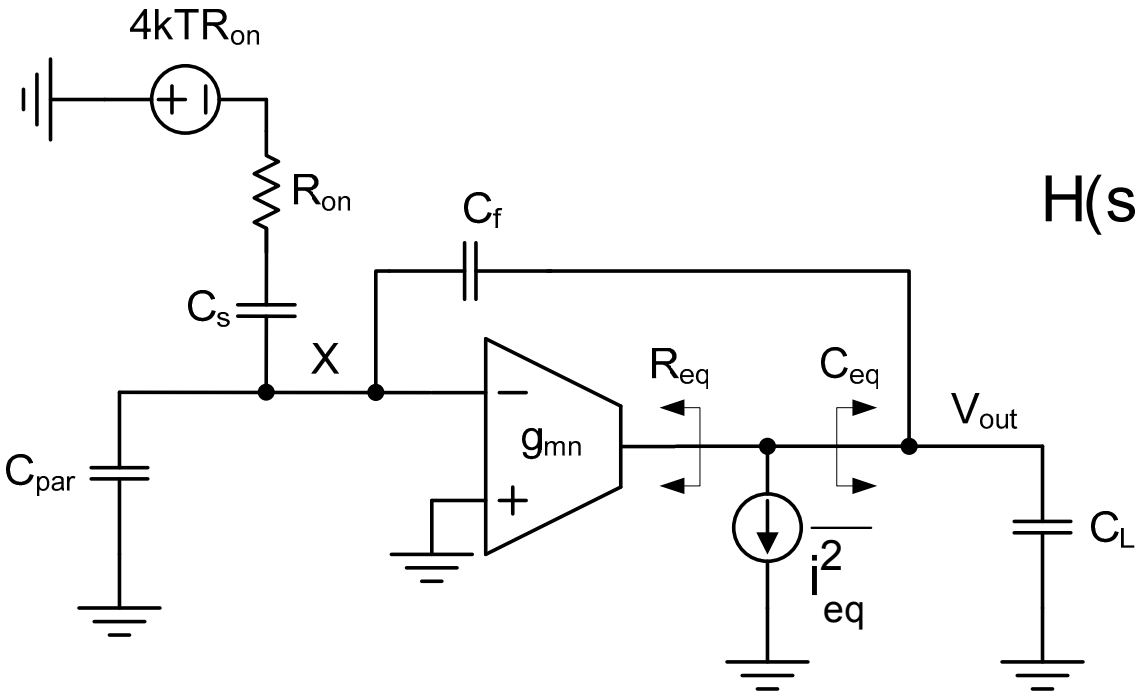


$$\beta = \frac{C_f}{C_f + C_s + C_{par}}$$

Feedback factor

$$R_{eq} = \frac{1}{\beta}\frac{1}{g_{mn}} \qquad C_{eq} = C_L + C_f(1-\beta) \qquad \tau_{OTA} = R_{eq}C_{eq}$$

Output Referred Noise



$$H(s) = \frac{1}{1 + sR_{eq}C_{eq}}$$

$$\frac{\overline{v_{out}^2}}{\Delta f} = \underbrace{4kTR_{on}\left(\frac{C_s}{C_f}\right)^2}_{A} |H(s)|^2 + \underbrace{\overline{i_{eq}^2} \cdot R_{eq}^2}_{B} |H(s)|^2$$

Output Referred Noise

$$\frac{A}{B} = \frac{4kTR_{on}\left(\frac{C_s}{C_f}\right)^2}{\overline{i_{ieq}^2} \cdot R_{eq}^2} = \frac{R_{on}}{\left(\frac{1}{g_{mn}}\right)} \cdot \frac{\beta^2\left(\frac{C_s}{C_f}\right)^2}{\gamma\alpha} << 1$$

$$\therefore \frac{\overline{v_{out}^2}}{\Delta f} \cong \overline{i_{eq}^2} \cdot R_{eq}^2 \left|H(s)\right|^2$$

- **OTA noise typically dominates, assuming $R_{on} << 1/g_{mn}$**

Output Referred Noise

$$\overline{v_{out,2}^2} = \int_0^\infty 4kT\gamma\alpha g_{mn} R_{eq}^2 \cdot \left| \frac{1}{1 + j\omega R_{eq} C_{eq}} \right|^2 df$$

$$= 4kT\gamma\alpha g_{mn} R_{eq}^2 \cdot \frac{1}{4R_{eq}C_{eq}}$$

$$\boxed{\overline{v_{out}^2} = \frac{1}{\beta}\frac{kT}{C_{eq}}\gamma\alpha}$$

- **Noise introduced during $\phi 2$ is $\propto kT/C_{eq}$**
  - **Depending on feedback factor and OTA topology**

Adding Up $\phi 1$ and $\phi 2$ Noises

$$\overline{v_{out,1}^2} = \frac{\overline{q_x^2}}{C_f^2} = \frac{kT\left(C_s + C_f + C_{par}\right)}{C_f^2}$$

$$\overline{v_{out,2}^2} \cong \frac{1}{\beta}\frac{kT}{C_{eq}}\gamma\alpha$$

$$\boxed{\overline{v_{out,tot}^2} = \frac{kT}{C_f}\left(\frac{C_s + C_f + C_{par}}{C_f}\right) + \frac{1}{\beta}\frac{kT}{C_{eq}}\gamma\alpha}$$

$$\boxed{\overline{v_{in,tot}^2} = \frac{kT}{C_s}\left(1 + \frac{C_f + C_{par}}{C_s}\right) + \frac{1}{\beta}\frac{kT}{C_{eq}}\gamma\alpha\left(\frac{C_f}{C_s}\right)^2}$$

Noise/Power Tradeoff

- Reducing the noise by 6 dB means
  - Increase all C by 4x
  - Increase all g_m by 4x to preserve speed
  - Increase I_D by 4x to maintain same g_m/I_D
- Bottom line
  - Improving the dynamic range in a noise limited circuit by 6 dB ("1bit") quadruples power dissipation!

Noise in Differential Circuits

- **In differential circuits, the noise power is doubled (due to two half circuits), and the signal power increases by 4x**

$$DR_{single} \propto \frac{\hat{V}_{out}^2}{\frac{kT}{C}} \qquad DR_{diff} \propto \frac{\left(2\hat{V}_{out}\right)^2}{2\frac{kT}{C}} = 2\frac{\hat{V}_{out}^2}{\frac{kT}{C}}$$

- **3 dB win in dynamic range, but at the expense of twice the power dissipation**
  - **Can get the same DR/power in a single ended circuit by doubling all cap sizes and g_m**

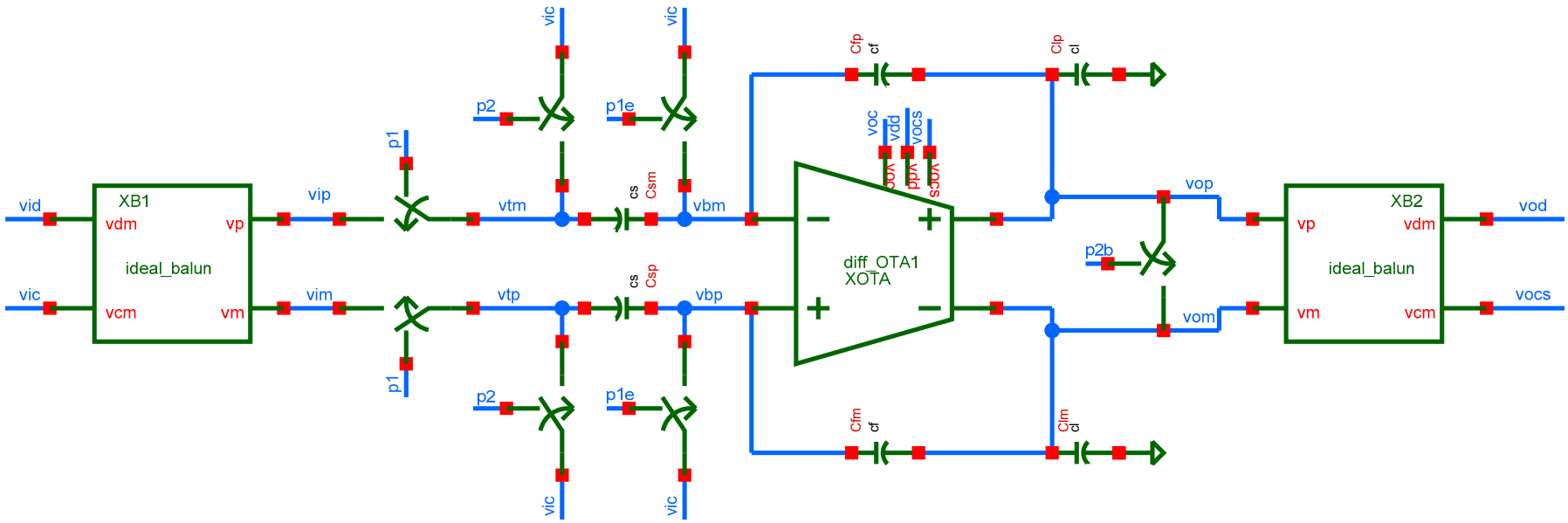
SC Noise Simulation

- There are at least three ways to simulate noise in switched capacitor circuits
- Basic .ac/.noise Spice simulations
  - Simulate noise in each clock phase separately
    - Activate ϕ1 switches, run .noise and integrate noise charge at relevant node over all frequencies and refer to output
    - Activate ϕ2 switches, run .noise and integrate noise over all frequencies at the output
    - Sum integrated noise from the two phases
  - This is analogous to the way we carried out the hand analysis

SC Noise Simulation

- Periodic Steady State Simulation
  - First run PSS analysis to find the periodic operating point
    - Analogous to .op for .ac/noise
  - Next run PNOISE analysis
    - Computes total noise, taking all clock phases, noise aliasing, noise correlations, etc. into account
- Transient Noise
  - Direct simulation of all noise sources using a transient simulation
  - Most physical way of simulating noise

Example T/H Circuit



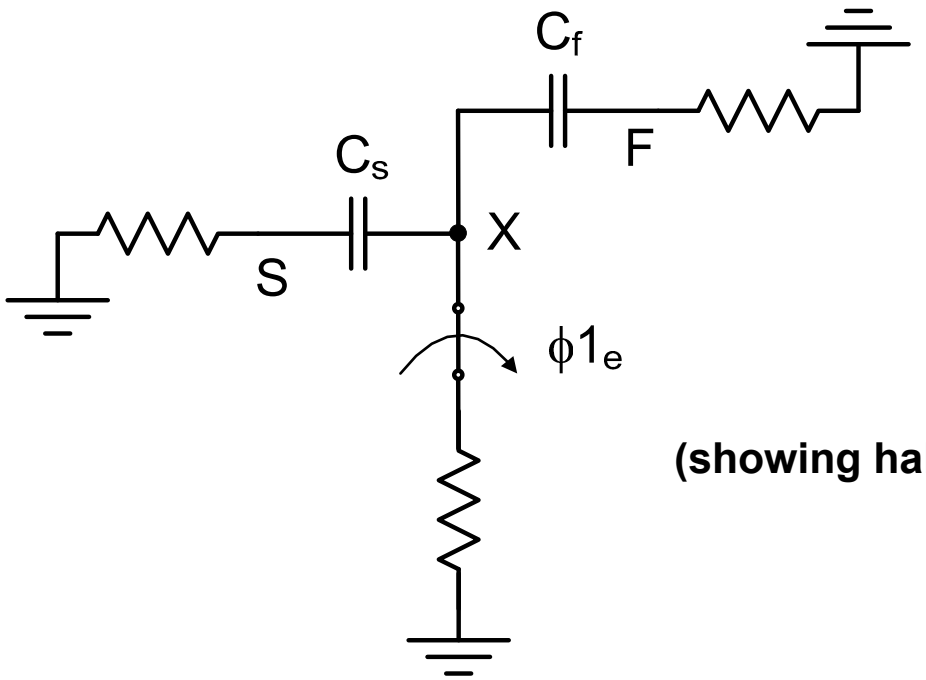
f_s = 100 MHz, α = 2, γ = 1

$C_s = C_f$ = 100 fF, C_L = 500 fF, $C_{par} \cong 0$

- OTA G_m chosen such than $(T_s/2) / \tau_{OTA} = 10$
- Switches sized 5 times faster, i.e. N = 5·10 = 50

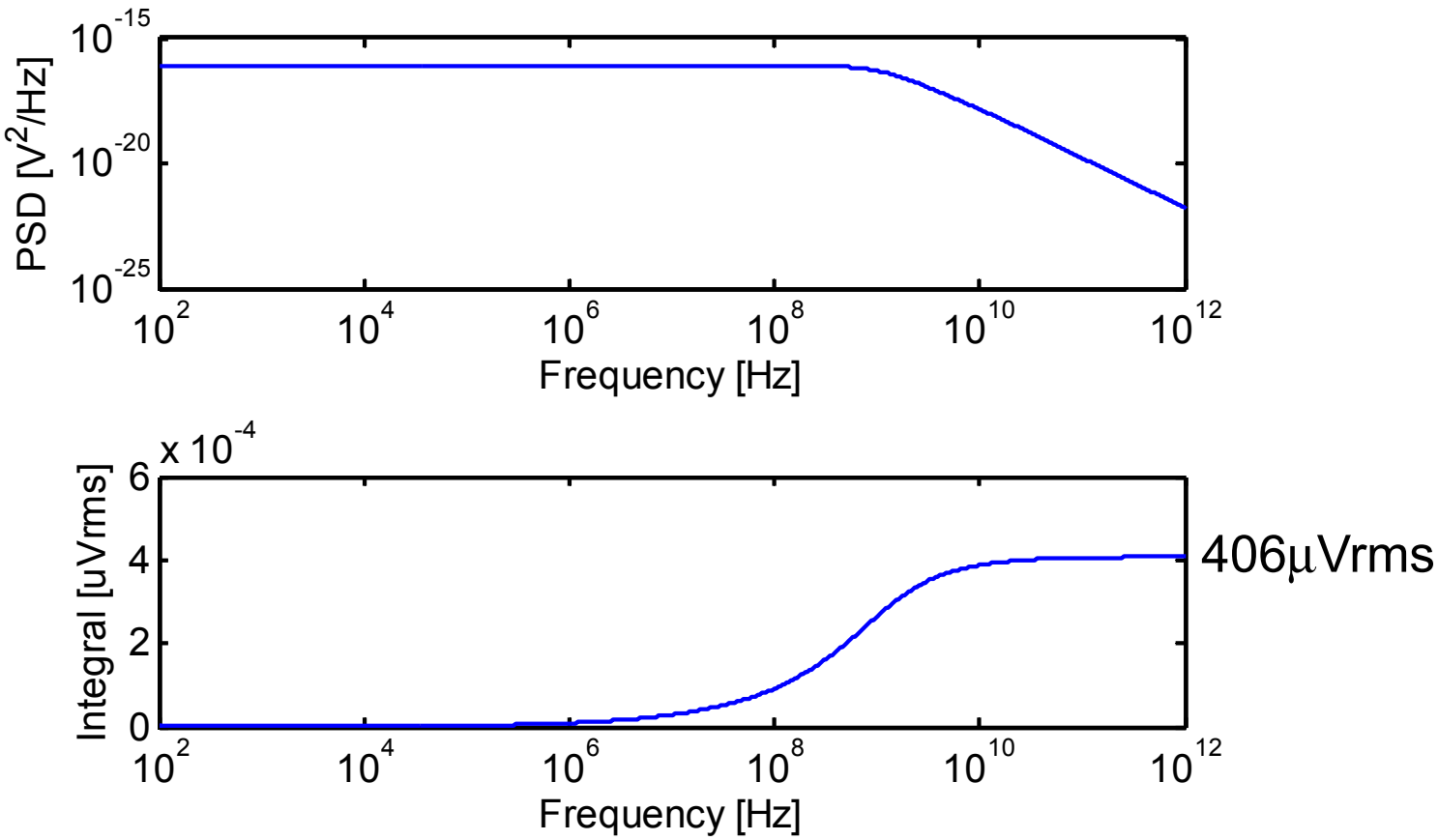
.Noise Simulation (ϕ1)

```
*** Compute noise charge at node X and refer to output via Cf
 en vno 0  vcvs vol =( cs*v(x,s) + cf*v(x,f) )/cf
.ac dec 100 100 1000Gig
.noise v(vno) vdummy
```

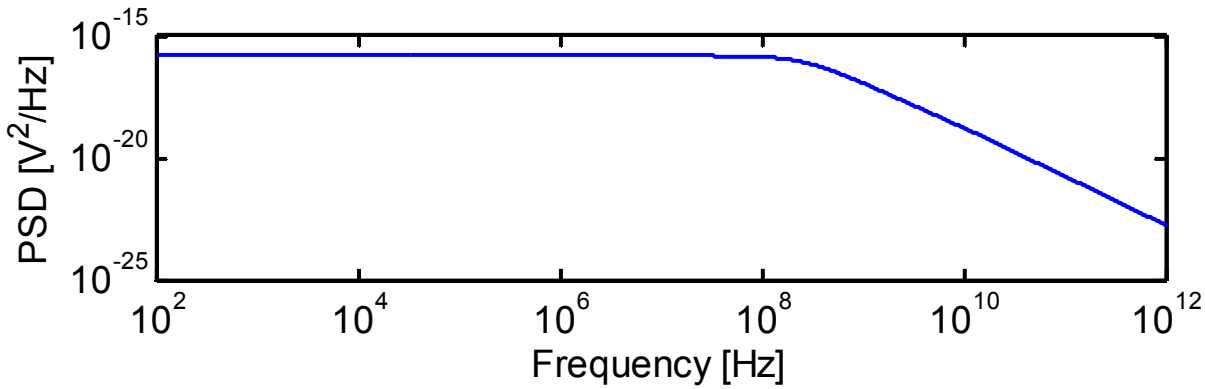


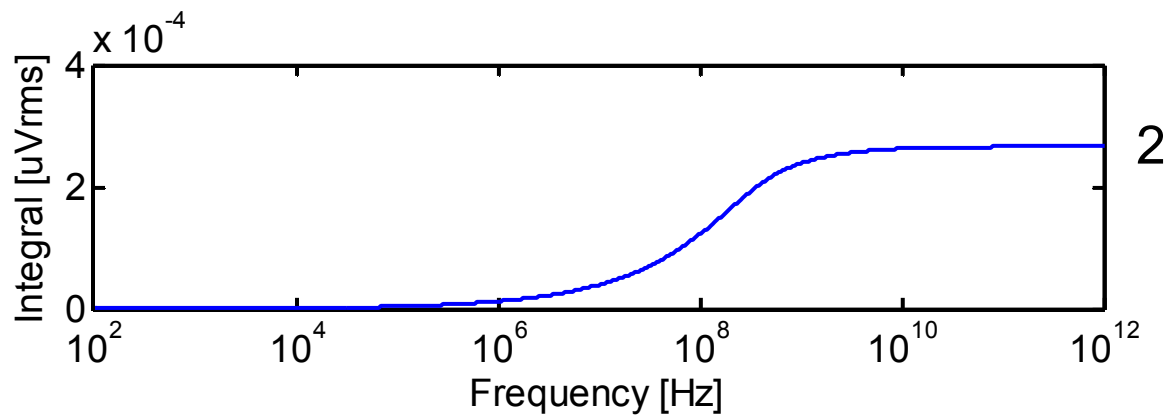
(showing half circuit for simplicity)

.Noise Simulation (ϕ1)



.Noise Simulation (ϕ2)

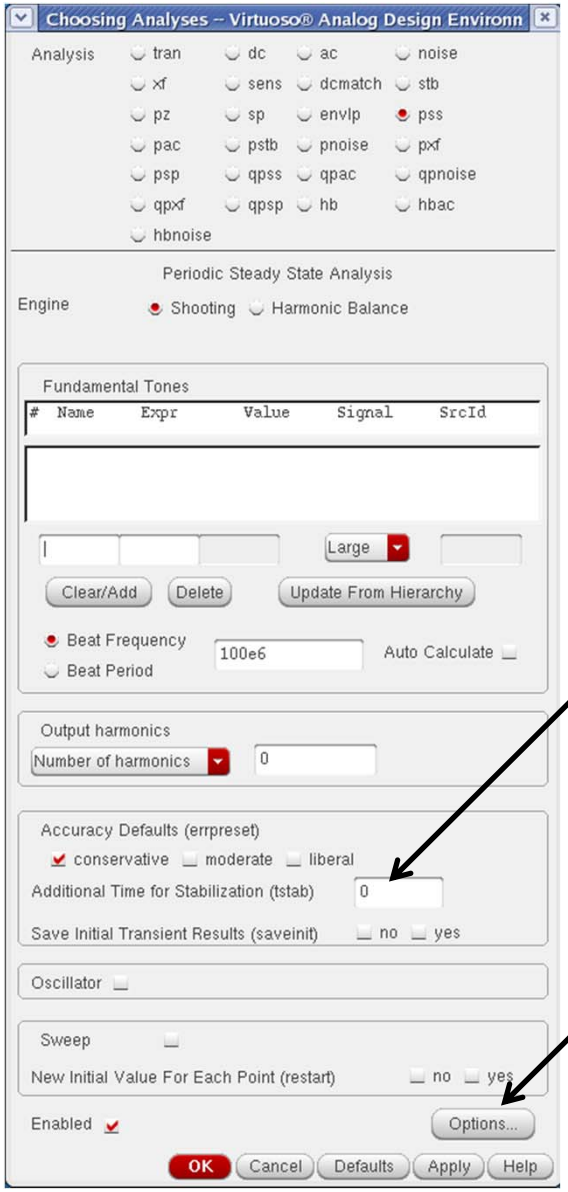




266μVrms

$$\sqrt{\overline{v_{out,tot}^2}} = \sqrt{(406\mu Vrms)^2 + (266\mu Vrms)^2} = 485\mu Vrms$$

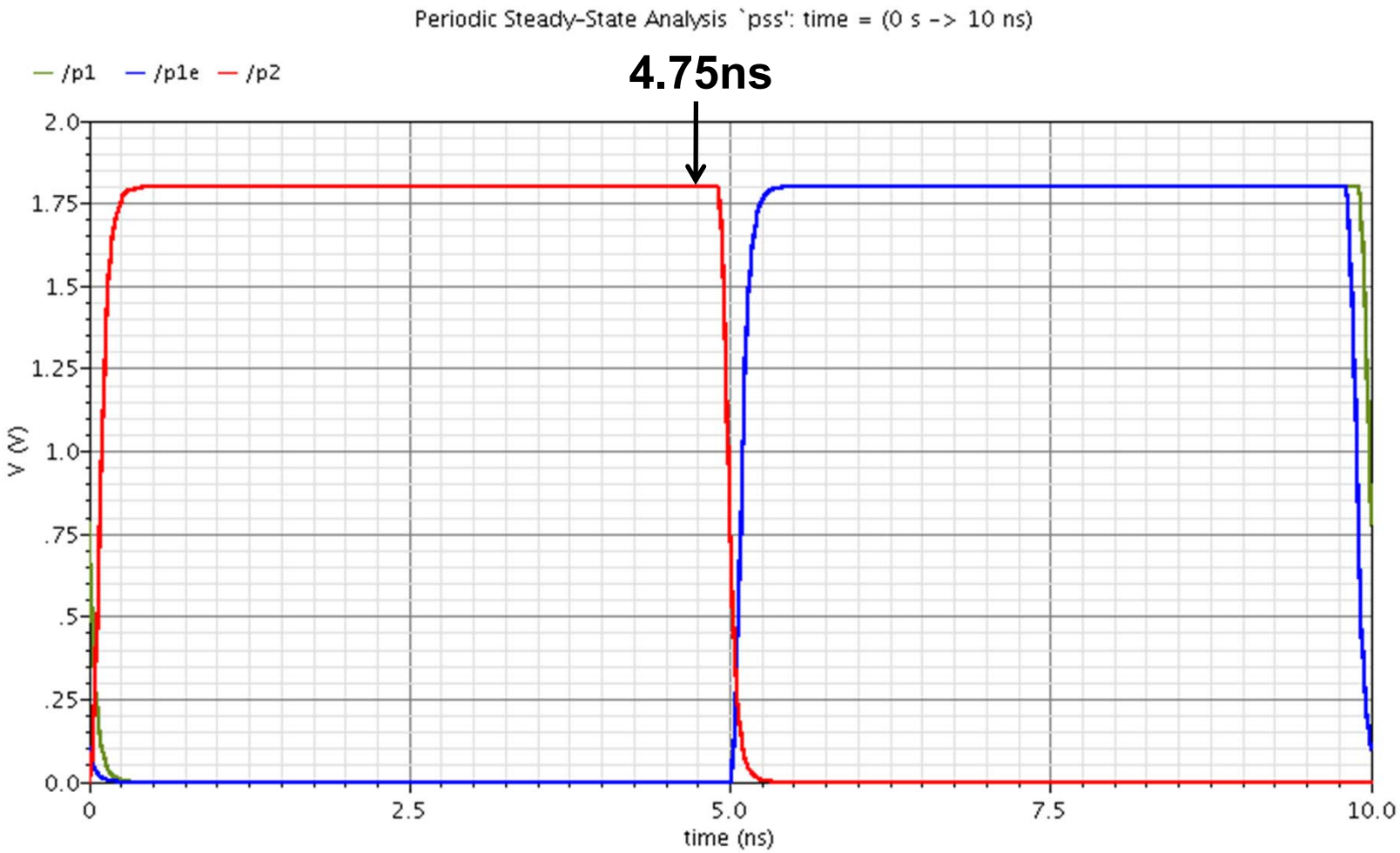
PSS Simulation Setup



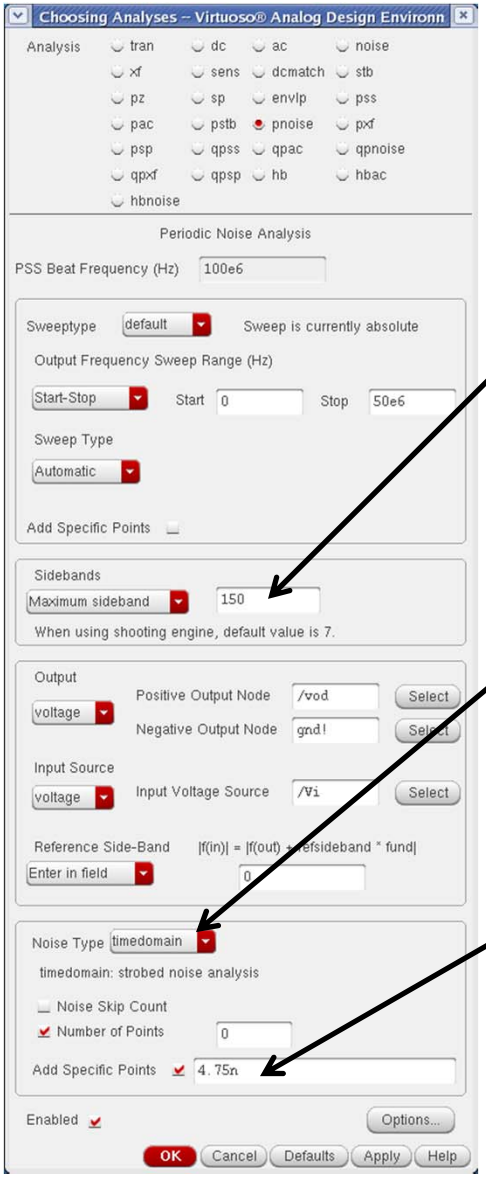
Set "tstab" if your circuit needs time to reach steady state (e.g. clock bootstrap circuits)

Under "options" set "maxacfreq" to the highest frequency from which you expect noise to fold down

PSS Waveforms (Clocks)



PNOISE Simulation Setup



Numsidebands ≅ f_{max}/f_s, where f_{max} is the maximum frequency from which you expect significant noise folding

"timedomain" means simulator computes spectrum of discrete time noise samples at the specified sampling instant

Sampling instant (4.75ns in this example)

How to Chose Parameters

- **Maxacfreq must be set commensurate with the speed of the switches**
  - **Common pitfall: Use nice 1mΩ switches → must consider noise from "DC to daylight"**
- **In our example**

$$\text{Maxacfreq} \cong 10 \cdot \frac{1}{2\pi R_{on} C} = \frac{10}{\pi} \cdot N \cdot f_s$$

$$\text{Maxacfreq} \cong 3 \cdot 50 \cdot 100\text{MHz} = 15\text{GHz}$$

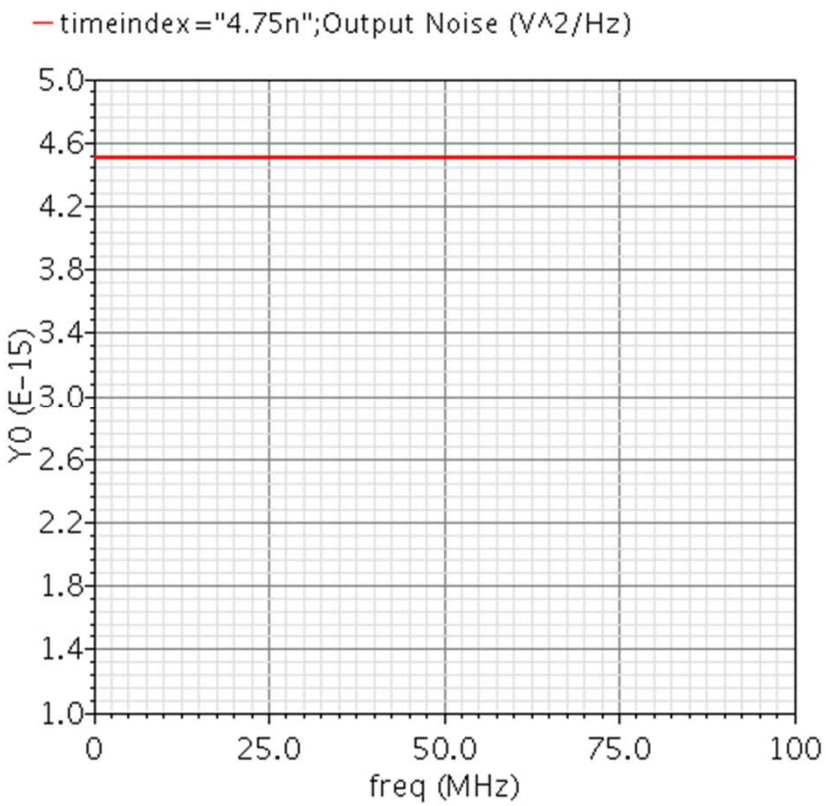
How to Chose Parameters

$$\text{Numsidebands} \cong \frac{\text{Maxacfreq}}{f_s} = \frac{15\text{GHz}}{100\text{MHz}} = 150$$

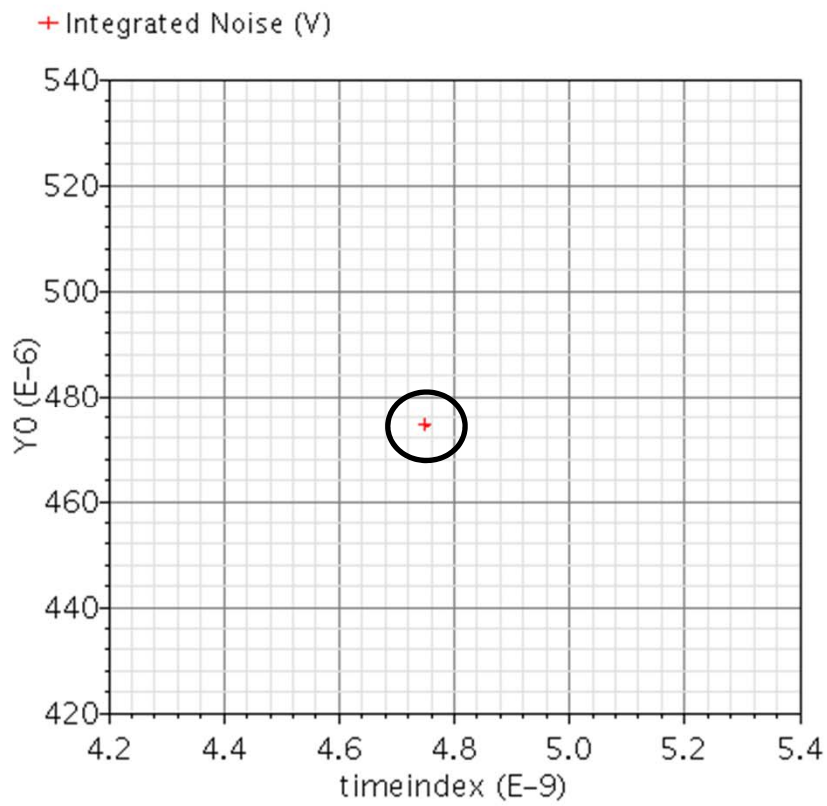
- **In traditional PSS/PNOISE simulators (such as SpectreRF), simulation time increases rapidly for large values of Numsidebands**
- **Berkeley Design Automation (BDA) Analog FastSPICE (AFS) automatically includes an infinite number of sidebands at significantly reduced simulation times**

PNOISE Result (SpectreRF)

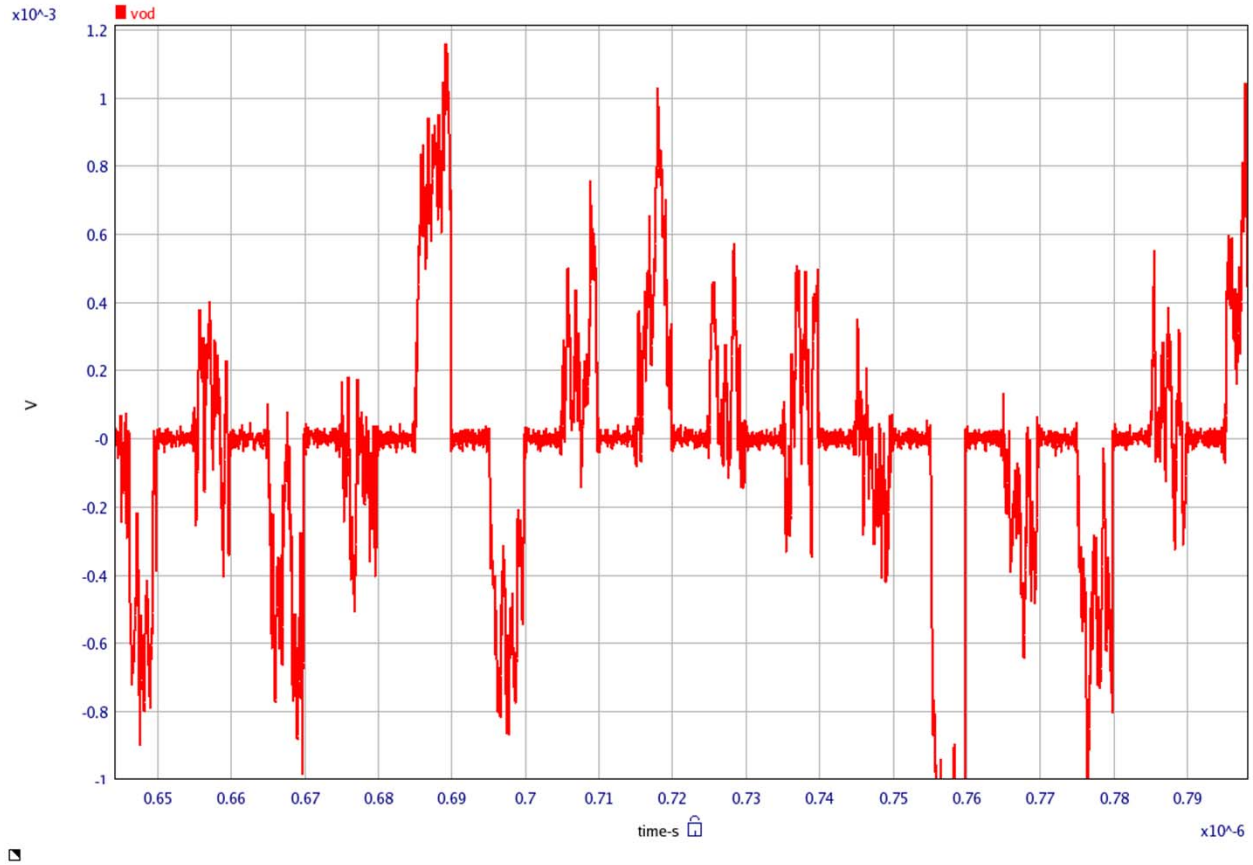
Sampled Noise PSD



Integrated Noise



Transient Noise Using BDA AFS



- **Simulated 1000 samples**
- **Only one critical setting: noisefmax = 15 GHz**

Comparison

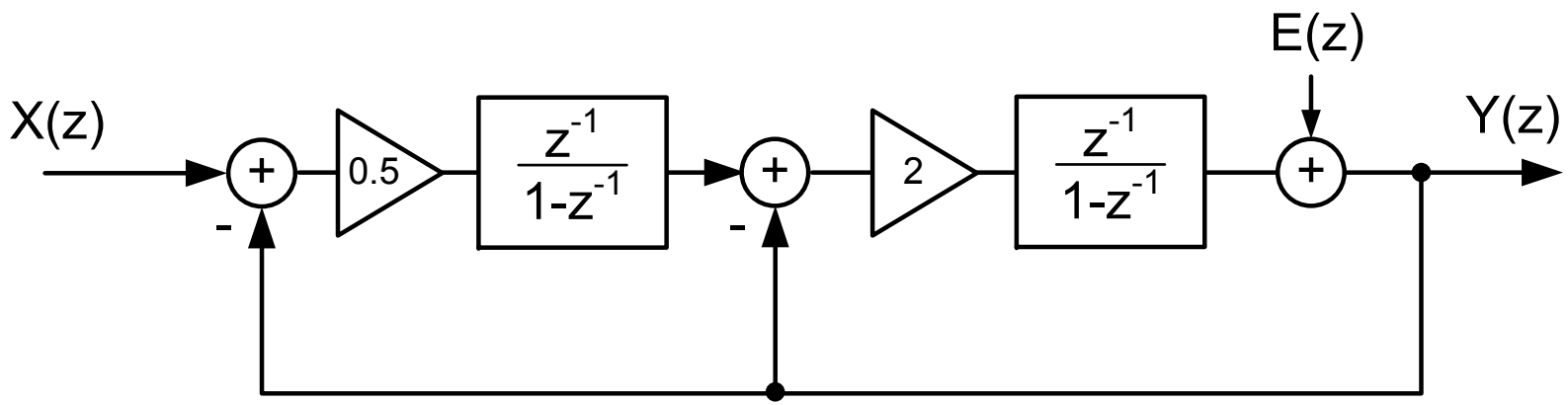
Method	ϕ1 Noise [μVrms]	ϕ2 Noise [μVrms]	Total [μVrms]	Comment
Calculation	406	245	474	Neglected switch noise during ϕ2 → smaller value than .NOISE
.NOISE	406	266	485	
PNOISE	-	-	475	Somewhat smaller than .NOISE due to finite Maxacfreq and Numsidebands
TRAN NOISE	-	-	477	Somewhat smaller than .NOISE due to statistical fluctuations (can use more samples)

- **Very good agreement between hand calculation and all three simulation approaches**

Advantages of TRAN NOISE

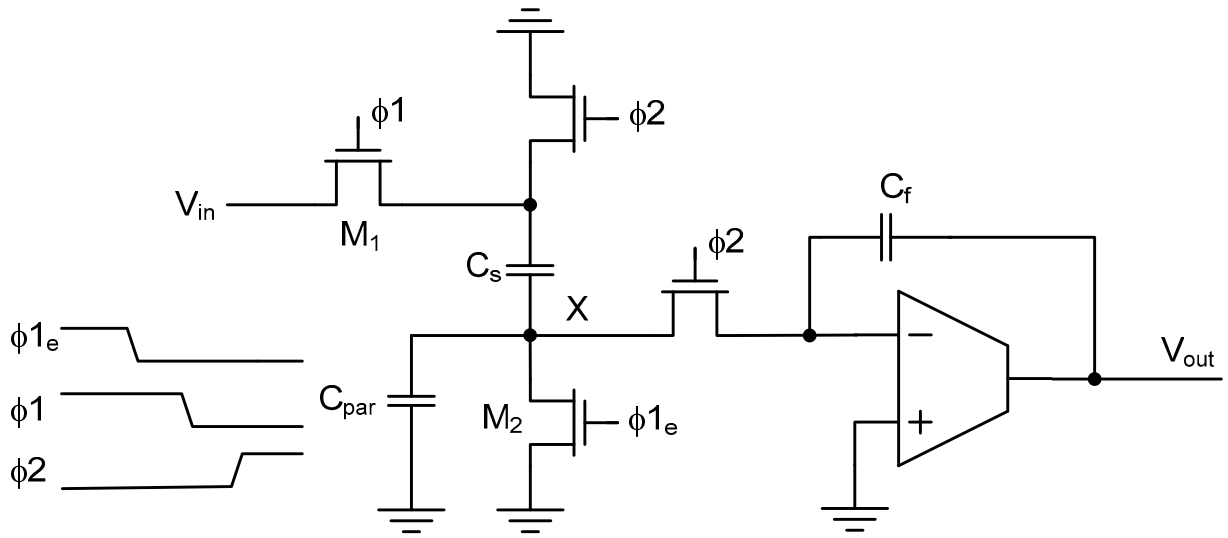
- Takes advantage of rapid advancements in very fast, spice-accurate transient simulators (such as BDA AFS)
  - Can handle much larger circuits compared to PSS/PNOISE (PSS tends to have convergence issues for large circuits)
- Intuitive inspection of waveforms
- No need to combine noises manually
  - Compared to .ac/.noise simulation flow
- Applicable also to non-periodic circuits

Second-Order ΔΣ Modulator



$$\mathrm{STF} = \frac{Y(z)}{X(z)} = z^{-2} \qquad \mathrm{NTF} = \frac{Y(z)}{E(z)} = \left(1 - z^{-1}\right)^2$$

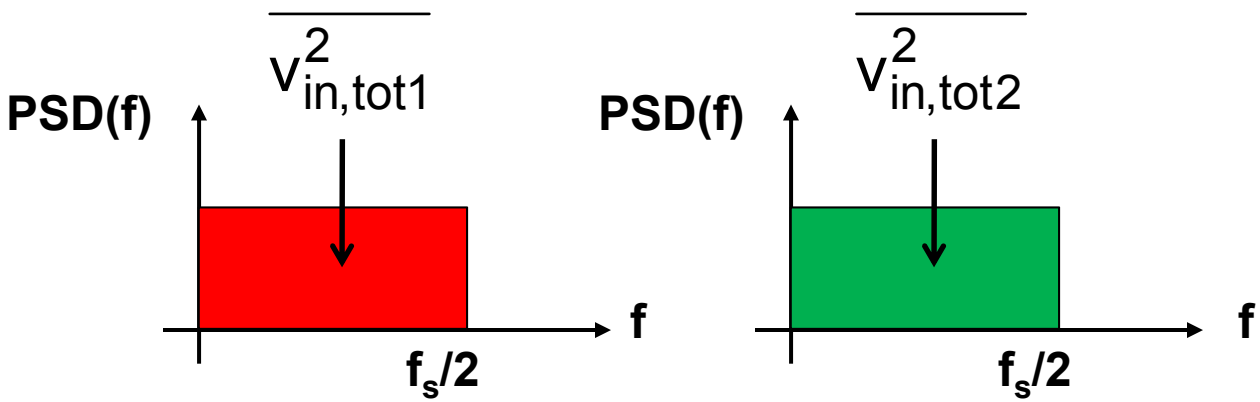
Integrator

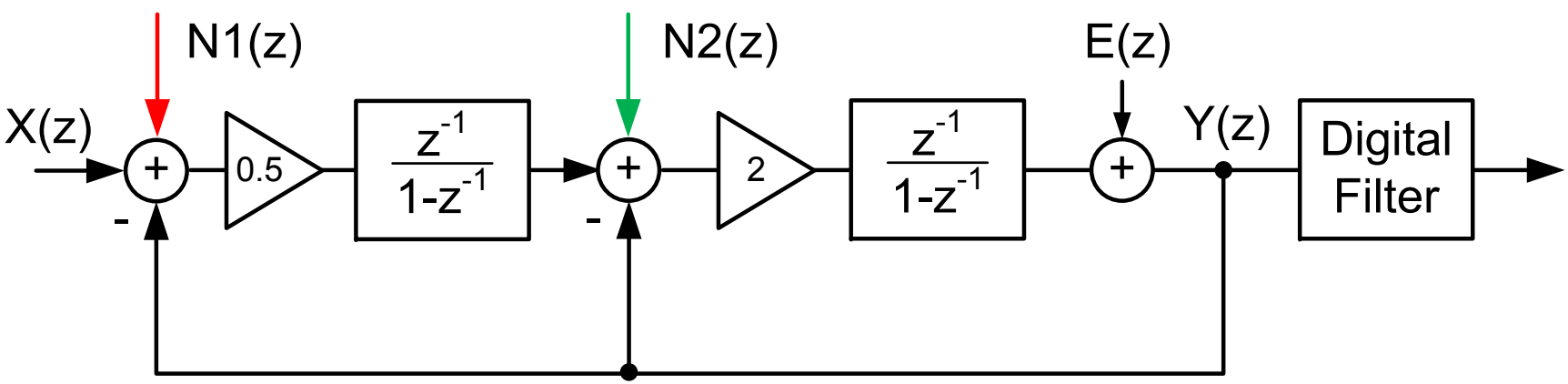


$$\overline{v_{in,tot}^2} = \frac{kT}{C_s}\left(1+\frac{C_{par}}{C_s}\right)+\frac{1}{\beta}\frac{kT}{C_{eq}}\gamma\alpha\left(\frac{C_f}{C_s}\right)^2$$

- **Input referred noise similar to T/H stage**
  - **Output referred noise is colored due to integration → best to work with input noise**

Second-Order ΔΣ Modulator

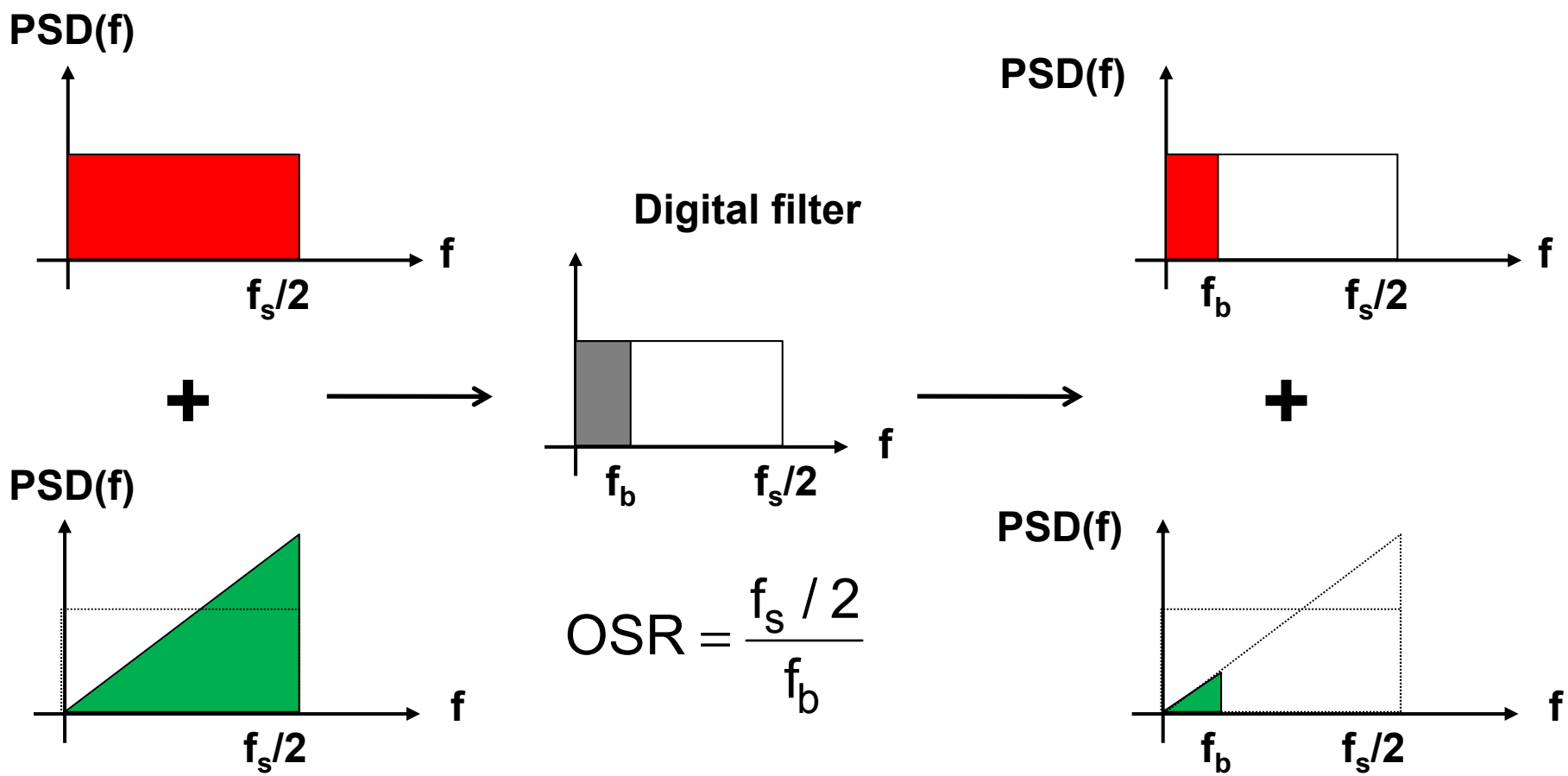




$$\frac{Y(z)}{N1(z)} = z^{-2}$$

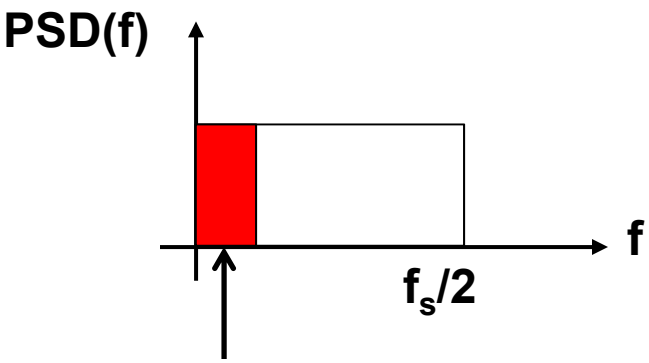
$$\frac{Y(z)}{N2(z)} = 2\left(1 - z^{-1}\right)z^{-1}$$

In-Band Noise



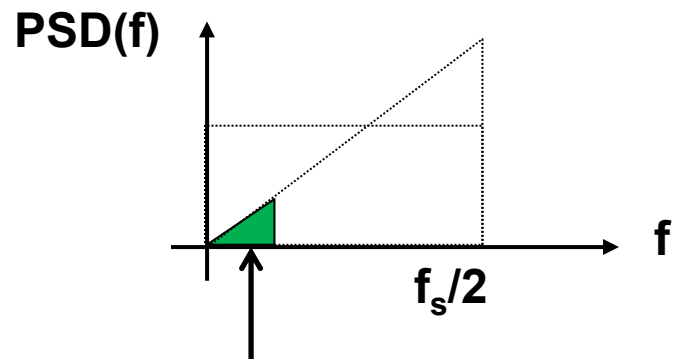
$$\mathrm{OSR} = \frac{f_s / 2}{f_b}$$

In-Band Noise



$$\overline{v_{in,tot1}^2} \cdot \frac{1}{OSR}$$

+



$$\overline{v_{in,tot2}^2} \cdot \frac{\pi^2}{3} \frac{1}{OSR^3}$$

Total in-band thermal noise at modulator input:

$$\overline{v_{in,tot}^2} = \overline{v_{in,tot1}^2} \cdot \frac{1}{OSR} + \overline{v_{in,tot2}^2} \cdot \frac{\pi^2}{3} \frac{1}{OSR^3}$$

Summary (1)

- General
  - Significance of kT/C noise and steep trade-off with power dissipation
  - Whiteness of kT/C noise samples
  - Noise folding
- Charge redistribution circuit analysis
  - Charge domain analysis of track mode noise
  - Watch out for parasitics at charge redistribution node

Summary (2)

- **Analysis of $\Delta\Sigma$ modulator**
  - **Convenient to work with input referred, equivalent white noise generators and corresponding noise transfer functions**
  - **The same approach works for SC filters**
- **SC noise simulation**
  - **Recent developments in transient simulators have made TRAN NOISE simulation an attractive alternative to more conventional methods**