

15.8 Capacitive Power-Management Circuit for Micropower Thermoelectric Generators with a 2.1 μ W Controller

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Energy scavenging [1] is an emerging method to power energy-autonomous wireless sensor systems by converting ambient environmental energy into electrical energy. Miniature as well as micro-machined thermoelectric generators (TEG) can become a suitable compact power supply for both on-the-body and industrial sensors. To minimize the overall size of the power supply, the generator has to work at its maximum power point. Due to varying thermal conditions, the generated power and voltage are not constant. Typically the output voltage is lower than the power supply voltage of the sensor. For these reasons, a power management circuit (PMC) with maximum power-point tracking capability and containing a DC/DC-converter with variable conversion factor is required that stores the generated energy in a rechargeable battery or capacitor [2].

The overall efficiency of such PMC depends on the efficiency of the DC/DC-conversion and on the power consumption of the control circuit. In high power applications, the efficiency of the DC/DC-converters is the main challenge and limitation. For ultra-low-power applications, the main challenge is the power used by the control circuit. As the power required for the operation of wireless sensor nodes is of the order of 50 to 100 μ W, the power consumption of the control circuit should be only a fraction of that. Ultra-low power PMC's reported consume 70 μ W [3] or tens of microWatts [4] which is clearly not compatible with this low converted power. This can only be compensated by an increased size of the generator. To overcome this limitation, a compact PMC has been designed that is capable of delivering micropower to its output while consuming only 1.4 μ A in the control circuit.

The TEG can be modeled as a voltage source proportional to the temperature across the TEG, in series with its internal impedance. This impedance limits the available power and introduces a maximum power point. At this point, the TEG operates at its matching point [2] and the input voltage of the converter is half the open circuit voltage of the TEG. The more flexible the conversion factor can be set, the closer to the maximum power point the TEG can operate.

The circuit consists of different blocks as shown in Fig. 15.8.1. The main block is the charge pump with a variable number of stages that performs the DC/DC-conversion. A current-sensor copies the current that flows to the output and provides it to the control circuit. A clock circuit drives the sequential logic and a voltage regulator is introduced to power the feedback circuit from the output. The current consumed by the voltage regulator does not flow through the current sensor, the current sensor measures only the power that goes actually to the output.

The principle of operation of the DC/DC-conversion determines the volume of the design. A PMC with a boost converter containing an LC-filter has a very flexible conversion factor but compact inductors have a low inductance and large series resistance. A charge-pump using capacitors has a discrete conversion factor, but results in a very compact, on-chip design.

The efficiency of such an integrated charge pump depends mainly on the ratio α of the parasitic capacitances of the bottom plate of the switching capacitors to the value of the actual switching capacitors [5]. For common poly-poly capacitors, α can be as high as 20% and this results in a peak efficiency of 64%, 55%, 52%, and 50% for 1, 2, 3 or 4 stages (Fig. 15.8.2). The present design in contrast uses metal-insulator-metal (MIM) capacitors. The distance between their bottom plate and the chip substrate is larger than for a poly-poly capacitor, reducing α to 3%. The calculated peak efficiency increases to respectively 82%, 77%, 74%, and 73% for 1, 2, 3 or 4

stages. Measurements on a charge pump with 1 or 2 stages in I3T80, a 0.35 μ m high-voltage CMOS process confirm this (Fig. 15.8.2).

The clock circuit has been developed using a relaxation oscillator operating at a frequency of 60kHz. The clock is required as an input for the charge pump. It is also used for fixing the time between the successive calculations of the optimal number of stages as well as for setting the delay between changing the number of stages and measuring the output current.

The feedback circuit is powered by the output of a linear voltage regulator. Measurements show that the voltage regulator provides the feedback circuit a power supply voltage of 1.508V with the difference between the input and output current of 109nA.

At start-up, when no output power is available and the control circuit cannot function, the output is charged through a diode and as soon as the output voltage exceeds 0.9V the power management circuit starts up. The digital control algorithm sets the number of stages (M) by maximizing the current that flows to the energy buffer. This can be done because the buffer-voltage stays constant, within a short period, and this makes the output current proportional to the output power. The current is copied, and a capacitor is charged by this current. The voltage across the capacitor is a measure for the power flowing to the buffer. The algorithm is shown in Fig. 15.8.3. Figure 15.8.4 shows the input voltage of the circuit in steady state. It can be seen that calculation of the number of stages takes only a fraction of the time. This reduces the power loss caused by working at a not-optimal number of stages.

When no power is delivered to the load, the circuit stores the number of stages of the charge pump and goes into sleep mode. The input voltage is used as a measure for the available power. The circuit starts up when the open circuit voltage of the TEG indicates that more power is available than will be consumed by the control circuit.

The PMC needs two customizations to be able to store the output power of a TEG, and they are mainly related to the internal impedance of the TEG and the power generated. The capacitor size in the charge pump must be adapted to estimated power levels. Second, the start-up voltage needs to be adaptable to the open circuit voltage of the TEG that corresponds to sufficient power.

A PMC containing a charge pump with 175pF capacitors and a maximum of 8 stages is realized in a high-voltage 0.35 μ m CMOS process. The measured overall system efficiency for a TEG with an impedance of 100k Ω is shown in Fig. 15.8.5. The controller selects the number of stages that corresponds with the highest overall efficiency. The peak efficiency is 58% for 1 stage. The circuit starts up at 1.28V when the buffer voltage is 2V, using 2 stages of the charge pump. Measurements (Fig. 15.8.6) show that the current that flows through the regulator to the control circuit is only 1.4 μ A. The voltage regulator requires 109nA of this current. The analog control blocks (current sensor, comparators) require 491nA. The clock and the digital control circuit require 800nA. As the total current through the control circuit is constant, the power consumption of the feedback and therefore the overall system efficiency depends on the output voltage. A micrograph of the circuit is shown in Fig. 15.8.7. The active area of the chip occupies 3.01mm².

References:

- [1] J. A. Paradiso, and T. Starmer, "Energy Scavenging for Mobile and Wireless Electronics," *IEEE Pervasive Computing*, vol. 4, pp. 18-27, Jan.-March 2005.
- [2] H. Nagayoshi, et al., "Comparison of Maximum Power Point Control Methods for Thermoelectric Power Generator," *Proc. 21st Intl Conf. on Thermoelectronics*, pp. 450-453, Aug. 2002.
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- [4] H. Shao, et al., "An Inductor-less Micro Solar Power Management System Design for Energy Harvesting Applications," *IEEE ISCAS*, pp. 1353-1356, May 2007.
- [5] G. Palumbo, et al., "Charge-Pump Circuits: Power-Consumption Optimization," *IEEE Trans. on Circuits and Systems - I*, vol. 49, pp. 1535-1542, Nov. 2002.

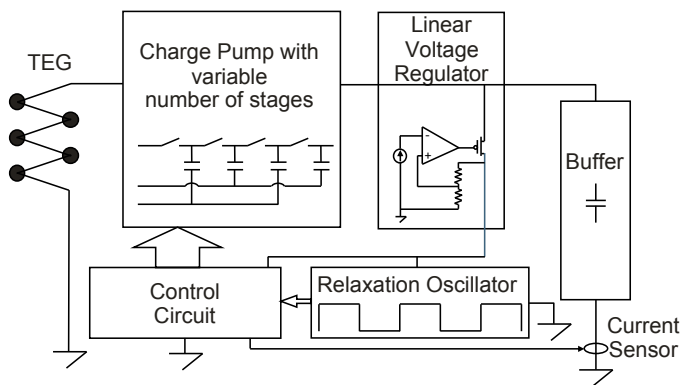


Figure 15.8.1: Block diagram of the system.

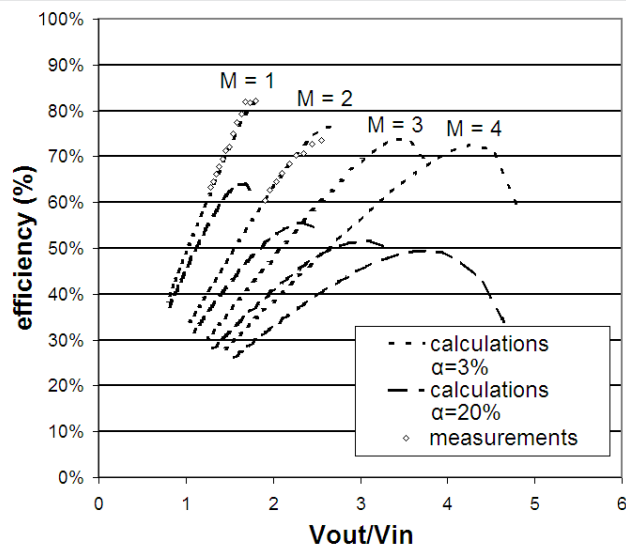


Figure 15.8.2: Charge pump efficiency calculation and measurement results.

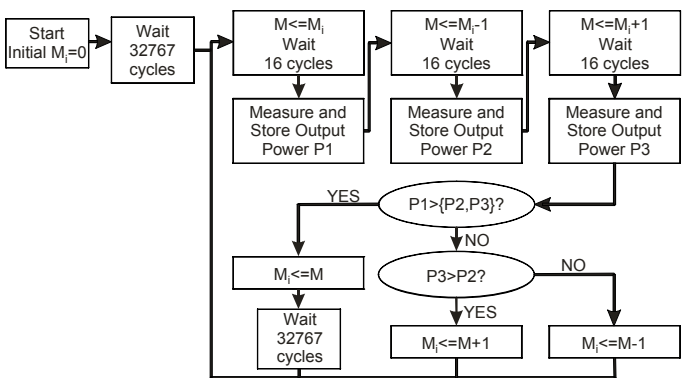


Figure 15.8.3: Digital control algorithm.

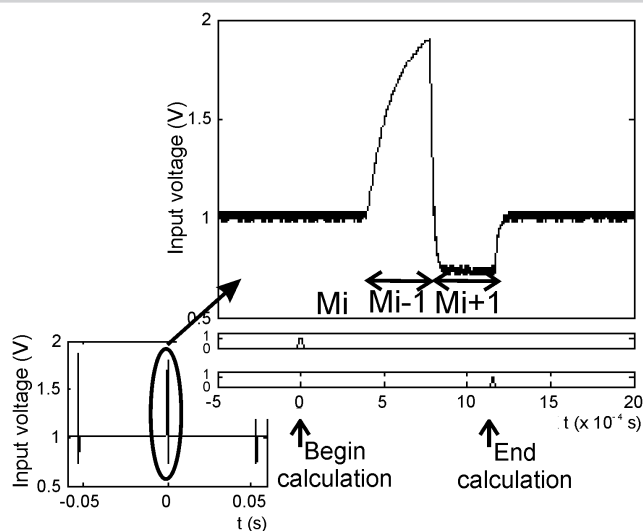


Figure 15.8.4: Measured input voltage during calculation of the optimal number of stages.

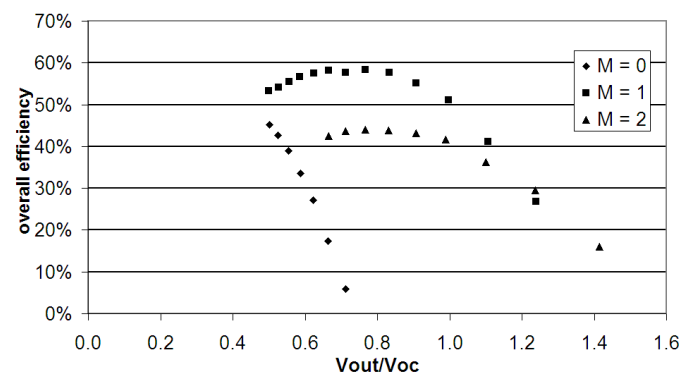


Figure 15.8.5: Overall efficiency.

	This work	[1]	[2] (simulated)
Voltage regulator output voltage	1.508V	1V	2.5V
Voltage regulator current consumption	109nA	-	-
Digital control circuit and oscillator current consumption	800nA	26.9μA	NA
Analog control circuit current consumption	491nA	43.1μA	NA
Total power consumption	2.1μW	70μW	> 10μW

Figure 15.8.6: Measurement results, compared to reference publications.

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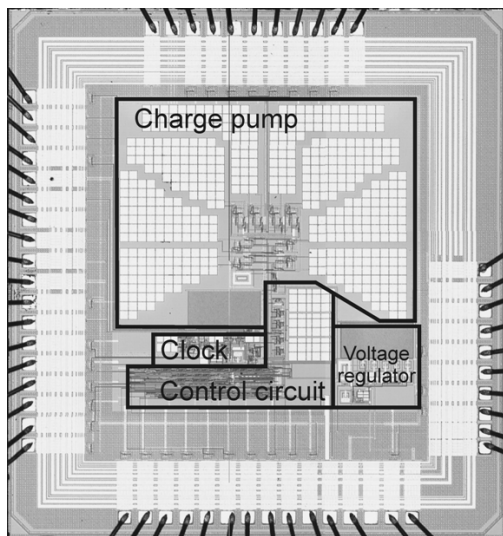


Figure 15.8.7: Die micrograph.