Design of 2Gb/s LVDS Transmitter and 3Gb/s LVDS Receiver for Optical Communication in 0.18μm CMOS Technology

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***Abstract*-Design of a high performance CMOS LVDS transceiver in optical communication application is presented. The proposed LVDS transceiver is composed of a transmitter (TX) circuit and a receiver (RX) circuit. Due to the differential transmission technique and the low voltage swing, the receiver circuit has a stable hysteresis voltage and is with high speed operation, meanwhile the transmitter circuit provides a low voltage differential signal by using a closed-loop control circuit. The simulation results show that the LVDS transceiver working stably at 3.3V power supply with maximal transmission speed of 2Gb/s. The core chip size of the circuit is 150×150mm^2, and the dynamic power consumption is only 23mW.**

Key words: LVDS; Transceiver; CMOS; low power

I. INTRODUCTION

With the development of integrated circuit technology and the increasing performance of the communication, network and computer systems, the requirement of higher bit rate and longer distance transmission on cable becomes more and more urgent. Otherwise, the power consumption becomes a very important issue to system, and the power saving is useful to increase the system stabilization, reliability and reduce the system costs related to packaging and additional cooling system.

Low Voltage Differential signaling (LVDS) technology[1] is then proposed and developed to resolve the bottleneck in high speed data transmission. Now the LVDS have becomes one of the most promising solution to massive data communication, such as optical communication, LCD panels and chip-to-chip transmission[2]-[4]. The LVDS has the low voltage swing (250mV-400mW) to minimize the power dissipation, the differential transmission mode to improve the robustness of the common-mode voltage bounce and crosstalk, and the current transmission mode to reduced noise margin. However, as the data rate increases rapidly, the data drift and data jitter due to manufacture defects, environment noise, cross-talks and et al, will make it difficult for LVDS receiver to restore the transmitted data[5]. This will require much redundant circuit and waste much chip area to detect and recover the data and clock fault. But the clock and data fault tolerant architectures and circuits are still a significant methodology to solve the problem in the design and manufacture of integrated circuits[6]. So how to design a high performance, low power dissipation and regular LVDS transceiver is very valuable to reduce the system reliability and cost.

To satisfy recent demand of broad bandwidth, a LVDS transceiver with a 3Gb/s receiver and a 2Gb/s transmitter is developed. In section II, the LVDS transceiver is presented, and the detailed design of the transmitter and receiver circuits on standard 0.18μm CMOS process is illustrated respectively. In section III, the performance of the LVDS transceiver is discussed by the simulations. The conclusion is drawn in section IV.

II. LVDS TRANSCEIVER CIRCUIT DESIGN

The LVDS transceiver is consists of a TX circuit and a RX circuit. Fig.1 shows the conventional LVDS transceiver architecture with point-to-point transmission. The TX circuit transfers the digital signal to the low voltage differential output signals. The difference between the output signal V_{OUT+} and V_{OUT-} is about ±250~400mV, and the common-mode output voltage is 1.125~1.275V. Fig.2 shows the standard output signal waveforms of the TX circuit.

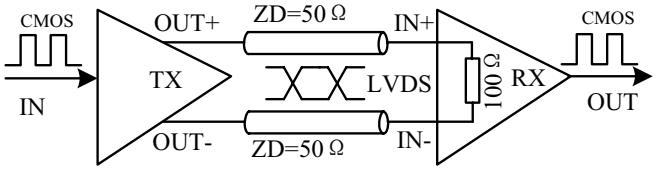

Fig.1 Connection of the LVDS TX and RX circuits

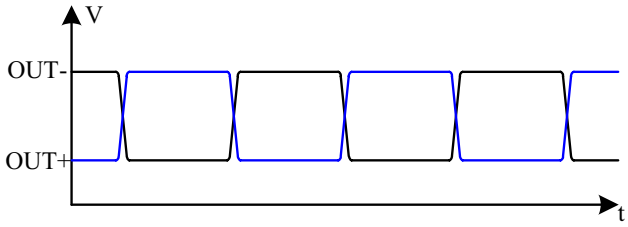

Fig.2 Output waveforms (Vout+ and Vout-) of the TX circuit

The signals V_{OUT+} and V_{OUT-} reach the input ports of the RX circuit through long distant cables, and then the RX circuit transfers the differential signals to the digital output signal. The RX digital output signal becomes "0" or "1" by the polarity of the difference $V_{ID}=V_{IN+}-V_{IN-}$. For there is a

different voltage between the ground of the TX circuit and RX circuit, the common voltage drift of V_{IN+} and V_{IN-} will be found. The RX circuit must work well in the large common input range of 0~2.4V by the LVDS criterion.

2.1 The TX circuit

The TX circuit is composed of three stages: LVDS level shifter, pre-buffer and driver circuit, which is shown in Fig.3. The voltage reference circuit is also required to implement a dc voltage which is independented over process, temperature, and supply voltage variation. The level shifter circuit converts the 1.8V CMOS digital signal to 3.3V digital signal. The pre-buffer increases the driver capability of the digital signal to control the driver circuit. The LVDS signals are generated by the driver circuit finally.

Fig.4 shows the LVDS driver circuit, which is the most important of the TX circuit. It operates as a current source with switched polarity. The driver circuit works more stably in the double current-source mode. The common-mode output voltage will be drift with the practical nonideal transmission lines and pad parasitic effect, so the common-mode feedback circuit is added to make the output common voltage into 1.2V steadily.

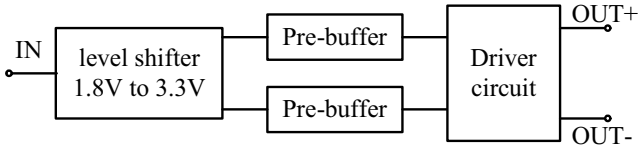

Fig.3 Architecture of the TX circuit

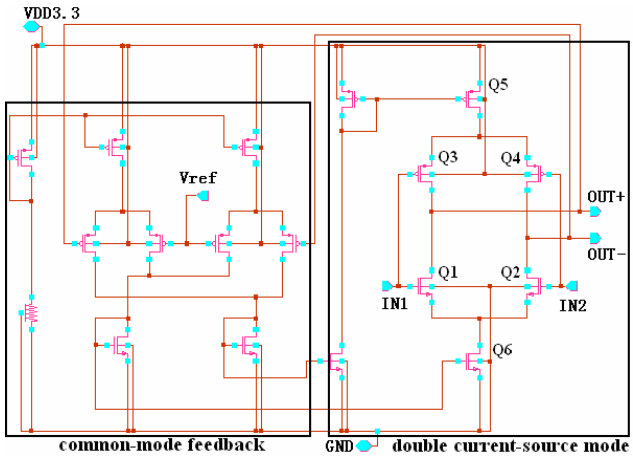

Fig.4 LVDS driver circuit

The current through Q5 and Q6 is set to 3.5mA by the internal current mirror circuit. The input signals of "IN1" and "IN2" are a pair of digital signals with opposite polarity. When Q2 and Q3 transistors are switched on, Q1 and Q4 transistors are switched off, and then the output current is positive to flow through the external 100Ω load resistor. The voltage difference between the signal OUT+ and OUT- is +350mV. When Q2 and Q3 transistors are switched off, and then the voltage difference between the signal OUT+ and OUT- is -350mV. The differential output voltage swing is established.

2.2 The RX circuit

The RX circuit is composed with three stages: pre-amplifier, hysteresis comparator and driver buffer. The whole structure of the LVDS receiver is shown in Fig.5.

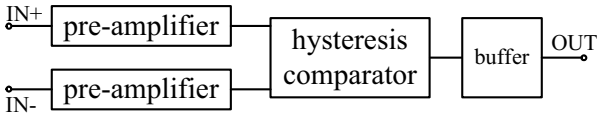

Fig.5 Architecture of the RX circuit

The amplitude of the low voltage differential signals and common-mode output voltage will be decreased when it is through the long cable distance, and then the receiver must amplify the low-voltage differential signal at first. The pre-amplifier circuit is a folded cascade amplifier with mixing NMOS and PMOS differential pair input to implement rail-to-rail common-mode input range (shown in Fig.6). The pre-amplifier gain is about 10dB and the -3dB bandwidth is 1GHz.

The hysteresis comparator transfers the amplified low-voltage differential signals to the digital output signal as shown in Fig.7. The hysteresis function is used to remove output oscillation effect which is generated by the input signal instability. By the LVDS criterion, the hysteresis voltage is set to 25mV and it will be designed not to be affected possibly by the manufacture process, temperature and common-mode voltage. Accessing the appropriate bias current and W/L of Q1, Q2, Q3 and Q4, the response speed, offset voltage and slew rate are other performance index to consider carefully.

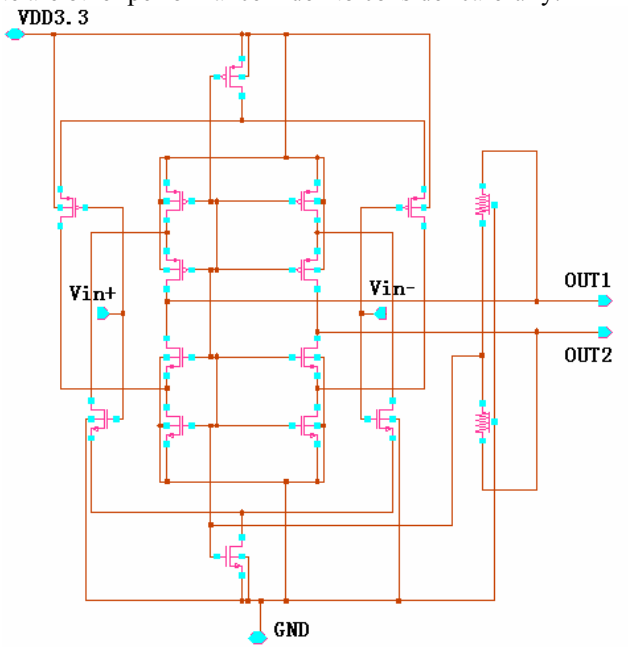

Fig.6 Pre-amplifier of the LVDS receiver

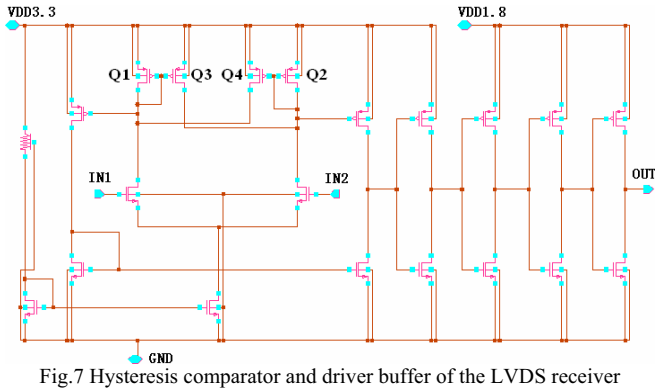

Fig.7 Hysteresis comparator and driver buffer of the LVDS receiver

III. LAYOUT AND SIMULATION

The LVDS transceiver circuit is designed with 0.18μm CMOS process using 1P6M layers. Fig.8 shows the core layout of the LVDS transmitter and receiver circuits. In order to evaluate the accurate performance of the LVDS transceiver circuit, the whole circuit is simulated by the Cadence Spectre software.

Fig.9 shows the LVDS waveforms of the connected TX and RX circuits at 2Gb/s data rate (Suppose the pad parasitic capacitor 3pF). The delay time of the LVDS output signals in the TX circuit is about 0.75ns. The delay time in the RX circuit is 1.75ns. The total power consumption of the TX and RX circuits is 21mW and 2mW at 2Gb/s data rate, respectively.

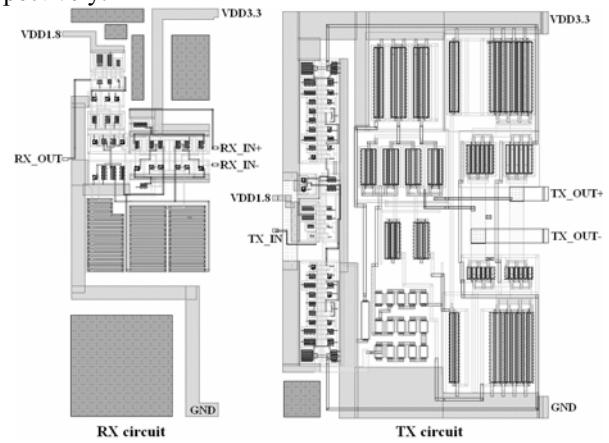

Fig.8 the core layout of the LVDS transceiver
(Left: RX circuit, Right: TX circuit)

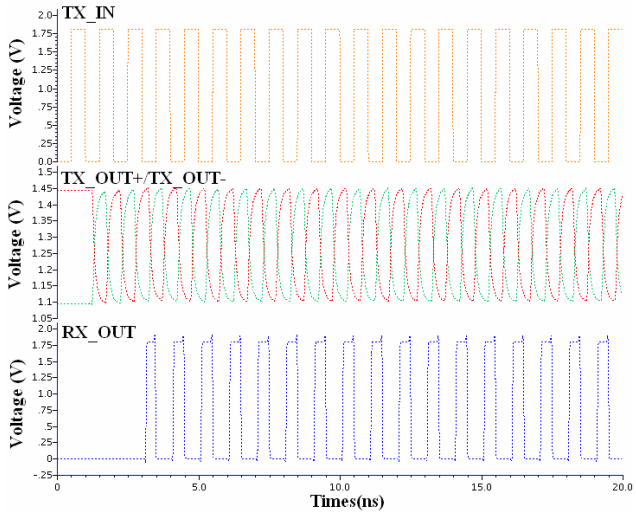

Fig.9 the LVDS waveforms of the connected TX and RX circuits at 2Gb/s data rate

IV. CONCLUSION

A high performance CMOS LVDS transceiver with 2Gb/s TX circuit and 3Gb/s RX circuit in optical communication application is proposed in this paper. The transceiver circuit is designed in standard 0.18μm CMOS process. The simulation result proves that the data rate is up to 2Gb/s, and the output low voltage differential signals are according with the LVDS standard specifications. The TX and RX circuits have low dynamic power dissipation with only 23mW when the data rate being up to 2Gb/s.

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