Multi-Voltage Designs

@UPF Flow

V0.1

What is UPF?

Unified Power Format (UPF), a format to describe ***low power intent*** for design implementation, analysis and verification, is the latest standard developed by **Accellera**.

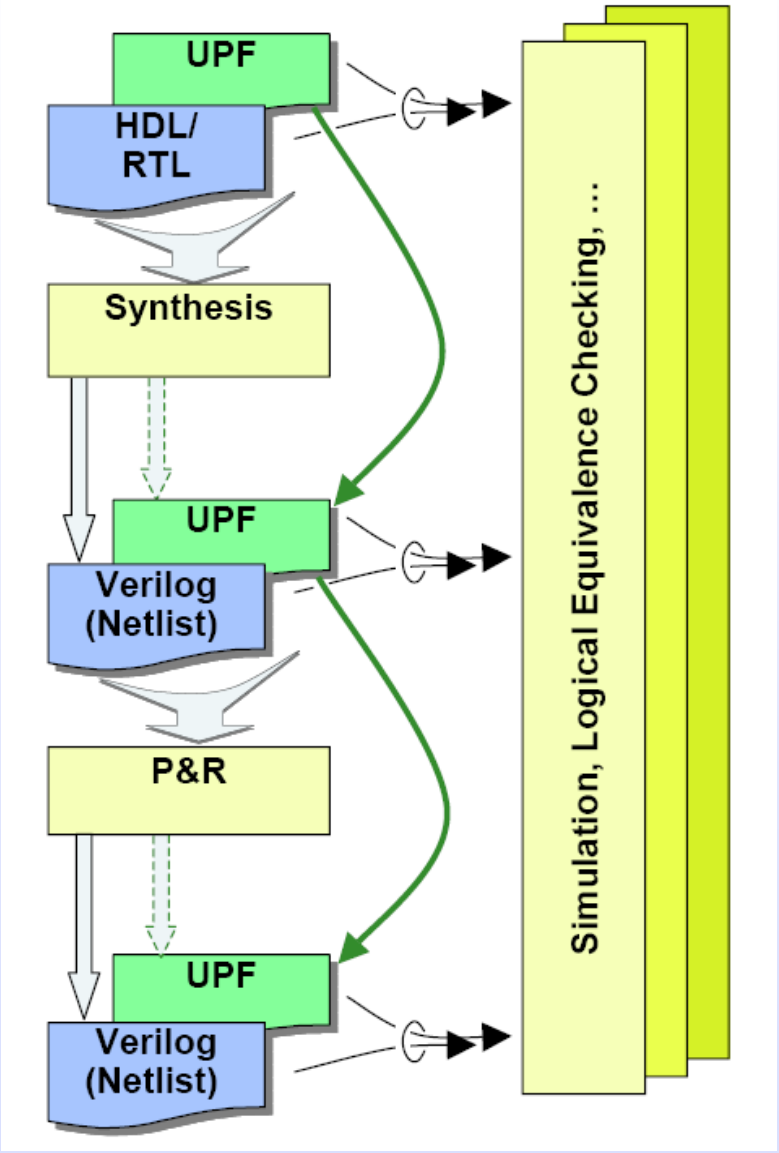
It enables ***open, multi-vendor*** tool flows and solutions for low-power ASIC and SoC design. The true value of a single, widely adopted standard is demonstrated by interoperability of products from a range of EDA suppliers who support the UPF standard. Designers of modern, low-power ICs are the ultimate beneficiaries of UPF

如果要問電子設計領域最重要的三件事是什麼：答案就是：低功率、低功率和低功率。

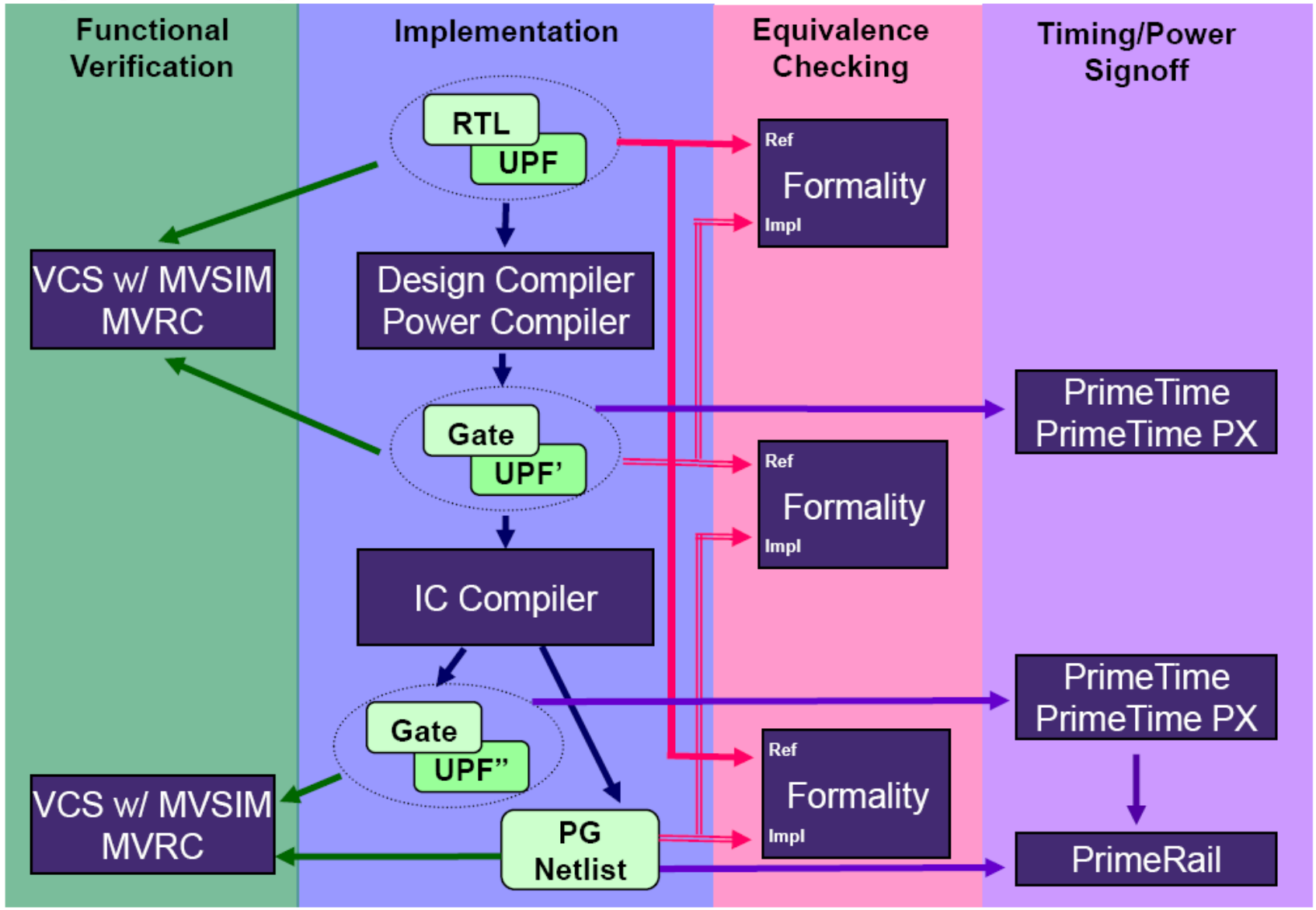
隨著工藝幾何尺寸不斷縮小到90納米、65納米及以下，漏電流問題越來越突出，限制了手持設備的電池壽命。為了把洩漏功率降至最低，設計人員開始採用功率門控技術—關斷未在使用的模組的電源，通常是利用片上開關關斷。這樣，在那些斷電和上電的域間就需要隔離單元，還需要一種策略來保存關斷期間的狀態。

UPF提供了一個機制來描述與 RTL無關設計的功率意圖。它允許設計人員定義功率門控所需的功率域、隔離策略和保持策略。它還允許設計人員定義電平轉換器策略和功率狀態表，用來處理多 個功率域。利用UPF，可以使全設計流程中的所有工具統一化，以實現和驗證同一套功率降低策略。

UPF Tool Flow

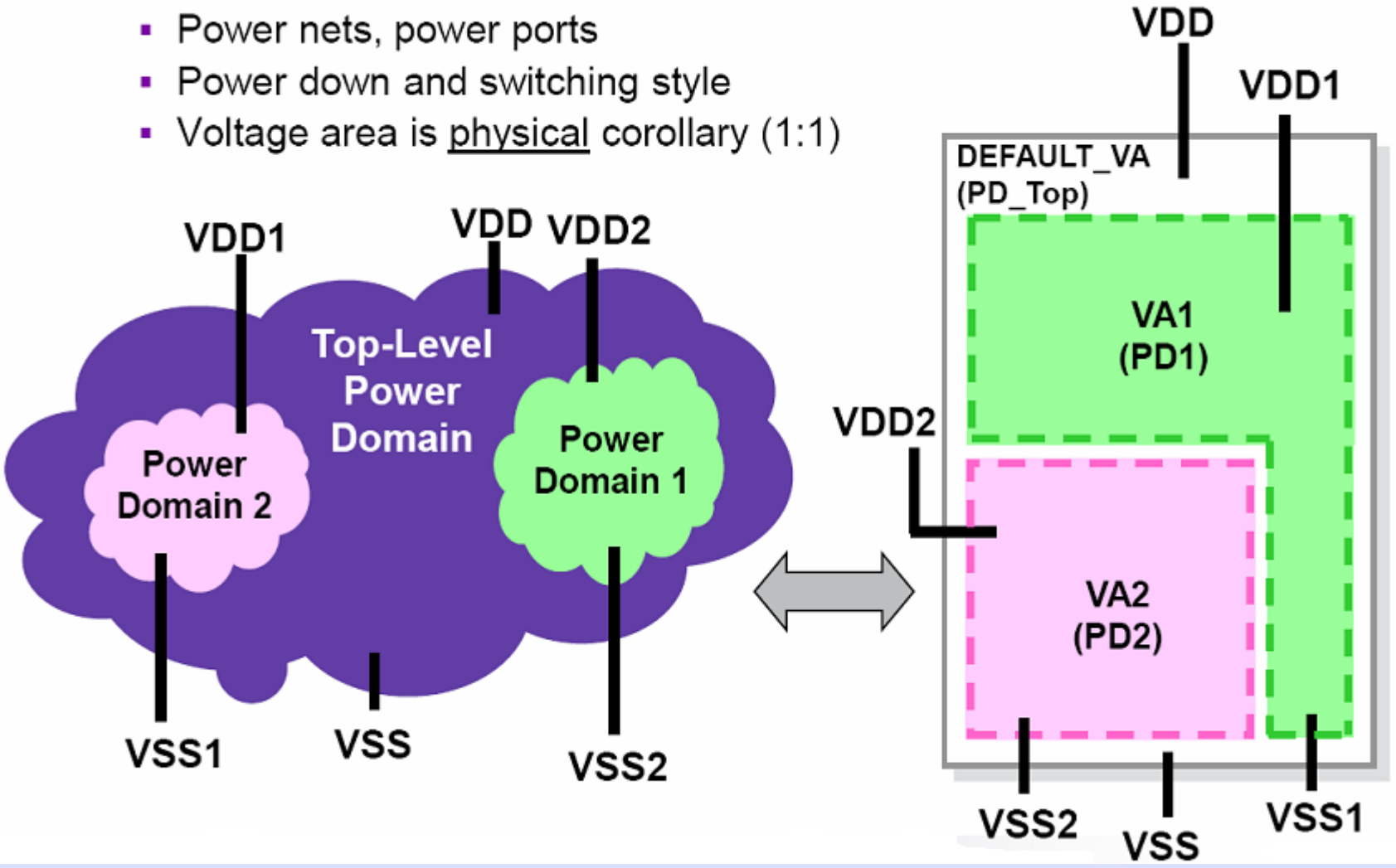


Synopsys Low Power Flow with UPF

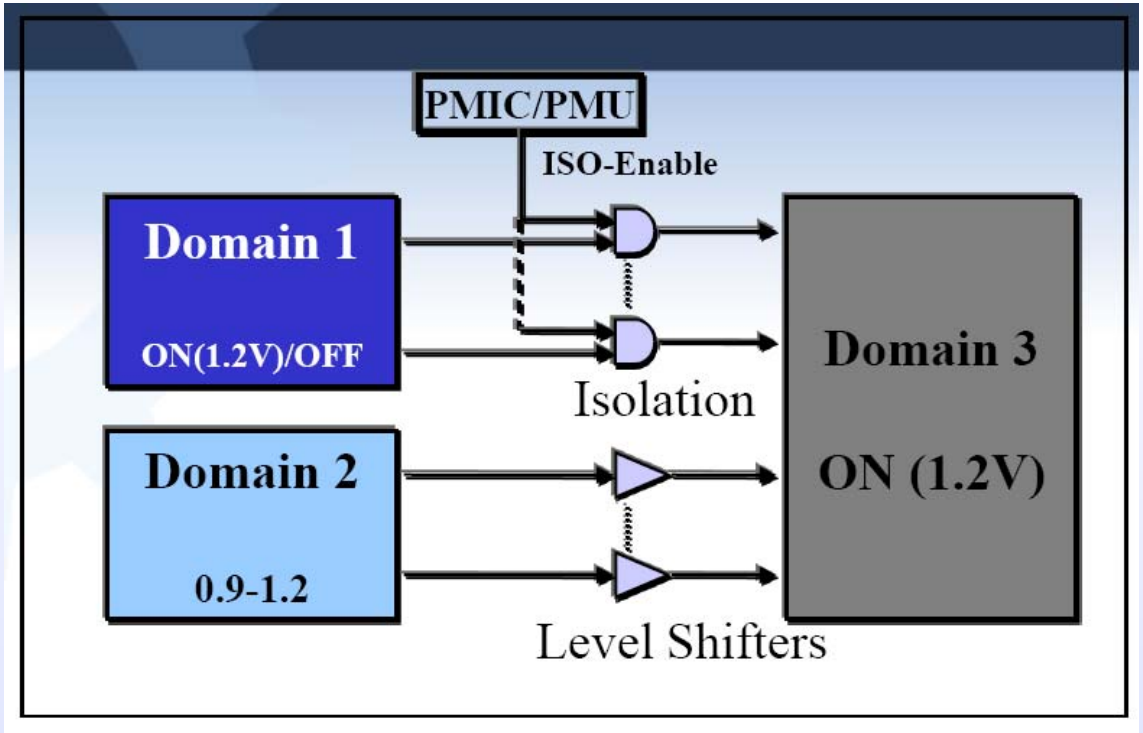


Power Domain Definition on top of the design

- Logic partition with common power characteristics
  - Power nets, power ports
  - Power down and switching style
  - Voltage area is physical corollary (1:1)



Structural Definition



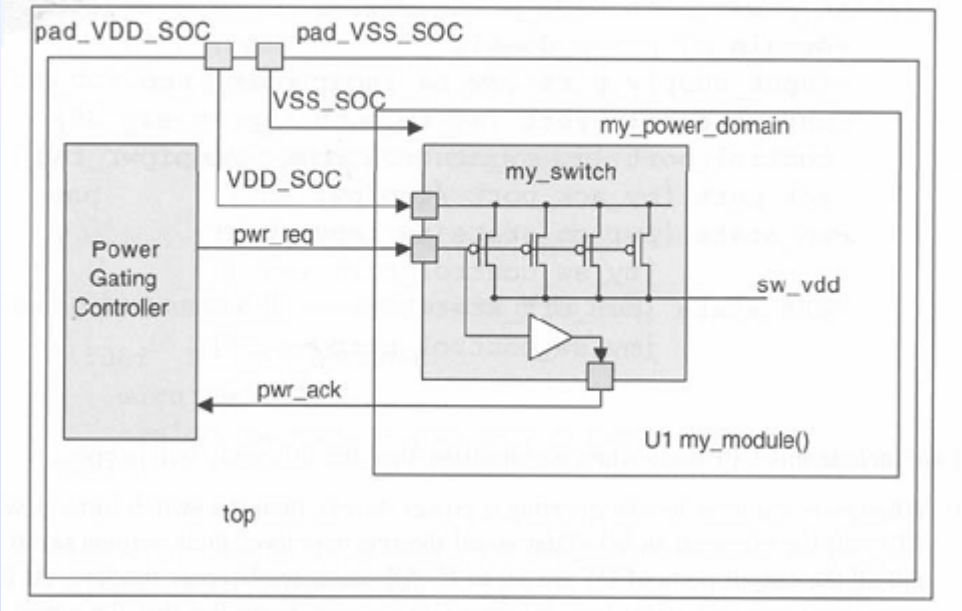
	Domain1	Domain2	Domain3
Mode1	1.2V	1.2V	1.2V
Mode2	Off	1.2V	1.2V
Mode3	Off	0.9V	1.2V

Design Verification – RTL Level

Hardware description languages (HDLs) do not directly support describing power connections on RTL level

1. Unified Power Format (UPF) standard defines language and simulation semantics, which some simulators already support
2. Or some scripting/manual power functionality description needed

➢Example system:



➢UPF declaration:

```
create_power_domain top -include_scope

create_power_domain top_power_domain -include_scope

create_supply_net VDD_SOC  -domain top_power_domain
connect_supply_net VDD_SOC -ports {pad_VDD_SOC}

create_supply_net VSS_SOC  -domain top_power_domain
connect_supply_net VSS_SOC -ports {pad_VSS_SOC}


set_scope U1
create_power_domain my_power_domain -include_scope

create_supply_net sw_vdd -domain my_power_domain

set_domain_supply_net my_power_domain
    -primary_power_net sw_vdd
    -primary ground_net /top/VSS_SOC
create_power_switch my_power_switch
    -domain my_power_domain
    -input_supply_port {my_sw_input_port /top/VDD_SOC}
    -output_supply_port {my_sw_output_port sw_vdd}
    -control_port {my_sw_control_port  /top/pwr_req}
    -ack_port {my_ack_port /top/pwr_ack}
    -on_state {pwr_on_state my_input_port
               {my_sw_control_port ==1 })}
    -off_state {pwr_off_state
               {my_sw_control_port == 0}}
```

How to Creating Power Domains

1. If power domains are defined $power, $isolate in the RTL:
   (only VCS support this setting)
   the infer_power_domain command translates RTL power domain constructs to power domain objects that Design Compiler can handle.

2. If the RTL does not have power domain constructs:
   Use UPF declaration, power domains can still be defined from the shell (in both Design Compiler and IC Compiler) using the create_power_domain command. Note that the top-level power domain must be created first. The create_power_net_info command creates the power net info objects.

UPF Example:

```
create_power_domain TOP
create_power_domain MULT \
                        -object_list [get_cells Multiplier] \
                        -power_down \
                        -power_down_ctrl [get_nets mult_off]

create_power_net_info VDDM -power
create_power_net_info VDDMS -power
create_power_net_info VSS -gnd
```

Power Aware Simulation @VCS

1. Synopsys power system task (verilog/VHDL) offers the capability to perform low power simulation with Synopsys VCS in RTL level. The verilog system task coding are $power and $isolate.
2. In RTL netlist, users need to describe shutdown domain's behavior through $power.
3. Users also have to illustrate connectivity between shutdown domain and regular domain through $isolate. This includes isolation cells' input/output signals, control signals and clamp signals.

4. VCS command can be invoked using the following syntax:
   % unix> vcs –power_aware [vcs options]

Power Aware Simulation @VCS

$power:

construct defines a power domain and designates its power control signals. In Verilog, a power domain is specified using a system task:

```
$power (<domain_name>,
        <power_on_net>,
        <on_sense_expression>,
        <power_on_ack_net>,
        <ack_sense_expression>,
        <instance1>, <instance2>, …, <instanceN>);
```

$isolate:

construct specifies the isolation behavior of a particular signal.

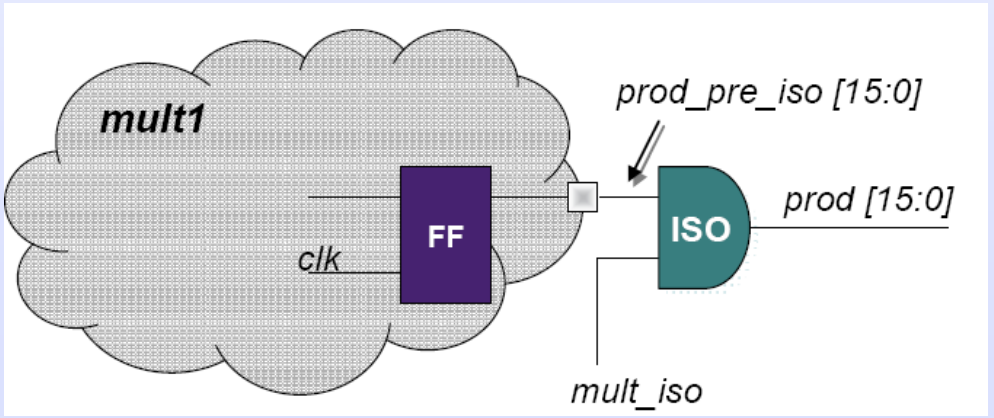
```
$isolate(<isolated_signal>, <enable>, <signal>, <clamp>)
```

Power Aware Simulation @VCS

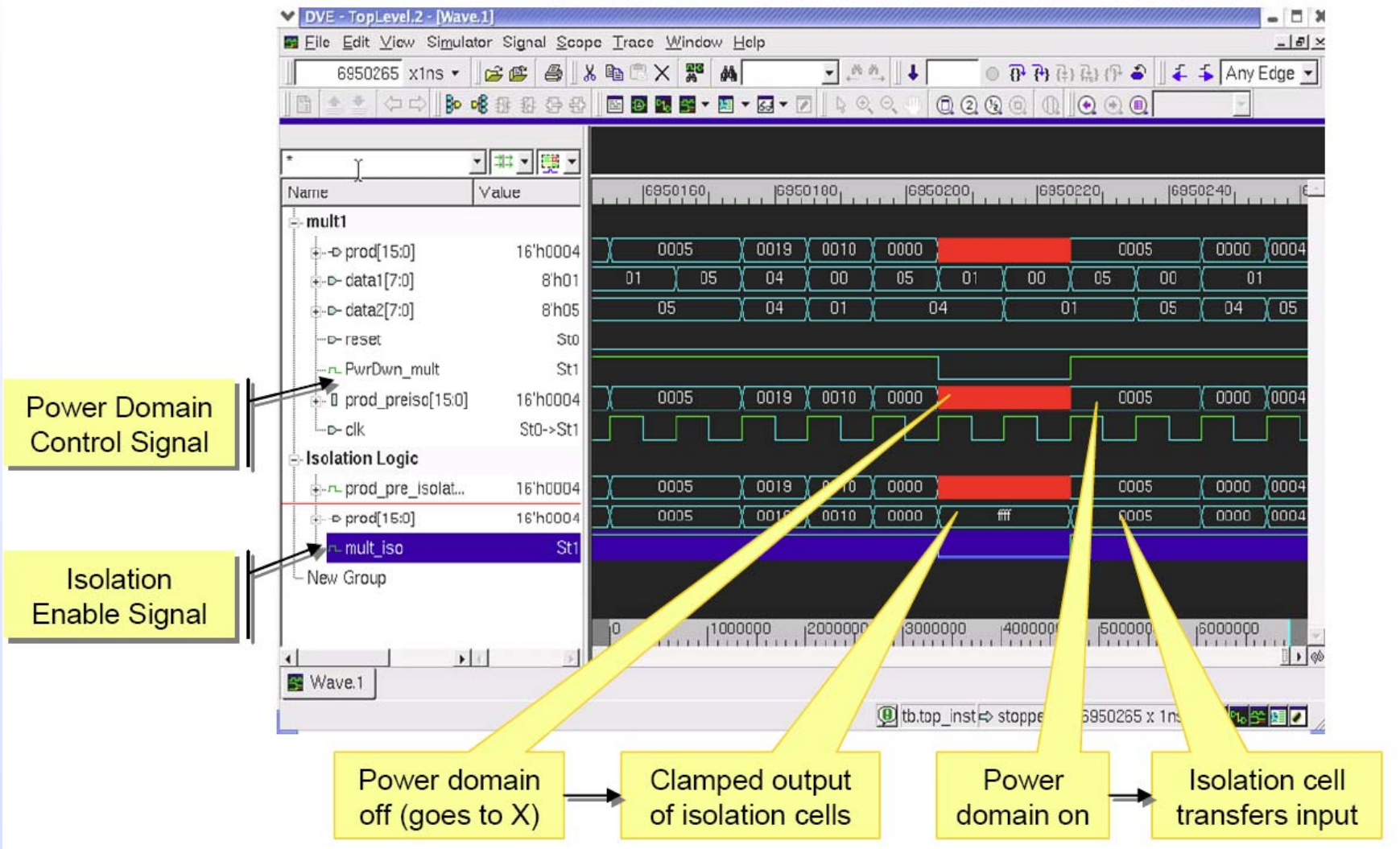
Power Aware Simulation Example:

```
initial
begin
  $power("PD_mult", PwrDwn_mult, 0'b0, "prod_pre_iso[15:0]");
end

always @*
begin
   $isolate(prod[15:0], multi_iso, prod_pre_iso[15:0], 16'hFFFF);
end
```

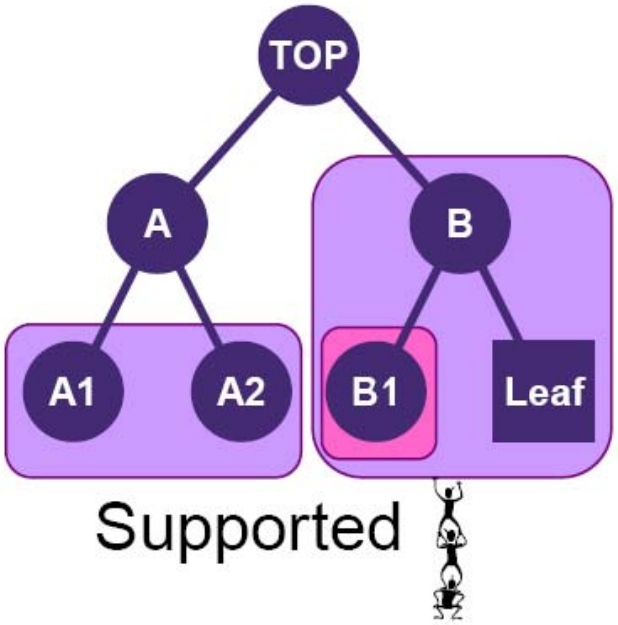


Power Aware Simulation @VCS

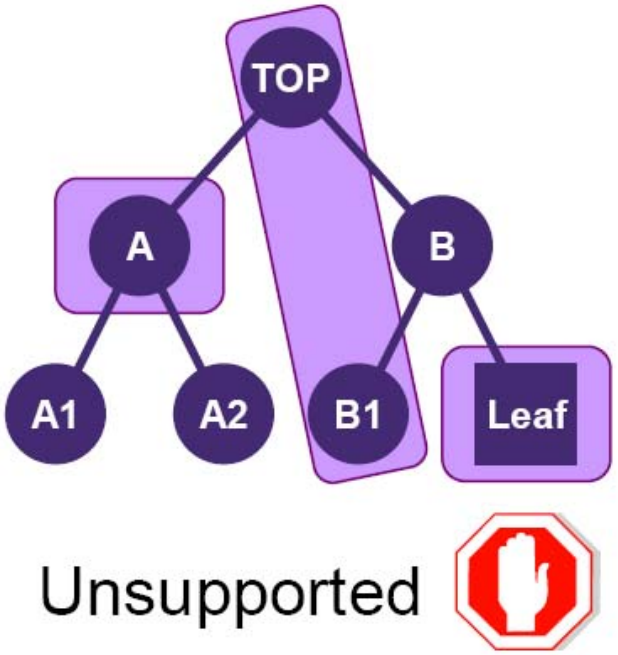


Power Domain vs. Logic Hierarchy

- Nested power domains are supported
- Logically disjoint power domains are not supported



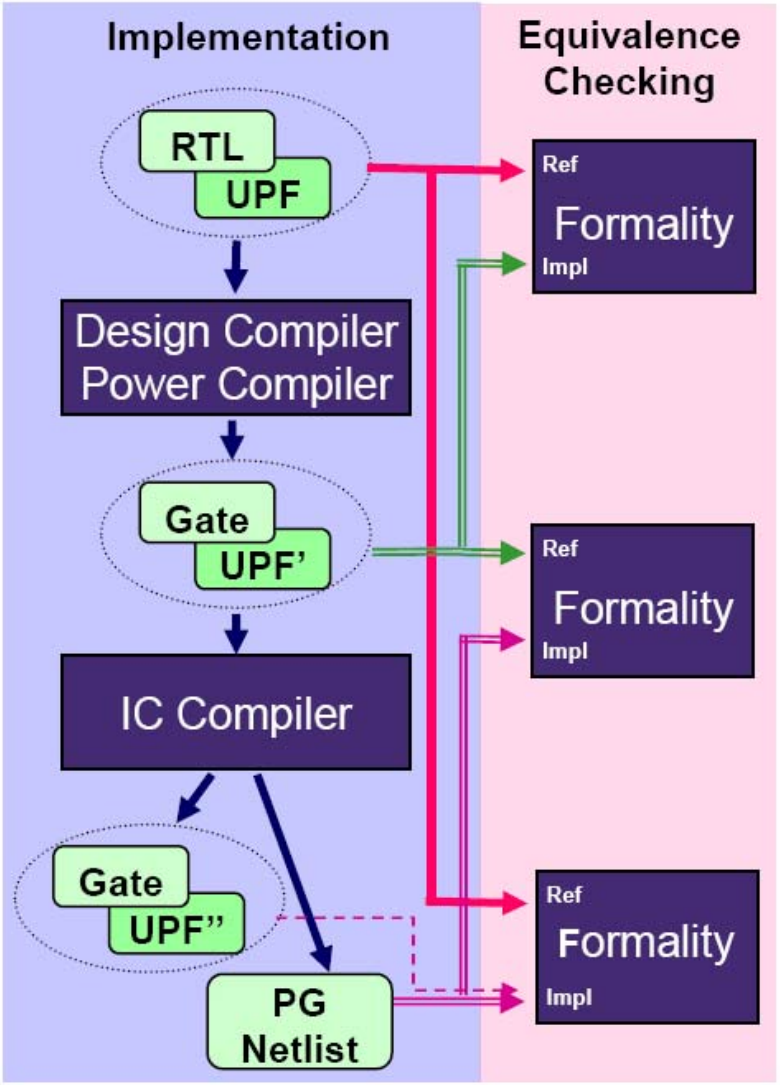
Supported



Unsupported

Equivalence Checking Using Formality

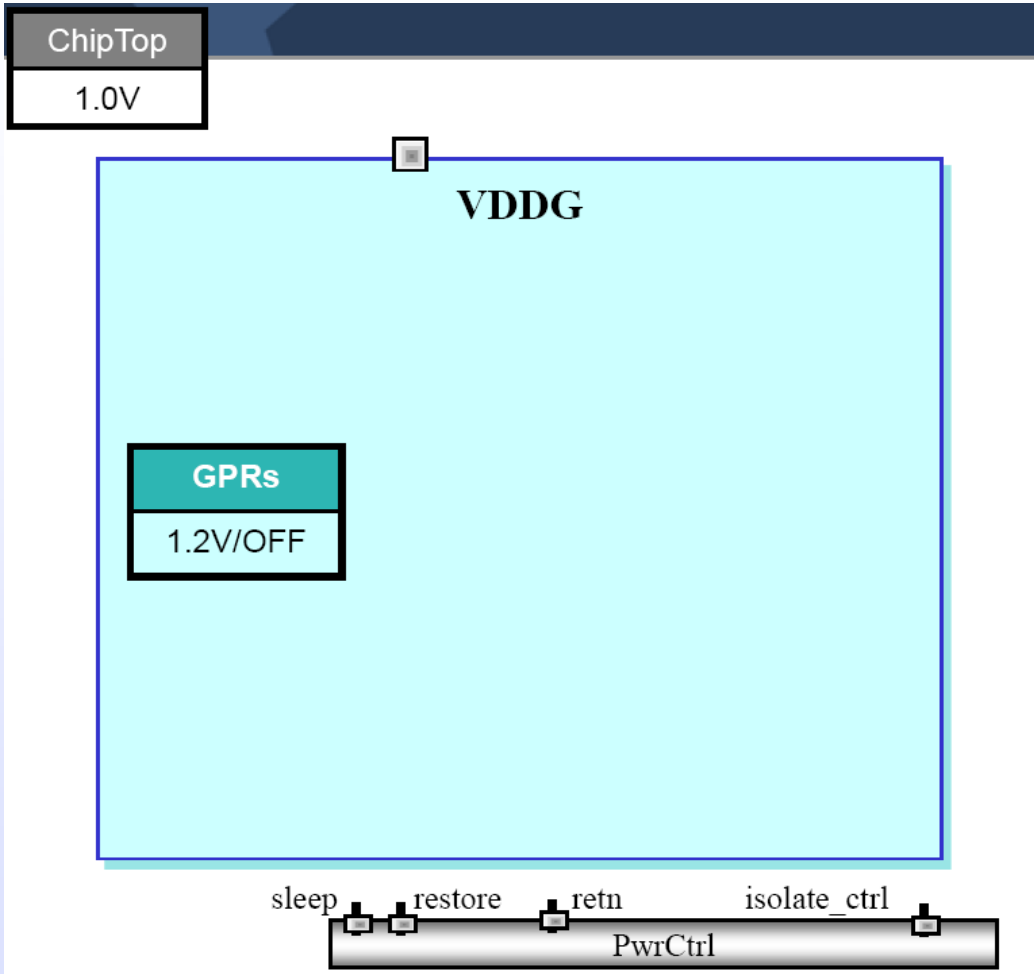
- Compares any of the following pairs
  - RTL+UPF vs. DC netlist+UPF'
  - RTL+UPF vs. ICC PG netlist
  - DC netlist+UPF' vs. ICC PG netlist
- Verifies
  - Powered-up functionality
  - Failing points if the implementation powers down in a manner inconsistent with the reference design + UPF
- Power domains that are shutdown in reference design are considered "dont care" and will not be verified



UPF Language Syntax

- create_power_domain
- create_supply_port
- create_supply_net
- connect_supply_net
- set_domain_supply_net
- connect_supply_net
- add_port_state
- create_pst
- add_pst_state
- create_power_switch
- set_retention
- set_retention_control
- map_retention
- set_isolation
- set_isolation_control
- set_level_shifter

Scope of a Power Domain



- Power domain created at lower level scope

```
create_power_domain
GPRS -elements GPRs
-scope GPRs
```

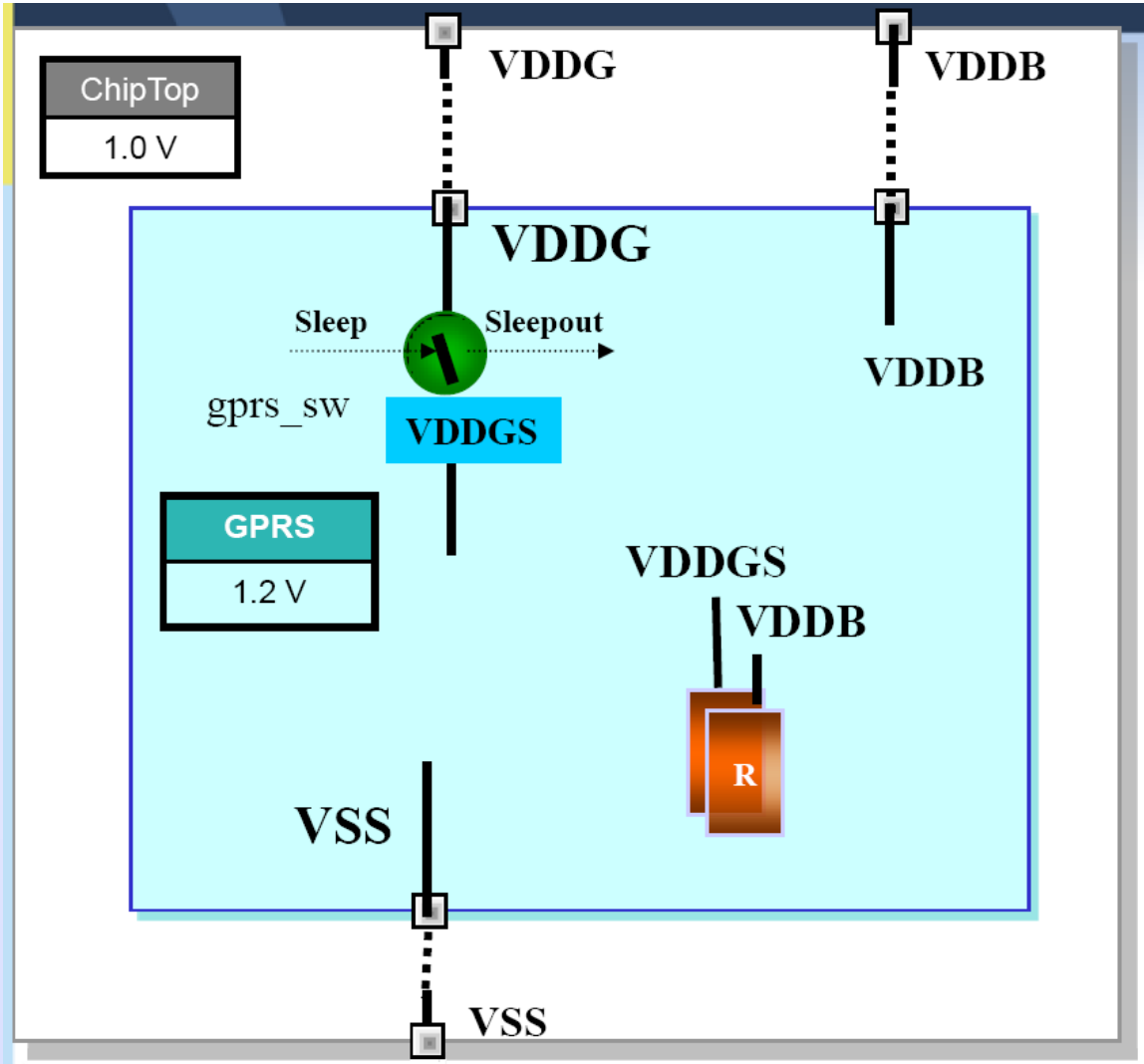
- Power domain created as

```
GPRs/GPRS
```

- Subsequently all UPF components for power domain GPRS will be created at GPRs level

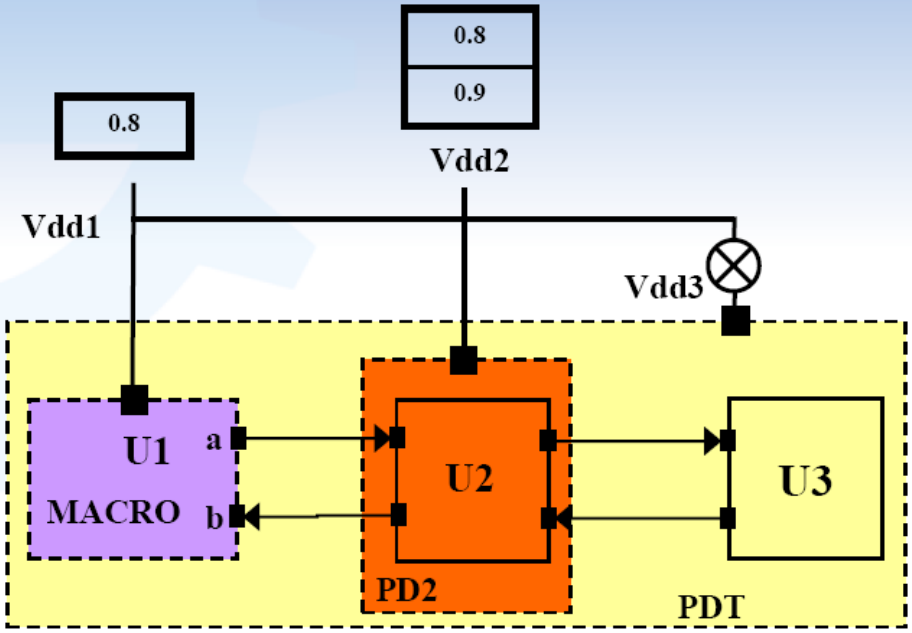
```
create_supply_port
VDDG -domain GPRS
```

Supply Network



- UPF can specify a complete power supply network
  - Supply ports
  - Supply nets
  - Power switches
  - Implicit connections based on PD
  - Explicit supply connections
- UPF commands
  - `create_supply_ports`
  - `create_supply_nets`
  - `create_power_switch`
  - `connect_supply_net`
  - `set_domain_supply_net`

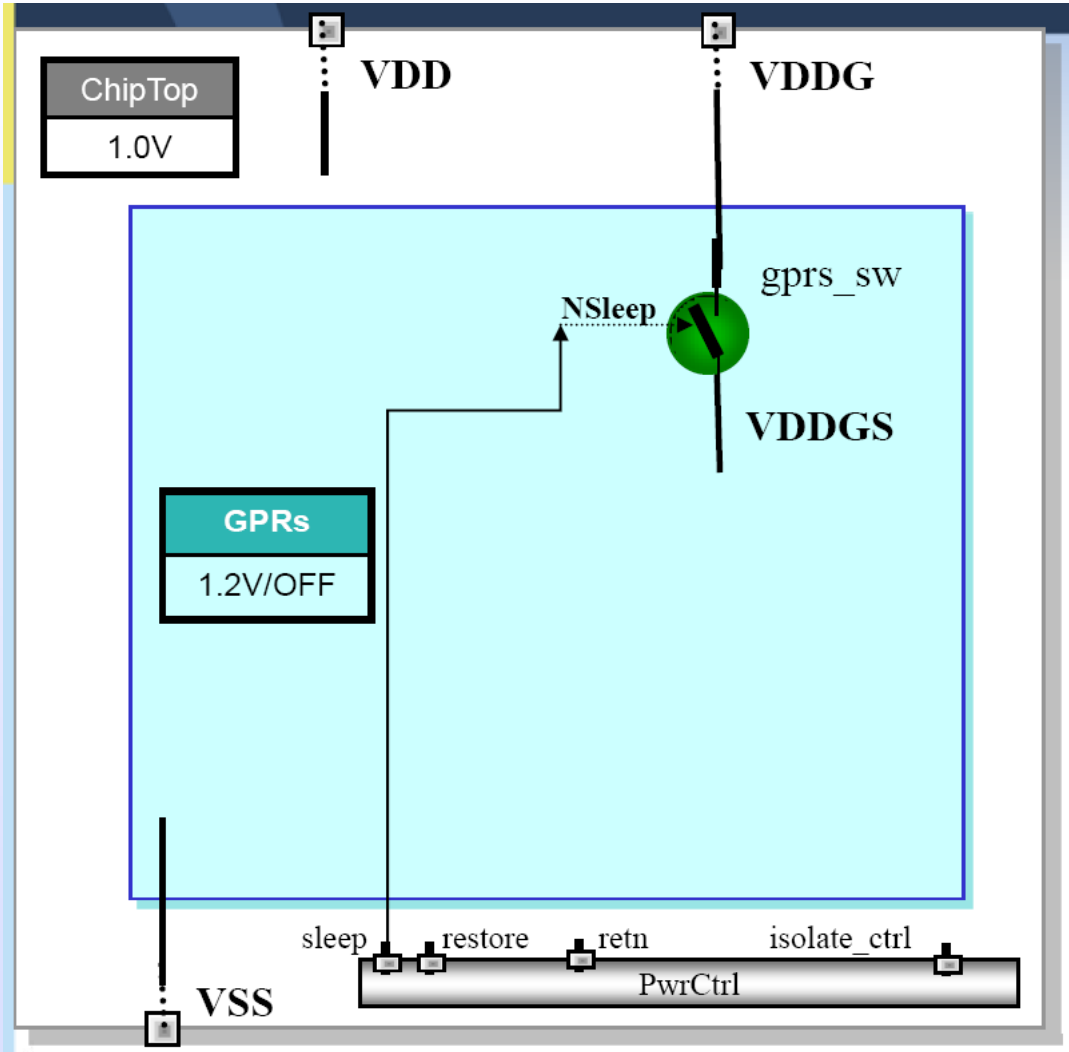
Dynamic Voltage and Frequency Scaling (DVFS): Power State



	Vdd1	Vdd2	Vdd3
PwrState1	0.8V	0.8V	0.8V
PwrState2	0.8V	0.9V	off

- Capture dynamic voltage scaling (DVS/DVFS) and shutdown scenarios with Power State Table (PST)
- UPF Commands
  - `add_port_state`
  - `create_pst`
  - `add_pst_state`

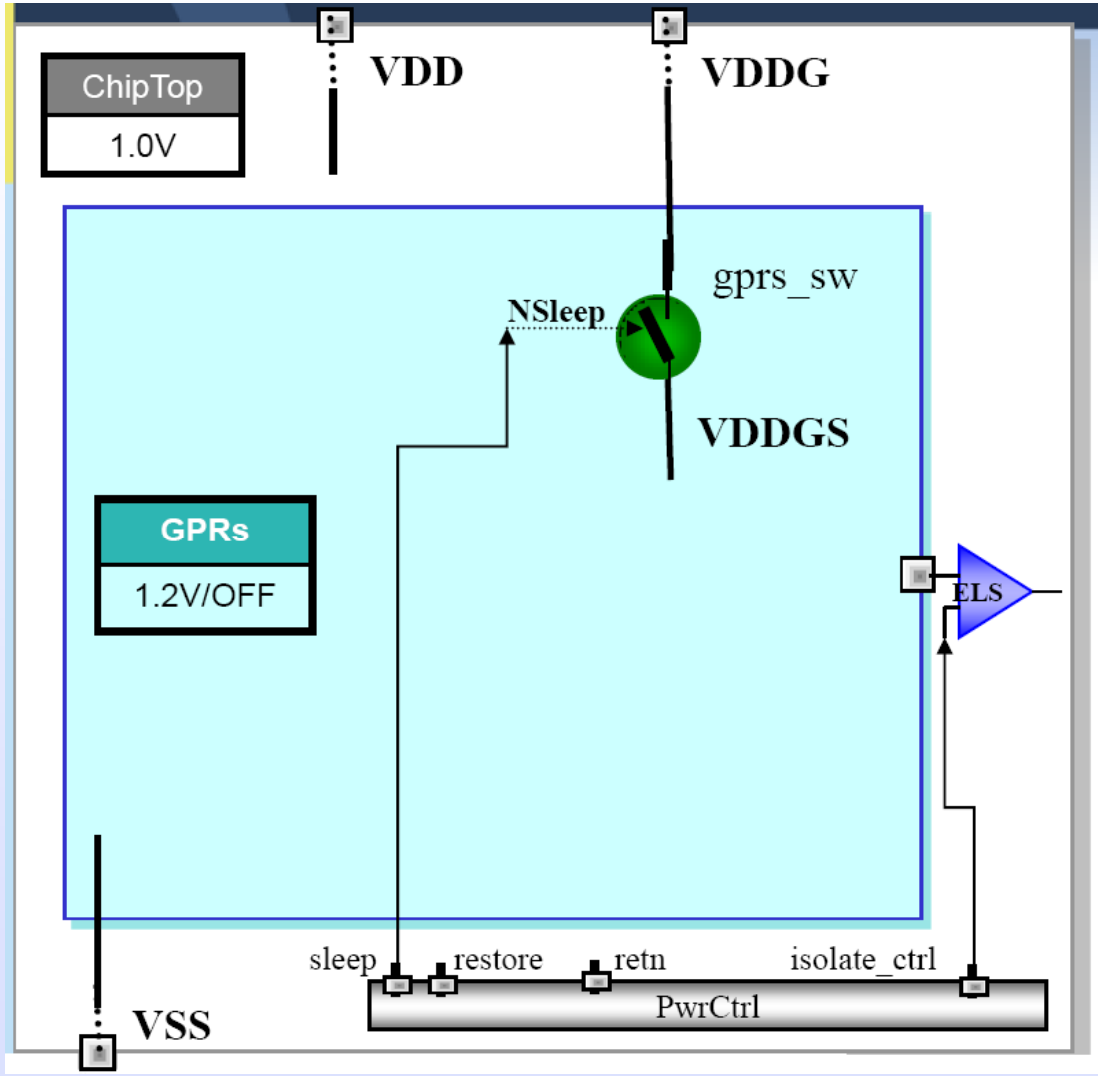
Power Switch



- Create power switch for GPRS

```
create_power_switch gprs_sw
 -domain GPRS
 -input_supply_port {in
VDDG} -output_supply_port
 {out VDDGS} -control_port
 {sleep PwrCtrl/sleep}
 -on_state {state2002 in
 {!sleep}}
```

Isolation Strategy

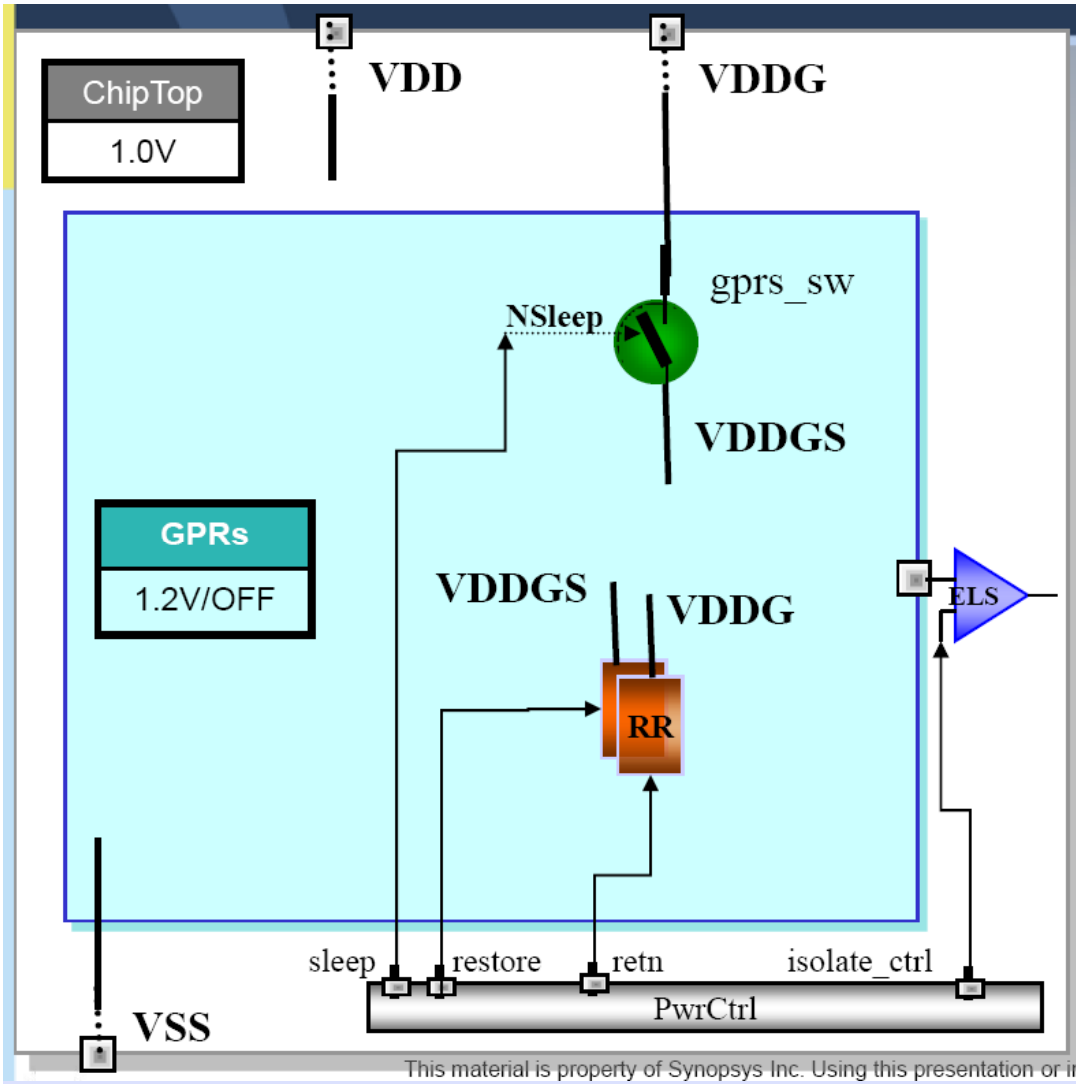


➢Isolation strategy for GPRS

```
set_isolation
gprs_iso_out -domain GPRS
-isolation_power_net VDD
-isolation_ground_net VSS
-clamp_value 1 -
applies_to outputs
```

```
set_isolation_control
gprs_iso_out -domain GPRS
-isolation_signal
PwrCtrl/isolate_ctrl
-isolation_sense low
-location parent
```

Retention Register Strategy



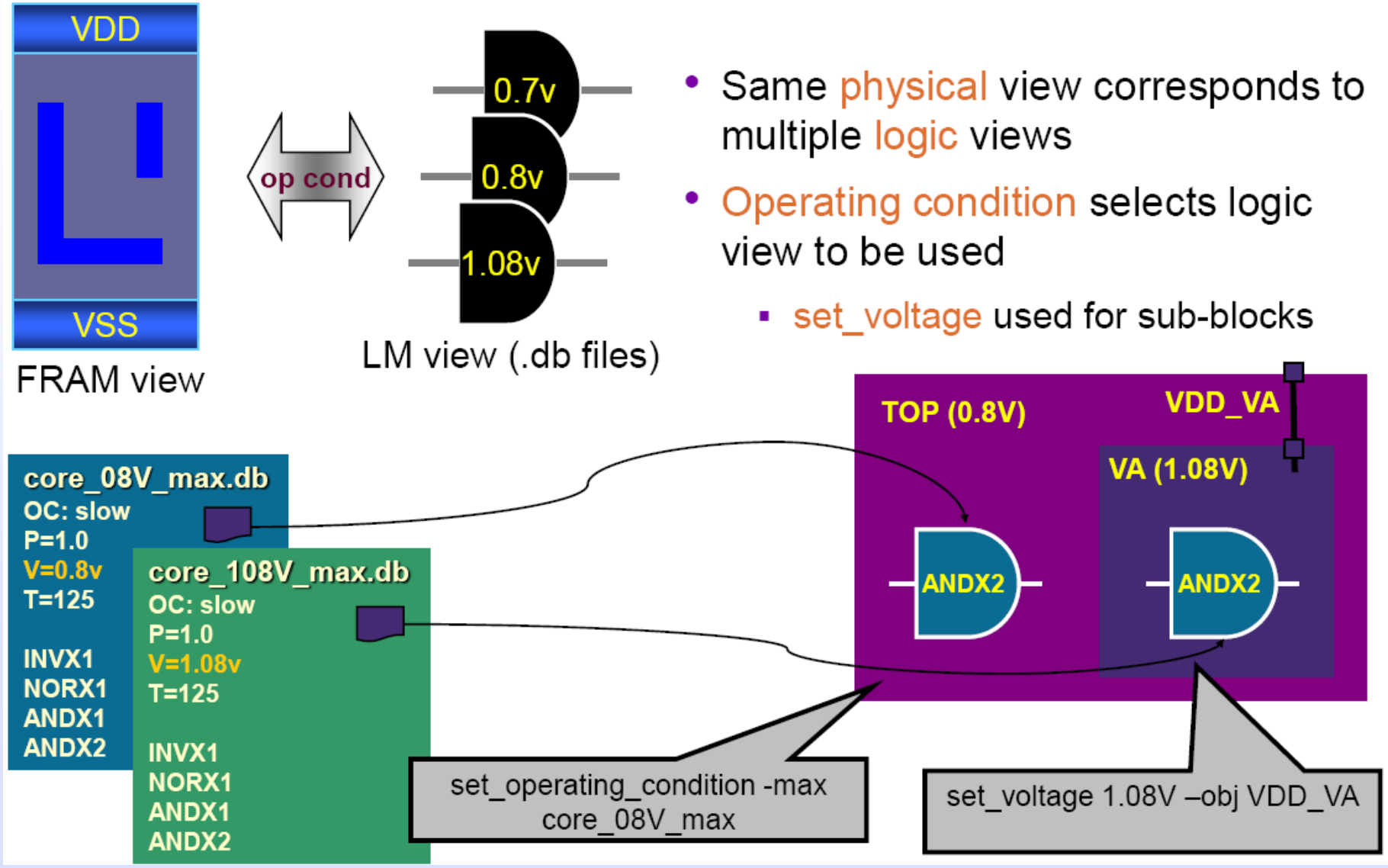
➢Retention strategy for GPRS

```
set_retention gprs_ret
-domain GPRS
-retention_power_net VDDG
-retention_ground_net VSS

set_retention_control
gprs_ret -domain GPRS
-save_signal
{PwrCtrl/retn high} -
restore_signal
{PwrCtrl/restore high}

map_retention_cell
gprs_ret -domain GPRS
-lib_cell_type RSDFCD1
```

Library Support -Multi-NLDM



Non-Linear Voltage/Temperature Scaling

- Dynamic and adaptive voltage scaling require modeling for multiple voltage and temperature operating points
- NLDM modeling requires multiple libraries
  - Power calculations scaled and interpolated between different PVT points
- CCS models eliminate need to have separate libraries for each incremental voltage and temperature