

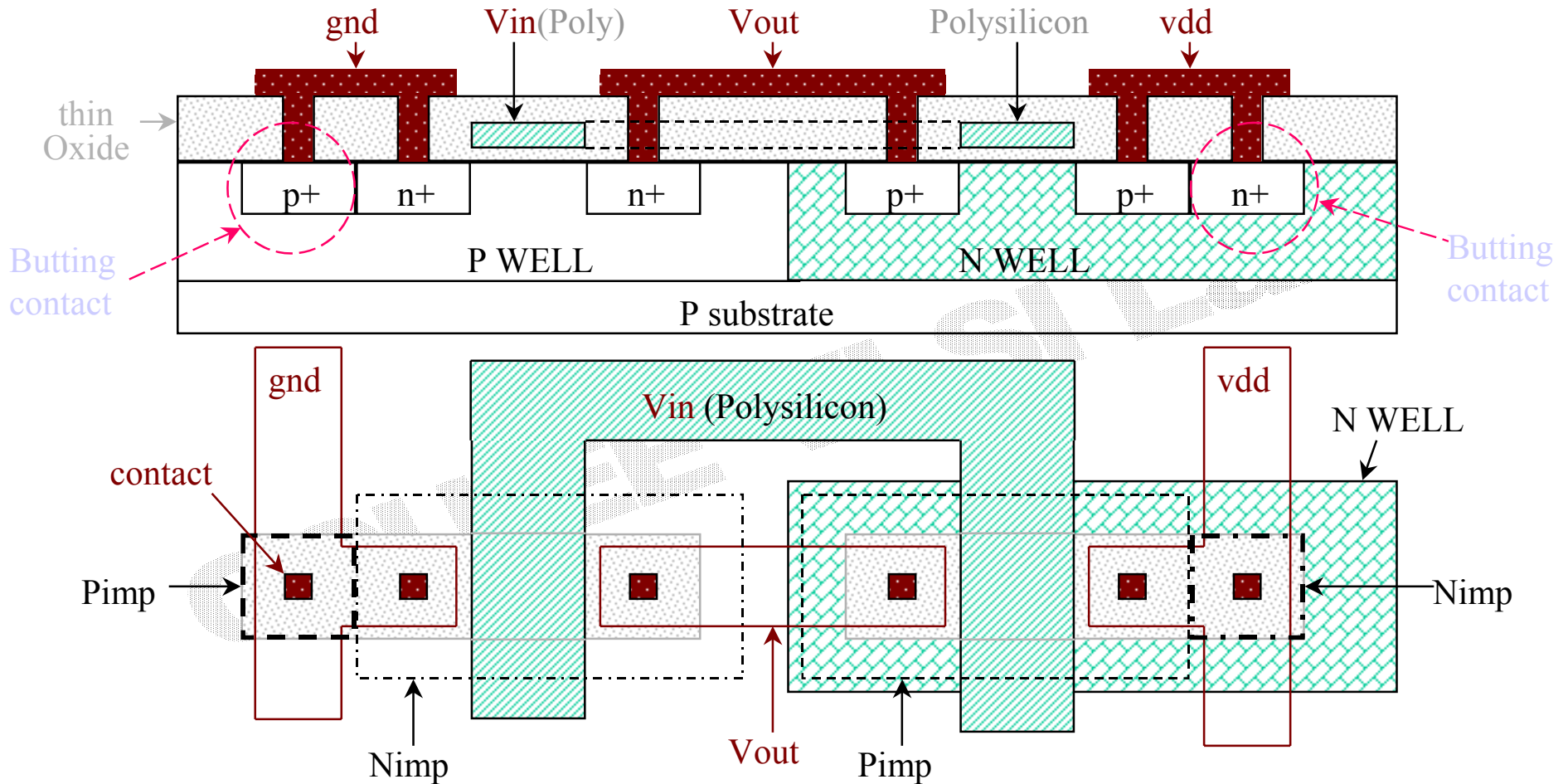


Layout Design and Verifications

- **Cross Section & Layout View**
- **Layout (Design) Rules**
- **Cell Butting Rules**
- **Edit Layout**
- **Verifications (DRC/LVS)**
- **Create Abstract**



Cross Section & Layout View



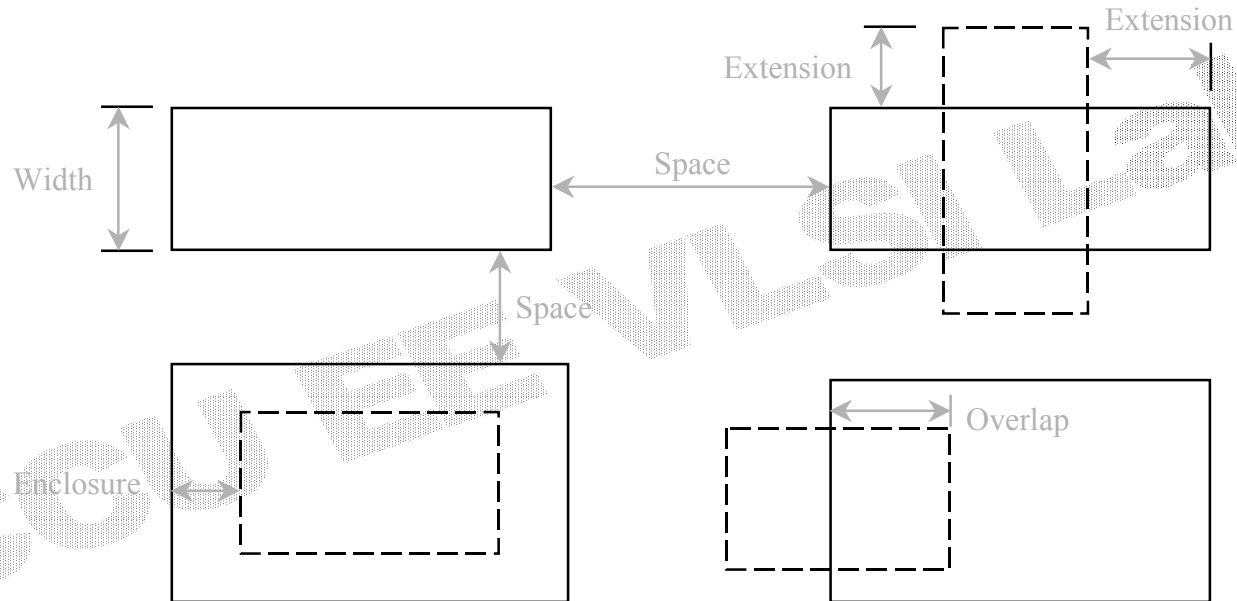
CMOS 的反相器的橫截面圖與佈局(layout)圖





Definition For Parameters Of Layout Rules

基本定義 (Definition)

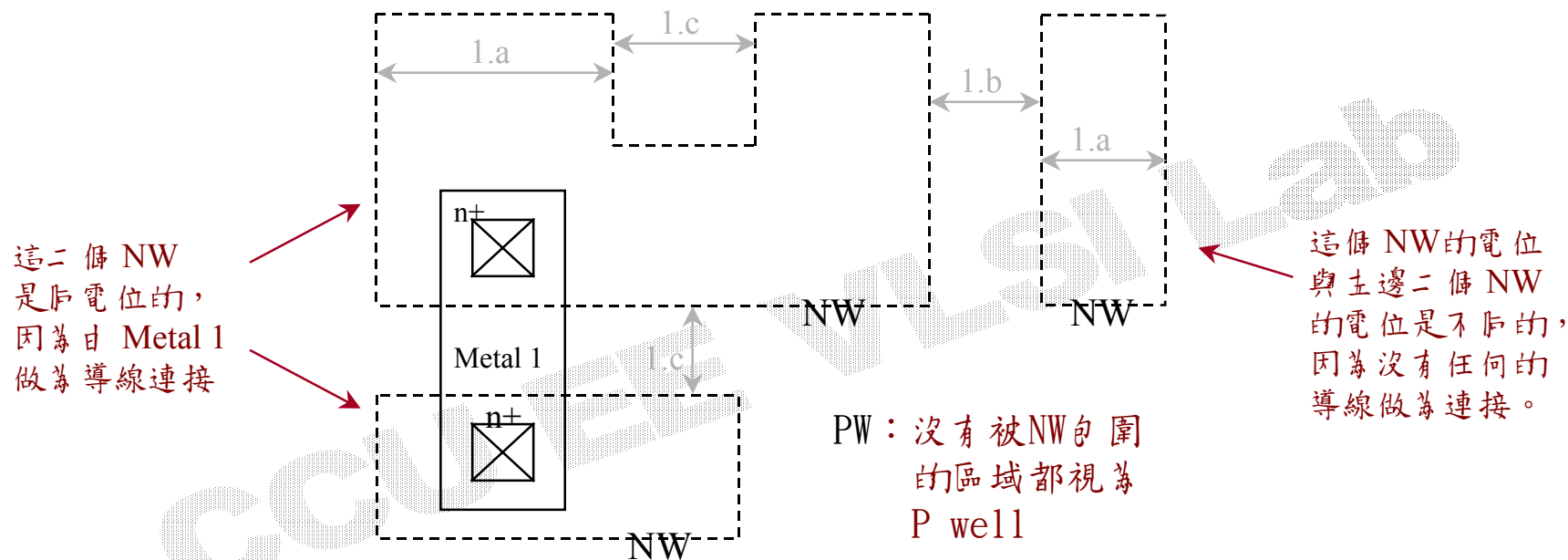


1. 請記住這些名稱的定義
2. 接下來所介紹的 layout rules 必須熟記在心，在劃 layout 時務必遵守這些規則。



Layout (Design) Rules (I)

1. NW (N well)



Rule No.	Rule Description	T-0.6 SPTM
1.a	minimum width NW	3.0
1.b	minimum space NW -to- NW with different potentials	4.8
1.c	minimum space NW -to- NW with the same potentials	1.5

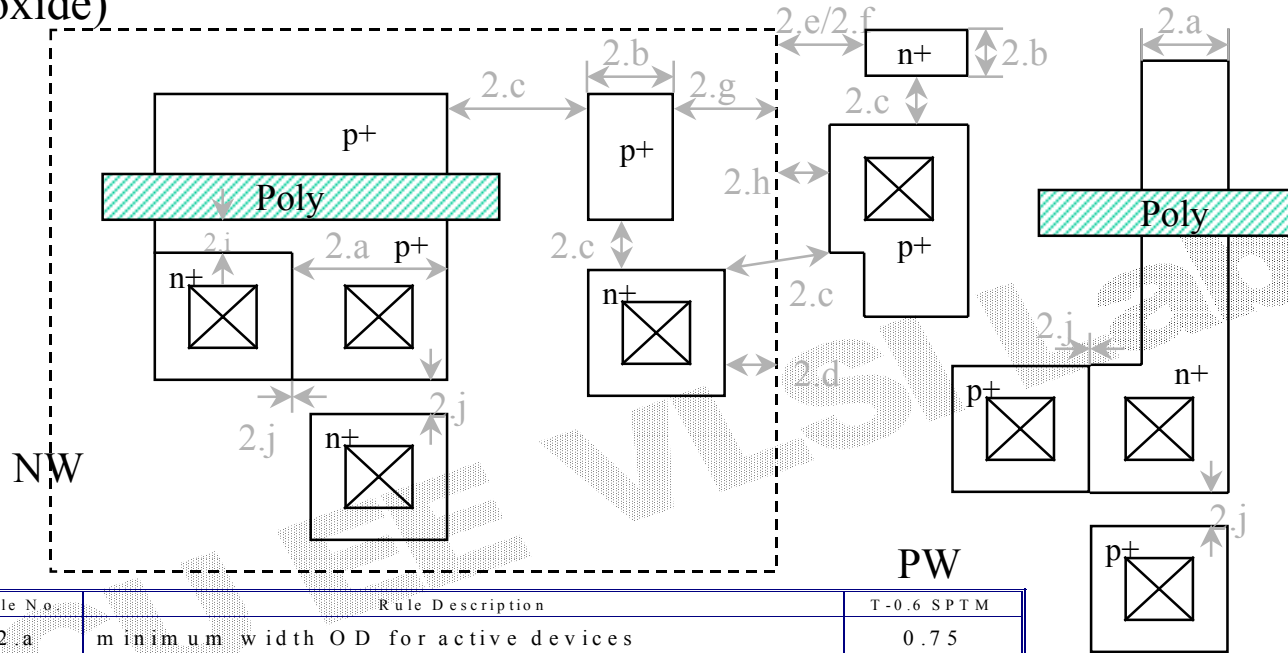
單位為 μm





Layout (Design) Rules (II)

2. OD (thin oxide)



Rule No.	Rule Description	T-0.6 SPTM
2.a	minimum width OD for active devices	0.75
2.b	minimum width OD for interconnection	0.6
2.c	minimum space OD-to-OD	1.2
2.d	minimum enclosure NW [OD (n+)]	0.4
2.e	minimum space NW (cold)-to-OD (n+)	1.8
2.f	minimum space NW (hot)-to-OD (n+)	4.0
2.g	minimum enclosure NW [OD (p+)]	1.8
2.h	minimum space NW-to-OD (p+)	0.4
2.i	minimum space PO-to-OD (on active region)	0.75
2.j	minimum space OD (p+)-to-OD (n+)	0.0 or 1.2

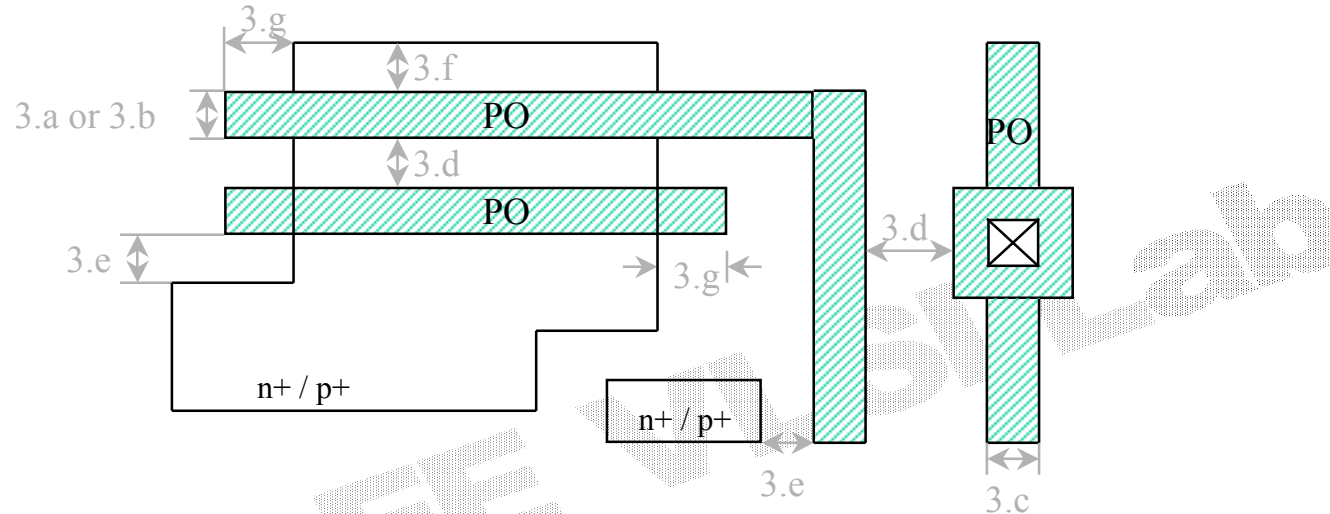
單位為 um





Layout (Design) Rules (III)

3. PO (Poly)



Rule No.	Rule Description	T-0.6 SPTM
3.a	minimum width PO for PMOS	0.6
3.b	minimum width PO for NMOS	0.6
3.c	minimum width PO for interconnection	0.6
3.d	minimum space PO-to-PO	0.75
3.e	minimum space PO-to-OD(on field)	0.3
3.f	minimum extension OD-over-PO	0.8
3.g	minimum extension PO-over-OD	0.6

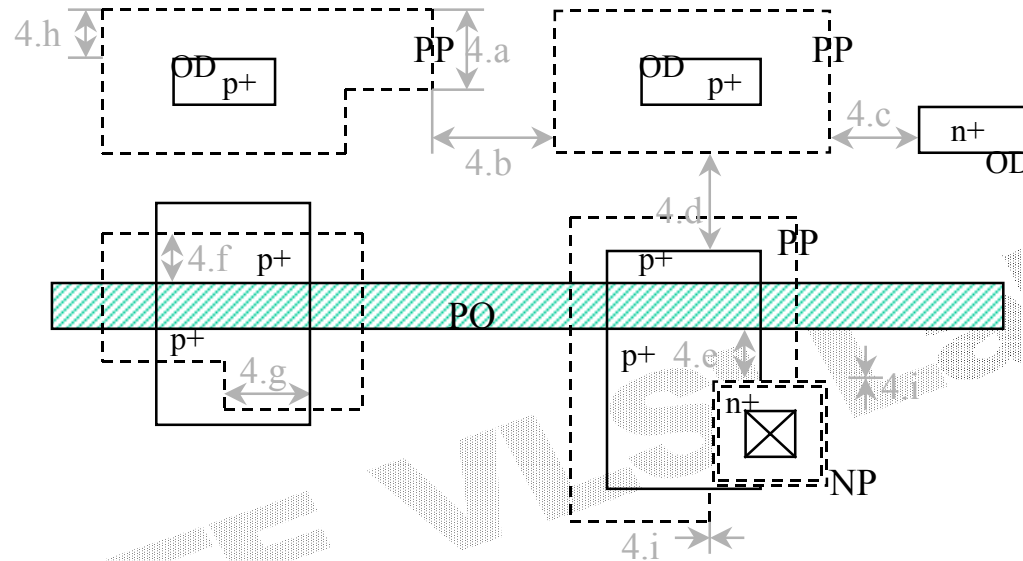
單位為 um





Layout (Design) Rules (IV)

4. PP(P implantation) NP(N implantation)



Rule No.	Rule Description	T-0.6 SPTM
4.a	minimum width PP(4.* also apply for NP)	0.9
4.b	minimum space PP-to-PP(merge if less)	0.9
4.c	minimum space PP-to-OD(n+ , hot)	0.75
4.d	minimum space PP-to-OD	0.75
4.e	minimum space NP-to-PO(on active region)	0.75
4.f	minimum extension PP-over-PO(to form S/D)	0.75
4.g	minimum overlap PP-over-OD	0.45
4.h	minimum enclosure PP[OD(p+)]	-
4.i	minimum enclosure PP[CO(butting)]	0.0

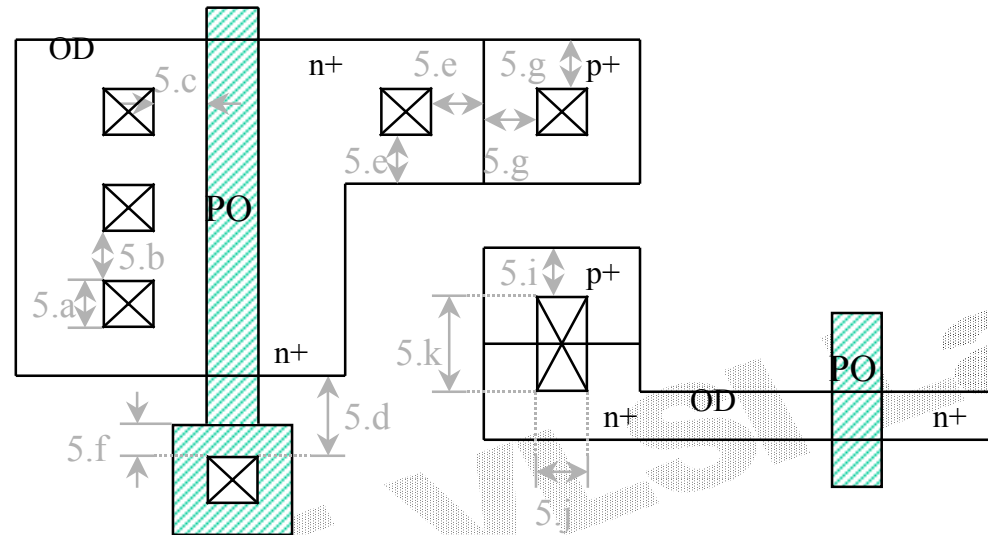
單位為 um





Layout (Design) Rules (V)

5. CO (contact)



Rule No.	Rule Description	T-0.6 SPTM
5.a	minimum width CO	0.6
5.b	minimum space CO-to-CO	0.6
5.c	minimum space CO-to-PO	0.6
5.d	minimum space CO-to-OD	0.6
5.e	minimum enclosure OD [CO]	0.35
5.f	minimum enclosure PO [CO]	0.4
5.g	minimum enclosure PP/NP [CO]	0.4
5.h	CO on gate region is not allowed.	-
5.i	minimum enclosure PP/NP [CO (butting)]	0.4
5.j	minimum width CO (butting)	0.6
5.k	minimum length CO (butting)	1.2

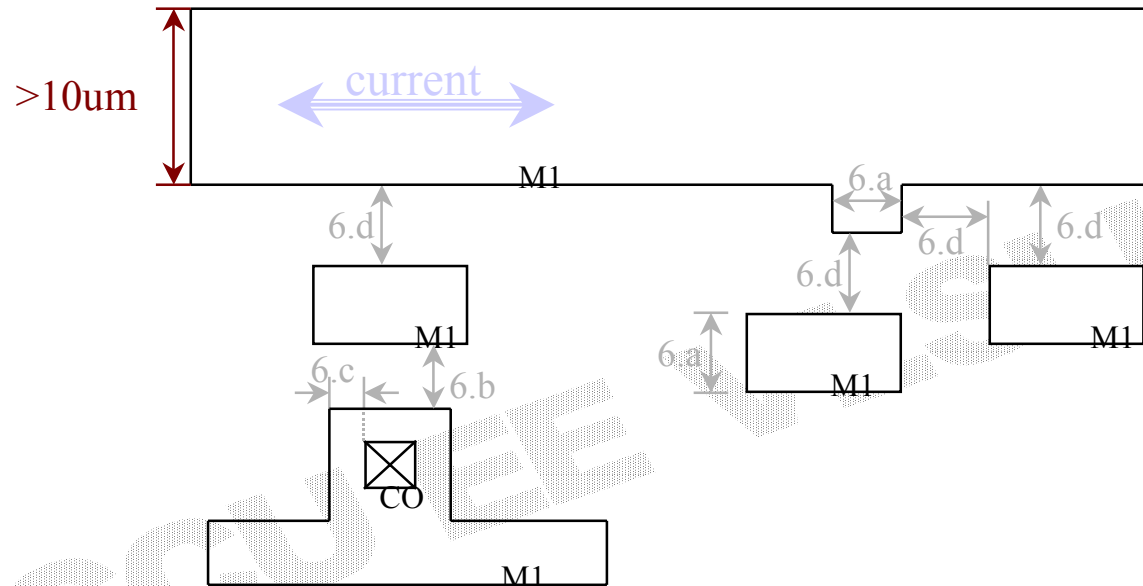
單位為 um





Layout (Design) Rules (VI)

6. M1 (Metal 1)



Rule No.	Rule Description	T-0.6 SPTM
6.a	minimum width M1	0.9
6.b	minimum space M1-to-M1	0.8
6.c	minimum enclosure M1[CO]	0.3
6.d	minimum space M1-to-M1(>10um)	1.3

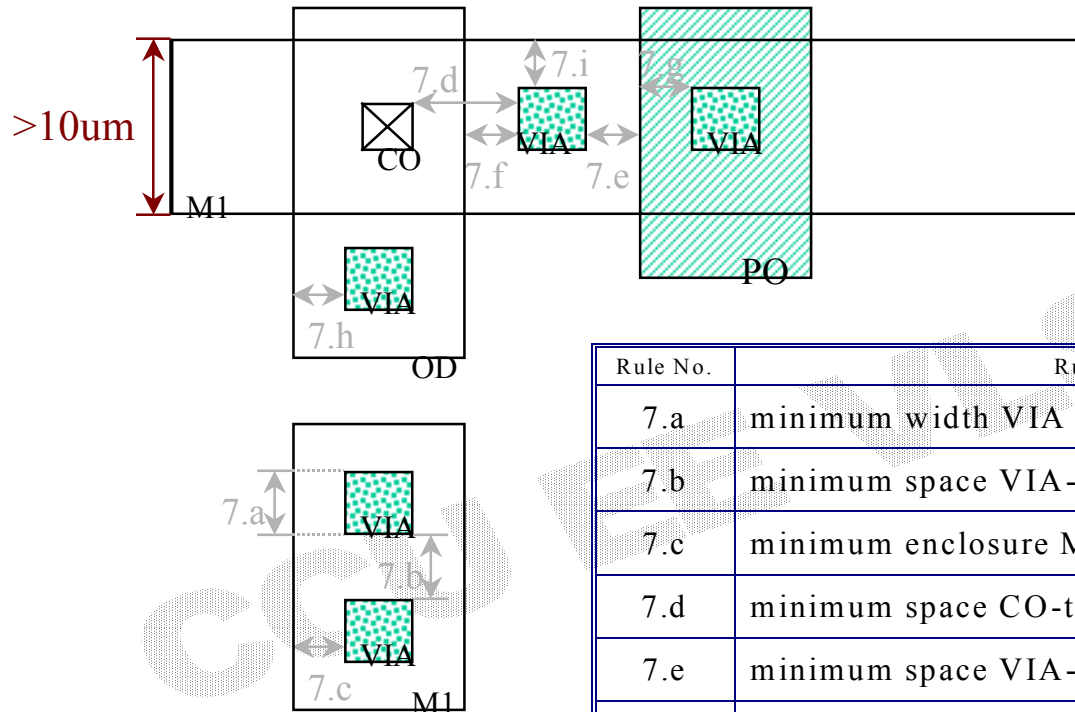
單位為 um





Layout (Design) Rules (VII)

7. VIA (VIA 1)



單位為 μm

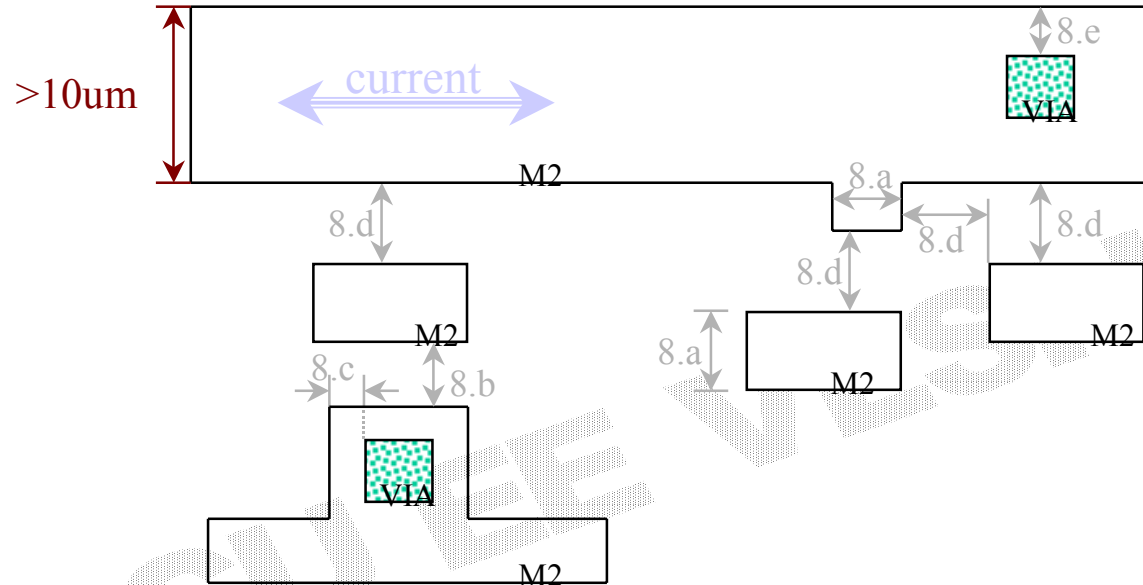
Rule No.	Rule Description	T-0.6 SPTM
7.a	minimum width VIA	0.7
7.b	minimum space VIA-to-VIA	0.7
7.c	minimum enclosure M1[VIA]	0.4
7.d	minimum space CO-to-VIA	0.0
7.e	minimum space VIA-to-PO	0.0
7.f	minimum space VIA-to-OD	0.0
7.g	minimum enclosure PO[VIA]	0.0
7.h	minimum enclosure OD[VIA]	0.0
7.i	minimum enclosure M1($>10\mu\text{m}$)[VIA]	1.5





Layout (Design) Rules (VIII)

8. M2 (Metal 2)



Rule No.	Rule Description	T-0.6 SPTM
8.a	minimum width M2	0.9
8.b	minimum space M2-to-M2	0.8
8.c	minimum enclosure M2[VIA]	0.4
8.d	minimum space M2-to-M2(>10um)	1.3
8.e	minimum enclosure M2(>10um)[VIA]	1.5

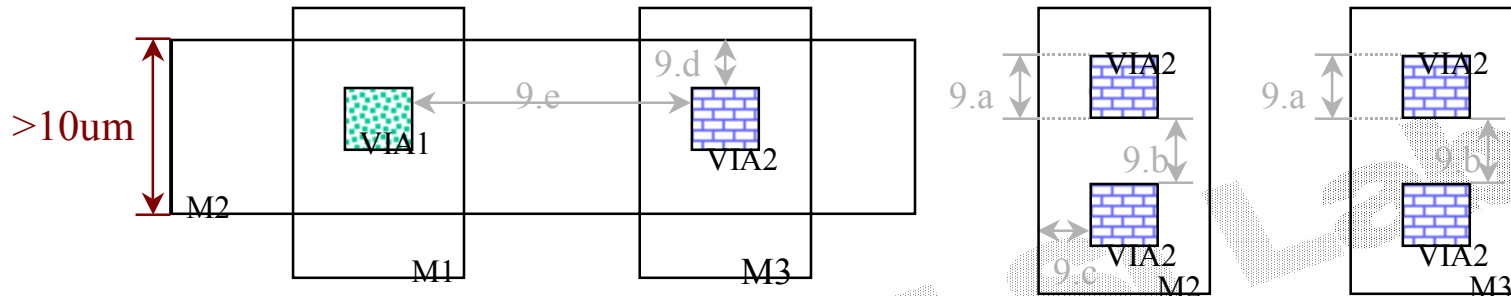
單位為 um





Layout (Design) Rules (IX)

9. VIA 2



Rule No.	Rule Description	T-0.6 SPTM
9.a	minimum width VIA2	0.7
9.b	minimum space VIA2-to-VIA2	0.7
9.c	minimum enclosure M2[VIA2]	0.4
9.d	minimum enclosure M2(>10um)[VIA2]	1.5
9.e	minimum space VIA1-to-VIA2	0.6

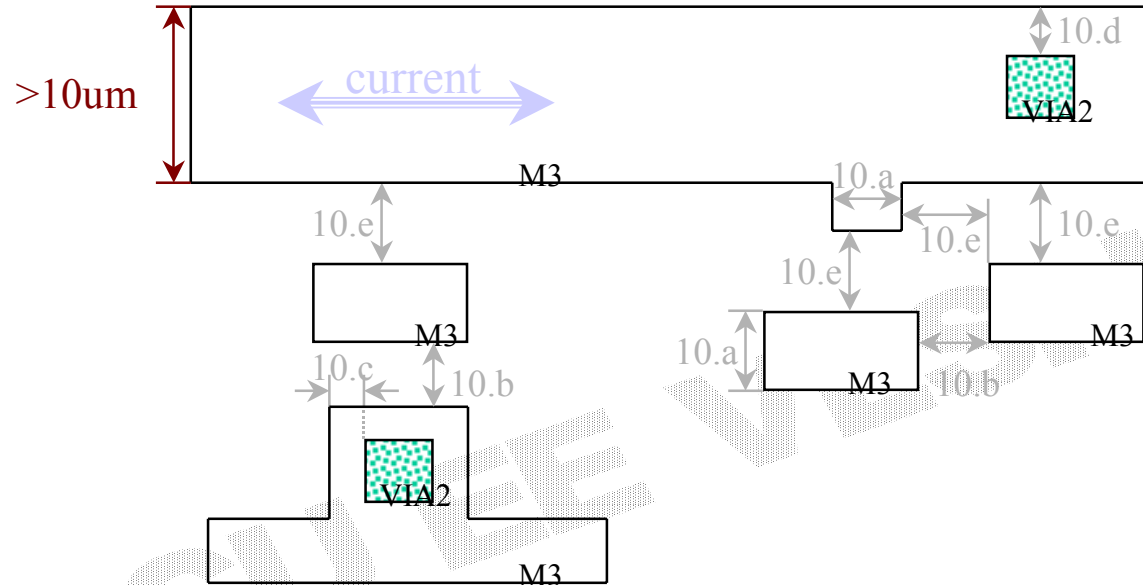
單位為 um





Layout (Design) Rules (X)

10. M3 (Metal 3)



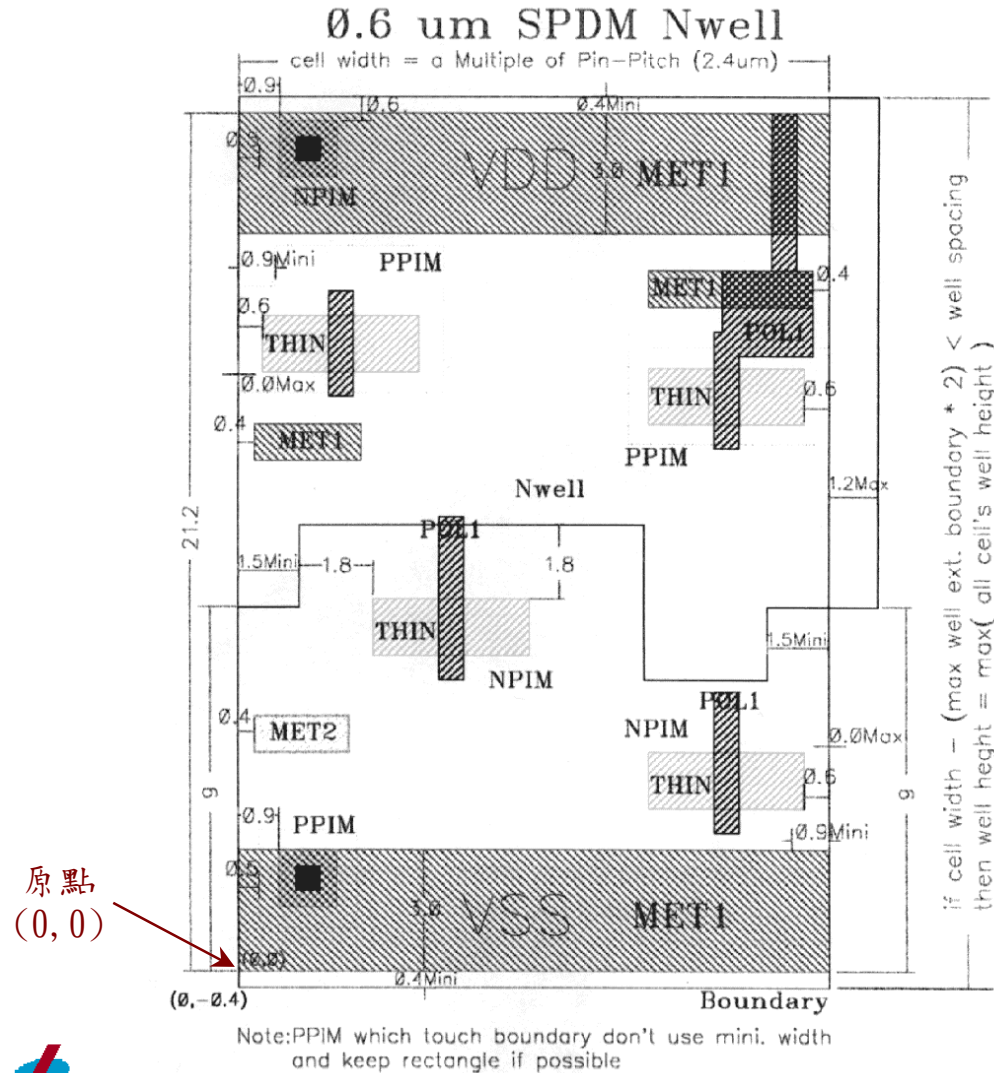
Rule No.	Rule Description	T-0.6 SPTM
10.a	minimum width M3	0.9
10.b	minimum space M3-to-M3	0.8
10.c	minimum enclosure M3[VIA2]	0.4
10.d	minimum enclosure M3($>10\mu\text{m}$)[VIA2]	1.5
10.e	minimum space M3-to-M3($>10\mu\text{m}$)	1.3

單位為 μm





Cell Butting Rules (A)

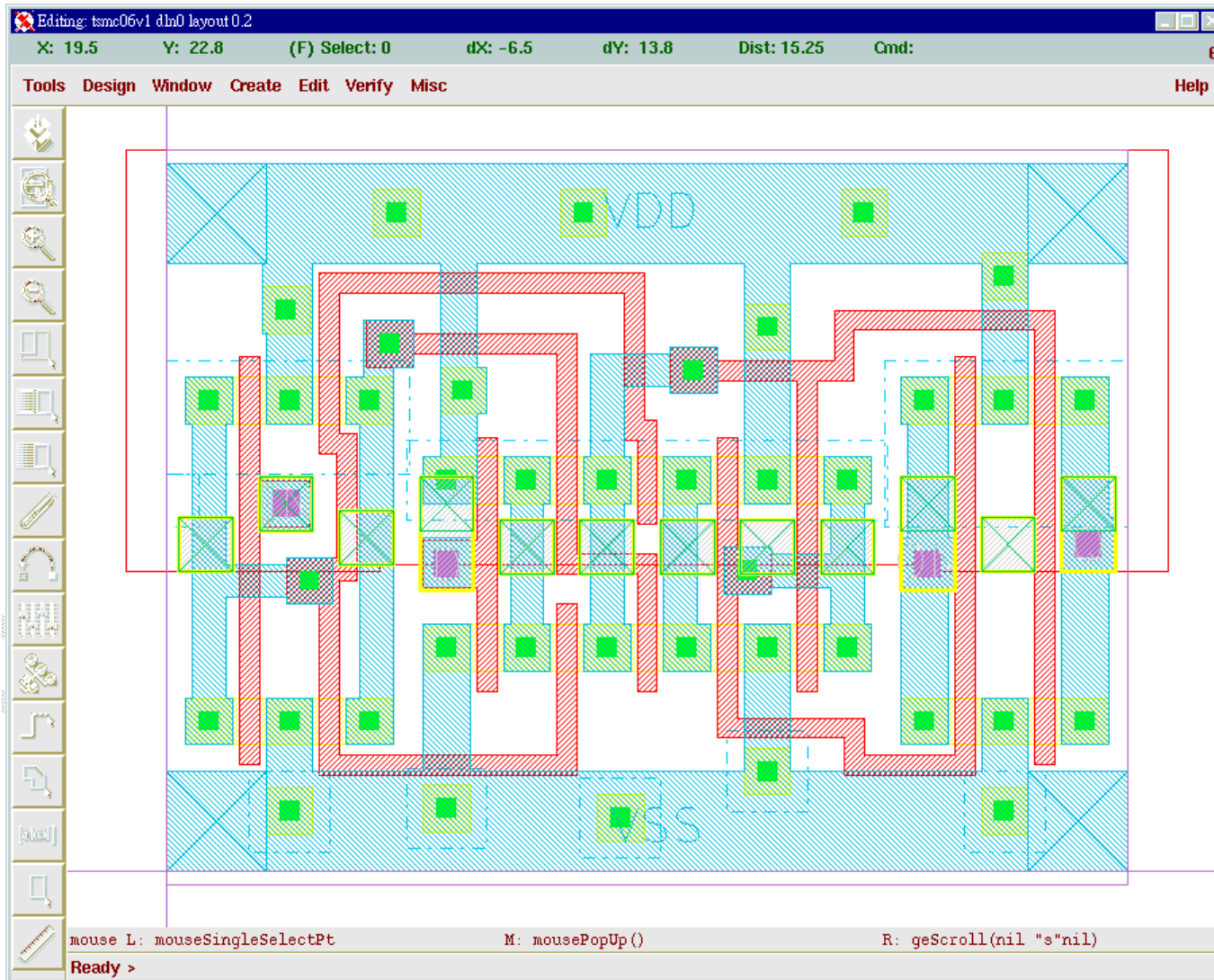


- ⇒主圖為使用 0.6um Single Poly Double Metal 製程之每一個 Standard Cell 都必須遵守 CMOS 第一種的共片規則例子。主要的用意是在使任意的兩個 Cell 在做連接後，都還能符合 Design Rule。
- ⇒一般高度都是固定的，而寬度以 pitch(2.4um) 為單位，依照 Cell 電晶體數目的不同，寬度的大小就不同，但都必須是 pitch 的倍數。
- ⇒而一般“單位 pitch”就是指兩個 pin 中心點相互間最小的距離。
- ⇒接地線(VSS/Metal 1)的主下座為原點須放在 layout 圖上游標所指的原點(0,0)。
- ⇒VDD與VSS須使用 Metal 1 做為連線且位置及高度都是固定的。(exp. , 21.2um)
- ⇒其餘的數字如 0.9 或 0.9Mini 意思是寬度至少大於 0.9um，而 1.2Max 意思是寬度不可以超過 1.2um。



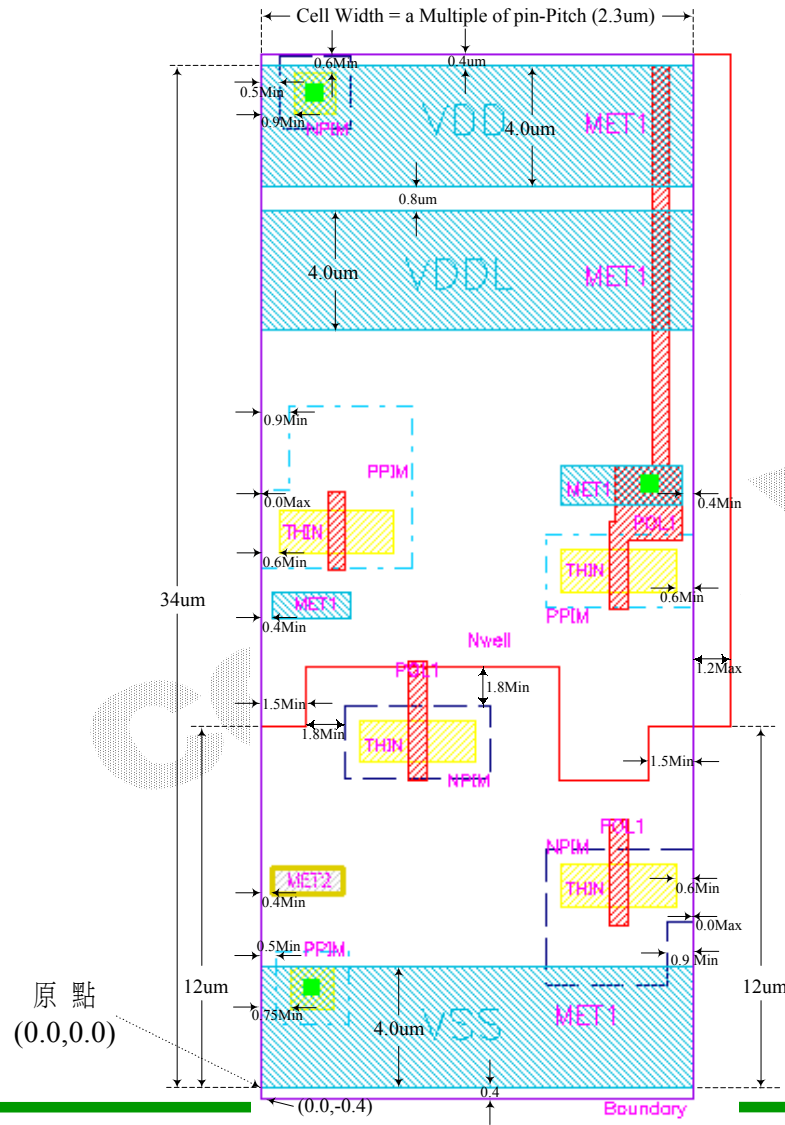


Example Using Cell Butting Rules (A)





Cell Butting Rules (B)

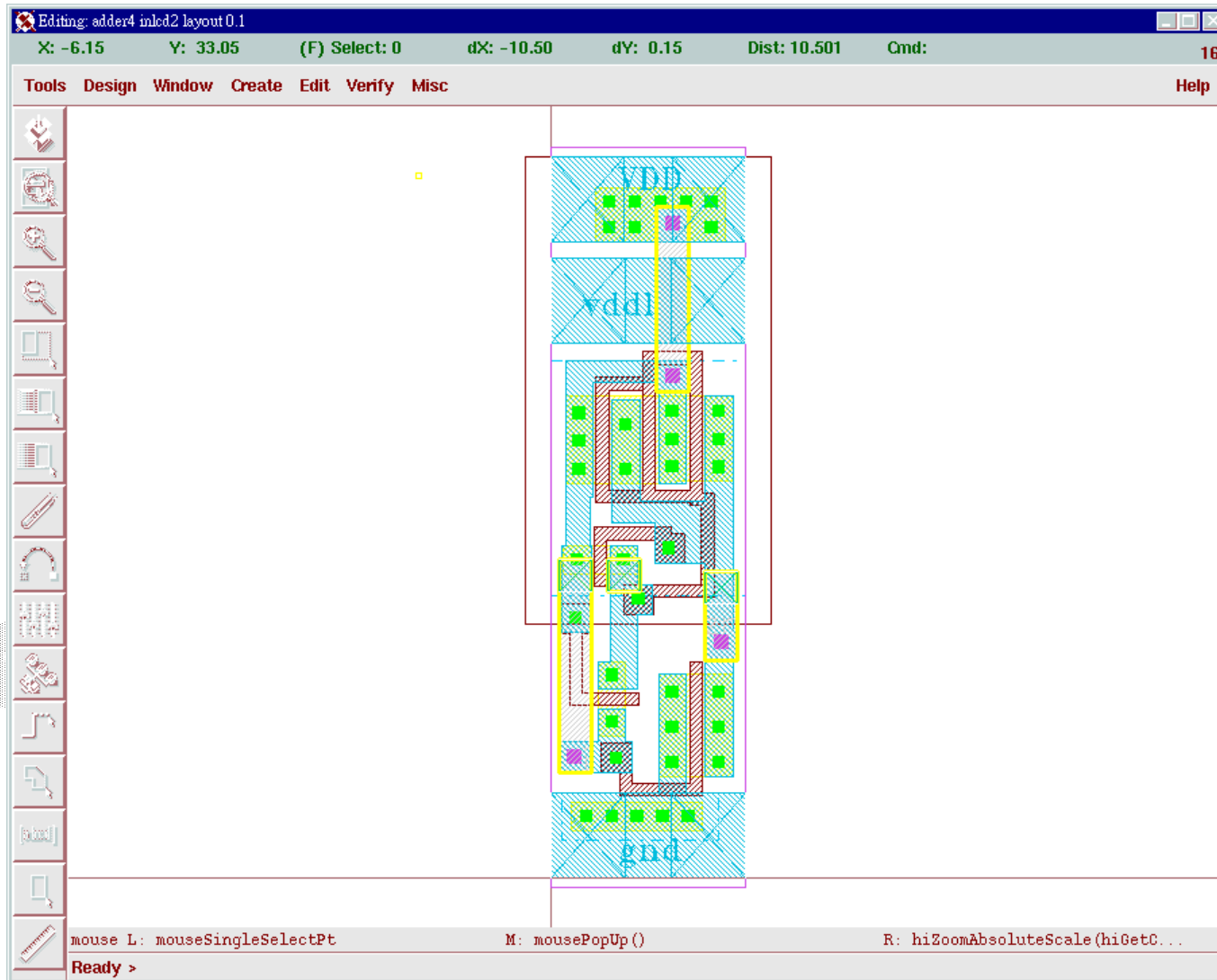


- ⇒主圖為使用 0.6um Single Poly Double Metal 製程之每一個 Standard Cell 都必須遵守 CMOS 第二種的共化規則例子。主要的用意是在使任意的兩個 Cell 在做連接後，都還能符合 Design Rule。
- ⇒一般高度都是固定的，而寬度以 pitch(2.3um) 為單位，依照 Cell 電晶體數目的不同，寬度的大小就不同，但都必須是 pitch 的倍數。
- ⇒而一般“單位 pitch”就是指兩個 pin 中心點相互間最小的距離。
- ⇒接地線(VSS/Metal 1)的主下座為原點須放在 layout 圖上游標所指的原點(0,0)。
- ⇒VDD、VDDL與VSS須使用 Metal 1 做為連線且位置及高度都是固定的。(exp., 34um)
- ⇒其餘的數字如 0.9Min 意思是寬度至少大於 0.9um，而 1.2Max 意思是寬度不可以超過 1.2um。



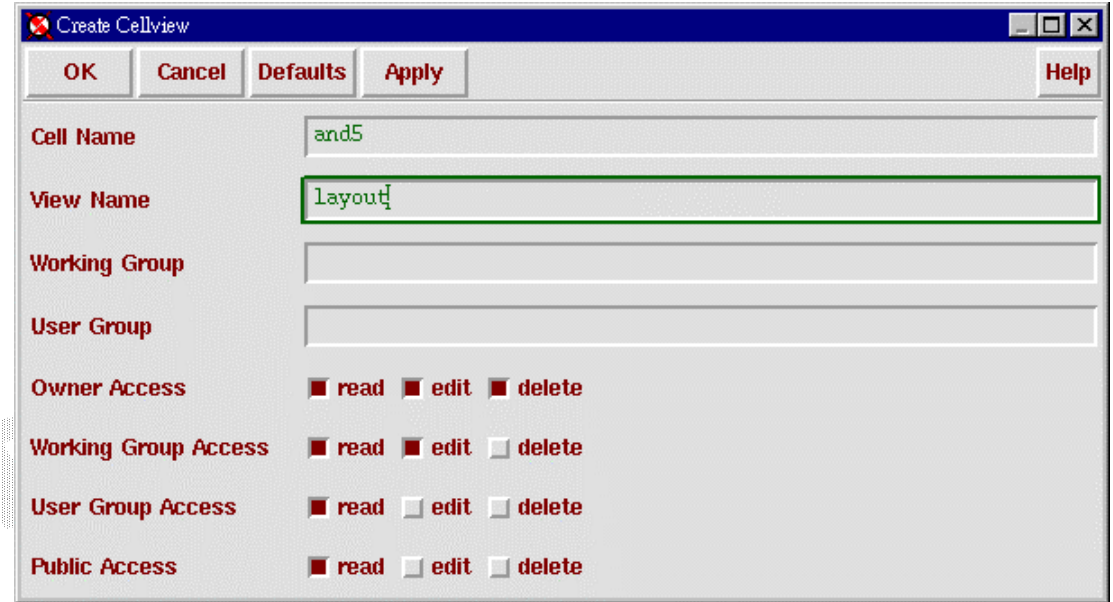
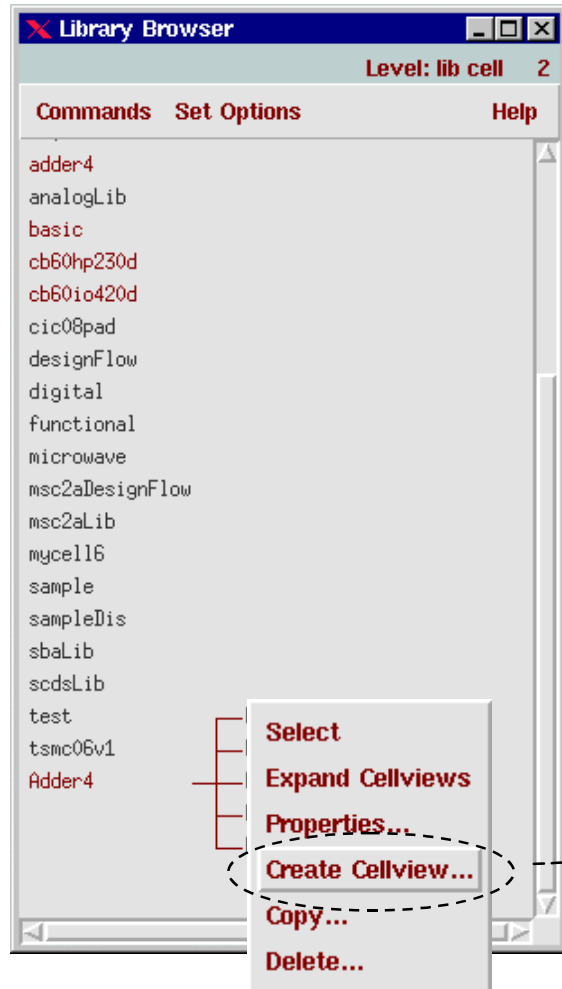


Example Using Cell Butting Rules (B)





Create Layout View



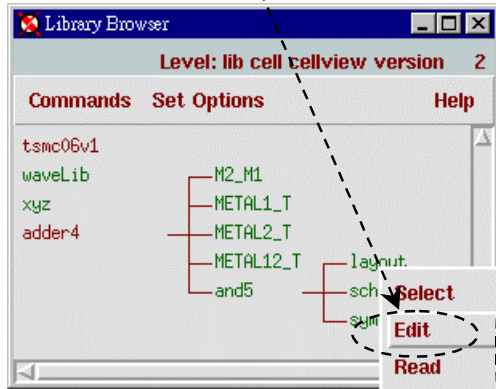
游標指到 Library Browser 的 Adder4-> and5
按滑鼠中鍵選擇 Create Cellview 並在
View Name 填入 layout，按 OK 即可。





Edit Layout

游標指到 Library Browser 的
Adder4-> and5 -> layout
按滑鼠中鍵選擇 Edit 即可開
出編輯視窗



Editing: adder4 and5 layout 0.0
X: 4,000 Y: 50,200 (F) Select: 0 (dX: dY) Dist: Cmd: 13
Tools Design Window Create Edit Verify Misc Help

與上一點的相對位置

目前的command

滑鼠的位置

放大縮小的快速圖示

這是 LSW (Layer Selection Window) 主要在配合 Edit 使用

設定可顯示於 CIW 上的層

設定 LSW 上所選層的顏色

目前選用的層

library name

設定 instance, pin 是否可編輯

除目前選用的層外其餘層皆不可選。

LSW 上所有層皆可選用

除目前選用的層外其餘層皆不會顯示出來

LSW 上所有層都會顯示出來

修改、移動及複製的快速圖示

這些是編輯時的快速圖示，也可以使用 hot key，在編輯時可以配合 Shift 做加選及 Ctrl 做少選。

量尺寸的快速圖示或按 k 鍵，而清除尺寸按 K 鍵。

mouse L: mouseSingleSelectPt M: mousePopUp()
Ready >





Compare Layers

```

Text Editor V3 [vlsi6] - test.tf, dir, /tmp_mnt/vlsi-b/ms84/vangjc
File View Edit Find








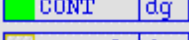


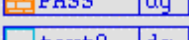
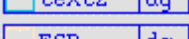
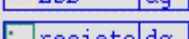






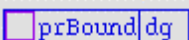

tfcDefinePurpose(
:( PurposeName Purpose# )
( warning 234 )
( tool1 235 )
( tool0 236 )
( label 237 )
( flight 238 )
( error 239 )
( annotate 240 )
( drawing1 241 )
( drawing2 242 )
( drawing3 243 )
( drawing4 244 )
( drawing5 245 )
( drawing6 246 )
( drawing7 247 )
( drawing8 248 )
( drawing9 249 )
( boundary 250 )
( pin 251 )
( drawing 252 )
( net 253 )
( cell 254 )
( all 255 )
)

tfcDefineLayer(
:( LayerName Purpose Layer# FillStyle Priority Vis Sel Blink Valid)
( text2 drawing 63 outline 18 t t nil t )
( NWELL drawing 2 outline 19 t t nil t )
( PWELL drawing 3 outline 20 t t nil nil )
( THIN drawing 4 outlineStipple 21 t t nil t )
( GPOLY drawing 13 outlineStipple 22 t t nil t )
( NDIFF drawing 8 outlineStipple 23 t t nil nil )
( PDIFF drawing 7 outlineStipple 24 t t nil nil )
( NPIMP drawing 6 outline 25 t t nil t )
( PPIMP drawing 5 outline 26 t t nil t )
( ESD drawing 30 outlineStipple 27 t t nil t )
( CONT drawing 15 solid 28 t t nil t )
( METAL1 drawing 16 outlineStipple 29 t t nil t )
( METAL1 net 16 outlineStipple 30 t t nil nil )
( METAL1 pin 16 outlineStipple 31 t t nil t )
( VIA1 drawing 17 solid 32 t t nil t )
( VIA1 net 17 solid 33 t t nil nil )
( METAL2 drawing 18 outlineStipple 34 t t nil t )
)

```

注意，在 Technology file 中所定義的每一個 Layer name 皆會對映一個 Layer number。有的 Layer name 會有 dg(drawing) 與 pn(pin) 兩種不同的屬性定義，主要的差別是 purpose 的定義不同，如 dg 是 252，而 pn 是 251。一般畫 Layout 是使用 dg 的，只有在宣告為 pin 腳時才使用 pn。

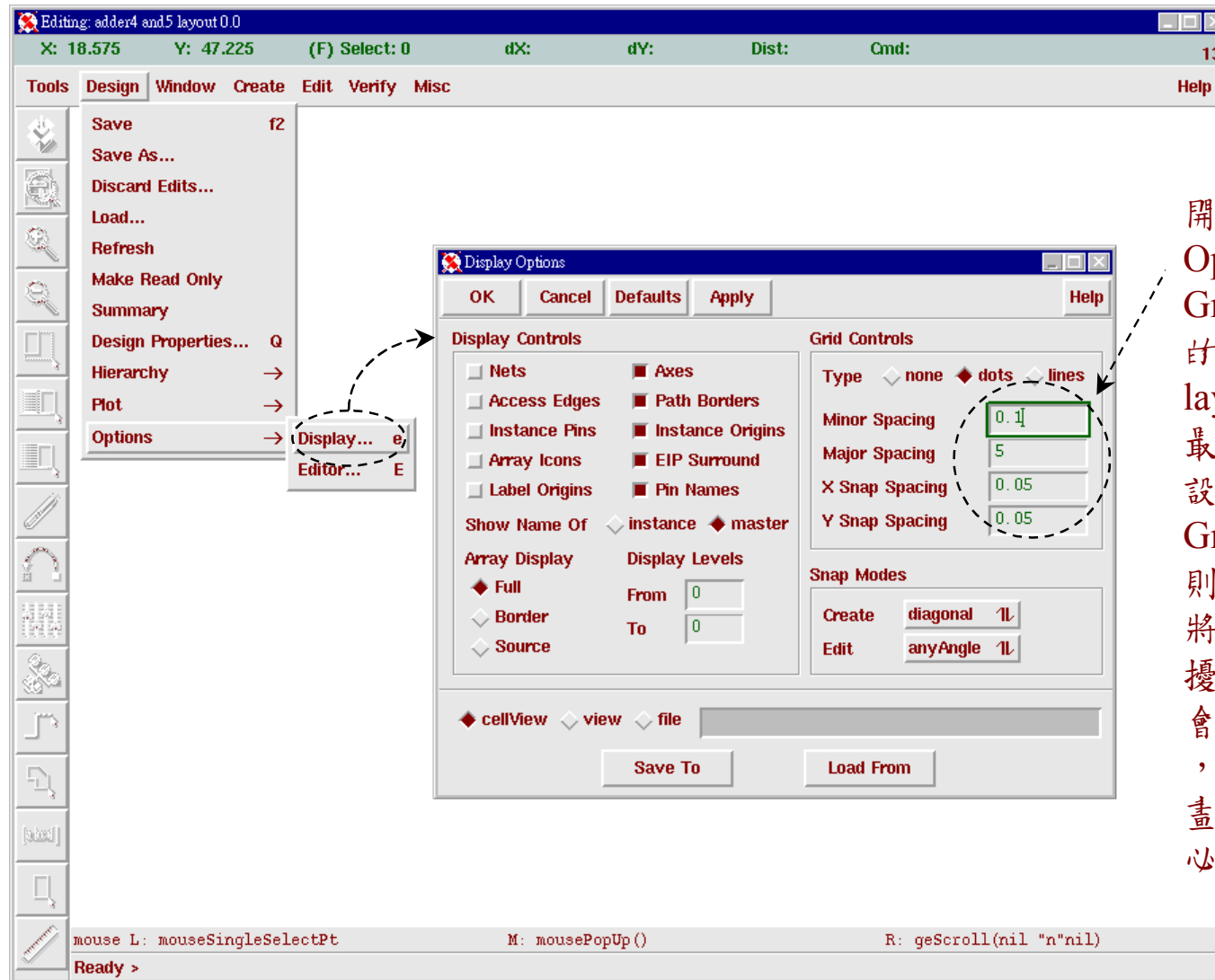
根據 Technology file 中所定義的 Layer name 與 Layout rule 中的 Layer name 之名稱對映。

 NWELL dg	NW (N Well)
 THIN dg	OD (thin oxide)
 PPIMP dg	PP (P implantation)
 NPIMP dg	NP (N implantation)
 GPOLY dg	PO (poly)
 METAL1 dg	M1 (metal 1)
 VIA1 dg	VIA (VIA 1)
 CONT dg	CO (contact)
 METAL2 dg	M2 (metal 2)
 backgro dg	
 PASS dg	
 text2 dg	
 ESD dg	
 resisto dg	
 PYGLBL dg	
 METAL2 pn	
 MT2LBL dg	
 METAL1 pn	
 GPOLY pn	
 MT1LBL dg	
 prBound dg	





Set Grid

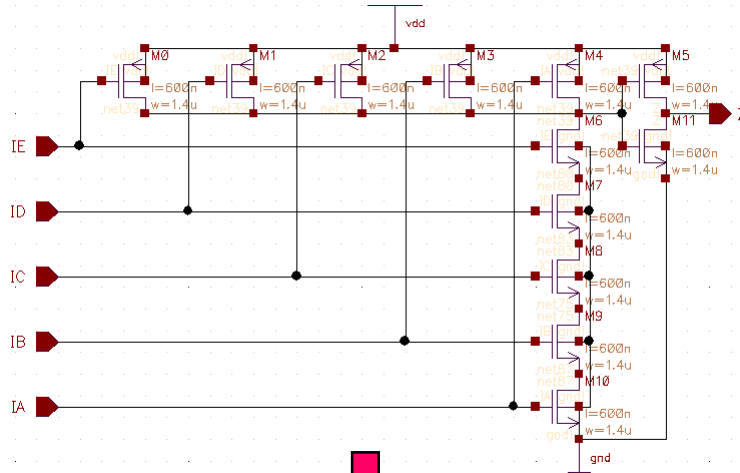


開啟Display Options 來設定 Grid。一般 Grid 的設法為所有 layout rules 裡的最小單位，在此設為 0.05。若是 Grid 沒有設好，則在畫 layout 時將會有很多的困擾，更嚴重可能會有 error 的情形，所以每次開始畫 layout 時請務必先做設定。

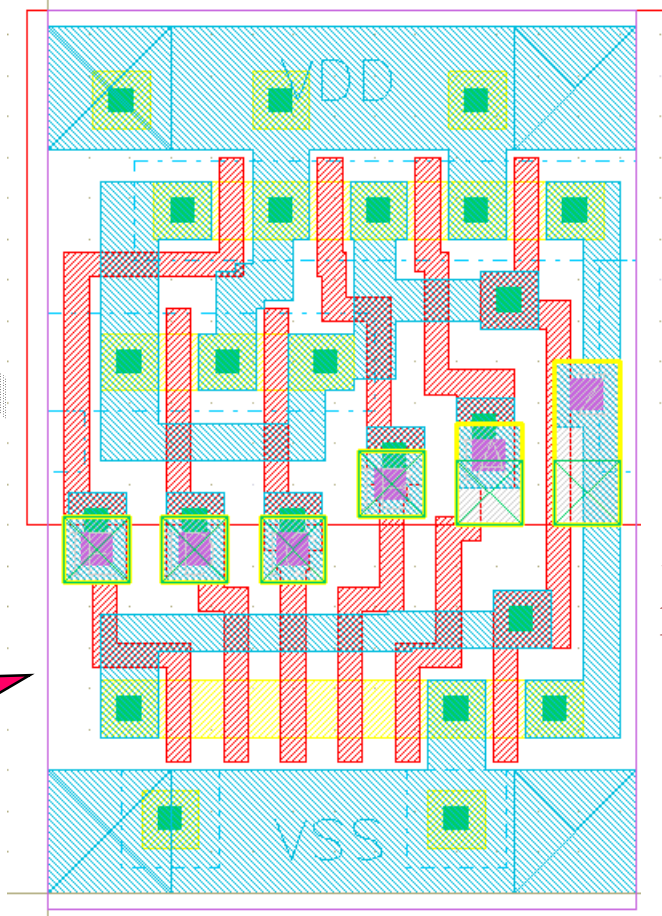
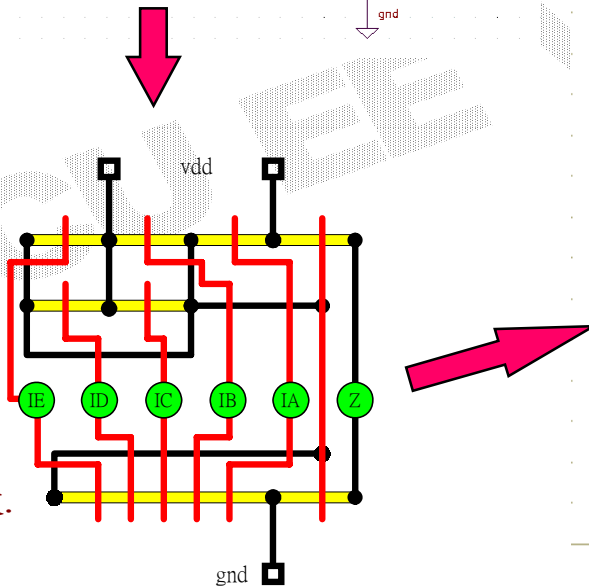




Start Layout



從一個 schematic 開始，設計到 layout，最好事先做好佈局的規劃，如右邊條形圖 (symbolic diagram)，先簡單粗略的擺設，使其能善用空間，做到使用最少的 pitch 數。

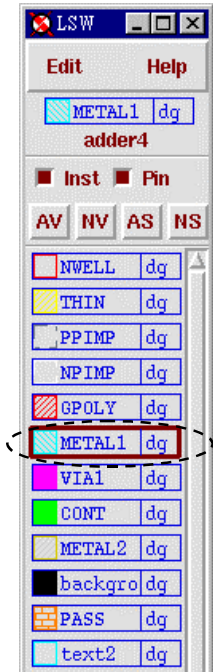


一個 pitch 最多只能存在一個輸出或輸入的 pin。此為“and5”，共有 6 個輸出入 pin，而 layout 的結果也只用 6 個 pitch 數，所以最省空間。





Practice Layout (I)



Editing: adder4 and5 layout0.1
X: 22.4 Y: 4.9 (F) Select: 1 dX: 0.9 dY: 4.0 Dist: 4.10 Cmd: Chop 11

Tools Design Window Create Edit Verify Misc Help

- 先至 LSW 中選好要畫的層，在此假設 METAL 1 接著按 r 鍵並配合 mouse 的主鍵 click 做為起點，而拖曳 mouse 即可劃出一個如主圖的矩形。
- 再到 LSW 中選擇 GPOLY 後用 r 方式，用 mouse 就可以再畫出一個主圖矩形的 polysilicon。
- 按 u 鍵可以取消前一個動作，而按 ESC 鍵則取消目前的這個命令；每次更換命令最好按 ESC。
- stretch: 先用 mouse 輕點 METAL 1 矩形的某一邊，之後按 s 鍵並配合 mouse 即可改變矩形的尺寸。
- move: 任意選擇所要搬移的目標，之後按 m 鍵並配合 mouse 即可。
- chop: 任意選擇所要分割的矩形，之後按 shift + c 鍵，再利用 mouse 來剪開矩形。
- merge: 只限於相同的層任意框選所要結合的矩形，或利用 shift 來加選，等確定後按 shift + m 即可。
- 按 k 鍵配合 mouse 可以畫出 R 規線，而按 shift + k 鍵則清除 R 規線。

目前命令的說明

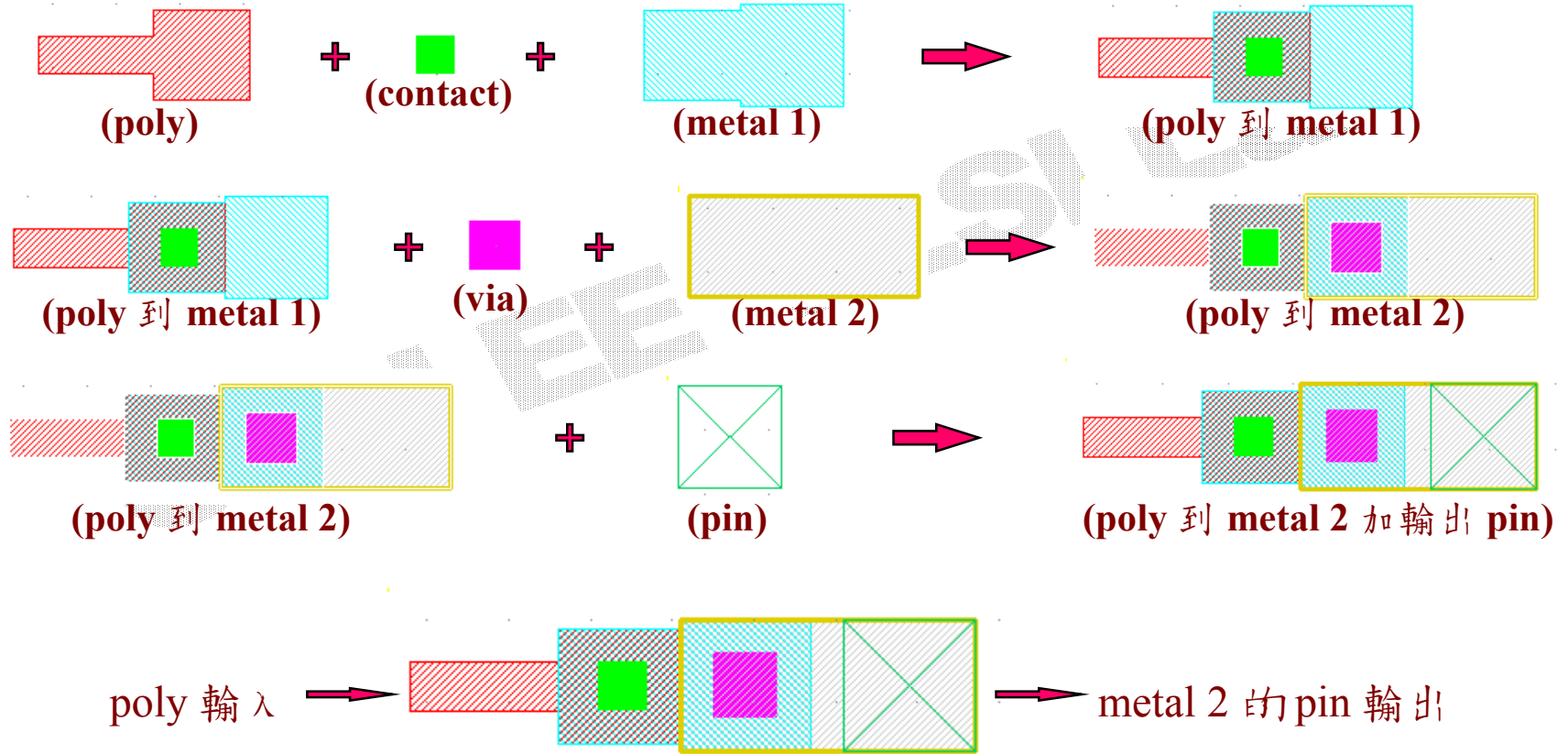
mouse L: Enter Point M: Point at the opposite corner of the chop rectangle R: Toggle L90 X/Y





Practice Layout (II)

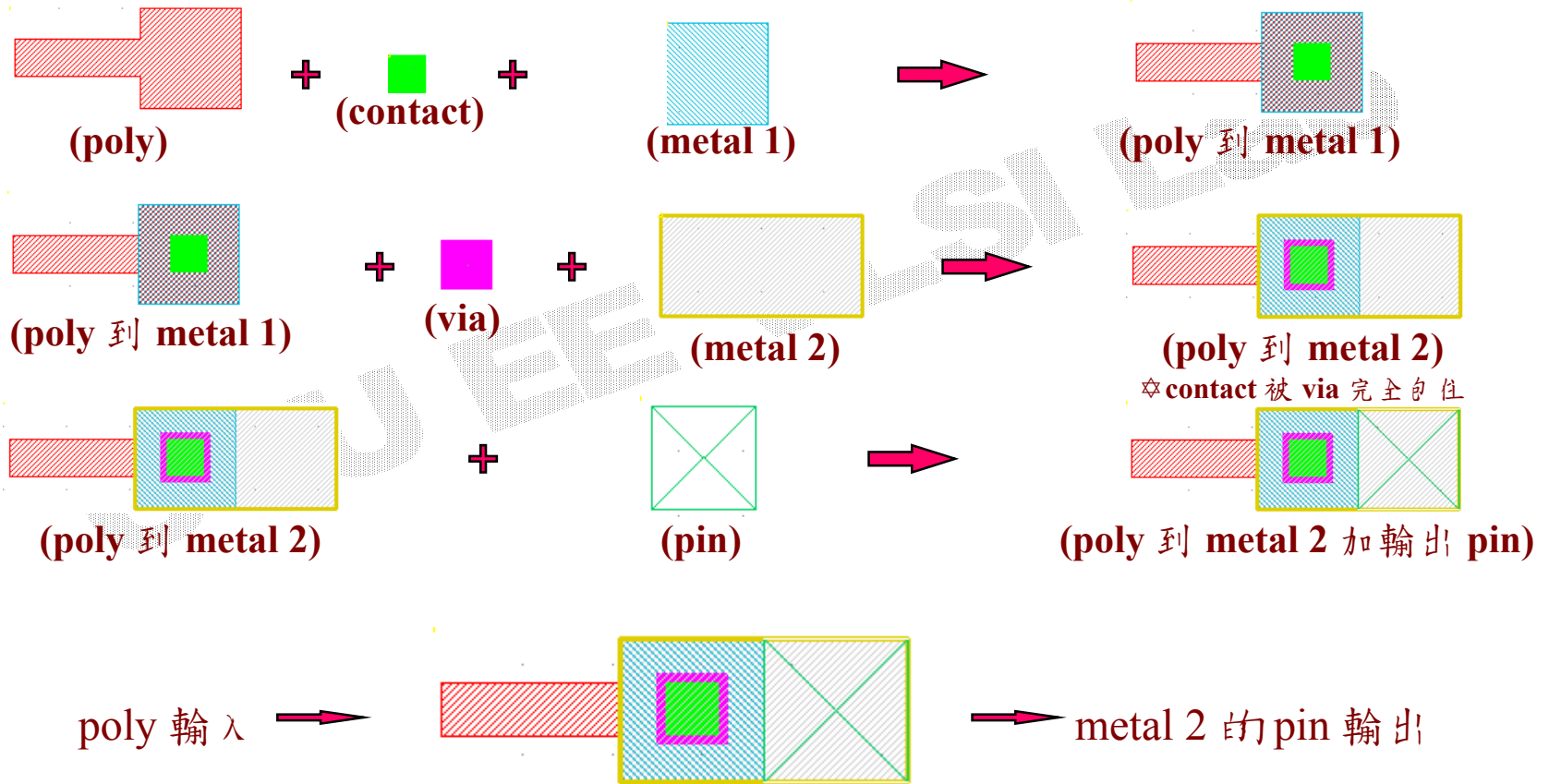
畫 layout 必須有層次的先後觀念，例如一個訊號從 poly 輸入，而從 metal 2 輸出，就必須先畫 poly 再疊上 contact，再疊上 metal 1，再疊上 via，最後再疊上 metal 2。其過程缺一不可。如下所示：





Practice Layout (III)

另一種方法比較節省面積，就是 via 與 contact 重疊在一起。同樣的例子，如一個訊號從 poly 輸入，而從 metal 2 輸出。如下所示：





Practice Layout (IV)

現在來學習加pin吧，開始

注意：
metal 2 (pn)層，而非(dg)層

請設定Names、I/O Type 及 Access 方向。Access 方向是依照cell design rule 的規定，一般 standard cell 的 metal 1 設定為 Access 方向，而 metal 2 設上下為 Access 方向。

設定完後配合 mouse 的 click 及 拖曳 就可以畫 pin

若要再察看 pin 的屬性，只要 冊先選好 pin 後按 q 鍵即開出 如下的視窗，選擇 connectivity 便可察看甚至修改。

mouse L: mouseSingleSelectPt M: mousePopUp() R: geScroll(nil "e" nil)



Practice Layout (V)

Feedthrough pin 的建立

此為 Feedthrough pin 其基本組合如下：

此為設定 pin 時的參考，建立過程請參考上一頁，值得注意的是 I/O Type 選 jumper 而 Name 任意取名，但不重複

Create Pin

Hide Cancel

Terminal Names

Pin Shape rectangle polygon auto pin

Display Name Set Name Display

Snap Mode 1L

I/O Type input output inputOutput
 switch jumper

Access Direction top bottom left right
 any none

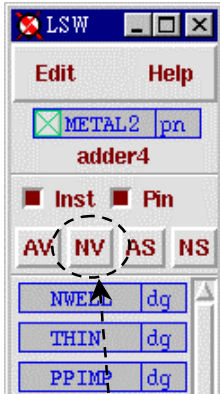
mouse L: mouseSingleSelectPt M: mousePopUp() R: hiZoom
Ready >





Practice Layout (VII)

檢查 pin 腳
輸出的方向



先選除目前選
用的層外其餘
層皆不會顯示
出來的方式。

如下選擇設定 Access Edges 等確
定後，就只會顯示 Access Edges

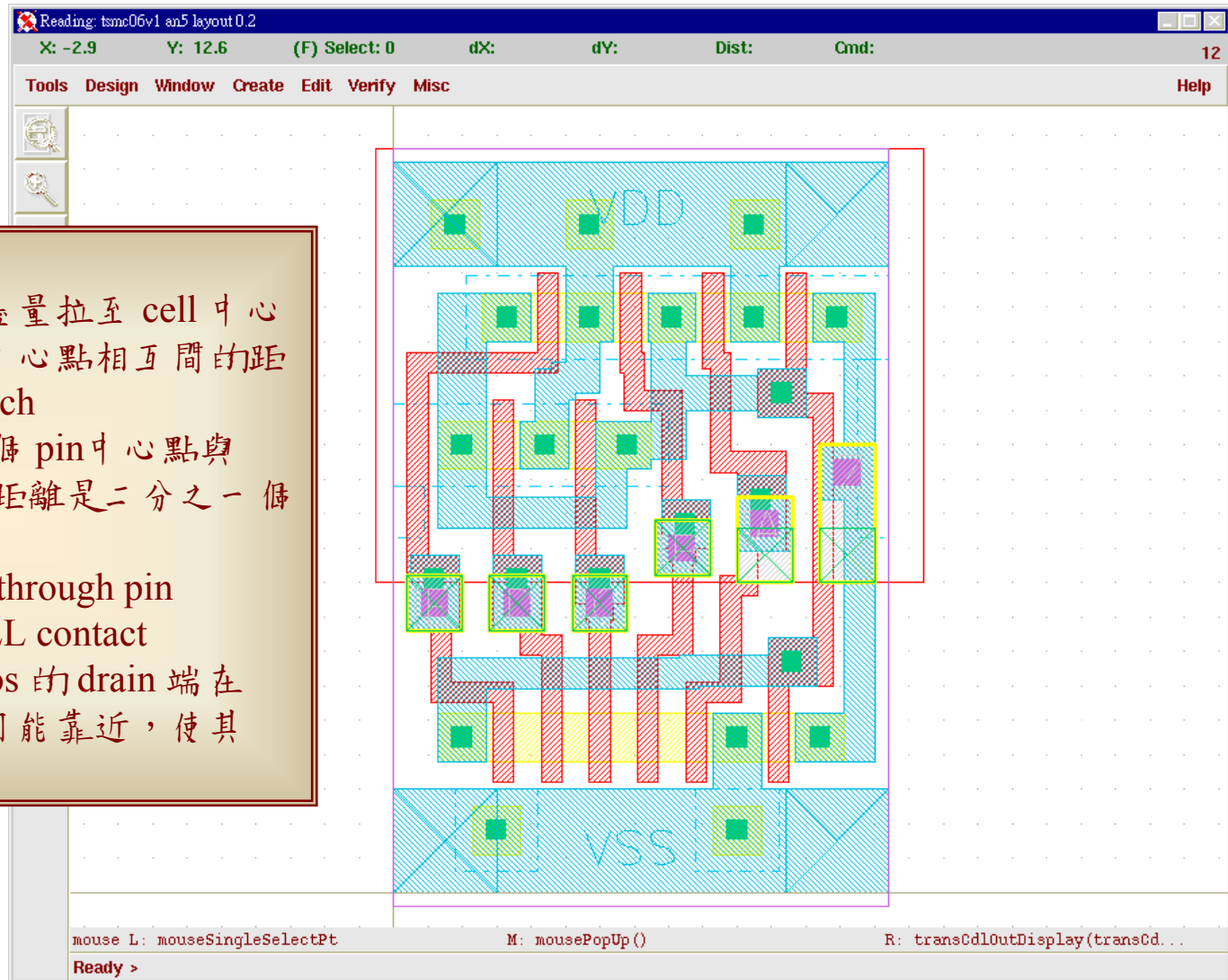




Finished Layout

一般注意事項：

- 輸出入 pin 盡量拉至 cell 中心
- 兩個 pin 的中心點相互間的距離是一個 pitch
- 最外面的二個 pin 中心點與 boundary 的距離是二分之一個 pitch
- 盡量加 Feedthrough pin
- 盡量加 WELL contact
- pmos 及 nmos 的 drain 端在 layout 時盡量靠近，使其面積最小





Verifications

Ckt layout 完成後所須作的驗證如下：

- DRC (Design Rule Check) :
對 IC 的佈局(layout) 作幾何空間的檢查以確保線路能夠被特定的製程技術所實現。
- ERC (Electrical Rule Check) :
檢查 power, ground 的 short, floating device, floating net 等指定的電氣特性。
- LVS (Layout Versus Schematic) :
將 layout 與 schematic 作比對，以檢查電路的連接，與 MOS 的 Length、Width 值是否配。
- LPE (Layout Parameter Extraction) :
從 layout database extract 電氣參數(如 MOS 的 W、L 值，BJT，diode 的 area，perimeter，node 的 parastic cap.)，並以 HSPICE netlist 方式表示電路。





Diva Versus Dracula

- 光罩或製程在 IC 製過程是相當昂貴的，所以佈局驗證的重要性自然是不言而喻，一般佈局驗證包括 DRC(Design Rule Check)，ERC(Electric Rule Check) 及 LVS(Layout vs. Schematic 的比較)。
- Cadence 擁有兩套佈局驗證系統：
 - Opus 中的 Diva 是 on-line 交談式，具有快速驗證小 cell 及與 Opus 完整整合的優點，缺點是對大晶片可能無法作完整驗證，又一般來說，Diva 之 run time 較 Dracula 長。
 - Dracula 是傳統 batch-job 方式，Dracula (吸血鬼) 被公認是佈局驗證的標準，幾乎全世界所有 IC 公司都拿它來作 sign-off 的憑據。
- 一般 Diva 用於對小 cell 或中型 block 的 layout 設計驗證，而 whole chip 的最後驗證則一定要交由 Dracula 處理。





Diva DRC (I)

The screenshot displays the Diva DRC software interface. The main window shows a layout editor with a grid and various components. A menu is open, highlighting the 'DRC...' option. A dashed arrow points from this menu item to the 'DRC' dialog box on the right. The dialog box contains several settings for the Design Rule Check (DRC) process, including checking methods, limits, and machine options. Below the dialog box, a text box contains a Chinese explanation of the CIW (Command Input Window) functionality. At the bottom, a log window shows the execution of the DRC command and the resulting output, indicating that no errors were found.

在 CIW 上可以看到檢查過程的訊息，並且在最後會列出違犯 rule 的項目，屆時 layout view 上亦會以閃動方式顯示錯誤。

```
icfb - Log: \vlsi-b\ms84\wangjc\CDS.log
Open Design Manager Technology File Utilities Translators Help 1
executing: drc(METAL2-PASS-(enc < 5) "CB.E.3 METAL2 OVERLAP PASS WINDOW <5um")
executing: ivif( (switch "extract?") then
executing: ivif( (switch "oparasitics") then
***** Summary of rule violation for cell "and5 layout" *****
Total errors found: 0
mouse L: mouseSingleSelectPt M: mousePopUp() R: ivHiDRC()
Ready >
```





Diva DRC (II)

The screenshot shows the Diva DRC software interface. The top window displays a log file with the following content:

```

icfb - Log: \vlsi-b\ms84\wangjc\CDS.log
Open Design Manager Technology File Utilities Translators Help 1
executing: ivIf( (switch "Cparasitics") then
***** Summary of rule violation for cell "and5 layout" *****
# errors Violated Rules
1 M1.S.1 METAL1 spacing < 0.8um
Total errors found
  
```

The design window shows a layout with a red hatched area indicating a violation. A context menu is open over this area, with the 'Markers' option selected, showing a sub-menu with 'Explain', 'Find...', 'Delete', and 'Delete All...'.

Three dialog boxes are shown:

- marker text**: Shows the location and reason for the violation: "location: ('adder4' 'and5' 'layout')", "reason: M1.S.1 METAL1 spacing < 0.8um".
- Find Marker**: A dialog for searching for markers, with 'Apply' selected.
- Delete All Markers**: A dialog for deleting all markers, with 'Apply' selected.

Annotations in red text provide instructions:

- click 於閃動處以得悉所違犯 rule 的說明 (Click on the flashing area to get the explanation of the violated rule)
- 按 Apply 會一一解釋所違犯的 rule (Pressing Apply will explain the violated rule one by one)
- 可以清除閃動的標記 (Can clear the flashing markers)

A text box at the bottom left contains the following instruction:

在 CIW 上所看到違犯 rule 的項目，必須一一解決，直到 DRC check 完全 no error 為止，並做 Save。





Create Extracted View

Extract 主要是
抽取出一些參數來
提供 LVS 時做
比對用。

The screenshot shows the Cadence Virtuoso interface. The main window is titled "Editing: adder4 and5 layout 0.1". The "Extractor" dialog box is open, showing options for "Extract Method" (flat), "Join Nets With Same Name" (unchecked), "Echo Commands" (checked), and "Switch Names" (empty). Below the dialog, a log window titled "icfb - Log: /vlsi-b/ms84/wangjc/CDS.log" displays the following text:

```
executing: ivIf( (switch "Cparasitics") then
saving rep ( _and5/extracted 0.0)
***** Summary of rule violation for cell "and5 layout" *****
(Total errors found: 0)
```

A callout box with a red border contains the text: "查看 CIW 上出現 no error 後再到 library browser 就可看到一個 extracted view". Below this, the "Library Browser" window shows a tree view for "adder4" with an "extracted" view selected under the "layout" category. The main workspace shows a circuit layout with various components and a green square highlighting a specific area.





Diva LVS (I)

The screenshot shows the Diva LVS software interface. The main window displays a circuit layout with various components and connections. A menu is open, highlighting the 'LVS...' option. The 'LVS' dialog box is open, showing the following settings:

- Run Directory Name: /vlsi-b/ms84/wangjc/LVS
- Generate New Netlist: schematic extracted
- Library Name: adder4
- Cell Name: and5
- View Name: schematic (selected), extracted
- Correspondence Points: terminals
- LVS Options: file, Create textual cross, Apply device fixing, Apply rewiring
- Job Priority (0 to 20): 0
- Machine: local remote
- Buttons: Run, Job Monitor..., Show Run I, Backannotate, Parasitic Simulation...

A 'Library Browser' window is open, showing a list of libraries: adder4, MET1_T, MET2_T, NTAP, NTR, PTAP, PTR, and5. The 'extracted' library is selected. A text box with a red border contains the Chinese text: "配合 library browser 來填寫資料，確定後按 Run 開始執行" (Use library browser to fill in data, confirm and press Run to start execution).

An 'Initialize Environment' dialog box is open, with the 'OK' button highlighted. A text box with a red border contains the Chinese text: "最好不選(即重新建立 si.env)" (It's best not to select (i.e., rebuild si.env)).

An 'Analysis Job Succeeded' window is open, displaying the message: "Job '/vlsi-b/ms84/wangjc/LVS' that was started at 'Mar 14 11:38:55 1997' has succeeded". A text box with a red border contains the Chinese text: "等到出現 succeeded 就代表比對完成了" (When 'succeeded' appears, it represents that the comparison is complete).





Diva LVS (II)

Show Run Information

OK Cancel Defaults Apply Help

Show Run Information Log **Output** Schematic Netlist Layout Netlist

LVS

Commands Help 17

Run Directory Name: /vlsi-b/ms84/wangjc/LVS

Generate New Netlist: schematic

Library Name: adder4

Cell Name: and5

View Name: schematic

Correspondence Points: terminals

LVS Options: Apply rewiring

Job Priority (0 to 20): 0

Machine: local

Run Job Monitor... Show Run Info... Error Display...

Backannotate Parasitic Simulation...

Output

File Help 18

The net-lists match.

	layout	schematic
instances		
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	12	12
total	12	12

	layout	schematic
nets		
un-matched	0	0
merged	0	0
pruned	0	0
active	13	13
total	13	13

	layout	schematic
terminals		
un-matched	0	0
total	8	8

End comparison: Mar 14 11:39:19 1997

Comparison program completed successfully.

一定要看到 The net-lists match 的字眼，否則就得檢查 output 的結果說明，並修改到完全 match 為止。





Create Abstract View (I)

The screenshot shows a software application window titled "Editing: adder4 and5 layout0.1". The menu bar includes "Tools", "Design", "Window", "Create", "Edit", "Verify", "Misc", "Abstract", and "Help". The "Abstract" menu is open, showing options like "Analog Artist", "Compactor", "Design-By-Example", "Device-Level Editor", "Floorplan/P&R", "Layout", "Layout Synthesis", "Microwave", "Module Maker", "Pcell", "Simulation", "Structure-Compiler", "Verification", "Verilog-XL", and "Veritime". A "Select PR Engines" dialog box is open, with "OK" circled. A text box with Chinese text says: "按 OK 後，在 menu bar 上就增加了一個 Abstract 功能". The dialog box also has "Cancel" and "Help" buttons, and a section for "Select Target P&R Engine" with radio buttons for "CE/BE" and "GE/C3". The background shows a circuit layout with various components and a "VSS" label.





Create Abstract View (II)

The screenshot shows a PCB design software interface with the following elements:

- Menu:** Tools, Design, Window, Create, Edit, Verify, Misc, Abstract, Help.
- Abstract Menu:** Lib Cell..., Layout Prep..., Auto Boundary, Abgen..., Create Obstruction..., Obstruction Merge, Create Pin..., Set Pin Connect..., Set Track Info..., Library Checking..., Set Cell Props..., Set Pin Props...
- Create Abstract Dialog:** OK, Cancel, Defaults, Apply, Help. Options: Generate From (Cellview, Library), Input View (layout), Output View (abstract), Copy Pins Only (checked), Insert FeedThrus (unchecked).
- Library Browser:** Level: lib cell cellview version 2. Commands: adder4, MET1_T, MET2_T, NTAP, NTR, PTAP, PTR, and5. Set Options: abstract, extracted, layout, schematic, symbol.
- Status Bar:** mouse L: mouseSingleSelectPC(), M: absMousePopUp(), R: absHiCreateObstruct(), Ready >

請選擇
Copy Pins Only
，再按 OK，
library browser
就會增加
abstract view





Abstract View Change Property (I)

The screenshot displays two windows from a CAD application. The left window, titled "Library Browser", shows a hierarchical tree of components. A context menu is open over the tree, with the "Edit" option circled in red. A dashed arrow points from this "Edit" option to the "Design Properties..." menu item in the right window. The right window, titled "Editing: test-lib an02d2 abstract 0.1", shows an abstract view of a circuit with a menu open over it. The "Design Properties..." option is highlighted in the menu. A solid arrow points from this menu item to a text box on the right. Another solid arrow points from the text box to the abstract view itself.

做完以上的步驟
到Library Browser
開出Abstract View，
且應該 show 如左圖

再設定該Abstract view
的property，使之可以被
auto P&R。





Abstract View Change Property (II)

OK Cancel Apply Next Previous Help

◇ Attribute ◇ Connectivity ◇ Parameter ◆ Property ◇ Common

abstractViewName abstract

absPREngine ce

drc Signature 5637896

drc Checked Fri Nov 22 16:09:24 1996

pin# 13

instancesLastChanged Sat Nov 23 11:05:10 1996

Add Delete Modify

設成Property

按下 Add鍵

OK Cancel Apply Help

Name prCellType

Value standard

Type String

Choices

Minimum Maximum





Abstract View Change Property (III)

★欲去掉不必要的 property information

用mouse點此文字部分再按Delete 即可

Property	Value
pin#	13
instancesLastChanged	Sat Nov 23 11:05:10 1996
maskLayoutSubType	abstract
originalViewName	layout
viewSubType	designPlanAbgen
prCellType	standard

Buttons: OK, Cancel, Apply, Next, Previous, Help, Add, Delete, Modify

★設定完後，再 Check & Save

