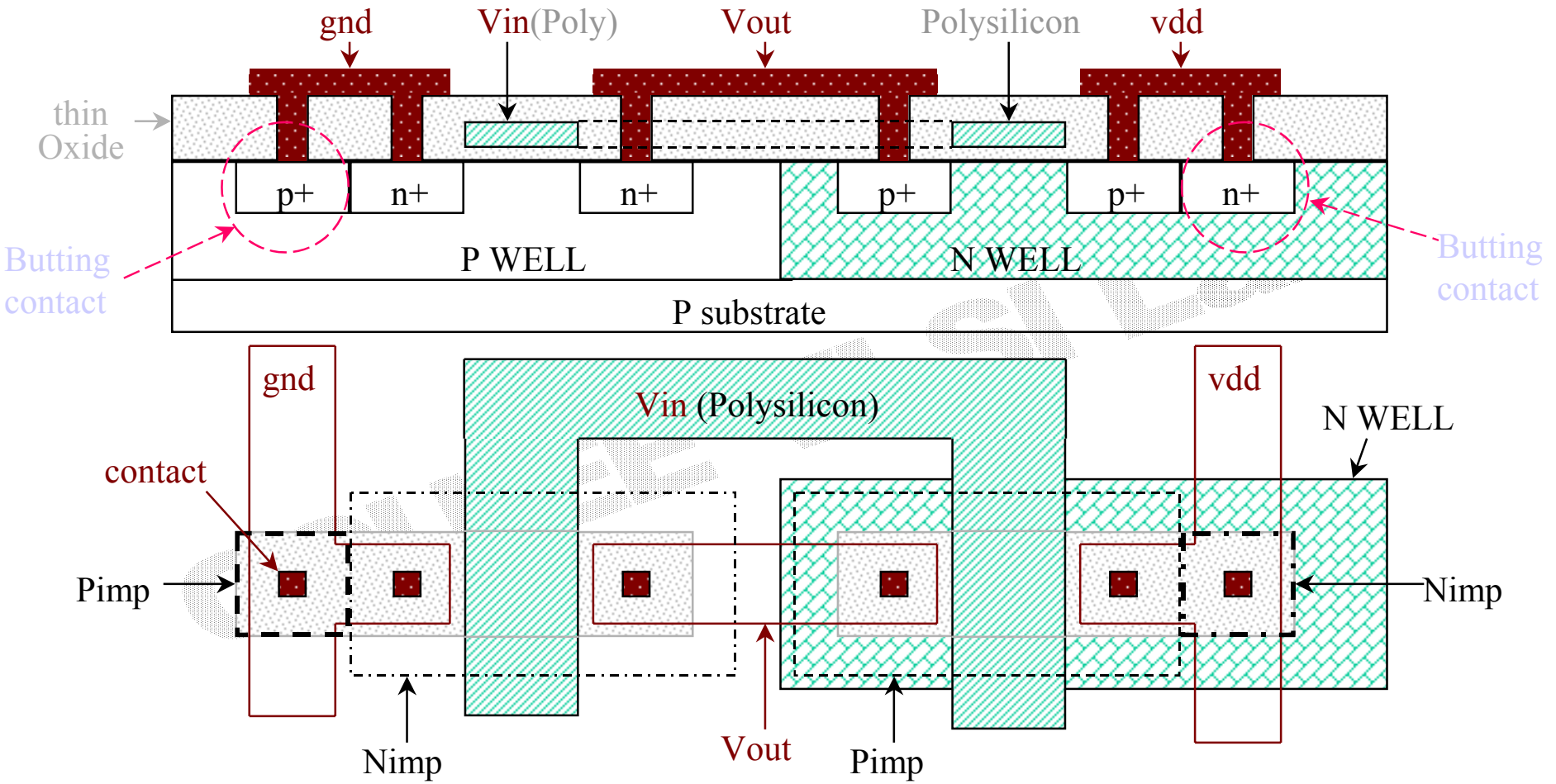
Layout Design and Verifications

- Cross Section & Layout View
- Layout (Design) Rules
- Cell Butting Rules
- Edit Layout
- Verifications (DRC/LVS)
- Create Abstract

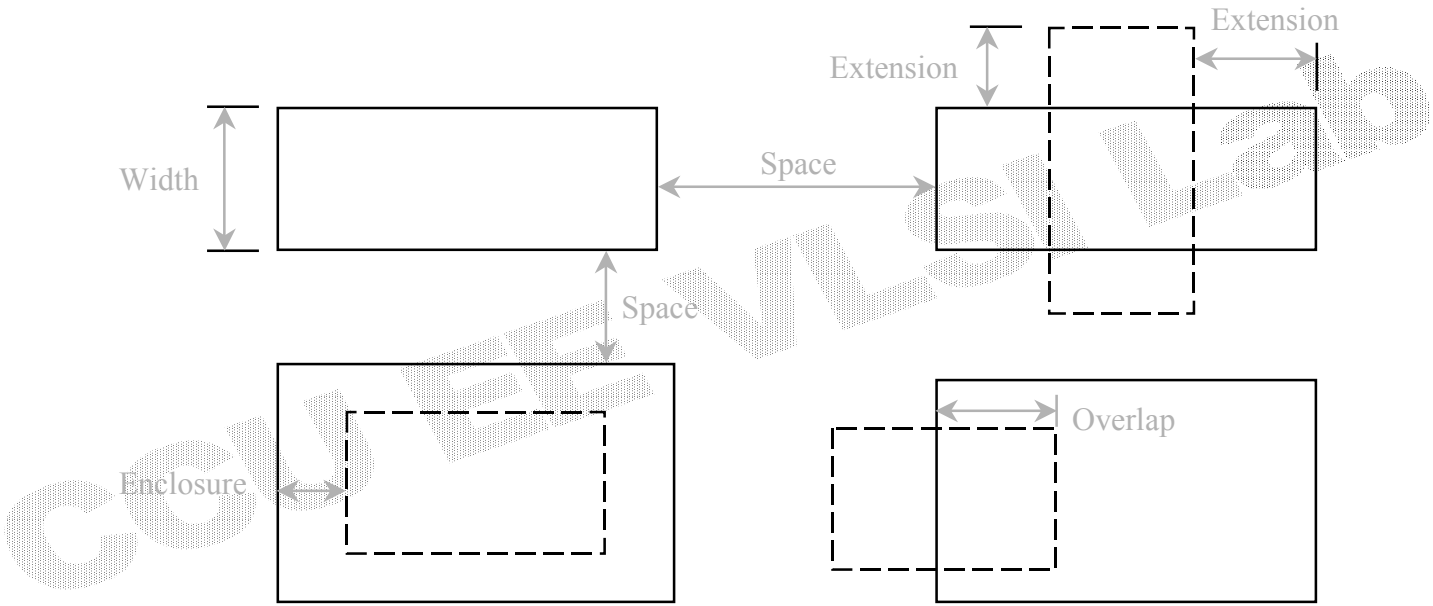
Cross Section & Layout View



CMOS 的反相器的橫截面圖與佈局(layout)圖

Definition For Parameters Of Layout Rules

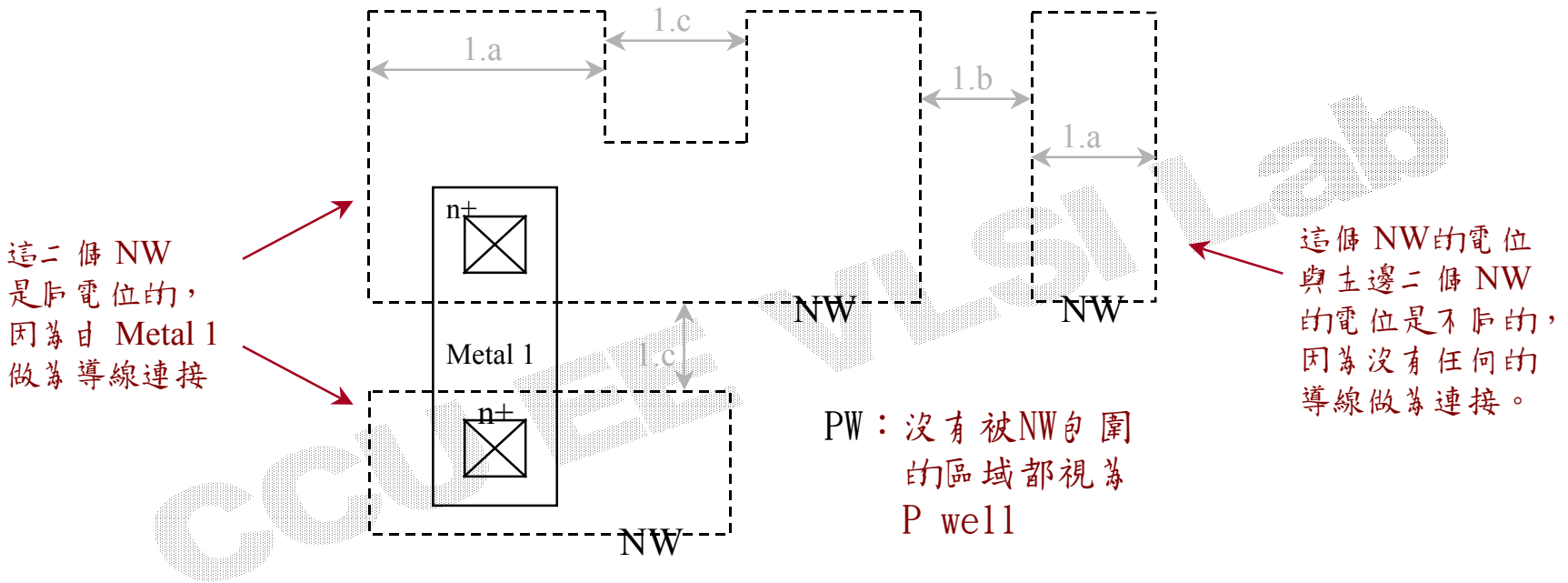
基本定義 (Definition)



1.請記住這些名稱的定義
2.接下來所介紹的layout rules必須熟記在心，
在劃layout時務必遵守這些規則。

Layout (Design) Rules (I)

1. NW (N well)

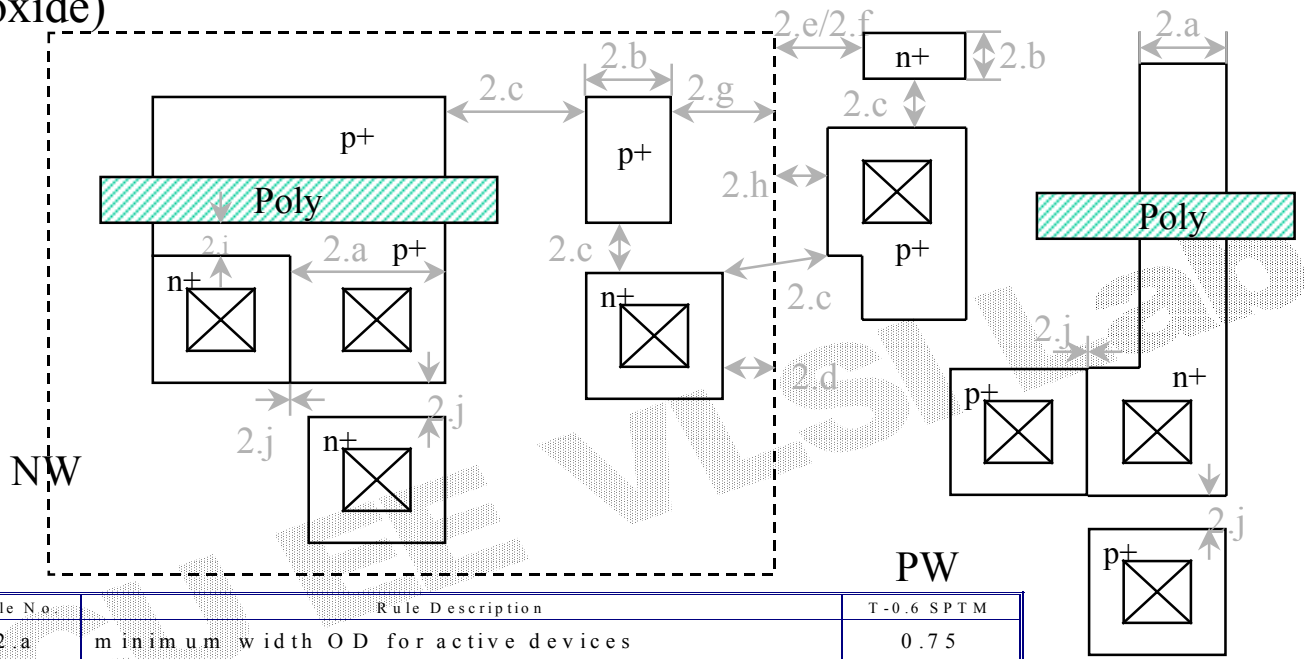


Rule No.	Rule Description	T-0.6 SPTM
1.a	minimum width NW	3.0
1.b	minimum space NW-to-NW with different potentials	4.8
1.c	minimum space NW-to-NW with the same potentials	1.5

單位為 um

Layout (Design) Rules (II)

2. OD (thin oxide)

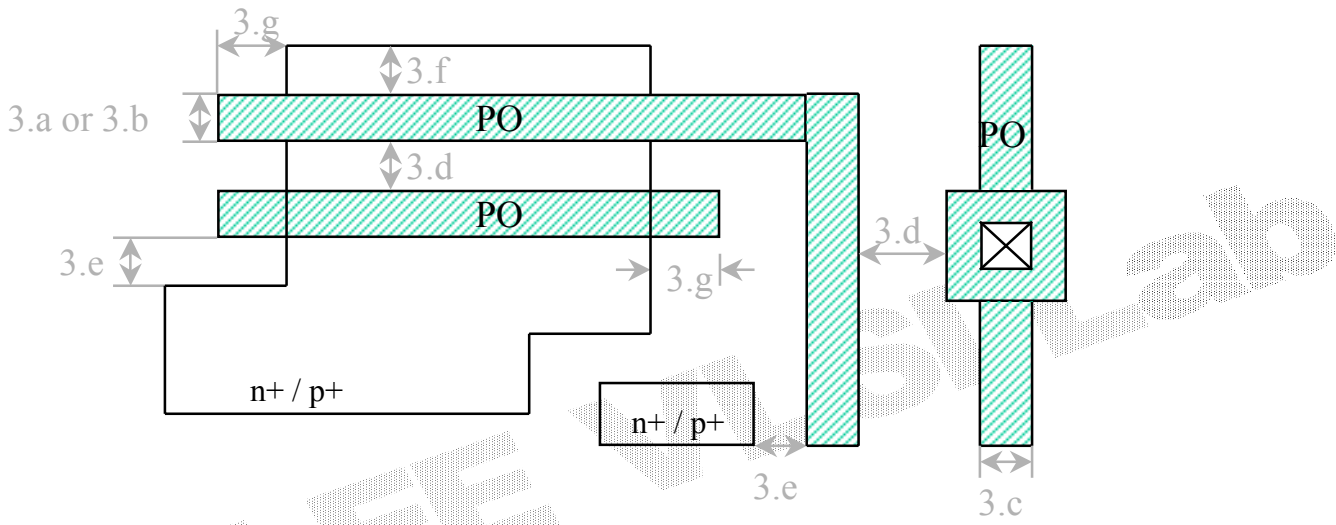


Rule No.	Rule Description	T-0.6 SPTM
2.a	minimum width OD for active devices	0.75
2.b	minimum width OD for interconnection	0.6
2.c	minimum space OD-to-OD	1.2
2.d	minimum enclosure NW [OD(n+)]	0.4
2.e	minimum space NW (cold)-to-OD(n+)	1.8
2.f	minimum space NW (hot)-to-OD(n+)	4.0
2.g	minimum enclosure NW [OD(p+)]	1.8
2.h	minimum space NW-to-OD(p+)	0.4
2.i	minimum space PO-to-OD (on active region)	0.75
2.j	minimum space OD(p+)-to-OD(n+)	0.0 or 1.2

單位為 um

Layout (Design) Rules (III)

3. PO (Poly)

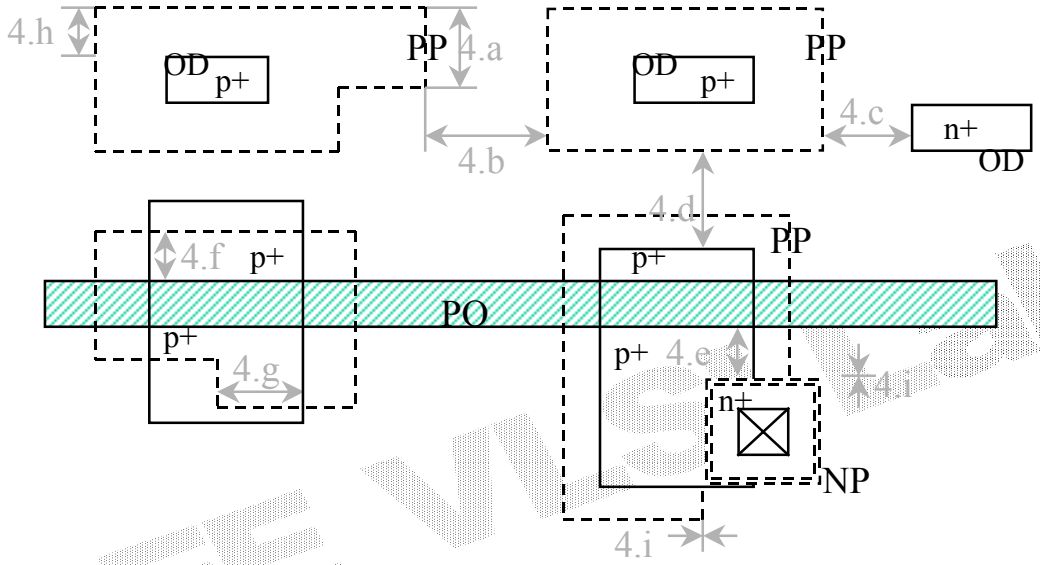


Rule No.	Rule Description	T-0.6 SPTM
3.a	minimum width PO for PMOS	0.6
3.b	minimum width PO for NMOS	0.6
3.c	minimum width PO for interconnection	0.6
3.d	minimum space PO-to-PO	0.75
3.e	minimum space PO-to-OD(on field)	0.3
3.f	minimum extension OD-over-PO	0.8
3.g	minimum extension PO-over-OD	0.6

單位為 um

Layout (Design) Rules (IV)

4. PP(P implantation)
   NP(N implantation)

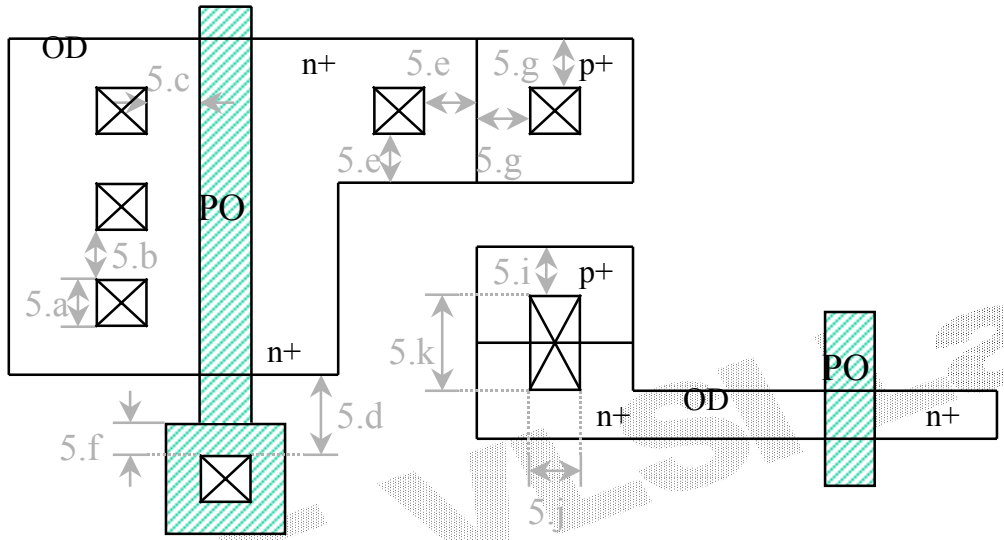


Rule No.	Rule Description	T-0.6 SPTM
4.a	minimum width PP(4.* also apply for NP)	0.9
4.b	minimum space PP-to-PP(merge if less)	0.9
4.c	minimum space PP-to-OD(n+ , hot)	0.75
4.d	minimum space PP-to-OD	0.75
4.e	minimum space NP-to-PO(on active region)	0.75
4.f	minimum extension PP-over-PO(to form S/D)	0.75
4.g	minimum overlap PP-over-OD	0.45
4.h	minimum enclosure PP[OD(p+)]	-
4.i	minimum enclosure PP[CO(butting)]	0.0

單位為 um

Layout (Design) Rules (V)

5. CO (contact)

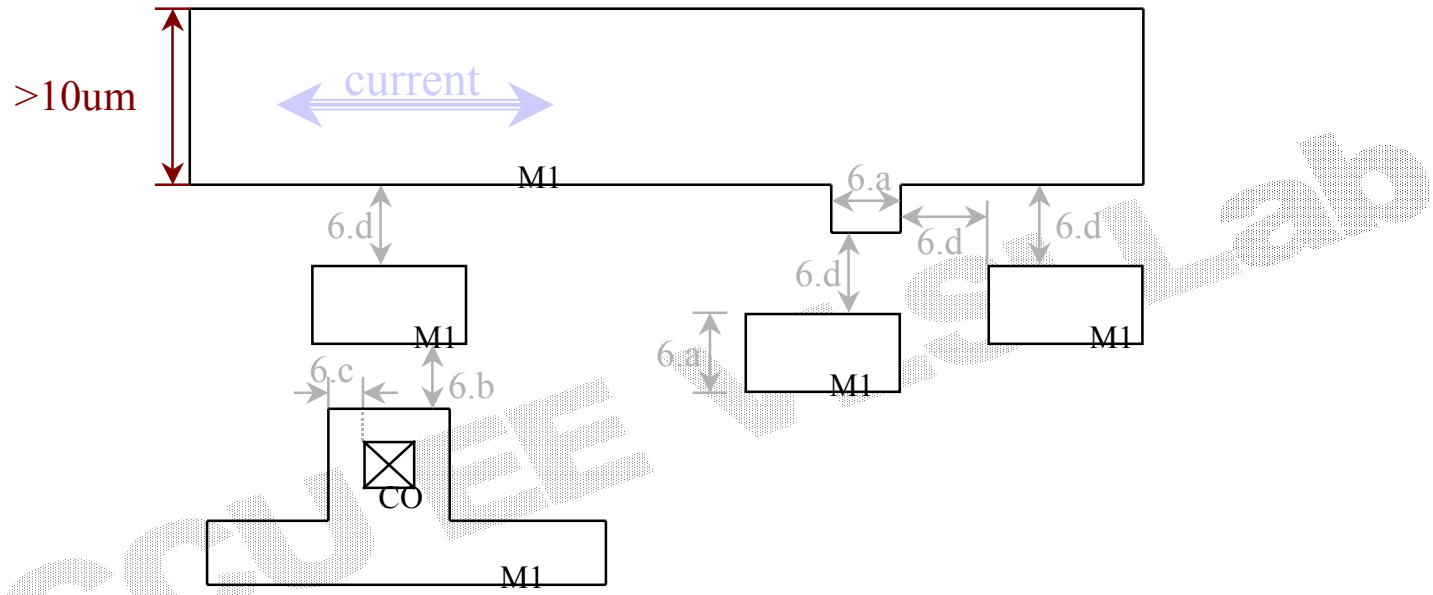


Rule No.	Rule Description	T-0.6 SPTM
5.a	minimum width CO	0.6
5.b	minimum space CO-to-CO	0.6
5.c	minimum space CO-to-PO	0.6
5.d	minimum space CO-to-OD	0.6
5.e	minimum enclosure OD[CO]	0.35
5.f	minimum enclosure PO[CO]	0.4
5.g	minimum enclosure PP/NP[CO]	0.4
5.h	CO on gate region is not allowed.	-
5.i	minimum enclosure PP/NP[CO(butting)]	0.4
5.j	minimum width CO(butting)	0.6
5.k	minimum length CO(butting)	1.2

單位為 um

Layout (Design) Rules (VI)

6. M1 (Metal 1)

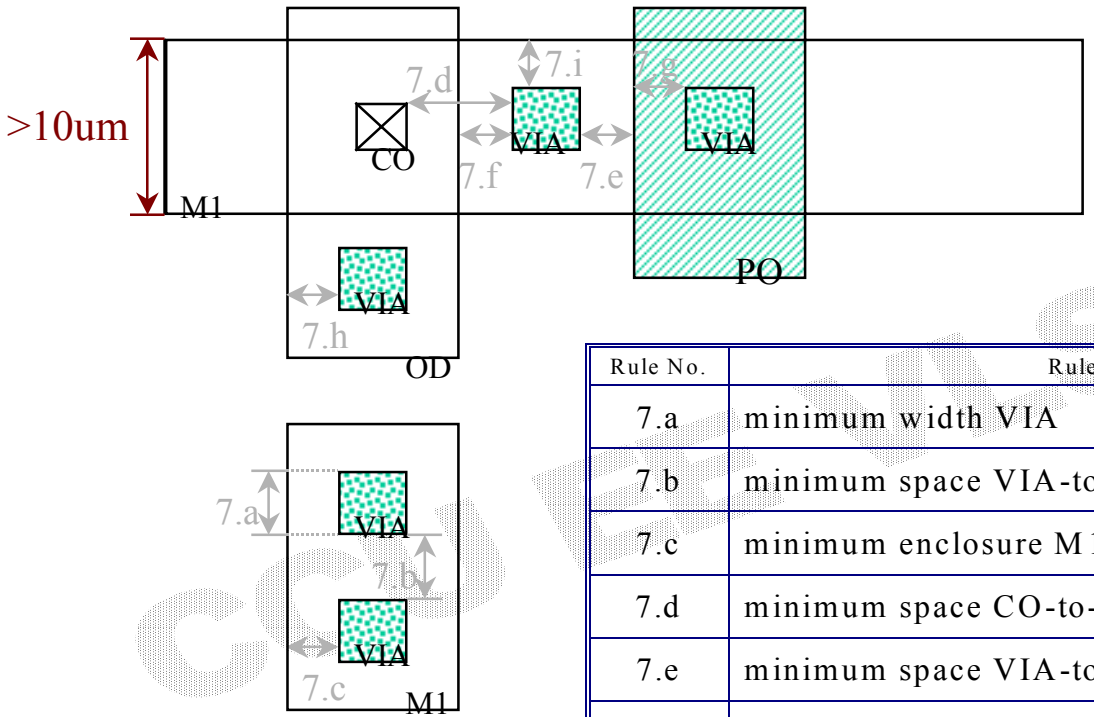


Rule No.	Rule Description	T-0.6 SPTM
6.a	minimum width M1	0.9
6.b	minimum space M1-to-M1	0.8
6.c	minimum enclosure M1[CO]	0.3
6.d	minimum space M1-to-M1(>10um)	1.3

單位為 um

Layout (Design) Rules (VII)

7. VIA (VIA 1)

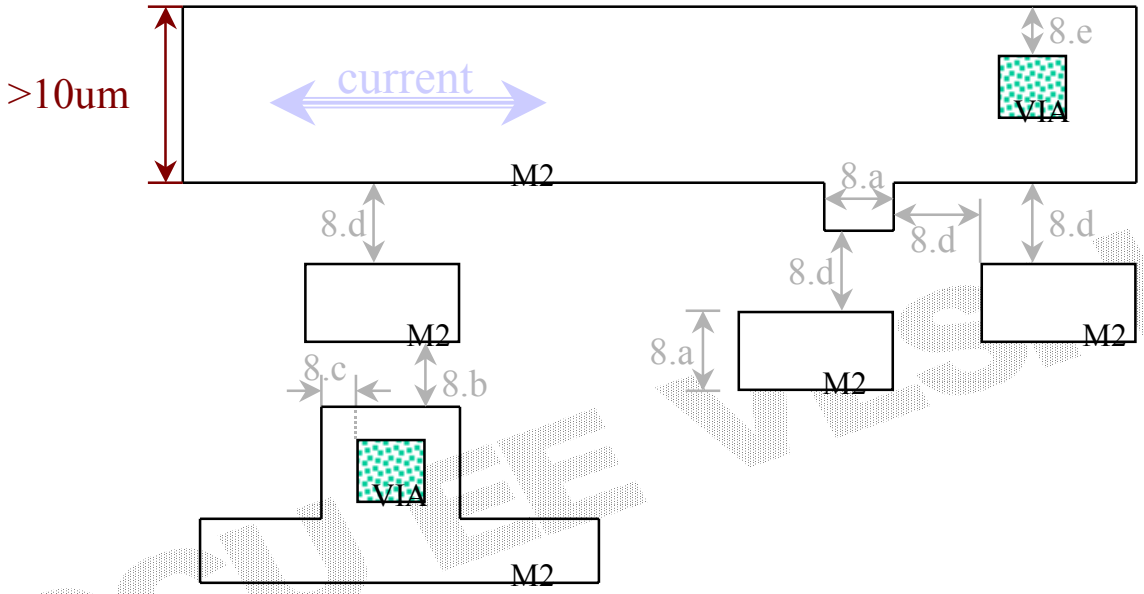


單位為 um

Rule No.	Rule Description	T-0.6 SPTM
7.a	minimum width VIA	0.7
7.b	minimum space VIA-to-VIA	0.7
7.c	minimum enclosure M1[VIA]	0.4
7.d	minimum space CO-to-VIA	0.0
7.e	minimum space VIA-to-PO	0.0
7.f	minimum space VIA-to-OD	0.0
7.g	minimum enclosure PO[VIA]	0.0
7.h	minimum enclosure OD[VIA]	0.0
7.i	minimum enclosure M1(>10um)[VIA]	1.5

Layout (Design) Rules (VIII)

8. M2 (Metal 2)

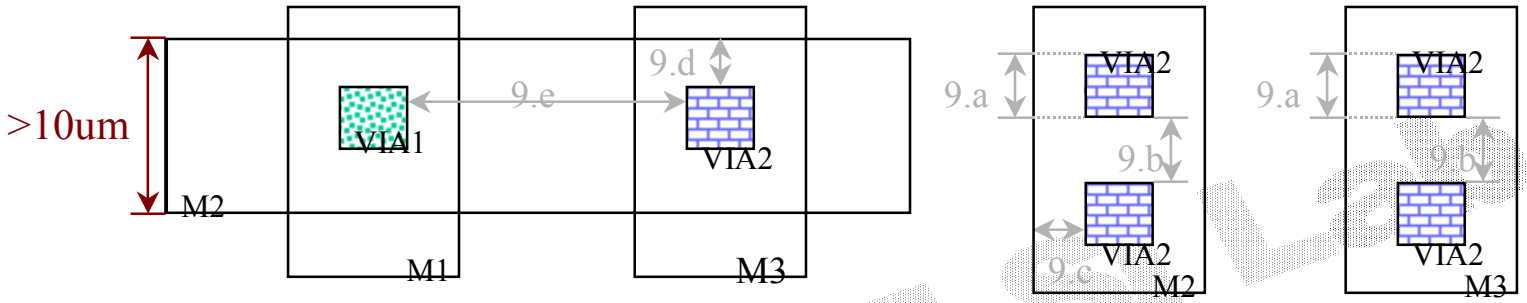


Rule No.	Rule Description	T-0.6 SPTM
8.a	minimum width M2	0.9
8.b	minimum space M2-to-M2	0.8
8.c	minimum enclosure M2[VIA]	0.4
8.d	minimum space M2-to-M2(>10um)	1.3
8.e	minimum enclosure M2(>10um)[VIA]	1.5

單位為 um

Layout (Design) Rules (IX)

9. VIA 2

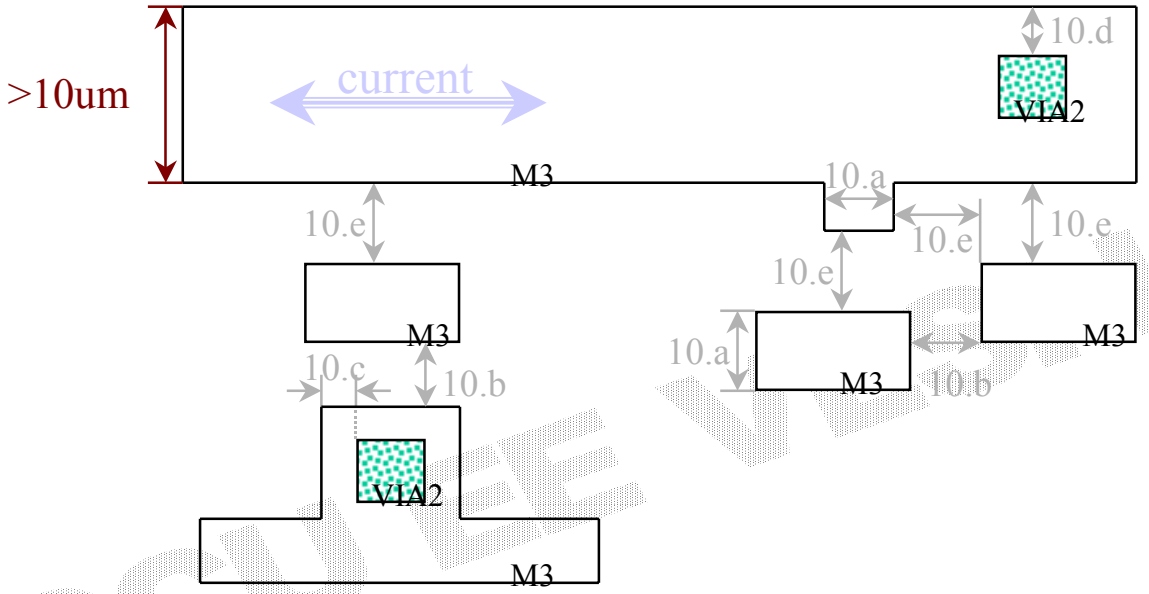


Rule No.	Rule Description	T-0.6 SPTM
9.a	minimum width VIA2	0.7
9.b	minimum space VIA2-to-VIA2	0.7
9.c	minimum enclosure M2[VIA2]	0.4
9.d	minimum enclosure M2(>10um)[VIA2]	1.5
9.e	minimum space VIA1-to-VIA2	0.6

單位為 um

Layout (Design) Rules (X)

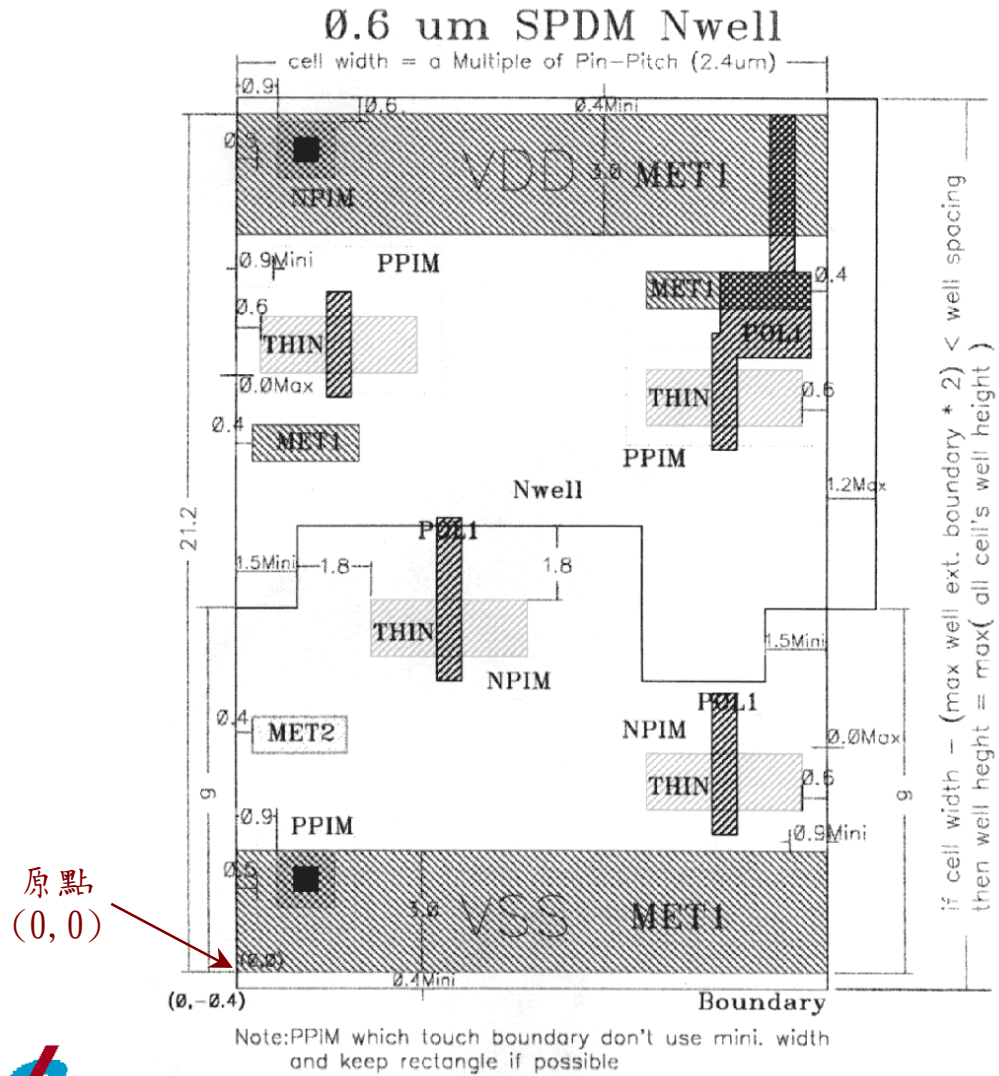
10. M3 (Metal 3)



Rule No.	Rule Description	T-0.6 SPTM
10.a	minimum width M3	0.9
10.b	minimum space M3-to-M3	0.8
10.c	minimum enclosure M3[VIA2]	0.4
10.d	minimum enclosure M3(>10um)[VIA2]	1.5
10.e	minimum space M3-to-M3(>10um)	1.3

單位為 um

Cell Butting Rules (A)



⇨左圖為使用 0.6um Single Poly Double Metal 製程之每一個 Standard Cell 都必須遵守CMOS 第一種的共同規則例子。主要的用意是在使任意的兩個 Cell 在做連接後，都還能符合 Design Rule。

⇨一般高度都是固定的，而寬度以 pitch(2.4um) 為單位，依照 Cell 電晶體數目的不同，寬度的大小就不同，但都必須是 pitch 的倍數。

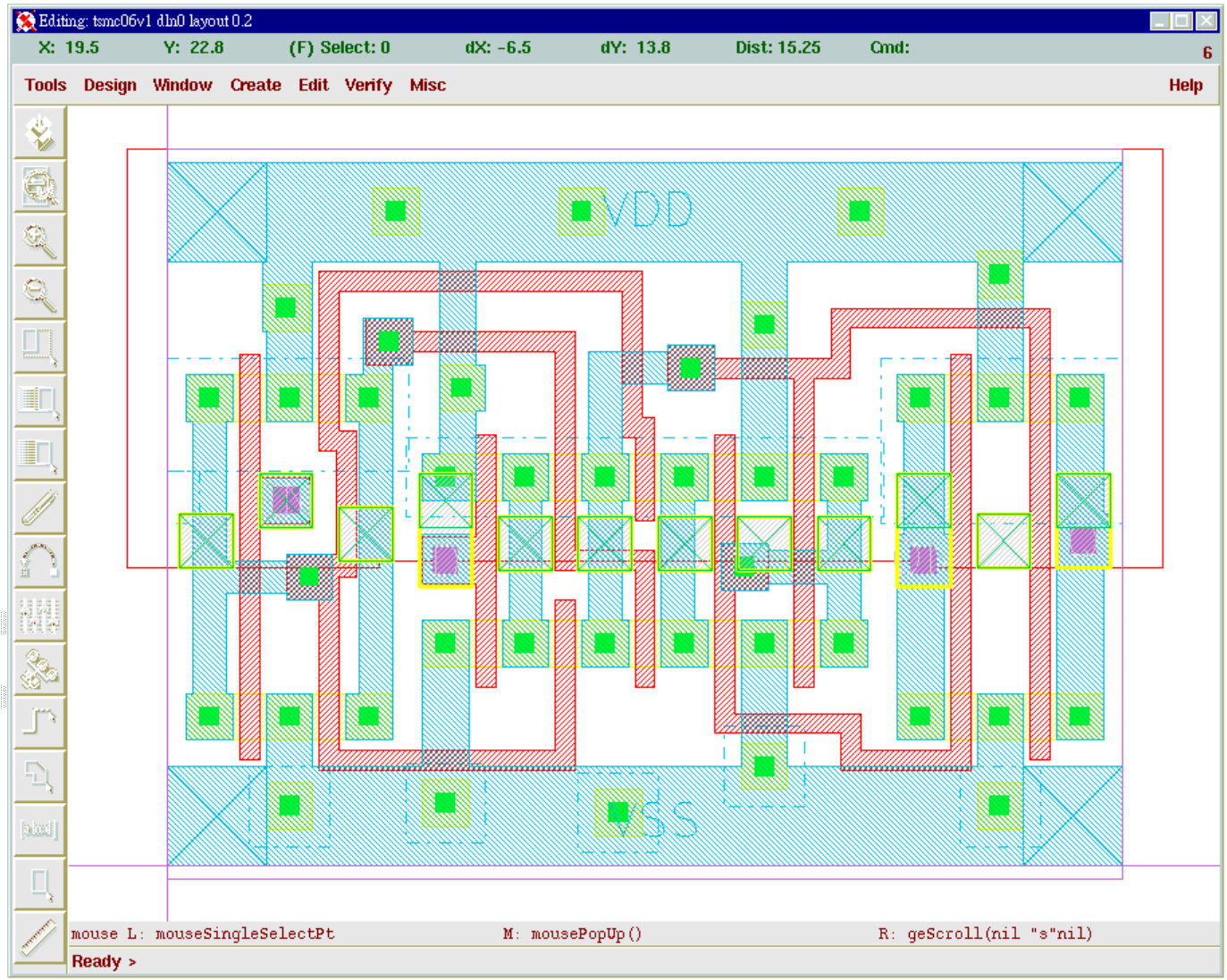
⇨而一般"單位 pitch"就是指兩個 pin 中心點相互間最小的距離。

⇨接地線(VSS/Metal 1) 的左下角為原點須放在 layout 圖上游標所指的原點(0,0)。

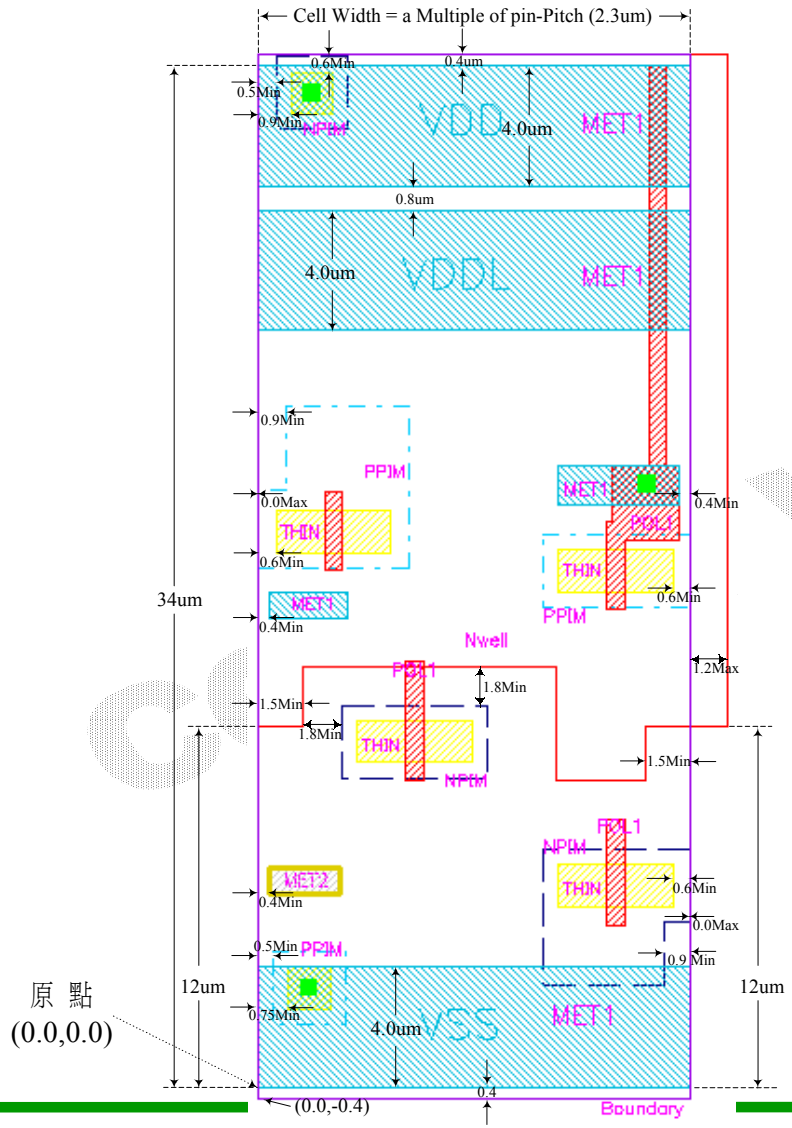
⇨VDD與VSS 須使用 Metal 1 做為連線且位置及高度都是固定的。(exp.，21.2um)

⇨其餘的數字如 0.9 或 0.9Mini 意思是寬度至少大於 0.9um，而 1.2Max 意思是寬度不可以超過 1.2um。

Example Using Cell Butting Rules (A)



Cell Butting Rules (B)



⇨上圖為使用 0.6um Single Poly Double Metal 製程之每一個 Standard Cell 都必須遵守 CMOS 第二種的共同規則例子。主要的用意是在使任意的兩個 Cell 在做連接後，都還能符合Design Rule。

⇨一般高度都是固定的，而寬度以 pitch(2.3um) 為單位，依照 Cell 電晶體數目的不同，寬度的大小就不同，但都必須是 pitch 的倍數。

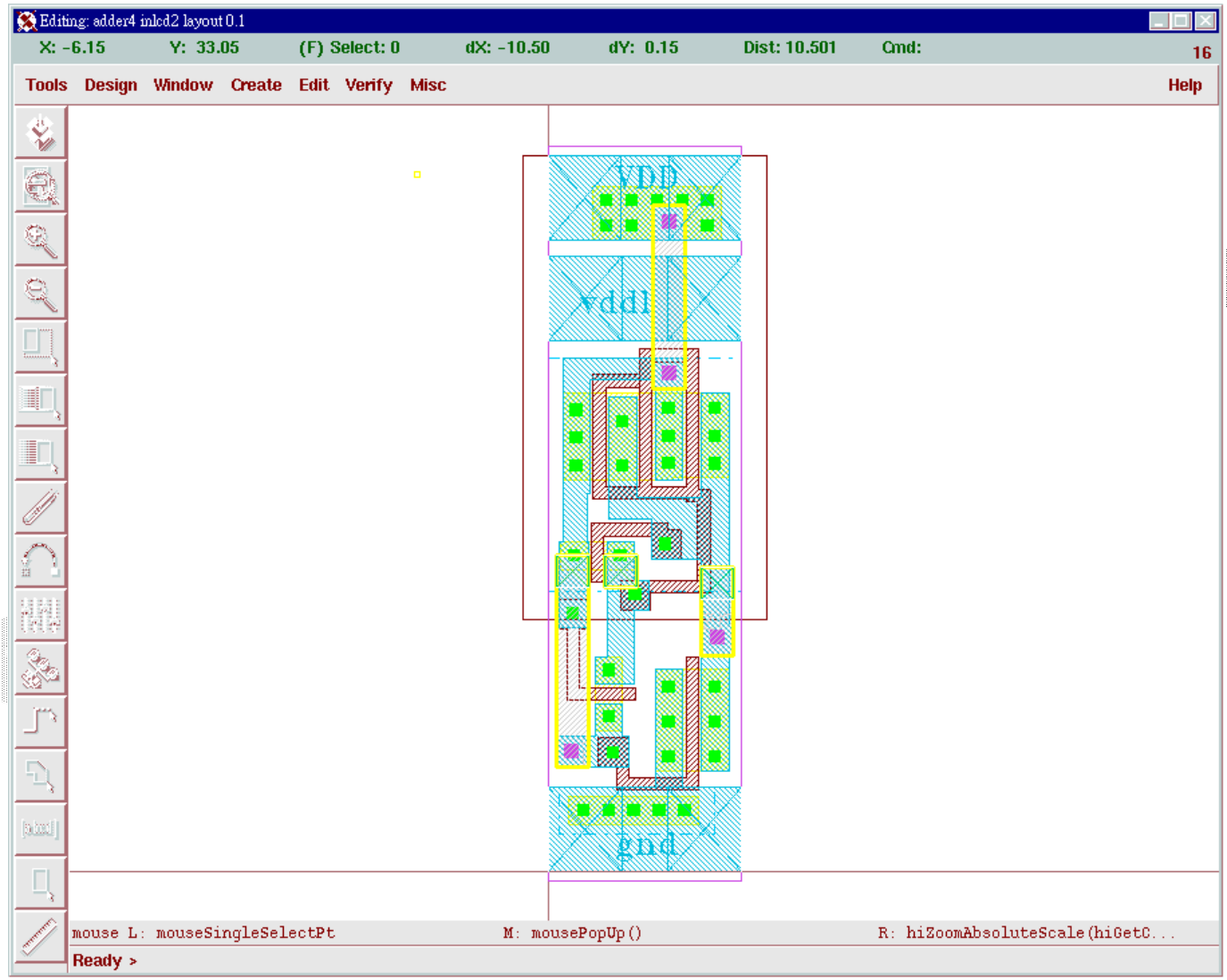
⇨而一般"單位 pitch"就是指兩個 pin 中心點相互間最小的距離。

⇨接地線(VSS/Metal 1)的上下角為原點須放在 layout 圖上游標所指的原點(0,0)。

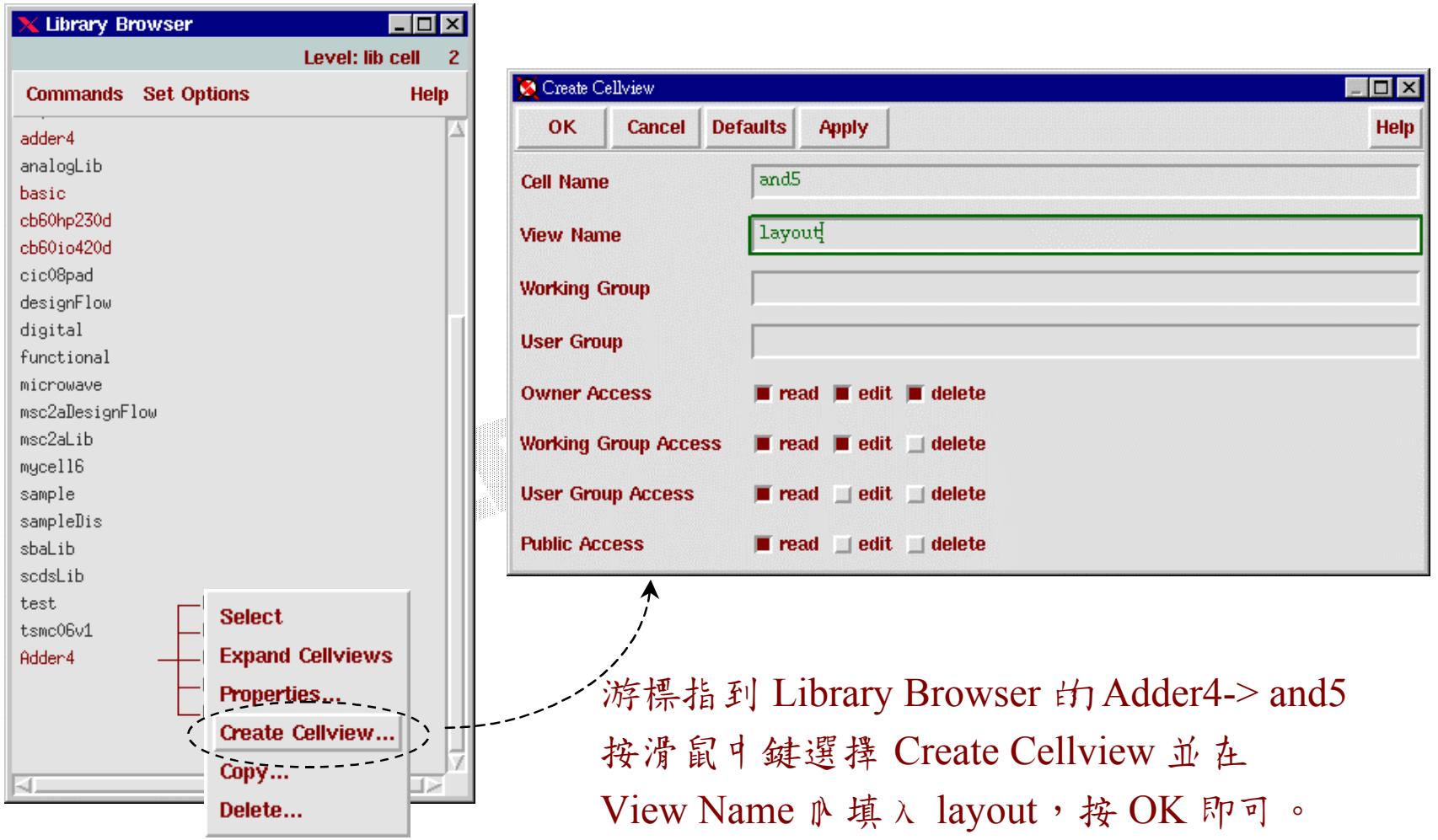
⇨ VDD、VDDL與VSS 須使用 Metal 1 做為連線且位置及高度都是固定的。(exp.，34um)

⇨其餘的數字如 0.9Min 意思是寬度至少大於 0.9um，而 1.2Max 意思是寬度不可以超過 1.2um。

Example Using Cell Butting Rules (B)



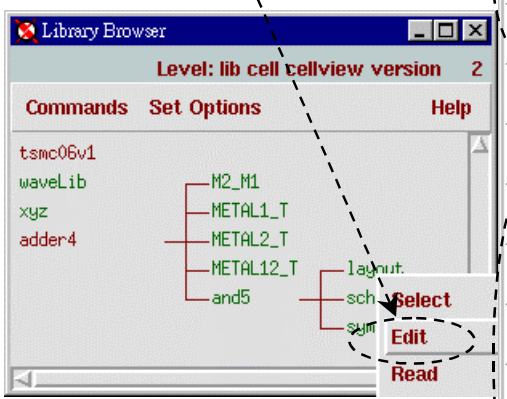
Create Layout View

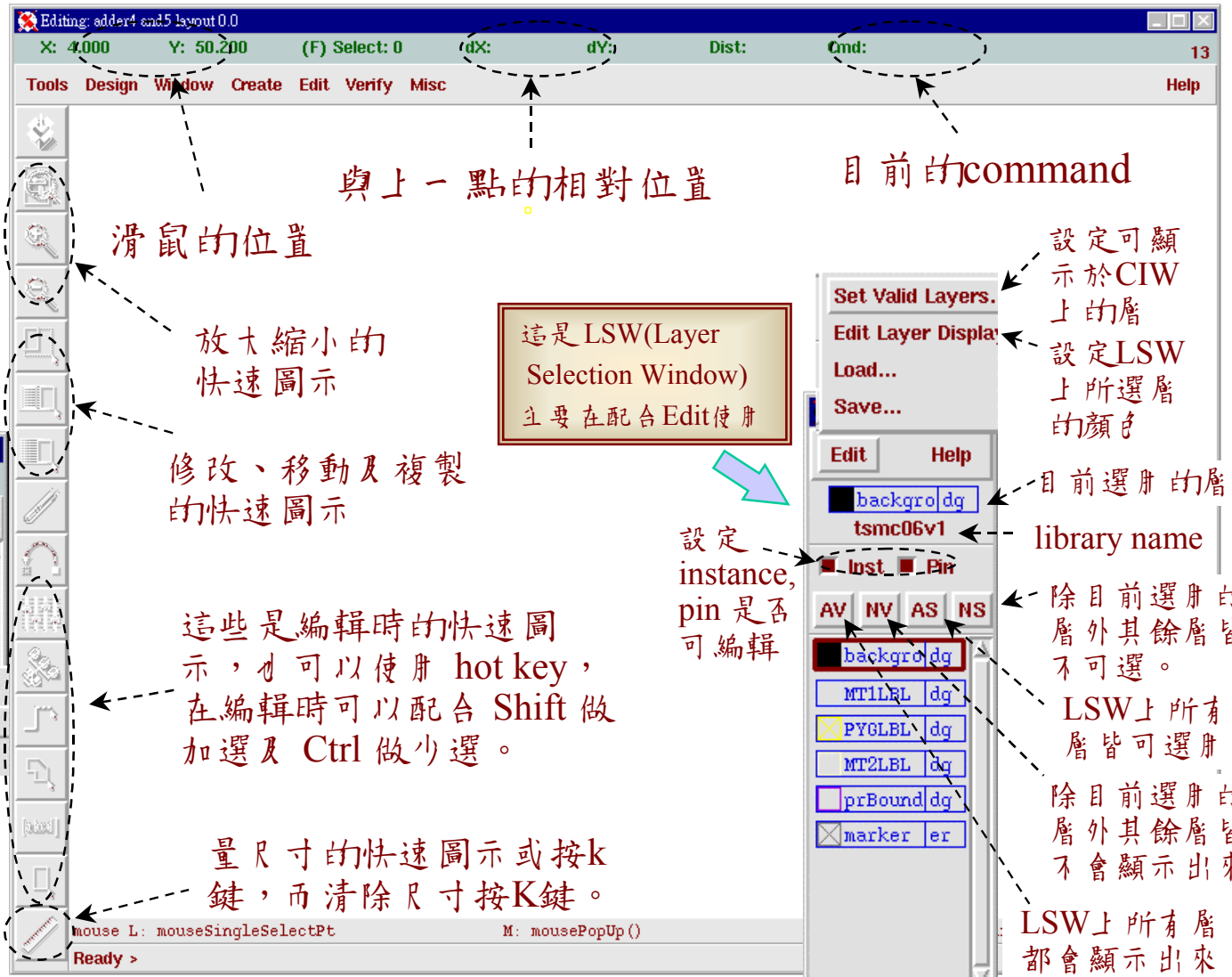


游標指到 Library Browser 的 Adder4-> and5
按滑鼠中鍵選擇 Create Cellview 並在
View Name 中填入 layout，按 OK 即可。

Edit Layout

游標指到 Library Browser 的 Adder4-> and5 -> layout
按滑鼠中鍵選擇 Edit 即可開出編輯視窗





滑鼠的位置

與上一點的相對位置

目前的command

放大縮小的快速圖示

修改、移動及複製的快速圖示

這些是編輯時的快速圖示，也可以使用 hot key，在編輯時可以配合 Shift 做加選及 Ctrl 做少選。

量尺寸的快速圖示或按k鍵，而清除尺寸按K鍵。

這是 LSW(Layer Selection Window) 主要在配合 Edit使用

設定可顯示於CIW上的層

設定LSW上所選層的顏色

目前選用的層

library name

設定 instance, pin 是否可編輯

除目前選用的層外其餘層皆不可選。

LSW上所有層皆可選用

除目前選用的層外其餘層皆不會顯示出來

LSW上所有層都會顯示出來

Compare Layers

Text Editor V3 [vlsi6] - test.tf, dir; /tmp_mnt/vlsi-b/ms84/wangjc

File View Edit Find

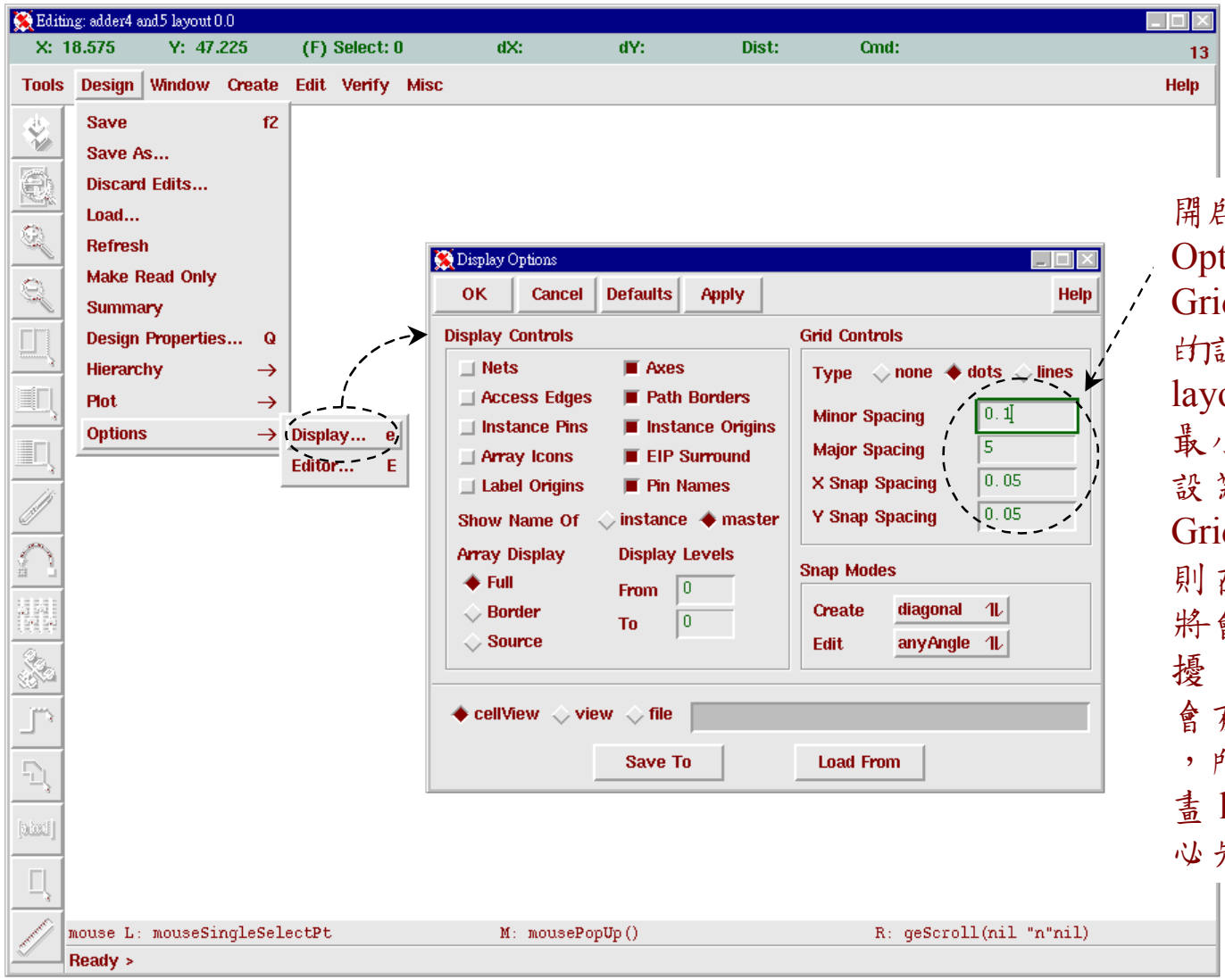
```
tfcDefinePurpose(
;( PurposeName          Purpose# )
  ( warning             234      )
  ( tool1               235      )
  ( tool0               236      )
  ( label               237      )
  ( flight              238      )
  ( error               239      )
  ( annotate            240      )
  ( drawing1            241      )
  ( drawing2            242      )
  ( drawing3            243      )
  ( drawing4            244      )
  ( drawing5            245      )
  ( drawing6            246      )
  ( drawing7            247      )
  ( drawing8            248      )
  ( drawing9            249      )
  ( boundary            250      )
  ( pin                 251      )
  ( drawing             252      )
  ( net                 253      )
  ( cell                254      )
  ( all                 255      )
)

tfcDefineLayer(
;( LayerName           Purpose  Layer# FillStyle     Priority Vis Sel Blink Valid)
  ( text2               drawing  63     outline        18      t   t   nil   t    )
  ( NWELL               drawing  2      outline        19      t   t   nil   t    )
  ( PWELL               drawing  3      outline        20      t   t   nil   nil  )
  ( THIN                drawing  4      outlineStipple 21      t   t   nil   t    )
  ( GPOLY               drawing  13     outlineStipple 22      t   t   nil   t    )
  ( NDIFF               drawing  8      outlineStipple 23      t   t   nil   nil  )
  ( PDIFF               drawing  7      outlineStipple 24      t   t   nil   nil  )
  ( NPIMP               drawing  6      outline        25      t   t   nil   t    )
  ( PPIMP               drawing  5      outline        26      t   t   nil   t    )
  ( ESD                 drawing  30     outlineStipple 27      t   t   nil   t    )
  ( CONT                drawing  15     solid          28      t   t   nil   t    )
  ( METAL1              drawing  16     outlineStipple 29      t   t   nil   t    )
  ( METAL1              net      16     outlineStipple 30      t   t   nil   nil  )
  ( METAL1              pin      16     outlineStipple 31      t   t   nil   t    )
  ( VIA1                drawing  17     solid          32      t   t   nil   t    )
  ( VIA1                net      17     solid          33      t   t   nil   nil  )
  ( METAL2              drawing  18     outlineStipple 34      t   t   nil   t    )
```

注意，在 Technology file 中所定義的每一個 Layer name 皆會對映一個 Layer number。有的 Layer name 會有 dg(drawing) 與 pn(pin) 兩種不同的屬性定義，主要的差別是 purpose 的定義不同，如 dg 是 252，而 pn 是 251。一般畫 Layout 是使用 dg 的，只有在宣告為 pin 腳時才使用 pn。

根據 Technology file 中所定義的 Layer name 與 Layout rule 中的 Layer name 之名稱對映。

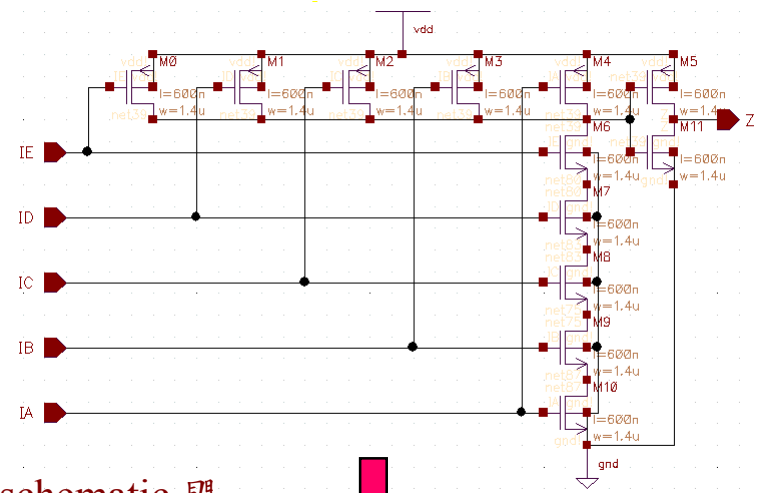
NWELL dg	NW (N Well)
THIN dg	OD (thin oxide)
PPIMP dg	PP (P implantation)
NPIMP dg	NP(N implantation)
GPOLY dg	PO (poly)
METAL1 dg	M1 (metal 1)
VIA1 dg	VIA (VIA 1)
CONT dg	CO (contact)
METAL2 dg	M2 (metal 2)
backgro dg	
PASS dg	
text2 dg	
ESD dg	
resisto dg	
PYGLBL dg	
METAL2 pn	
MT2LBL dg	
METAL1 pn	
GPOLY pn	
MT1LBL dg	
prBound dg	

Set Grid

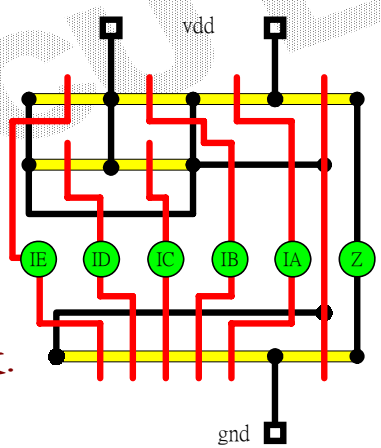


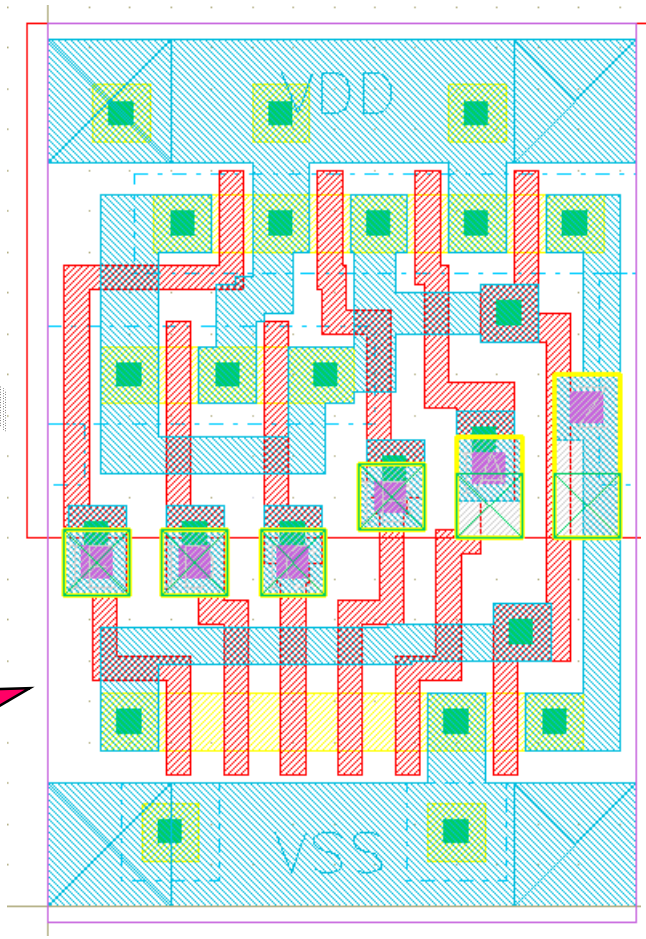
開啟Display Options 來設定 Grid。一般 Grid 的設法為所有 layout rules 裡的最小單位，在此設為 0.05。若是 Grid 沒有設好，則在畫 layout 時將會有很多的困擾，更嚴重可能會有 error 的情形，所以每次開始畫 layout 時請務必先做設定。

Start Layout



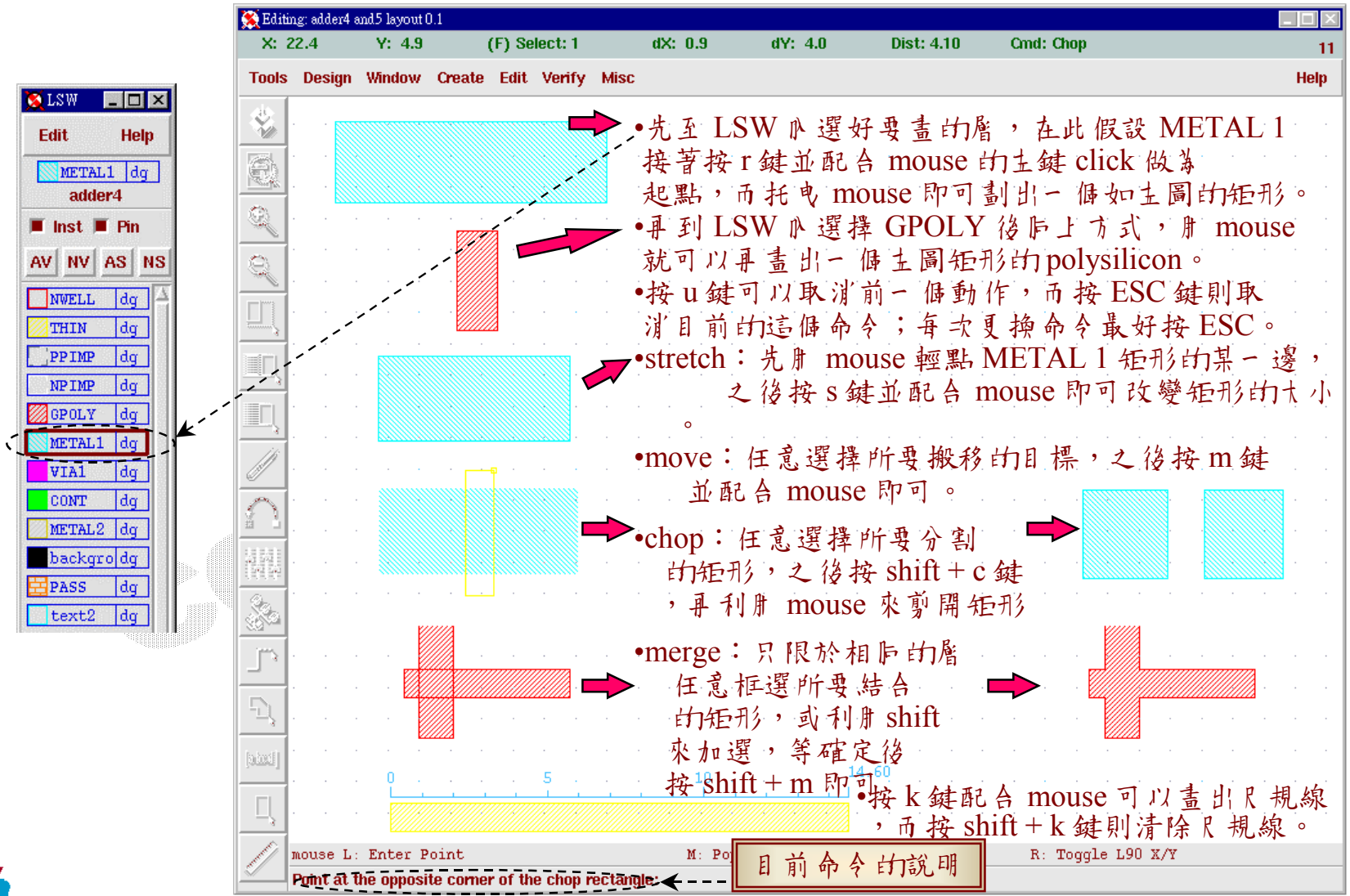
從一個 schematic 開始，設計到 layout，最好事先做好佈局的規劃，如右邊條形圖(symbolic diagram)，先簡單粗略的擺設，使其能善用空間，做到使用最少的pitch 數.





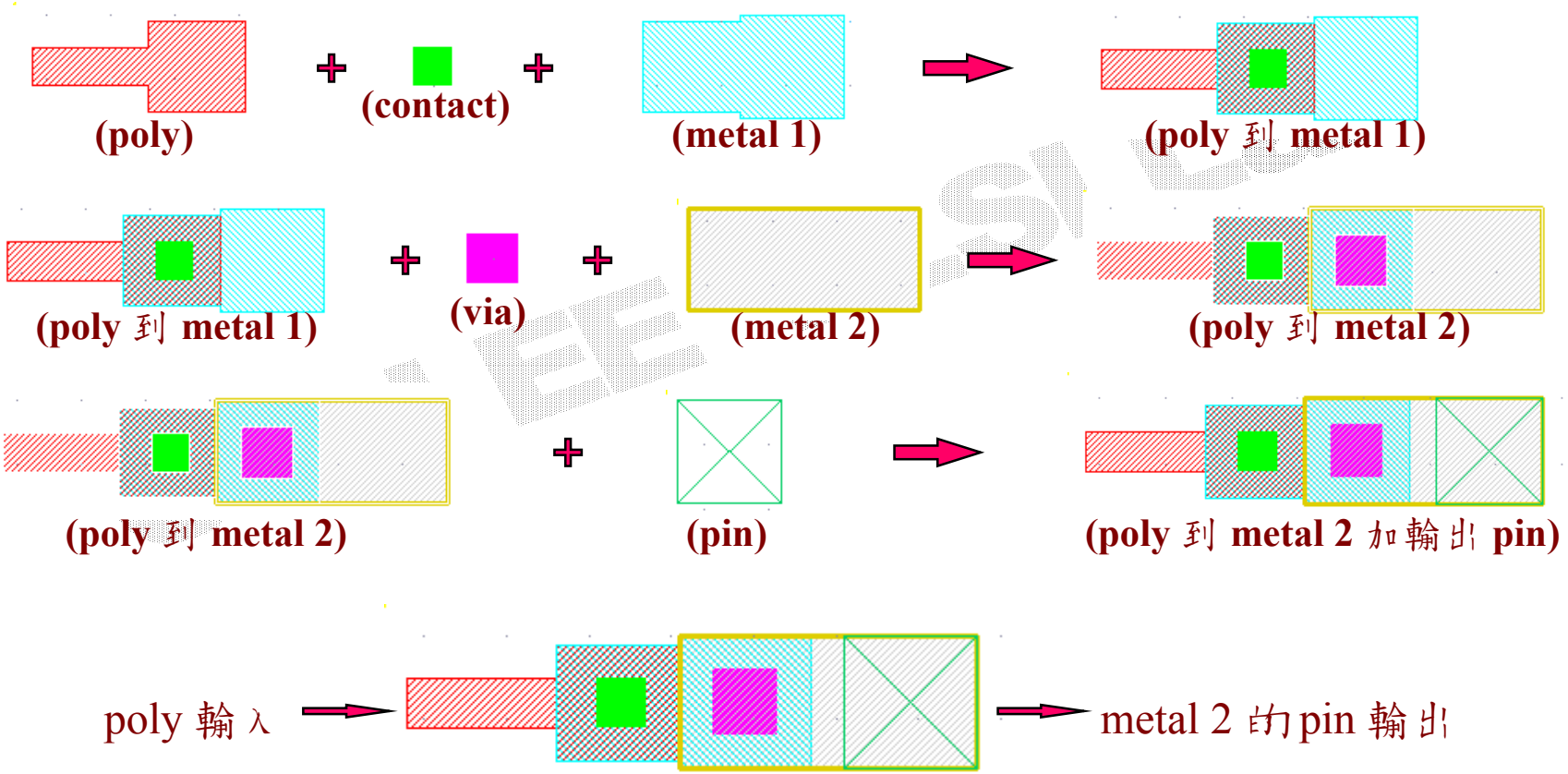
一個 pitch 最多只能存在一個輸出或輸入的 pin。此為“and5”，共有 6 個輸出入 pin，而 layout 的結果也只使用 6 個 pitch 數，所以最省空間.

Practice Layout (I)



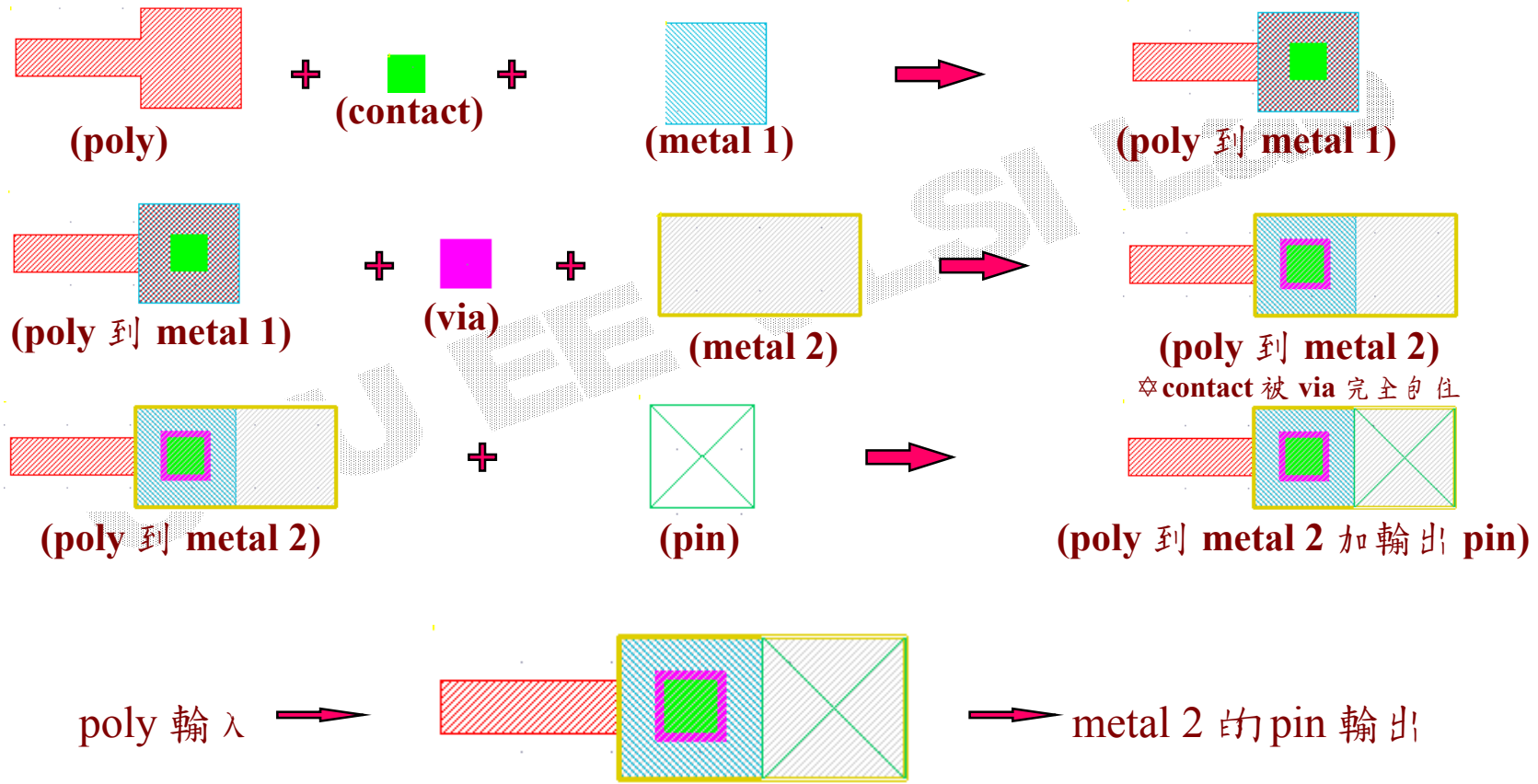
Practice Layout (II)

畫 layout 必須有層次的先後關念，例如一個訊號從poly 輸入，而從metal 2 輸出，就必須先畫 poly 再疊上 contact，再疊上 metal 1，再疊上 via，最後再疊上 metal 2。其過程缺一不可。如下所示：

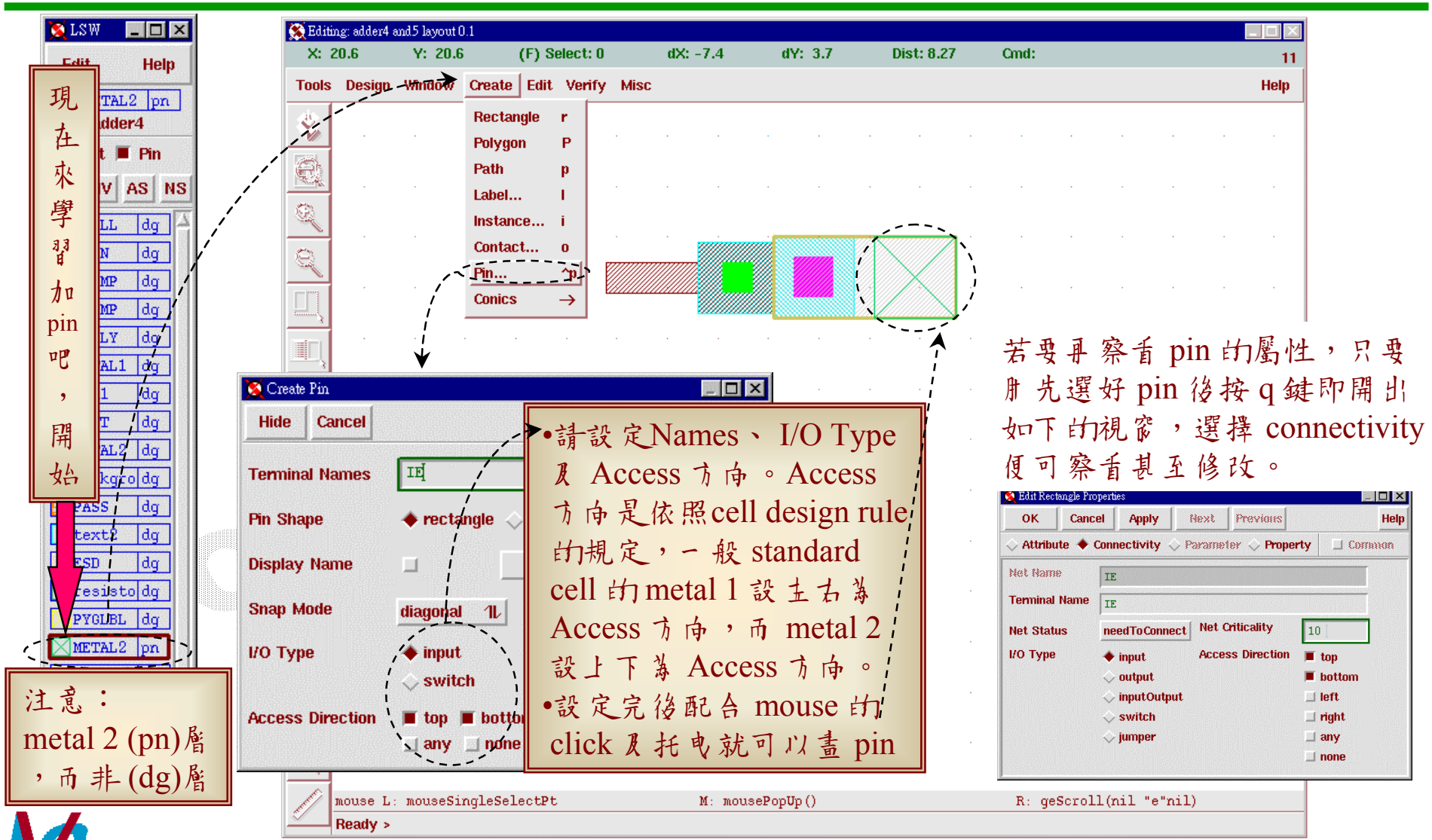


Practice Layout (III)

另一種方法比較節省面積，就是via與contact重疊在一起。此樣的例子，如一個訊號從poly輸入，而從metal 2輸出。如下所示：

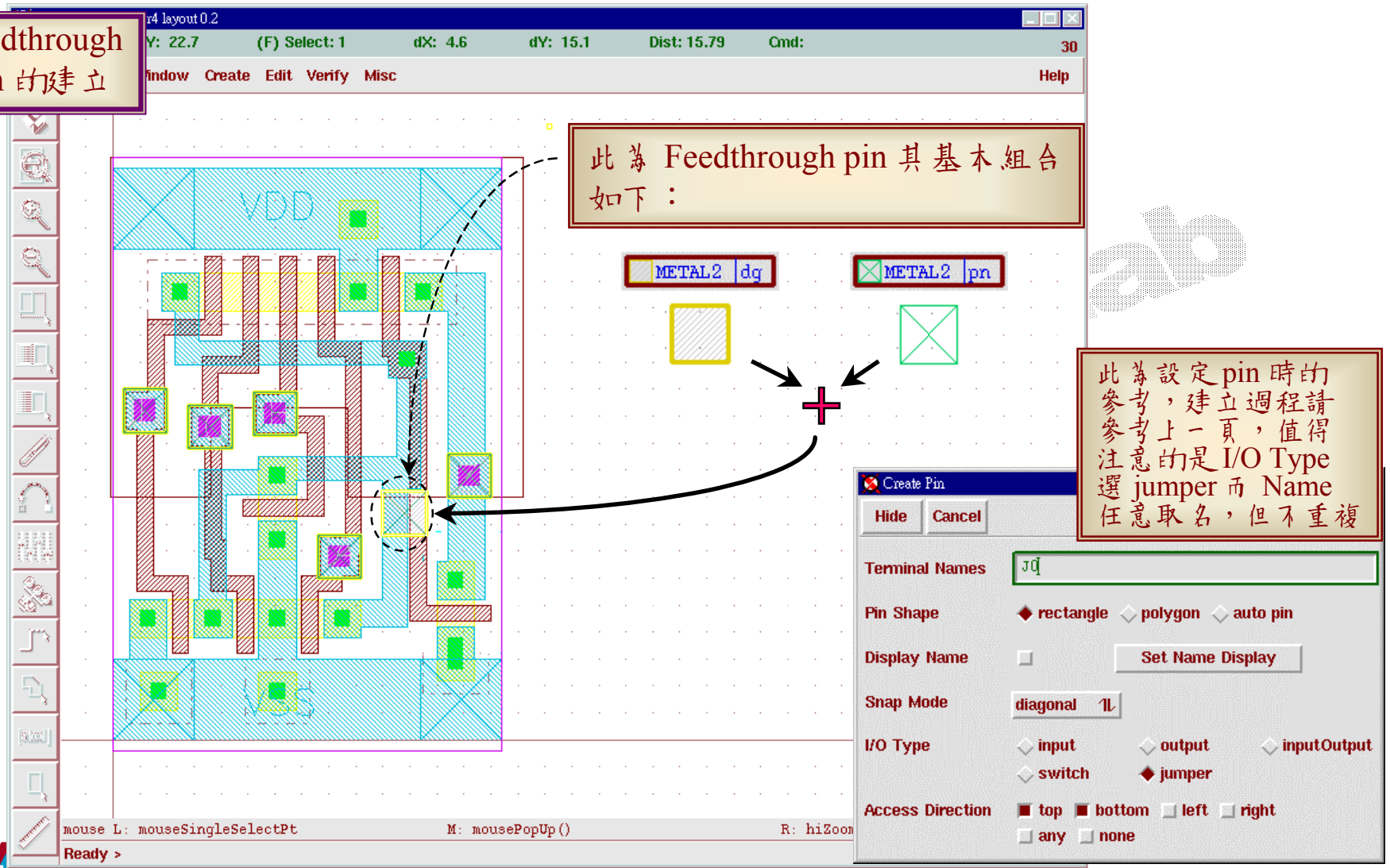


Practice Layout (IV)



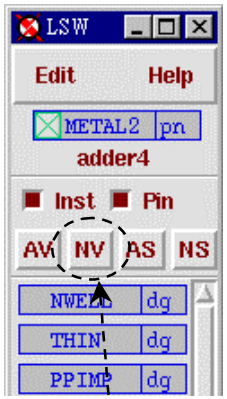
Practice Layout (V)

Feedthrough pin 的建立

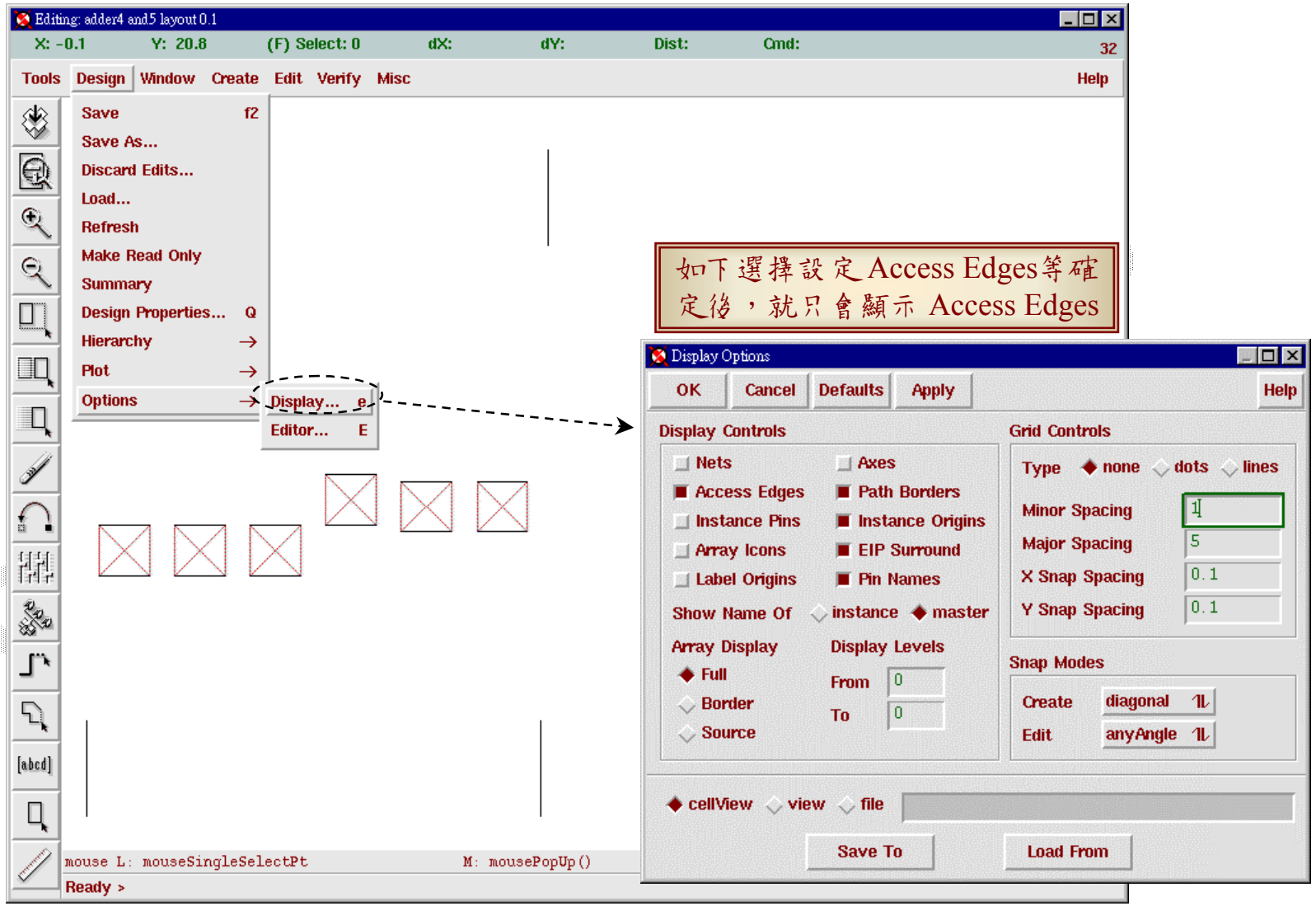


Practice Layout (VII)

檢查 pin 腳輸出的方向



先選除目前選用的層外其餘層皆不會顯示出來的方式。

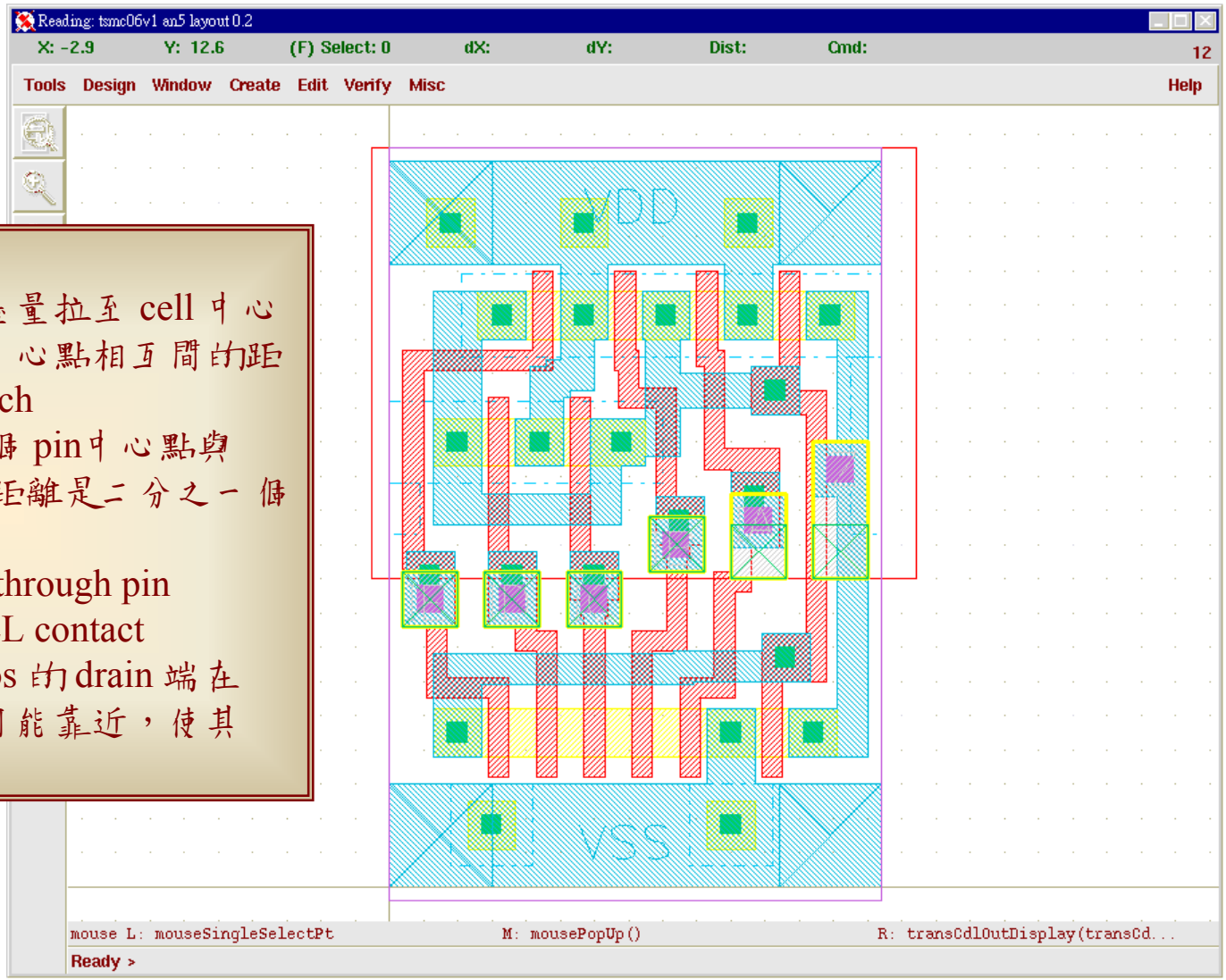


如下選擇設定 Access Edges等確定後，就只會顯示 Access Edges

Finished Layout

一般注意事項：

- 輸出入 pin 盡量拉至 cell 中心
- 兩個 pin 的中心點相互間的距離是一個 pitch
- 最外面的二個 pin中心點與 boundary 的距離是二分之一個 pitch
- 盡量加 Feedthrough pin
- 盡量加 WELL contact
- pmos 及 nmos 的drain 端在 layout 時盡可能靠近，使其面積為最小



Verifications

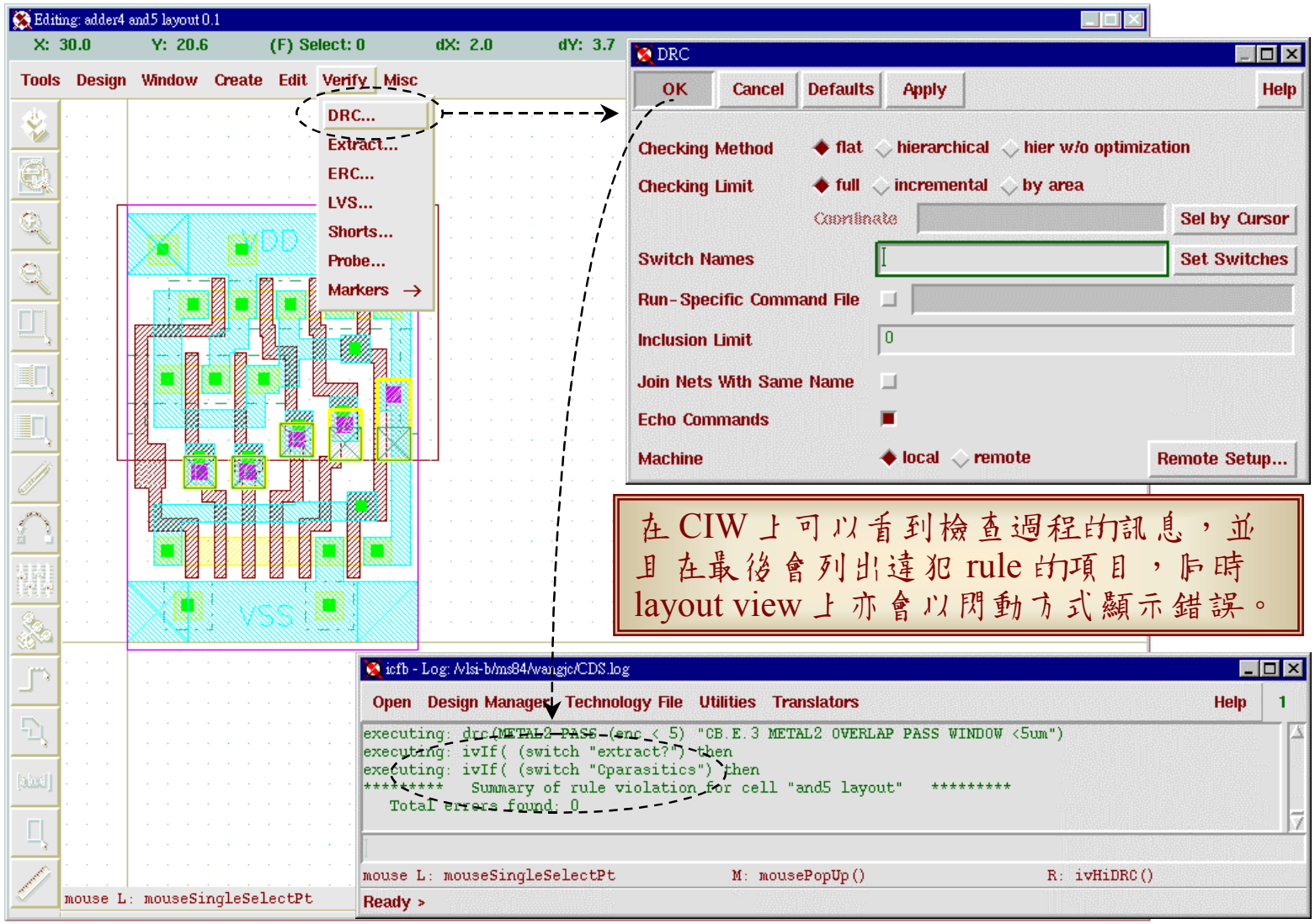
Ckt layout 完成後所須作的驗証如下：

- DRC (Design Rule Check)：
  對 IC 的佈局(layout) 作幾何空間的檢查以確保線路能夠被特定的製程技術所實現。
- ERC (Electrical Rule Check)：
  檢查 power, ground 的 short, floating device, floating net 等指定的電氣特性。
- LVS (Layout Versus Schematic)：
  將 layout 與 schematic 作比對，以檢查電路的連接，與 MOS 的 Length、Width 值是否配。
- LPE (Layout Parameter Extarction)：
  從 layout database extract 電氣參數 (如 MOS 的 W、L 值，BJT，diode 的 area，perimeter，node 的 parastic cap.)，並以 HSPICE netlist 方式表示電路。

Diva Versus Dracula

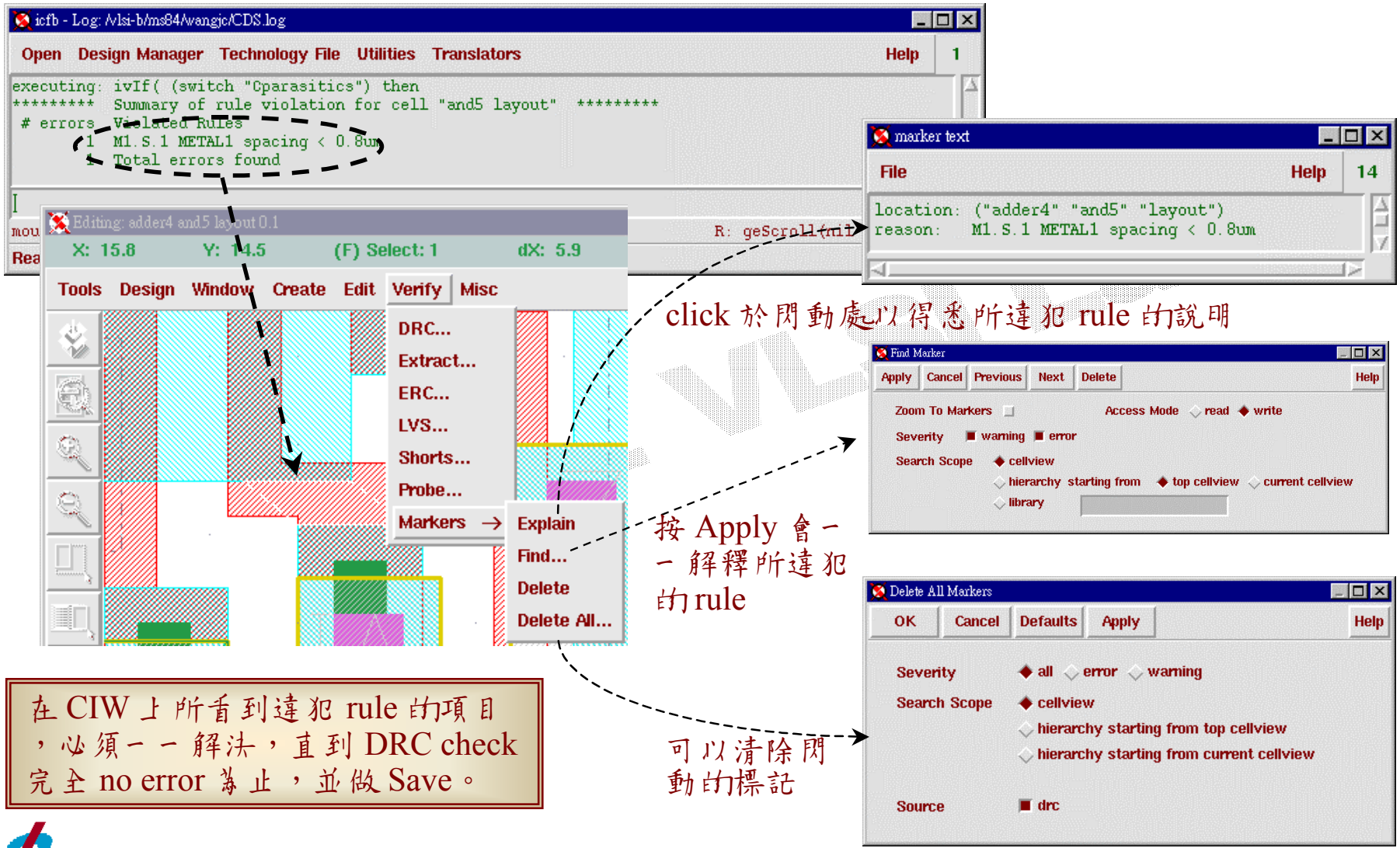
- 光罩式製程在IC製過程中是相當昂貴的，所以佈局驗証的重要性自然是不可言喻，一般佈局驗証包括 DRC(Design Rule Check)，ERC(Electric Rule Check) 及 LVS(Layout vs. Schematic 的比較)。
- Cadence 擁有兩套佈局驗系統：
  - ➢ Opus 中的Diva 是on-line 交談式，具有快速驗証小 cell 及與 Opus 完整整合的優點，缺點是對大晶片可能無法作完整驗証，又一般來說，Diva 之 run time 較 Dracula 長 。
  - ➢ Dracula 是使用 batch-job 方式，Dracula (吸血鬼) 被公認是佈局驗証的標準，幾乎全世界所有 IC 公司都拿它來作 sign-off 的憑據。
- 一般 Diva 用於對小 cell 或中型 block 的layout 設計驗証，而 whole chip 的最後驗証則一定要交由 Dracula 處理。

Diva DRC (I)



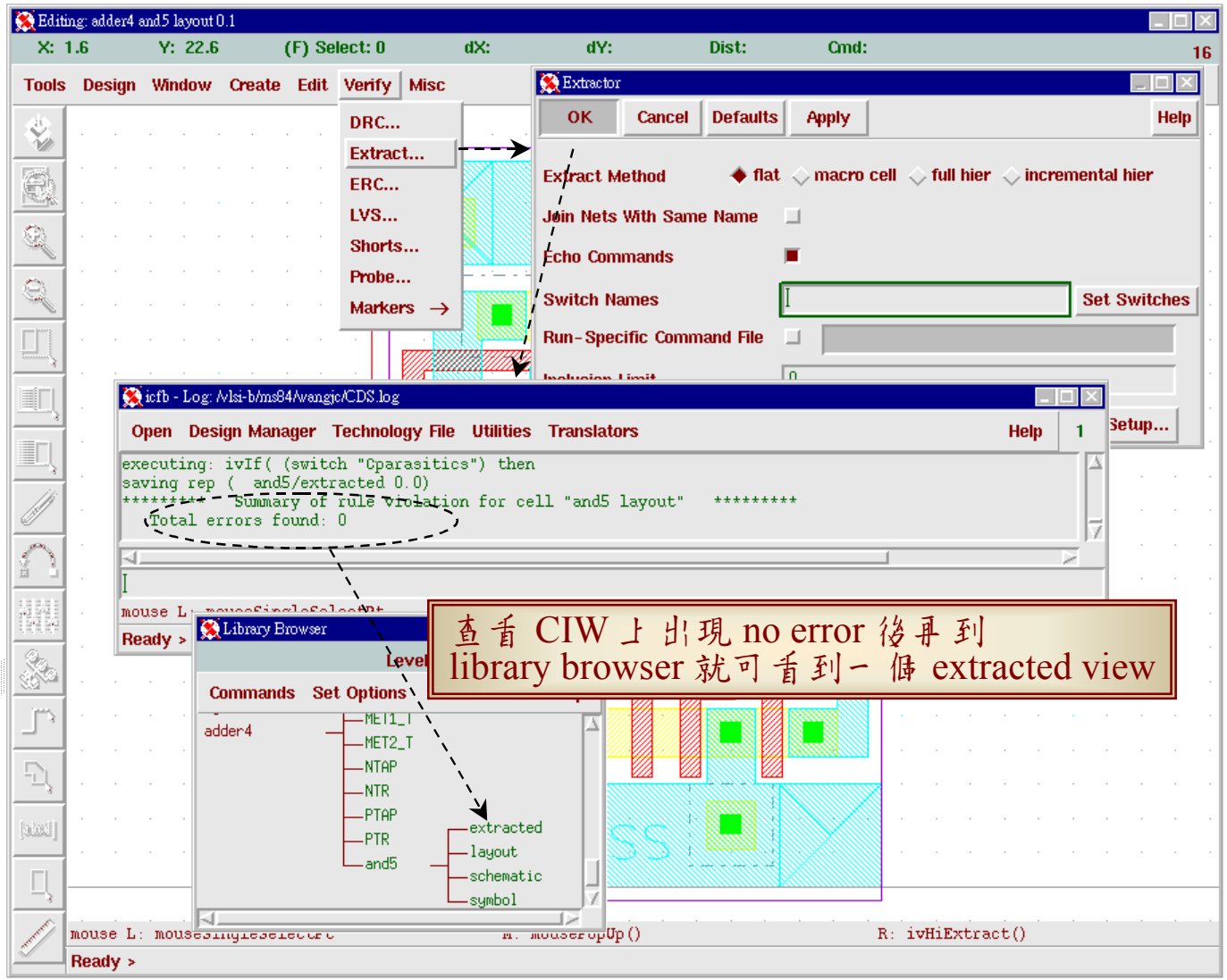
在 CIW 上可以看到檢查過程的訊息，並且在最後會列出違犯 rule 的項目，同時 layout view 上亦會以閃動方式顯示錯誤。

Diva DRC (II)

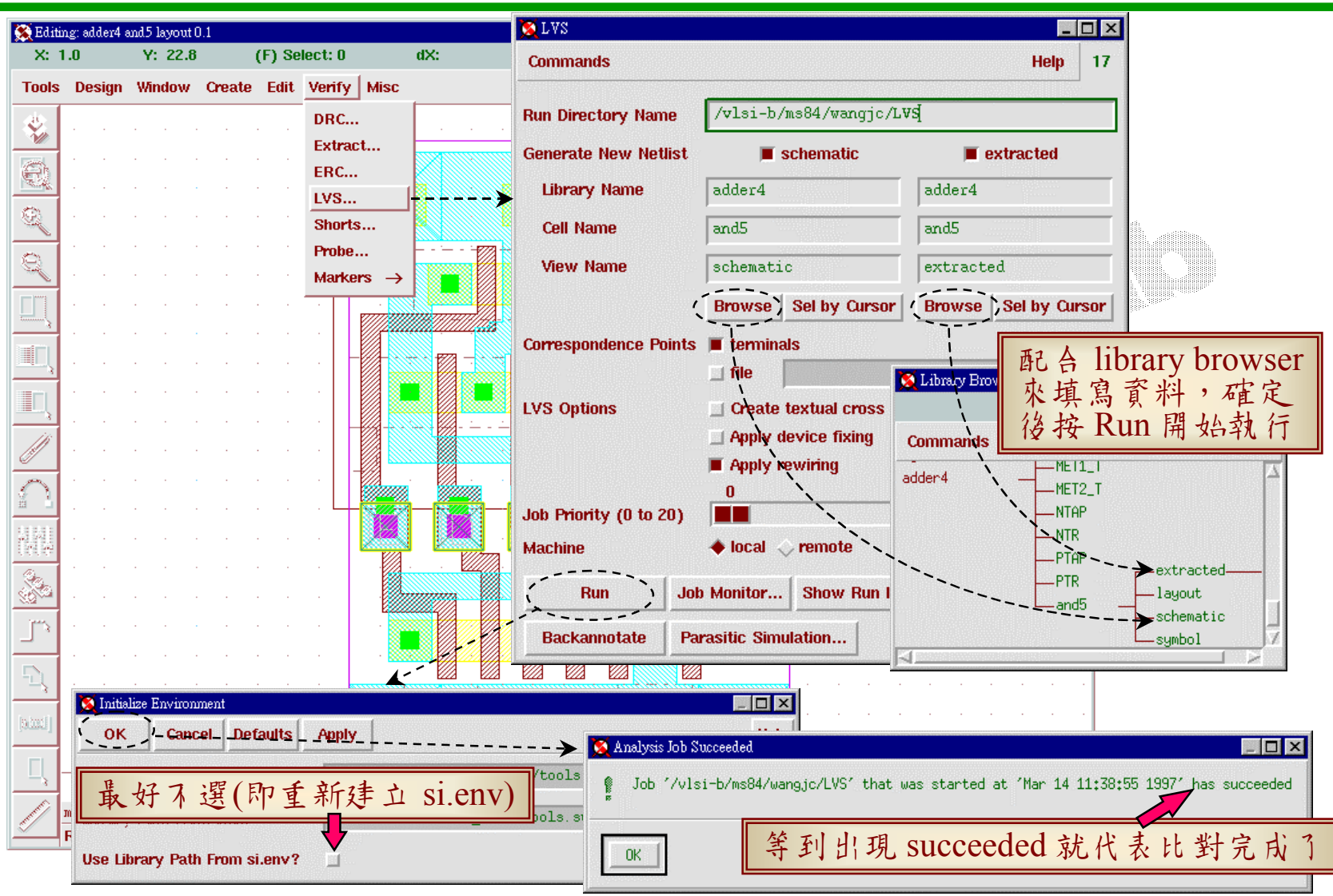

icfb - Log: /vlsi-b/ms84/wangjc/CDS.log
Open Design Manager Technology File Utilities Translators Help 1
executing: ivIf((switch "Cparasitics") then
********* Summary of rule violation for cell "and5 layout" *********
# errors Violated Rules
1 M1.S.1 METAL1 spacing < 0.8um
1 Total errors found
Editing: adder4 and5 layout 0.1
X: 15.8 Y: 14.5 (F) Select: 1 dX: 5.9
Tools Design Window Create Edit Verify Misc
DRC...
Extract...
ERC...
LVS...
Shorts...
Probe...
Markers
Explain
Find...
Delete
Delete All...
marker text
File Help 14
location: ("adder4" "and5" "layout")
reason: M1.S.1 METAL1 spacing < 0.8um
click 於閃動處以得悉所違犯 rule 的說明
Find Marker
Apply Cancel Previous Next Delete Help
Zoom To Markers
Access Mode read write
Severity warning error
Search Scope cellview
hierarchy starting from top cellview current cellview
library
按 Apply 會一一解釋所違犯的 rule
Delete All Markers
OK Cancel Defaults Apply Help
Severity all error warning
Search Scope cellview
hierarchy starting from top cellview
hierarchy starting from current cellview
Source drc
可以清除閃動的標記
在 CIW 上所看到違犯 rule 的項目，必須一一解決，直到 DRC check 完全 no error 為止，並做 Save。

Create Extracted View

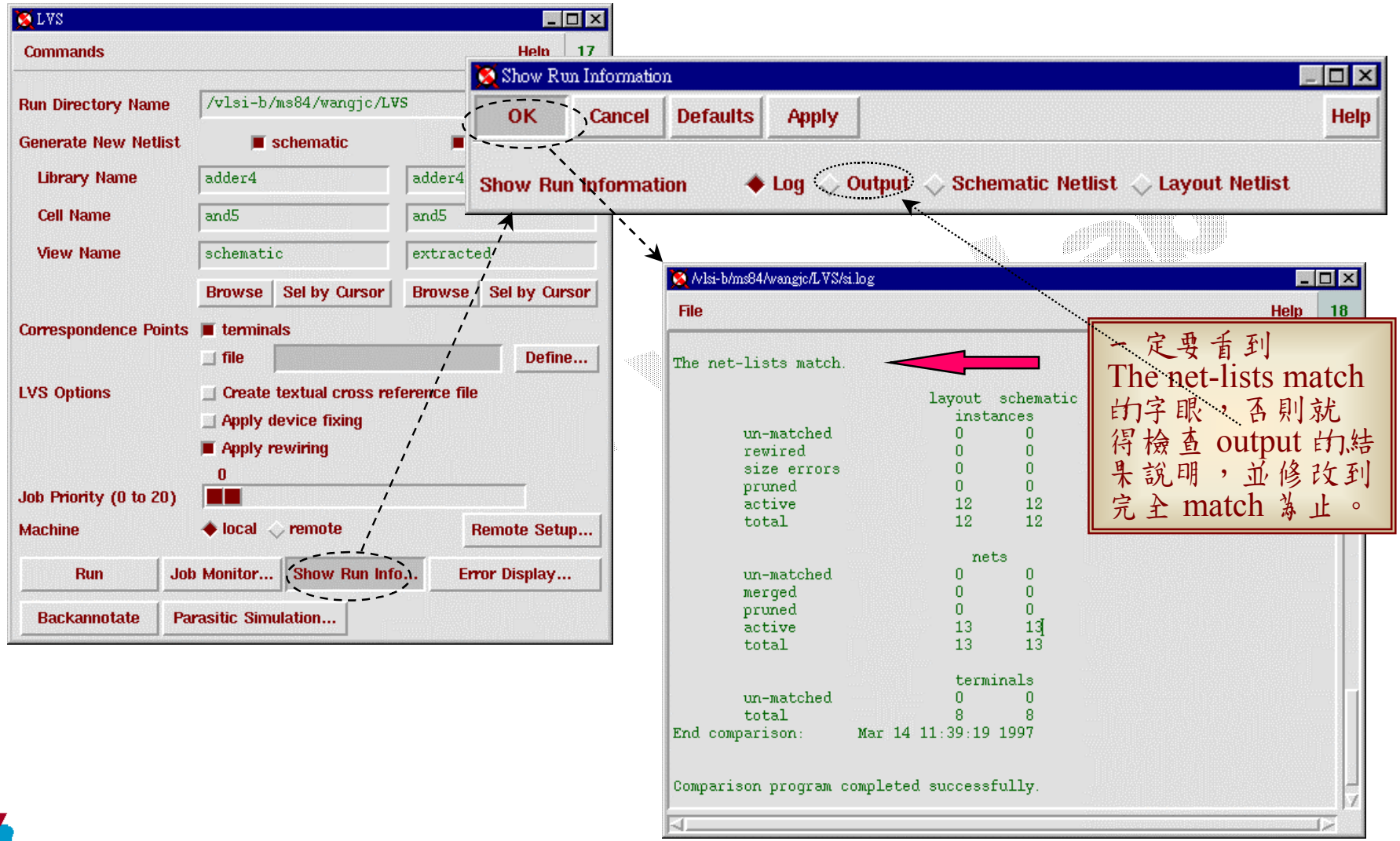
Extract 主要是抽取出一些參數來提供 LVS 時做比對用。



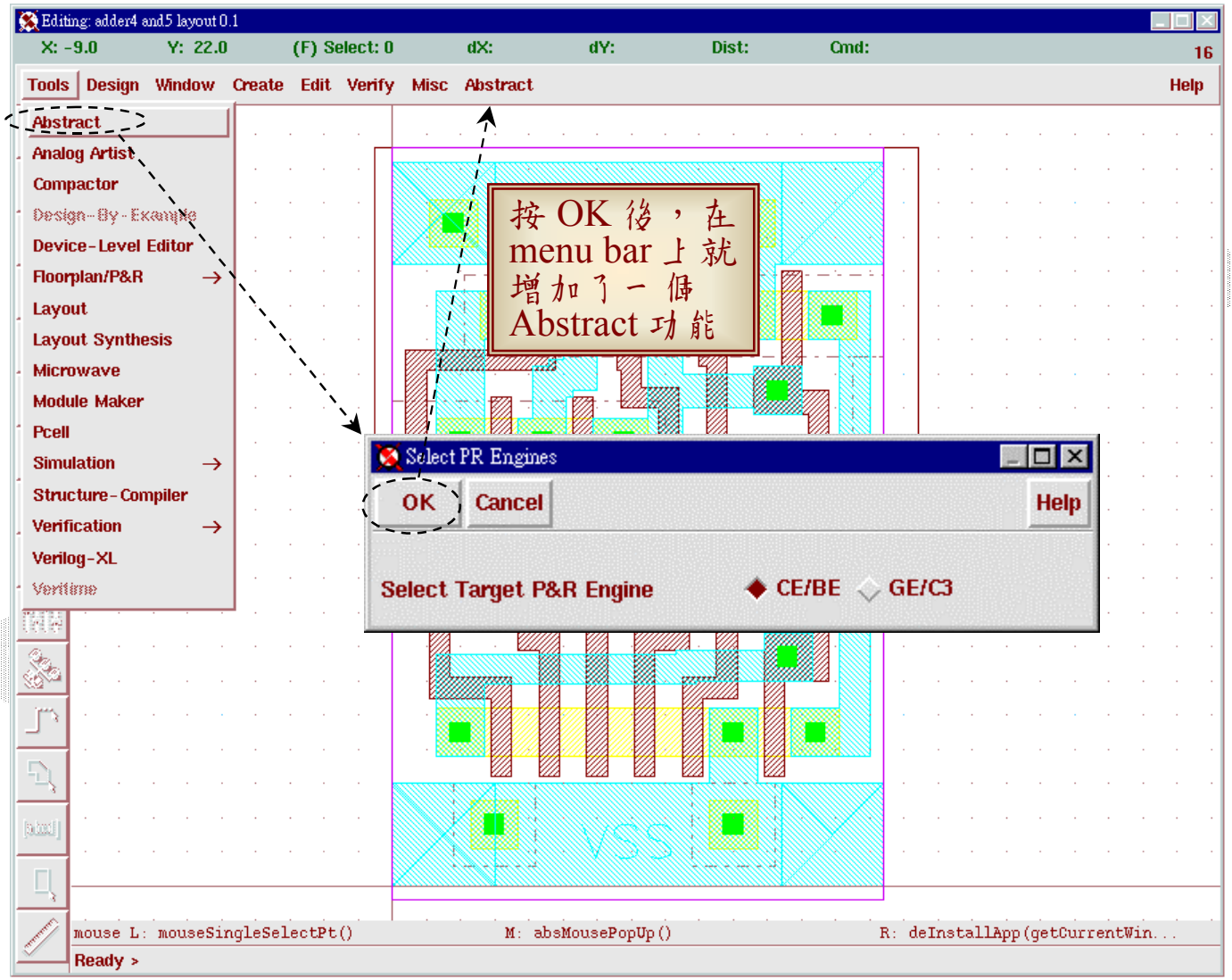
Diva LVS (I)


Editing: adder4 and5 layout 0.1
X: 1.0
Y: 22.8
(F) Select: 0
dX:
Tools
Design
Window
Create
Edit
Verify
Misc
DRC...
Extract...
ERC...
LVS...
Shorts...
Probe...
Markers
LVS
Commands
Help
17
Run Directory Name
/vlsi-b/ms84/wangjc/LVS
Generate New Netlist
schematic
extracted
Library Name
adder4
adder4
Cell Name
and5
and5
View Name
schematic
extracted
Browse
Sel by Cursor
Browse
Sel by Cursor
Correspondence Points
terminals
file
LVS Options
Create textual cross
Apply device fixing
Apply rewiring
0
Job Priority (0 to 20)
Machine
local
remote
Run
Job Monitor...
Show Run I
Backannotate
Parasitic Simulation...
Library Brov
Commands
adder4
MET1_T
MET2_T
NTAP
NTR
PTAP
PTR
and5
extracted
layout
schematic
symbol
配合 library browser 來填寫資料，確定後按 Run 開始執行
Initialize Environment
OK
Cancel
Defaults
Apply
Use Library Path From si.env?
最好不選(即重新建立 si.env)
Analysis Job Succeeded
Job '/vlsi-b/ms84/wangjc/LVS' that was started at 'Mar 14 11:38:55 1997' has succeeded
OK
等到出現 succeeded 就代表比對完成了

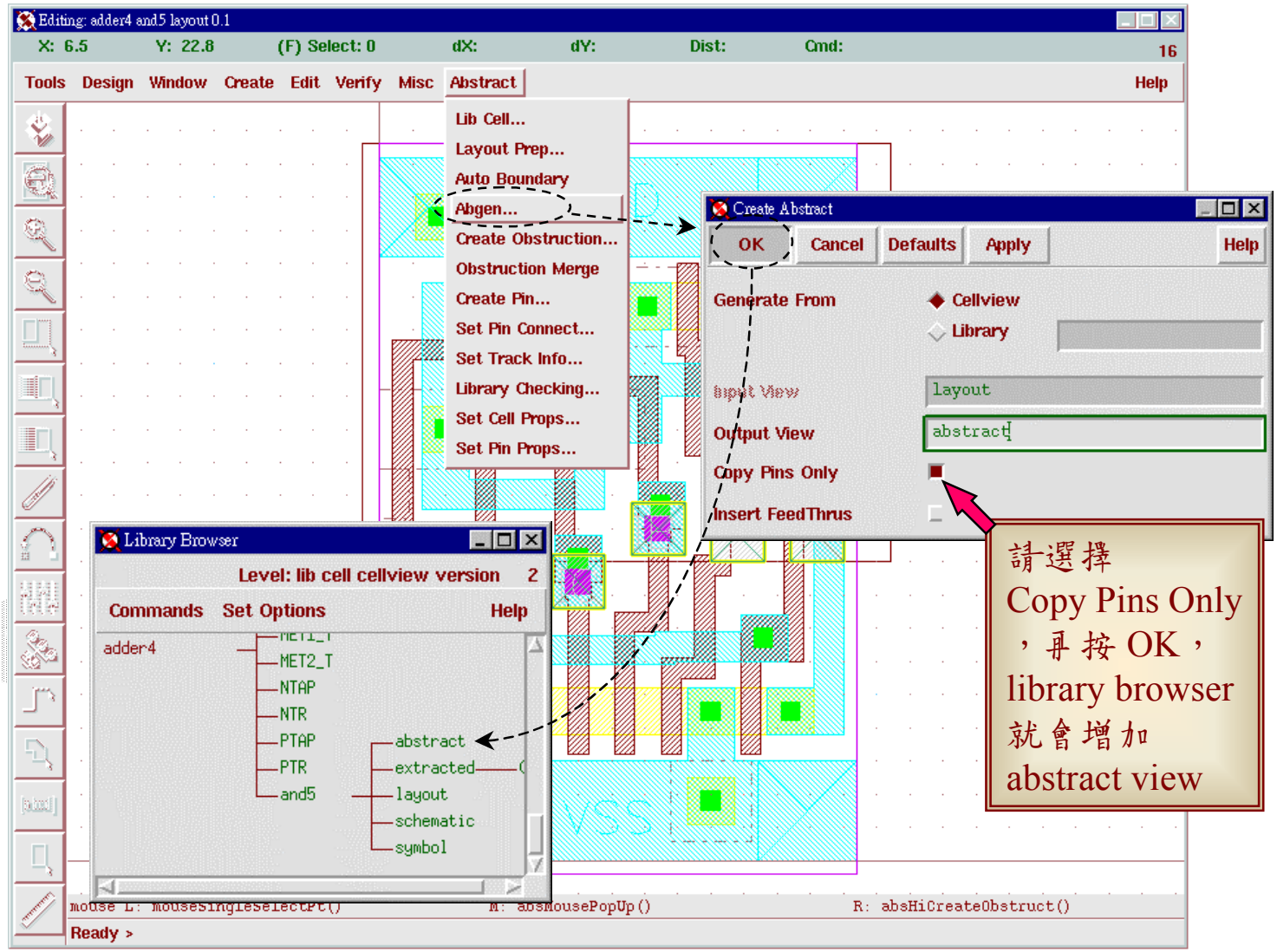
Diva LVS (II)


LVS
Commands
Help
17
Run Directory Name
/vlsi-b/ms84/wangjc/LVS
Generate New Netlist
schematic
Library Name
adder4
adder4
Cell Name
and5
and5
View Name
schematic
extracted
Browse
Sel by Cursor
Browse
Sel by Cursor
Correspondence Points
terminals
file
Define...
LVS Options
Create textual cross reference file
Apply device fixing
Apply rewiring
0
Job Priority (0 to 20)
Machine
local
remote
Remote Setup...
Run
Job Monitor...
Show Run Info...
Error Display...
Backannotate
Parasitic Simulation...
Show Run Information
OK
Cancel
Defaults
Apply
Help
Show Run Information
Log
Output
Schematic Netlist
Layout Netlist
/vlsi-b/ms84/wangjc/LVS/si.log
File
Help
18
The net-lists match.
layout schematic
instances
un-matched 0 0
rewired 0 0
size errors 0 0
pruned 0 0
active 12 12
total 12 12
nets
un-matched 0 0
merged 0 0
pruned 0 0
active 13 13
total 13 13
terminals
un-matched 0 0
total 8 8
End comparison: Mar 14 11:39:19 1997
Comparison program completed successfully.
一定要看到
The net-lists match
的字眼，否則就
得檢查 output 的結
果說明，並修改到
完全 match 為止。

Create Abstract View (I)

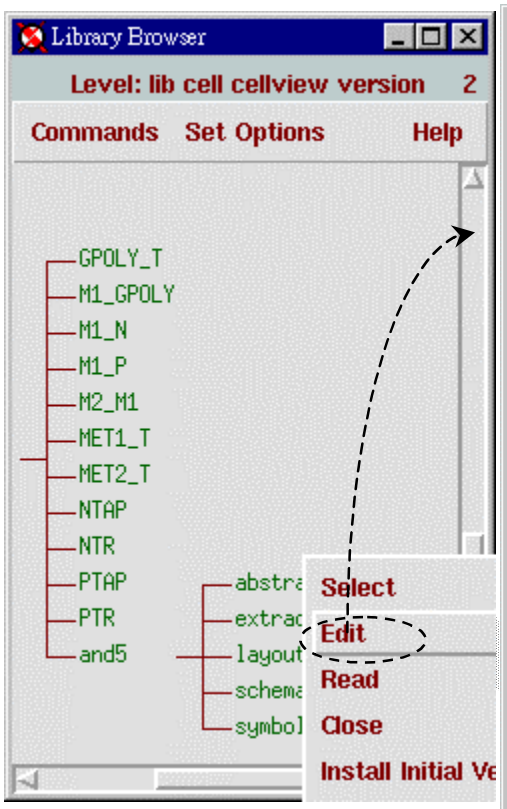


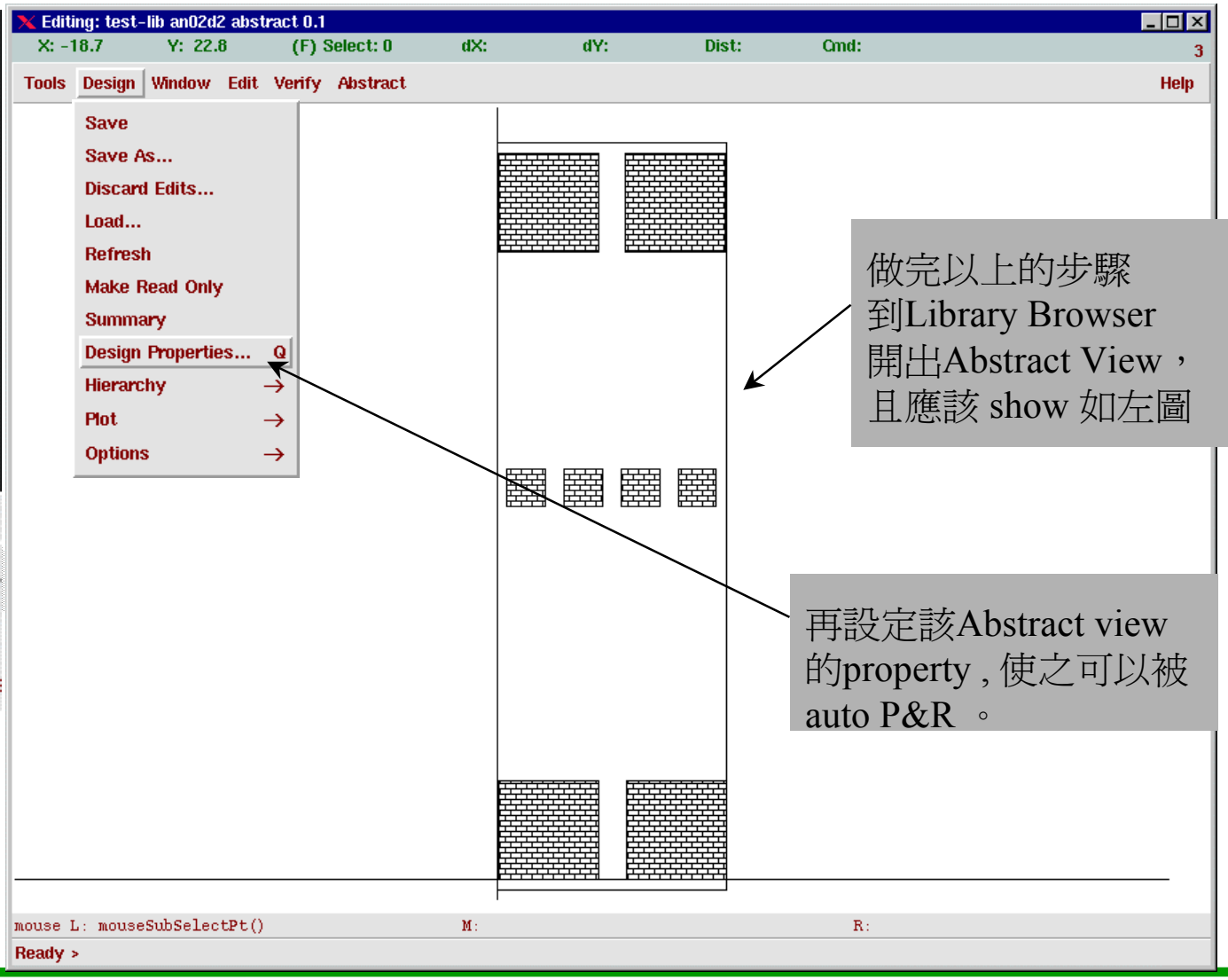
Create Abstract View (II)



請選擇 Copy Pins Only，再按 OK，library browser 就會增加 abstract view

Abstract View Change Property (I)

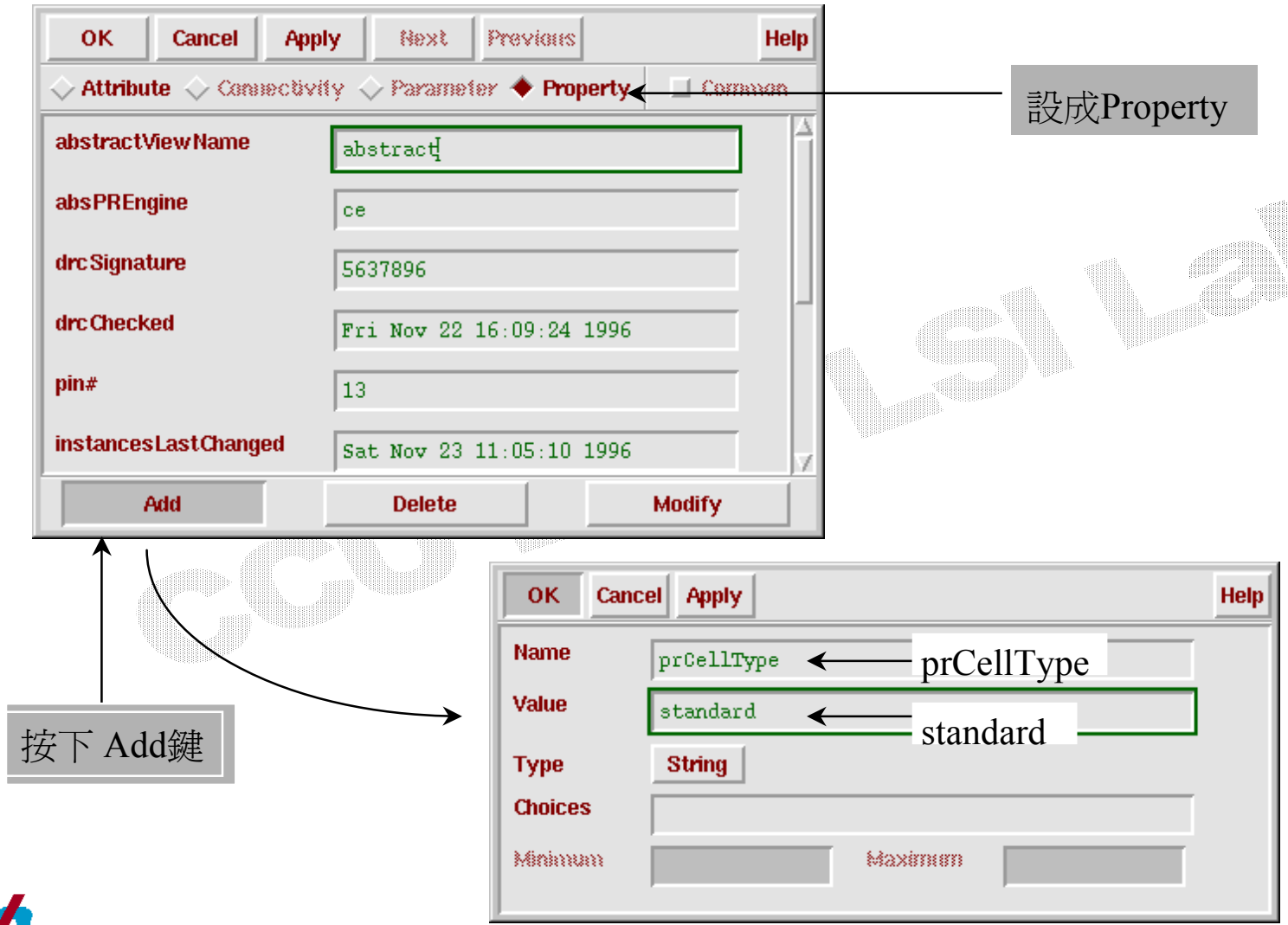




做完以上的步驟
到Library Browser
開出Abstract View，
且應該 show 如左圖

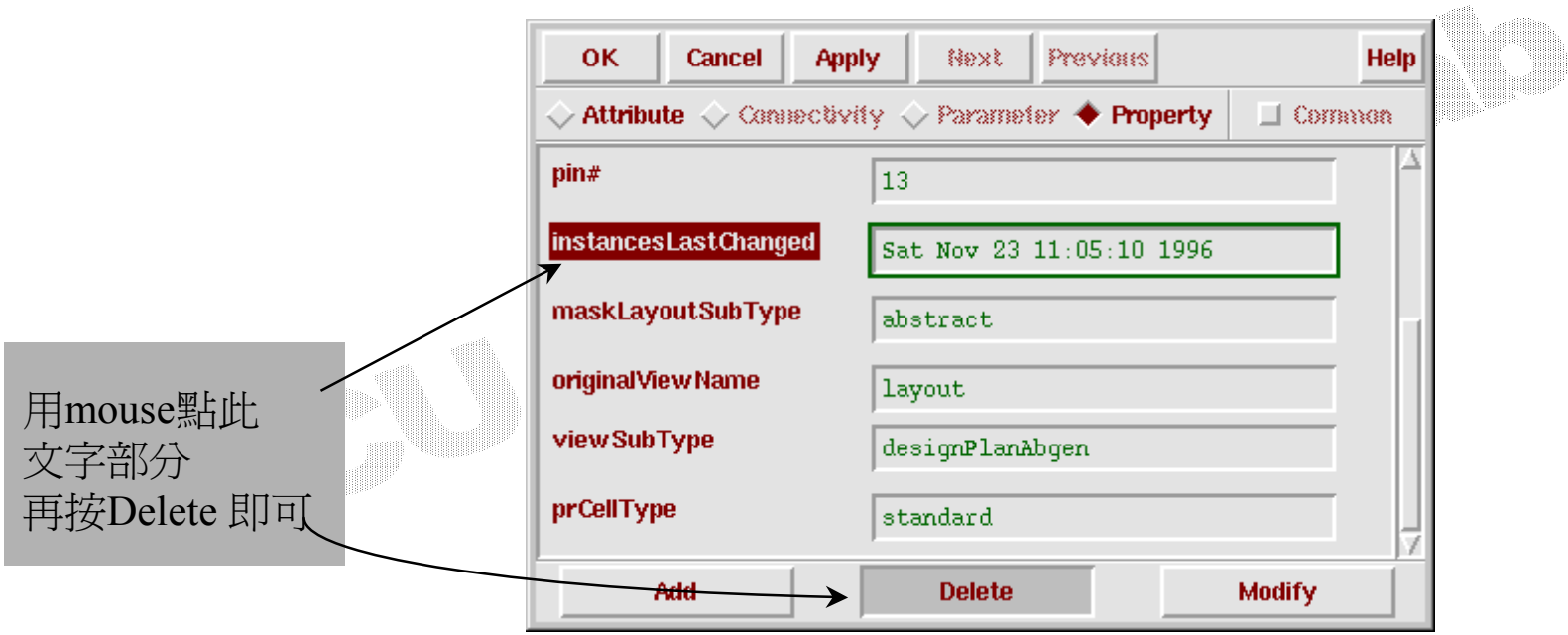
再設定該Abstract view
的property , 使之可以被
auto P&R 。

Abstract View Change Property (II)



Abstract View Change Property (III)

★欲去掉不必要的 property information



★設定完後，再 Check & Save