Clock Multiplication Techniques Using Digital Multiplying Delay-Locked Loops

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***Abstract*—A highly-digital clock multiplication architecture that achieves excellent jitter and mitigates supply noise is presented. The proposed architecture utilizes a calibration-free digital multiplying delay-locked loop (MDLL) to decouple the tradeoff between time-to-digital converter (TDC) resolution and oscillator phase noise in digital phase-locked loops (PLLs). Both reduction in jitter accumulation down to sub-picosecond levels and improved supply noise rejection over conventional PLL architectures is demonstrated with low power consumption. A digital PLL that employs a 1-bit TDC and a low power regulator that seeks to improve supply noise immunity without increasing loop delay is presented and used to compare with the proposed MDLL. The prototype MDLL and DPLL chips are fabricated in a 0.13 μm CMOS technology and operate from a nominal 1.1 V supply. The proposed MDLL achieves an integrated jitter of 400 fs rms at 1.5 GHz output frequency from a 375 MHz reference clock, while consuming 890 μW. The worst-case supply noise sensitivity of the MDLL is 20 fs_{pp}/mV_{pp} which translates to a jitter degradation of 3.8 ps in the presence of 200 mV supply noise. The proposed clock multipliers occupy active die areas of 0.25 mm^2 and 0.2 mm^2 for the MDLL and DPLL, respectively.**

***Index Terms*—Calibration-free, clock multiplier, delta-sigma DAC, deterministic jitter, digital loop filter, digital MDLL, digital PLL, digitally-controlled oscillator (DCO), DPLL, jitter, multiplying delay-locked loop (MDLL), 1-bit TDC, phase-locked loop (PLL), power efficient, power supply noise, reference spur, ring oscillator, supply noise sensitively, TDC-oscillator tradeoff, time-to-digital converter (TDC), transfer function, voltage controlled oscillator (VCO).**

I. Introduction

HIGHLY digital clock generator architectures, most commonly implemented using digital phase-locked loops (DPLLs), are evolving as the preferred means for synthesizing high frequency on-chip clocks [1]–[7]. By obviating the need for a large loop filter capacitor and high performance charge-pump, DPLLs offer many advantages over classical charge-pump PLLs. Their main benefits include small area, reduced sensitivity to analog circuit imperfections, immunity to process, voltage, and temperature (PVT) variations, and easier scalability to newer processes. Because the digital loop filter can be reconfigured dynamically, DPLLs offer flexibility in setting their loop response and optimizing locking behavior [6], [8].

The block diagram of a classical digital PLL is shown in Fig. 1(a). It is composed of a time-to-digital converter (TDC), a digital loop filter (DLF), a supply regulated digitally controlled oscillator (DCO), and a feedback divider. The TDC generates a digital word proportional to the phase difference between the reference (REF) and feedback clock. The TDC output is fed to the DLF, which consists of proportional and integral paths whose gains are denoted as K_{BB} and K_I, respectively. The proportional-integral filter realizes the Type-II PLL response, and a digital-to-analog converter (DAC) interfaces the DLF to the voltage controlled oscillator (VCO). The output of the DCO is divided by the feedback divider and fed to the TDC input.

In spite of the many advantages of DPLLs, it is difficult to achieve low jitter compared to that of analog PLLs. This is due to different conflicting design requirements. Primary among them is the TDC/DCO coupled noise bandwidth tradeoff, which is illustrated in Fig. 1(b). The TDC quantization noise is low-pass filtered, while the oscillator phase noise is high-pass filtered. This conflicting bandwidth requirement poses several design challenges to simultaneously suppress TDC quantization error and oscillator phase noise (see Fig. 1(c)). For instance, a lower bandwidth suppresses TDC quantization error but cannot adequately suppress oscillator phase noise and vice versa. Consequently, either a high resolution TDC or a low noise oscillator is needed to achieve low jitter at the expense of large power dissipation and area [7]. In [1] a low phase noise LC-DCO is combined with a very low DPLL bandwidth to suppress TDC quantization error. In contrast to this approach, we propose to decouple the TDC/DCO noise bandwidth tradeoff by using a digital multiplying delay-locked loop (MDLL) and use a low resolution TDC and low power oscillator to achieve low jitter.

Jitter is also degraded by supply noise in the oscillator, which often limits the overall jitter performance of a PLL embedded in a large SoC. A low-dropout regulator is commonly used to shield the oscillator from supply noise at the expense of additional area, power, and voltage headroom [9]–[13]. Since the worst-case jitter sensitivity occurs in the vicinity of the DPLL bandwidth, the regulated-PLL power supply noise rejection (PSNR) greatly depends on the regulator to PLL bandwidth ratio. For reasonable suppression, the regulator bandwidth must

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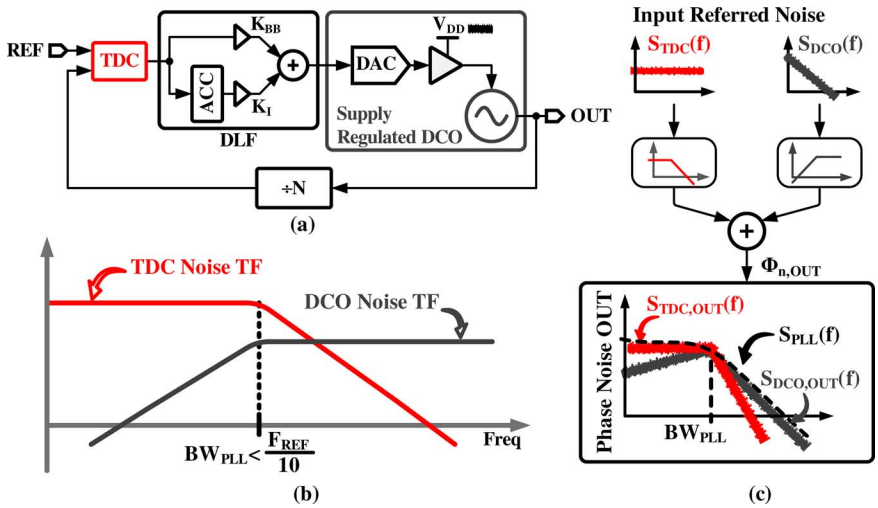

Fig. 1. (a) Supply regulated digital PLL block diagram, (b) coupled TDC/DCO bandwidth tradeoff in DPLLs, and (c) the transfer functions from noise sources to output phase noise.

be made much larger than the PLL bandwidth. For instance, to achieve a modest 8 dB of worst-case PSNR, the regulator bandwidth must be fifty times the PLL bandwidth [9]. Therefore, designing the regulator with such a wide bandwidth increases power dissipation.

Additionally, the highly non-linear nature of digital PLLs (DPLLs) makes their output jitter sensitive to loop delay and noise (reference clock jitter). As a result, DPLL design optimization for low jitter becomes very complex [14]. Adding a supply regulator as shown in Fig. 1(a), increases loop delay and further complicates the design. Because the worst-case jitter sensitivity in an analog PLL occurs in the vicinity of its bandwidth, the regulator bandwidth can be appropriately chosen to meet the noise suppression requirements [9]. Unfortunately, the loop delay makes it difficult to predict supply noise to output jitter transfer characteristics of a DPLL. As a result, the regulator bandwidth must be large enough such that it does not impact the loop delay, which mandates it to be much higher than that used in an analog PLL. Using the regulator outside the PLL loop eliminates the impact of loop dynamics on supply noise rejection properties, but this reduces the tuning range of the oscillator. Additionally, generating the regulator's reference voltage requires either using a band-gap voltage reference circuit or a low bandwidth passive RC filter.

To overcome the drawbacks of DPLLs, a new digital MDLL (DMDLL) clock multiplier that seeks reduction of both random and deterministic jitter using a highly digital implementation is presented[15]. The proposed DMDLL achieves sub-picosecond jitter without either using a high resolution TDC or low phase noise DCO. By lowering the MDLL bandwidth aggressively to suppress TDC quantization error, a simple 1-bit TDC is utilized without any oscillator phase noise penalty. The MDLL also demonstrates an outstanding supply noise rejection over a wide operating range using a low-power replica-biased regulator. Implemented in a 0.13 μm CMOS technology, the prototype DMDLL achieves an integrated rms jitter of 400 fs, and a worst case supply noise sensitivity of less than 20 $\mathrm{fs_{pp}/mV_{pp}}$ (3.8 ps in the presence of 200 mV supply noise) at 1.5 GHz output frequency while consuming only 890 μW from a nominal 1.1 V supply.

The rest of the paper is organized as follows. After providing a brief overview of conventional MDLLs in Section II, the proposed highly digital MDLL architecture is presented and analyzed in Section III. The circuit implementation details of key building blocks are discussed in Section IV. In Section V, we present a separately optimized DPLL that is used for comparison with the proposed DMDLL. Section VI shows the experimental results obtained from the prototype IC. Finally, key contributions of this work are summarized in Section VII.

II. Overview of Multiplying Delay-Locked Loops

Multiplying delay-locked loops (MDLLs) have been recently proposed for clock multiplication to overcome jitter accumulation in PLLs[16], [17]. The block diagram of a conventional MDLL is shown in Fig. 2. It consists of a phase detector, loop filter, multiplexed ring oscillator, and selection logic. The select logic generates a pulse during which the positive edge of the VCO is replaced by the positive edge of the reference clock as illustrated by timing diagrams in Fig. 3. To ensure clean edge replacement, the reference (REF) and output (OUT) clock edges have to be aligned as shown in Fig. 3(a). In practice, phase detector and charge-pump mismatches causes the loop to settle with a static phase offset (SPO), and the misalignment between REF and OUT clock edges caused by SPO leads to deterministic jitter (shown as $\Delta \mathrm{T_{D,J}}$ in Fig. 3(b)). In other words, SPO appears as periodic error in the output clock period at each reference selection and appears in the output clock spectrum as spurs at integer multiples of the reference frequency. To reduce these spurs, it is important to accurately tune the oscillator until $\Delta \mathrm{T_{D,J}}$ becomes zero.

MDLLs offer superior suppression of VCO phase noise. Fig. 4(a) illustrates the phenomenon of jitter accumulation in VCOs. The accumulated jitter in a VCO is plotted as a function of measurement time interval ΔT[18] shows that jitter accumulates indefinitely in an open loop VCO. However, when the VCO is embedded in a PLL, the feedback prevents indefinite

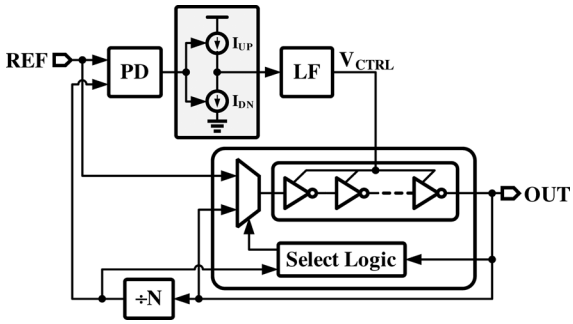

Fig. 2. Conventional MDLL block diagram.

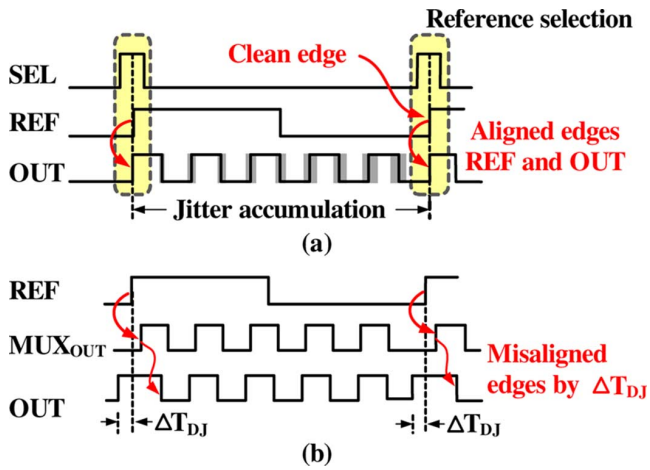

Fig. 3. MDLL timing diagram illustrating periodic reference injection.

jitter accumulation, and the PLL loop suppresses VCO noise within its bandwidth. Because this bandwidth is at most one tenth the reference frequency ($F_{REF}/10$), the jitter suppression is limited as well. However, when the same VCO is embedded in an MDLL loop its jitter accumulation is reset periodically due to the injection of reference clock into the VCO. As a result, MDLL suppresses VCO noise within its bandwidth which is shown to be at least twice the PLL bandwidth[17]. The jitter suppression in an MDLL can also be seen clearly in the frequency domain phase noise plot shown in Fig. 4(b). In both the PLL and MDLL, the VCO phase noise is high-pass shaped by the loop bandwidth. Because MDLL bandwidth can be at least 2.5 × higher than that of a PLL, the in-band phase noise in an MDLL is at least 8 dB lower than that of a PLL.

While analog MDLL clock generators have been shown to have superior random jitter performance compared with PLLs [16], [17], [19], [20], their performance is limited by SPO induced deterministic jitter degradation. In practice, SPO can be as high as 20-to-30 ps, which severely limits the deterministic jitter performance of the MDLL. By obviating the need for a charge-pump, a digital MDLL implementation can eliminate the biggest source of deterministic jitter. In general, MDLLs provide the benefit of better suppression of oscillator's noise at the cost of deterministic jitter caused by mismatches in the charge-pump or phase offset comparison path, and lower filtering of the reference clock noise. In [21], a digital MDLL was proposed using a high resolution TDC to eliminate SPO and

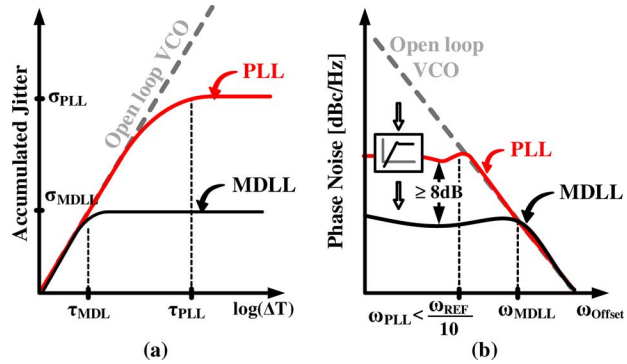

Fig. 4. (a) Jitter accumulation in an open loop VCO, VCO embedded in a PLL, and an MDLL. (b) Frequency domain view of the VCO phase noise suppression in PLLs and MDLLs.

achieve low jitter. While this digital MDLL implementation reduces static phase offset and achieves low jitter, it still requires a high resolution power hungry TDC and is also susceptible to supply noise. To overcome the drawbacks of conventional MDLL implementations, we present a highly digital MDLL architecture that uses only a 1-bit TDC and low power supply regulator to achieve excellent jitter performance and supply noise immunity.

III. Proposed Digital MDLL Architecture

The block diagram of the proposed digital MDLL is shown in Fig. 5 [15]. It consists of a separate frequency-locking loop (FLL) and a type-I multiplying delay-locked loop. The FLL, composed of a frequency detector and accumulator, drives a digitally-controlled multiplexed ring oscillator (DXRO) toward frequency lock. Unlike traditional MDLLs [16], [17], [19], [20] where performance is limited by the phase detector and charge-pump mismatches, the proposed digital MDLL tuning loop utilizes a 1-bit TDC and a digital loop filter (DLF) to drive the digitally-controlled multiplexed ring oscillator (DXRO) toward phase lock. The 1-bit TDC, as opposed to the high resolution power hungry TDC in [21], allows significant power reduction. The divider and selection logic blocks are used to reset jitter accumulation in the oscillator by periodically injecting a clean reference edge. To ensure clean reference injection, the multiplexer in the DXRO is carefully designed. A 1-to-4 demultiplexer eases the speed requirements of fully-synthesized control logic. The effect of loop latency was minimized by feeding only the 14-MSBs of the 18-bit digital accumulator output to the $\Delta\Sigma$ DAC. The DACs are implemented with a cascade of a digital delta-sigma modulator that truncates the accumulator output and a 15-level current-mode DAC. A second order passive low-pass filter suppresses the out-of-band quantization error and guarantees precise setting of the oscillation frequency to ensure proper reference injection.

Fig. 6 shows the generalized s-domain model of digital MDLLs and PLLs used to calculate the loop bandwidth and noise transfer functions. K_{TDC} is the TDC gain, K_{DCO} is the DXRO gain when configured as an oscillator, N is the feedback divide ratio, K_P is the proportional gain, and K_{ACC} denotes the integral path gain. In Fig. 6, the effect of reference selection and the oscillator's phase realignment transfer functions are

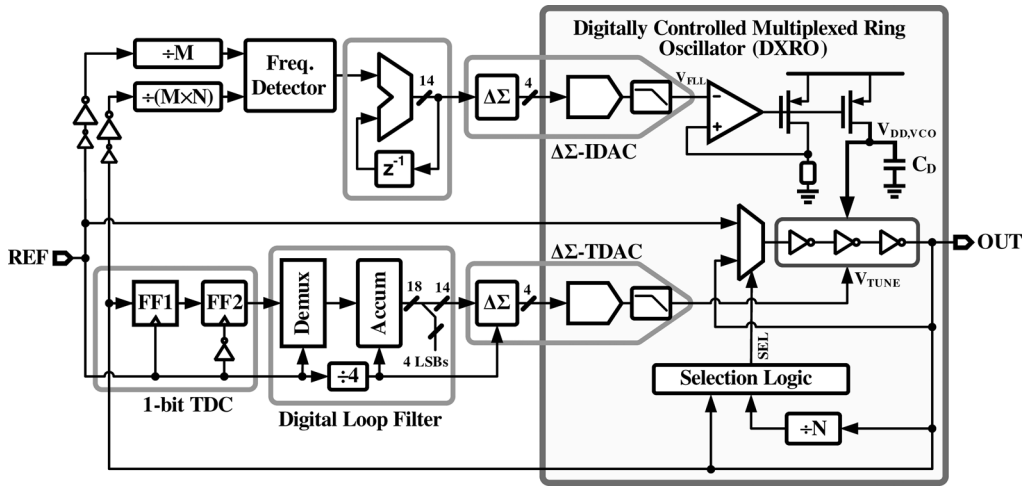

Fig. 5. Block diagram of the proposed DMDLL.

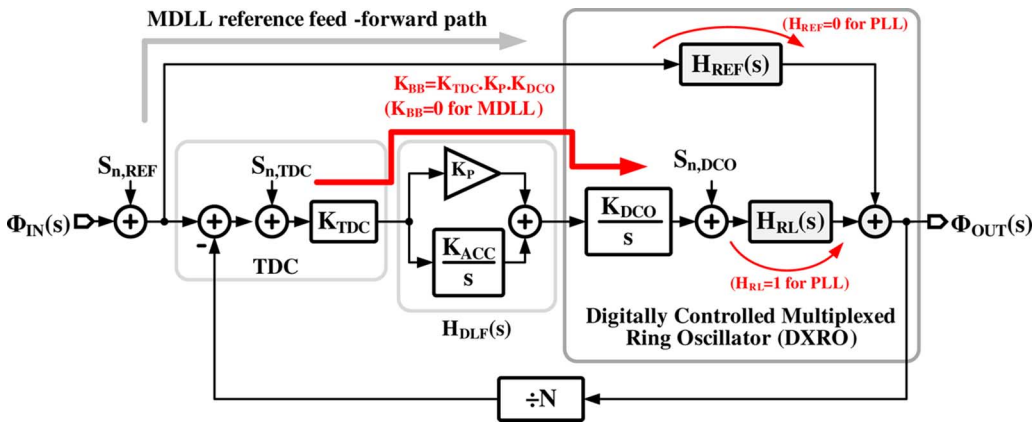

Fig. 6. Generalized DMDLL/DPLL model.

represented by $H_{RL}(s)$ and $H_{REF}(s)$, respectively and is given by [17]:

$$H_{RL}(s) = 1 - \frac{\beta}{1+(\beta-1)e^{-sT_{REF}}} e^{-sT_{REF}/2} \cdot \frac{\sin\left(\left|s \times \frac{T_{REF}}{2}\right|\right)}{\left|s \times \frac{T_{REF}}{2}\right|} \quad (1)$$

and

$$H_{REF}(s) = \frac{N\beta}{1+(\beta-1)e^{-sT_{REF}}} \cdot e^{-sT_{REF}/2} \cdot \frac{\sin\left(\left|s \times \frac{T_{REF}}{2}\right|\right)}{\left|s \times \frac{T_{REF}}{2}\right|} \quad (2)$$

where β represents the realignment coefficient ($\beta_{MDLL} = 1$, $\beta_{PLL} = 0$), and T_{REF} is the reference clock period. The closed loop transfer function of the MDLL/DPLL is given by

$$\frac{\Phi_{OUT}(s)}{\Phi_{IN}(s)} = \frac{N\left(1+\frac{sK_{BB}}{K_I}\right) \times H_{RL}(s)}{\left(1+\frac{sK_{BB}}{K_I}\right) \times H_{RL}(s) + \frac{s^2 N}{K_I}} + H_{REF}(s) \quad (3)$$

where K_{BB} and K_I represents the cumulative gains through the bang-bang proportional and integral paths, respectively, and the transfer functions $H_{RL}(s)$ and $H_{REF}(s)$ are given in (1) and (2), respectively. Mathematically, K_{BB} and K_I are equal to:

$$K_{BB} = K_{TDC} \cdot K_P \cdot K_{DCO}, \quad (4)$$

$$K_I = K_{TDC} \cdot K_{ACC} \cdot K_{DCO}. \quad (5)$$

K_{BB} is equal to zero for the MDLL since the periodic reference selection acts as a proportional path and stabilizes the loop. Because the resetting action happens every reference cycle, the MDLL behaves more like a DLL in its loop dynamics and can be a treated as a first order feedback system. Stability ensured by the reference feed forward injection is illustrated by the second term in (3), $H_{REF}(s)$. By setting $H_{RL} = 1$ and $H_{REF} = 0$ (see Fig. 6), the model can be used for PLLs and (3) simplifies to the well-known PLL transfer function

$$\frac{\Phi_{OUT}(s)}{\Phi_{IN}(s)} = \frac{N\left(1+\frac{sK_{BB}}{K_I}\right)}{1+\frac{sK_{BB}}{K_I}+\frac{s^2 N}{K_I}}. \quad (6)$$

The low bandwidth FLL continuously runs in the background and has no impact on the loop dynamics and is hence not considered in this analysis. Once the FLL is locked, the MDLL tuning loop was designed to cover a wide range of voltage and temperature variations.

Because oscillator noise is suppressed by reference injection, the MDLL bandwidth can be lowered to aggressively suppress TDC quantization error without any oscillator phase noise penalty. This is illustrated by the decoupled TDC/DCO noise

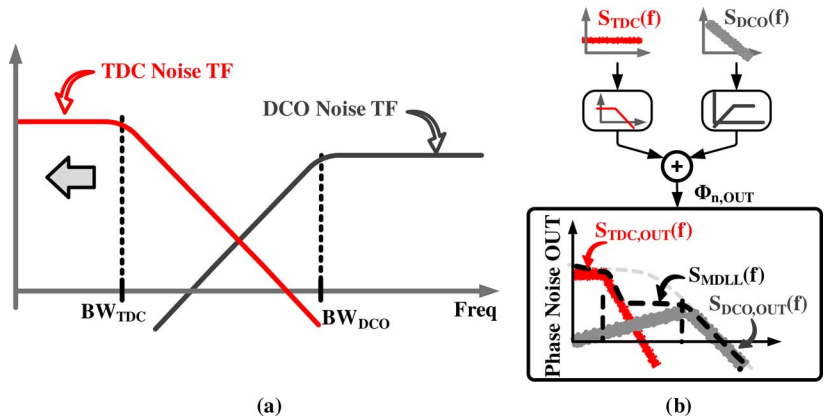

Fig. 7. Decoupled TDC/DCO bandwidth tradeoff in an MDLL, and output phase noise.

bandwidth tradeoff of an MDLL in Fig. 7, where $\mathrm{BW_{TDC}}$ and $\mathrm{BW_{DCO}}$ are 3 dB noise bandwidths of the TDC and DCO, respectively. As indicated in Fig. 7, in MDLLs the TDC bandwidth can be lowered independently without affecting the oscillator's phase noise filtering, which is not the case in DPLLs. The oscillator's phase noise is also attenuated significantly for frequencies lower than $\mathrm{BW_{DCO}}$ which can be found to be around $\mathrm{F_{REF}}/4$ using (1)–(3). This is at least 2.5× higher than PLLs' highest bandwidth ($\mathrm{F_{REF}}/10$) which translates to at least 8 dB of phase noise and supply noise suppression. While the TDC and DCO noise can be suppressed in MDLLs much more than PLLs, the reference phase noise is attenuated less compared to PLLs. Leveraging this decoupled tradeoff, the proposed MDLL uses a 1-bit TDC to detect the sign of the phase error. The TDC output is then fed to the digital loop filter which drives the digitally-controlled multiplexed oscillator toward phase lock. The divider in combination with the selection logic resets jitter accumulation in the oscillator. To achieve a wide operating range, a fully synthesized frequency-locking loop (FLL) is used to drive the DXRO toward frequency lock. Using separate DACs in the FLL and the MDLL relaxes the stringent quantization error requirements otherwise present in a shared DAC architecture.

Interestingly, the reference injection that reduces jitter accumulation in MDLLs also makes them more immune to supply noise compared to PLLs. Because supply noise also causes jitter to accumulate in a VCO, realignment of the VCO edge with the reference edge reduces supply noise induced jitter as well. The magnitude response of the VCO supply to PLL phase output transfer function exhibits a well-known band-pass transfer characteristic indicating that the PLL is most sensitive around its bandwidth. However, in an MDLL the output phase noise due to supply noise is inherently suppressed by at least 8 dB more, just like oscillator phase noise as discussed earlier. In our design, this property is combined with a high PSRR regulator to achieve excellent supply noise immunity. A low drop-out replica-biased regulator is used to shield the oscillator supply, which makes the proposed DMDLL immune to supply noise. Since the regulator is embedded in very low bandwidth FLL, the regulator bandwidth can also be chosen to be low. This allows to improve regulator's PSRR with minimal power penalty.

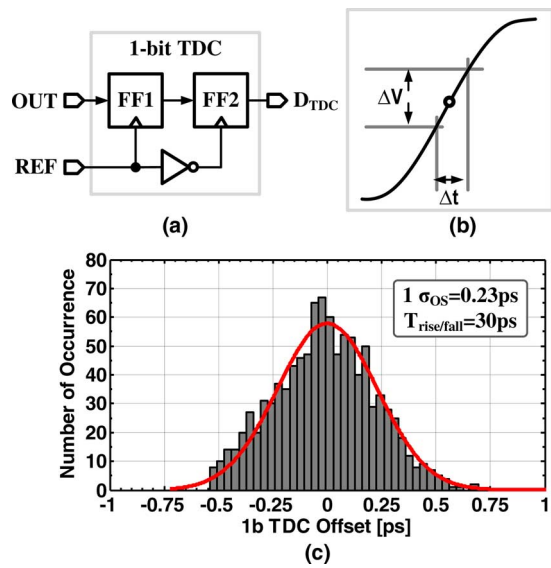

Fig. 8. (a) Schematic of the 1-bit TDC, (b) the effect of clock jitter on the sampling voltage error, and (c) simulated TDC phase offset using Monte-Carlo analysis.

IV. Building Blocks

The transistor-level implementation details of key building blocks are discussed in this section. All digital building blocks such as the digital $\Delta\Sigma$ modulators and accumulators are synthesized using standard cells.

A. Low Power 1-Bit TDC

The schematic of the 1-bit TDC is shown in Fig. 8(a) wherein the flip-flops are realized using sense-amplifier flip-flops [22]. The TDC sub-samples the output clock with the input reference clock using a flip-flop. It detects the sign of the phase error in the form of early/late decisions. The first flip-flop, FF1, output is re-sampled by an identical flip-flop, FF2, to reduce hysteresis caused by output state-dependent loading. Because there are only two flip-flops clocked at relatively low reference frequency, this TDC is very power efficient. However, as with analog MDLLs, the input referred voltage offset of the FF1 appears as static phase offset and causes deterministic jitter (see Fig. 3(b)).

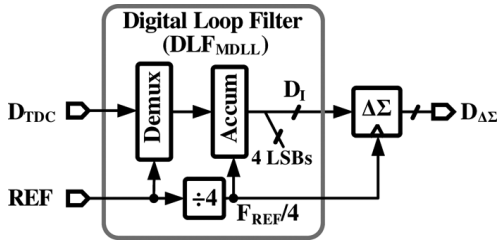

Fig. 9. Block diagram of the MDLL digital loop filter ($\mathrm{DLF_{MDLL}}$).

The voltage offset is minimized by increasing device dimensions, and the impact of voltage offset on phase offset is minimized by reducing the rise/fall times of both the reference and feedback clocks. Fig. 8(b) illustrates graphically the relationship between voltage offset of the 1-bit TDC and the sampling error. If the input to the TDC is a time-varying signal, then a sampling time error of $\Delta\mathrm{t}$ results in a change in the sampled voltage by $\Delta\mathrm{V}$, and vice versa. The 1-bit TDC offset was simulated using Monte-Carlo analysis and the histogram of the SPO is shown in Fig. 8(c). The standard deviation of the voltage offset is approximately 7.5 mV. Therefore, with a rise/fall time of 30 ps, the voltage offset translates to a phase offset of less than 0.23 ps as indicated by the histogram in Fig. 8(c).

B. Digital Loop Filter (DLF)

The block diagram of the digital loop filter is shown in Fig. 9. It consists of a simple digital accumulator which is driven by the sign of the phase error. A 1-to-4 demultiplexer is used to ease the speed requirements of the fully-synthesized 18-bit accumulator. The impact of TDC quantization error on output jitter is minimized by lowering the time constant of the digital accumulator. Recall that lowering the DMDLL bandwidth does not exacerbate oscillator phase noise. The dithering jitter caused by excessive loop delay is reduced by ignoring the accumulator's lower 4-LSBs. In other words, only the 14-MSBs are used by the high resolution $\Delta\Sigma$ digital-to-analog converter.

C. $\Delta\Sigma$ Digital-to-Analog Converter

The block diagram of the digital-to-analog converter (DAC) used in both the MDLL tuning loop and the FLL loop is shown in Fig. 10. A 14-bit second order digital delta-sigma modulator (DSM) truncates the 14-bit accumulator output ($\mathrm{D_I}$) to 15-levels and drives a current mode DAC. The current-mode DAC consisting of 15 matched current sources converts the digital input to an equivalent output current (see Fig. 10). Resistor R converts the DAC output current to voltage. A second order passive low-pass filter (LPF), with a 500 kHz bandwidth, suppresses out-of-band quantization error and generates control voltage of the oscillator, ($\mathrm{V_{FLL}}$ or $\mathrm{V_{TUNE}}$). While the $\Delta\Sigma$ DAC architecture eases hardware requirements, the LPF increases loop latency and degrades jitter performance. Loop delay causes the accumulator code to dither by more than 1-LSB. To minimize resulting jitter degradation, the lower 4-LSBs of the accumulator output are ignored. In other words, an 18-bit accumulator is implemented and only the 14-MSBs are fed to the digital $\Delta\Sigma$ modulator.

D. Digitally Multiplexed Ring Oscillator (DXRO)

The schematic of the multiplexed ring oscillator is shown in Fig. 11. It is composed of a cascade of a multiplexer and three pseudo-differential delay cells that are tuned by the FLL and the MDLL by varying the supply voltage and the output time constant, respectively. The delay cells are implemented using CMOS inverters coupled in a feed-forward manner to ensure differential operation. The supply noise sensitivity of the oscillator is reduced by using a replica-biased regulator which buffers the frequency-tuning voltage $\mathrm{V_{FLL}}$ and generates the DXRO supply voltage, $\mathrm{V_{DD,VCO}}$. The degradation of jitter due to supply noise in the delay tuning path of the DXRO is minimized by reducing the gain and decoupling control voltage, $\mathrm{V_{TUNE}}$, from the supply voltage. The simulated VCO phase noise plot at 1.5 GHz output frequency is shown in Fig. 12. At 1 MHz offset, the VCO phase noise is $-88\ \mathrm{dBc/Hz}$ for the open loop VCO, which reduces to $-130\ \mathrm{dBc/Hz}$ when the VCO is used in the proposed DMDLL. The oscillator consumes only 250 μW of power and yet achieving an excellent overall phase noise.

E. Replica-Biased Regulator

The schematic of the replica-biased regulator, optimized to achieve high supply noise rejection, is shown in Fig. 13(a). It buffers the FLL control voltage, and generates the virtual supply voltage of the oscillator denoted as $\mathrm{V_{DD,VCO}}$. Because the regulator is placed in the low-bandwidth FLL, wide-band supply noise rejection is achieved by introducing a low-frequency pole ω_D at the VCO supply node[9]. By making ω_D to be lower than the pole at the amplifier output, ω_A, the peaking present in the power supply rejection plots of conventional regulators can be eliminated. By closing the feedback around the replica of the VCO, a replica-biased regulator facilitates an area efficient means to introduce the low frequency pole ω_D. The simulated PSRR curves for various values of the bypass capacitance $\mathrm{C_D}$ shown in Fig. 13(b) illustrate this improvement. As expected, increasing $\mathrm{C_D}$ lowers ω_D and improves PSRR beyond the amplifier output pole ω_A. The value of $\mathrm{C_D}$ was chosen to be 150 pF in the prototype, as a tradeoff between PSRR and area. The replica load is implemented with stacked diode-connected devices to achieve good matching with the VCO.

F. Frequency-Locking Loop (FLL)

To extend the operating range of the MDLL, a fully synthesized frequency-locking loop (FLL) is used to drive the DXRO toward frequency lock (see Fig. 5). A counting type frequency detector is employed in this implementation, and its schematic is shown in Fig. 14. Frequency error is found by measuring the difference between the number of oscillator periods in adjacent reference periods. The DXRO clock is first divided by 64 before it is provided to a 14-bit counter to relax the counter speed requirements. Deviation of the counter output from 128, between the two divided clocks, is the measure of frequency error. A cascade of two registers is used to perform digital differentiation $1 - z^{-1}$ and the resulting frequency error is fed to the digital loop filter. The 14-bit DAC in the FLL is implemented using a delta-sigma modulator and 15-level current mode DAC (shown as $\Delta\Sigma$-IDAC in Fig. 5). A second order passive low pass filter

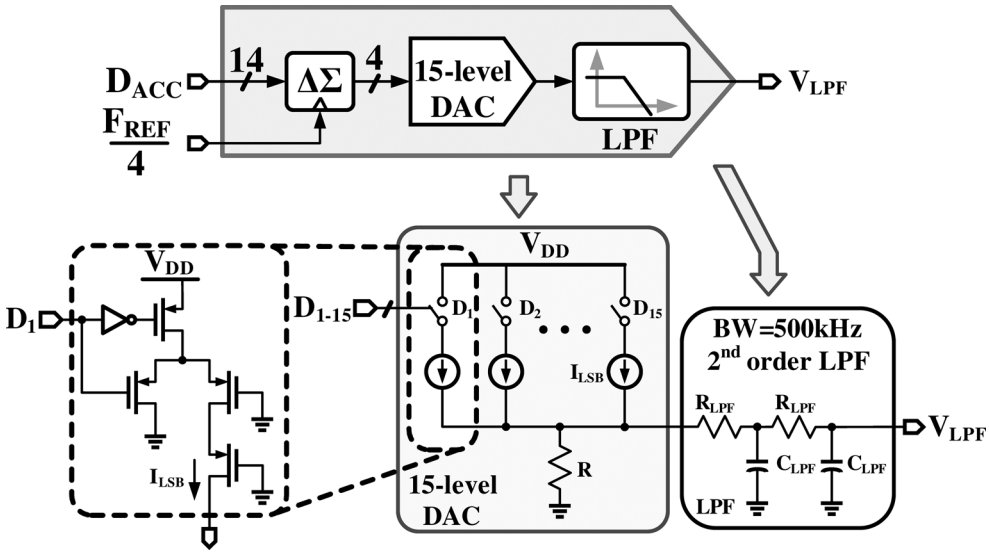

Fig. 10. Block diagram of the delta-sigma DAC and circuit schematic of the 15-level current mode DAC and post filter.

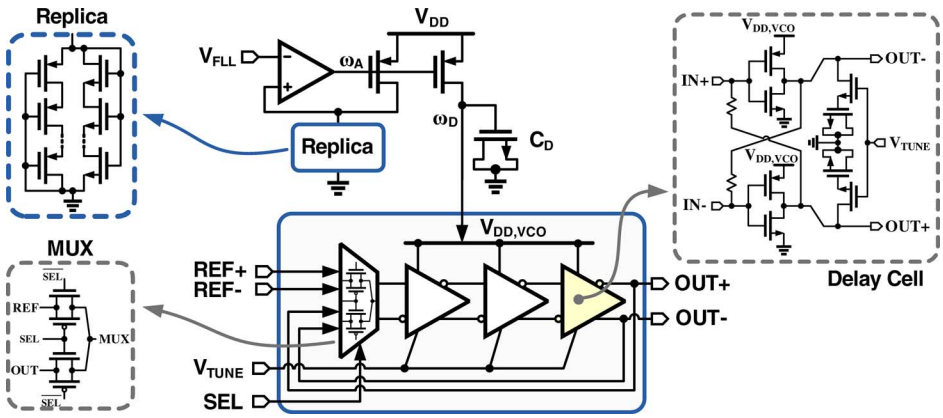

Fig. 11. Schematic of the proposed regulated multiplexed ring oscillator.

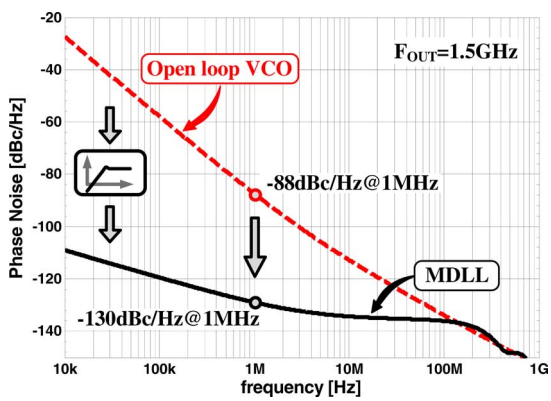

Fig. 12. Simulated phase noise for the proposed DMDLL at 1.5 GHz output frequency.

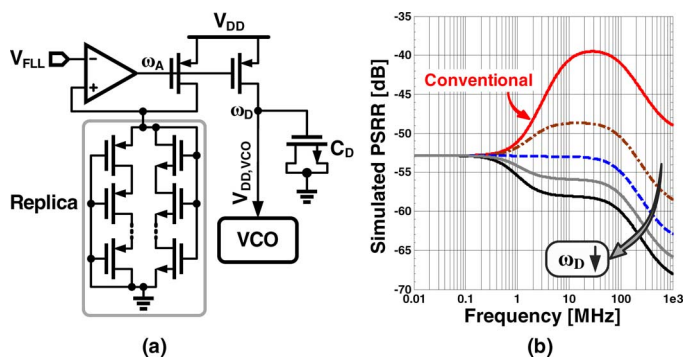

Fig. 13. (a) Schematic of the high PSRR replica-biased regulator, and (b) the simulated PSRR for different bypass capacitor (C_D) values.

and the low bandwidth regulator suppress the delta-sigma truncation error.

V. Optimized DPLL Architecture

For comparison with the proposed DMDLL, a digital PLL was also implemented using identical blocks to those of the

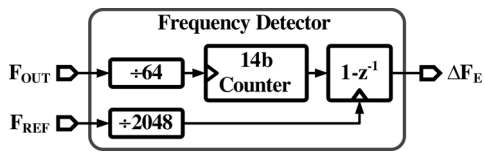

Fig. 14. Block diagram of the frequency detector.

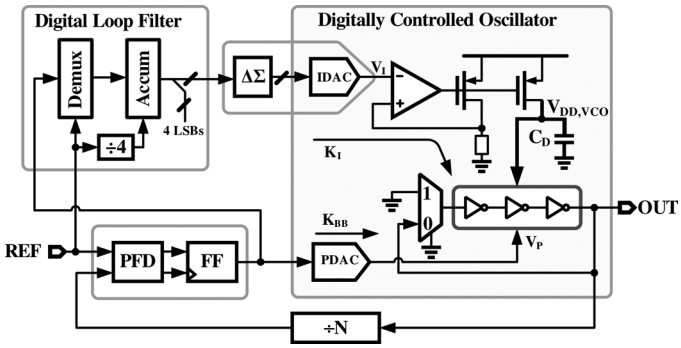

Fig. 15. Block diagram of the optimized DPLL implemented using identical blocks to the MDLL.

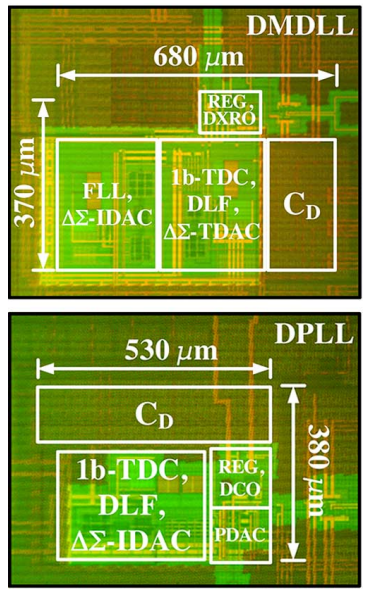

Fig. 16. MDLL and DPLL die photographs.

MDLL and the same reference clock frequency [23]. The DPLL is separately optimized for low jitter and high supply noise rejection. The block diagram of the supply noise regulated Type-II DPLL is shown in Fig. 15. It consists of separate bang-bang 1-bit TDC proportional and digital integral paths, a digitally controlled oscillator (DCO), a replica regulator, and a feedback divider. A flip-flop (FF) acts as an early/late detector on classical 3-state PFD outputs and drives the oscillator and the digital accumulator to implement the proportional and integral controls, respectively.

Similar to the MDLL, the low bandwidth digital integral path suppresses phase quantization error of the FF, the dithering jitter is mainly caused by the proportional path. The digital loop filter and the digital $\Delta\Sigma$ modulator are identical to those of the DMDLL, and a second order passive low-pass filter suppresses the out-of-band quantization error and drives the integral control voltage input of the oscillator. In the DPLL, the same DXRO is used in a continuously running digitally-controlled oscillator (DCO) mode, and the reference edge injection is disabled by always selecting the oscillator's output to close the oscillator's feedback loop. An identical replica-biased regulator was used for fair comparison with regard to the supply noise rejection properties. As will be shown next in the measurement results section, the DPLL performance is comparable to the state-of-the-art digital PLL clock multipliers.

VI. Experimental Results

The prototype DMDLL and DPLL were fabricated in a 0.13 μm CMOS process and the die photographs are shown in Fig. 16. The prototype chips occupy active areas of 0.25 mm^2 and 0.2 mm^2 for the DMDLL and DPLL, respectively. Both designs operate over a wide range of output frequencies of 0.8-to-2 GHz from a 1.1 V supply. At 1.5 GHz output frequency, the DMDLL consumes only 890 μW and the DPLL consumes 1.35 mW.

The measurement setup used to characterize the prototype ICs is shown in Fig. 17. Supply noise measurements are performed by modulating the VCO supply with sinusoidal tone. An arbitrary waveform generator (Tektronix AWG7122B) is used to provide the input reference clock, while an RF signal generator (Fluke 6062A) is used to introduce sinusoidal noise tones on the VCO supply. Since the prototype chips' feedback divide ratio is fixed at four, the desired output frequency was obtained by varying the reference frequency. A communication signal analyzer (Tektronix CSA8200) was used for the time domain long-term absolute jitter measurements. The spectrum analyzer (Tektronix RSA3308B) is used to measure the reference and noise spurs. To guarantee the fidelity of all supply noise measurements, an integrated supply noise monitor, implemented using a wide bandwidth voltage follower, is used to measure the amount of on-chip VCO supply noise. Unless otherwise stated, all measurement results reported are obtained with a reference frequency of 375 MHz. Fig. 18 shows the measured phase noise spectrum at 1.5 GHz output frequency. The measured phase noise at 1 MHz offset is nearly -129 dBc/Hz and -112 dBc/Hz for the DMDLL and DPLL designs, respectively. The measured MDLL phase noise at 1 MHz (-129 dBc/Hz), is only 1 dB higher than the simulated phase noise (-130 dBc/Hz as shown in Fig. 12), demonstrates the ability of the MDLL to suppress the -88 dBc/Hz open loop oscillator's noise significantly. The rms jitter obtained by integrating phase noise from 10 kHz-to-100 MHz is only 400 fs for DMDLL and it is 3.2 ps for the DPLL. In the case of the DPLL, limit cycle induced peaking at around 40 MHz increases the rms jitter. This peaking also exacerbates supply noise sensitivity, and as expected, no such peaking is observed for the DMDLL.

The quality of the external reference clock is important in determining the quality of the MDLL. Even though a low jitter reference clock was used, the DMDLL output phase noise was dominated by the arbitrary waveform generator (AWG7122B) for frequencies lower than 100 MHz. The reference phase noise is -110 dBc/Hz and -145 dBc/Hz at frequency offsets of 10 kHz and 1 MHz, respectively [24]. As shown in Fig. 18, the phase noise of the DMDLL is -97 dBc/Hz and -129 dBc/Hz at frequency offsets of 10 kHz and 1 MHz, respectively. This is only 12.5 dB (ideally 12 dB for a divide ratio of 4) higher than the reference frequency at the low frequency (10 kHz). At 1 MHz frequency offset, the output phase noise is 15 dB

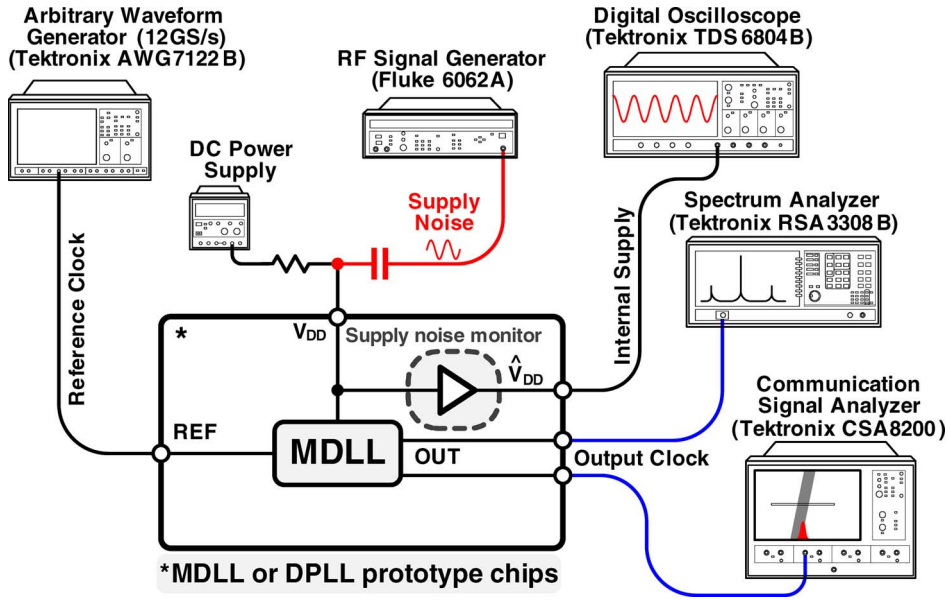

Fig. 17. Measurement setup.

higher than the reference noise, and the phase noise is dominated by the oscillator's phase noise at higher frequencies (measured -129 dBc/Hz, and simulated -130 dBc/Hz at 1 MHz as shown in Fig. 12).

The jitter accumulation in both designs is investigated by measuring the long-term jitter. Fig. 19 shows the measured jitter histograms at 1.5 GHz output frequency. The long-term absolute jitter measured over 5 M hits is only 920 $\mathrm{fs_{rms}}$ and 9.2 ps peak-to-peak for the DMDLL, which is about 4 $\times$ lower than that of the DPLL. The DPLL jitter is about 4.2 $\mathrm{ps_{rms}}$ and 32 ps peak-to-peak.

The effectiveness of the proposed supply regulation scheme is evaluated by measuring the output jitter when a large 200 $\mathrm{mV_{pp}}$ sinusoidal tone is superimposed on the VCO supply voltage. The measured peak-to-peak jitter degradation (calculated by subtracting the jitter in the absence of the supply noise) is plotted in Fig. 20. This plot quantifies the measured dynamic supply noise sensitivity by plotting peak-to-peak jitter degradation as the supply noise frequency is swept from 1 MHz-to-1.4 GHz. In the worst case, long-term peak-to-peak MDLL jitter degraded by only 3.8 ps peak-to-peak resulting in a supply noise sensitivity of less than 20 fs/mV (see Fig. 21). This is 3 $\times$ lower than the 12 ps (50 $\mathrm{fs_{pp}/mV_{pp}}$) of the DPLL. The plot corresponding to the DPLL (Fig. 20) shows that the supply noise sensitivity is highest around 40 MHz, which is the peaking frequency identified earlier in the phase noise plot. This peaking is attributed to the limit cycles present in the steady-state of the DPLL.

Fig. 22 shows the measured output spectrum of the DMDLL. The reference spur, shown in Fig. 22(a), is -55.6 dBc, which translates to only 0.7 $\mathrm{ps_{pp}}$ deterministic jitter estimated using the following equation [9]:

$$\mathrm{DJ_{OUT}} = \frac{2}{\pi}\mathrm{T_{OUT}} \times 10^{\mathrm{Spurs(dBc)}/20} \tag{7}$$

where $\mathrm{T_{OUT}}$ is the output clock period, Spurs (dBc) is the difference between the spurious reference tone and that of the carrier. The measured output spectrum when 200 $\mathrm{mV_{pp}}$ supply noise is introduced at the worst case noise frequency of 100 MHz is depicted in Fig. 22(b). Compared to the case when there is no supply noise, the reference spurs are not degraded but the spurs due to supply noise are found to be at about -48 dBc level which translates to a supply noise induced jitter degradation of only 1.6 ps peak-to-peak.

Similarly for the case of DPLL, the measured reference spurs are found to be -46 dBc (illustrated in Fig. 23(a)). In the presence of 200 $\mathrm{mV_{pp}}$ supply noise, the worst-case reference and supply noise spurs are measured to be -46 dBc and -31 dBc, respectively (shown Fig. 23(b)). The deterministic jitter degradation due to these spurs is 11.5 ps peak-to-peak, which is 7$\times$ worse than the MDLL. Fig. 24 demonstrates the impact of $\mathrm{K_{BB}}$ on the jitter performance in the absence of supply noise for the DPLL and the MDLL. In case of the DPLL, at lower values of $\mathrm{K_{BB}}$ the oscillator phase noise dominates the output jitter, and as $\mathrm{K_{BB}}$ increases, the dithering jitter starts to dominate. Larger $\mathrm{K_{BB}}$ values leads to increased phase noise peaking at frequencies much higher than DPLL tracking bandwidth which results in much higher jitter. This peaking is due to the limit cycles present in the steady-state of the bang-bang PLLs [14] as illustrated earlier in the phase noise plot. Note that, the DPLL is separately optimized for low jitter and $\mathrm{K_{BB}}$ is always much higher than $\mathrm{K_I}$ to maintain the DPLL's loop stability for all $\mathrm{K_{BB}}$ values. However, for the MDLL the worst-case peak-to-peak jitter is not degraded for different values of $\mathrm{K_I}$.

The performance of the prototype digital MDLL and DPLL are summarized and compared with state-of-the-art MDLLs and supply regulated PLLs in Table I. The proposed MDLL and DPLL achieve excellent jitter performance while consuming only 890 μW and 1.35 mW for the MDLL and DPLL, respectively. The MDLL achieves the lowest supply noise sensitivity of 20 fs/mV with 3$\times$ lower power compared to state-of-the-art

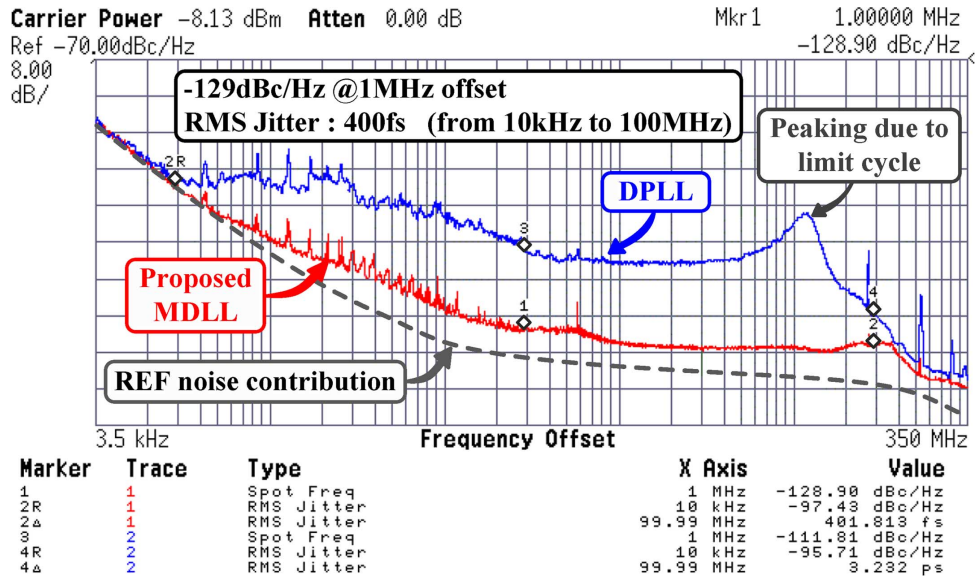

Fig. 18. Measured phase noise at 1.5 GHz output frequency.

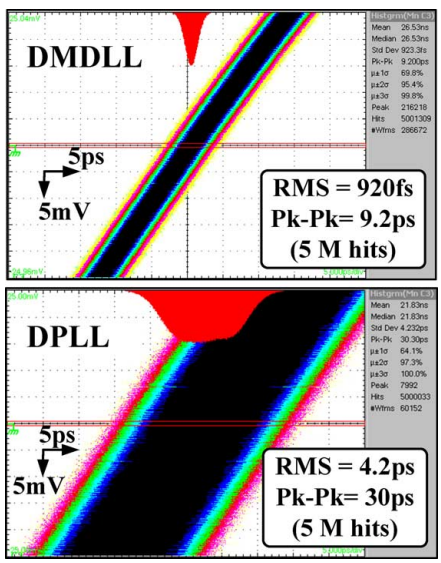

Fig. 19. Measured long-term jitter histograms (5 M hits) at 1.5 GHz output frequency.

MDLLs designs and 4× lower power than supply regulated analog PLLs. Compared to state-of-the-art DPLLs, the proposed MDLL demonstrates 40× supply noise sensitivity improvement with lower power consumption while achieving less jitter.

Table II shows that the proposed MDLL compares very favorably with state-of-the-art clock multipliers with similar reference frequency range and multiplication ratio. For lower reference frequencies, the increase in output jitter due to the oscillator's phase noise (less DCO bandwidth $\mathrm{BW_{DCO}} = \mathrm{F_{REF}}/4$) can be simply mitigated with a small power penalty. Compared to a PLL where the oscillator's power needed to achieve the same jitter performance is significantly higher, MDLLs offer a very attractive alternative with great power savings and excellent jitter performance.

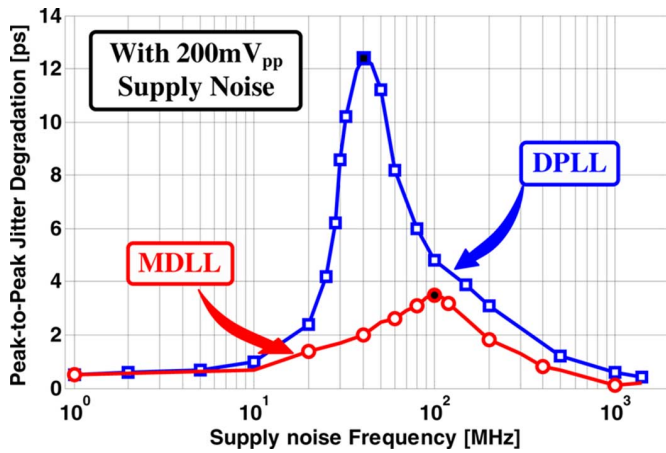

Fig. 20. Measured peak-to-peak jitter degradation as a function of supply noise frequency at 1.5 GHz output frequency.

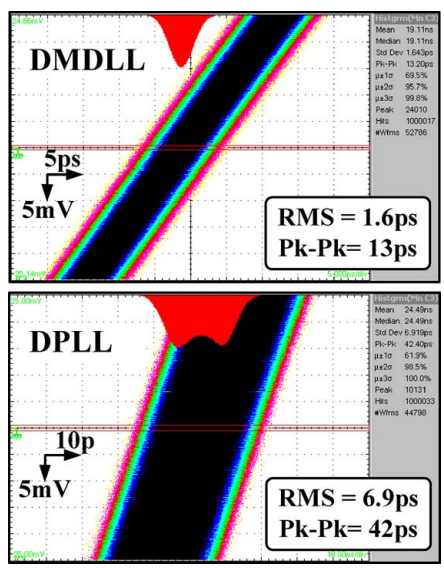

Fig. 21. Measured long-term jitter histograms at 1.5 GHz output frequency with 200 $\mathrm{mV_{pp}}$ supply noise at the worst case noise frequency.

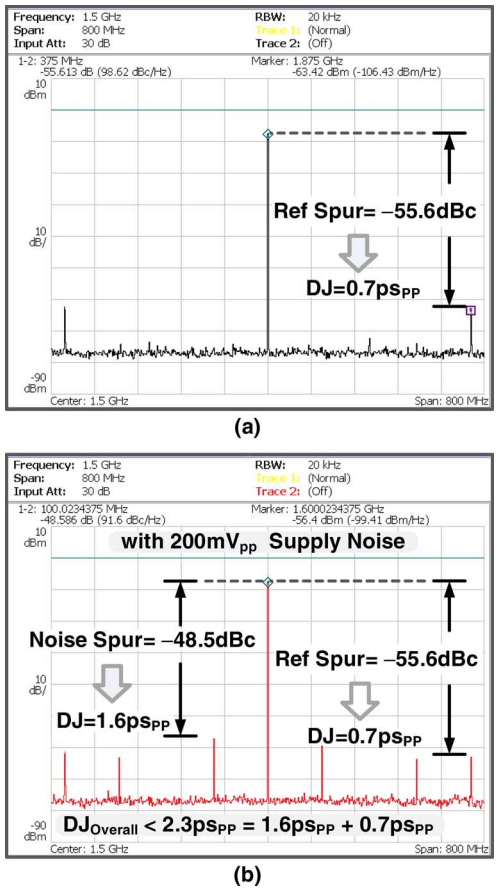

Fig. 22. Measured MDLL spurs (a) reference spurs for a quiet supply voltage, and (b) reference and supply noise induced spurs, in the presence of 200 mV_{pp} at worst case supply noise frequency.

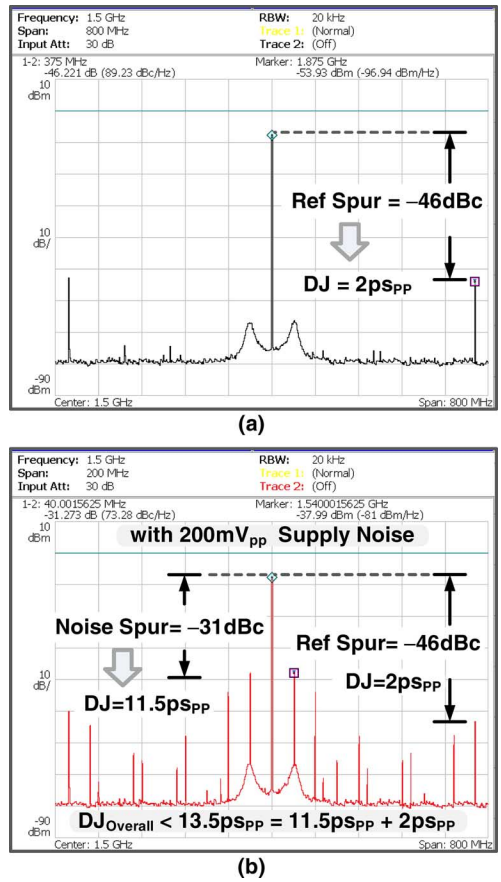

Fig. 23. Measured DPLL (a) reference spurs for a quiet supply voltage, and (b) reference and spurs with 200 mV_{pp} supply noise at the worst case supply noise frequency of 40 MHz.

VII. Conclusion

Digital phase-locked loops have emerged as attractive alternatives to classical analog PLLs in many applications. While DPLLs offer many advantages in terms of reconfigurability, small area, and design time, they suffer from coupled tradeoff between TDC resolution and DCO phase noise. Because the TDC quantization error is low-pass filtered and the oscillator phase noise is high-pass filtered, it is very challenging to simultaneously suppress both these noise sources. In practice, either a high resolution TDC or low phase noise DCO is used to lower jitter. In contrast to this, the proposed architecture utilizes a calibration-free digital multiplying delay-locked loop to decouple this tradeoff with minimal power penalty. Because oscillator noise is suppressed by reference injection, we propose to reduce the MDLL bandwidth to aggressively suppress TDC quantization error without any oscillator phase noise penalty. Consequently, the prototype MDLL employs only a 1-bit TDC and achieves an integrated jitter of 400 fs rms at 1.5 GHz output frequency while consuming 890 μW. Compared to this, an optimized DPLL consumes 1.35 mW and its jitter is worse than 3 ps rms.

This paper also addressed the issue of supply noise in both digital PLLs and MDLLs. By using a low power regulator only in the integral path of a DPLL and MDLL, supply noise immunity is improved without increasing loop delay. The

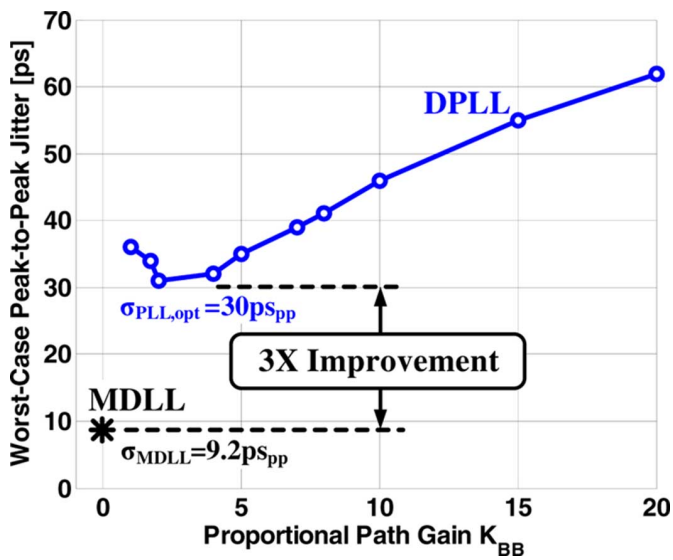

Fig. 24. Measured peak-to-peak DPLL and MDLL output jitter.

worst-case supply noise sensitivity of the MDLL and DPLL is 20 fs_{pp}/mV_{pp} and 50 fs_{pp}/mV_{pp}, respectively. This translates to a jitter degradation of 3.8 ps (MDLL) and 12 ps (DPLL) in the presence of 200 mV supply noise. The proposed clock multipliers occupy active die areas of 0.25 mm^2 and 0.2 mm^2 for the MDLL and DPLL, respectively.

TABLE I
PERFORMANCE COMPARISON OF THE PROPOSED MDLL AND DPLL WITH STATE-OF-THE-ART DESIGNS.

	This Work		[20]	[16]	[21]	[25]	[9]
	MDLL	DPLL	ISSCC 11	JSSC 02	JSSC 08	CICC 10	JSSC 09
Technology	0.13μm	0.13μm	65nm	0.18μm	90nm	65nm	0.18μm
Supply [V]	1.1	1.1	1.2/1.0	1.8	1.2	1.0	1.8
Output Freq. [GHz]	1.5	1.5	4.6	2.0	1.6	3.0	1.5
Ref Freq. [MHz]	375	375	575	250	50	300	375
Ref Spurs [dBc]	-55.6	-46.5	-46	-37	-58.3	N/A	N/A
Integ RMS Jitter [ps]	0.4	3.2	N/A	N/A	0.68	N/A	N/A
Power [mW]	0.89	1.35	6.8	12	9.2*	2.0	3.9
Jitter RMS/PP [ps]	0.9/9.2	4.2/30	2.0/17.8	1.73/15.6	0.93/11.1	2.1/21.9	1.9/15
w/o Supply Noise	5M hits	5M hits	235k hits	25k hits	30M hits	153k hits	20k hits
Jitter RMS/PP [ps]	1.6/13	6.9/42	N/A	N/A	N/A	3.93/34.4	4.9/25
w/ Supply Noise	200mV$_{pp}$, 100MHz	200mV$_{pp}$, 40MHz				14.7mV$_{RMS}$	200mV$_{pp}$, 8.85MHz
Worst-case SN Freq.	100MHz	40MHz	N/A	N/A	N/A	N/A	8.85MHz
Supply Sensitivity	20fs/mV	50fs/mV	N/A	N/A	N/A	850fs/mV**	50fs/mV
Power [mW/GHz]	0.6	0.9	1.48	6.0	5.75*	0.66	2.6
Implementation	DMDLL	DPLL	MDLL	MDLL	DMDLL	DPLL	PLL
Area [mm^2]	0.25	0.2	0.025	0.05	0.76*	0.26	0.093

* Off-chip components: area of 0.7mm^2 and power of 4.1 mW [21]

** Supply noise sensitivity in fs$_{PP}$/mV$_{RMS}$, while the rest are in fs$_{PP}$/mV$_{PP}$

TABLE II
COMPARISON OF THE MDLL WITH CLOCK MULTIPLIERS USING SIMILAR REFERENCE CLOCK FREQUENCY.

	This Work	CICC 12 [26]	VLSI 11 [27]	JSSC 08 [4]
Technology	0.13μm	40nm	40nm	65nm
Supply [V]	1.1	1.1	1.1	1.2
Reference [MHz]	200-500	200-800	312.5-700	125-500
Output Frequency [GHz]	0.8-2.0	0.8-3.2	1.25-2.8	1.0-4.0
Integrated RMS Jitter [ps]	0.4	N/A	N/A	N/A
Power [mW/GHz]	0.6	3.5-5.0	2.4**	8.4
Jitter RMS/PP [ps]	0.9 /9.2	N/A	N/A	6.0 /N/A
Implementation	DMDLL	MILO*	MILO*	DPLL

* Multiplying Injection Locked Oscillator (MILO)

** mW/Gb/s/lane, individual MILO power is not reported [27]

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