



Global Standards for the Microelectronics Industry

LPDDR5 System Perspective & Highlights

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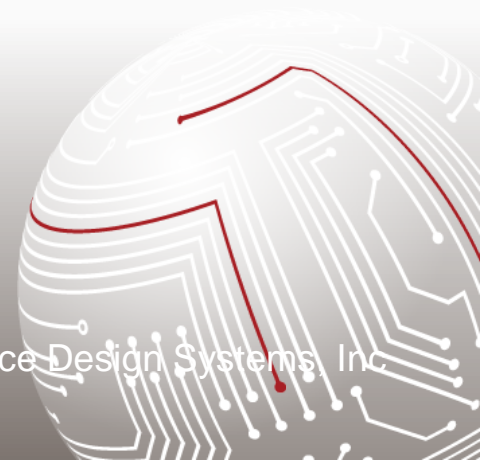
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LPDDR5 Workshop

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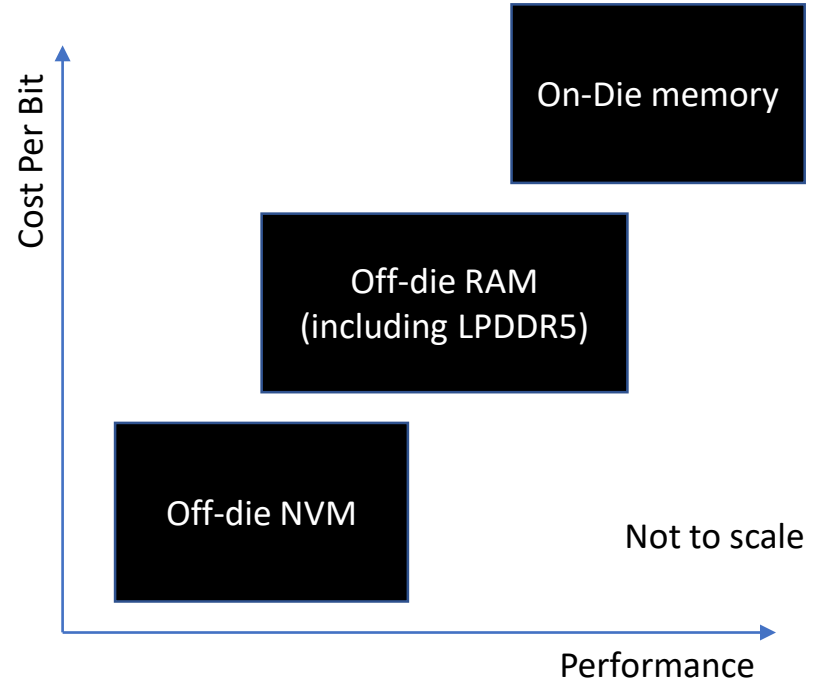


Agenda

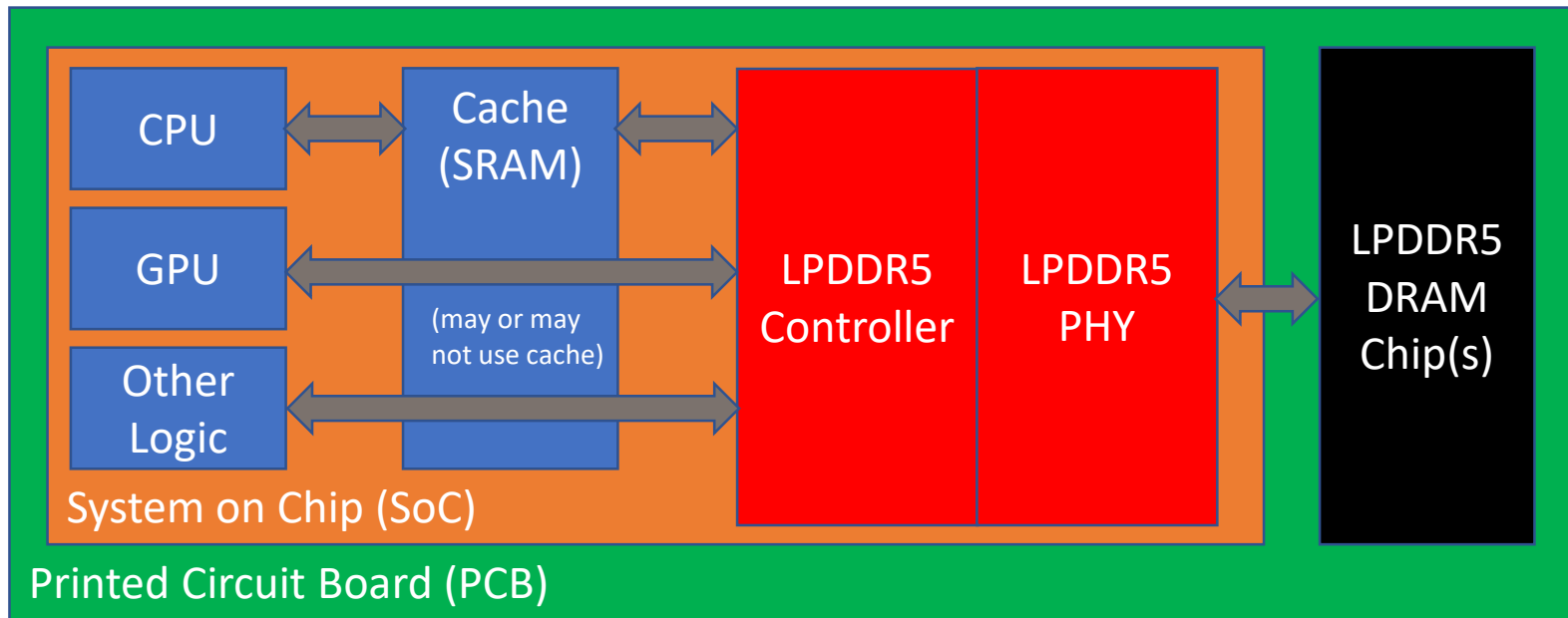
- What is DRAM, what is DDR, and why do we use it
- Market predictions: the four waves of LPDDR5
- Comparing different memory technologies
- Conclusions

A brief introduction to memory

- 3 main categories of memory from system perspective:
 - On-die memory (on same System on Chip as CPU and logic)
 - Usually SRAM, embedded DRAM, or embedded Non-Volatile Memory (NVM)
 - Off die RAM
 - Usually DRAM (including LPDDR5) or SRAM
 - Off die Non-Volatile Memory (NVM)
 - Many types including NAND Flash, NOR Flash, others



Where does LPDDR5 fit in the system?



Typical system - not to scale – yours may be different

LPDDR5 in non-mobile uses

	DDR1/ LPDDR1	DDR2/ LPDDR2	DDR3/ LPDDR3	DDR4/ LPDDR4	DDR5/ LPDDR5
Database	Commonly DDRx				Both
Server					
Compute/AI					
Networking					
Client					
Ultra-thin	Commonly LPDDRx				Both
AR/VR					(Didn't exist or DRAM not commonly used)
Automotive					
Tablet					
Phone					

What do we want from LPDDR5?

Feature or property	Which markets need it	How LPDDR5 satisfies that need
Less energy per bit transferred	All, particularly mobile	Reduced voltage, new low-power features
High bandwidth	All	Support up to 6400MT/s per current standard
Reliability and Longevity	Automotive	As was the case with LPDDR4, we predict that memory manufacturers will make LPDDR5 products that incorporate high temperature operation ability, automotive certifications, and multi-year availability
More capacity	Mobile, Compute, Client, Storage DRAM Buffer (SSD)	Standard allows for up to 32Gbit per die and multi-die packages (subject to memory manufacturer availability)
“Right Sized” memory with correct ratio of bandwidth:capacity	Networking, AI, Video	Higher LPDDR5 bandwidth improves bandwidth:capacity ratio for applications that need more bandwidth with less capacity, compared to DDRx solutions with less bandwidth

Four Waves of LPDDR5 (a market prediction)



First Wave

Mobile Devices

Cares about:

Power, Bandwidth, Capacity

SoC Design Starts:

2018+

Second Wave

Networking, AI, HPC

Cares about:

Bandwidth, “right” capacity

SoC Design Starts:

2019+

Third Wave

Automotive AD/ADAS

Cares about:

Reliability, Longevity

SoC Design Starts:

2020+

Fourth Wave

Everything else

Cares about:

Cost

SoC Design Starts:

2021+

LPDDR5 Markets – Mobile

- Battery-operated mobile devices are a large market for LPDDR
- System requirements:
 - Occasional use at very high data rates
 - low power in moderate use
 - extended standby power
 - Large capacity
- Lowered voltage, and Dynamic Voltage and Frequency Scaling (DVFS) helps to meet system power requirements



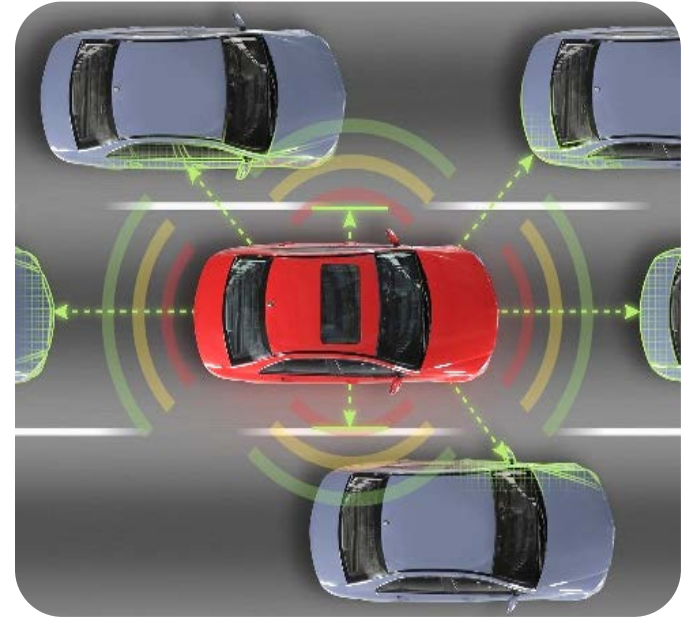
LPDDR5 Markets – Networking, AI, Video

- Networking, AI, Video
- Processing large quantities of data with short tenure
- System requirements:
 - “Right Sized” memory with high bandwidth
 - 16-bit interface per die @ 6400MT/s
= 102Gbit/s peak bandwidth per LPDDR5 die
 - 2x bandwidth of DDR4-3200 & less energy per bit



LPDDR5 Markets - Automotive

- ADAS and Autonomous Driving control
- Processing sensor data
- System requirements:
 - High reliability
 - ASIL Certification
 - Optional link ECC function
 - High temperature
 - AEC Q100 Certification
 - High data rates
 - Longevity (long-term memory supply)



LPDDR5 Markets – Consumer and client

- “Smart Screen” applications, Tablets based on mobile devices, Client/laptop, VR/AR, Cameras, displays, TV, ...
- General purpose processing, video
- System Requirements:
 - Low cost
 - High bandwidth
 - High capacity (in some cases)



LPDDR5 Ecosystem – Ready Now

Ecosystem item	Industry status
LPDDR5 standard	Released February 2019
LPDDR5 devices	Engineering samples available from memory vendors
LPDDR5 models	IBIS and other I/O models available from memory vendors
LPDDR5 verification IP	Verification IP available from EDA vendors
LPDDR5 controller design IP	Silicon-proven testchips from IP vendors
LPDDR5 PHY design IP	Silicon-proven testchips from IP vendors
LPDDR5 test equipment	Available (more details in 2:30PM session)

LPDDR5 test board



TC30 LPDDR5 test board with Test Chip and Memory soldered down

Testchip is on top of PCB (under socket)
LPDDR5 device is on bottom of PCB (not shown)

Feature Comparison vs other LPDDR

	LPDDR3	LPDDR4	LPDDR4X	LPDDR5
Vdd1 (Core 1 power)	1.8v	1.8v	1.8v	1.8v
Vdd2 (Core 2 power / Input buffer power)	1.2v	1.1v	1.1v	1.05v/0.9v
Vddq (I/O buffer power)	1.2v	1.1v	0.6v	0.5v/0.3v
Max data rate per current standard	2133MT/s	4267MT/s	4267MT/s	6400MT/s

- Reducing IO buffer voltage saves V^2/R power
- LPDDR5 Dynamic voltage scaling for core and I/O
 - High/Low range shown for LPDDR5
- Advances in I/O technology and system assumption allow higher speed with less voltage

Feature comparison vs DDR4

Comparison	DDR4	LPDDR5
Common system assumption	Placed on DIMM. Used in desktop/client machine or server.	Placed on PCB. Used in mobile application.
Max data rate	3200MT/s	6400MT/s, +
Capacity per die (standard/common)	2-32Gbit; 4 and 8Gbit common	2-32Gbit, 8Gbit+ predicted
Data bits per die	4, 8 or 16	8 or 16
Frequency change	Requires DLL reset, so slower	Can do rapid frequency change
Min clock frequency	625MHz (DLL on)	5MHz

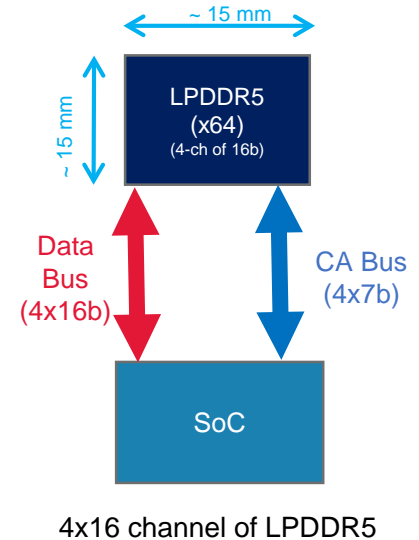
- LPDDR5 system assumption is for less capacity and point-to-point (or P-2P) connections
- Allows higher data rate with fast frequency change and no DLL

How did LPDDR get into Automotive?

- LPDDR is used in many mobile devices
 - If it hangs, reboot it
 - No error correction
- DDR is used in server/storage applications
 - High reliability
 - Strong error correction and RAS
- Wouldn't we expect DDR to be the basis for automotive DRAM?

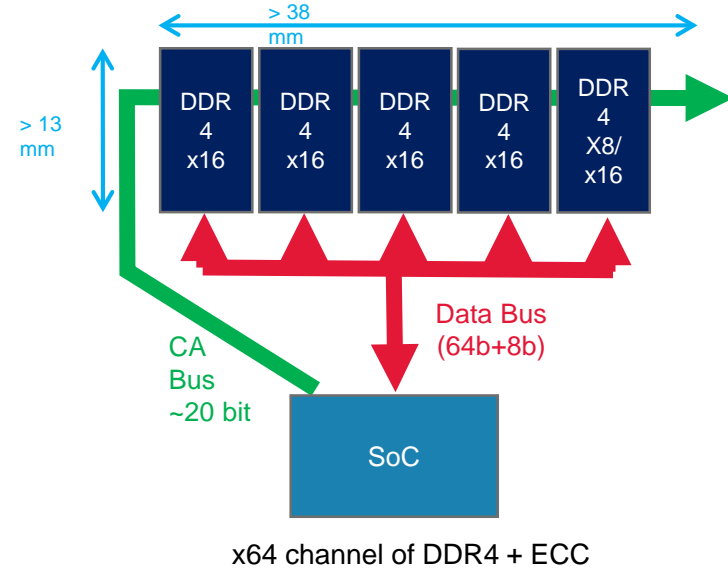
Automotive LPDDR5 System example

- Dual, Quad or 8-die package x64
 - Total bandwidth: 51.2GByte/sec for QDP or 8DP
 - Memory capacity: 2-32Gbit/die
 - 8Gbit/die+ predicted to be common
- Advantages:
 - Compact DRAM PCB Area: ~ 225 mm²
 - Optional Link ECC available
- But...
 - Cannot implement sideband ECC
 - In-band ECC is possible

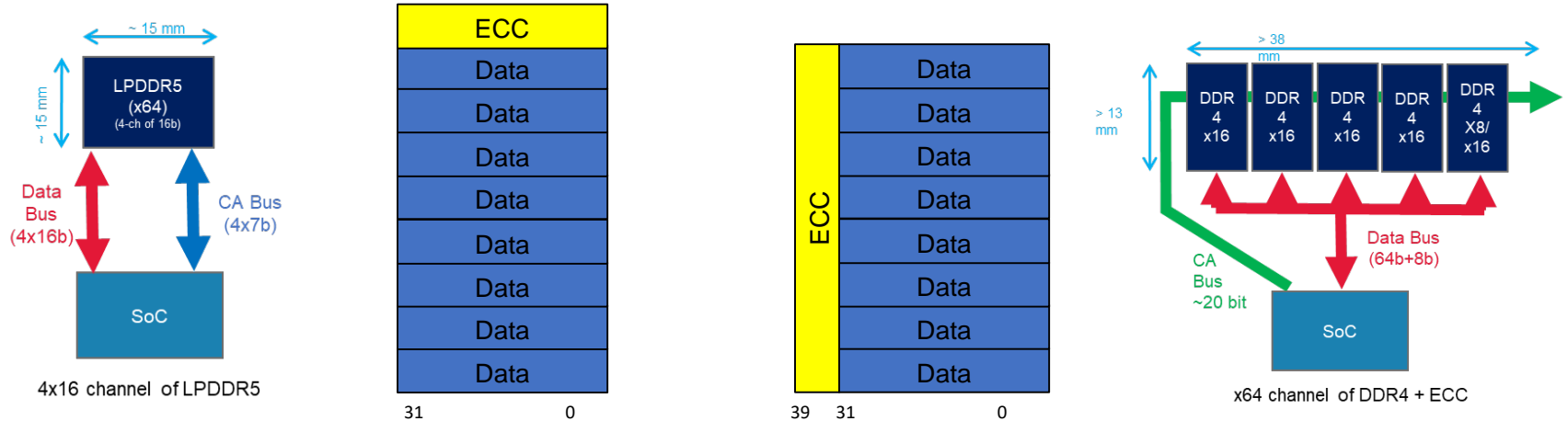


Automotive DDR4 System Example

- X64 channel (4x16 parts) with ECC
 - Total bandwidth: 25.6 GBps
 - Memory capacity: 2-32Gbit/die
 - 4Gbit/die and 8Gbit/die common
- Advantages
 - DDR4 is low cost DRAM
 - System Sideband ECC
- But...
 - 3200MT/s data rate per standard
 - No X32 devices
 - Total DRAM Area: ~ 500 mm²



in-line or in-band ECC vs sideband ECC



- Inline ECC (left, LPDDR5 example) - stores Error Correction Codes in the same memory as the data
 - more area efficient
- Sideband ECC (right, DDR4 example) stores Error Correction Codes in a different memory device
 - more bandwidth efficient – but note difference in data rates

Conclusions

- LPDDR5 is next-generation Low Power DRAM
- Improved Bandwidth vs previous DDR and LPDDR families
- Reduced energy per bit with lower operating voltage and Dynamic Voltage and Frequency Scaling
- Mobile, Consumer, Client, AI, Networking, HPC and Automotive products can use LPDDR5
- LPDDR5 is ready for design starts now