EE315A
VLSI Signal Conditioning Circuits

- Spring 2013 -

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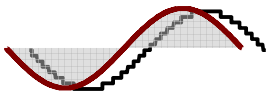

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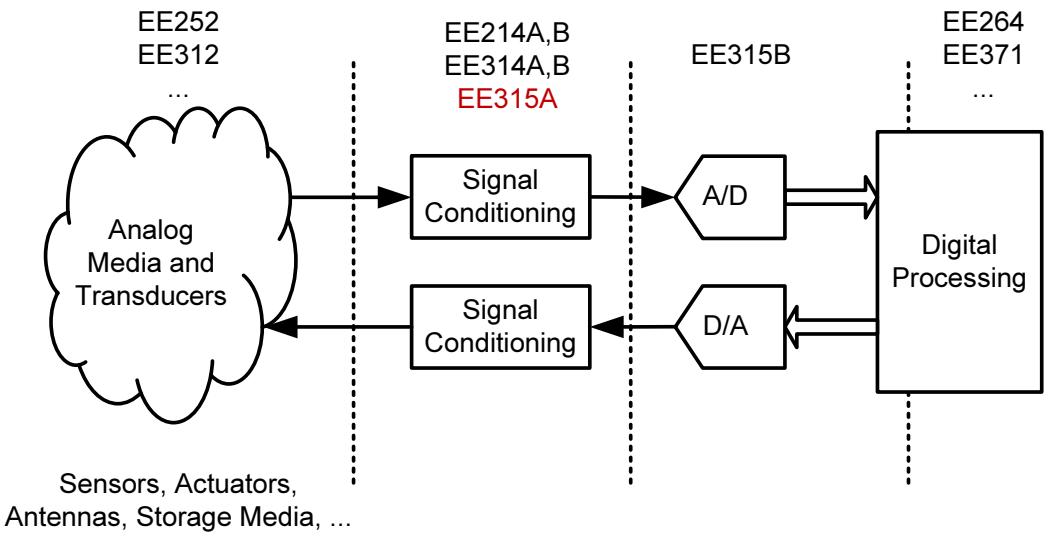
Mixed Signal System



Signal Conditioning

(′sig·nəl kən′dish·ən·iŋ) (*communications*) Processing the form or mode of a signal so as to make it intelligible to or compatible with a given device, such as a data transmission line, including such manipulation as pulse shaping, pulse clipping, digitizing, and linearizing.

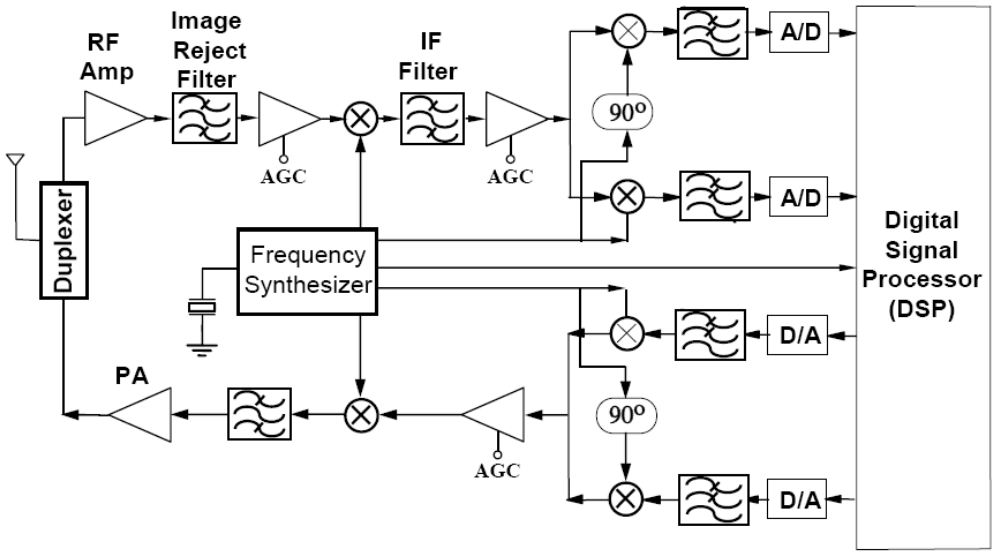
[www.answers.com]

In electronics, signal conditioning means manipulating an analogue signal in such a way that it meets the requirements of the next stage for further processing.

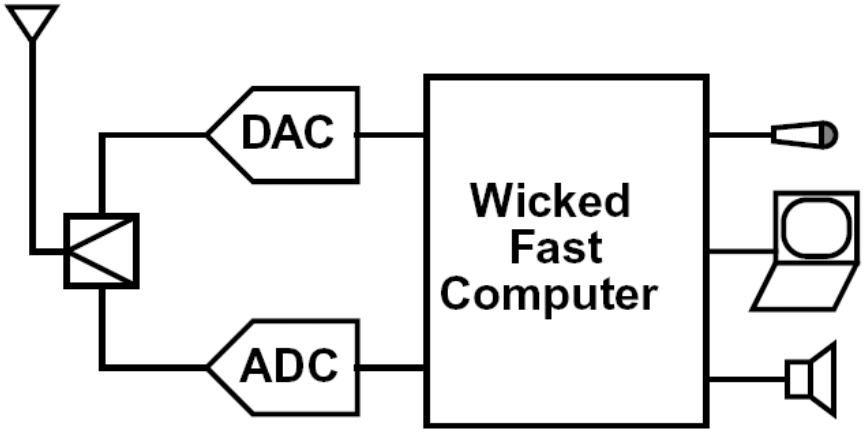
Signal conditioning can include amplification, filtering, converting, range matching, isolation and any other processes required to make sensor output suitable for processing after conditioning.

[http://en.wikipedia.org]

Example: Cellular Phone

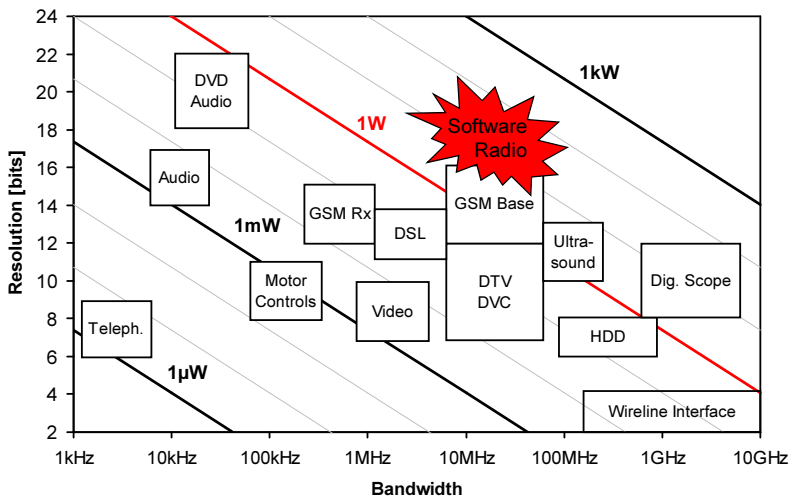


The Vision – "Software Radio"



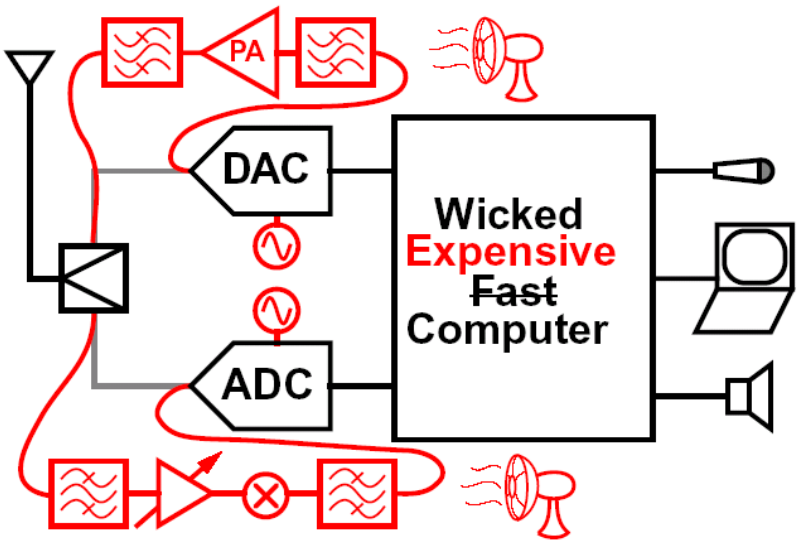
[Schreier, "ADCs and DACs: Marching Towards the Antenna," GIRAFE workshop, ISSCC 2003]

ADC for Software Radio



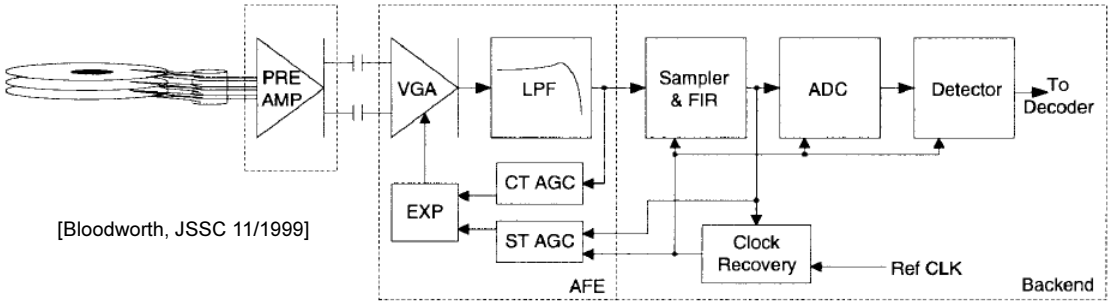
- Ouch!

Reality



[Schreier, "ADCs and DACs: Marching Towards the Antenna," GIRAFE workshop, ISSCC 2003]

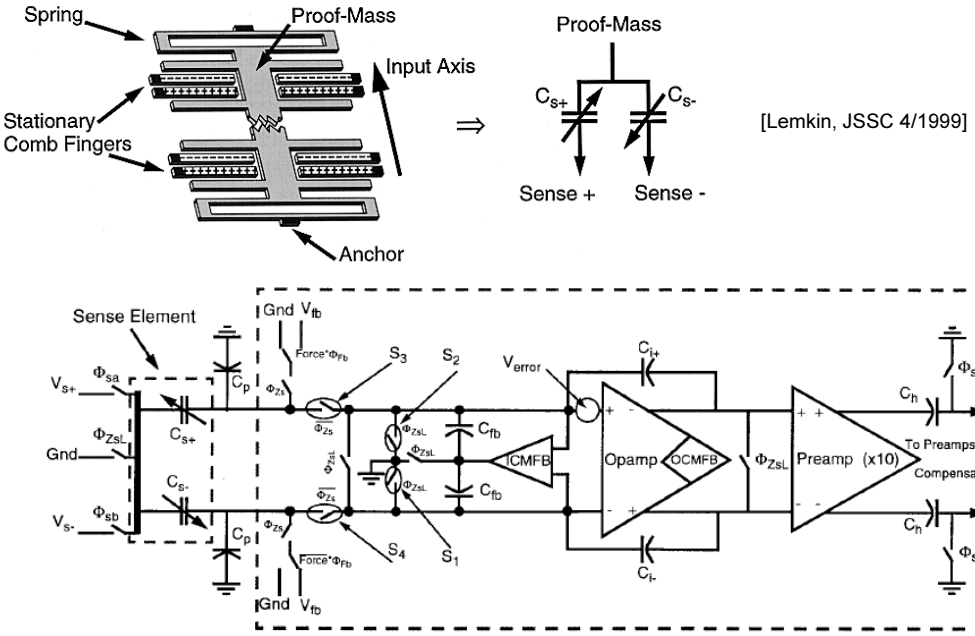
Example: Hard Disk Drive



[Bloodworth, JSSC 11/1999]

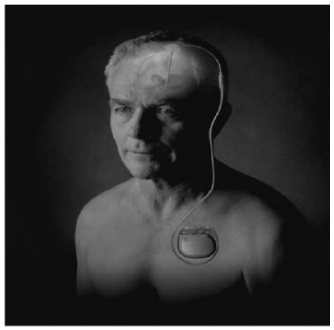
AGC Specifications		LPF Specifications	
Input Signal Range	45 mVppd < V_{IN} < 500 mVppd	LPF Bandwidth	20 MHz ≤ f_c ≤ 120 MHz
Output Target	1.400 Vppd	Cutoff Variation	< ± 2.5 %
PGA Gain Settings	-3 dB, 3 dB, 9 dB	Group Delay Variation ($0.30f_c$ to f_c)	< 5 %
VGA Gain Range	-24 dB ≤ A_V ≤ 0 dB	Group Delay Variation (f_c to $1.75f_c$)	< 8 %
w/Extended Range	-30 dB ≤ A_V ≤ 6 dB	Group Delay Adjustment	± 30 %
AFE THD	< 1.0 %	Boost	0 dB to 15 dB at f_c
AFE SNR	> 35 dB	CT Acquisition Time	< 10 bytes
AFE Output Offset	< 5.0 mV	Power Dissipation	< 250 mW

Example: MEMS Accelerometer



Example: Neural Field Potential Amplifier

Electroencephalography (EEG) = recording of electrical activity along the scalp produced by the firing of neurons within the brain



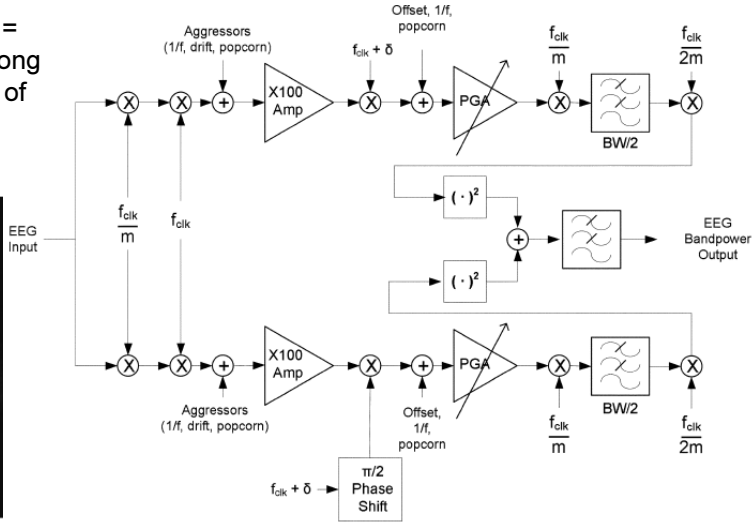


Fig. 1. Key elements of a deep-brain stimulator. The battery and circuitry form the IPG, which is implanted in the chest. The electrodes are placed into a specific neural circuit within the brain. Connections are made between the IPG and electrodes via a lead system placed in the neck.

[Avestruz, JSSC 12/2008]

Course Objective

- Acquire a thorough understanding of the basic principles, challenges and limitations in signal conditioning circuit design
  - Focus on concepts that are unlikely to expire
  - Preparation for further study of state-of-the-art "fine-tuned" realizations
- Strategy
  - Acquire basic intuition by studying a selection of commonly used circuit and design techniques
  - Acquire depth through a design project that entails design, optimization and thorough characterization of a filter circuit in modern technology

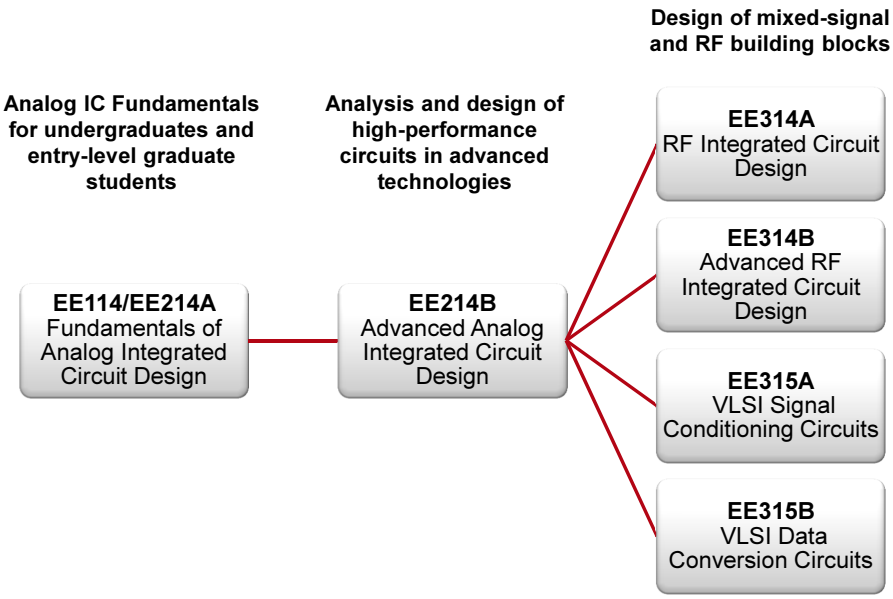
Staff and Website

- Teaching assistants
  - TBD
- Administrative support
  - Ann Guerra, Allen 207
- Lecture videos are provided on the web, but please come to class to keep the discussion intercative
- Web page: http://ccnet.stanford.edu/ee315a
  - Check regularly, especially the "bulletin board" section
  - Only enrolled students can register for ccnet access
    - We synchronize the ccnet database with axess.stanford.edu manually, ~ once per day during first week of instruction

Preparation

- Course prerequisites
  - EE214B or equivalent
    - Device physics and models
    - Transistor level analog circuits, elementary gain stages
    - Frequency response, feedback, noise
  - Prior exposure to Spice, Matlab
  - Basic signals and systems
    - Laplace and z-transforms
- Please talk to me if you are not sure if you have the required background

Analog Circuit Sequence



Assignments

- Homework: (30%)
  - Handed out on Thu, due following Thu after lecture (1 pm)
  - Lowest HW score is dropped in final grade calculation
- Project: (30%)
  - Design of a high performance filter circuit
  - Architecture design using idealized components
  - Implementation of a critical sub-block at the transistor level
  - Project report in the format of an IEEE journal paper
- Final Exam (40%)

Honor Code

- Please remember you are bound by the honor code
  - I will trust you not to cheat
  - I will try not to tempt you
- But if you are found cheating it is very serious
  - There is a formal hearing
  - You can be thrown out of Stanford
- Save yourself and me a huge hassle and be honest
- For more info
  - http://www.stanford.edu/dept/vpsa/judicialaffairs/guiding/pdf/honorcode.pdf

Tools and Technology

- Primary tools
  - Cadence Virtuoso Schematic Editor
  - Cadence Virtuoso Analog Design Environment
  - Cadence SpectreRF simulator
  - You can use your own tools/setups “at own risk“
- Getting started
  - Read “remote connection” tutorial
  - Read “virtuoso tutorial”
  - All tool related documents are in the “CAD” section of the website
- EE315A Technology
  - 0.18-μm CMOS
  - BSIM3v3 models provided under /usr/class/ee315a/models
  - Same models are used in EE214B

Reference Books

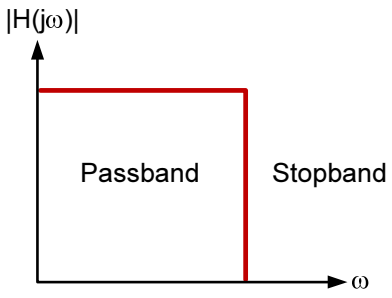
- **Schauman, Xiao and Van Valkenburg, *Design of Analog Filters*, 2nd Edition, Oxford University Press, 2009**
- **Chan Carusone, Johns, Martin, *Analog Integrated Circuit Design*, 2nd Edition, Wiley, 2011**
- Deliyannis, Sun, and Fidler, *Continuous-Time Active Filter Design*, CRC Press 1998, http://www.crcnetbase.com/isbn/9780849325731
- Gray, Hurst, Lewis and Meyer, *Analysis and Design of Analog Integrated Circuits*, 5th Edition, Wiley, 2008 (Chapter 12)
- Laker and Sansen, *Design of Analog Integrated Circuits and Systems*, McGraw-Hill, 1994
- Gregorian and Temes, *Analog MOS Integrated Circuits for Signal Processing*, Wiley, 1986
- Williams and Taylor, *Electronic Filter Design Handbook*, 3rd edition, McGraw-Hill, 1995
- Zverev, *Handbook of Filter Synthesis*, Wiley, 1967

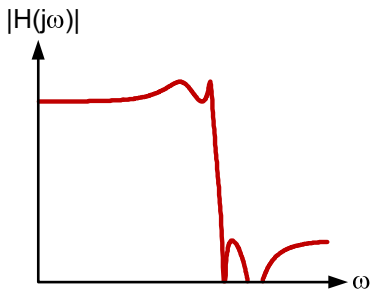
Course Topics

- Continuous time filters
  - Biquad and ladder-based designs
  - Active-RC and G_m-C filters
- Switched capacitor filters
  - Approximation errors
  - Circuit simulation (periodic ac and noise analysis)
- Design of Operational Transconductance Ampilfiers (OTAs)
  - Analysis and design of fully differential implementations
  - G_m/I_D-based optimization (BW – noise – power dissipation)
- Precision Analog Circuit Techniques
- Sensor interface examples
- Layout techniques

The Filter Approximation Problem

- Ideal Filter
  - Brick-wall characteristic
  - Flat magnitude response in the passband
  - Infinite attenuation in the stopband
- Practical filter
  - Ripple in either or both the passband and stopband
  - Limited attenuation in the stopband

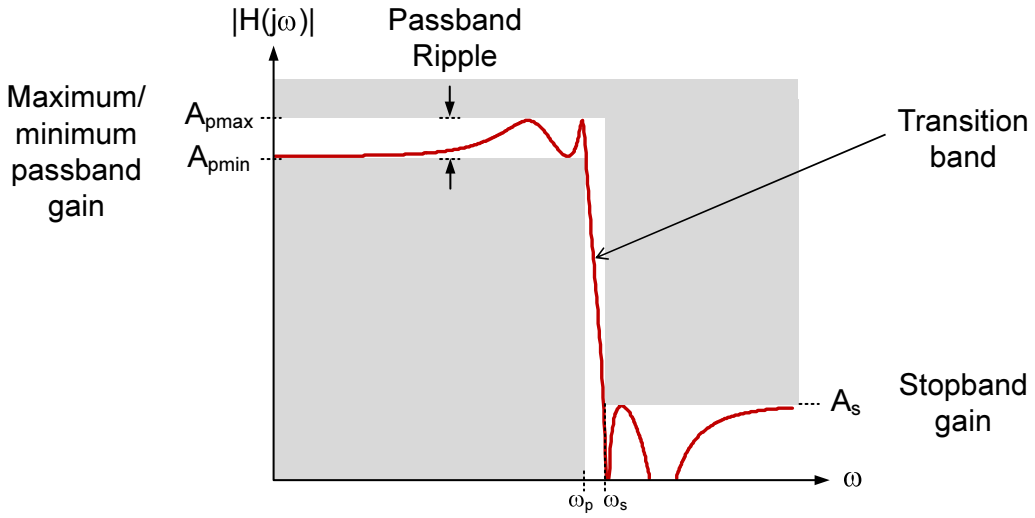




Filter Design

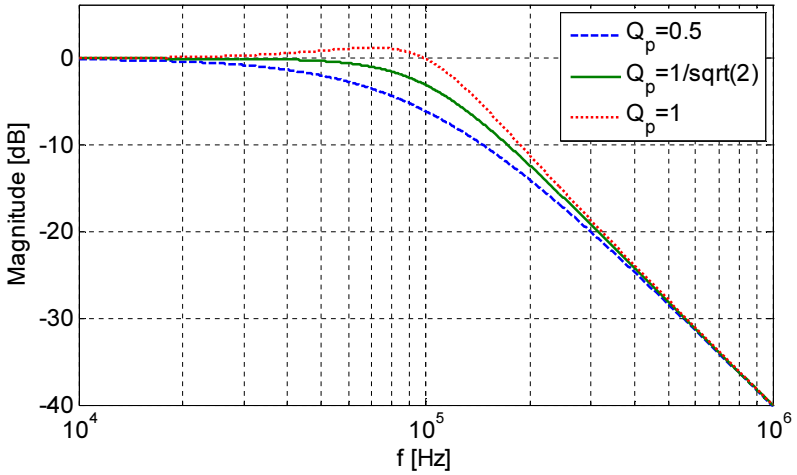
- Ideal filters are non-causal or otherwise impractical
- No global optimization techniques known
- In practice, chose from several known solutions
  - Butterworth, Elliptic, Bessel, …
- The overall goal of filter design is to approximate the ideal response by one that implements a reasonable compromise between filter complexity (number of poles and zeros) and approximation error
- Filter design, in general, requires a compromise between magnitude response, phase response, step response, complexity, etc.

Lowpass Filter Template



- Magnitude response is fully specified by A_{pmin}, A_{pmax}, A_s, ω_p, ω_s

Second Order Lowpass Filter



$$H(s) = \frac{1}{1 + \frac{s}{\omega_P Q_P} + \frac{s^2}{\omega_P^2}}$$

- Magnitude response is “maximally flat” (no peaking) for Q_P = 1/sqrt(2)

Pole Positions

- The poles are the roots of the denominator polynomial

$$1 + \frac{s}{\omega_0 Q_P} + \frac{s^2}{\omega_0^2} = 0$$

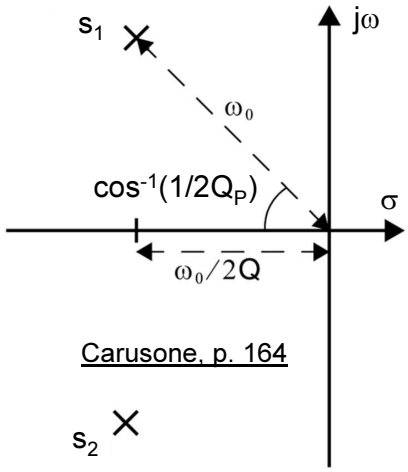
$for\ Q_P > 0.5 \qquad s_{1,2} = -\frac{\omega_0}{2Q\_P}\left(1 \pm j\sqrt{4Q_P^2 - 1}\right)$

→ **Complex Conjugate Poles**

$for\ Q_P \leq 0.5 \qquad s_{1,2} = -\frac{\omega_0}{2Q}\left(1 \pm \sqrt{1 - 4Q_P^2}\right)$

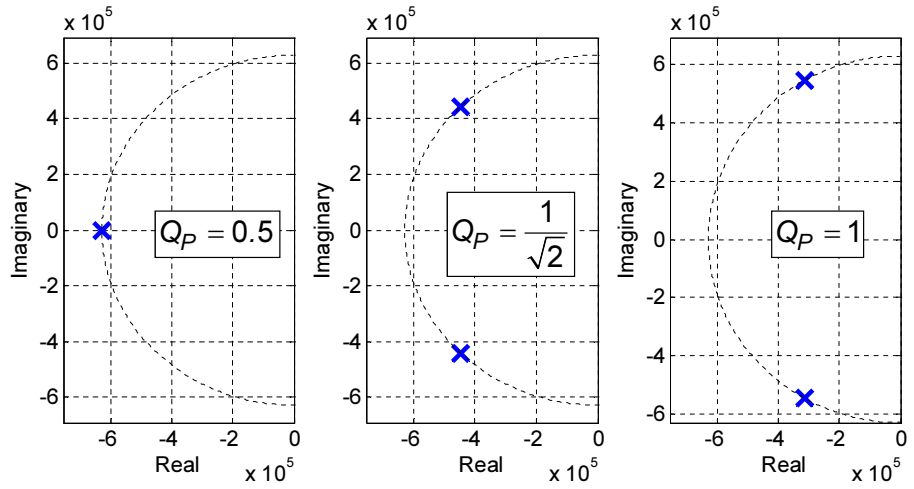
→ **Real Poles**

Location in the s-plane for $Q_P > 0.5$



Carusone, p. 164

Pole Positions

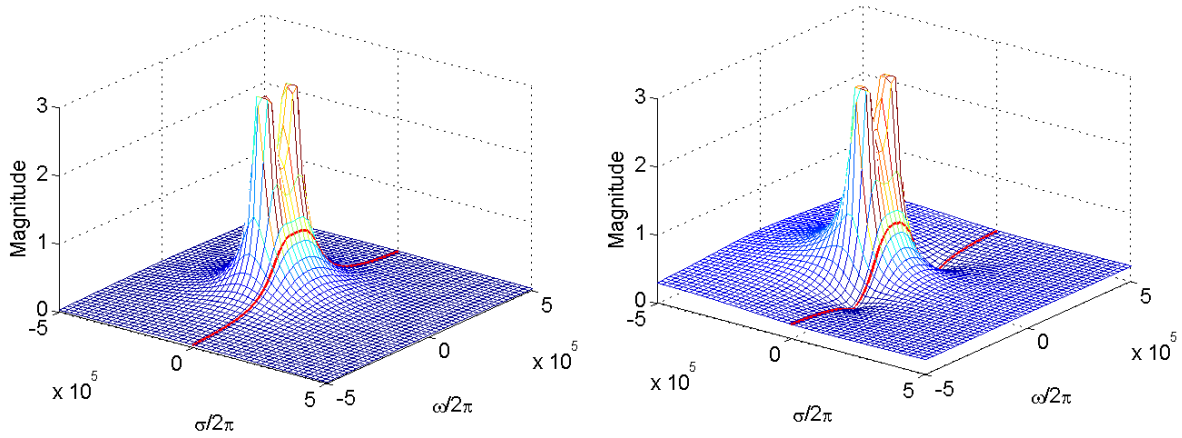


$$\psi = \cos^{-1}\left(\frac{1}{2Q_P}\right) = 0^\circ \qquad \psi = \cos^{-1}\left(\frac{1}{2Q_P}\right) = 45^\circ \qquad \psi = \cos^{-1}\left(\frac{1}{2Q_P}\right) = 60^\circ$$

Improvements

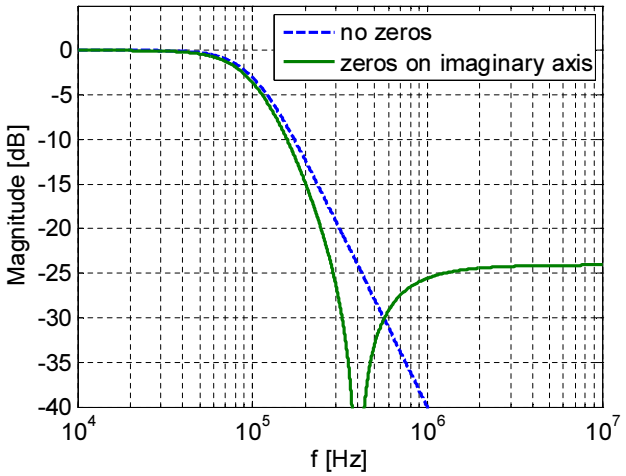
- A maximally flat response is great, but how can we make the roll-off steeper?
- Let's look at
  - Imaginary zeros
  - Increasing the filter order
  - High-Q poles
  - High-Q poles and imaginary zeros

Adding Zeros on the Imaginary Axis



"pegs"

Bode Plot

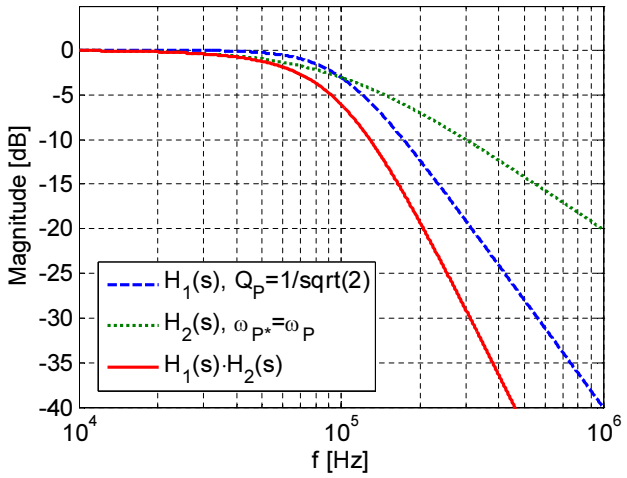


$$H(s) = \frac{1 + \left(\frac{s}{\omega_Z}\right)^2}{1 + \frac{s}{\omega_P Q_P} + \left(\frac{s}{\omega_P}\right)^2}$$

$$\left|H(j\omega)\right|_{\omega \to \infty} = \left(\frac{\omega_P}{\omega_Z}\right)^2$$

- Steeper roll-off at the expense of reduced stopband rejection

Adding Another Pole



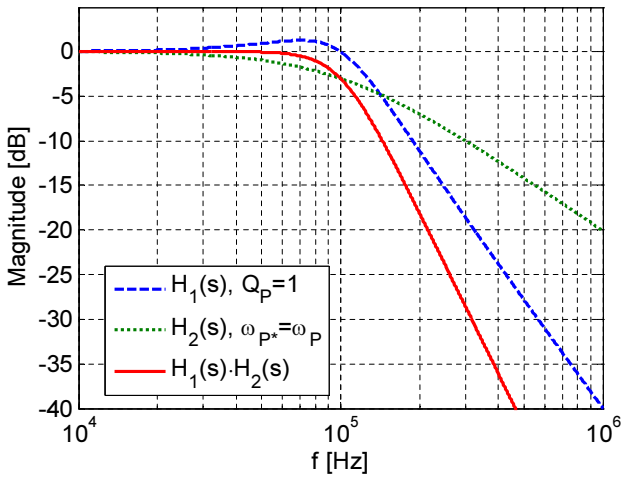
$$H(s) = H_1(s) \cdot H_2(s)$$

$$H_1(s) = \frac{1}{1 + \frac{s}{\omega_P Q_P} + \left(\frac{s}{\omega_P}\right)^2}$$

$$H_2(s) = \frac{1}{1 + \left(\frac{s}{\omega_{P^*}}\right)}$$

- As expected, steeper roll-off, but transition is not all that sharp
- Can fix this issue by increasing Q_P of $H_1(s)$!

Utilizing Peaking in $H_1(s)$



$$H(s) = H_1(s) \cdot H_2(s)$$

$$H_1(s) = \frac{1}{1 + \frac{s}{\omega_P Q_P} + \left(\frac{s}{\omega_P}\right)^2}$$

$$H_2(s) = \frac{1}{1 + \left(\frac{s}{\omega_{P^*}}\right)}$$

- Win-win improvement
  - Passband flat, roll-off steeper

n^{th} Order Generalization

- Stephen Butterworth showed in 1930 that the magnitude response of an n^{th} order maximally flat lowpass filter is given by

$$|H(j\omega)| = \frac{1}{\sqrt{1+\left(\frac{\omega}{\omega_P}\right)^{2n}}}$$

- This magnitude response is monotonically decreasing and satisfies

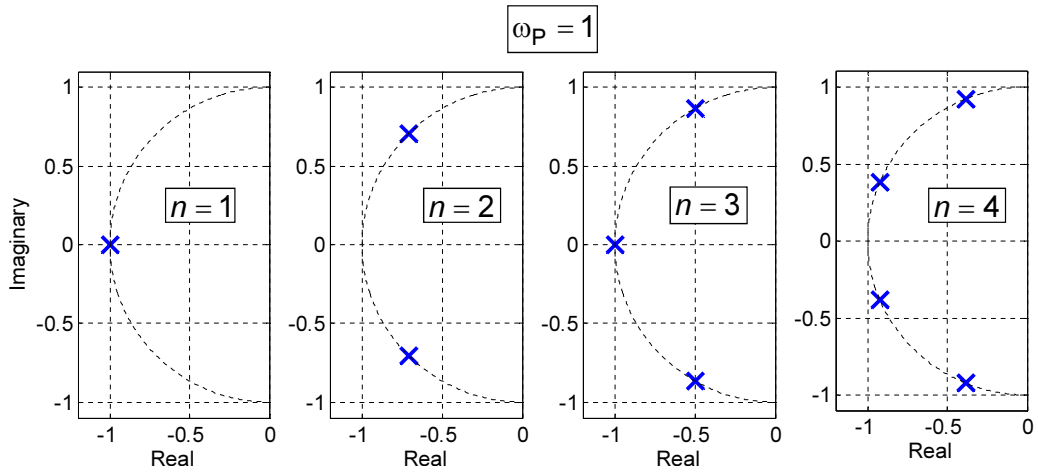
$$\left.\frac{d^k|H(j\omega)|}{d\omega^k}\right|_{\omega=0} = 0 \quad \text{for} \quad 1 \le k \le 2n-1$$

- The corresponding pole locations can be determined using

$$|H(s)|^2 = H(s)\cdot H(-s) = \frac{1}{1+\left(\frac{-s^2}{\omega_P^2}\right)^n} \qquad \frac{-s^2}{\omega_P^2} = (-1)^{1/n} = e^{\frac{j(2k-1)\pi}{n}} \qquad k = 1,2,3\ldots,n$$

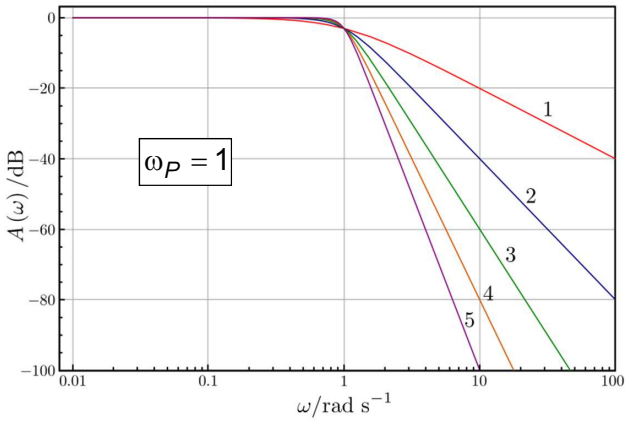
Pole Locations

- The poles lie equally spaced (in angle) on a circle in the s-plane centered at the origin with radius ω_P
- The LHP roots are taken to be the poles of H(s), while those in the RHP are regarded as the poles of H(–s)



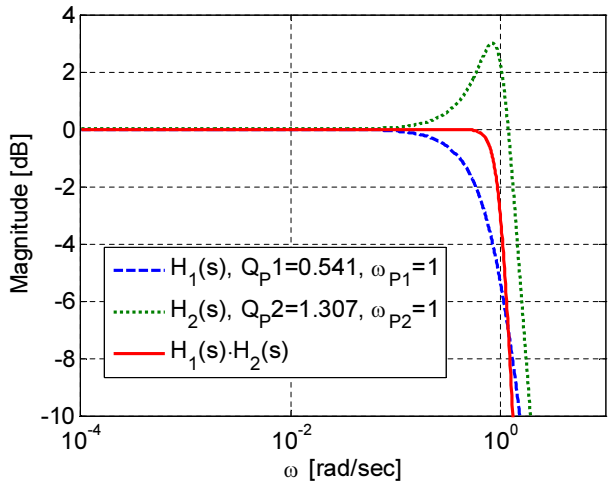
Magnitude Response and Coefficients

http://en.wikipedia.org/wiki/Butterworth_filter



n	Denominator Polynomial
1	$(s + 1)$
2	$s^2 + 1.4142s + 1$
3	$(s + 1)(s^2 + s + 1)$
4	$(s^2 + 0.7654s + 1)(s^2 + 1.8478s + 1)$
5	$(s + 1)(s^2 + 0.6180s + 1)(s^2 + 1.6180s + 1)$
6	$(s^2 + 0.5176s + 1)(s^2 + 1.4142s + 1)(s^2 + 1.9319s + 1)$
7	$(s + 1)(s^2 + 0.4450s + 1)(s^2 + 1.2470s + 1)(s^2 + 1.8019s + 1)$
8	$(s^2 + 0.3902s + 1)(s^2 + 1.1111s + 1)(s^2 + 1.6629s + 1)(s^2 + 1.9616s + 1)$

A Closer Look at n=4



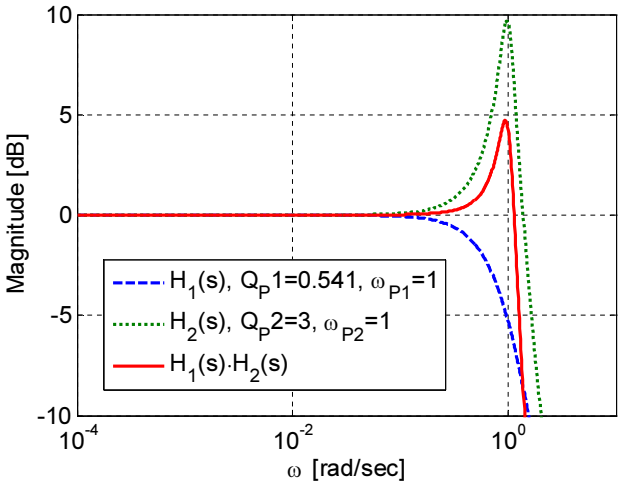
$$H(s) = H_1(s) \cdot H_2(s)$$

$$H_1(s) = \frac{1}{1 + \frac{s}{\omega_{P1} Q_{P1}} + \left(\frac{s}{\omega_{P1}}\right)^2}$$

$$H_2(s) = \frac{1}{1 + \frac{s}{\omega_{P2} Q_{P2}} + \left(\frac{s}{\omega_{P2}}\right)^2}$$

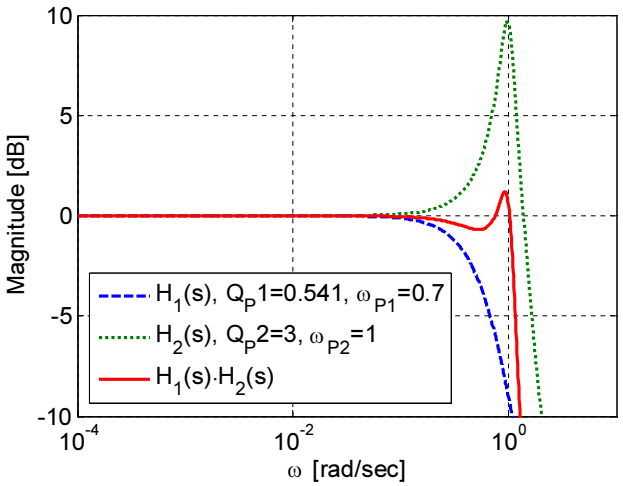
$$\psi = \cos^{-1}\left(\frac{1}{2Q_P}\right) \qquad Q_{P1} = \frac{1}{2\cos(22.5^\circ)} = 0.541 \qquad Q_{P2} = \frac{1}{2\cos(67.5^\circ)} = 1.307$$

Increasing Q_{P2}



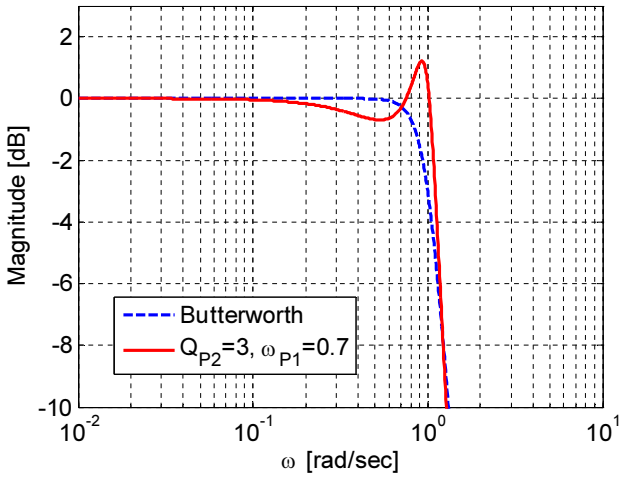
- Helps make the roll-off steeper, but introduces peaking
- We can try to alleviate this problem this by reducing ω_{P1}

Increased Q_{P2}, Reduced ω_{P1}



- This may not a bad choice of we can tolerate some peaking or ripple

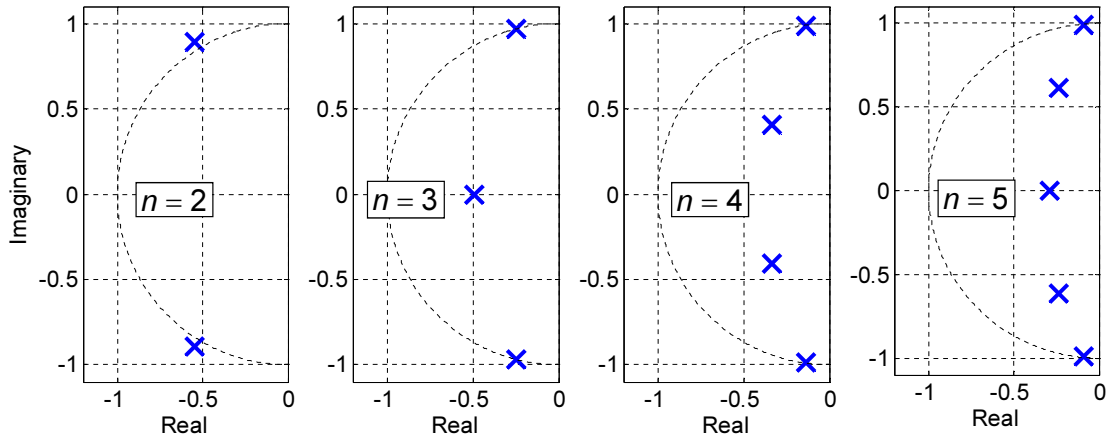
Comparison with Original Butterworth



- How can we optimize this situation, i.e. minimize the transition band for a given tolerable peaking (or "ripple") in the passband?

Chebyshev1 Filter Approximation

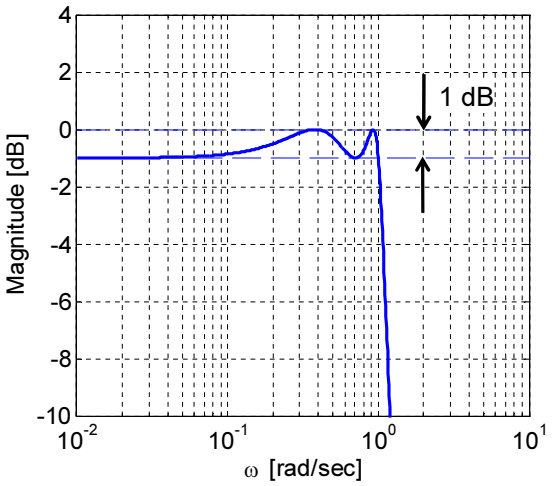
- Fortunately someone has already figure this out
- The "Chebyshev1" filter approximation minimizes the error between the idealized response and the actual filter, with the passband ripple as a parameter (1dB for examples below)



Matlab Code

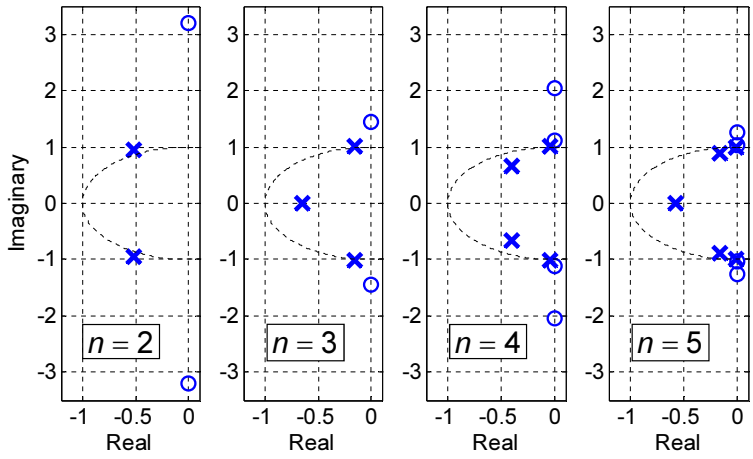
```
wp = 1; % Edge of passband
R = 1;  % Passband ripple in dB
[z, p, k] = cheby1(4, R, wp, 's');
sys = zpk(z, p, k);
w = logspace(-2, 1, 1000);
[mag, phase] = bode(sys, w);
db = 20*log10(reshape(mag, 1, length(w)));

figure(1)
semilogx(w, db, 'linewidth', 2); hold on;
plot([w(1) w(end)], [0 0], '--');
plot([w(1) w(end)], [-1 -1], '--');
set(gca, 'fontsize', 14);
xlabel('\omega [rad/sec]')
ylabel('Magnitude [dB]');
axis([min(w) max(w) -10 4])
grid;
```



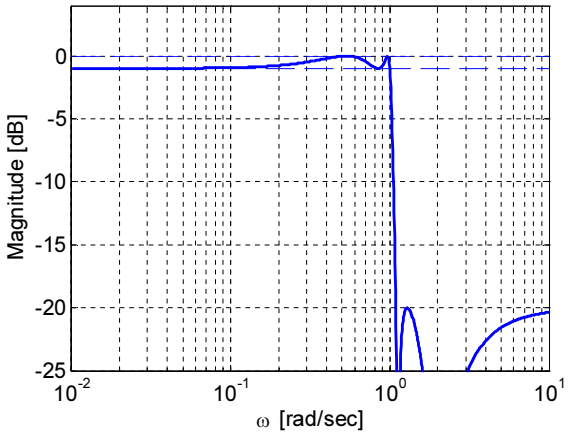
Elliptic (Cauer) Filter Approximation

- The Elliptic filter approximation combines our previous ideas and adds imaginary zeros to sharpen the transition band
- This approximation has the passband ripple and stopband attenuation as a parameter (1dB and 20dB, respectively, for example below)



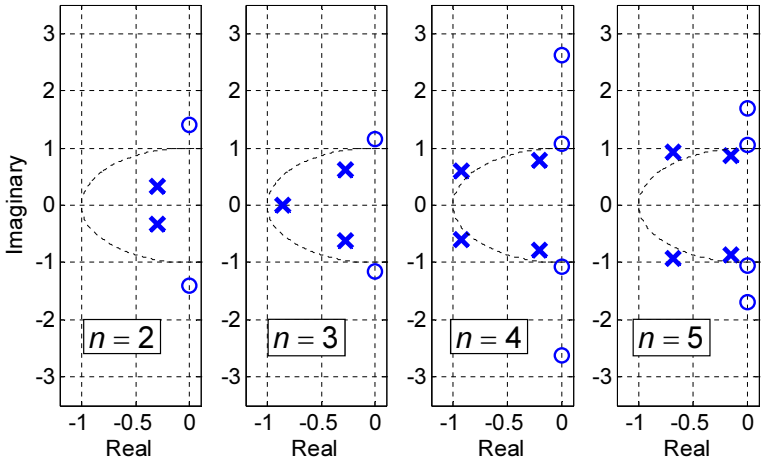
Matlab Code

```
wp = 1; % Edge of passband
Rp = 1;  % Passband ripple in dB
Rs = 20; % Stopband attenuation
[z, p, k] = ellip(4, Rp, Rs, wp, 's');
```



Chebyshev2 Filter Approximation

- No ripple in the passband, but finite stopband attenuation and ripple due to imaginary zeros
- This approximation takes the stopband attenuation as a parameter (20 dB in the example below)

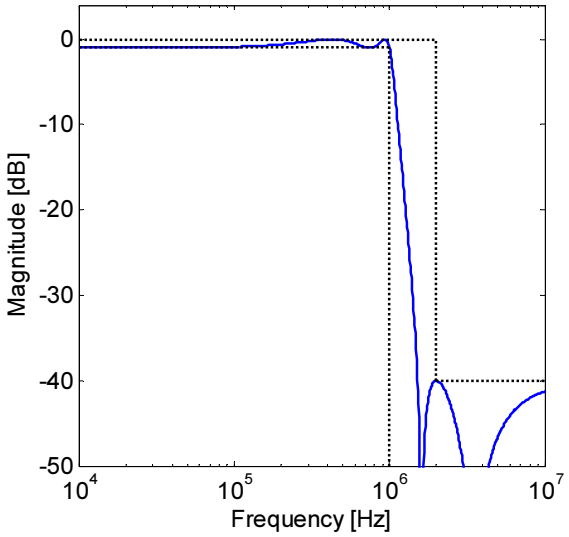


Design Example

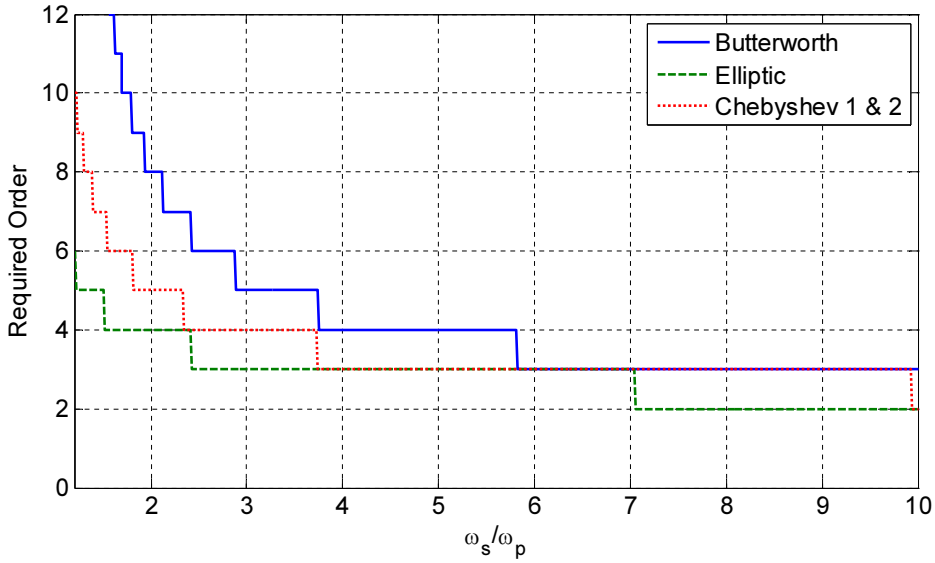
```
wp=2*pi*1e6; % Passband edge
ws=2*pi*2e6; % Stopband edge
Rp=1;  % Passband ripple
Rs=40; % Stopband attenuation

% Determine required order and synthesize
[N, wp] = ellipord(wp, ws, Rp, Rs, 's');
[z, p, k] = ellip(N, Rp, Rs, wp, 's');

sys = zpk(z, p, k);
f = logspace(4, 7, 1000);
[mag, phase] = bode(sys, 2*pi*f);
db = 20*log10(reshape(mag, 1, length(f)));
figure(1)
semilogx(f, db, 'linewidth', 2);
```

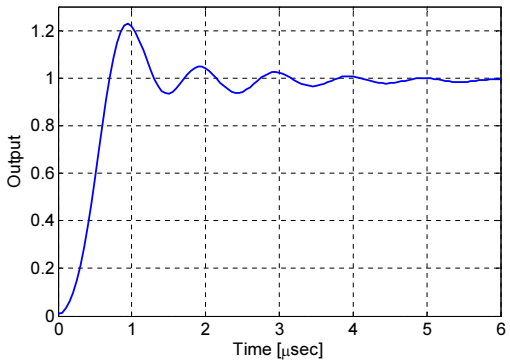


Filter Order for R_p=1dB, R_s=40dB



- Why not always use an Elliptic filter?

Step Response of Design Example



- Overshoot and other forms of pulse deformation can be problematic in some systems
  - Consider e.g. oscilloscopes, pulse-based data links, etc.
- The pulse deformation is mostly due to the fact that different frequency components pass the filter with different time delays
  - This is called phase distortion

Phase Distortion (1)

- Consider a filter with transfer function

$$H(j\omega) = |H(j\omega)| e^{j\phi(\omega)}$$

- Apply two sine waves at different frequencies

$$v_{in}(t) = A_1 \sin(\omega_1 t) + A_2 \sin(\omega_2 t)$$

$$v_{out}(t) = A_1 |H(j\omega_1)| \sin(\omega_1 t + \phi(\omega_1)) + A_2 |H(j\omega_2)| \sin(\omega_2 t + \phi(\omega_2))$$

$$= A_1 |H(j\omega_1)| \sin\left(\omega_1 \left[t + \underbrace{\frac{\phi(\omega_1)}{\omega_1}}_{\text{Phase delay } \tau_{d1}}\right]\right) + A_2 |H(j\omega_2)| \sin\left(\omega_2 \left[t + \underbrace{\frac{\phi(\omega_2)}{\omega_2}}_{\text{Phase delay } \tau_{d2}}\right]\right)$$

Phase Distortion (2)

- Assuming that the difference between $|H(j\omega_1)|$ and $|H(j\omega_2)|$ is small, the "shape" of the time-domain output signal will be preserved as long as

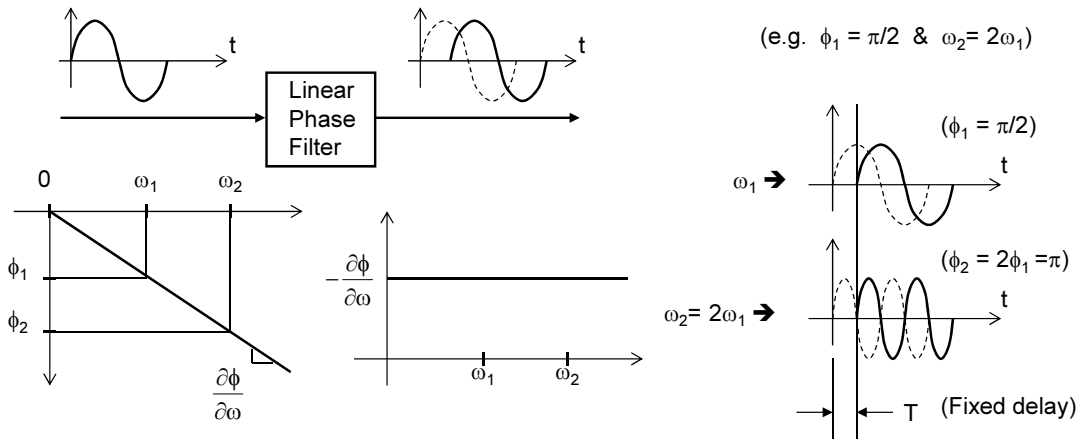
$$\frac{\phi(\omega_1)}{\omega_1} - \frac{\phi(\omega_2)}{\omega_2} = 0$$

- This condition is satisfied for

$$\phi(\omega) = T \cdot \omega \qquad T = \text{constant}$$

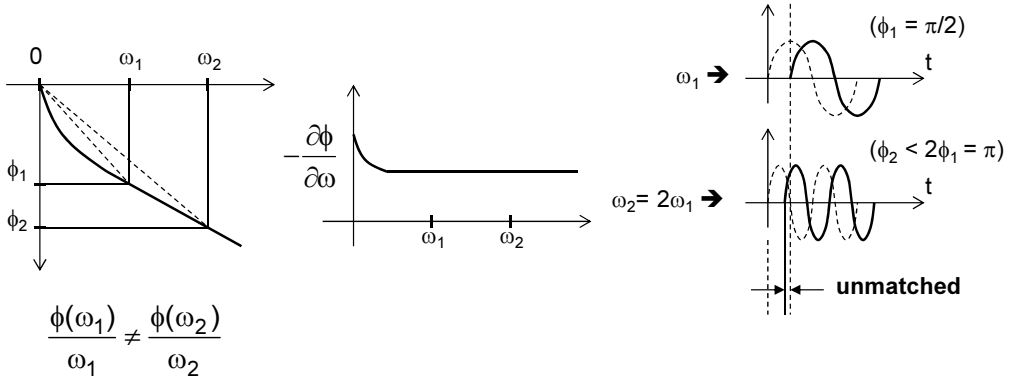
- A filter with this characteristic is called "linear phase"

Delay with Linear Phase



[U. Moon]

Delay with Nonlinear Phase



$$\frac{\phi(\omega_1)}{\omega_1} \neq \frac{\phi(\omega_2)}{\omega_2}$$

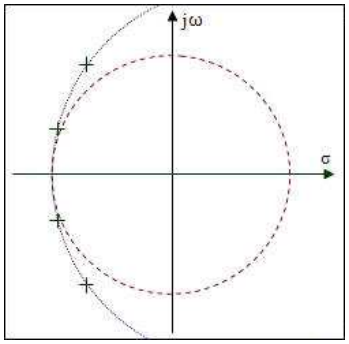
- Phase distortion occurs whenever the phase is nonlinear, i.e. the derivative of the phase is not constant
- The (negative) derivative of the phase is also called “group delay” or τ_g
- Note that for a linear phase filter, we have $\tau_g = \tau_d = \text{const.}$

Group Delay

- The name group delay (or envelope delay) comes from the fact that it specifies the delay experienced by a narrow-band “group‘” of sinusoidal components within some $\Delta\omega$ around a carrier w_c
- The width of $\Delta\omega$ is limited to a range over which $d\phi/d\omega$ is approximately constant
- For example, for an AM modulated signal, the carrier experiences a delay of τ_p (phase delay) and the envelope sees a delay of τ_g (group delay)
- For a proof, see e.g.
  - http://ccrma-www.stanford.edu/~jos/fp2/Derivation_Group_Delay_Modulation.html
- In this course, we are using the term group delay merely to refer $-d\phi/d\omega$ (and not to argue about group delay per se)

Bessel Filter Approximation

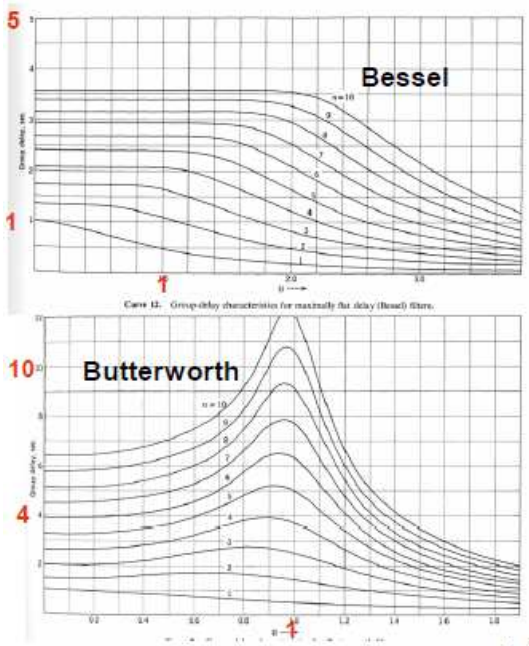
- All poles
- Poles are relatively low Q
- Maximally flat group delay
- Poor stopband attenuation

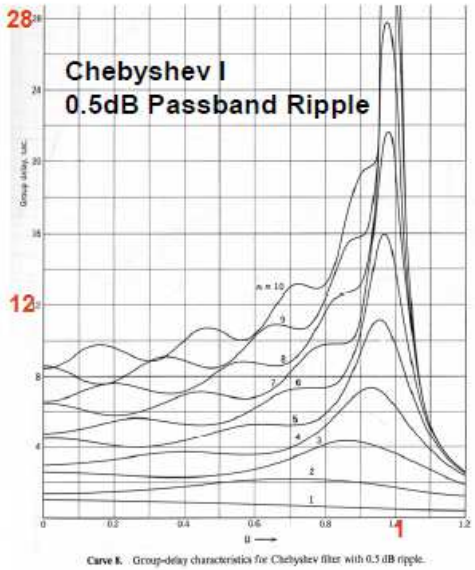


Order (N)	Re Part (-σ)	Im Part (±jω)
1	1.0000	
2	1.1030	0.6368
3	1.0509 1.3270	1.0025
4	1.3596 0.9877	0.4071 1.2476
5	1.3851 0.9606 1.5069	0.7201 1.4756

http://www.rfcafe.com/references/electrical/bessel-poles.htm

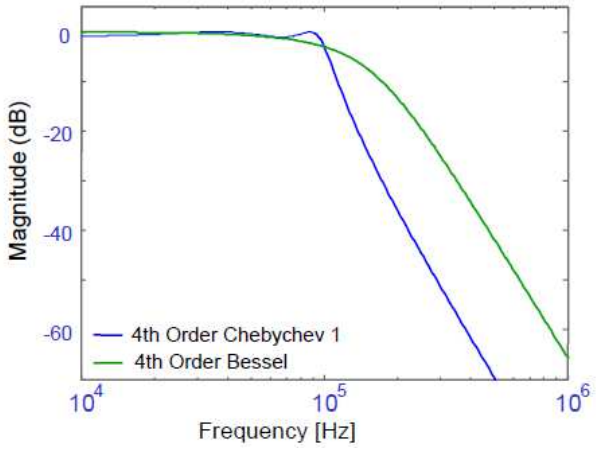
Group Delay Comparison





Ref: A. Zverev, *Handbook of filter synthesis*, Wiley, 1967.

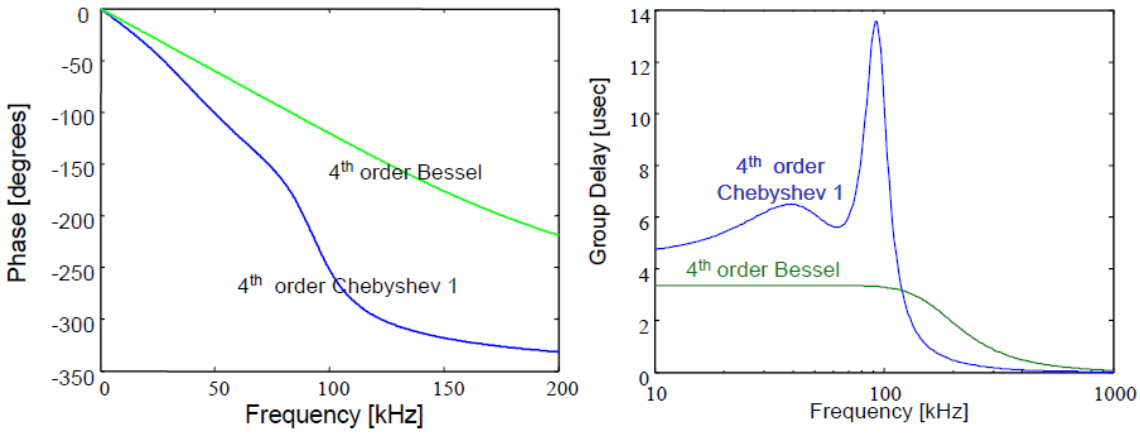
Comparison: Bessel vs. Chebyshev1



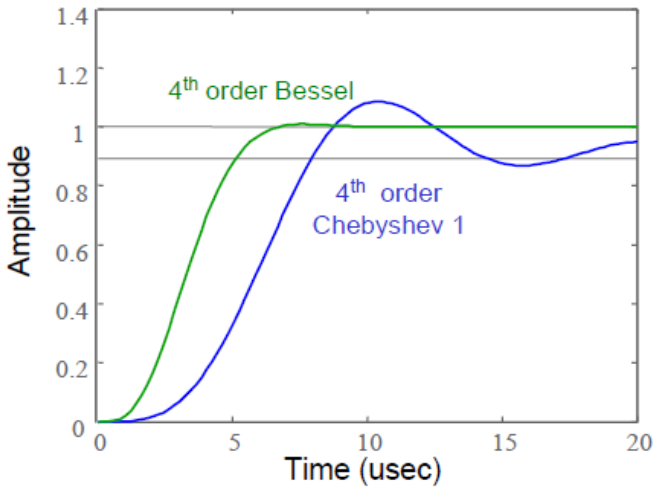
- Lowpass filters with 100 kHz passband
- Both filters are 4th order with the same -3 dB frequency
- Passband ripple of 1dB for Chebyshev I

[H. Khorramabadi]

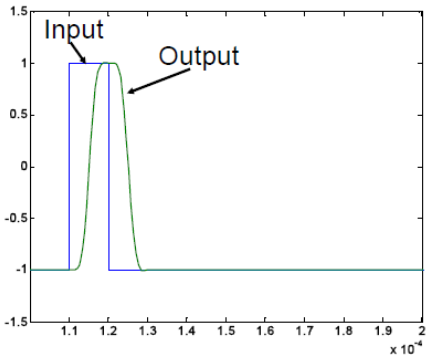
Phase and Group Delay



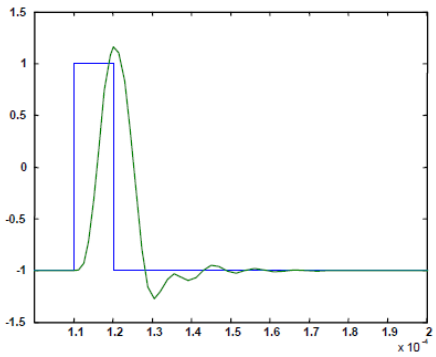
Step Response



Pulse Response



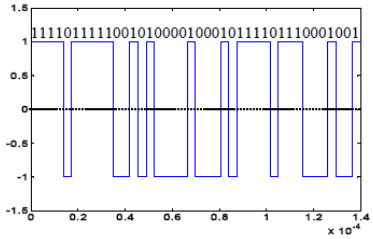
4th order Bessel

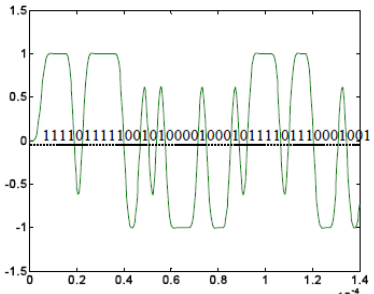


4th order Chebyshev I

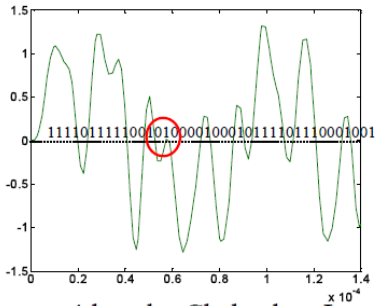
Intersymbol Interference

Input Signal:
Symbol rate 1/130kHz



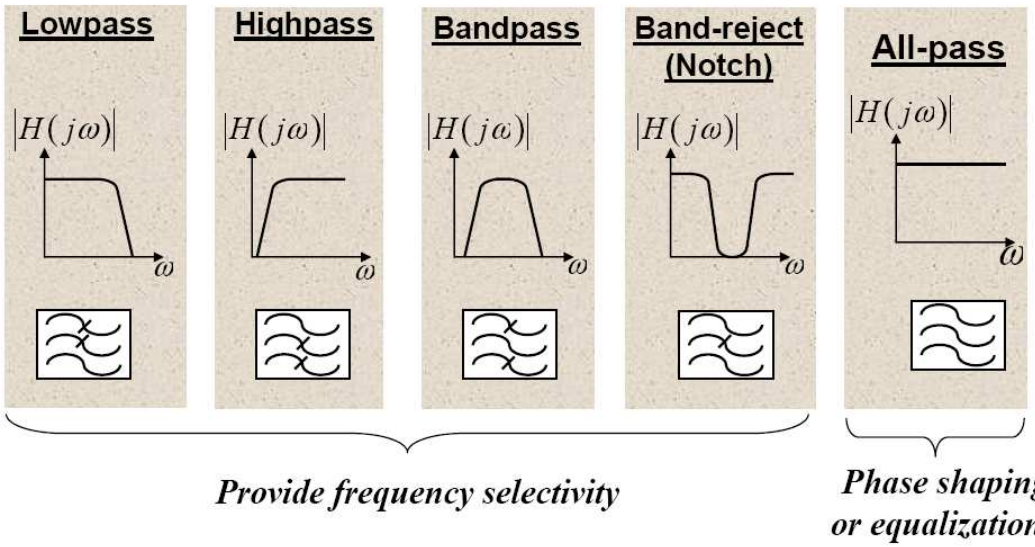


4th order Bessel



4th order Chebyshev I

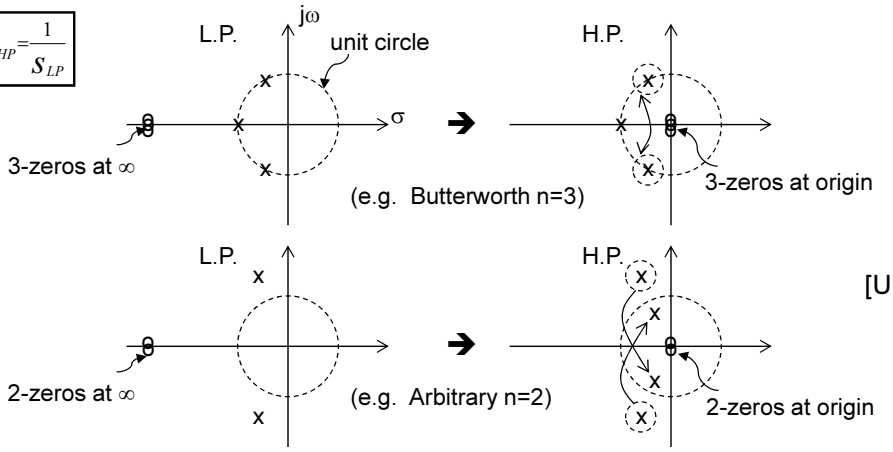
Beyond Lowpass Filtering



[H. Khorramabadi]

Lowpass to Highpass Transformation

$$s_{HP} = \frac{1}{s_{LP}}$$



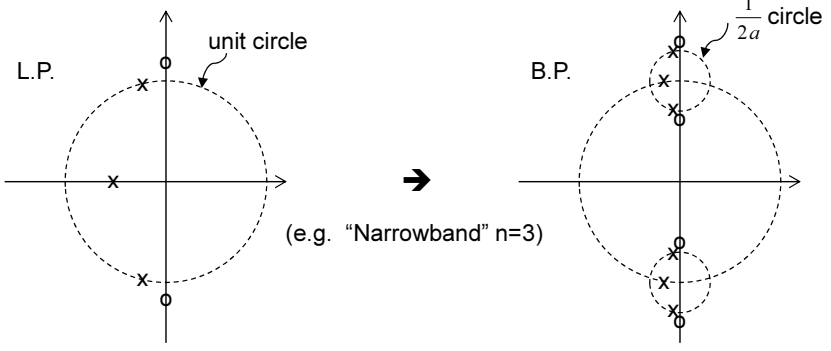
[U. Moon]

The s-domain poles and zeros simply become inverted. As shown by the examples, zeros at infinity move to the origin, and finite-valued poles become $|1/\text{pole}_{LP}|$ in magnitude and become conjugates (flips between quadrant II & III). The mapping boundary is the *unit circle*.

Lowpass to Bandpass Transformation

$$s_{BP} = \frac{s_{LP}}{2a} \pm j\sqrt{1-\left(\frac{s_{LP}}{2a}\right)^2} \approx \frac{s_{LP}}{2a} \pm j$$

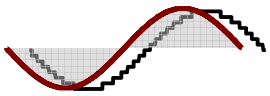
where $a = \frac{f_m}{\Delta f} = \text{“Q”}\ ;\ f_m = \sqrt{f_1 f_2}\ ;\ \Delta f = f_2 - f_1$



[U. Moon]

For a “narrowband” approximation, the s-domain poles and zeros simply become replicated at ±jω with a smaller unit circle of radius 1/2*a*. To realize a wideband filter, use a cascade of highpass and lowpass filters.

Biquad Filter Realization



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Stanford University
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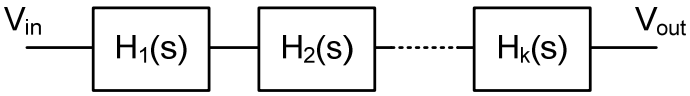
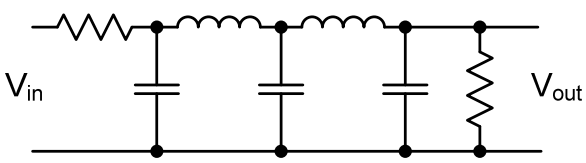
Architectural Options for High-Order Filters

- Cascades of (active) first and second-order sections

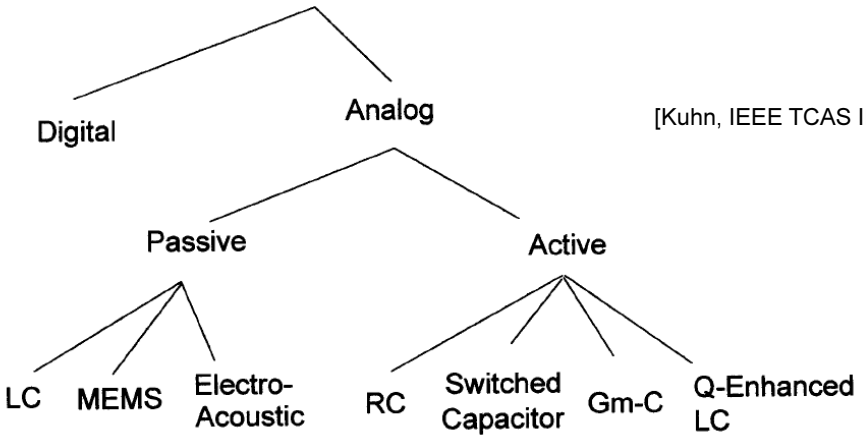


- Ladder filters (passive or emulated using active components)



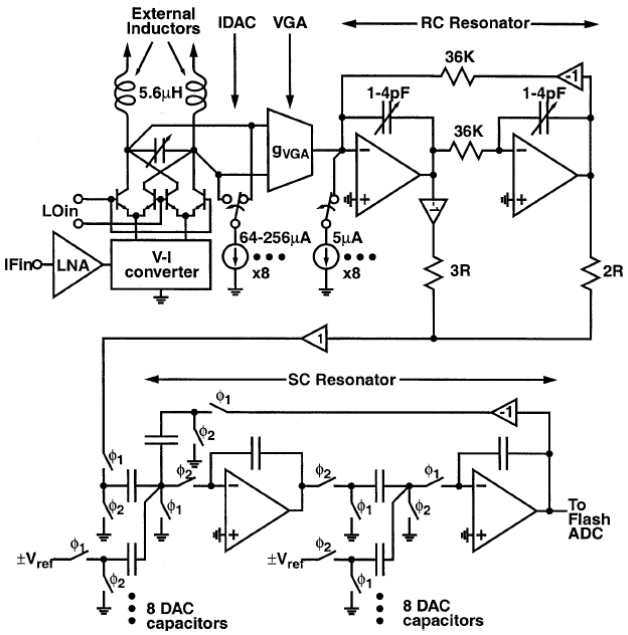
- Specialized architectures, typically emphasizing low complexity
  - Watch out for sensitivity issues (more later)

Building Block Options



[Kuhn, IEEE TCAS II, 10/2003]

Example



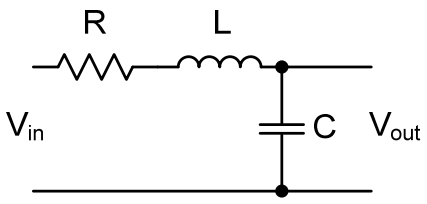
- An interesting filter that combines three different approaches
  - Passive LC
  - Active RC
  - Switched capacitor

[Schreier, JSSC 12/2002]

The Challenge

- Way too many options available
- Deciding on which implementation is “best” may only be possible once several options have been thoroughly compared
  - In terms of both first-order properties and second-order nonidealities, which aren’t always easy to understand
- The following discussion starts from the most basic ideas, and derives some of the most popular solutions used in practice
- For now, we will focus on the realization of second order sections, and cover ladder-based implementations in chapter 3
  - The treatment of second order sections will help us understand why we may ultimately want to go for a ladder implementation

Passive LC Lowpass Filter

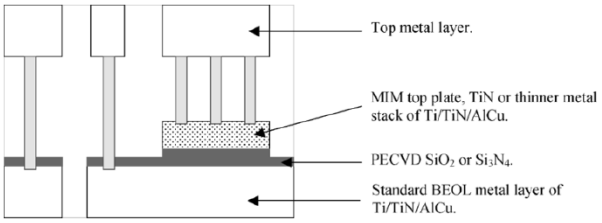


$$H(s) = \frac{\frac{1}{sC}}{\frac{1}{sC} + R + sL} = \frac{1}{1 + sRC + s^2LC} = \frac{1}{1 + \frac{s}{\omega_P Q_P} + \frac{s^2}{\omega_P^2}}$$

$$\omega_P = \frac{1}{\sqrt{LC}} \qquad Q_P = \frac{1}{R}\sqrt{\frac{L}{C}}$$

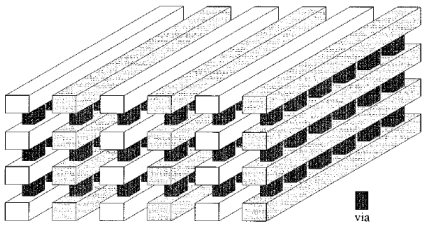
On-Chip Capacitors

Metal-Insulator-Metal (MIM)



[Ng, Trans. Electron Dev., 7/2005]

Vertical Parallel Plate (VPP)

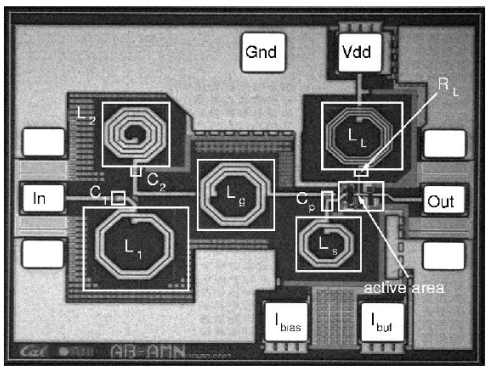


[Aparicio, JSSC 3/2002]

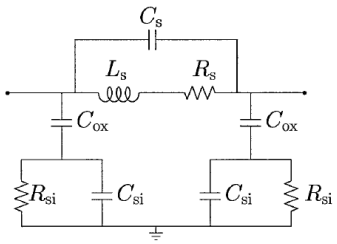
- Typically 1-2 fF/μm^2 (10-20 fF/μm^2 for advanced structures)
  - For 1 fF/μm^2, a 10 pF capacitor occupies ~100μm x 100μm
- Both MIM and VPP capacitors have good electrical properties
  - Mostly worry about parasitic caps
  - Series and parallel resistances are often not a concern

On-chip Inductors

~1mm



[Bevilacqua, ISSCC 2004]

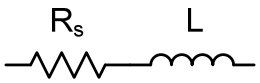


[Mohan, JSSC 10/1999]

- Many nonidealities, hard to model, low "Q"
- Area inefficient, typically achieve L < 10nH
- Sometimes bondwires are used as an alternative, L ~ 1nH/mm

Inductor Quality Factor

In general $$Y = \frac{1}{R + jX(\omega)} \quad \Rightarrow \quad Q = \frac{X(\omega)}{R}$$



$$Y = \frac{1}{R_s + j\omega L} \quad \Rightarrow \quad Q_L = \frac{\omega L}{R_s}$$

- On-chip inductors typically achieve Q_L < 5-10 at our frequencies of interest (EE315A)

LC Lowpass Example

- Assuming that we (very generously) use C=100pF, L=10nH

$$\omega_P = \frac{1}{\sqrt{LC}} = 2\pi \cdot 160MHz$$

- Integrated passive LC filters become practical for f > 200-500MHz
- For our LC lowpass, if we assume R=Rs (i.e. we only use the parasitic resistor of the inductor, no explicitly added resistance)

$$Q_L = \frac{\omega L}{R_s} \qquad Q_P = \frac{1}{R}\sqrt{\frac{L}{C}} = \frac{Q_L}{\omega L}\sqrt{\frac{L}{C}} = Q_L \frac{\omega_P}{\omega}$$

- This means that at $\omega=\omega_P$, the magnitude peaking that we can get is limited to the Q_L of the inductor (~5-10); not all that great

Summary

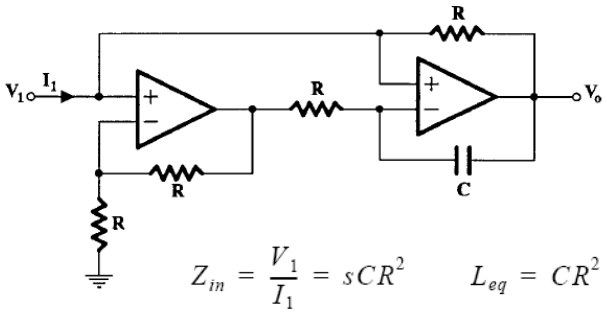
- On-chip capacitors are great, even though they're usually not as large as we would like them to be
- On-chip inductors tend to be avoided whenever possible, and are typically not useful in a filter with poles at frequencies below < 200-500 MHz
- The solution to this problem is to "simulate" the inductors using active components

Gyrators

- Gyrators are "active inductors"

T. L. Deliyannis, J. K. Fidler and Y. Sun, *Continuous-Time Active Filter Design*

http://www.engnetbase.com/ejournals/books/book_summary/summary.asp?id=475
(Section 3.5)

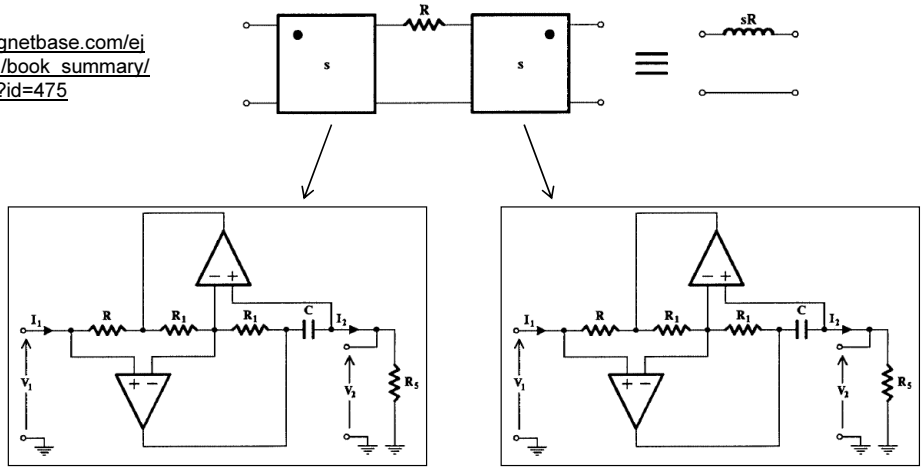


$$Z_{in} = \frac{V_1}{I_1} = sCR^2 \qquad L_{eq} = CR^2$$

- The above circuit is not all that useful for our lowpass filter; we need a "floating" inductor
  - Don't want the inductance to be ground referenced

Floating Gyrator

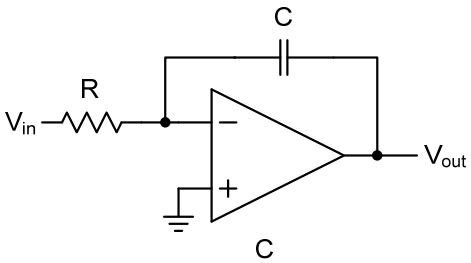
http://www.engnetbase.com/ejournals/books/book_summary/summary.asp?id=475
(Section 6.4)

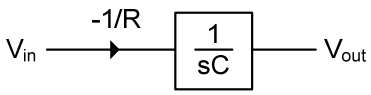


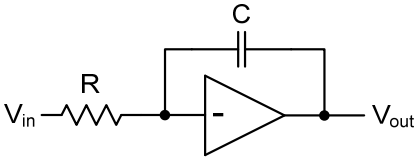
- Floating gyrators are pretty complex (and sensitive to parasitics)
  - There must be a better way to solve this problem…

Integrators

- A circuit that we can build without much sweat is an active integrator, e.g. using an op-amp
  - Many more options exist (more later)
- Assuming the availability of an ideal op-amp, we have



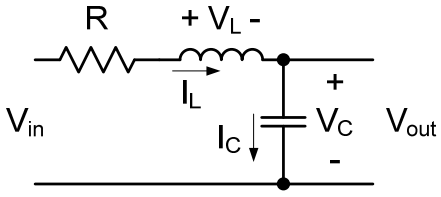




$$v_{out}(t) = -\frac{1}{C}\int \frac{v_{in}(t)}{R}\,dt$$

$$V_{out}(s) = -\frac{1}{sRC}V_{in}(s)$$

State-Space Realization



State variables
(integrator outputs)

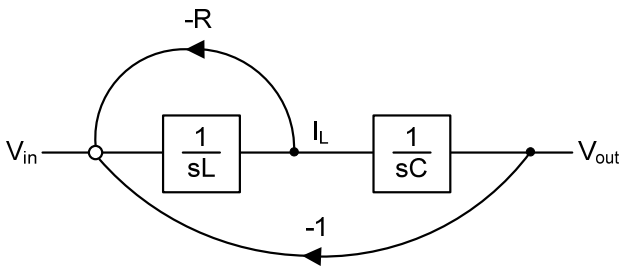
$$v_c(t) = \frac{1}{C}\int i_c(t)dt \qquad i_L(t) = \frac{1}{L}\int v_L(t)dt$$

$$V_c(s) = \frac{1}{sC} I_c(s) \qquad I_L(s) = \frac{1}{sL} V_L(s)$$

$$V_c = \frac{1}{sC} I_c = \frac{1}{sC} I_L = V_{out}$$

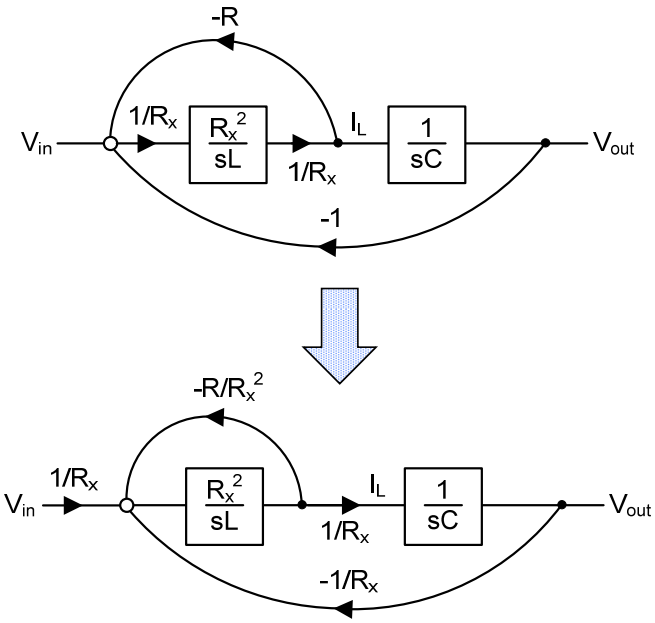
$$I_L = \frac{1}{sL} V_L = \frac{1}{sL}\left(V_{in} - I_L R - V_{out}\right)$$

Block Diagram

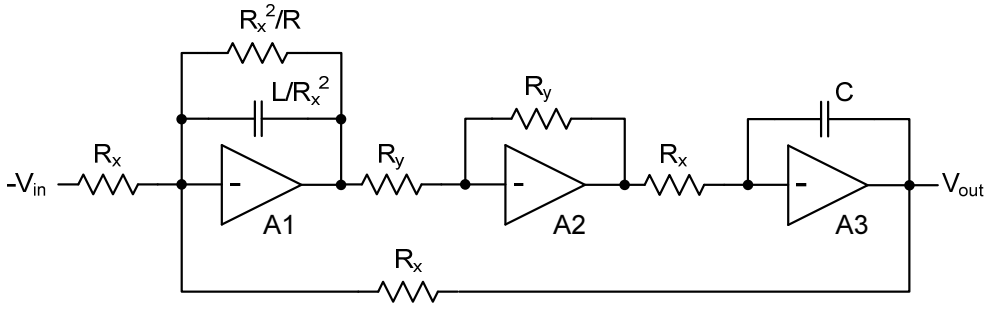


- Looks promising, but the problem with this realization is that the first integrator takes a voltage at the input and produces a current at the output
  - We need the opposite if we want to realize the circuit with an RC integrator

Modified (Equivalent) Block Diagrams



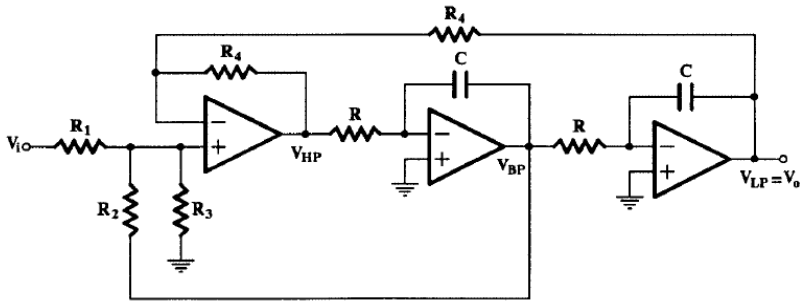
Implementation



$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{-1}{1 + sRC + s^2LC}$$

- One remaining issue is that the transfer function is inverted
  - We could fix that (if needed) using a fourth op-amp
  - Or by pushing A2 toward the input, and utilizing both its inverting and non-inverting input
    - The latter trick is used in the so-called KHN biquad

KHN Biquad



W.J. Kerwin, L.P. Huelsman, R.W Newcomb, "State-Variable Synthesis for Insensitive Integrated Circuit Transfer Functions," *IEEE JSSC,* vol.2, no.3, pp. 87-92, Sep. 1967.

http://www.engnetbase.com/ejournals/books/book_summary/summary.asp?id=475 (Section 4.9)

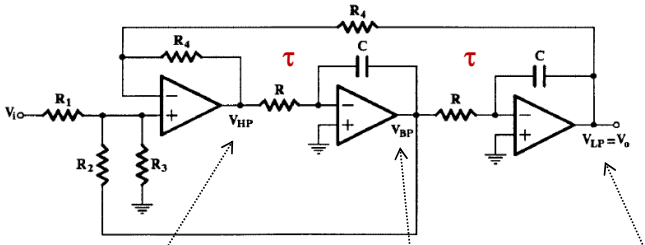
$$\frac{V_o}{V_i} = \frac{V_{LP}}{V_i} = \frac{K'}{1 + \frac{s}{\omega_o Q} + \frac{s^2}{\omega_o{}^2}}$$

$$\omega_o = \frac{1}{RC} \qquad Q = \frac{R_1R_2 + R_1R_3 + R_2R_3}{2R_1R_3}$$

$$K' = \frac{2R_2R_3}{R_1R_2 + R_1R_3 + R_2R_3} = \frac{R_2}{R_1} \cdot \frac{1}{Q}$$

Highpass and Bandpass Output

- An interesting feature of some biquads (including the HKN) is that they provide additional highpass and bandpass outputs for "free"

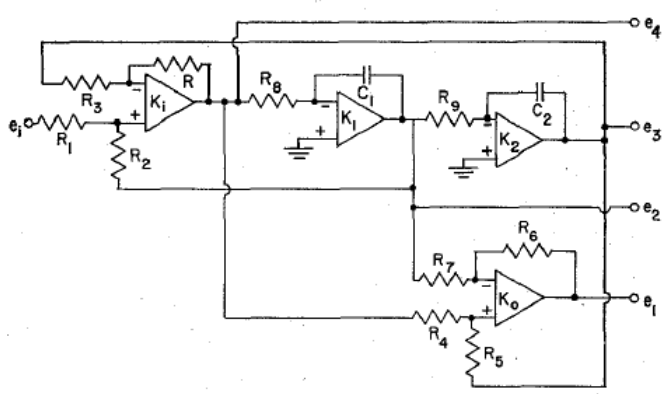


$$H_{HP}(s) = \frac{s^2\tau^2}{1 + \frac{s}{\omega_P Q_P} + \frac{s^2}{\omega_P^2}}$$

$$H_{BP}(s) = \frac{-s\tau}{1 + \frac{s}{\omega_P Q_P} + \frac{s^2}{\omega_P^2}}$$

$$H_{LP}(s) = \frac{1}{1 + \frac{s}{\omega_P Q_P} + \frac{s^2}{\omega_P^2}}$$

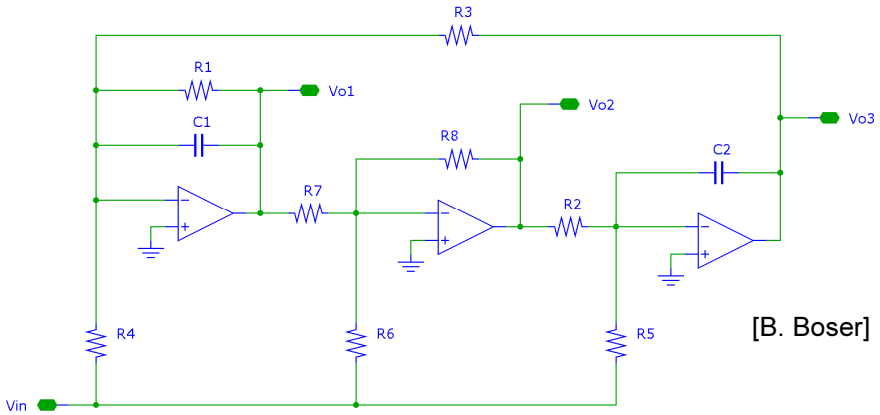
The General KHN Biquad



$$H_{GENERAL}(s) = \frac{b_2 s^2 + b_1 s + b_0}{1 + \frac{s}{\omega_P Q_P} + \frac{s^2}{\omega_P^2}}$$

Implements arbitrary poles and zeros

Tow-Thomas Biquad



[B. Boser]

P. E. Fleischer and J. Tow, "Design Formulas for biquad active filters using three operational amplifiers," Proc. IEEE, vol. 61, pp. 662-3, May 1973.

- General biquad using only three op-amps

Tow-Thomas Transfer Functions

$$\frac{V_{o1}}{V_{in}} = -k_2 \frac{(b_2 a_1 - b_1)s + (b_2 a_0 - b_0)}{s^2 + a_1 s + a_0}$$

$$\frac{V_{o2}}{V_{in}} = \frac{b_2 s^2 + b_1 s + b_0}{s^2 + a_1 s + a_0}$$

$$\frac{V_{o3}}{V_{in}} = -\frac{1}{k_1\sqrt{a_0}} \frac{(b_0 - b_2 a_0)s + (a_1 b_0 - a_0 b_1)}{s^2 + a_1 s + a_0}$$

- V_{o2}/V_{in} implements a general biquad section with arbitrary poles and zeros
- V_{o1}/V_{in} and V_{o3}/V_{in} realize the same poles but are limited to at most one finite zero

Tow-Thomas Design Equations

$$b_0 = \frac{R_8}{R_3 R_5 R_7 C_1 C_2}$$

$$b_1 = \frac{1}{R_1 C_1}\left(\frac{R_8}{R_6} - \frac{R_1 R_8}{R_4 R_7}\right)$$

$$b_2 = \frac{R_8}{R_6}$$

$$a_0 = \frac{R_8}{R_2 R_3 R_7 C_1 C_2}$$

$$a_1 = \frac{1}{R_1 C_1}$$

$$k_1 = \sqrt{\frac{R_2 R_8 C_2}{R_3 R_7 C_1}}$$

$$k_2 = \frac{R_7}{R_8}$$

For given a_i, b_i, k_i, C_1, C_2 and R_8 :

$$R_1 = \frac{1}{a_1 C_1}$$

$$R_2 = \frac{k_1}{\sqrt{a_0} C_2}$$

$$R_3 = \frac{1}{k_1 k_2}\frac{1}{\sqrt{a_0} C_1}$$

$$R_4 = \frac{1}{k_2}\frac{1}{a_1 b_2 - b_1}\frac{1}{C_1}$$

$$R_5 = \frac{k_1\sqrt{a_0}}{b_0 C_2}$$

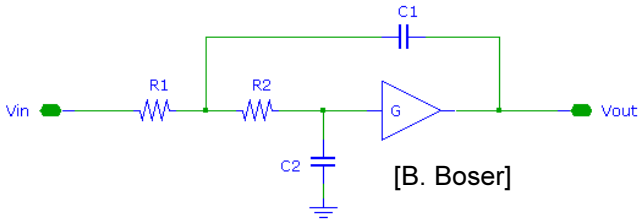
$$R_6 = \frac{R_8}{b_2}$$

$$R_7 = k_2 R_8$$

$$\omega_P = \sqrt{\frac{R_8}{R_2 R_3 R_7 C_1 C_2}}$$

$$Q_P = \omega_P R_1 C_1$$

Sallen-Key LPF



[B. Boser]

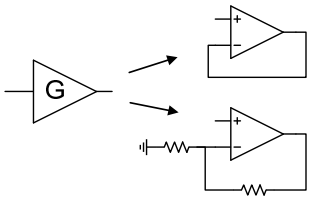
R.P. Sallen and E. L. Key "A Practical Method of Designing RC Active Filters." *IRE Trans. Circuit Theory,* Vol. CT-2, pp. 74-85, 1955

$$H(s) = \frac{G}{1 + \frac{s}{\omega_p Q_p} + \frac{s^2}{\omega_p{}^2}}$$

$$\omega_p = \frac{1}{\sqrt{R_1 C_1 R_2 C_2}}$$

$$Q_p = \frac{\omega_p}{\frac{1}{R_1 C_1} + \frac{1}{R_2 C_1} + \frac{1-G}{R_2 C_2}}$$

- Single gain element
  - typically $1 \leq G \leq 10$
- Poles only, no zeros
- Sensitive to parasitic capacitances
- Versions exist for HP, BP, …
  - http://en.wikipedia.org/wiki/Sallen_Key_filter



Tow-Thomas or Sallen-Key?

- Suppose we now wanted to realize a biquad that has poles only
- Should we use a Tow-Thomas or Sallen-Key realization?
- Clearly, from the perspective of complexity, we would probably want to go for Sallen-Key
- Unfortunately, the Sallen-Key realization comes with disadvantages in terms of sensitivity to component variations
- Let's take a closer look…

Sensitivity

- The sensitivity of any variable y to any parameter x is defined as (See e.g. Gray & Meyer, Section 4.2)

$$S_x^y = \lim_{\Delta x \to 0}\left(\frac{\Delta y / y}{\Delta x / x}\right) = \frac{x}{y}\lim_{\Delta x \to 0}\frac{\Delta y}{\Delta x} = \frac{x}{y}\frac{\partial y}{\partial x}$$

- In order to relate fractional changes in y to fractional changes in x we can then write

$$\frac{\Delta y}{y} \cong S_x^y \frac{\Delta x}{x}$$

- Example

$$S_x^y = 10 \qquad \frac{\Delta x}{x} = 2\% \qquad \Rightarrow \frac{\Delta y}{y} \cong 20\%$$

- Common sense: sensitivity is a first order approximation, accurate only for “small” errors

Parameter Variations (1)

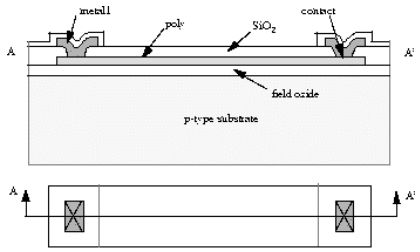
- Discrete resistors and capacitors

- Come in many different shapes and sizes and accuracies
  - E.g. metal film resistors, ~0.1% accurate, 5ppm/°C
  - E.g. C0G dielectric capacitors, 2% accurate, very small temperature dependence

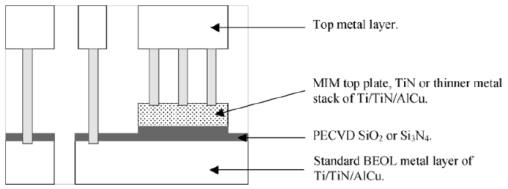
Parameter Variations (2)

- Integrated resistors and capacitors

Poly resistor



MIM Capacitor



- Important to distinguish between
  - Global process variations → On the order of +/- 20% !
  - Device-to-device mismatch → On the order of 1% or less

Sensitivity to Global Variations

Tow-Thomas

$$\omega_P = \sqrt{\frac{R_8}{R_2 R_3 R_7 C_1 C_2}} \propto \frac{1}{RC}$$

$$Q_P = \omega_P R_1 C_1 \propto 1$$

Sallen-Key

$$\omega_P = \frac{1}{\sqrt{R_1 C_1 R_2 C_2}} \propto \frac{1}{RC}$$

$$Q_P = \frac{\omega_P}{\frac{1}{R_1 C_1} + \frac{1}{R_2 C_1} + \frac{1-G}{R_2 C_2}} \propto 1$$

- Q_P is independent of global variations in both realizations
  - Assuming all R and C use the same device structure, respectively
- ω_P varies with the RC product of the components

Sensitivity to Mismatch (Sallen-Key)

$$\omega_P = \frac{1}{\sqrt{R_1 C_1 R_2 C_2}}$$

$$Q_P = \frac{\omega_P}{\frac{1}{R_1 C_1} + \frac{1}{R_2 C_1} + \frac{1-G}{R_2 C_2}}$$

$$S_{R_1}^{\omega_P} = S_{R_2}^{\omega_P} = S_{C_1}^{\omega_P} = S_{C_2}^{\omega_P} = -\frac{1}{2}$$

$$S_{R_1}^{Q_P} = -S_{R_2}^{Q_P} = -\frac{1}{2} + Q_P \sqrt{\frac{R_2 C_2}{R_1 C_1}}$$

$$S_{C_1}^{Q_P} = -S_{C_2}^{Q_P} = -\frac{1}{2} + Q_P \left(\sqrt{\frac{R_1 C_2}{R_2 C_1}} + \sqrt{\frac{R_2 C_2}{R_1 C_1}} \right)$$

$$S_G^{Q_P} = Q_P G \sqrt{\frac{R_1 C_1}{R_2 C_2}}$$

- Sensitivity depends on Q_P and "component spread" i.e. the ratios of the resistors and capacitors, respectively

Example (1)

- Want to design a Sallen-Key filter with Q_P=10
- Choice 1: All R and C are the same $\Rightarrow$ G = 3 -(1/Q_P) = 2.9
  - Very nice from the perspective of component spread, but bad for sensitivity, e.g.

$$S_{R_1}^{Q_P} = -S_{R_2}^{Q_P} = -\frac{1}{2} + Q_P = 9.5$$

- Choice 2: Reduce sensitivity by accepting large component spread
  - Can show that G=1 is a good choice
    - See e.g. http://www.maxim-ic.com/appnotes.cfm/an_pk/738
      - Note: The expression for S^Q_K is incorrect this application note (R_3 and R_1 should be interchanged in this expression to match the result from slide 36)

Example (2)

- For G=1, we have

$$Q_P = \frac{\omega_P}{\frac{1}{R_1 C_1} + \frac{1}{R_2 C_1}}$$

and it follows that

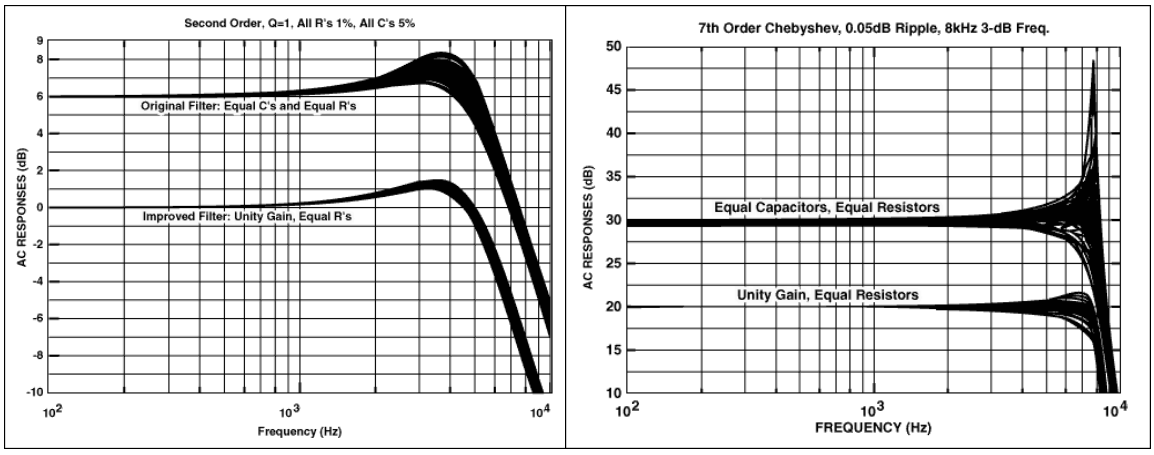
$$S_{R_1}^{Q_P} = -S_{R_2}^{Q_P} = -\frac{1}{2} + \frac{R_2}{R_1 + R_2} = 0 \quad for \quad R_1 = R_2$$

- Unfortunately, in this case

$$\frac{C_1}{C_2} = 4Q_P^2 = 400 \quad for \quad Q_P = 10$$

- Bottom line: The Sallen-Key realization suffers from a strong tradeoff between sensitivity and component spread

Case Studies



MAXIM APPLICATION NOTE 738
Minimizing Component-Variation Sensitivity in Single Op Amp Filters
http://www.maxim-ic.com/appnotes.cfm/an_pk/738/

Sensitivity to Mismatch (Tow-Thomas)

$$\omega_P = \sqrt{\frac{R_8}{R_2 R_3 R_7 C_1 C_2}}$$

$$Q_P = \omega_P R_1 C_1 = R_1 \sqrt{\frac{R_8 C_1}{R_2 R_3 R_7 C_2}}$$

$$S_{R2}^{\omega_P} = S_{R3}^{\omega_P} = S_{R3}^{\omega_P} = -S_{R8}^{\omega_P} = S_{C1}^{\omega_P} = S_{C2}^{\omega_P} = -\frac{1}{2}$$

$$S_{R_1}^{Q_P} = 1$$

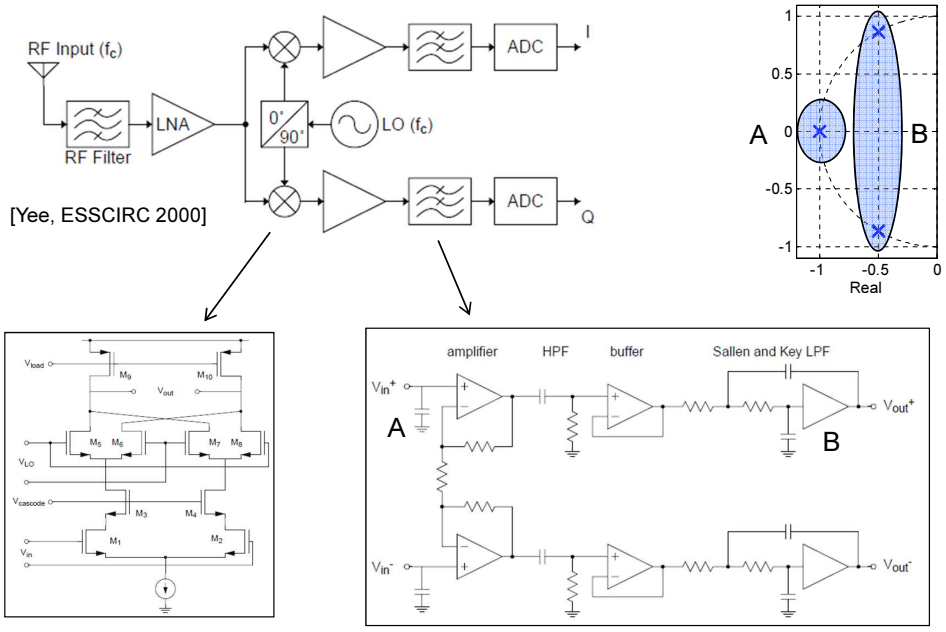
$$S_{R_2}^{Q_P} = S_{R_3}^{Q_P} = S_{R_7}^{Q_P} = -S_{R_8}^{Q_P} = -S_{C_1}^{Q_P} = S_{C_2}^{Q_P} = -\frac{1}{2}$$

- Constant sensitivities, independent of Q and component spread
  - Much nicer!

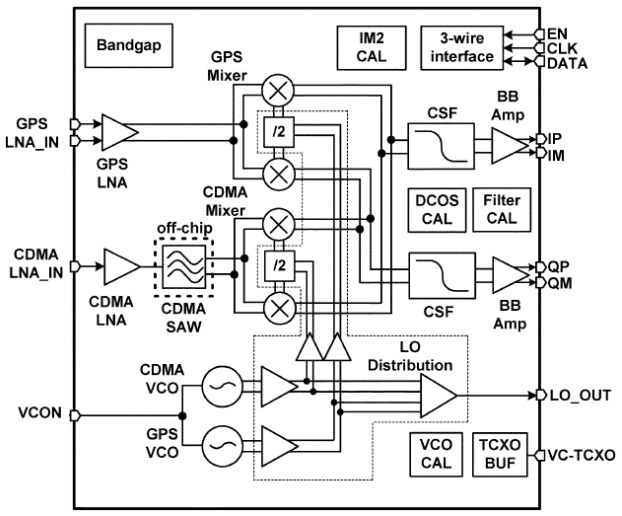
Conclusions

- Biquads can be realized in numerous different ways
- Implementation and component sizing have a big impact on sensitivity to variations
  - Of course, we must avoid high-sensitivity circuits in practice
- No theory for finding a low-sensitivity architecture
  - Use proven circuits & check!
- Tow-Thomas biquad
  - Arbitrary poles and zeros, three amplifiers
  - Well-behaved sensitivities
- Sallen-Key biquad
  - Only poles, one amplifier
  - Sensitivities trade off with component spread
    - Typically use G=1 and use this circuit only for “low Q” poles

Example1: WCDMA Receiver



Example 2: CDMA/GPS Receiver



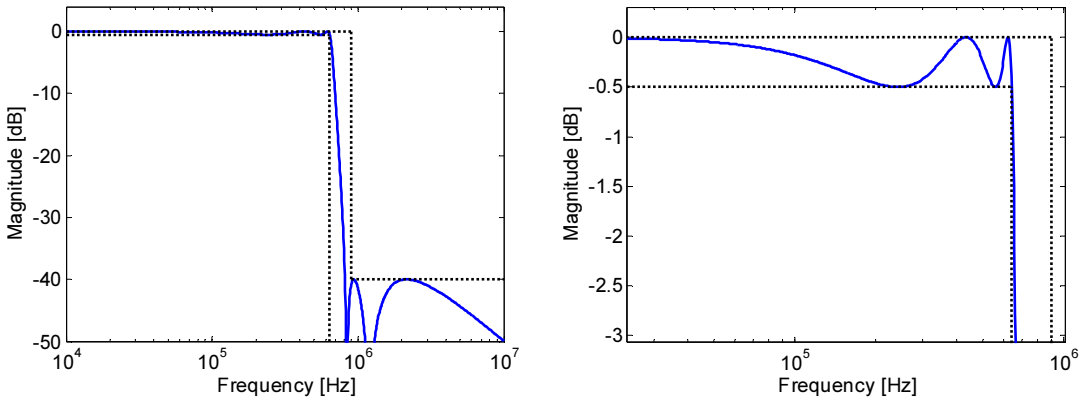
Lim et al., "A Fully Integrated Direct-Conversion Receiver for CDMA and GPS Applications," IEEE JSSC, Nov. 2006

- Channel select filters (CSF)
  - 640 kHz passband, lowpass
  - 0.5 dB passband ripple
  - > 40 dB stopband attenuation at 900 kHz
- 5th order elliptical filter
- Phase distortion can be tolerated in this application

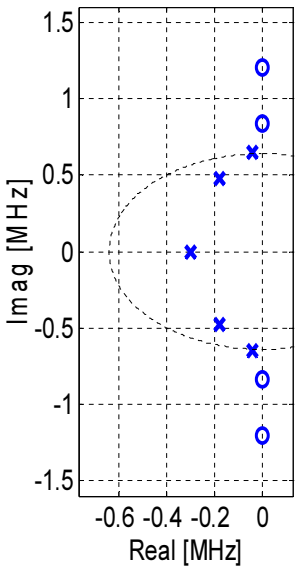
Matlab Synthesis Result

$$\frac{204155.1855\ (s^2 + 2.786e013)\ (s^2 + 5.715e013)}{(s+1.89e006)\ (s^2 + 2.217e006s + 1.034e013)\ (s^2 + 5.315e005s + 1.664e013)}$$

$$= \frac{(s^2/2.786e013 + 1)\ (s^2/5.715e013 + 1)}{(s/1.89e006 + 1)\ (s^2/1.034e013 + s/4.6640e+006 + 1)\ (s^2/1.664e013 + s/3.1308e+007 + 1)}$$



Pole and Zero Locations



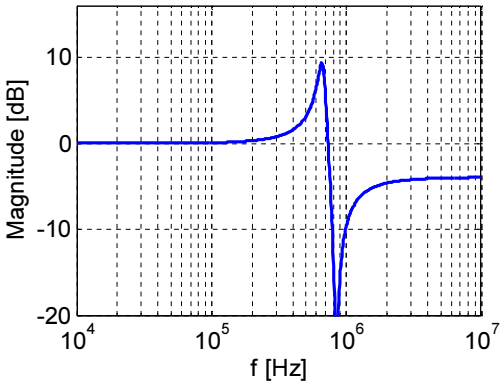
		ω_P	Q_P
$p_{1,2}$	-42.30 ± j6.4783 kHz	649.21 kHz	7.6748
$p_{3,4}$	-176.45 ± j4.8030 kHz	511.68 kHz	1.4499
p_5	-300.80 kHz		

$z_{1,2}$	± j1203.2 kHz
$z_{3,4}$	± j840.1 kHz

Pairing Options for $p_{1,2}$ (High-Q)

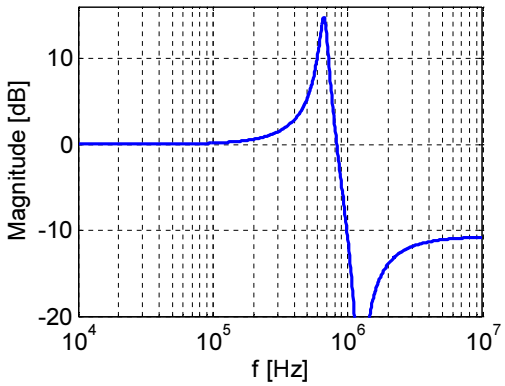
- Pairing with nearby zero

```
          (s^2/2.786e013 + 1)
-----------------------------------
(s^2/1.664e013 + s/3.1308e+007 + 1)
```



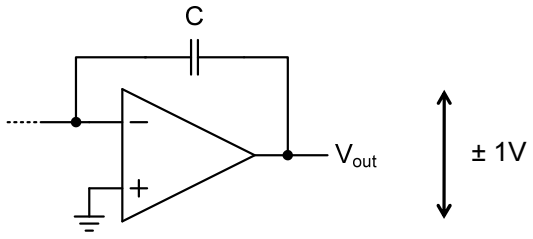
- Pairing with remote zero

```
          (s^2/5.715e013 + 1)
-----------------------------------
(s^2/1.664e013 + s/3.1308e+007 + 1)
```

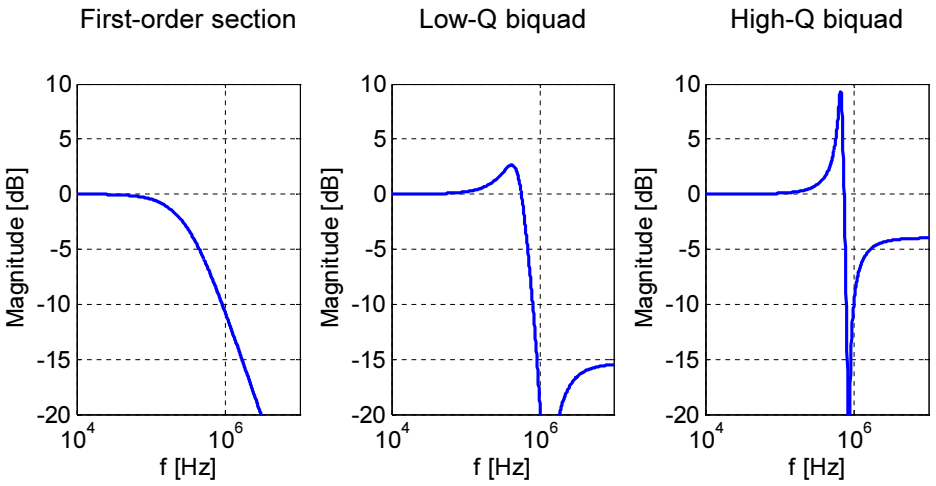


Pole-Zero Pairing

- Pairing high-Q poles with nearby zeros is desirable from a dynamic range perspective
  - Say that the amplifier at the output of the biquad can handle a maximum signal of 1 V_{peak}
  - If the biquad response peaks 20 dB above unity, this means that we can only process inputs with 100 mV amplitude near the frequency of the peak (which lies in the passband)
  - The signal is therefore reduced relative to the thermal noise of the circuit, which is highly undesirable

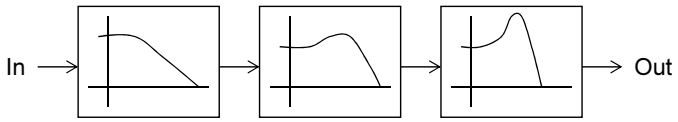


Response of the Individual Sections

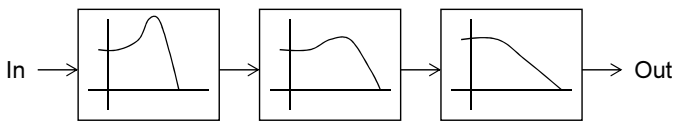


- In which order should we cascade these sections?

Biquad Ordering



Ordering the Biquads from low-Q to high-Q generally yields "smooth" transfer functions from the input to the intermediate nodes, and often helps minimize harmonic distortion, but the output will have significant noise peaking near the corner frequency due to the last stage with high-Q.



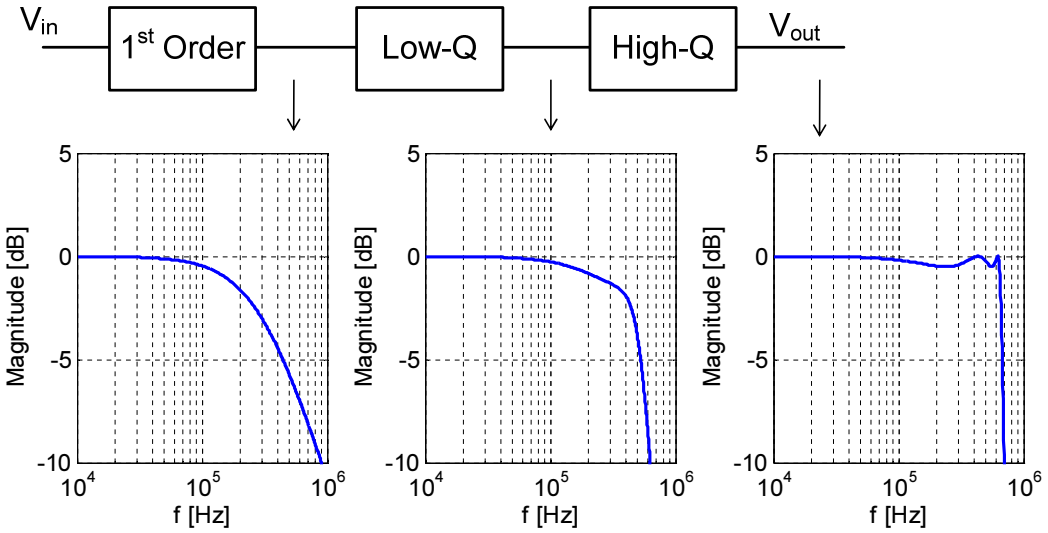
Reversing the ordering will allow the later stages to filter out the noise peaking near corner frequency. May also filter out harmonics (but not intermodulation).

In practical filter design, it would be worthwhile giving some thoughts to the options that you may have for the ordering of the biquads. In a non-lowpass filter application, inherent ac-coupling may also be used to your advantage to suppress offset accumulation.

(Some good system-level discussions in Schaumann/Ghausi/Laker.)

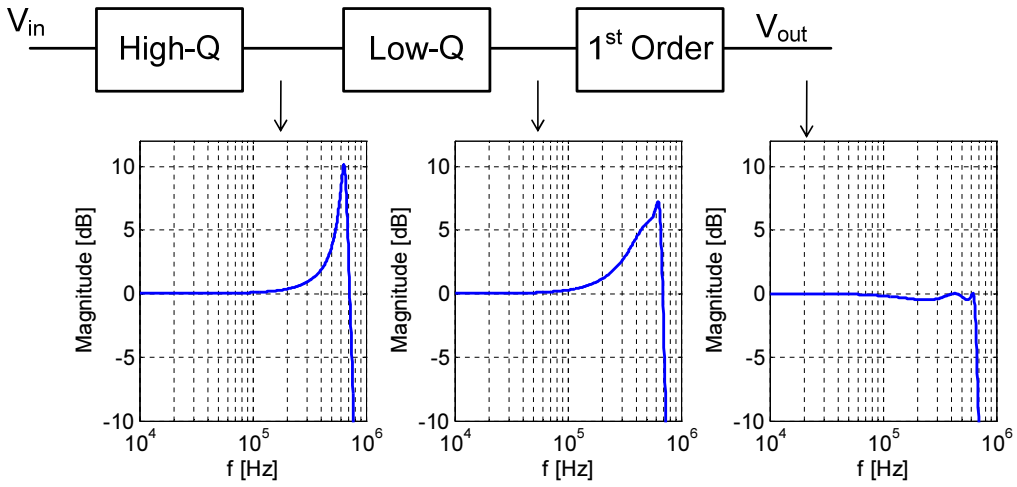
[U. Moon]

Intermediate Outputs for Low-Q → High-Q



- This ordering is most frequently used in practice

Intermediate Outputs for High-Q → Low-Q



- At first glance this looks bad, but the noise from the high-Q biquad is filtered before it reaches the output
  - We will revisit this situation in the context of noise analysis

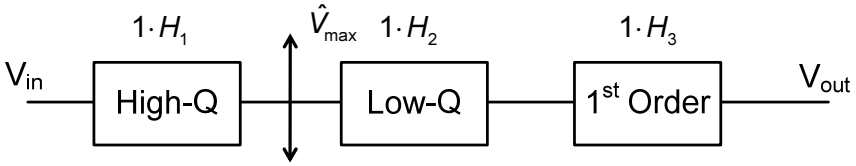
Dynamic Range Scaling

- Suppose we decided that the second ordering is what we want to use for our design
- In this case, we need to think about a proper gain distribution that avoids “clipping” in the individual amplifiers
- For this purpose, we introduce gain scale factors for each section, while keeping the overall gain constant ($K_1K_2K_3 = 1$ in this example)

```
        (s^2/2.786e013 + 1)                (s^2/5.715e013 + 1)                1
-----------------------------------  -----------------------------------  ----------------
(s^2/1.664e013 + s/3.1308e+007 + 1)  (s^2/1.034e013 + s/4.6640e+006 + 1)  (s/1.89e006 + 1)
```

```
      K1*(s^2/2.786e013 + 1)             K2*(s^2/5.715e013 + 1)             K3
-----------------------------------  -----------------------------------  ----------------
(s^2/1.664e013 + s/3.1308e+007 + 1)  (s^2/1.034e013 + s/4.6640e+006 + 1)  (s/1.89e006 + 1)
```


Analysis (1)



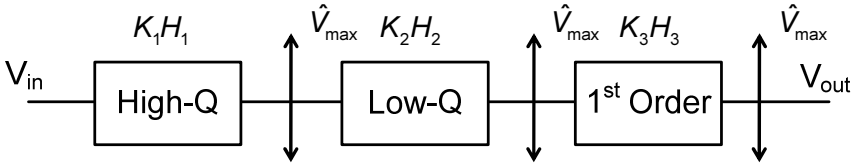
- Suppose we chose $K_1=K_2=K_3=1$ and assume that we will apply single sine waves with arbitrary frequencies to the input
- Since H_1 has significant peaking ($|H1|_{max} \cong 3.19 \cong 10$ dB), we can guarantee proper operation only for input amplitudes up to

$$\frac{\hat{V}_{max}}{|H_1|_{max}} \quad \text{e.g.} \quad \frac{1V}{3.19} = 314mV$$

- Since the overall gain is unity (with no peaking above 1), this means V_{out} swings only 314mV, meaning that we are “wasting” available signal range

Analysis (2)

- A more desirable outcome may be to scale K_1, K_2, K_3 such that all stages utilize the maximum available swing as the input tone is swept across all frequencies
  - Note that in general, the maximum output swings for each stage may not occur at the same frequency



Analysis (3)

- This is achieved for

$$K_1|H_1|_{max} = K_1K_2K_3|H_1H_2H_3|_{max}$$
$$K_1K_2|H_1H_2|_{max} = K_1K_2K_3|H_1H_2H_3|_{max}$$

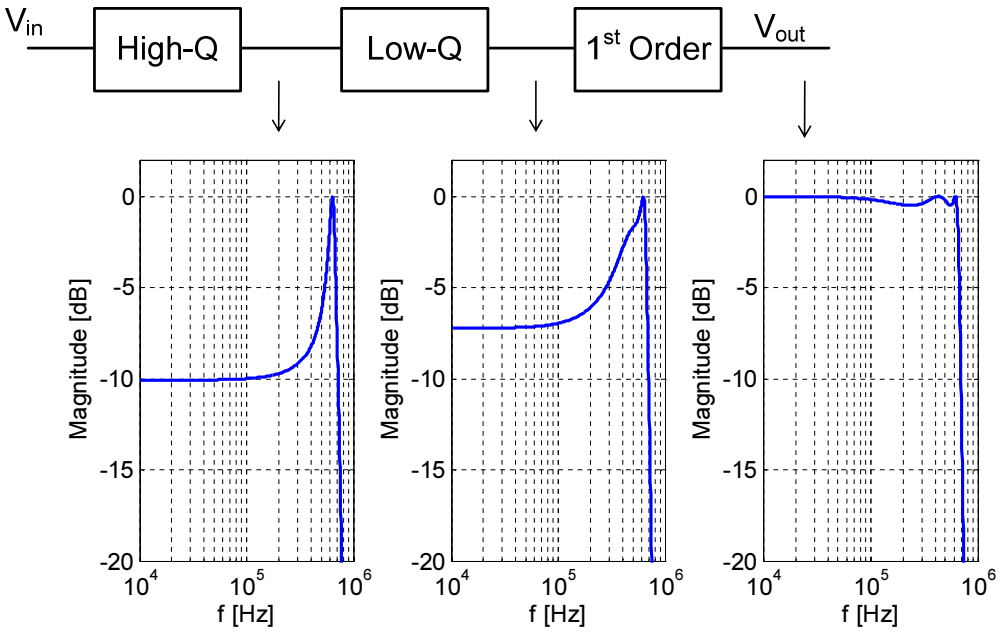
- In our example

$$K_1K_2K_3 = 1 \qquad |H_1|_{max} = 3.19 \qquad |H_1H_2|_{max} = 2.3 \qquad |H_1H_2H_3|_{max} = 1$$

and therefore

$$K_1 = \frac{1}{|H_1|_{max}} = \frac{1}{3.19} \qquad K_2 = \frac{1}{K_1|H_1H_2|_{max}} = \frac{3.19}{2.3} \qquad K_3 = \frac{1}{K_1K_2} = \frac{3.19 \cdot 2.3}{3.19}$$

Intermediate Outputs After DR Scaling



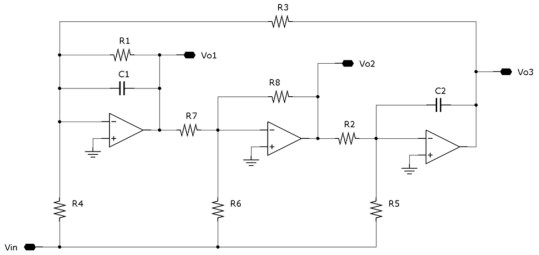
Arguments Against "Sinusoidal" DR Scaling

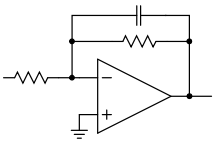
- If the input signal is wide-band (as in many telecommunication systems), the node with peaking may not saturate due to limited signal power in that frequency region
  - May want to optimize the gain distribution based on a power spectral density "template" of the incoming signal
- Aligning the peaks for each output perfectly will require non-integer component ratios
  - But we may want to use integer ratios to improve matching
- For a discussion on why sinusoidal dynamic range scaling may not always the best choice, see Behbahani, JSSC 4/2000

Expressions for Implementation

```
    0.3133*(s^2/2.786e013 + 1)          1.3865*(s^2/5.715e013 + 1)          2.3021
-----------------------------------  -----------------------------------  ---------------
(s^2/1.664e013 + s/3.1308e+007 + 1)  (s^2/1.034e013 + s/4.6640e+006 + 1)  (s/1.89e006 + 1)
```

2x Tow-Thomas





$$\frac{V_{o2}}{V_{in}} = \frac{b_2 s^2 + b_1 s + b_0}{s^2 + a_1 s + a_0} \qquad b_1 = 0$$

Tow-Thomas Component Values (b_1=0)

$$R_1 = \frac{1}{a_1 C_1} \qquad R_2 = \frac{k_1}{\sqrt{a_0} C_2} \qquad R_3 = \frac{1}{k_1 k_2} \frac{1}{\sqrt{a_0} C_1}$$

$$R_4 = \frac{1}{k_2} \frac{1}{a_1 b_2} \frac{1}{C_1} \qquad R_5 = \frac{k_1 \sqrt{a_0}}{b_0 C_2} \qquad R_6 = \frac{R_8}{b_2} \qquad R_7 = k_2 R_8$$

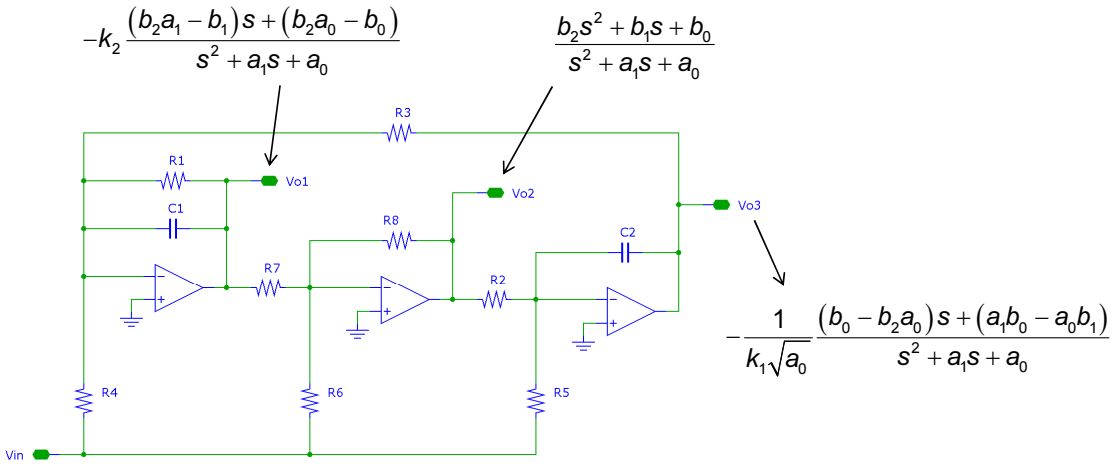
$$\omega_Z = \sqrt{\frac{R_6}{R_3 R_5 R_7 C_1 C_2}} \qquad \omega_P = \sqrt{\frac{R_8}{R_2 R_3 R_7 C_1 C_2}} \qquad Q_P = \omega_P R_1 C_1$$

- a_0, a_1, b_0, b_1, b_2 are known; can pick k_1, k_2, C_1, C_2 and R8
- Reasonable starting values
  - $k_1 = k_2 = 1$
  - Set $C_1 = C_2$ to a reasonable value that is easily implemented, e.g. 1pF
  - Set R_8 to a reasonable value that is easily implemented and represents an integer multiple or fraction of R_2, R_3 or R_7

Example Design Flow

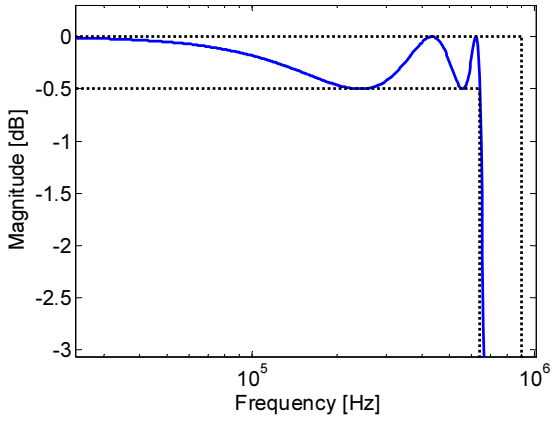
- First cut component calculation using reasonable starting values for k_1, k_2, C_1, C_2 and R_8
- Dynamic range scaling of internal amplifier outputs by adjusting k_1 and k_2
- Thermal noise scaling using ideal amplifiers
  - Increase all capacitors and reduce all resistors until noise specification is met
- Design amplifiers
- Repeat thermal noise scaling to accommodate amplifier noise
- Analyze sensitivity to component variations and devise tuning mechanism (if needed)

Dynamic Range Scaling of Internal Nodes



- Scale k_1 and k_2 such that peak magnitude at V_{o1} and V_{o2} corresponds to maximum available amplifier swing

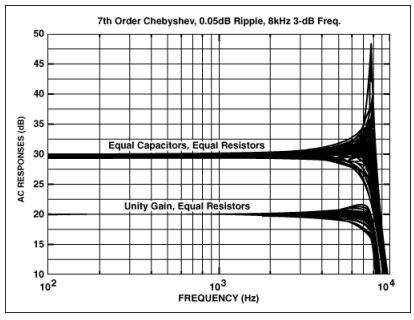
Sensitivity Analysis



- Ideally, we would like to have an analytical expression that relates “interesting points” of the response to variations in all components
  - E.g. calculate variations in the passband ripple as a function of the percent error in R_2
- This is almost impossible or at least impractical to do in practice

Sensitivity Analysis – Monte Carlo

- Monte Carlo Analysis
  - Have a statistical model for all components
  - Run a large number of simulations (Matlab or Spectre) to capture many statistical outcomes and create overlay plot from all runs



MAXIM APPLICATION NOTE 738: Minimizing Component-Variation Sensitivity in Single Op Amp Filters
http://www.maxim-ic.com/appnotes.cfm/an_pk/738/

- Such an analysis is very useful for validation, but perhaps too much work for intuition building and/or design guidance

Basic Sensitivity Analysis

- Say we just want to get a basic feel for the sensitivities
- Look at impact of
  - Global process variations
  - Component mismatch
- For global process variations, we have already seen that

$$\omega_Z = \sqrt{\frac{R_6}{R_3 R_5 R_7 C_1 C_2}} \propto \frac{1}{RC} \qquad \omega_P = \sqrt{\frac{R_8}{R_2 R_3 R_7 C_1 C_2}} \propto \frac{1}{RC} \qquad Q_P = \omega_P R_1 C_1 \propto 1$$

- If all R and C vary by the same percentage, the filter "shape" is preserved and shifted back and forth along the frequency axis
- If this is a problem for the application, we can "tune" either R or C to bring the filter response back to the desired location

Mismatch Analysis

$$\omega_Z = \sqrt{\frac{R_6}{R_3 R_5 R_7 C_1 C_2}} \qquad \omega_P = \sqrt{\frac{R_8}{R_2 R_3 R_7 C_1 C_2}} \qquad Q_P = \omega_P R_1 C_1$$

- Suppose we had resistors and capacitors that deviate from their nominal component value (which is subject to global variations) by a standard deviation of 1%
- Since

$$S_{R2}^{\omega_P} = S_{R3}^{\omega_P} = S_{R3}^{\omega_P} = -S_{R8}^{\omega_P} = S_{C1}^{\omega_P} = S_{C2}^{\omega_P} = -\frac{1}{2}$$

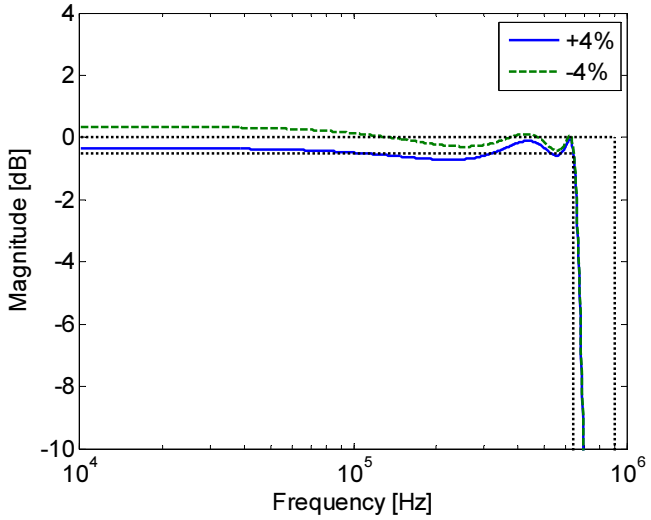
  this means

$$\sigma_{\Delta\omega_P/\omega_P} = \frac{1}{2}\sqrt{6} \cdot 1\% = 1.22\%$$

$$3\sigma_{\Delta\omega_P/\omega_P} = 3.67\% \cong 4\%$$

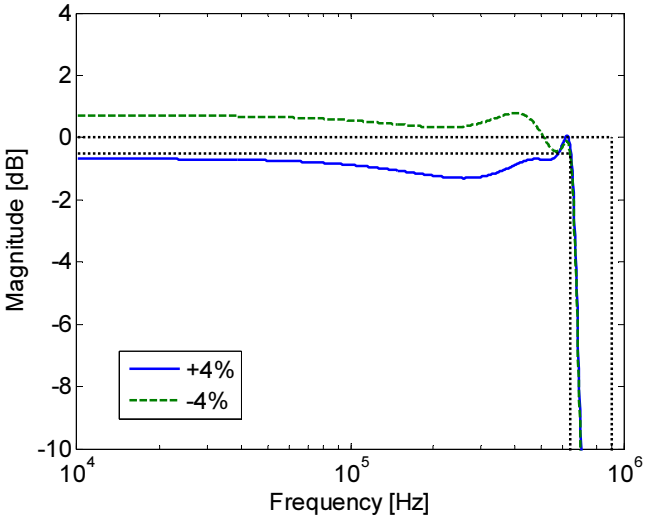
Passband with Pole Errors (1)

- $\pm$ 4% change in ω_P of first order section



Passband with Pole Errors (2)

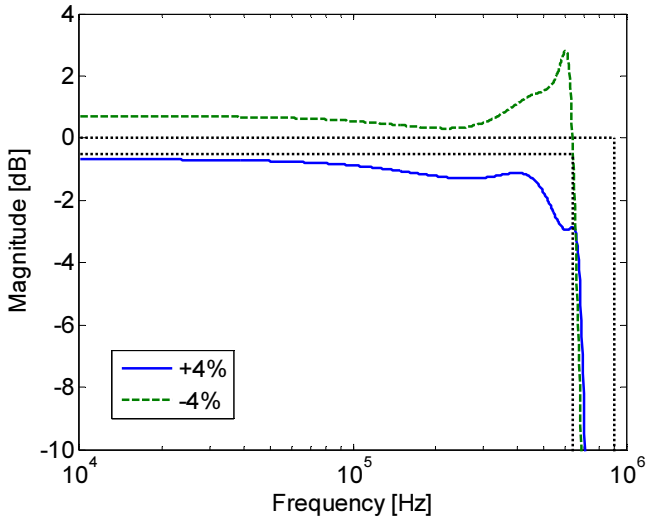
- $\pm$ 4% change in ω_P of low-Q section



Worse.

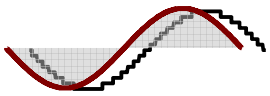
Passband with Pole Errors (3)

- $\pm$ 4% change in ω_P of high-Q section



Bad !

Ladder Filter Realization



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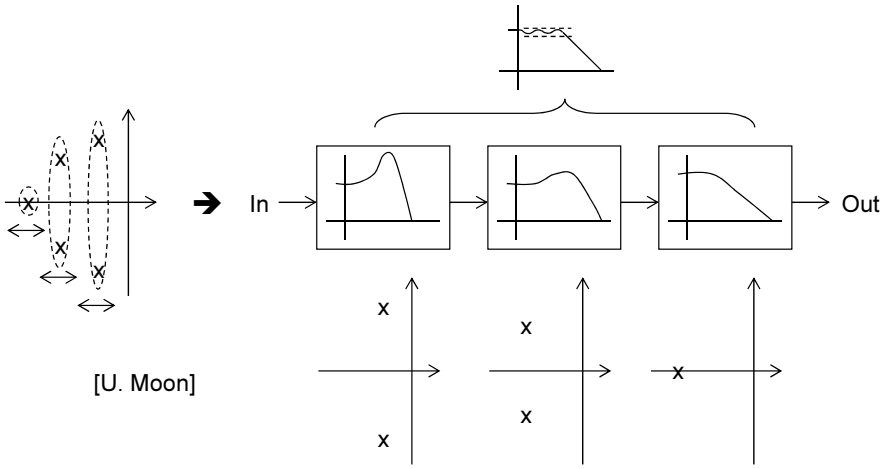
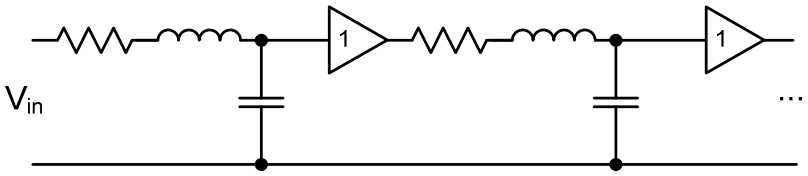
Sensitivity Problem with Cascaded Biquads



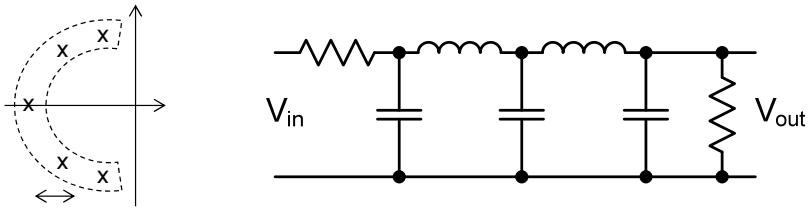
- Passband response is sensitive to shifts in the pole positions
  - Especially for high Q
- Typically, integrated continuous time filters use biquads to realize filters only up to ~5th order

Conceptual View of a Biquad Cascade



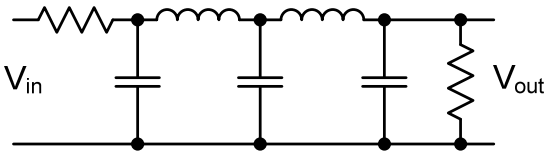
- Individual sections are actively decoupled
  - Variations in individual components affect only one pair of poles (and/or zeros)
- Ideally, we would like all the poles (and zeros) to "move together"
  - This would at least preserve the "shape" of the filter response

Doubly Terminated LC Ladder Filters

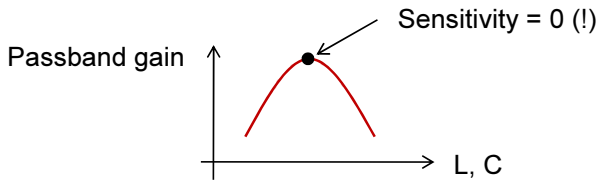


- The passband response of ladder filters is much less sensitive to component variations when compared to a biquad cascade
  - Poles "tend" to move together
- For a sensitivity analysis, see e.g.
  - G. C. Temes and H. J. Orchard, "First order sensitivity and worst-case analysis of doubly terminated reactance two-ports," IEEE Trans. Circuit Theory, 20 (5), pp. 567–571, 1973.

Basic Intuition

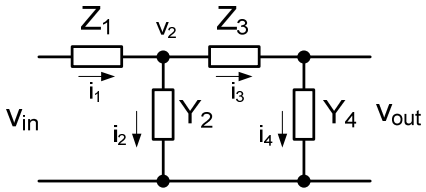


- In the passband, the gain from V_{in} to V_{out} is maximum (0.5)
- Any detuning of L and C can only reduce the passband gain
- Therefore, the passband gain is convex in L and C, and the sensitivity is zero around the nominal design point!



Analysis Example (1)

$$i_4 = v_{out} Y_4 = i_3$$
$$v_2 = i_3 Z_3 + v_{out}$$
$$i_2 = v_2 Y_2$$
$$i_1 = i_2 + i_3$$
$$v_{in} = i_1 Z_1 + v_2$$
$$= \left(v_2 Y_2 + v_{out} Y_4\right) Z_1 + v_2$$
$$= \left(\left[Y_4 Z_3 v_{out} + v_{out}\right] Y_2 + v_{out} Y_4\right) Z_1 + v_{out} Y_4 Z_3 + v_{out}$$



$$\frac{v_{out}}{v_{in}} = \frac{1}{\left(\left[Y_4 Z_3 + 1\right] Y_2 + Y_4\right) Z_1 + Y_4 Z_3 + 1}$$
$$= \frac{1}{Y_4 Z_3 Y_2 Z_1 + Y_4 Z_3 + Y_4 Z_1 + Y_2 Z_1 + 1}$$

Analysis Example (2)

- E.g. for

$$Z_1 = R_1 \qquad Z_3 = sL_3$$
$$Y_2 = sC_2 \qquad Y_4 = sC_4$$

  it follows that

$$\frac{v_{out}}{v_{in}} = \frac{1}{s^3 C_4 L_3 C_2 R_1 + s^2 C_4 L_3 + s\left(C_4 R_1 + C_2 R_1\right) + 1}$$

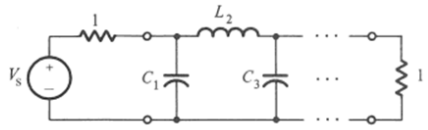
- A third order lowpass filter
- Zeros can be realized by utilizing parallel and series combinations of inductors and capacitors
- Analysis is doable
  - But very tedious!

LC Ladder Synthesis

- Filter tables
  - A. Zwerev, *Handbook of filter synthesis*, Wiley, 1967
  - R. Saal, *Handbook of filter synthesis*, AEG-Telefunken, 1979
  - A. B. Williams and F. J. Taylor, *Electronic filter design*, 3rd edition, McGraw-Hill, 1995
- CAD tools
  - http://www.circuitsage.com/filter.html
    - Comprehensive list of available tools
  - http://tonnesoftware.com/elsie.html
    - Free version of Elsie supports ladder synthesis up to 7th order
  - http://www.nuhertz.com/download.html
    - FilterFree – up to 3rd order
    - FilterSolutions – $$$
  - Agilent ADS

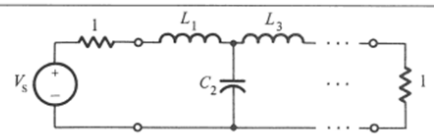
Butterworth Filter Table

TABLE 13.1 Table of Element Values for Doubly Terminated Butterworth Filters for $n = 2$ to $n = 10$ Normalized to Half-Power Frequency of 1 rad/s



n	C_1	L_2	C_3	L_4	C_5	L_6	C_7	L_8	C_9	L_{10}
2	1.414	1.414								
3	1.000	2.000	1.000							
4	0.7654	1.848	1.848	0.7654						
5	0.6180	1.618	2.000	1.618	0.6180					
6	0.5176	1.414	1.932	1.932	1.414	0.5176				
7	0.4450	1.247	1.802	2.000	1.802	1.247	0.4450			
8	0.3902	1.111	1.663	1.962	1.962	1.663	1.111	0.3902		
9	0.3473	1.000	1.532	1.879	2.000	1.879	1.532	1.000	0.3473	
10	0.3129	0.9080	1.414	1.782	1.975	1.975	1.782	1.414	0.9080	0.3129

n	L_1	C_2	L_3	C_4	L_5	C_6	L_7	C_8	L_9	C_{10}



[Schaumann]

- Denormalization

$$L_{i,den} = L_i \frac{R}{\omega_{-3dB}}$$

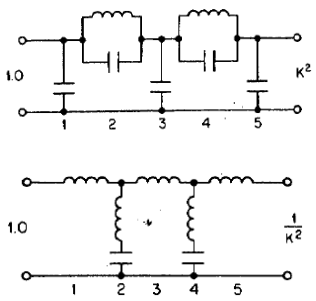
$$C_{i,den} = C_i \frac{1}{\omega_{-3dB} \cdot R}$$

- R is the desired value of the source and termination resistor

5th Order Elliptic Filter Table (1)

$$\theta = \sin^{-1}\left(\frac{\omega_p}{\omega_s}\right)$$

0.17dB passband ripple



[Williams & Taylor]
Table 11-56

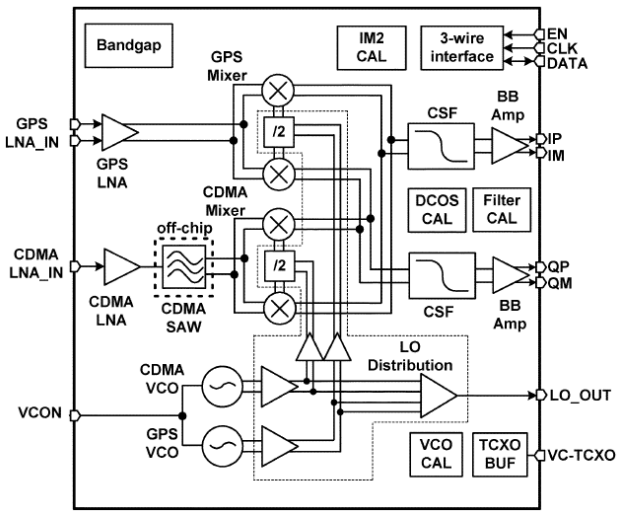
	$K^2 = 1.0$						
θ	C_1	C_2	L_2	C_3	C_4	L_4	C_5
C	1.302	0.0000	1.346	2.129	0.0000	1.346	1.302
1.0	1.30183	0.00008	1.34548	2.12855	0.00020	1.34532	1.30170
2.0	1.30163	0.00031	1.34523	2.12770	0.00082	1.34459	1.30112
3.0	1.30150	0.00070	1.34483	2.12660	0.00184	1.34339	1.30016
4.0	1.30084	0.00125	1.34426	2.12507	0.00328	1.34170	1.29881
5.0	1.30024	0.00196	1.34353	2.12311	0.00513	1.33954	1.29708
6.0	1.29951	0.00282	1.34264	2.12070	0.00740	1.33689	1.29496
7.0	1.29865	0.00384	1.34159	2.11786	0.01008	1.33376	1.29246
8.0	1.29766	0.00502	1.34037	2.11459	0.01318	1.33015	1.28957
9.0	1.29653	0.00637	1.33899	2.11088	0.01671	1.32607	1.28630
10.0	1.29527	0.00787	1.33744	2.10675	0.02067	1.32150	1.28264
11.0	1.29387	0.00953	1.33573	2.10217	0.02506	1.31646	1.27859
12.0	1.29234	0.01136	1.33386	2.09717	0.02989	1.31094	1.27417
13.0	1.29067	0.01335	1.33182	2.09172	0.03516	1.30495	1.26936
14.0	1.28887	0.01551	1.32961	2.08588	0.04089	1.29848	1.26416
15.0	1.28693	0.01783	1.32724	2.07959	0.04707	1.29154	1.25858
16.0	1.28485	0.02033	1.32470	2.07288	0.05371	1.28413	1.25261
17.0	1.28263	0.02300	1.32199	2.06574	0.06084	1.27625	1.24627
18.0	1.28027	0.02584	1.31911	2.05819	0.06844	1.26790	1.23953
19.0	1.27778	0.02885	1.31607	2.05021	0.07655	1.25909	1.23241
20.0	1.27514	0.03205	1.31285	2.04182	0.08515	1.24981	1.22491
21.0	1.27236	0.03542	1.30945	2.03301	0.09428	1.24007	1.21703
22.0	1.26943	0.03898	1.30589	2.02379	0.10393	1.22987	1.20876
23.0	1.26636	0.04272	1.30215	2.01416	0.11414	1.21921	1.20010
24.0	1.26314	0.04666	1.29823	2.00412	0.12490	1.20809	1.19107
25.0	1.25978	0.05079	1.29413	1.99368	0.13625	1.19652	1.18164
26.0	1.25262	0.05511	1.28985	1.98283	0.14819	1.18450	1.17183
27.0	1.25259	0.05963	1.28540	1.97159	0.16075	1.17203	1.16164
28.0	1.24877	0.06436	1.28075	1.95995	0.17396	1.15911	1.15106
29.0	1.22480	0.06930	1.27592	1.94792	0.18783	1.14576	1.14010
30.0	1.24067	0.07446	1.27091	1.93550	0.20239	1.13196	1.12874

5th Order Elliptic Filter Table (2)

$K^2 = 1.0$

θ	C_1	C_2	L_2	C_3	C_4	L_4	C_5
31.0	1.23638	0.07983	1.26570	1.92270	0.21768	1.11772	1.11700
32.0	1.23192	0.08543	1.26030	1.90952	0.23371	1.10305	1.10487
33.0	1.22731	0.09126	1.25470	1.89596	0.25054	1.08795	1.09235
34.0	1.22252	0.09732	1.24890	1.88203	0.26819	1.07242	1.07944
35.0	1.21757	0.10363	1.24290	1.86773	0.28671	1.05648	1.06614
36.0	1.21244	0.11019	1.23669	1.85307	0.30614	1.04011	1.05244
37.0	1.20714	0.11701	1.23028	1.83806	0.32654	1.02332	1.03835
38.0	1.20166	0.12410	1.22364	1.82269	0.34795	1.00613	1.02386
39.0	1.19600	0.13146	1.21679	1.80698	0.37044	0.98853	1.00897
40.0	1.19015	0.13911	1.20971	1.79093	0.39408	0.97053	0.99368
41.0	1.18411	0.14706	1.20241	1.77455	0.41894	0.95213	0.97798
42.0	1.17787	0.15532	1.19486	1.75784	0.44510	0.93335	0.96187
43.0	1.17144	0.16389	1.18708	1.74081	0.47265	0.91417	0.94535
44.0	1.16480	0.17280	1.17904	1.72347	0.50170	0.89462	0.92841
45.0	1.15794	0.18206	1.17075	1.70583	0.53236	0.87470	0.91105
46.0	1.15088	0.19169	1.16219	1.68789	0.56476	0.85441	0.89326
47.0	1.14359	0.20169	1.15336	1.66967	0.59903	0.83376	0.87504
48.0	1.13607	0.21210	1.14425	1.65117	0.63534	0.81276	0.85638
49.0	1.12831	0.22293	1.13484	1.63241	0.67386	0.79141	0.83727
50.0	1.12031	0.23421	1.12513	1.61339	0.71481	0.76973	0.81771
51.0	1.11206	0.24596	1.11509	1.59413	0.75841	0.74773	0.79768
52.0	1.10354	0.25821	1.10473	1.57465	0.80492	0.72541	0.77717
53.0	1.09476	0.27099	1.09401	1.55494	0.85465	0.70278	0.75619
54.0	1.08569	0.28433	1.08293	1.53504	0.90794	0.67986	0.73470
55.0	1.07633	0.29828	1.07147	1.51496	0.96518	0.65667	0.71270
56.0	1.06666	0.31288	1.05960	1.49471	1.02684	0.63320	0.69016
57.0	1.05668	0.32817	1.04731	1.47431	1.09344	0.60949	0.66709
58.0	1.04636	0.34422	1.03456	1.45379	1.16561	0.58554	0.64344
59.0	1.03570	0.36109	1.02134	1.43317	1.24407	0.56138	0.61920
60.0	1.02467	0.37885	1.00760	1.41247	1.32969	0.53702	0.59435
θ	L_1	L_2	C_3	L_3	L_4	C_4	L_5

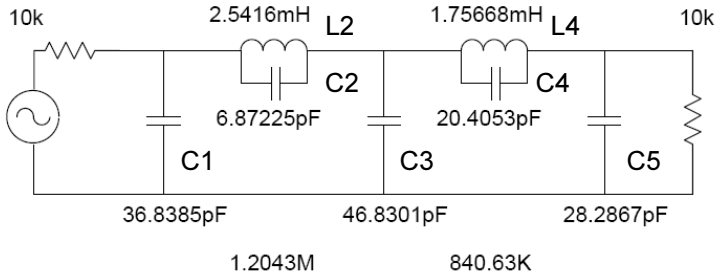
Back to Our Design Example



- Channel select filters (CSF)
  - 640 kHz passband, lowpass
  - 0.5 dB passband ripple
  - > 40 dB stopband attenuation at 900 kHz
- 5th order elliptical filter

Lim et al., "A Fully Integrated Direct-Conversion Receiver for CDMA and GPS Applications," IEEE JSSC, Nov. 2006

Synthesis Result (Using Elsie)

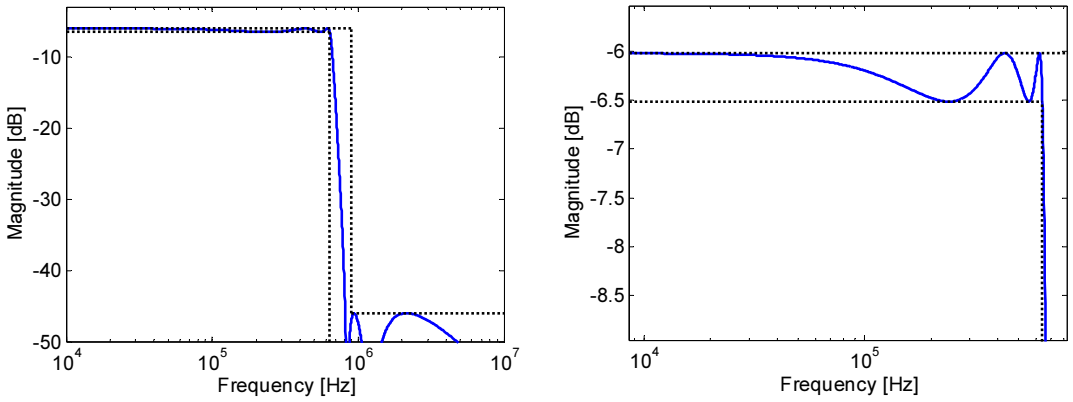


Bandwidth: 640K Family: Cauer Passband ripple: 0.49426
Stopband freq: 815K Stopband depth: 40

4/11/2009 5:56:58 PM - Elsie 2.29 - www.tonnesoftware.com

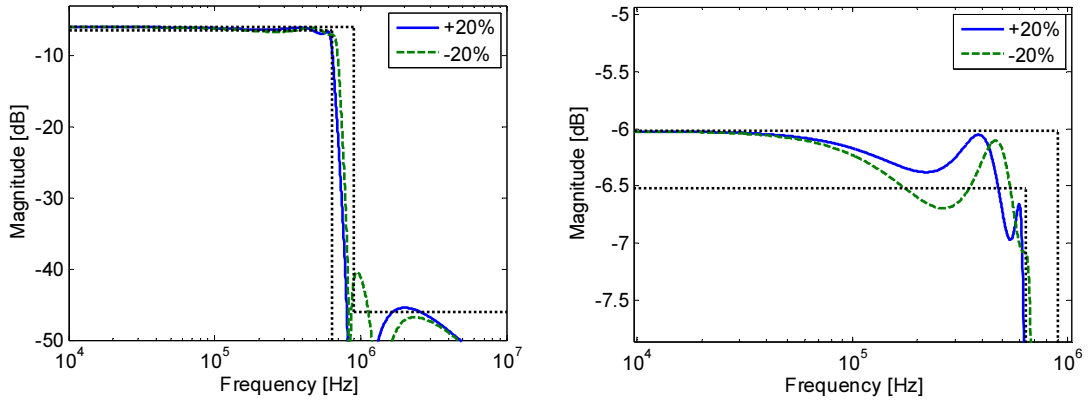
- Termination resistors arbitrarily set to 10kΩ

Spice Simulation Result



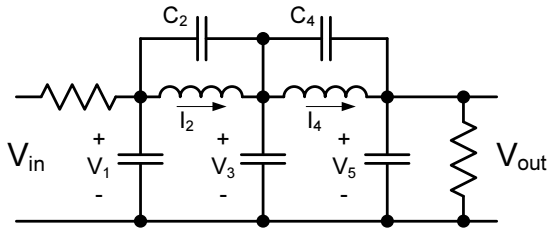
- 6 dB passband attenuation due to resistive termination
  - Easy to change to 0dB in an active realization

20% Variation in L2



- Only a very small change in the passband response; moderate degradation in the stopband
  - Smaller (i.e. more realistic) variations than 20% can be easily handled through overdesign

State-Space Description for C_1



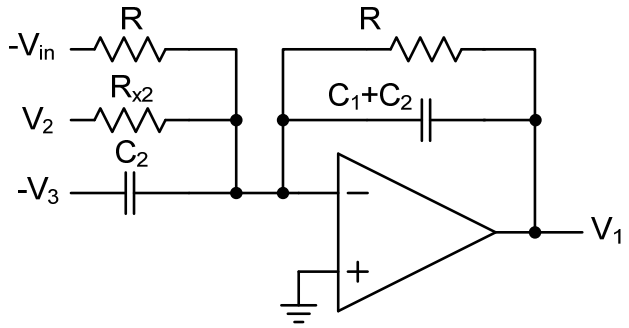
$$V_1 = \frac{I_1}{sC_1} = \frac{1}{sC_1}\left(\frac{V_{in}-V_1}{R} - I_2 + \left[V_3 - V_1\right]sC_2\right)$$

$$V_1\left(1+\frac{C_2}{C_1}\right) = \left(\frac{V_{in}-V_1}{R} - I_2\right)\frac{1}{sC_1} + V_3\frac{C_2}{C_1}$$

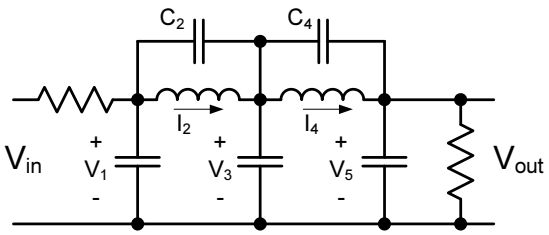
$$V_1 = -\frac{1}{s\left(C_1+C_2\right)}\left(-\frac{V_{in}}{R} + \frac{V_1}{R} + \frac{V_2}{R_{x2}} - V_3 sC_2\right)$$

Implementation of C_1 Integrator

$$V_1 = -\frac{1}{s(C_1 + C_2)}\left(-\frac{V_{in}}{R} + \frac{V_1}{R} + \frac{V_2}{R_{x2}} - V_3 s C_2\right)$$

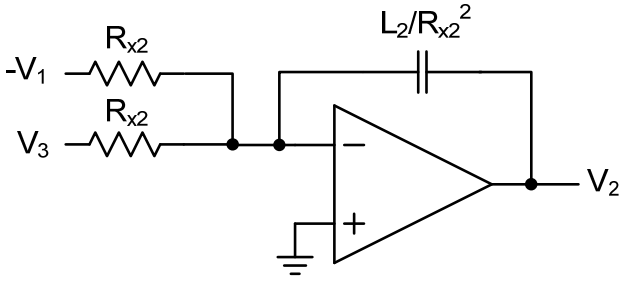


Implementation of L_2 Integrator



$$I_2 = \frac{1}{sL_2}(V_1 - V_3)$$

$$V_2 = I_2 R_{x2} = -\frac{R_{x2}^2}{sL_2}\left(-\frac{V_1}{R_{x2}} + \frac{V_3}{R_{x2}}\right)$$



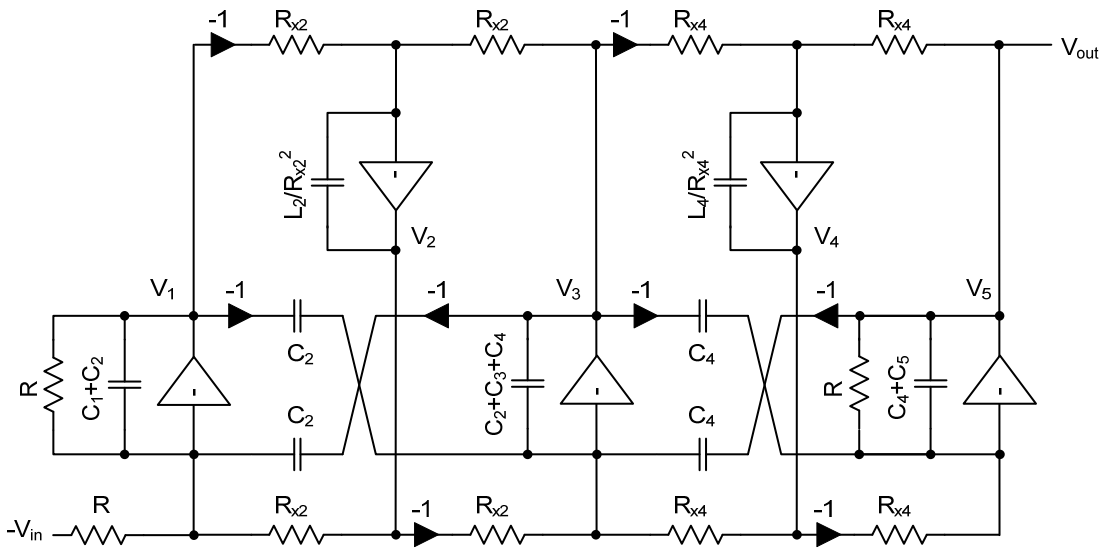
Remaining Integrators

$$V_3 = -\frac{1}{s\left(C_2 + C_3 + C_4\right)}\left(-\frac{V_2}{R_{x4}} + \frac{V_4}{R_{x4}} - V_1 sC_2 - V_5 sC_4\right)$$

$$V_4 = I_4 R_{x4} = -\frac{R_{x4}^2}{sL_4}\left(-\frac{V_3}{R_{x4}} + \frac{V_5}{R_{x4}}\right)$$

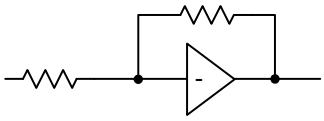
$$V_{out} = V_5 = -\frac{1}{s\left(C_4 + C_5\right)}\left(\frac{V_5}{R} - \frac{V_4}{R_{x4}} - V_3 sC_4\right)$$

Complete Realization

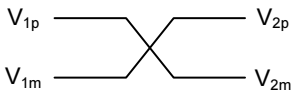


Signal Inversion

Symbol



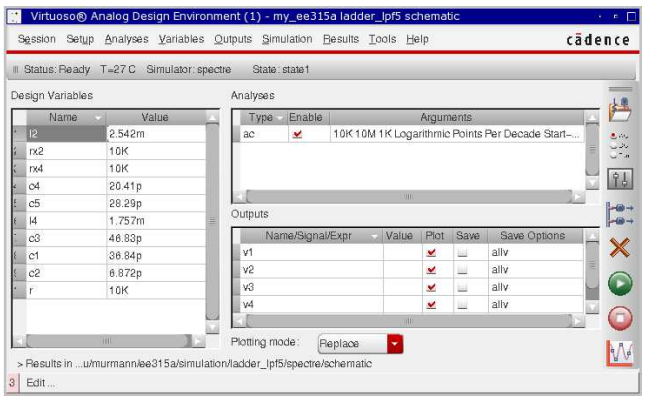
Realization in a single-ended circuit
(need only one shared circuit per state)



Realization in a differential circuit

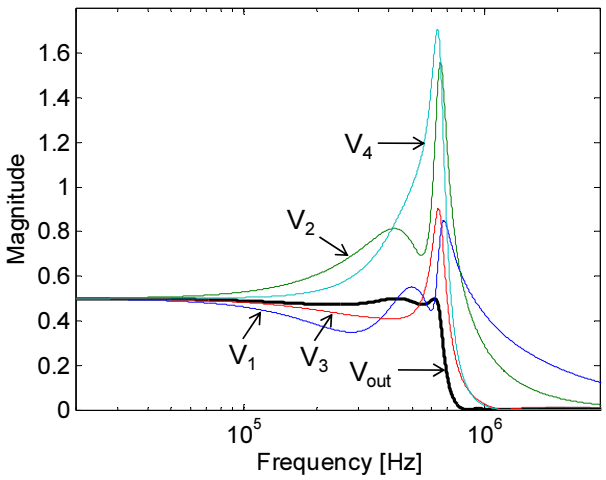
- In a first-cut (single-ended) simulation, signal inversion can also be achieved using negative resistors and capacitors

Simulation Setup



- AC analysis with 1V applied at the input
- Amplifiers are ideal, with an open loop gain of 10^6
- Set $R_{x2}=R_{x4}=R=10k\Omega$
  - Somewhat arbitrary at this point

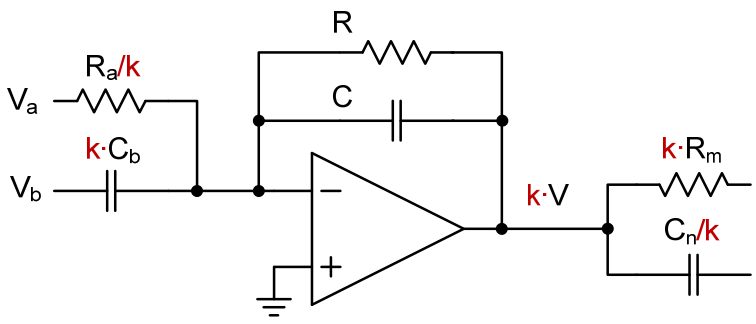
Frequency Response



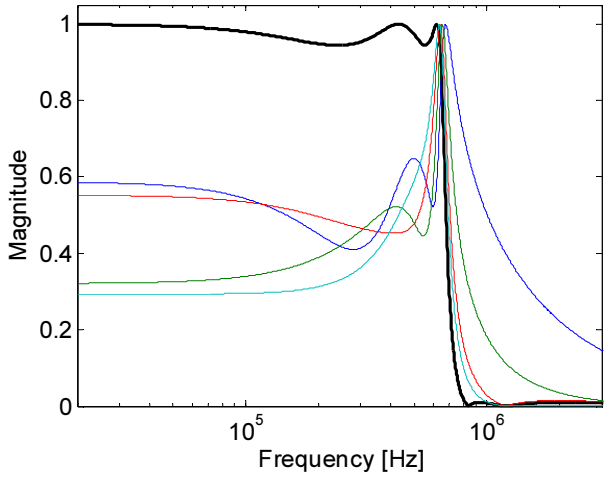
$|V_1|_{max}$ = 0.8505 V
$|V_2|_{max}$ = 1.5585 V
$|V_3|_{max}$ = 0.9039 V
$|V_4|_{max}$ = 1.7072 V
$|V_{out}|_{max}$ = 0.5000 V

Node Voltage Scaling

- To scale the peak output voltage of an integrator by a factor of k, scale all resistors and capacitors connected to the input and output node as shown below
- Feedback R and C remain unchanged
  - Will be scaled together with all other components to adjust the thermal noise (more later)



Frequency Response After 0dB Scaling

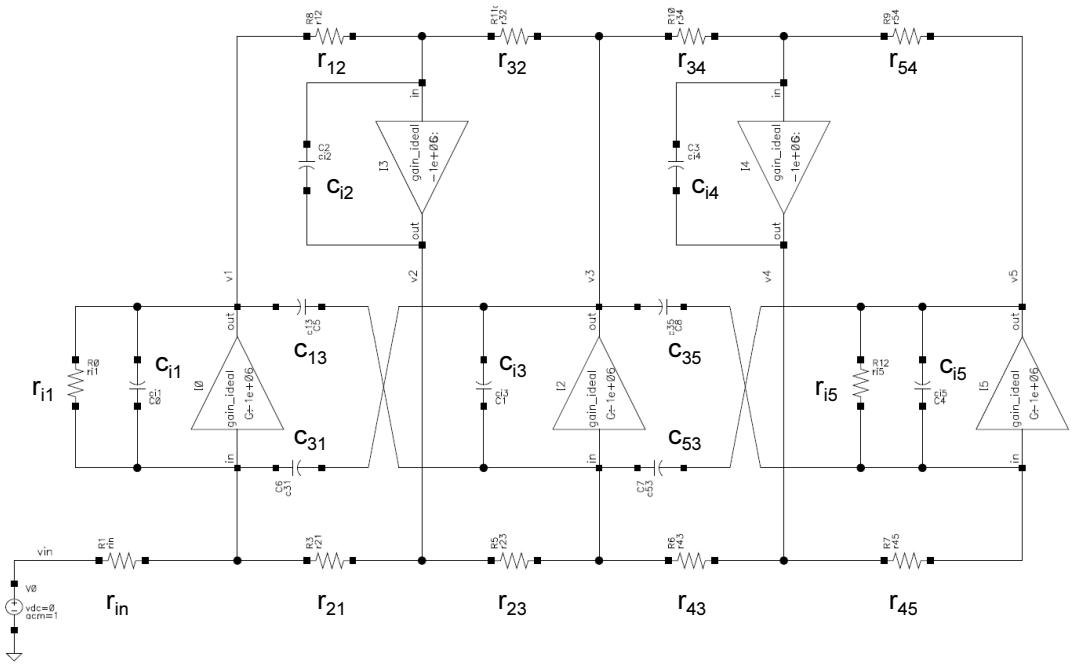


Component Values After 0dB Scaling

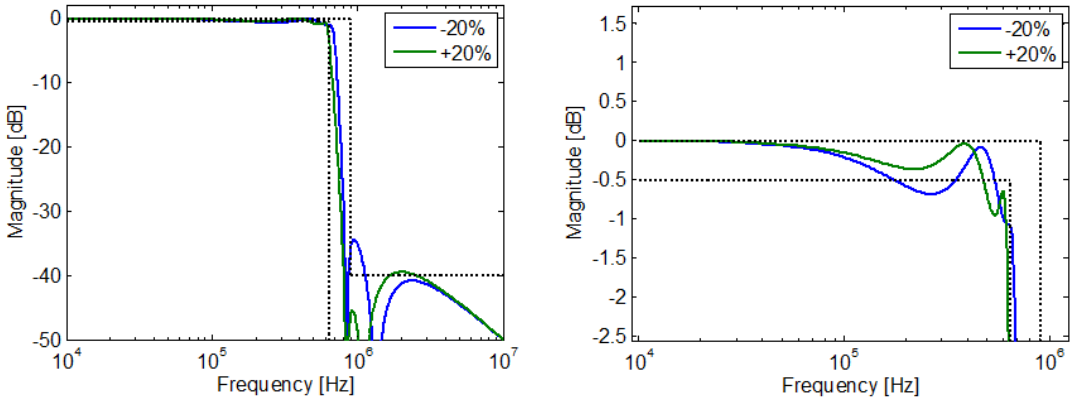
```
% feedback R [Ω] and C [F]
ci1 =   4.3711e-011
ri1 =   10000
ci2 =  2.5416e-011
ci3 =  7.4108e-011
ci4 =  1.7567e-011
ci5 =  4.8692e-011
ri5 =  10000

% coupling R [Ω]
rin = -8.5052e+003
r12 = -1.8324e+004
r21 =  5.4573e+003
r23 = -5.7997e+003
r32 =  1.7242e+004
r34 = -1.8888e+004
r43 =  5.2944e+003
r45 = -2.9287e+003
r54 =  3.4145e+004

% zero C [F]
c13 = -6.4665e-012
c31 = -7.3035e-012
c35 = -3.6888e-011
c53 = -1.1287e-011
```

- Resistors
  - R_{min} = 2.93 kΩ
  - R_{max} = 34.1 kΩ
- Capacitors
  - C_{min} = 6.47 pF
  - C_{max} = 48.7 pF
- Component spread ~10
  - Manageable in practice
  - May be able to reduce spread by scaling integration capacitors, subject to noise constraints
    - A very complex optimization problem!

Schematic



20% Variation in C_{i2}

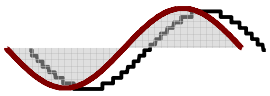


- Only small passband variations despite large component variation
- Active realization of ladder retains low sensitivity of passive prototype
- More analysis is needed to determine the actual precision requirements for all components
  - E.g. through a Monte Carlo simulation

Summary

- Higher-order filter realization
  - Cascade of biquads
    - High sensitivity often problematic for order ≥ 5
  - Ladder filters
    - Based on LC prototypes
    - Low sensitivity
    - Active RC simulation retains low sensitivity

Integrator Realization & Nonidealities



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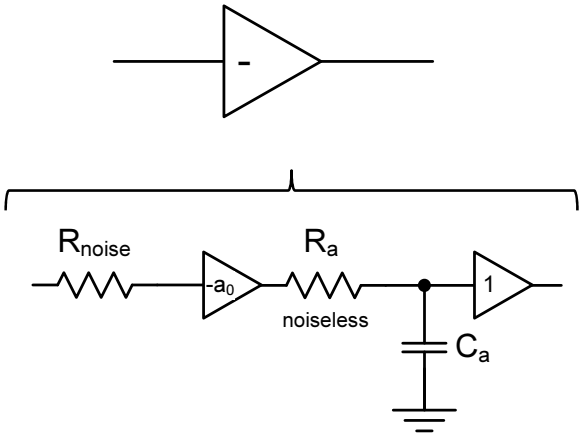
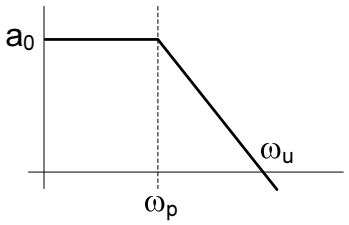
Outline

- Impact of finite amplifier bandwidth and gain in active RC integrators
- Thermal noise
  - Passive filters
  - Active RC filters
- Alternative integrator realizations
- Parameter tuning

Amplifier Model with First Order Nonidealities

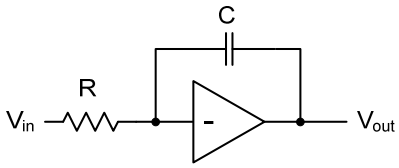




$$\omega_p = \frac{1}{R_a C_a} \qquad \omega_u \cong a_0 \cdot \omega_p$$

$$a(s) = -\frac{a_0}{1+\frac{s}{\omega_p}} \cong -\frac{a_0\omega_p}{s} \cong -\frac{\omega_u}{s} \qquad \text{for} \quad \omega >> \omega_p$$

RC Integrator with Nonideal Amplifier



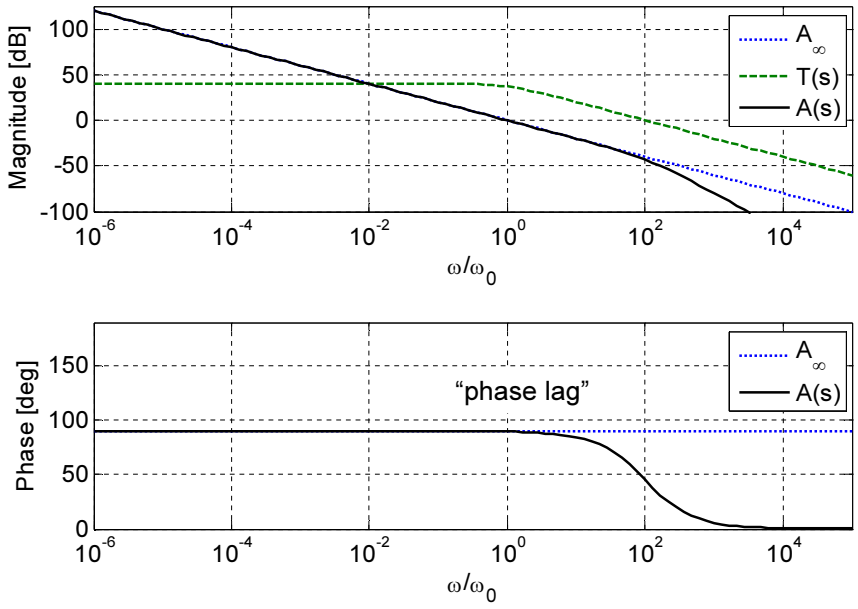
- Using return ratio analysis, we can write

$$A_\infty = -\frac{1}{sRC} = -\frac{\omega_0}{s} \qquad A(s) = \frac{V_{out}(s)}{V_{in}(s)} = A_\infty \frac{T(s)}{1+T(s)}$$

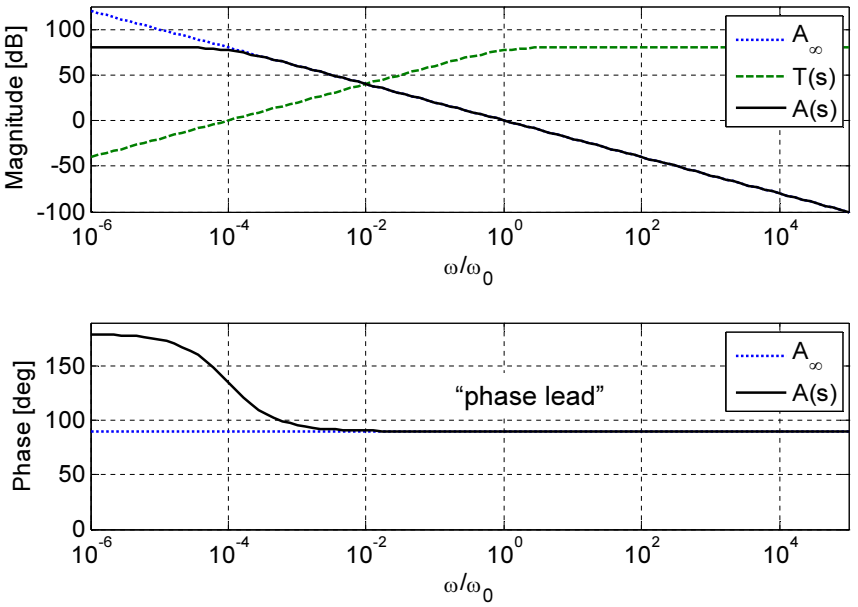
$$T(s) = -a(s)\frac{R}{R+\frac{1}{sC}} = \frac{a_0}{1+\frac{s}{\omega_p}} \frac{\frac{s}{\omega_0}}{1+\frac{s}{\omega_0}} \qquad \omega_p \cong \frac{\omega_u}{a_0}$$

- As long as T(s) is large, the transfer function A(s) is close to the desired ideal transfer function (A_∞)

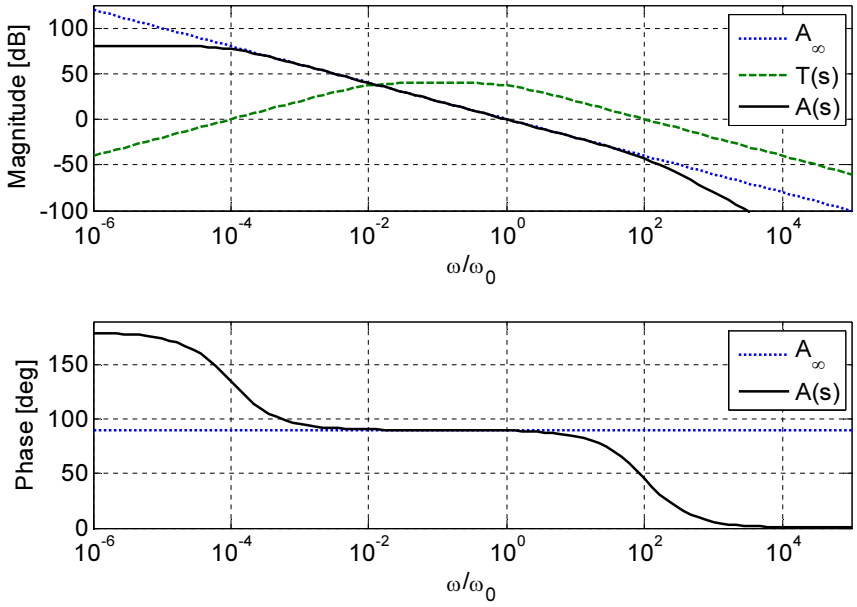
$a_0 \to \infty$, $\omega_u = 100\omega_0$



$a_0 = 10{,}000$, $\omega_u \to \infty$



a_0=10,000, ω_u=100ω_0



RC Integrator with Finite ω_u

- Ignoring finite DC gain for the time being, i.e. using

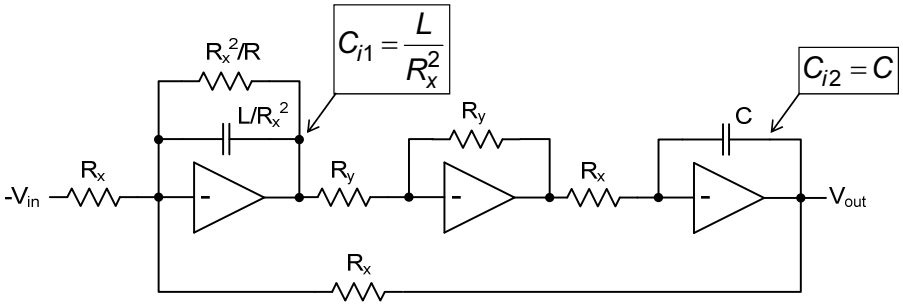
$$a(s) = -\frac{\omega_u}{s}$$

- The equations from slide 4 yield for this case

$$A_{actual}(s) = \underbrace{-\frac{\omega_o}{s}}_{A_{ideal}} \underbrace{\frac{1}{1+\frac{\omega_0}{\omega_u}}}_{\text{Magnitude error}} \underbrace{\frac{1}{1+\frac{s}{\omega_o+\omega_u}}}_{\text{Undesired pole (Magnitude and phase error)}}$$

- The first error term modifies only the magnitude, and effectively alters the integration time constant (RC = $1/\omega_0$)

Significance of ω_0 (Biquad Example)



$$H(s) = -\frac{1}{1 + sRC + s^2LC} = -\frac{1}{1 + \frac{s}{\omega_P Q_P} + \frac{s^2}{\omega_P^2}} \qquad \omega_P = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{R_x C_{i1} R_x C_{i2}}} = \sqrt{\omega_{01} \cdot \omega_{02}}$$

- Integrator ω_0 typically not too far off from pole frequency ω_P

Baseline Requirement for ω_u

$$A_{actual}(s) = \underbrace{-\frac{\omega_o}{s}}_{A_{ideal}} \underbrace{\frac{1}{1 + \frac{\omega_0}{\omega_u}}}_{\text{Magnitude error}} \underbrace{\frac{1}{1 + \frac{s}{\omega_o + \omega_u}}}_{\text{Undesired pole (Magnitude and phase error)}}$$

- High-Q filters will be sensitive to variations and uncertainty in the "effective" value of ω_0
- In a practical design, we therefore require $\omega_u >> \omega_0$, typically $\omega_u = 10\ldots50 \cdot \omega_0$
- Assuming that we comply with this guideline, we are left with

$$A_{actual}(s) \cong -\frac{\omega_o}{s} \frac{1}{1 + \frac{s}{\omega_u}}$$

Effect on Filter Response

- For a filter that uses ideal integrators, we know that

$$H_{\text{filter}}(s)\Big|_{s=p_{\text{ideal}}} \to \infty$$

- For the case with finite ω_u

$$H_{\text{filter}}\left(s\left(1+\frac{s}{\omega_u}\right)\right)\Bigg|_{s=p_{\text{actual}}} \to \infty$$

and therefore

$$p_{\text{ideal}} = p_{\text{actual}}\left(1+\frac{p_{\text{actual}}}{\omega_u}\right) \qquad p_{\text{ideal}} = \alpha_i \pm j\beta_i \qquad p_{\text{actual}} = \alpha_a \pm j\beta_a$$

Solving for p_{actual} (1)

$$\alpha_i + j\beta_i = \left(\alpha_a + j\beta_a\right)\left(1+\frac{\alpha_a + j\beta_a}{\omega_u}\right)$$

- Equating real and imaginary parts, we find

$$\alpha_i = \alpha_a\left(1+\frac{\alpha_a}{\omega_u}\right)-\frac{\beta_a^2}{\omega_u} \qquad \beta_i = \beta_a\left(1+2\frac{\alpha_a}{\omega_u}\right)$$

- To proceed, it makes sense to customize the analysis for high-Q poles, which should represent the most critical case

$$Q_{\text{Pideal}} = -\frac{1}{2}\frac{\omega_{\text{Pideal}}}{\alpha_i} >> 1 \qquad \omega_{\text{Pideal}} = \sqrt{\alpha_i^2+\beta_i^2} \cong \beta_i$$

$$Q_{\text{Pactual}} = -\frac{1}{2}\frac{\omega_{\text{Pactual}}}{\alpha_a} >> 1 \qquad \omega_{\text{Pactual}} = \sqrt{\alpha_a^2+\beta_a^2} \cong \beta_a$$

Solving for p_{actual} (2)

$$\alpha_i = \alpha_a\left(1+\frac{\alpha_a}{\omega_u}\right)-\frac{\beta_a^2}{\omega_u} \qquad \beta_i = \beta_a\left(1+2\frac{\alpha_a}{\omega_u}\right)$$

- We can now simplify using

$$\alpha_a << \omega_{Pactual} \cong \omega_0 << \omega_u$$

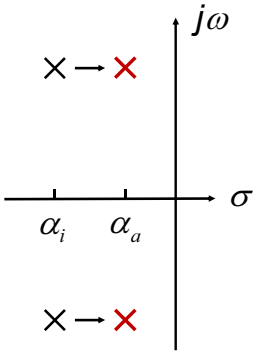
to obtain

$$\alpha_i \cong \alpha_a - \frac{\beta_a^2}{\omega_u} \qquad \beta_i \cong \beta_a$$

$$\alpha_a \cong \alpha_i + \frac{\beta_a^2}{\omega_u} \qquad \beta_a \cong \beta_i$$

- Negligible change in the pole's imaginary part; real part affected by finite ω_u

Effect on Pole Locations



$$\alpha_a \cong \alpha_i + \frac{\beta_a^2}{\omega_u}$$

$$Q_{Pactual} = -\frac{1}{2}\frac{\omega_{Pactual}}{\alpha_i+\frac{\beta_a^2}{\omega_u}} \cong -\frac{1}{2}\frac{\omega_{Pideal}}{\alpha_i+\frac{\omega_{Pideal}^2}{\omega_u}} = -\frac{1}{2}\frac{\omega_{Pideal}}{\alpha_i}\frac{1}{1+\frac{\omega_{Pideal}^2}{\alpha_i\omega_u}}$$

$$= Q_{Pideal}\frac{1}{1-2Q_{Pideal}\frac{\omega_{Pideal}}{\omega_u}} \cong Q_{Pideal}\left(1+2Q_{Pideal}\frac{\omega_{Pideal}}{\omega_u}\right)$$

- Example for $Q_{Pideal} = 30$, <2% (0.17dB) increase in $Q_{Pactual}$

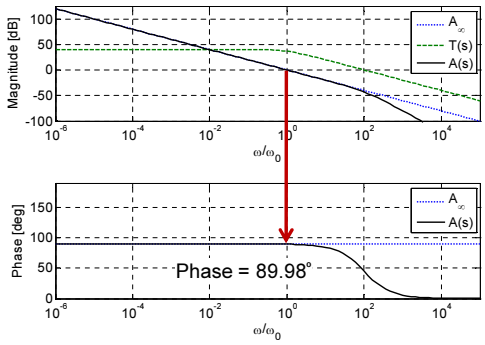
$$2\cdot 30\cdot\frac{\omega_{Pideal}}{\omega_u} < 2\% \qquad \frac{\omega_u}{\omega_{Pideal}} > 3000 \quad (!)$$

Corresponding Phase Error

- For $\omega_u = 3000\omega_{Pideal}$ and $\omega_{Pideal} \cong \omega_0$

  we can estimate the phase error of the integrator at ω_0 using

$$\phi_{err} = \angle\left(\frac{1}{1+j\frac{\omega_0}{\omega_u}}\right) \cong \angle\left(1-j\frac{\omega_{P_{ideal}}}{\omega_u}\right) = \tan^{-1}\left(-\frac{\omega_{P_{ideal}}}{\omega_u}\right) \cong -\frac{1}{3000} = -\frac{1}{3000}\cdot\frac{180^\circ}{\pi} = -0.02^\circ$$



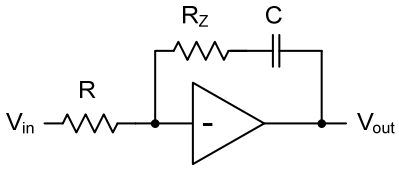
Pole-Zero Cancellation (1)

$$H(s) = -\frac{1+sR_zC}{sRC\left(1+\frac{s}{\omega_u}\right)+\frac{s}{\omega_u}(1+sR_zC)}$$

$$= \underbrace{-\frac{1}{sRC}}_{\text{Ideal response}} \underbrace{\frac{1+sR_zC}{1+\frac{s}{\omega_u}+\frac{1}{\omega_u RC}(1+sR_zC)}}_{\text{Should be 1}}$$

$$= -\frac{\omega_o}{s}\frac{1+sR_zC}{1+\frac{\omega_o}{\omega_u}+\frac{s}{\omega_u}\left(1+\frac{R_z}{R}\right)}$$

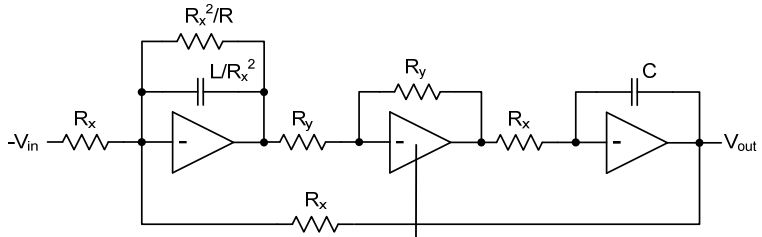
$$= -\frac{\omega_o}{s}\frac{1}{1+\frac{\omega_o}{\omega_u}}\frac{1+sR_zC}{1+s\frac{\left(1+\frac{R_z}{R}\right)}{\omega_u\left(1+\frac{\omega_o}{\omega_u}\right)}}$$



Pole-Zero Cancellation (2)

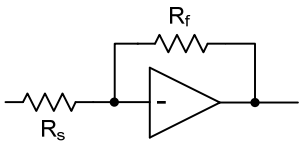
- We can achieve "ideal" operation by letting $$\frac{\left(1+\frac{R_z}{R}\right)}{\omega_u\left(1+\frac{\omega_o}{\omega_u}\right)} = R_z C$$
- Assuming $\omega_u >> \omega_0$, this is accomplished for $$R_z \cong \frac{1}{\omega_u C}$$
- In high-speed filters, this trick typically helps reduce the amplifier bandwidth requirements by more than an order of magnitude
  - Note that the requirements do not drop to "zero" because we still need to maintain $\omega_u >> \omega_0$
- Practicality issue: How to ensure that R_Z tracks variations in ω_u and C, for both global variations and random mismatch errors

Auxiliary Amplifiers



$$A_\infty = -\frac{R_f}{R_s}$$

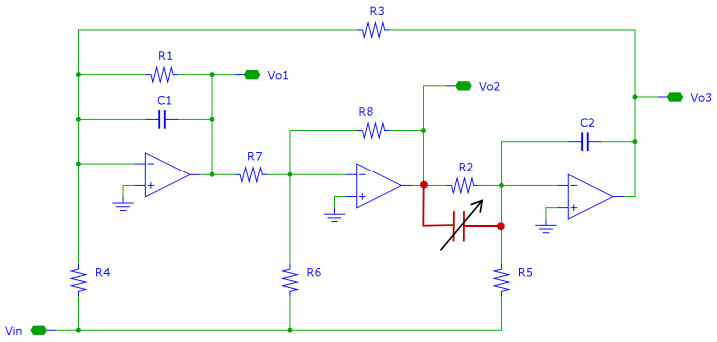
$$T(s) \cong \frac{\omega_u}{s}\frac{R_s}{R_s+R_f}$$



$$A(s) = -\frac{R_f}{R_s}\frac{1}{1+\frac{s}{\omega_u}\left(1+\frac{R_f}{R_s}\right)}$$

- No (good) way to cancel error from inverting or summing amplifiers
  - But these amplifiers also contribute to the overall phase shift

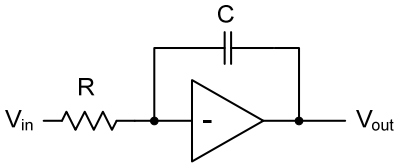
"Tweaking" a Tow-Thomas Biquad



L. C. Thomas, "The Biquad: Part I -Some Practical Design Considerations," IEEE Trans. Ckt. Theory, Vol. CT-I, No. 3, May 1971.

- May be able to cancel the phase error from all stages by introducing a "strategically" tuned zero
  - Practicality questionable

RC Integrator with Finite Gain



$$a(s) = -a_0$$

$$T(s) = a_0 \frac{R}{R + \frac{1}{sC}} = a_0 \frac{sRC}{sRC + 1}$$

$$A_{actual}(s) = -\frac{1}{sRC}\frac{1}{1+\frac{1}{T(s)}} = -\frac{1}{sRC}\frac{1}{1+\frac{1+sRC}{a_0 sRC}} = -\omega_0 \frac{1}{s\left(1+\frac{1}{a_0}\right)+\frac{\omega_0}{a_0}}$$

Effect on Filter Response

- For the case of finite gain, we can therefore write

$$p_{\text{ideal}} = p_{\text{actual}}\left(1+\frac{1}{a_0}\right)+\frac{\omega_0}{a_0}$$

- For the case of high-Q poles, it can then be shown that

$$Q_{\text{Pactual}} \cong Q_{Pideal}\frac{1}{1+2\frac{Q_{Pideal}}{a_0}} \cong Q_{Pideal}\left(1-2\frac{Q_{Pideal}}{a_0}\right)$$

- Example for $Q_{\text{pideal}} = 30$, <2% (0.17dB) decrease in Q_{Pactual}

$$2\cdot\frac{30}{a_0} < 2\% \qquad a_0 > 3000$$

Summary

- Finite amplifier bandwidth leads to Q_P enhancement
  - Typically seen as excess peaking in the filter's magnitude response
- Finite amplifier gain leads to Q_P degradation
  - Typically seen as droop in the filter's magnitude response
- Wait!
  - Can't we cancel the Q_P enhancement against the Q_P degradation?

Q-Tuning

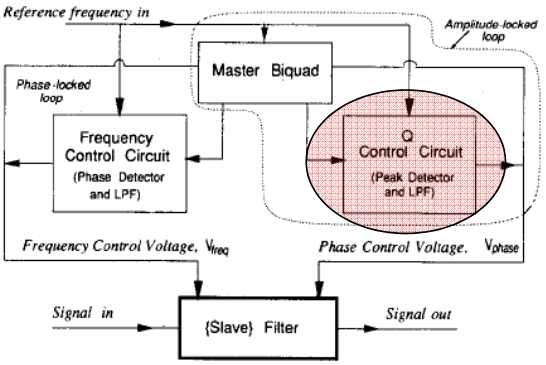


Fig. 1. Master–slave tuning scheme.

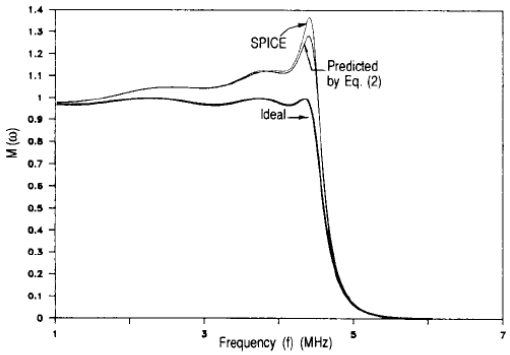
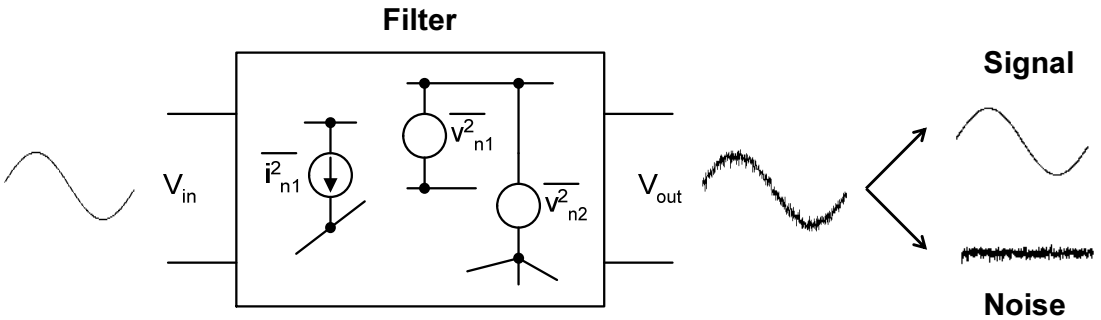


Fig. 2. Prediction of filter response with integrator nonidealities.

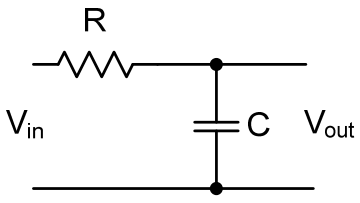
V. Gopinathan et al., "Design Considerations for High-Frequency Continuous-Time Filters and Implementation of an Anti-aliasing Filter for Digital Video," IEEE JSSC, Vol. 25, No. 6, Dec. 1990.

Noise



$$SNR = \frac{P_{signal}}{P_{noise}} = \frac{\frac{1}{2}\hat{v}^2_{out}}{\int_{f_1}^{f_2} \frac{\overline{v^2_{out}}}{\Delta f} \cdot df}$$

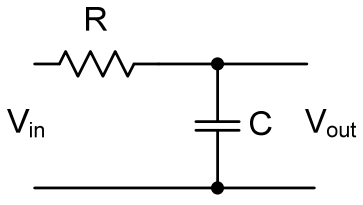
RC Lowpass Filter



$$\overline{v_{out}^2} = \int_{f_1}^{f_2} 4kTR \cdot \left| \frac{1}{1 + j2\pi f \cdot RC} \right|^2 df$$

$$= 4kTR \int_{f_1}^{f_2} \frac{df}{1 + (2\pi fRC)^2}; \qquad \int \frac{du}{1+u^2} = tan^{-1} u$$

Total Integrated Noise



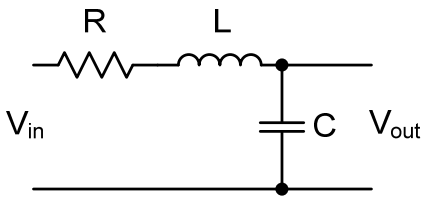
$$\overline{v_{out,tot}^2} = \int_0^{\infty} 4kTR \cdot \left| \frac{1}{1 + j2\pi f \cdot RC} \right|^2 df$$

$$= 4kTR \int_0^{\infty} \frac{df}{1 + (2\pi fRC)^2}; \qquad \int \frac{du}{1+u^2} = tan^{-1} u$$

$$= 4kTR \cdot \frac{1}{4RC}$$

$$= \frac{kT}{C}$$

LC Lowpass Filter



$$\overline{v_{out,tot}^2} = \int_0^\infty 4kTR \cdot \left| \frac{1}{1 + \frac{s}{\omega_P Q_P} + \frac{s^2}{\omega_P^2}} \right|^2 df$$

$$\omega_P = \frac{1}{\sqrt{LC}}$$

$$Q_P = \frac{1}{R}\sqrt{\frac{L}{C}}$$

Useful Integrals

$$\int_0^\infty \left| \frac{1}{1 + \frac{s}{\omega_0}} \right|^2 df = \frac{\omega_0}{4}$$

$$\int_0^\infty \left| \frac{1}{1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}} \right|^2 df = \frac{\omega_0 Q}{4}$$

$$\int_0^\infty \left| \frac{\frac{s}{\omega_0}}{1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}} \right|^2 df = \frac{\omega_0 Q}{4}$$

$$\int_0^\infty \left| \frac{n_2 s^2 + n_1 s + n_0}{d_3 s^3 + d_2 s^2 + d_1 s + d_0} \right|_{s=j\omega}^2 df = 1/4 \, \frac{{n_2}^2 d_1 d_0 + {n_1}^2 d_3 d_0 + {n_0}^2 d_3 d_2 - 2\, n_2\, n_0\, d_3\, d_0}{d_3\ (d_2\, d_1 - d_3\, d_0)\, d_0}$$

A. Dastgheib and B. Murmann, "Calculation of total integrated noise in analog circuits," *IEEE Trans. on Circuits and Systems I,* Vol. 55, pp. 2988-2993, Nov. 2008.

Total Integrated Noise of LC Filter

$$\overline{v_{out,tot}^2} = \int_0^\infty 4kTR \cdot \left| \frac{1}{1 + \frac{s}{\omega_P Q_P} + \frac{s^2}{\omega_P^2}} \right|^2 df$$

$$= 4kTR \frac{\omega_P Q_P}{4}$$

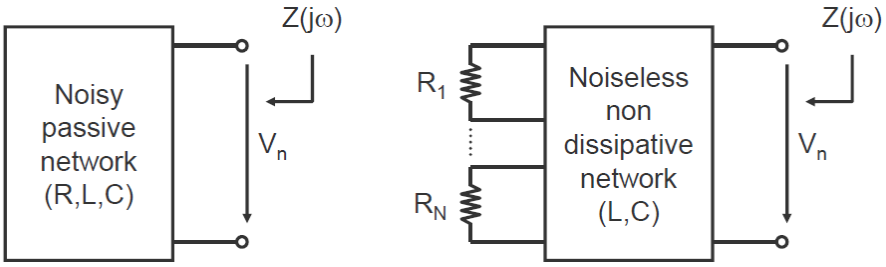
$$= \frac{kT}{C}$$

$$\omega_P = \frac{1}{\sqrt{LC}}$$

$$Q_P = \frac{1}{R}\sqrt{\frac{L}{C}}$$

$$\omega_P Q_P = \frac{1}{RC}$$

The Nyquist Theorem

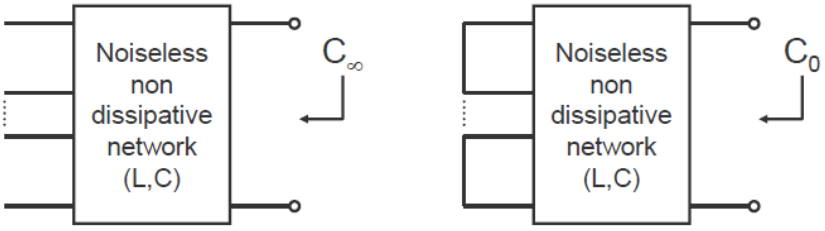


Christian C. Enz and Eric A. Vittoz, Charge-Based MOS Transistor Modeling: The EKV Model for Low-Power and RF IC Design, Wiley, 2006 (p. 106)

$$\frac{\overline{v_n^2}}{\Delta f} = 4kT \cdot Re\{Z(j2\pi f)\}$$ PSD

$$\overline{v_n^2} = 4kT \cdot \int_0^\infty Re\{Z(j2\pi f)\}$$ Variance

The Bode Theorem



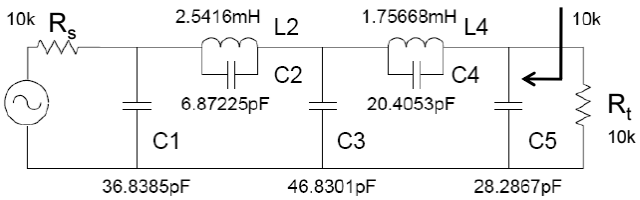
Christian C. Enz and Eric A. Vittoz, Charge-Based MOS Transistor Modeling: The EKV Model for Low-Power and RF IC Design, Wiley, 2006 (p. 107)

$$\frac{1}{C_\infty} = \lim_{s\to\infty}[s \cdot Z(s)] \qquad \frac{1}{C_0} = \lim_{s\to\infty}[s \cdot Z(s)]$$

$$\boxed{\overline{v_n^2} = kT \cdot \left[\frac{1}{C_\infty} - \frac{1}{C_0}\right]}$$

- Let's you calculate the total integrated noise of passive networks without sweating through integrals!

Example: LC Ladder



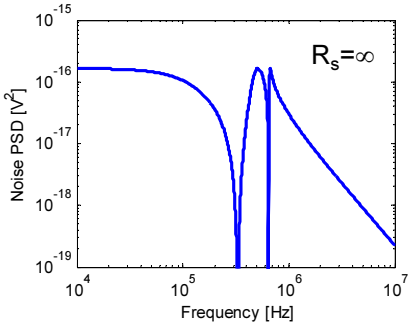
$$C_\infty = 43pF \qquad \frac{1}{C_0} = 0$$

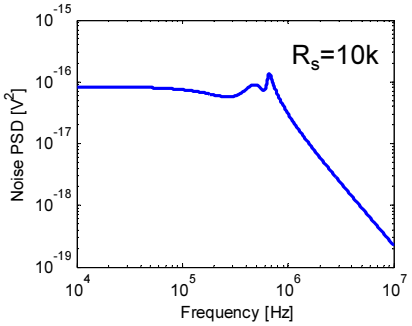
$$\boxed{\overline{v_n^2} = \frac{kT}{C_\infty} = 9.7\mu V_{rms}}$$

Simulation with and without R_s (makes no difference!)

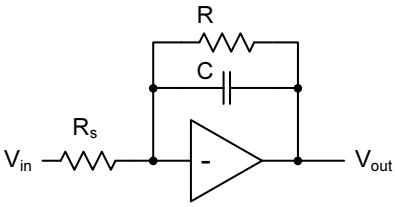
```
**** the results of the sqrt of integral (v**2 / freq)
 **** total output noise voltage   =    9.6683u volts
```

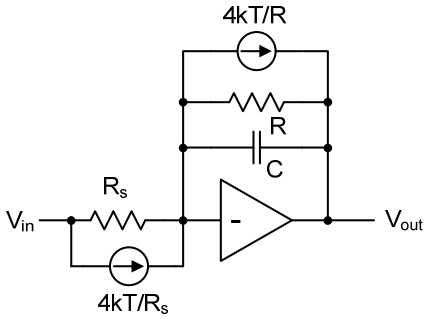
```
**** the results of the sqrt of integral (v**2 / freq)
 **** total output noise voltage   =    9.6683u volts
```





Active RC Lowpass



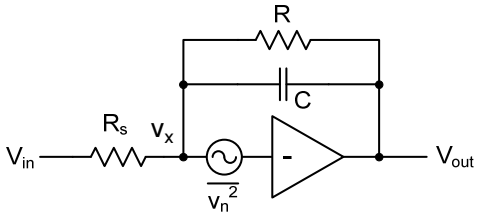


$$\overline{v_{out,res}^2} = \int_0^\infty 4kT\left(\frac{1}{R}+\frac{1}{R_s}\right)\cdot\left|\frac{R}{1+j2\pi f\cdot RC}\right|^2 df$$

$$= \int_0^\infty 4kT\left(R\left[1+\frac{R}{R_s}\right]\right)\cdot\left|\frac{1}{1+j2\pi f\cdot RC}\right|^2 df$$

$$= \frac{kT}{C}\left(1+\frac{R}{R_s}\right)$$ (noise due to resistors only)

Amplifier Noise Analysis (1)



$$\overline{v_n^2} = 4kTR_{noise}\Delta f$$

$$v_{out} = -\frac{\omega_u}{s}\left(v_x + v_n\right) \qquad \frac{v_x}{v_{out}} = \frac{R_s}{R_s+\frac{1}{\frac{1}{R}+sC}} = \frac{1}{1+\frac{R}{R_s}}\frac{1+\frac{s}{\omega_0}}{1+\frac{s}{\omega_x}}$$

$$\omega_0 = \frac{1}{RC} \qquad \omega_x = \frac{1}{R_xC} \qquad R_x = R\|R_s$$

Amplifier Noise Analysis (2)

- Solving for v_{out}/v_n yields

$$\frac{v_{out}}{v_n} = -\frac{R}{R_x}\frac{1+\frac{s}{\omega_x}}{1+s\left(\frac{1}{\omega_u}\frac{R}{R_x}+\frac{1}{\omega_0}\right)+\frac{s^2}{\omega_u\omega_0}}$$

$$\overline{v_{out,amp}^2} = \int_0^\infty 4kTR_{noise}\cdot\left(\frac{R}{R_x}\right)^2\left|\frac{1+\frac{s}{\omega_x}}{1+s\left(\frac{1}{\omega_u}\frac{R}{R_x}+\frac{1}{\omega_0}\right)+\frac{s^2}{\omega_u\omega_0}}\right|^2 df$$

$$\int_0^\infty\left|\frac{1+\frac{s}{z}}{1+\frac{s}{\omega_n Q}+\frac{s^2}{\omega_n^2}}\right|^2 df = \frac{\omega_n Q}{4}\left(1+\frac{\omega_n^2}{|z|^2}\right)$$

$$\omega_n Q = \left(\frac{1}{\omega_u}\frac{R}{R_x}+\frac{1}{\omega_0}\right)^{-1}$$

$$\omega_n^2 = \omega_u\omega_0 \qquad z = -\omega_x$$

Amplifier Noise Analysis (3)

$$\overline{v_{out,amp}^2} = 4kTR_{noise}\left(\frac{R}{R_x}\right)^2\frac{\omega_n Q}{4}\left(1+\frac{\omega_n^2}{|z|^2}\right) = kTR_{noise}\left(\frac{R}{R_x}\right)^2\left(\frac{1}{\frac{1}{\omega_u}\frac{R}{R_x}+\frac{1}{\omega_0}}\right)\left(1+\frac{\omega_u\omega_0}{\omega_x^2}\right)$$

$$= kTR_{noise}\omega_u\left(\frac{1+\frac{\omega_u}{\omega_0}\left[\frac{R_x}{R}\right]^2}{\frac{R_x}{R}\left(1+\frac{\omega_u}{\omega_0}\frac{R_x}{R}\right)}\right) \cong kTR_{noise}\omega_u$$

$$\cong \frac{kT}{C}\frac{R_{noise}}{R}\frac{\omega_u}{\omega_0}$$

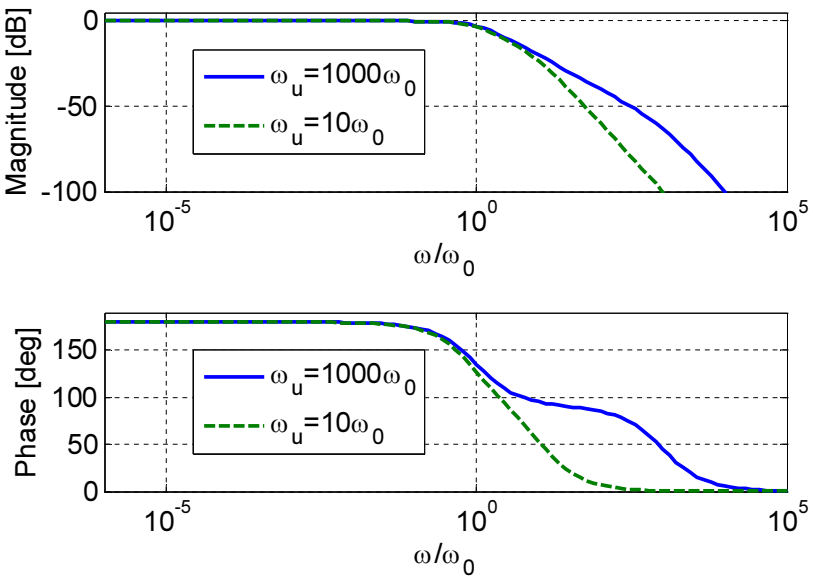
Note: The same result can be obtained by approximating v_{out}/v_n as a single pole response before carrying out the integral.

Total Noise for Active RC Filter

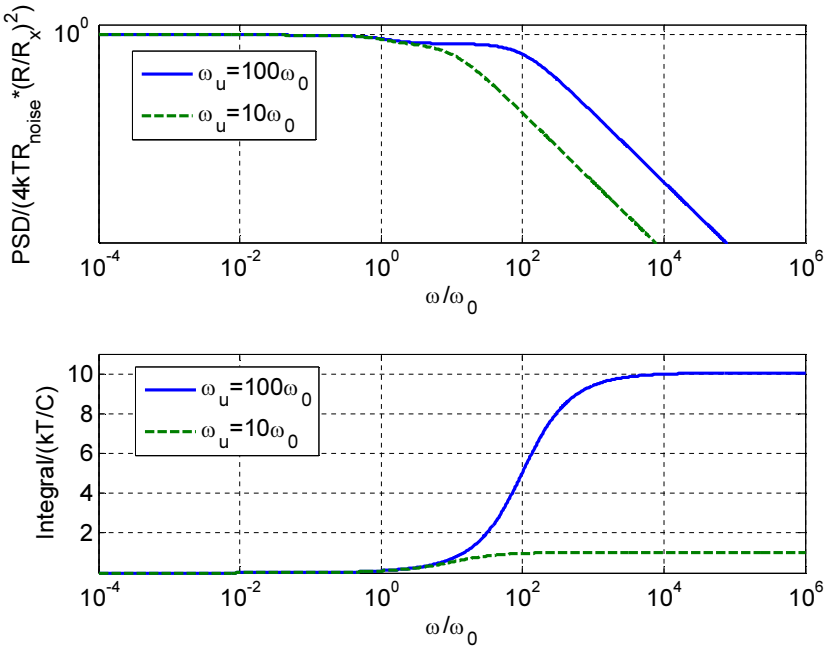
$$\overline{v_{out,tot}^2} = \overline{v_{out,res}^2} + \overline{v_{out,amp}^2} \cong \frac{kT}{C}\left(1 + \frac{R}{R_s} + \frac{R_{noise}}{R}\frac{\omega_u}{\omega_0}\right)$$

- Amplifier noise contribution is large for large ω_u/ω_0
  - But, unfortunately, we need $\omega_u >> \omega_0$ to maintain an accurate transfer function
- Given that we need $\omega_u >> \omega_0$, the only option we have is to choose $R_{noise} << R$ to minimize amplifier noise
  - In a transistor-level implementation, this requires large g_m (and large I_{BIAS}), since $R_{noise} \sim 1/g_m$

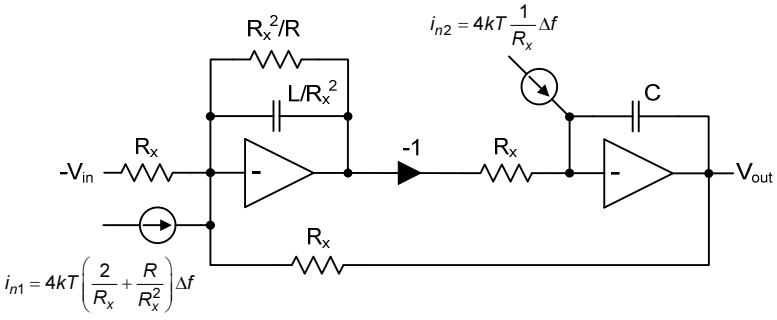
Frequency Response with Finite ω_u



Amplifier Noise Contribution (R_{noise}=0.1R)



Active Second Order Lowpass



$$H(s) = \frac{1}{1 + \frac{s}{\omega_P Q_P} + \frac{s^2}{\omega_P^2}}$$

$$\omega_P = \frac{1}{\sqrt{LC}}$$

$$Q_P = \frac{1}{R}\sqrt{\frac{L}{C}}$$

$$\frac{v_{out}}{i_{n1}} = \frac{R_x}{1 + \frac{s}{\omega_P Q_P} + \frac{s^2}{\omega_P^2}}$$

$$\frac{v_{out}}{i_{n2}} = R\frac{\left(1 + s\frac{Q_P}{\omega_P}\right)}{1 + \frac{s}{\omega_P Q_P} + \frac{s^2}{\omega_P^2}} \cong R\frac{s\frac{Q_P}{\omega_P}}{1 + \frac{s}{\omega_P Q_P} + \frac{s^2}{\omega_P^2}}$$

(after some algebra)

Analysis

$$\overline{v_{out,1}^2} = \int_0^\infty 4kT\left(\frac{2}{R_x}+\frac{R}{R_x^2}\right)\cdot\left|\frac{R_x}{1+\frac{s}{\omega_P Q_P}+\frac{s^2}{\omega_P^2}}\right|^2 df$$

$$= 4kT\left(2R_x+R\right)\frac{\omega_P Q_P}{4}$$

$$= \frac{kT}{C}\frac{2R_x+R}{R}$$

$$= \frac{kT}{C}\left(1+2\frac{R_x}{R}\right)$$

$$\overline{v_{out,2}^2} = \int_0^\infty 4kT\frac{Q_P^2R^2}{R_x}\cdot\left|\frac{\frac{s}{\omega_P}}{1+\frac{s}{\omega_P Q_P}+\frac{s^2}{\omega_P^2}}\right|^2 df$$

$$= 4kT\frac{Q_P^2}{R_x}\frac{\omega_P Q_P}{4}$$

$$= \frac{kT}{C}\frac{R}{R_x}Q_P^2$$

- For high Q_P, we definitely need to make $R << R_x$

Optimum

$$N = \left(1+2k\right)+Q_P^2\frac{1}{k} \qquad k = \frac{R_x}{R}$$

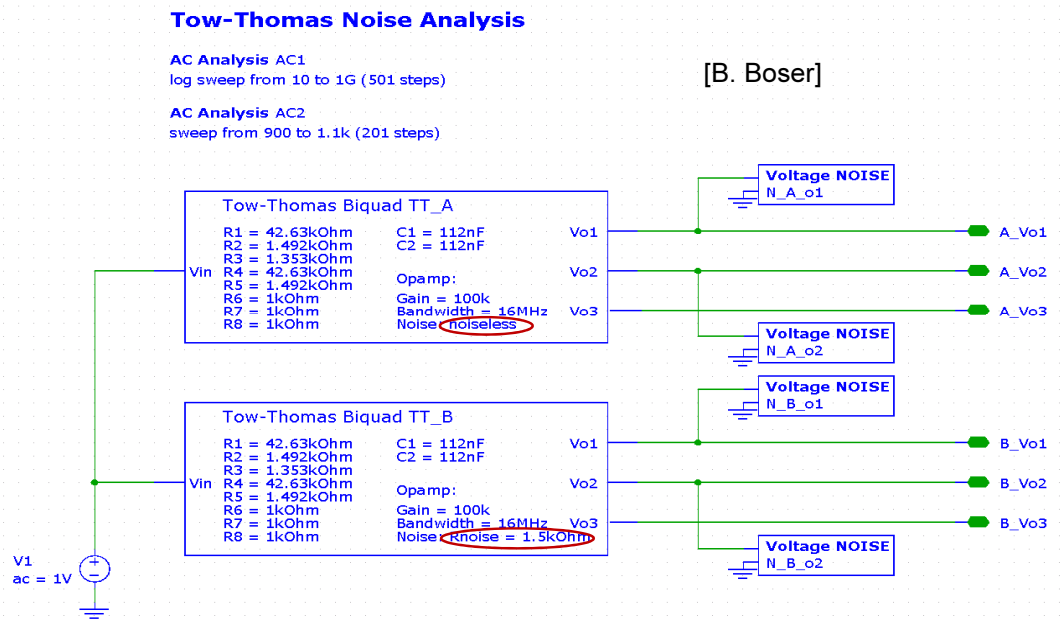
$$\frac{dN}{dk} = 2-Q_P^2\frac{1}{k^2} = 0$$

$$k_{opt} = \frac{Q_P}{\sqrt{2}}$$

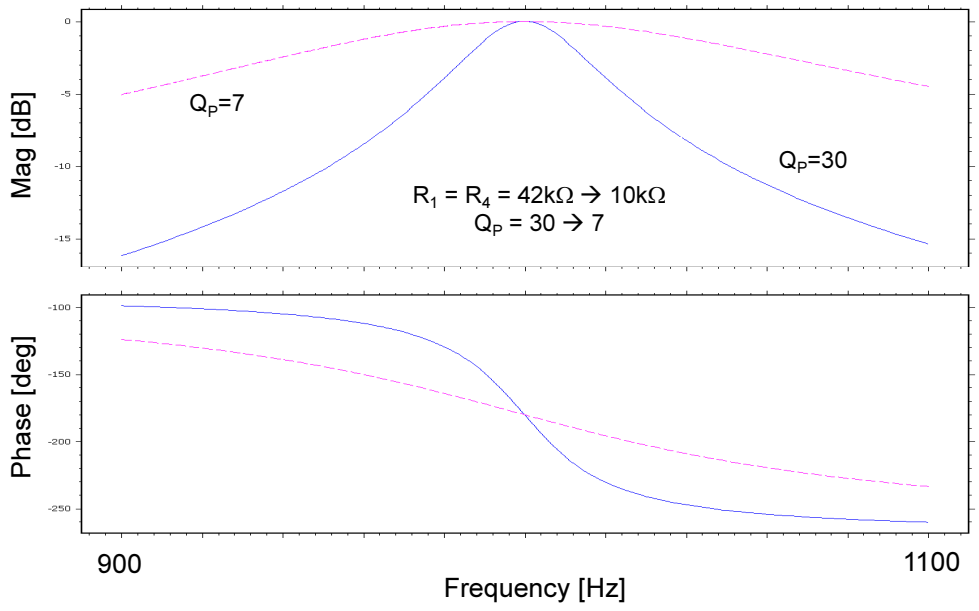
$$\overline{v_{out}^2} = \overline{v_{out,1}^2}+\overline{v_{out,1}^2} = \frac{kT}{C}\left(1+\left[\frac{2}{\sqrt{2}}+\sqrt{2}\right]Q_P\right) = \frac{kT}{C}\left(1+2\sqrt{2}Q_P\right)$$

- In a properly designed filter (and for large Q_P,) the noise will be roughly proportional to Q_P
- For a poorly designed filter, the noise can be proportional to Q_P^2

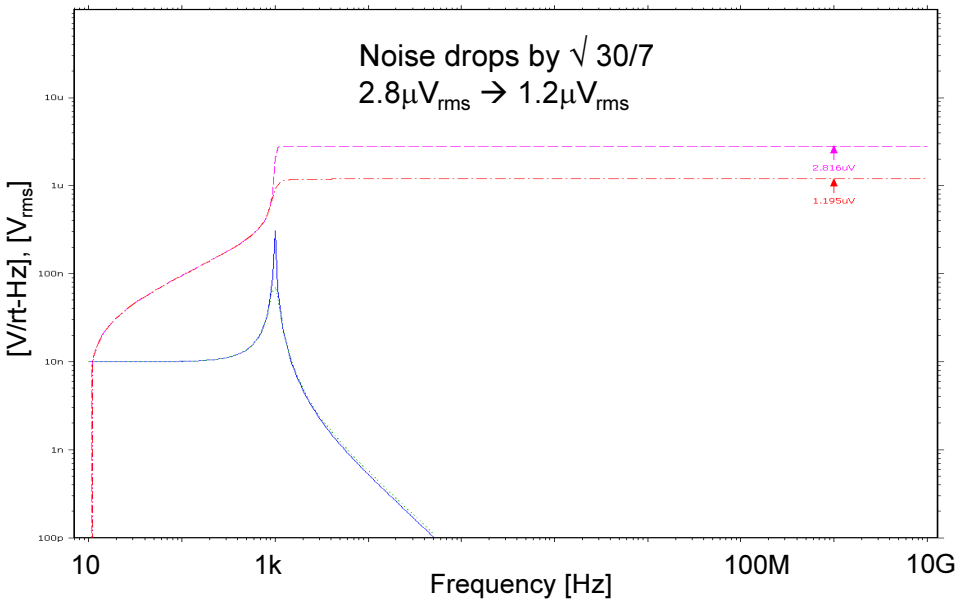
Tow-Thomas Noise Example



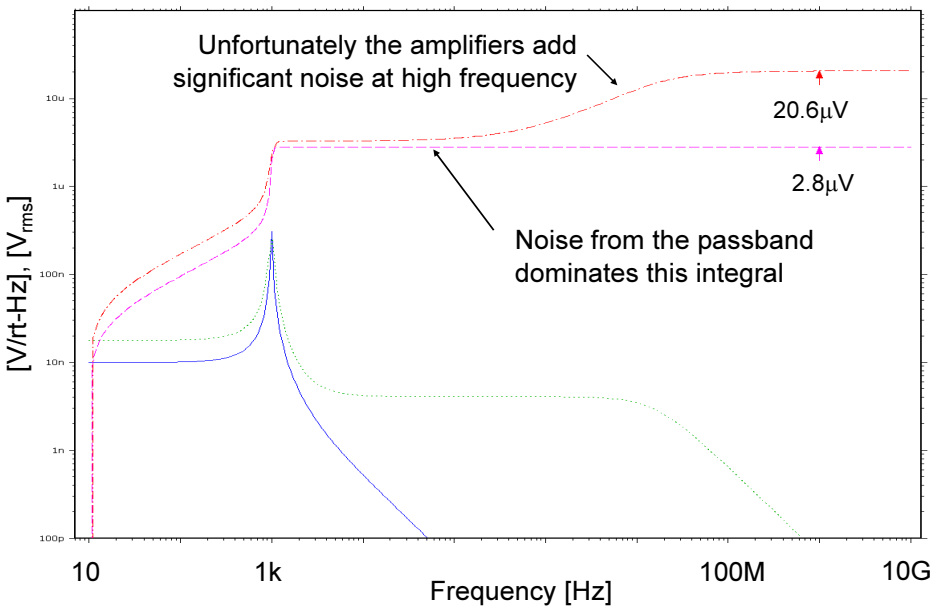
Frequency Response (BP Output)



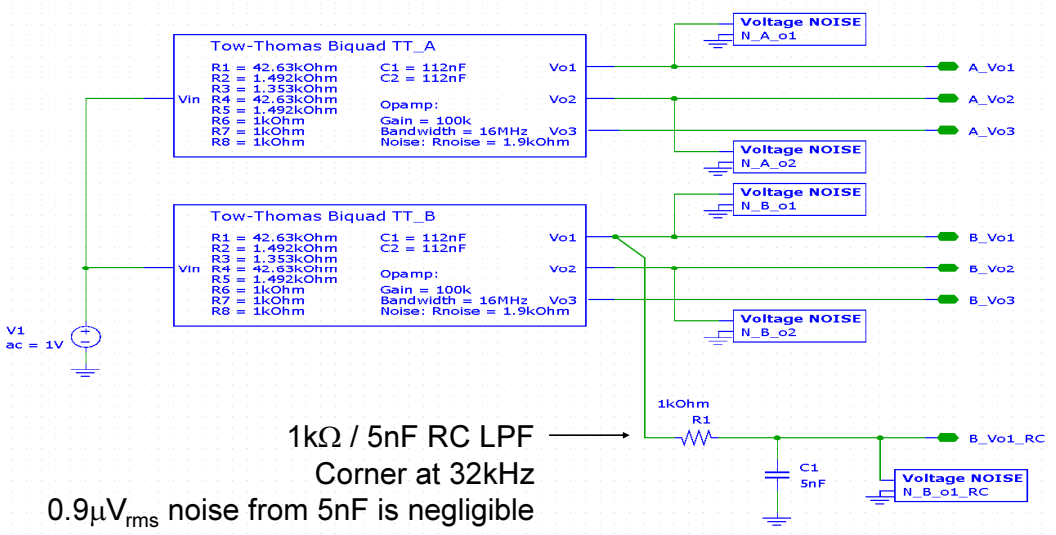
Noise versus Q_P (Noiseless Amplifier)



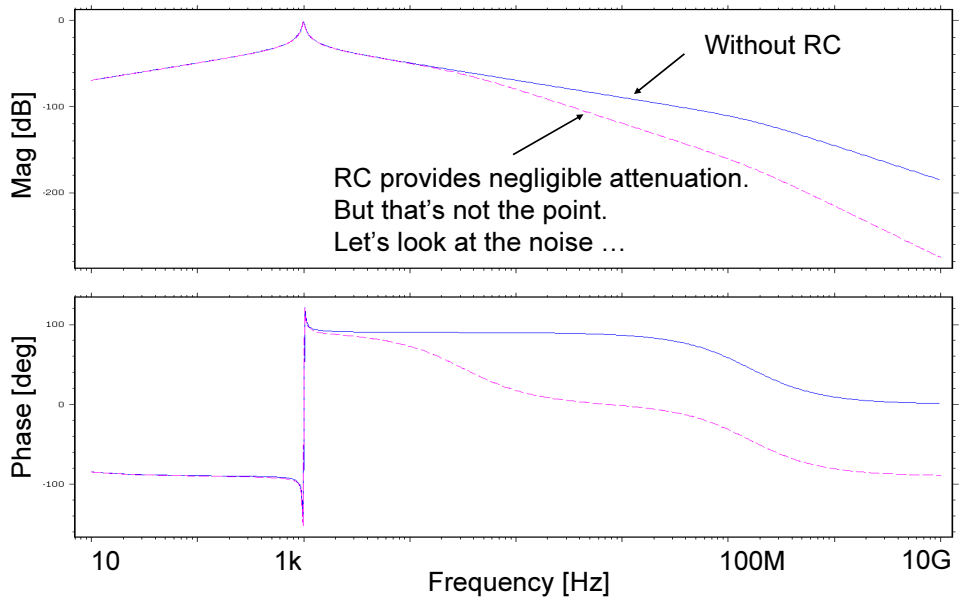
Noisy Amplifiers



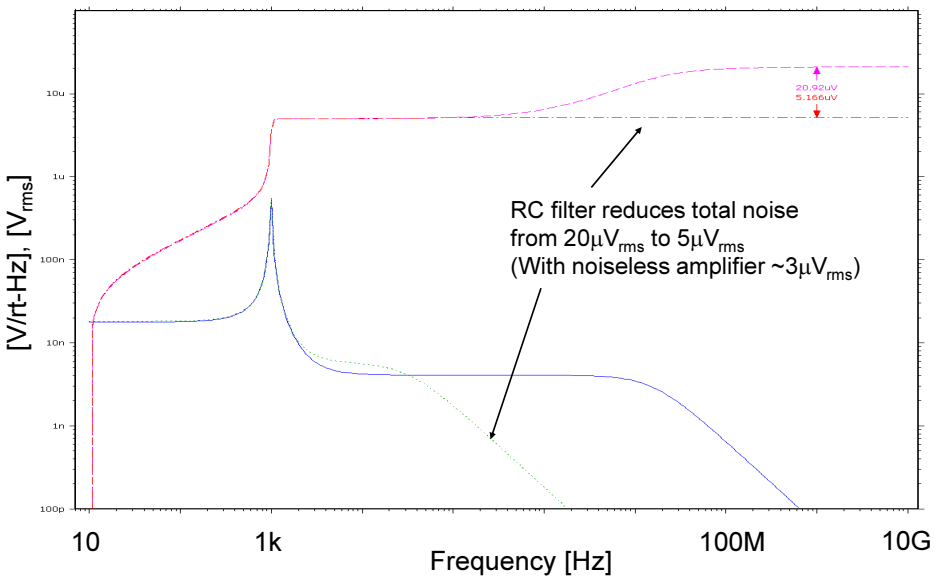
Adding an RC Filter



Frequency Response with RC Filter



Noise after RC Filter



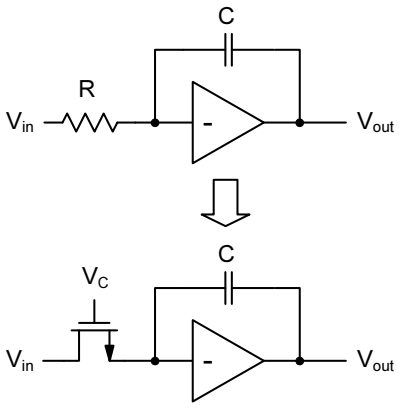
Summary

- The total integrated thermal noise of filter circuits is related to capacitor size
  - Usually a multiple of kT/C
- In filters, noise is proportional to the filter order, Q_P, and strongly dependent on the implementation
- Amplifiers can contribute significantly to (if not dominate the) overall filter noise
  - Minimizing the amplifier noise contribution costs power
    - Need small R_{noise}, i.e. large g_m (I_{BIAS})

Alternative Integrator Realizations

- Thus far, we have primarily employed active RC integrators in our filter implementations
- Next, we'll consider a number of alternative implementations that have found their use in practice
  - MOSFET-Opamp-C
  - G_m-OTA-C
  - G_m-C

MOSFET-C Integrator

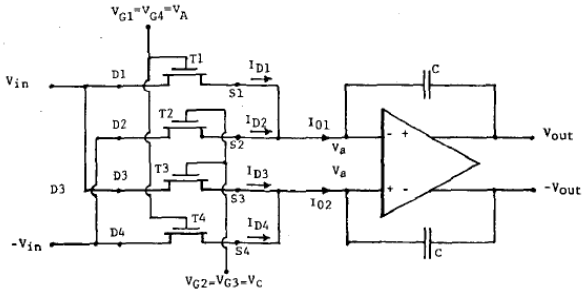


$$I_D = \mu C_{ox} \frac{W}{L}\left(V_{GS} - V_t - \frac{V_{DS}}{2}\right)V_{DS}$$

$$\frac{1}{R_{MOS}} = \frac{dI_D}{dV_{DS}} = \mu C_{ox} \frac{W}{L}\left(V_{GS} - V_t - V_{DS}\right)$$

- MOSFET in triode used to replace resistor
- Advantages
  - Continuous tuning mechanism for integrator time constant
  - Potentially cheaper fabrication process
- Disadvantages
  - Large parasitics, distributed RC along channel
  - Bias point sensitivity
  - Weakly nonlinear

Czarnul Circuit



Z. Czarnul, "Modification of Banu-Tsividis continuous-time integrator structure," *Circuits and Systems, IEEE Trans. Ckt. Syst.*, pp. 714-716, July 1986.

- Mitigates bias point sensitivity and removes second harmonic distortion
- Remaining issues
  - Backgate effect
  - Short channel effects

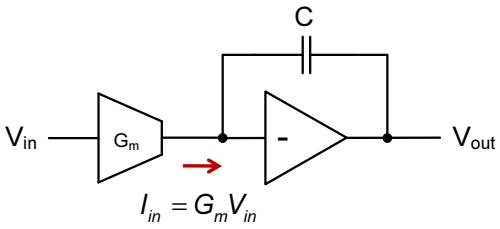
Assuming $V_a = 0$ (without loss of generality)

$$I_{O1} = I_{D1} + I_{D2} = \mu C_{ox} \frac{W}{L}\left([V_A - V_t]V_{in} - V_{in}^2 + [V_C - V_t](-V_{in}) - V_{in}^2\right)$$

$$I_{O2} = I_{D3} + I_{D4} = \mu C_{ox} \frac{W}{L}\left([V_C - V_t]V_{in} - V_{in}^2 + [V_A - V_t](-V_{in}) - V_{in}^2\right)$$

$$I_{O1} - I_{O2} = 2\mu C_{ox} \frac{W}{L}[V_A - V_C]V_{in}$$

G_m-Opamp-C Integrator



$$H(s) \cong -\frac{G_m}{sC}$$

$$R \leftrightarrow \frac{1}{G_m}$$

- Transconductor replaces resistor
  - Built e.g. using a differential pair
- Advantages
  - Main amplifier sees only capacitive loads
    - Can replace with "OTA"
  - Continuous tuning mechanism for integrator time constant
    - E.g. via I_{BIAS} of G_m cell
  - Potentially cheaper process
- Disadvantages
  - Nonlinearity of G_m cell
  - Extra power dissipation

Example (1)

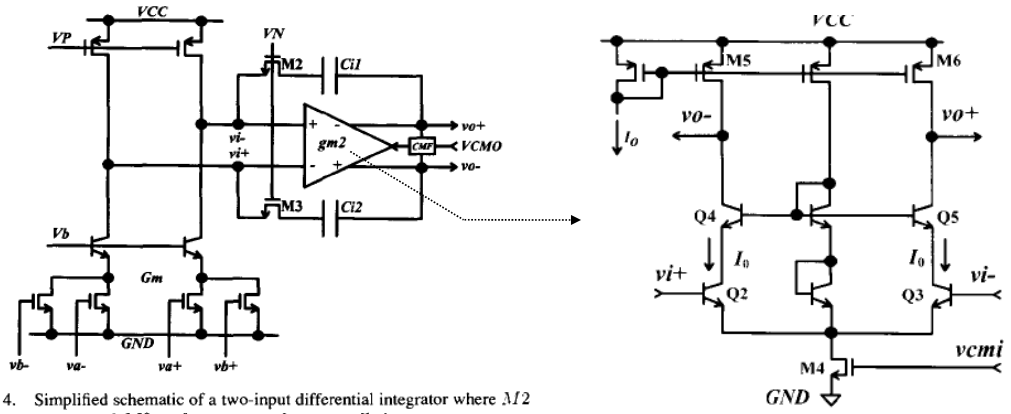


Fig. 4. Simplified schematic of a two-input differential integrator where $M2$ and $M3$ perform excess phase cancellation.

C.A. Laber, P.R. Gray, "A 20-MHz sixth-order BiCMOS parasitic-insensitive continuous-time filter and second-order equalizer optimized for disk-drive read channels ," *IEEE J. Solid-State Circuits,* vol. 28, no. 4, pp.462-470, Apr. 1993.

Example (2)

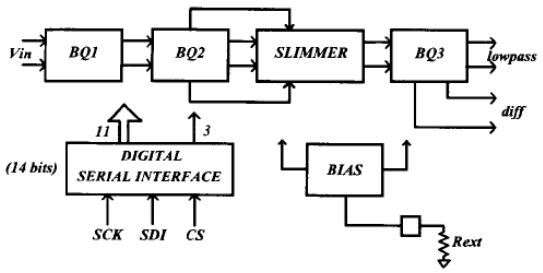


Fig. 9. Block diagram of the filter and equalizer chip. Both low-pass and differentiated outputs are required for pulse detection.

$$G_m = \frac{k_T \Delta i/2}{\Delta v/2} = \frac{k_T}{R_{ext}}.$$

$$\omega_0 = \frac{G_m}{C_i} = \frac{k_T}{R_{ext} C_i}.$$

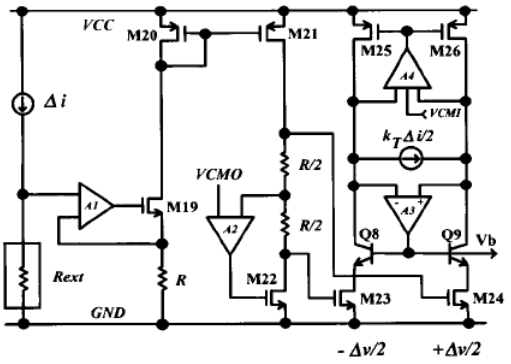
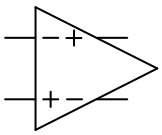


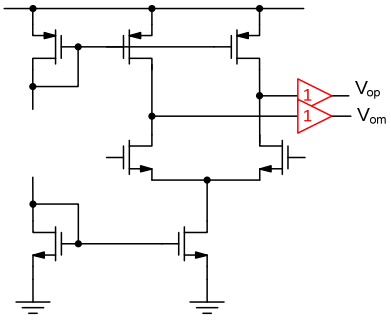
Fig. 8. Simplified schematic of the circuit used to set the bandwidth of the filter by setting the G_m of the transconductor by means of an external resistor. The output voltage V_b is used in Fig. 4 to set the value of G_m.

C.A. Laber, P.R. Gray, "A 20-MHz sixth-order BiCMOS parasitic-insensitive continuous-time filter and second-order equalizer optimized for disk-drive read channels ," *IEEE J. Solid-State Circuits,* vol. 28, no. 4, pp.462-470, Apr. 1993.

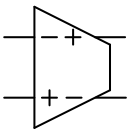
OpAmps versus OTAs (1)

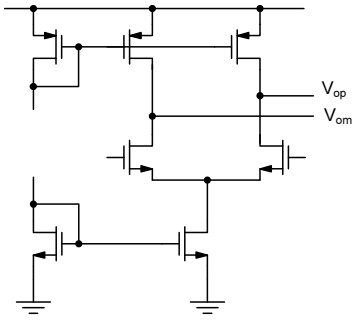
Operational Amplifier





Operational Transconductance Amplifier





OpAmps versus OTAs (2)

OTA

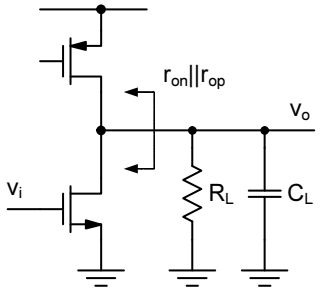
- Mostly used “on-chip”
- High output impedance
  - Ideally a voltage controlled current source
- Not well suited for resistive loads, mostly used to drive capacitive loads
- Usually lower (total integrated) noise

OpAmp

- "General Purpose"
- Low output impedance
  - Ideally a voltage controlled voltage source
- Can drive resistive and capacitive loads
- Essentially an OTA + buffer
  - Buffer increases complexity and power dissipation

Loading Considerations (1)

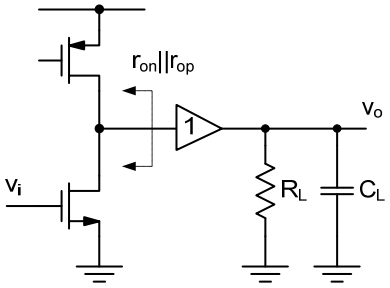
Single-ended OTA model



- Low load resistance will "destroy" the gain of our amplifier
  - R_L may be an explicit load or due to loading from the feedback network
- But, we want large (loop) gain for good precision

Loading Considerations (2)

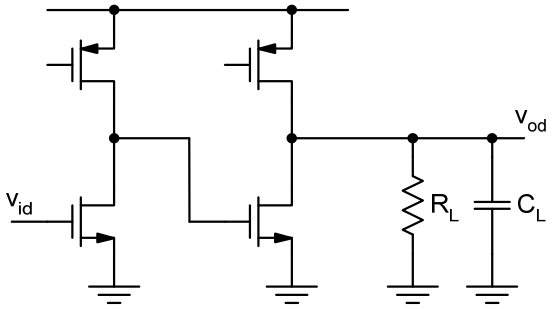
Single-ended OpAmp model



- Adding a buffer allows us to drive resistive loads and still achieve high gain
- But
  - Buffer can be difficult to build
  - Is costly in terms of headroom (e.g. source follower)
  - Adds additional area, power

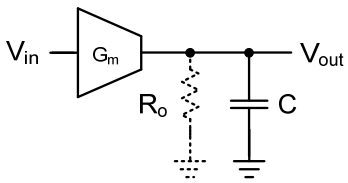
Loading Considerations (3)

Single-ended model of a two-stage OTA



- Resistive load "destroys" gain of second stage only
  - First stage sees capacitive load
- Costs additional area, power and must sacrifice stage 2 gain
- Can work acceptably well for moderate resistive loads
  - More later

G_m-C Integrator

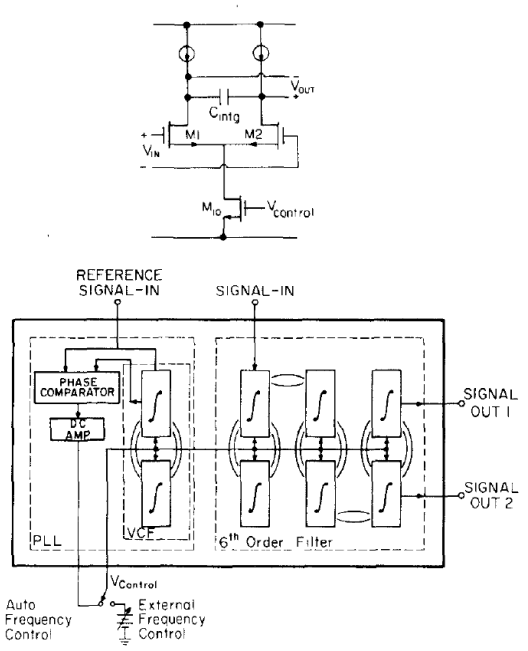


For $R_o \to \infty$

$$H(s) \cong \frac{G_m}{sC}$$

- Advantages
  - No OTA, no op-amp!
    - Lower power
    - Less phase shift!
  - Continuous tuning mechanism for integrator time constant
    - Via I_{BIAS} of G_m cell
- Disadvantages
  - Nonlinearity of G_m cell
  - Sensitive to finite output resistance (R_o)
  - Sensitive to parasitics

Original Paper



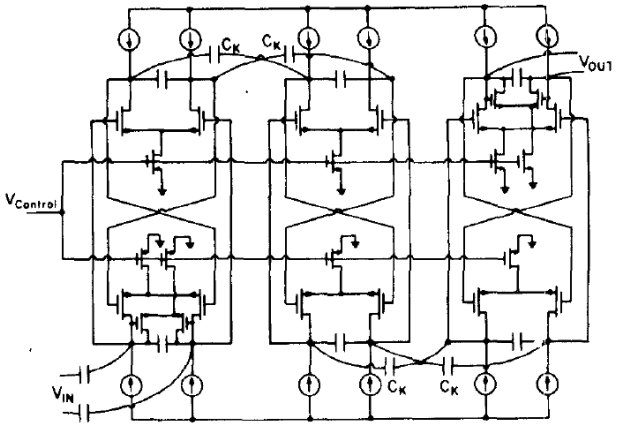
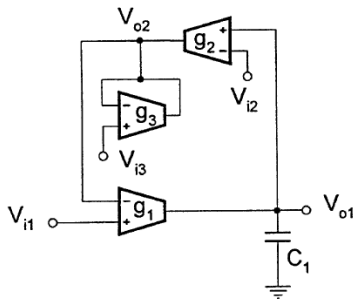


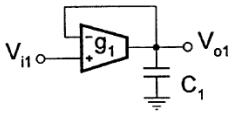
Fig. 10. Active implementation of the sixth-order ladder filter.

H. Khorramabadi and P. R. Gray, "High-frequency CMOS continuous-time filters," *IEEE J. Solid-State Circuits,* vol.19, no.6, pp. 939-948, Dec. 1984.

First-Order G_m-C Filters

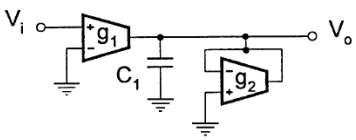


(a)

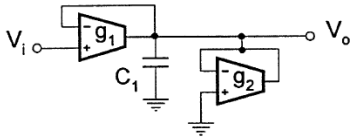


(b)

[Deliyannis, Section 9.2]

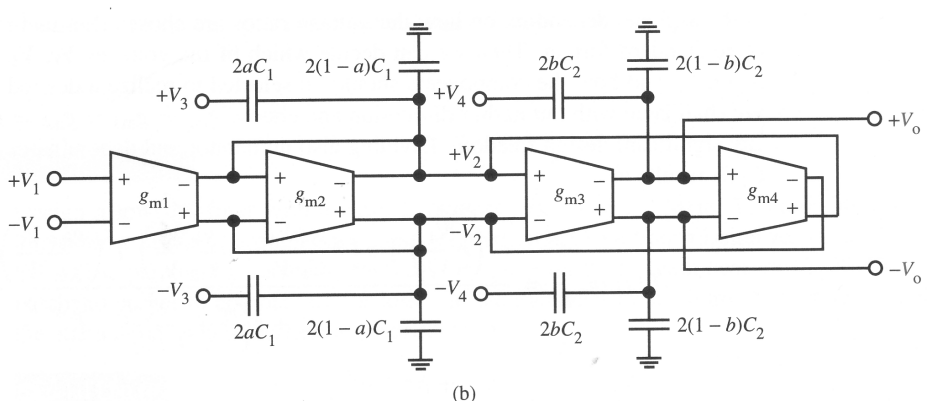


(c)



(d)

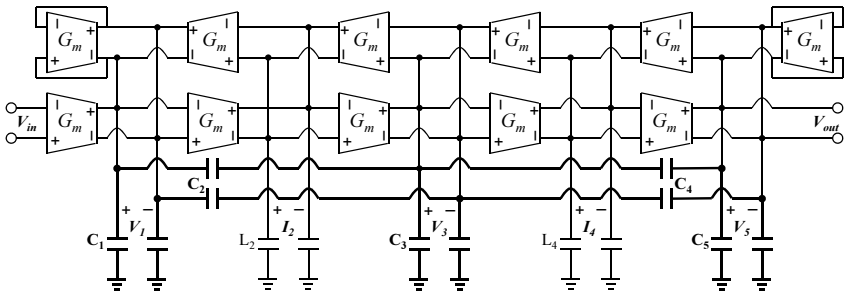
G_m-C Biquad



(b)

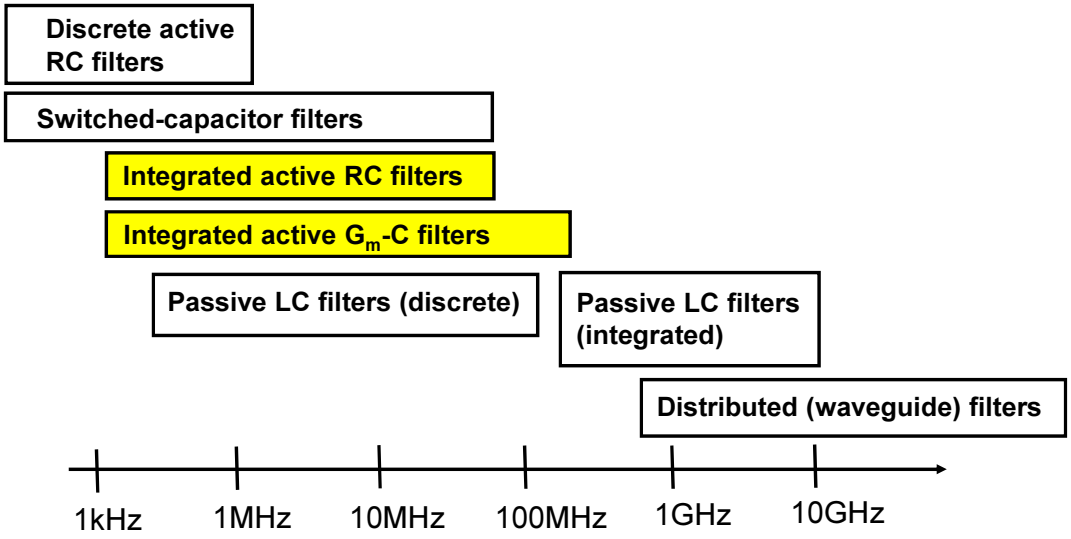
$$\frac{V_o}{V_i} = \frac{s^2 bC_1C_2\frac{V_4}{V_i} + s\left(bC_2 g_{m2}\frac{V_4}{V_i} - aC_1 g_{m3}\frac{V_3}{V_i}\right) + g_{m1}g_{m3}\frac{V_1}{V_i}}{s^2C_1C_2 + sC_2 g_{m2} + g_{m3}g_{m4}}$$

5th-Order G_m-C Ladder Filter



- Can show that capacitor network is unchanged from passive ladder prototype

Choosing an Implementation



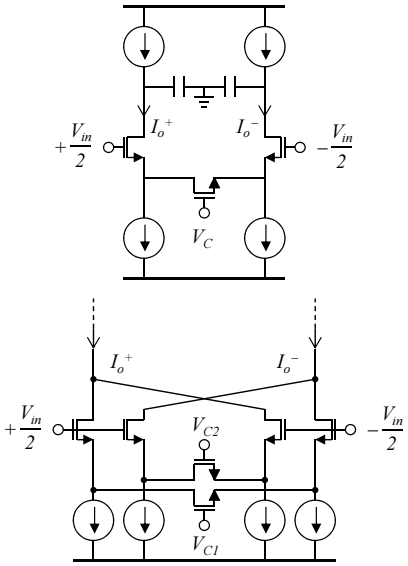
Active RC versus G_m-C

- RC filters (using op-amps)
  - Superior linearity
  - Dynamic range ~60-90 dB
  - Usable signal BW typically up to few tens of MHz
- G_m-C
  - Linearity limited
    - Usually have to use degeneration, etc.
  - Dynamic range ~40-70 dB
  - Distortion performance limited to ~60 dB level
  - Usable signal BW up to a few hundred MHz
- Both implementations typically require some form of tuning

Transconductor Implementation

- Hundreds of papers on "linearized" G_m cells
- Bottom line
  - Very hard to beat a basic differential pair with (or without) degeneration
- Let's look at a few ideas that have been proposed over the years…

Linearized G_m-Stage Using Triode Device



$$i_o = i_o^+ - i_o^- \cong \frac{1}{R_{MOSFET}} = \mu C_{OX}\frac{W}{L}\left((V_{GS}-V_{TH})V_{in} - \frac{1}{2}V_{in}^2\right)$$

Second-order nonlinear term is cancelled by a duplicate MOSFET with small V_{GS} control voltage:

$$i_o = \mu C_{OX}\frac{W}{L}\left((V_{GS1}-V_{TH})V_{in} - \frac{1}{2}V_{in}^2\right)$$

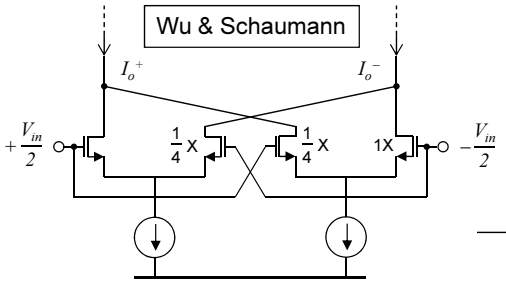
$$- \mu C_{OX}\frac{W}{L}\left((V_{GS2}-V_{TH})V_{in} - \frac{1}{2}V_{in}^2\right)$$

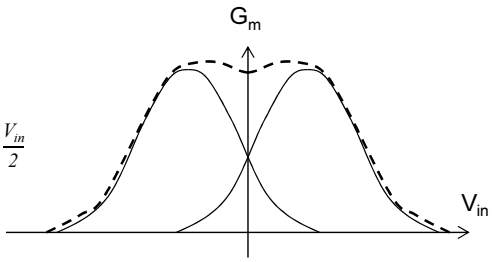
$$= \mu C_{OX}\frac{W}{L}\left(\underbrace{(V_{GS1}-V_{GS2})}V_{in}\right)$$

"$V_{GS1} > V_{GS2}$" because $V_{C1} > V_{C2}$

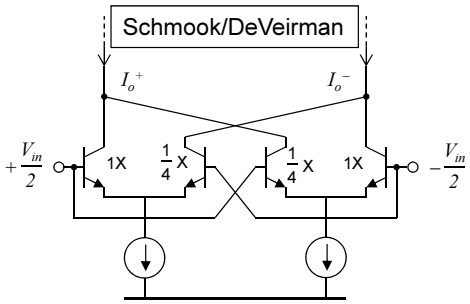
Z. Czarnul, Y. Tsividis, "MOS tunable transconductor," Electronics Letters, June 19, 1986, pp. 721-722.

Composite G_m-Stage to Increase Input Range



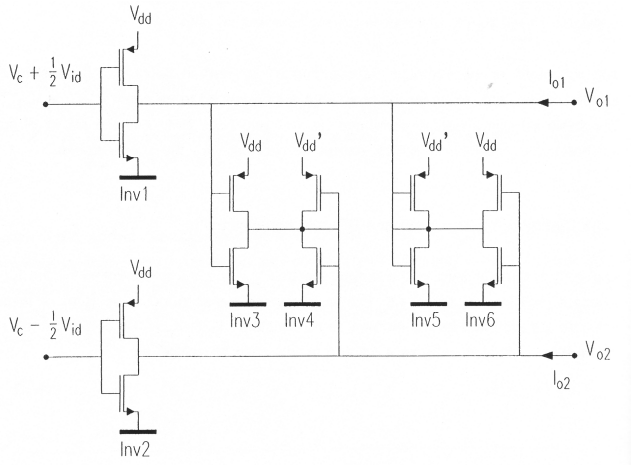


The net result is *increased input range*.
Linearity is unchanged.



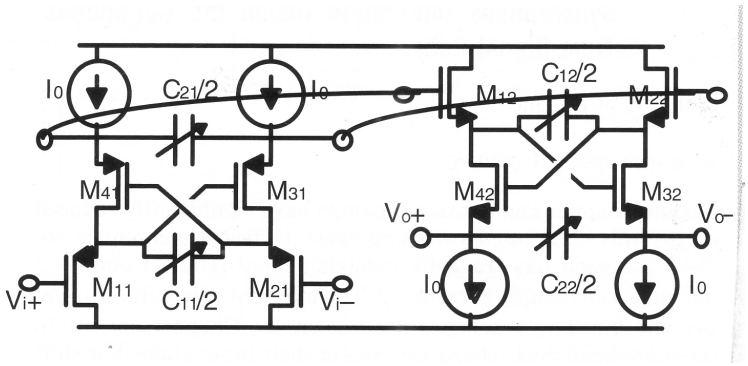
Bipolar implementation by Schmook (1975) and later modified/improved version by DeVeirman (1992).

Nauta Cell



B. Nauta, "A CMOS Transconductance-C Filter Technique for Very High Frequencies", IEEE J. Solid-State Circuits, Feb. 1992.

Source-Follower Based Filter



S. D'Amico et al., "A 4.1mW 79dB-DR 4th order Source-Follower-Based Continuous-Time Filter for WLAN Receivers", IEEE J. Solid-State Circuits, Dec. 2006.

Parameter Tuning

- Various objectives
  - Tune out circuit nonidealities such as phase lead/lag
  - Absorb global process variations
    - G_m, R, C
  - Vary filter bandwidth
  - Vary other filter parameters
    - E.g. "boost" in disk drive filters

Q-Tuning

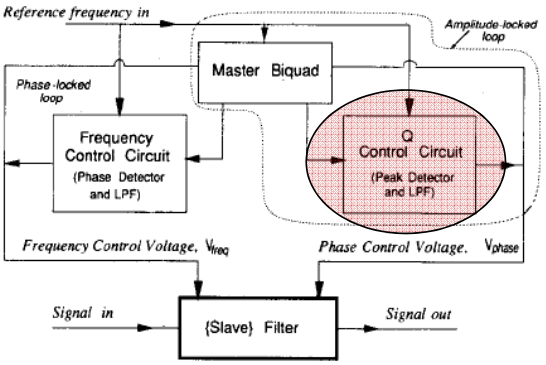


Fig. 1. Master–slave tuning scheme.

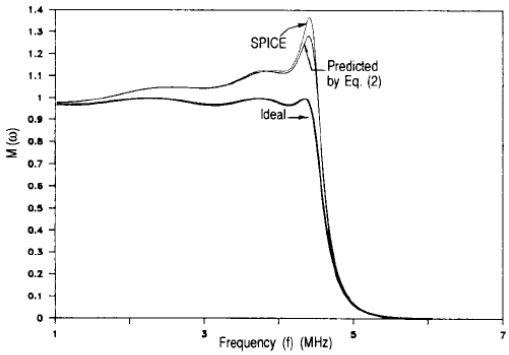
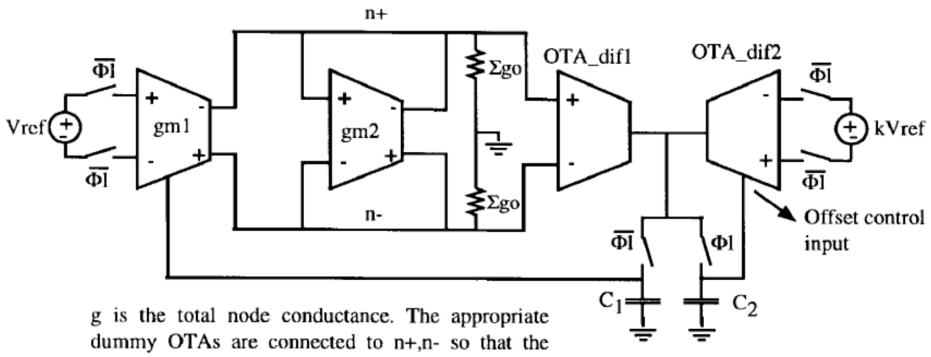


Fig. 2. Prediction of filter response with integrator nonidealities.

V. Gopinathan et al., "Design Considerations for High-Frequency Continuous-Time Filters and Implementation of an Anti-aliasing Filter for Digital Video," IEEE JSSC, Vol. 25, No. 6, Dec. 1990.

Finite g_o (R_o) Tuning



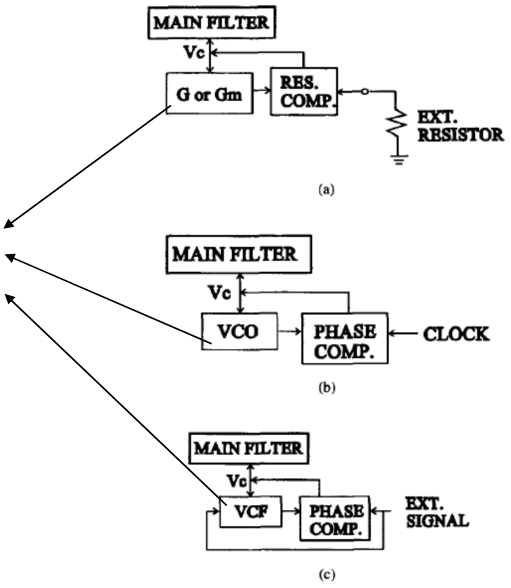
g is the total node conductance. The appropriate dummy OTAs are connected to n+,n- so that the node conductance is the same as in the biquad

$g = gm2 + \Sigma go$

Dehaene et al., "A 50-MHz Standard CMOS Pulse Equalizer for Hard Disk Read Channels," IEEE J. Solid-State Circuits, July1997.

Tuning of the Filter Time Constants

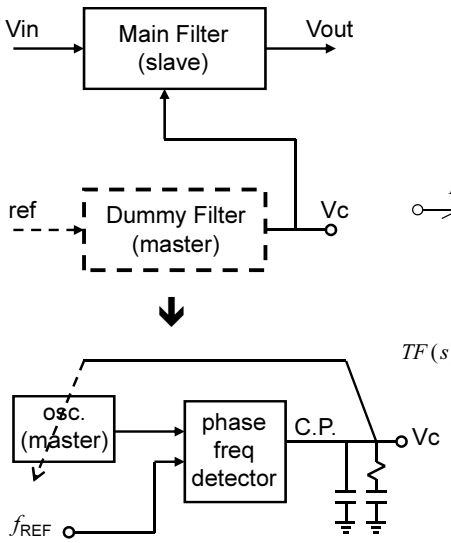
Built using same RC or G_m–C cell used in main filter

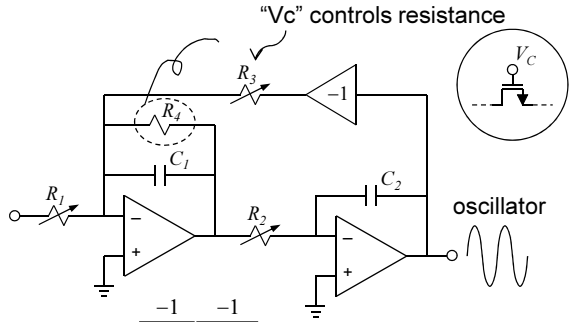


- Lock R ($1/G_m$) or frequency (G_m/C, $1/RC$) in a replica to a reference
- Slave replica's control voltage into main filter circuit

Y.P. Tsividis, "Integrated continuous-time filter design - an overview," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 3, pp.166-176, March 1994.

VCO Tuning Example





$$TF(s) = \frac{\frac{-1}{sR_1C_1}\frac{-1}{sR_2C_2}}{1+\frac{1}{sR_4C_1}+\frac{1}{sR_3C_1}\frac{1}{sR_2C_2}} = \frac{G_1G_2}{s^2C_1C_2+sC_2G_4+G_2G_3}$$

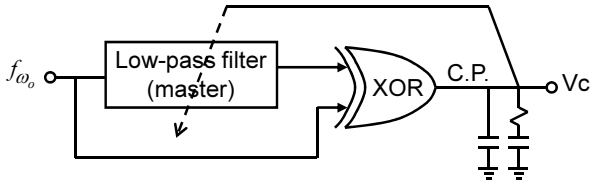
Without R_4 ➔ $D(s) = s^2C_1C_2 + G_2G_3 \equiv 0$

poles at $\pm j\sqrt{\frac{G_2G_3}{C_1C_2}}$ Banu (1985)

VCF Tuning Approach

- Use of a low-pass filter, instead of an oscillator, as the reference for tuning
- Two phases into XOR gate is offset by 90° when phase-locked

$$LP(s) = \frac{K\omega_o^2}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2}$$

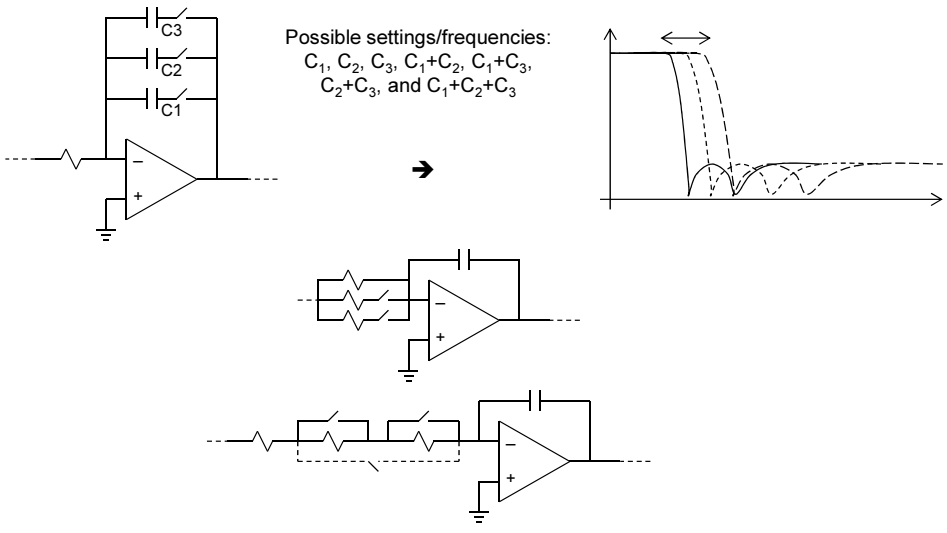


$$\angle LP(s)\big|_{s=j\omega_o} = \angle \frac{1}{-\omega_o^2 + j\frac{\omega_o^2}{Q} + \omega_o^2} = -90^\circ$$

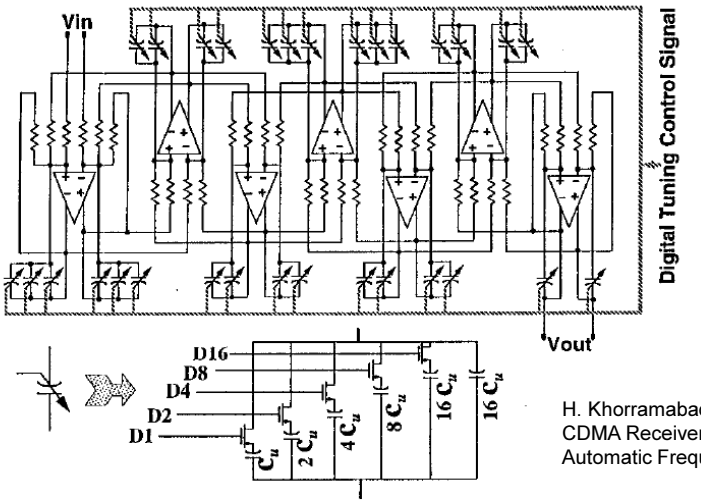
V. Gopinathan et al., "Design Considerations for High-Frequency Continuous-Time Filters and Implementation of an Anti-aliasing Filter for Digital Video," IEEE JSSC, Vol. 25, No. 6, Dec. 1990.

Discrete Frequency Programming/Tuning

- Switch in/out capacitors or resistors to control corner frequencies.



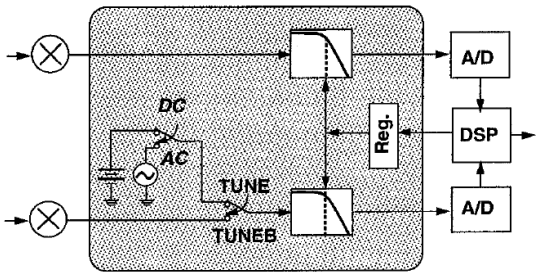
Example (1)



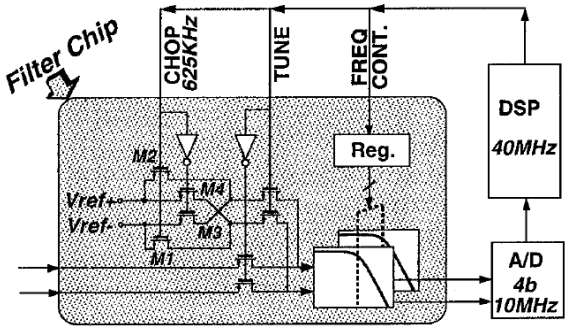
H. Khorramabadi, "Baseband Filters for 6-95 CDMA Receiver Applications Featuring Digital Automatic Frequency Tuning," ISSCC 1996.

Figure 1: Seventh-order active RC low-pass filter with digitally-controlled variable capacitors.

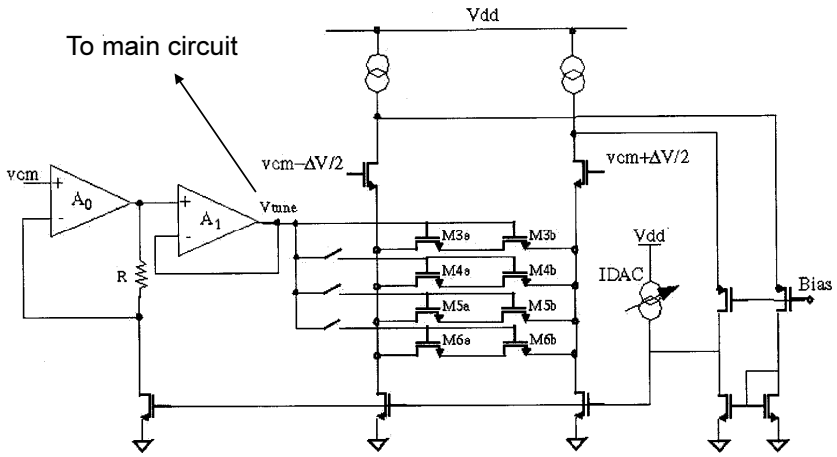
Example (2)



H. Khorramabadi, "Baseband Filters for 6-95 CDMA Receiver Applications Featuring Digital Automatic Frequency Tuning," ISSCC 1996.



Tuning G_m Over a Wide Range



G. Bollati et al., "An Eighth-Order CMOS Low-Pass Filter with 30–120 MHz Tuning Range and Programmable Boost," IEEE J. Solid-State Circuits, July 2001.

Reference Papers (1)

- **Y. Tsividis, "Integrated continuous-time filter design—an overview," IEEE J. Solid-State Circuits, pp. 15-30, Mar. 1994.**
- Y. Tsividis, M. Banu, and J. Khoury, "Continuous-Time MOSFET-C Filters in VLSI", IEEE J. Solid State Circuits, Feb. 1986, pp. 15-30; and IEEE Trans. Circuits and Systems, Feb. 1986, pp. 125-140.
- Z. Czarnul, "Modification of the Banu-Tsividis Continuous-Time Integrator Structure," IEEE Transactions on Circuits and Systems, Vol. CAS-33, No. 7, pp. 714-716, July 1986.
- U.-K. Moon, and B.-S. Song, "Design of a Low-Distortion 22-kHz Fifth Order Bessel Filter," IEEE Journal of Solid State Circuits, Vol. 28, No. 12, pp. 1254-1264, Dec.1993.
- H. Khorramabadi and P.R. Gray, "High Frequency CMOS continuous-time filters," IEEE Journal of Solid-State Circuits, pp.939-948, Dec. 1984.
- K.S. Tan and P.R. Gray, "Fully integrated analog filters using bipolar FET technology," IEEE, J. Solid-State Circuits, pp. 814-821, December 1978.
- J. Schmook, "An input stage transconductance reduction technique for high-slew rate operational amplifiers," IEEE J. Solid-State Circuits, pp. 407-411, Dec. 1975.

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- A. Durham, J. Hughes, and W. Redman- White, “Circuit Architectures for High Linearity Monolithic Continuous-Time Filtering,” IEEE TCAS, pp. 651-657, Sept. 1992.
- C. Laber and Gray, “A 20MHz 6th Order BiCOM Parasitic Insensitive Continuous Time Filter and Second Order Equalizer Optimized for Disk Drive Read Channels,” IEEE J. of Solid State Circuits, Vol. 28, pp. 462-470, April 1993.
- H. Khorramabadi et al., “Baseband Filters for IS-95 CDMA Receiver Applications Featuring Digital Automatic Frequency Tuning,” ISSCC 1996, pp. 172-173.
- R. Castello, I. Bietti and F. Svelto, "High-Frequency Analog Filters in Deep-Submicron CMOS Technology," ISSCC Digest of Technical Papers, Feb. 1999, pp.74-75.
- Y. Tsividis, Z. Czarnul and S.C. Fang, “MOS transconductors and integrators with high linearity,” Electronics Letters, vol. 22, pp. 245-246, Feb. 27, 1986.
- I. Mehr and D.R. Welland, “A CMOS Continuous-Time Gm-C Filter for PRML Read Channel Applications at 150 Mb/s and Beyond”, IEEE J. of Solid-State Circuits, Vol.32, No.4, April 1997, pp. 499-513.
- R. Alini, A. Baschirotto, and R. Castello, “Tunable BiCMOS Continuous-Time Filter for High-Frequency Applications,” IEEE Journal of Solid State Circuits, Vol. 27, No. 12, pp. 1905-1915, Dec. 1992.

Reference Papers (3)

- J. Khoury, “Design of a 15-MHz CMOS Continuous-Time Filter with On-Chip Tuning”, IEEE J. Solid-State Circuits, Dec. 1991.
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- G. DeVeirman and R. Yamasaki, “Design of a bipolar 10-MHz continuous-time 0.05deg equiripple linear phase filter,” IEEE J. Solid-State Circuits, pp. 324-331, Mar. 1992.
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Reference Papers (4)

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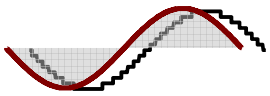
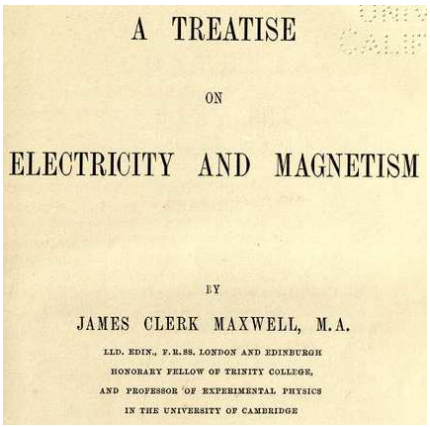
Switched Capacitor Filters



Boris Murmann
Stanford University
murmann@stanford.edu

History: 1873

- Maxwell recognized that a switched capacitor behaves like a resistor in terms of average current
  - James C. Maxwell, *A treatise on electricity and magnetism.* Oxford: Clarendon Press, 1873, vol. 2, pp. 374-375
    - http://www.archive.org/stream/electricandmag02maxwrich#page/n405/mode/2up



A TREATISE

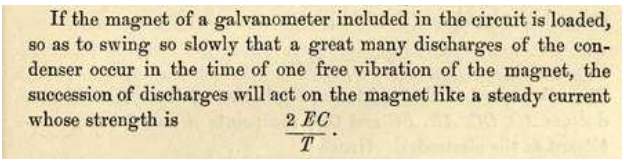
ON

ELECTRICITY AND MAGNETISM

BY

JAMES CLERK MAXWELL, M.A.

LL.D. EDIN., F.R.SS. LONDON AND EDINBURGH
HONORARY FELLOW OF TRINITY COLLEGE,
AND PROFESSOR OF EXPERIMENTAL PHYSICS
IN THE UNIVERSITY OF CAMBRIDGE



If the magnet of a galvanometer included in the circuit is loaded, so as to swing so slowly that a great many discharges of the condenser occur in the time of one free vibration of the magnet, the succession of discharges will act on the magnet like a steady current whose strength is $\frac{2EC}{T}$.

History: 1968

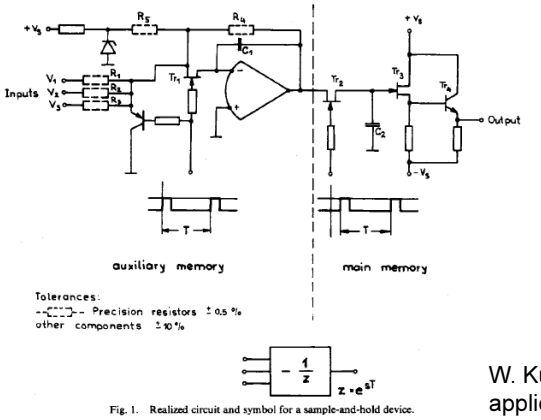


Fig. 1. Realized circuit and symbol for a sample-and-hold device.

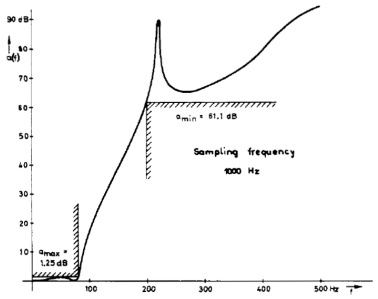


Fig. 4. Measured attenuation response of the digital Cauer low-pass.

W. Kuntz, "A new sample-and-hold device and its application to the realization of digital filters," *Proc. IEEE* , vol.56, no.11, pp. 2092- 2093, Nov. 1968.

An important application of these sample-and-hold devices is the realization of digital filters in the real-time domain. All presently known methods use digital computers, but these are too slow and too expensive for some applications.

History: 1972

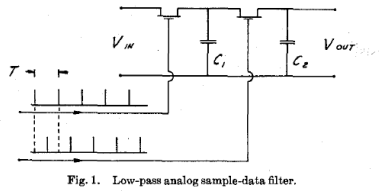


Fig. 1. Low-pass analog sample-data filter.

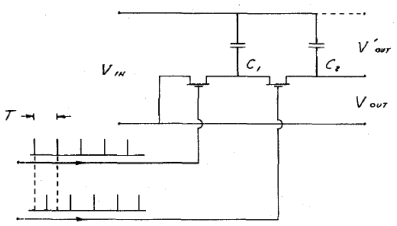


Fig. 2. High-pass analog sample-data filter.

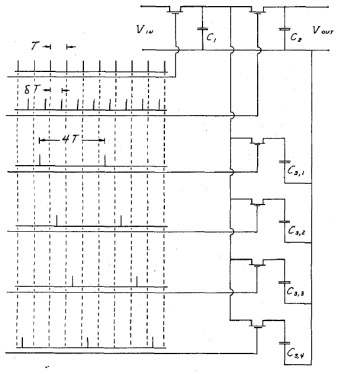
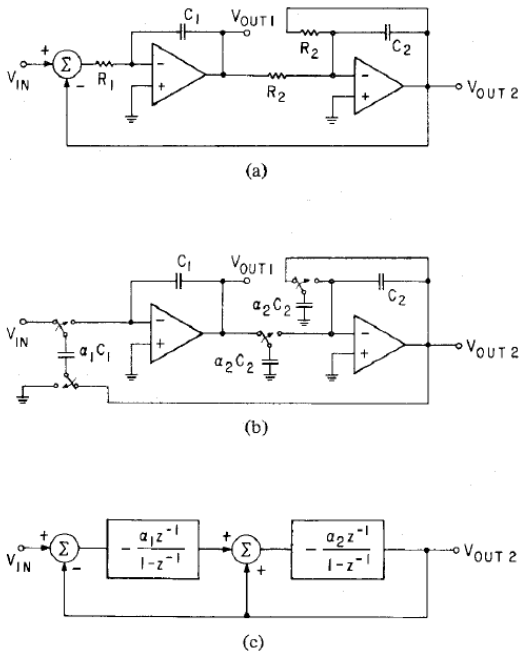


Fig. 3. High-Q bandpass analog sample-data filter/fixed Q.

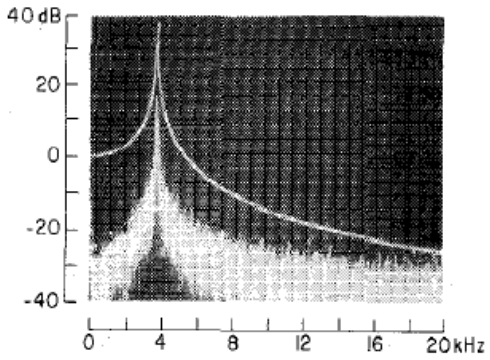
D.L. Fried, "Analog sample-data filters," IEEE J. Solid-State Circuits, vol.7, no.4, pp. 302- 304, Aug. 1972.

We would like to call attention to what we believe is a rather interesting and previously unrecognized filter-design concept.

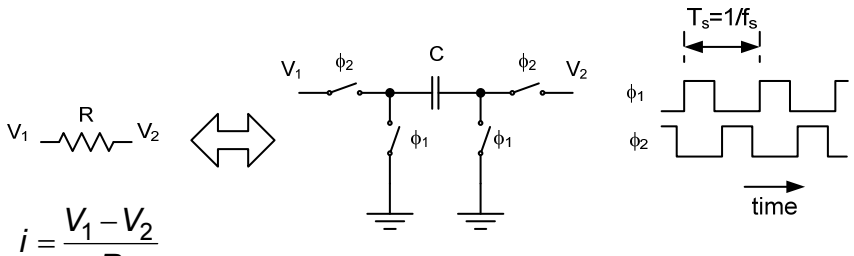
History: 1977



B. J. Hosticka, R. W. Brodersen, and P. R. Gray, "MOS sampled data recursive filters using switched capacitor integrators," IEEE Journal of Solid-State Circuits, vol. 12, no. 6, pp. 600-608, Dec. 1977.



Emulating a Resistor



$$i = \frac{V_1 - V_2}{R}$$

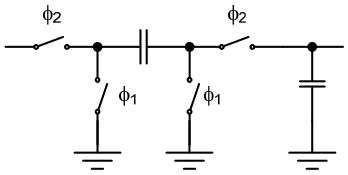
$$\Delta q = C(V_1 - V_2)$$

$$i_{avg} = \frac{\Delta q}{\Delta t} = \frac{\Delta q}{T_s} = f_s \cdot C(V_1 - V_2)$$

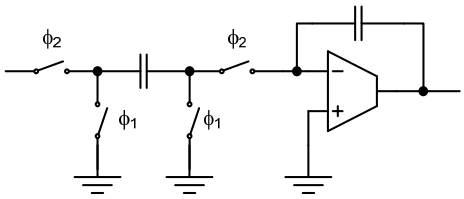
$$R_{avg} = \frac{1}{f_s \cdot C}$$

(Note: current flows in "bursts")

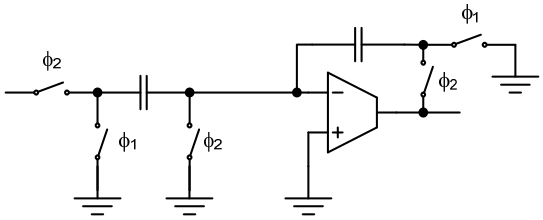
Switched Capacitor Circuits



SC low-pass filter (passive)



SC integrator



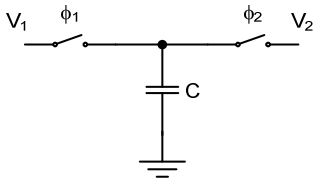
SC gain stage

(Actual implementations are differential)

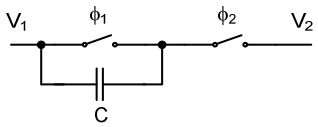
Discussion

- One of the most significant inventions in the history of ICs
- Predominant approach for precision signal processing in CMOS
  - CMOS technology provides good switches & capacitors
- SC circuits have many advantages over RC implementations
  - Transfer function set by **ratio** of capacitors
    - RC product suffers from large process variations
  - Corner frequencies (of filters) can be adjusted by changing clock frequency
  - Can make large time constants without using large resistors
    - RC lowpass, 100Hz: R=16MΩ, C=100pF
    - SC lowpass, 100Hz: f=10kHz, C_1=6.25pF, C_2=100pF
- Reference
  - R. Gregorian et al., "Switched-Capacitor Circuit Design," Proceedings of the IEEE, Vol. 71, No. 8, August 1983.

"Parasitic Sensitive" Configurations



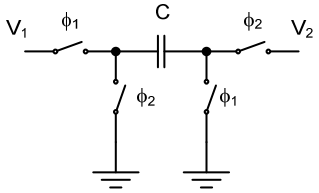
$$R_{avg} = \frac{1}{f_s \cdot C}$$



$$R_{avg} = \frac{1}{f_s \cdot C}$$

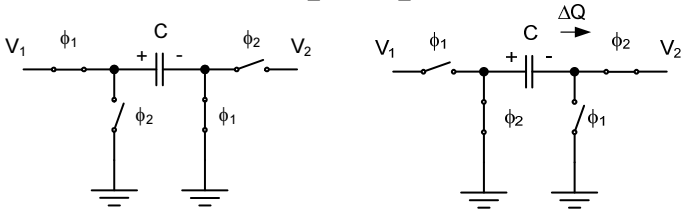
- R_{avg} is affected by parasitic capacitances (e.g. wire capacitance, junction capacitance, etc.)

Inverting Configuration



During ϕ1:

$q_1 = CV_1$



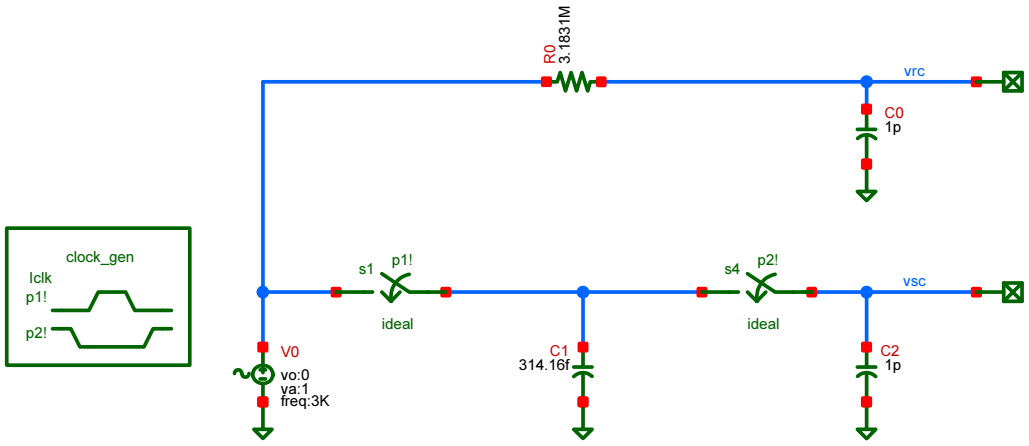
During ϕ2:

$q_2 = -CV_2$

$$\Delta q = -CV_2 - CV_1 = C(-V_1 - V_2) \qquad i_{avg} = f_s C(-V_1 - V_2)$$

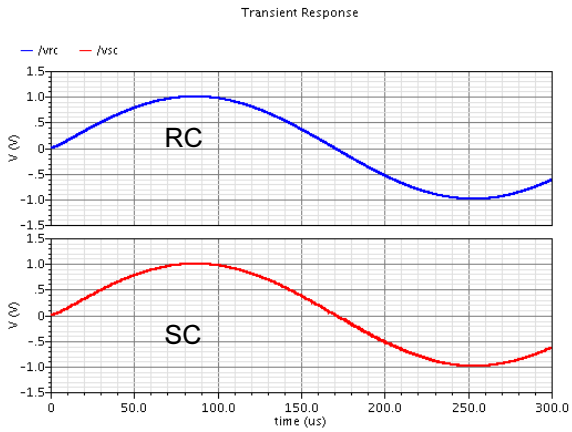
- Compared to the circuit on slide 3, the effect of V_1 is "inverted" because C is flipped upside down during ϕ2 (+ terminal at GND)
  - Provides signal inversion

RC and SC Filter Transient Analysis (1)

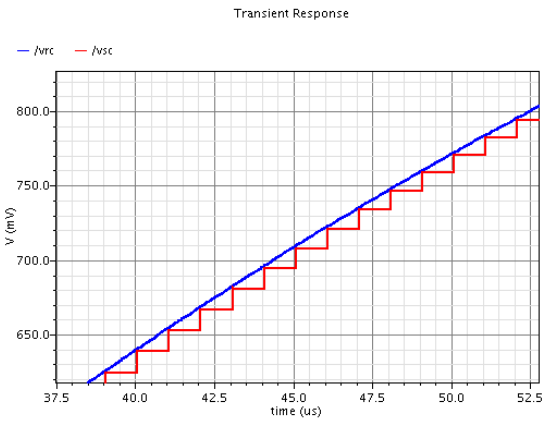


f_s = 1MHz, f_c = 50kHz, f_{in}=3kHz

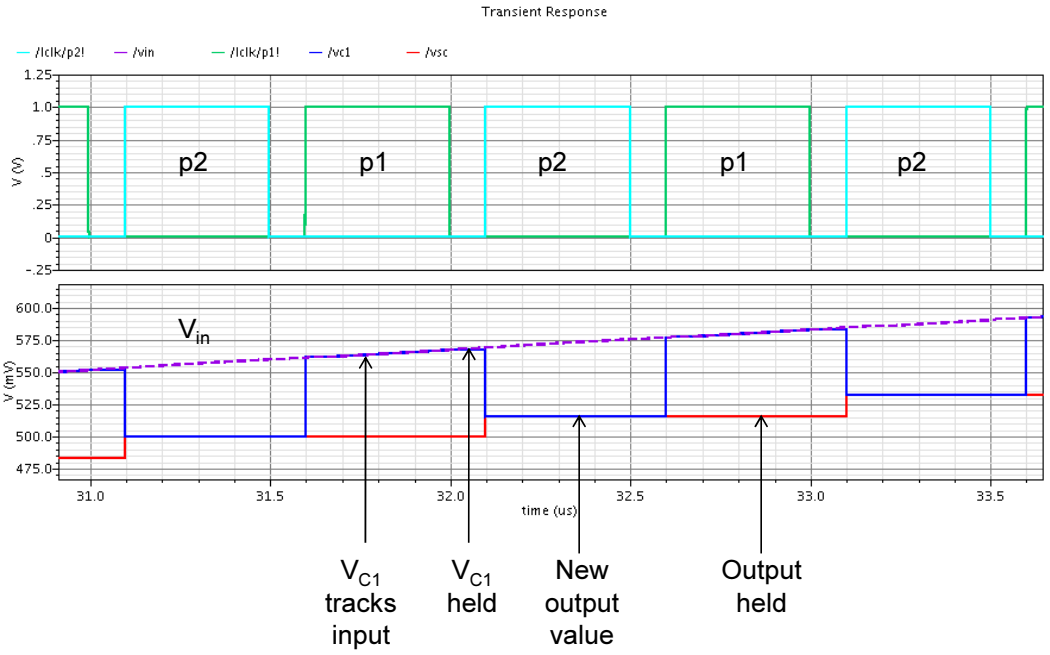
RC and SC Filter Transient Analysis (2)



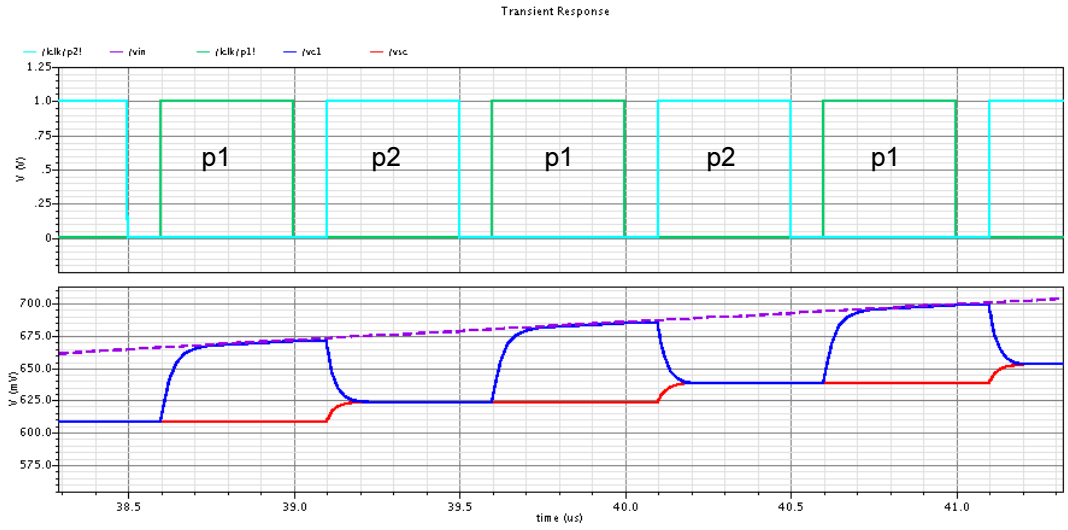
- SC output is a "staircase approximation" of the RC filtered signal
  - Slightly delayed



Waveform Details



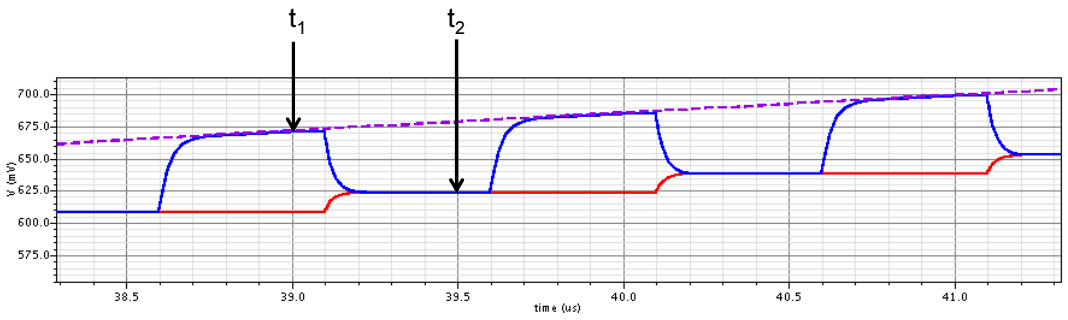
Waveforms with Larger R_{on} (1Ω → 100kΩ)



Frequency Response ?

- Looking at the transient waveforms is fun, but what can we say about the frequency response of the SC circuit?
- Looks like a tough question since the output signal looks "complicated"
  - Not just a sine wave with shifted phase and altered magnitude, as in the RC case
  - Instead we have a staircase waveform with "rounded" edges (due to finite switch resistance)
- Part of the problem is that SC circuits are time variant
  - The configuration is periodically switched between two states
- Time variant circuits, in principle, introduce new frequencies
  - Think about spectral components caused by the voltage "steps" at the output

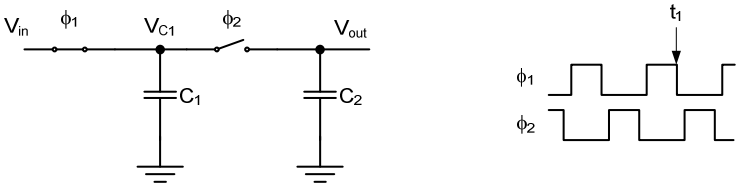
First Pass Analysis



- Let's try to find the relationship between $V_{in}(t_1)$ and $V_{out}(t_2)$
  - This means we are looking at the relationship between "discrete time samples" of the voltages and ignore the fact that the output is really a continuous time signal

Circuit Analysis (1)

- During $\phi 1$, V_{C1} tracks V_{in}



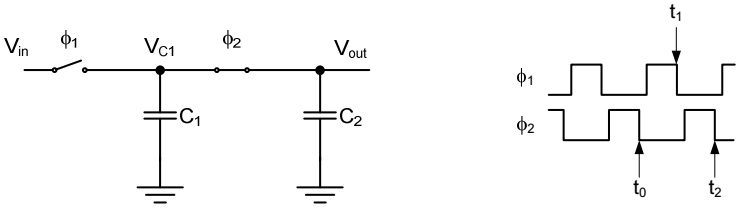
- If we assume that the tracking is reasonably fast, such that there is only a negligible difference between the input and V_{C1}, we can write

$$V_{C1}(t_1) = V_{in}(t_1)$$

$$Q_{C1}(t_1) = C_1 V_{in}(t_1)$$

Circuit Analysis (2)

- During $\phi 2$, the output voltage and V_{C1} are equalized



- Again, assuming that the circuit settles precisely, we can write

$$V_{C1}(t_2) = V_{out}(t_2) \qquad Q_{C1}(t_2) + Q_{C2}(t_2) = (C_1 + C_2)V_{out}(t_2)$$

- The sum of the charges must be equal to the charges that were previously on C_1 and C_2, before the $\phi 2$ switch turned on, i.e.

$$Q_{C1}(t_2) + Q_{C2}(t_2) = Q_{C1}(t_1) + Q_{C2}(t_0)$$

Circuit Analysis (3)

$$Q_{C1}(t_2) + Q_{C2}(t_2) = Q_{C1}(t_1) + Q_{C2}(t_0)$$

$$(C_1 + C_2)V_{out}(t_2) = C_1 V_{in}(t_1) + C_2 V_{out}(t_0)$$

$$V_{out}(t_2) = \frac{C_1}{C_1 + C_2} V_{in}(t_1) + \frac{C_2}{C_1 + C_2} V_{out}(t_0)$$

$$V_{out}(t_2) = \frac{C_1}{C_1 + C_2} V_{in}\left(t_2 - \frac{T_s}{2}\right) + \frac{C_2}{C_1 + C_2} V_{out}\left(t_2 - T_s\right)$$

- Laplace Transform

$$V(t) \rightarrow V(s)$$

$$V(t - \Delta t) \rightarrow V(s)e^{-s\Delta t}$$

Circuit Analysis (4)

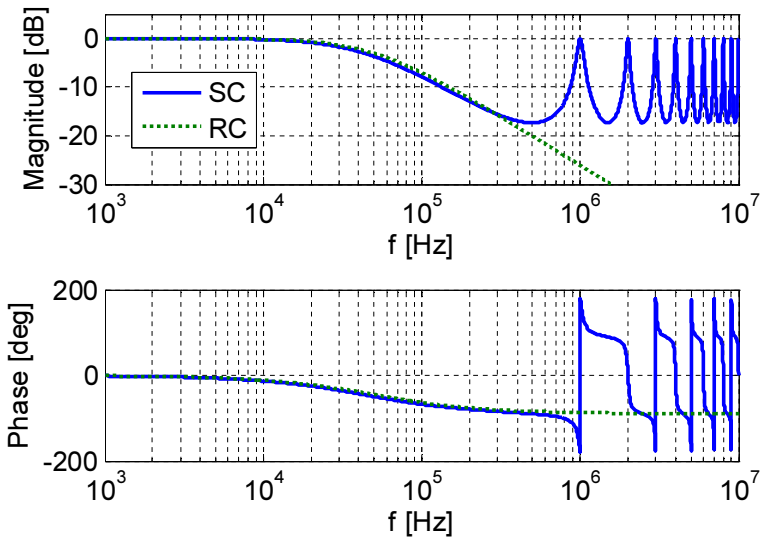
$$V_{out}(s) = \frac{C_1}{C_1 + C_2} V_{in}(s) e^{-s\frac{T_s}{2}} + \frac{C_2}{C_1 + C_2} V_{out}(s) e^{-sT_s}$$

$$V_{out}(s)\left(1 - \frac{C_2}{C_1 + C_2} e^{-sT_s}\right) = \frac{C_1}{C_1 + C_2} V_{in}(s) e^{-s\frac{T_s}{2}}$$

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{e^{-s\frac{T_s}{2}}}{1 + \frac{C_2}{C_1}\left(1 - e^{-sT_s}\right)}$$

- Let's plot this frequency response and compare to the simple RC filter

Frequency Response



Close only for f << f_s

First Order Approximation

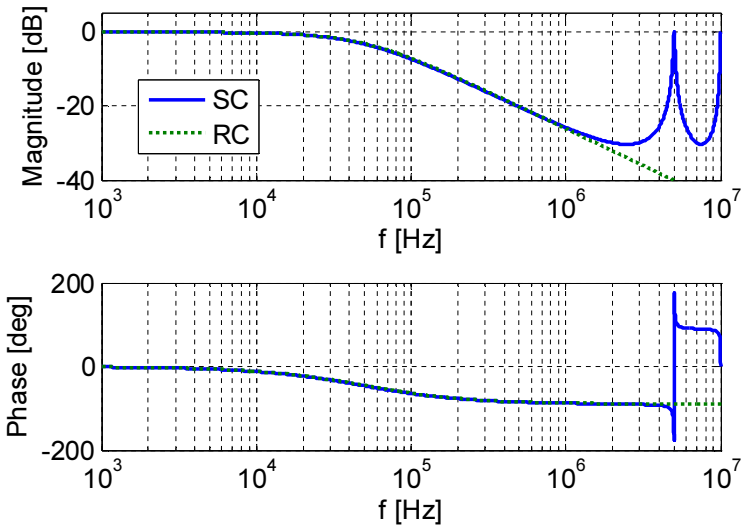
$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{e^{-s\frac{T_s}{2}}}{1+\frac{C_2}{C_1}\left(1-e^{-sT_s}\right)}$$

$$H(j\omega) = \frac{V_{out}(j\omega)}{V_{in}(j\omega)} = \frac{e^{-j\omega\frac{T_s}{2}}}{1+\frac{C_2}{C_1}\left(1-e^{-j\omega T_s}\right)} \qquad \omega T_s = 2\pi\frac{f}{f_s}$$

$$e^{jx} = cos(x) + j\,sin(x) \cong 1 + jx \quad \text{(for small x)}$$

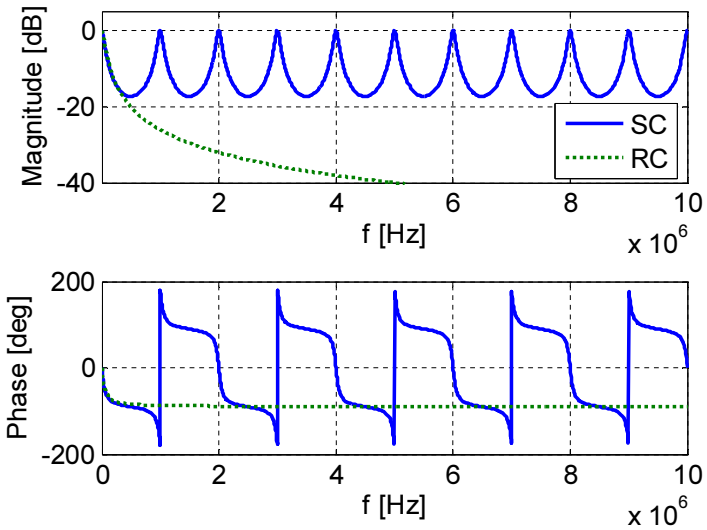
$$\frac{V_{out}(j\omega)}{V_{in}(j\omega)} \cong \frac{1-j\omega\frac{T_s}{2}}{1+\frac{C_2}{C_1}j\omega T_s} = \frac{1-j\pi\frac{f}{f_s}}{1+j\omega\frac{1}{\underbrace{f_s\cdot C_1}_{"R_{avg}"}}C_2}$$

f_s = 5MHz (Previously 1MHz)



Better!

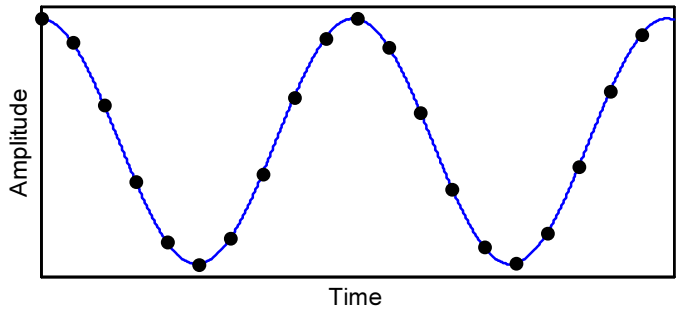
Linear Frequency Axis



The transfer function is periodic with period f_s

Why?

Aliasing (1)



$$f_s = \frac{1}{T_s} = 1000kHz$$

$$f_{in} = 101kHz$$

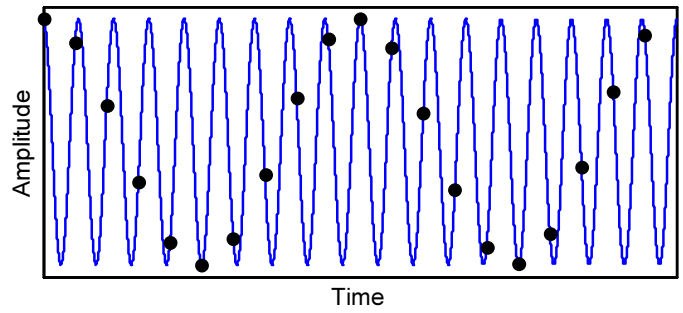
$$v_{in}(t) = \cos(2\pi \cdot f_{in} \cdot t)$$

$$t \rightarrow n \cdot T_s = \frac{n}{f_s}$$

$$v_{in}(n) = \cos\left(2\pi \cdot \frac{f_{in}}{f_s} \cdot n\right)$$

$$= \cos\left(2\pi \cdot \frac{101}{1000} \cdot n\right)$$

Aliasing (2)

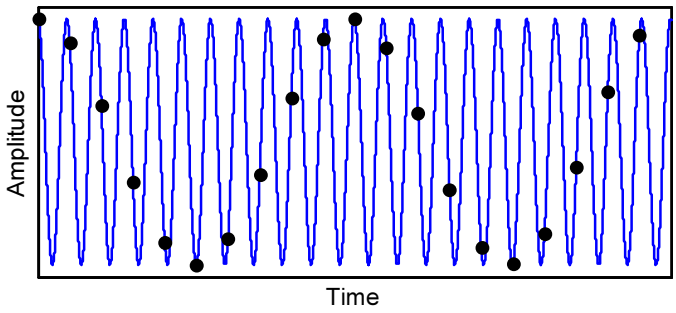


$$f_s = \frac{1}{T_s} = 1000kHz$$

$$f_{in} = 899kHz$$

$$v_{in}(n) = \cos\left(2\pi \cdot \frac{899}{1000} \cdot n\right) = \cos\left(2\pi \cdot \left[\frac{899}{1000} - 1\right] \cdot n\right) = \cos\left(2\pi \cdot \frac{101}{1000} \cdot n\right)$$

Aliasing (3)



$$f_s = \frac{1}{T_s} = 1000kHz$$

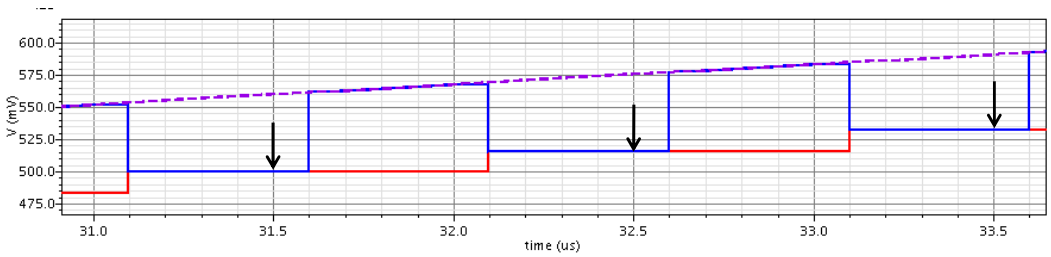
$$f_{in} = 1101kHz$$

$$v_{in}(n) = cos\left(2\pi \cdot \frac{1101}{1000} \cdot n\right) = cos\left(2\pi \cdot \left[\frac{1101}{1000} - 1\right] \cdot n\right) = cos\left(2\pi \cdot \frac{101}{1000} \cdot n\right)$$

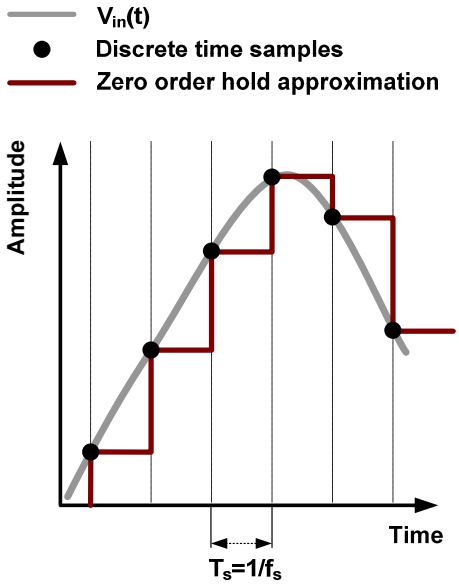
- Bottom line
  - The frequencies f_{in} and $N \cdot f_s \pm f_{in}$ (N integer), are indistinguishable when the signal is represented using discrete times samples at a rate of f_s

Spectrum of Continuous Time Output

- The previous analysis allows us to reason about the output values at discrete time instances (falling edge of ϕ_2)
- What can we say about the spectrum of the continuous time waveform?
- Let's first simplify this question by assuming a very "sharp" staircase waveform, i.e. assume $R_{on} \rightarrow 0$

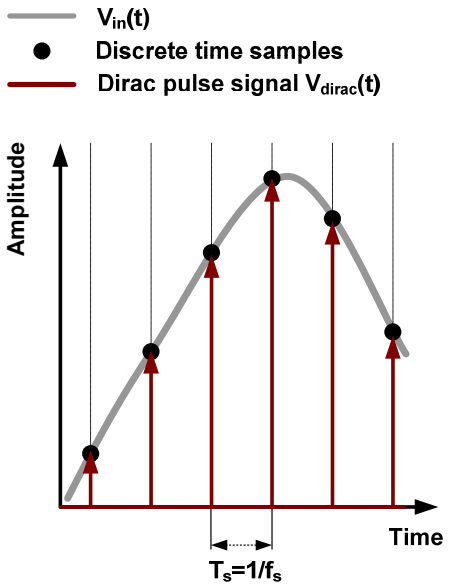


Zero-Order Hold Signal



- A basic way to think about this is to assume that the discrete time values are held for one cycle to generate a continuous time staircase
  - For simplicity, we'll ignore details relating to the "phase" position of the hold pulse relative to the discrete time sample and focus on the magnitude response
- What will the spectrum of the continuous time signal look like?
- We'll analyze this in two steps
  - First look at infinitely narrow pulses in continuous time

Dirac Pulses



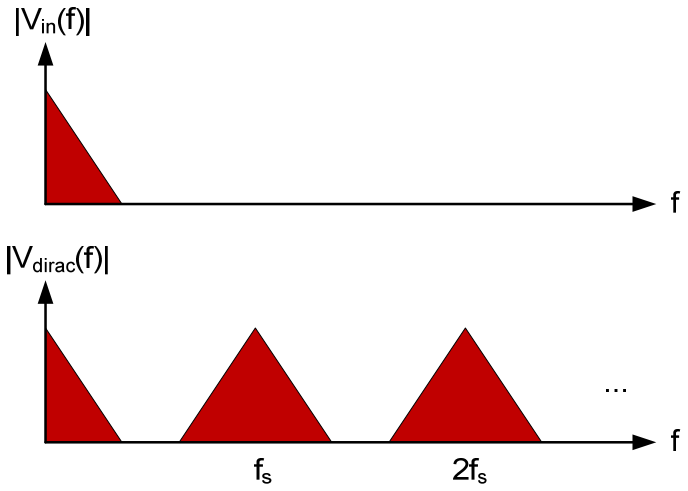
- $V_{dirac}(t)$ is zero between pulses
  - Note that the discrete time sequence is undefined at these times

$$V_{dirac}(t) = V_{in}(t) \cdot \sum_{n=-\infty}^{\infty} \delta(t - nT_s)$$

- Multiplication in time means convolution in frequency
  - Resulting spectrum

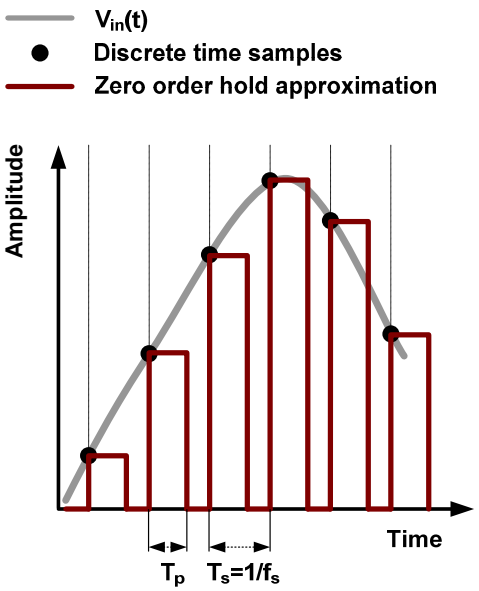
$$V_{dirac}(f) = \frac{1}{T_s} \sum_{n=-\infty}^{\infty} V_{in}\left(f - \frac{n}{T_s}\right)$$

Spectrum



- Spectrum of Dirac Signal contains replicas of $V_{in}(f)$ at integer multiples of the sampling frequency

Effect of Finite Hold Pulse



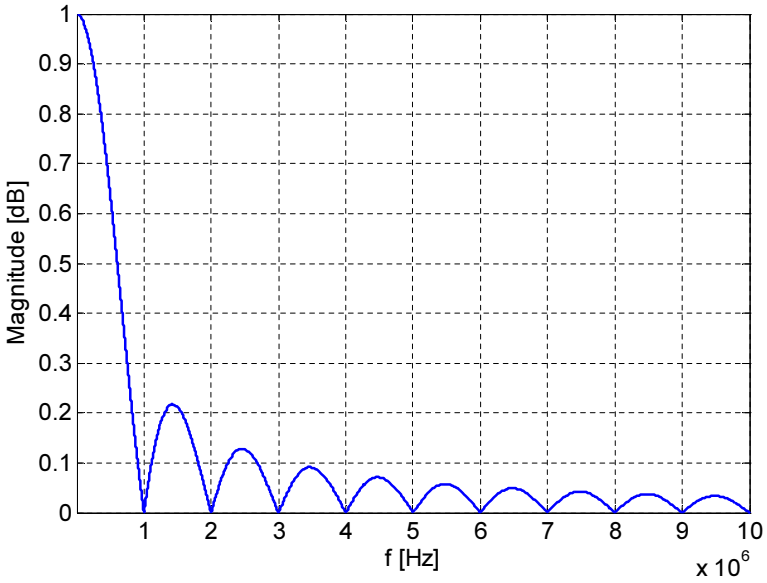
- Consider the general case with a rectangular pulse $0 < T_p \leq T_s$
- The time domain signal follows from convolving the Dirac sequence with a rectangular unit pulse
- The spectrum follows from multiplication with the Fourier transform of the pulse

$$H_p(f) = T_p \frac{sin(\pi f T_p)}{\pi f T_p} \cdot e^{-j\pi f T_p}$$

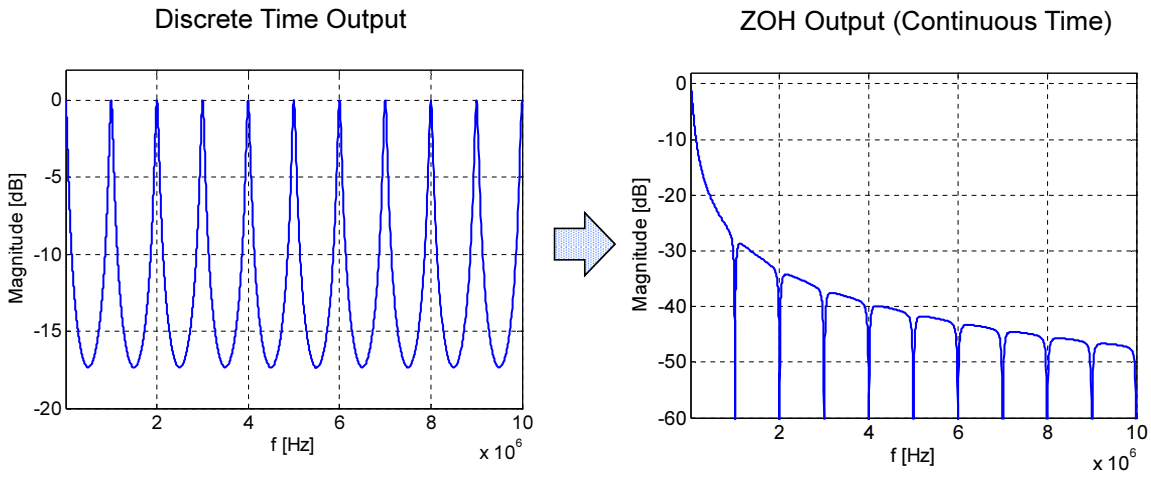
$$V_{ZOH}(f) = \underbrace{\frac{T_p}{T_s} \frac{sin(\pi f T_p)}{\pi f T_p}}_{\text{Amplitude Envelope}} \cdot e^{-j\pi f T_p} \sum_{n=-\infty}^{\infty} V_{in}\left(f - \frac{n}{T_s}\right)$$

"Sinc" Envelope with $T_p=T_s$

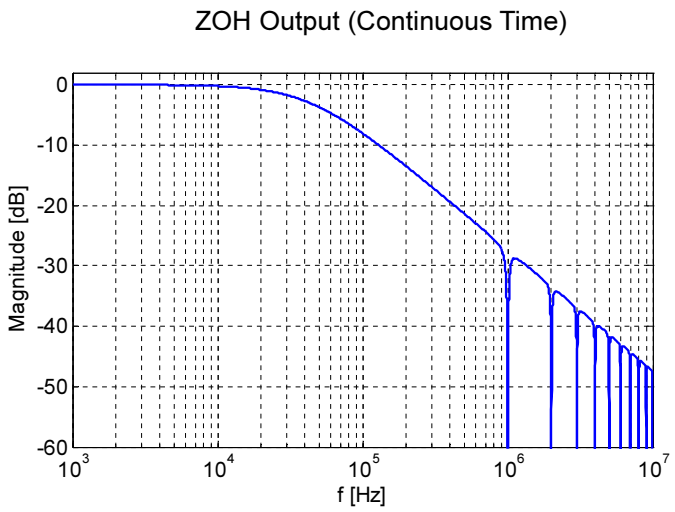
$$\left|\frac{T_p}{T_s}\frac{\sin(\pi f T_p)}{\pi f T_p}\right|$$



Overall Filter Magnitude Response



Logarithmic Frequency Axis



Note: These magnitude plots must be looked at with a "grain of salt" (since the system we're looking at is not LTI). They are not really "transfer functions" in the traditional sense.

Example 1: When you apply an input tone at 2kHz, you get the same frequency at the output (scaled by the shown magnitude), PLUS other tones around multiples of f_s (due to the ZOH operation). These additional tones will have amplitudes scaled by the sinc envelope (as shown in the plot to the left).

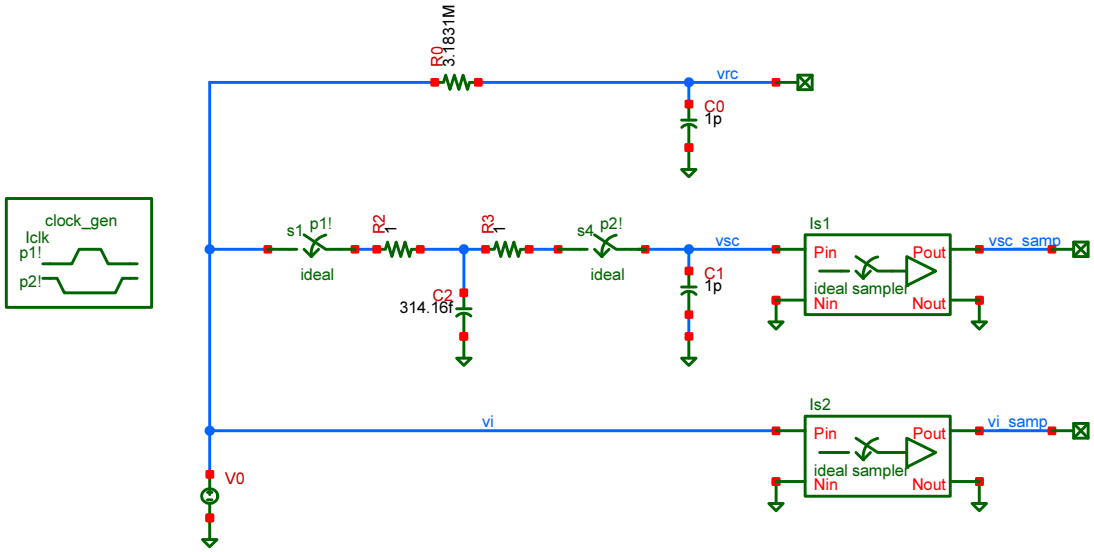
Example 2: When you apply an input tone at 1010kHz, the signal aliases down to 10kHz upon sampling. The "main" tone at the output is therefore at 10kHz, scaled by the magnitude at that frequency. Of course, you will also get the additional tones around multiples of f_s (as per the previous examples. Note that one of these additional tones will be at 1010kHz; i.e. the frequency you actually applied at the input.

We will usually not apply signals at high frequencies. In fact, we will try to remove such frequencies prior to sampling using an anti-alias filter…

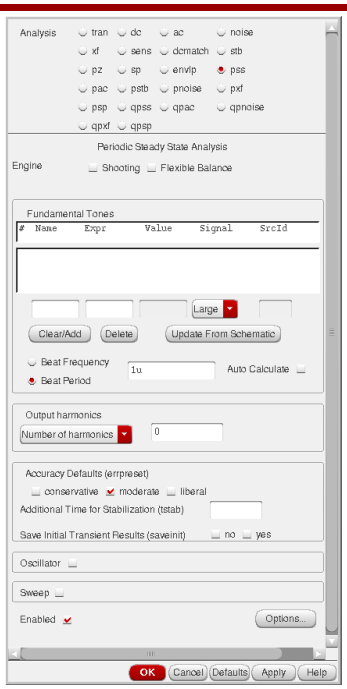
Periodic AC Analysis

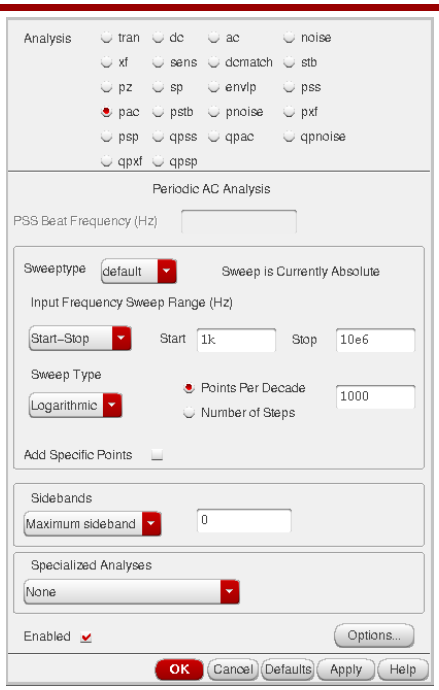
- Can we simulate this frequency response using a circuit simulator?
- Spice
  - .op (operating point) → .ac (ac analysis)
  - Works only for time invariant circuits
- SpectreRF
  - PSS (periodic operating point) → PAC (periodic ac analysis)
  - Works for periodically varying circuits
- Reference
  - http://www.designers-guide.org/Analysis/sc-filters.pdf

Setup for PAC Analysis (1)

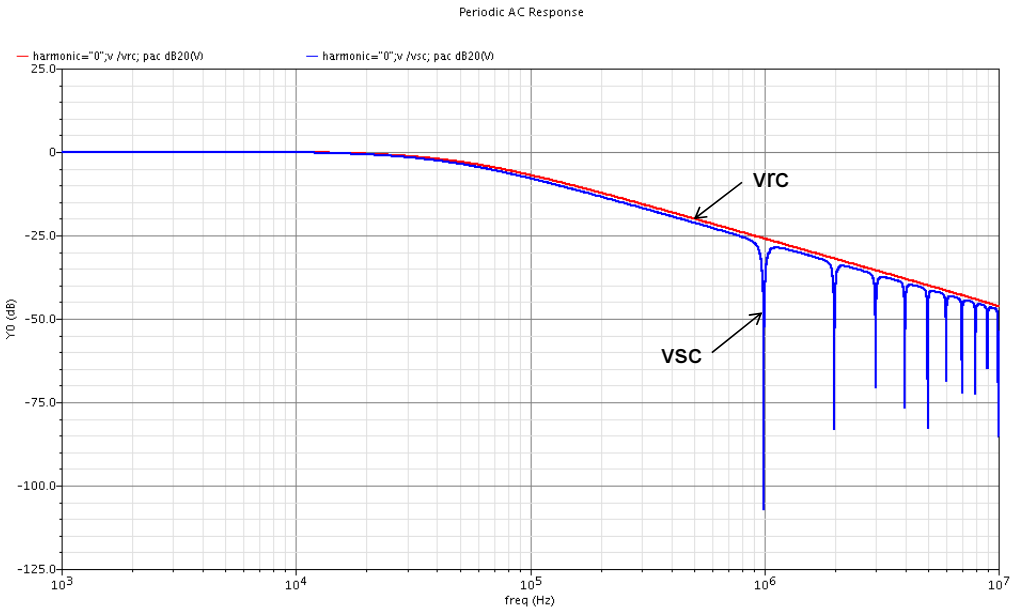


Setup for PAC Analysis (2)

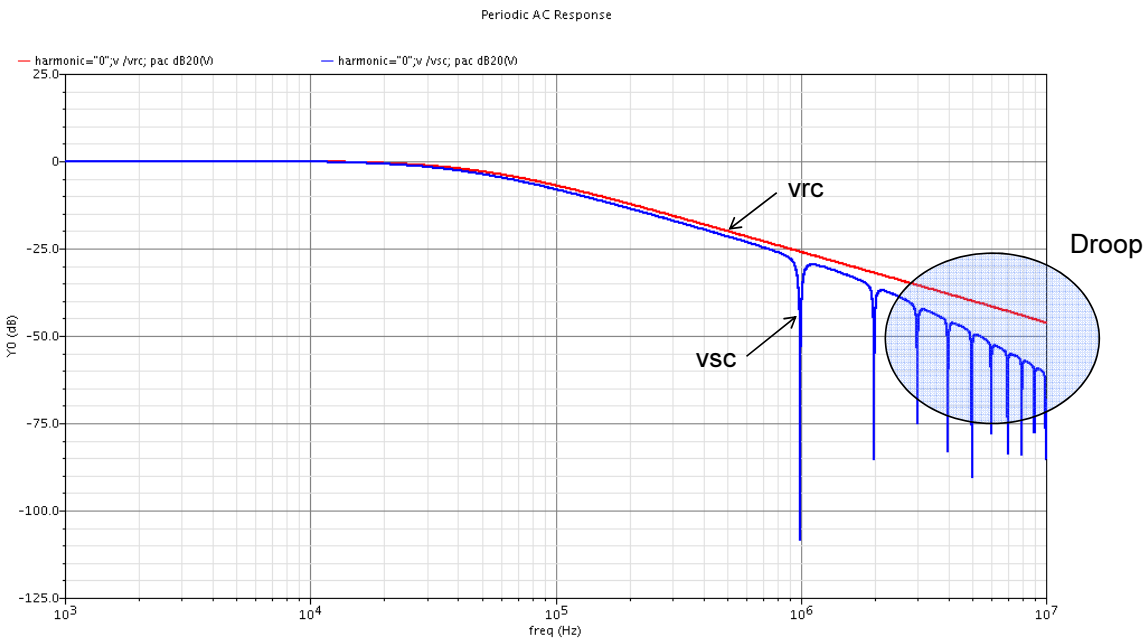




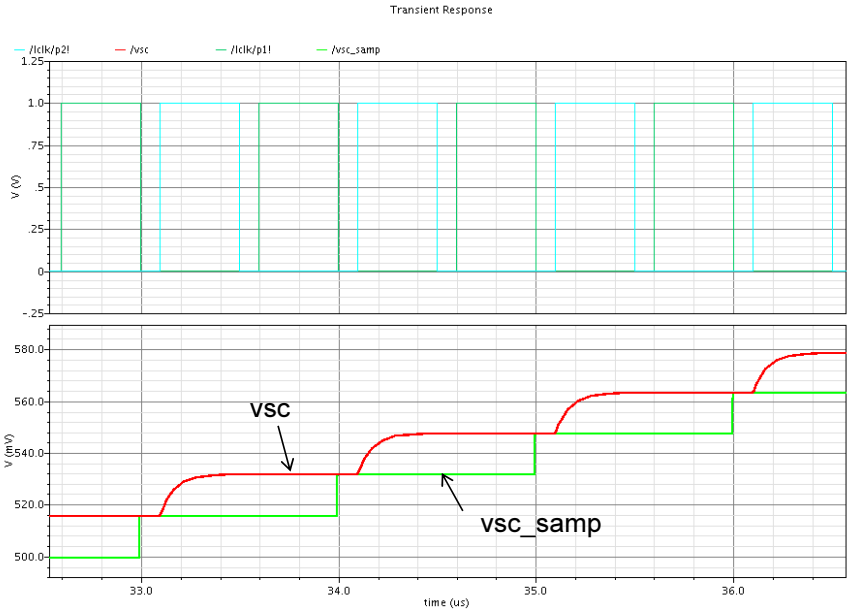
PAC Magnitude Response



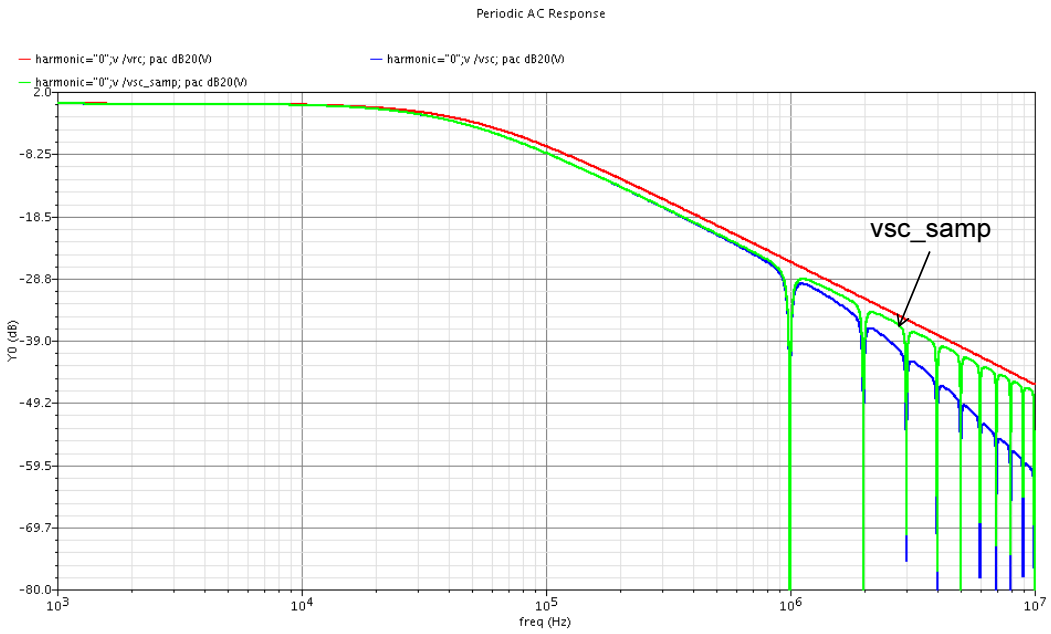
R3 Changed to 300kΩ (from 1Ω)



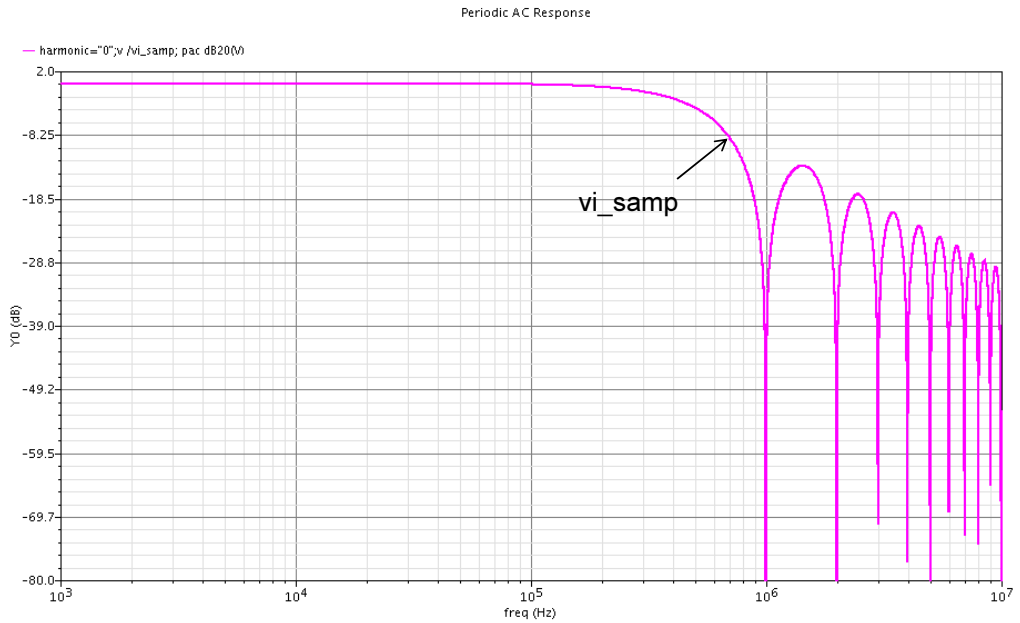
Transient Waveforms



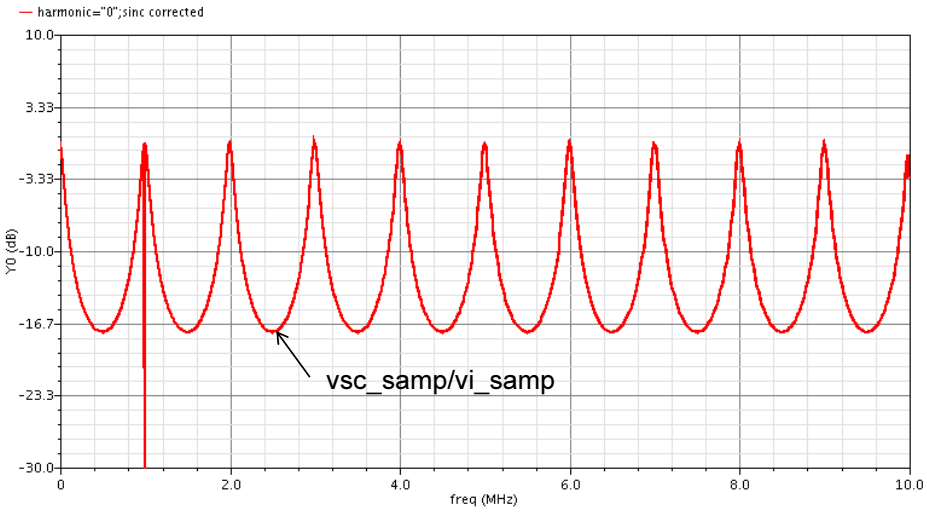
Response After Output Sampler



Sampled Input ("Dummy" Sinc)

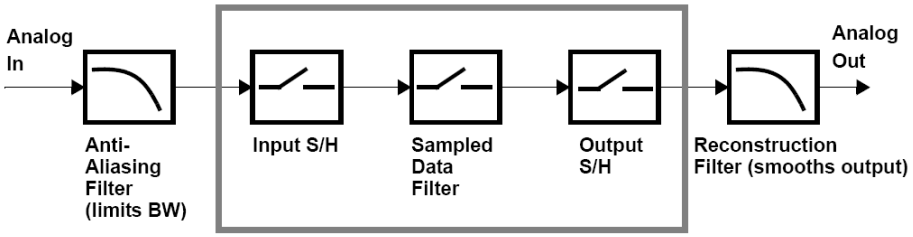


Sinc Corrected Response



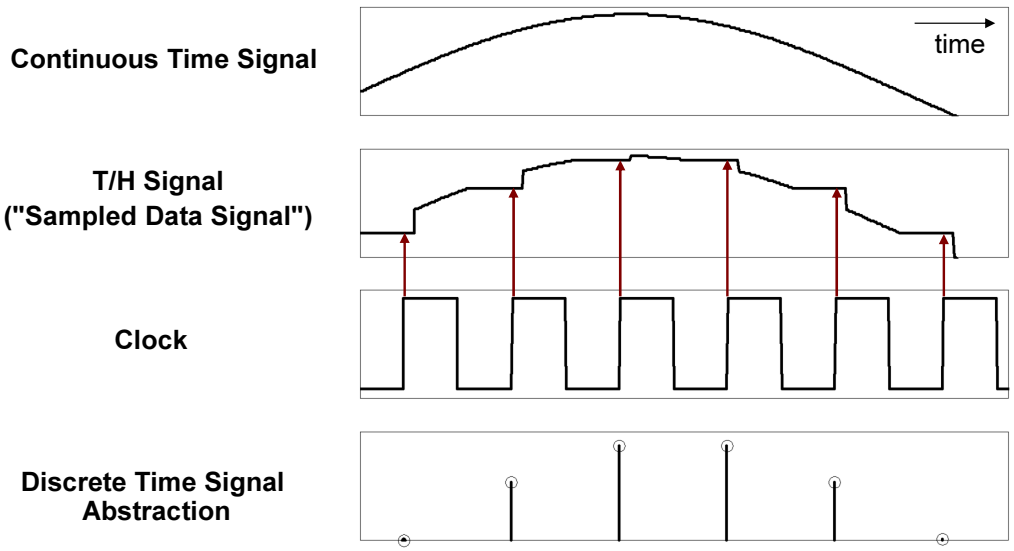
- Matches Matlab result exactly
  - But, of course, in SpectreRF we can now study nonidealities at the circuit level…

Anatomy of a Complete SC Filter

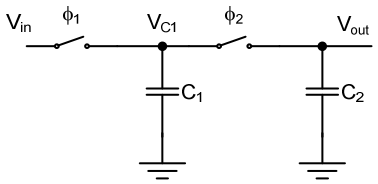


- All signals in this processing chain are continuous in time (as all physical signals)
- However, the core of the filter (“sampled data filter” block) can typically be modeled as a “discrete time” system → z-transform
  - The core takes voltage samples at the input and produces samples at the output
  - The internal transients that generate these samples are irrelevant, as long as they have settled at the time the sample is taken

Signal Nomenclature



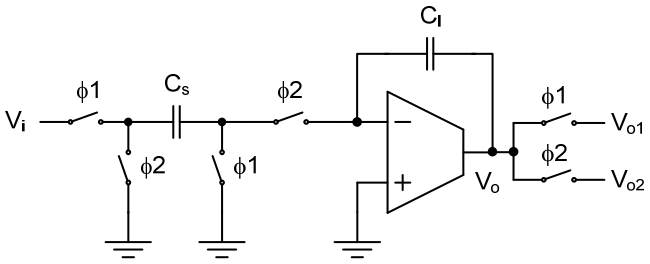
z-Domain Representation of Simple SC Filter

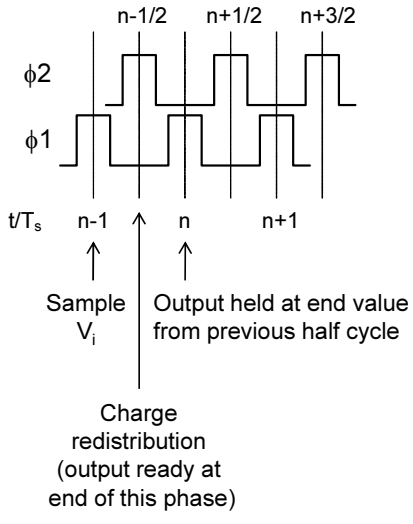


$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{e^{-s\frac{T_s}{2}}}{1 + \frac{C_2}{C_1}\left(1 - e^{-sT_s}\right)} \qquad z = e^{sT_s}$$

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{z^{-\frac{1}{2}}}{1 + \frac{C_2}{C_1}\left(1 - z^{-1}\right)}$$

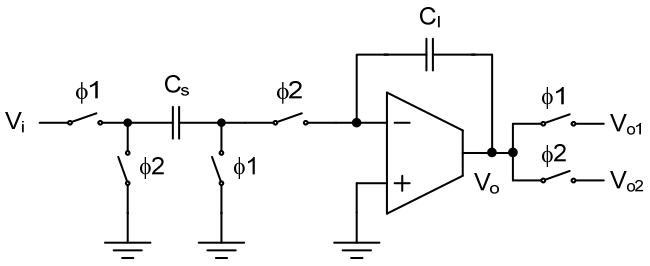
Noninverting Integrator Analysis (1)

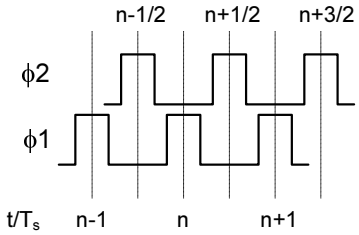




- Output can be sampled during either ϕ1 or ϕ2
- Sampling at ϕ1 means that there will be an additional ½ clock cycle delay ($z^{-1/2}$)

Noninverting Integrator Analysis (2)





t/T_s	Q_s	Q_I	
n-1	$C_s \cdot V_i(n-1)$	$C_I \cdot V_o(n-1) = C_I \cdot V_o(n-3/2)$	
n-1/2	0	$C_I \cdot V_o(n-1/2) = C_I \cdot V_o(n-3/2) + C_s \cdot V_i(n-1)$	$\longrightarrow V_{o2}$
n	$C_s \cdot V_i(n)$	$C_I \cdot V_o(n) = C_I \cdot V_o(n-1) + C_s \cdot V_i(n-1)$	$\longrightarrow V_{o1}$
n+1/2	…	…	

Noninverting Integrator Analysis (3)

$$C_I V_{o2}\left(n-\frac{1}{2}\right) = C_I V_{o2}\left(n-\frac{3}{2}\right) + C_s V_i(n-1)$$

$$C_I V_{o2}(z) z^{-\frac{1}{2}} = z^{-\frac{3}{2}} C_I V_{o2}(z) + z^{-1} C_s V_i(z)$$

$$H_2(z) = \frac{V_{o2}(z)}{V_i(z)} = \frac{C_s}{C_I} \frac{z^{-\frac{1}{2}}}{1-z^{-1}}$$

"LDI Integrator"
(Lossless Digital Integrator)

$$H_1(z) = \frac{V_{o1}(z)}{V_i(z)} = \frac{C_s}{C_I} \frac{z^{-1}}{1-z^{-1}}$$

"DDI Integrator"
(Direct Digital Integrator)

- What is the frequency response of this integrator?
  - First look at $H_2(z)$

Frequency Response (H_2)

$$H_2(\omega) = H_2(z)\big|_{z=e^{j\omega T_s}} = \frac{C_s}{C_I}\frac{z^{-1/2}}{1-z^{-1}}\bigg|_{z=e^{j\omega T_s}} = \frac{C_s}{C_I}\frac{1}{z^{\frac{1}{2}}-z^{-\frac{1}{2}}}\bigg|_{z=e^{j\omega T_s}=\cos(\omega T_s)+j\sin(\omega T_s)}$$

$$= \frac{C_s}{C_I}\frac{1}{\cos\left(\frac{\omega T_s}{2}\right)+j\sin\left(\frac{\omega T_s}{2}\right)-\cos\left(\frac{\omega T_s}{2}\right)+j\sin\left(\frac{\omega T_s}{2}\right)}$$

$$= \underbrace{\frac{C_s}{C_I}\frac{1}{j\omega T_s}}_{Ideal}\underbrace{\frac{\omega T_s}{2\sin\left(\frac{\omega T_s}{2}\right)}}_{Magnitude\ error} \cong \frac{C_s}{C_I}\frac{1}{j\omega T_s} \qquad \text{for} \qquad \frac{\omega T_s}{2} = \pi\frac{f}{f_s} << 1$$

- Behaves like an RC integrator for low frequencies (f << f_s)
  - R replaced by $1/(f_s C_s)$, as before

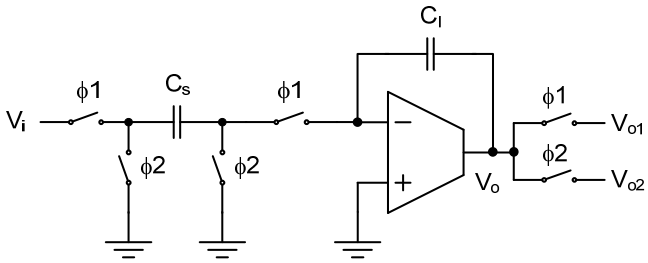
Frequency Response (H_1)

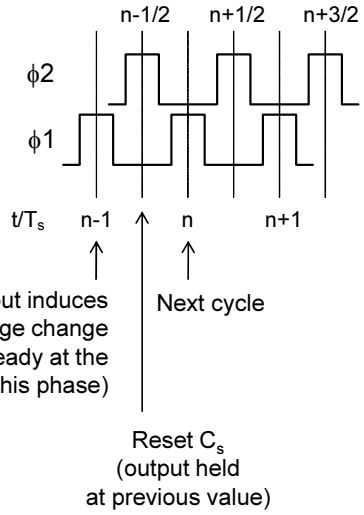
$$H_1(\omega) = H_1(z)\big|_{z=e^{j\omega T_s}} = \frac{C_s}{C_I}\frac{z^{-1}}{1-z^{-1}}\bigg|_{z=e^{j\omega T_s}}$$

$$= \frac{C_s}{C_I}\frac{z^{-\frac{1}{2}}}{z^{\frac{1}{2}}-z^{-\frac{1}{2}}}\bigg|_{z=e^{j\omega T_s}} = \underbrace{\frac{C_s}{C_I}\frac{1}{j\omega T_s}}_{Ideal}\underbrace{\frac{\omega T_s}{2\sin\left(\frac{\omega T_s}{2}\right)}}_{Magnitude\ error}\underbrace{e^{-j\frac{\omega T_s}{2}}}_{Phase\ error}$$

- Magnitude error as before, but now there's also a phase error
  - Bad news if we are looking to build a high Q filter
- Numerical example for f=f_s/32
  - Magnitude error = 0.16% → may not be a problem
  - Phase error = -5.6 degrees → big problem!

Inverting Integrator

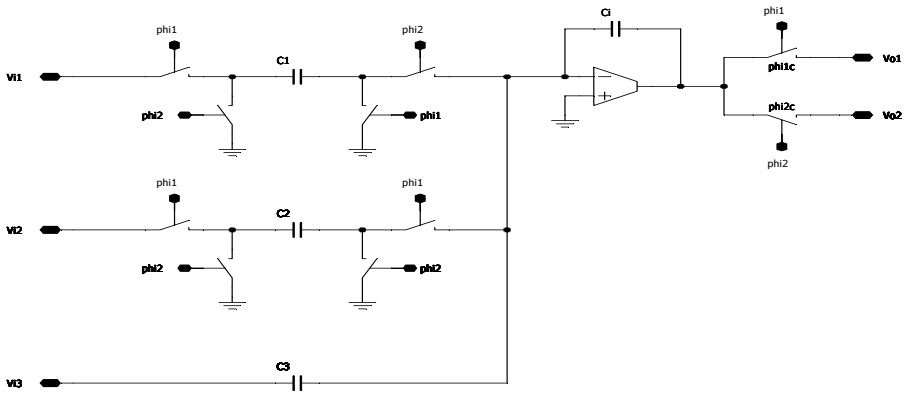




$$H_1(z) = -\frac{C_s}{C_I}\frac{1}{1-z^{-1}}$$

$$H_2(z) = -\frac{C_s}{C_I}\frac{z^{-\frac{1}{2}}}{1-z^{-1}}$$ "LDI"

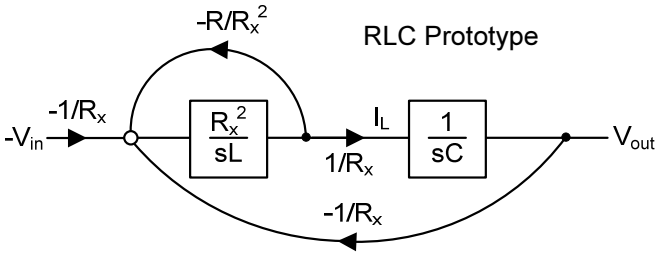
General Building Block



$$V_{o1}(z) = \frac{C_1}{C_i}\frac{z^{-1}}{1-z^{-1}}V_{i1}(z) - \frac{C_2}{C_i}\frac{1}{1-z^{-1}}V_{i2}(z) - \frac{C_3}{C_i}V_{i3}(z)$$

$$V_{o2}(z) = \frac{C_1}{C_i}\frac{z^{-1/2}}{1-z^{-1}}V_{i1}(z) - \frac{C_2}{C_i}\frac{z^{-1/2}}{1-z^{-1}}V_{i2}(z) - \frac{C_3}{C_i}V_{i3}(z)$$

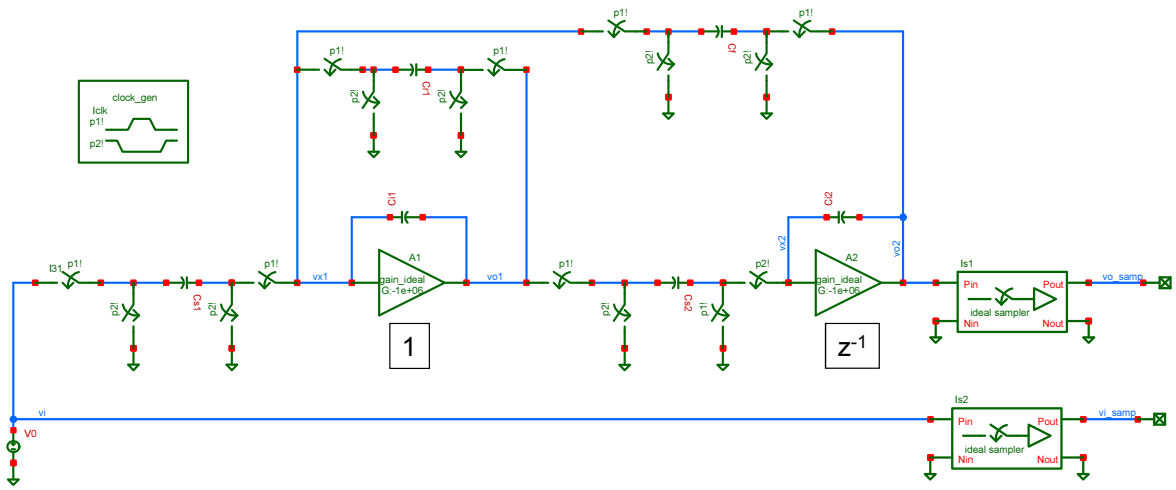
Let's Build a Biquad



$$\frac{1}{s} \rightarrow \frac{z^{-\frac{1}{2}}}{1 - z^{-1}}$$

- Key objective
  - Avoid integrator phase errors
- Conceptually two possible solutions
  - Try to use only LDI integrators
  - Combine delaying (DDI) and non-delaying integrator to achieve LDI behavior

Realization



Component Values

Target: $\omega_P := 2\cdot\pi\cdot 10\text{kHz}$ $Q_P := 5$

Pick: $C := 10\text{pF}$ $R_X := 1\text{M}\Omega$ $f_s := 1\text{MHz}$

LC component values: $R := \frac{1}{\omega_P \cdot Q_P \cdot C} = 318.31\cdot\text{k}\Omega$ $L := \frac{1}{\omega_P^2 \cdot C} = 25.33\,\text{H}$

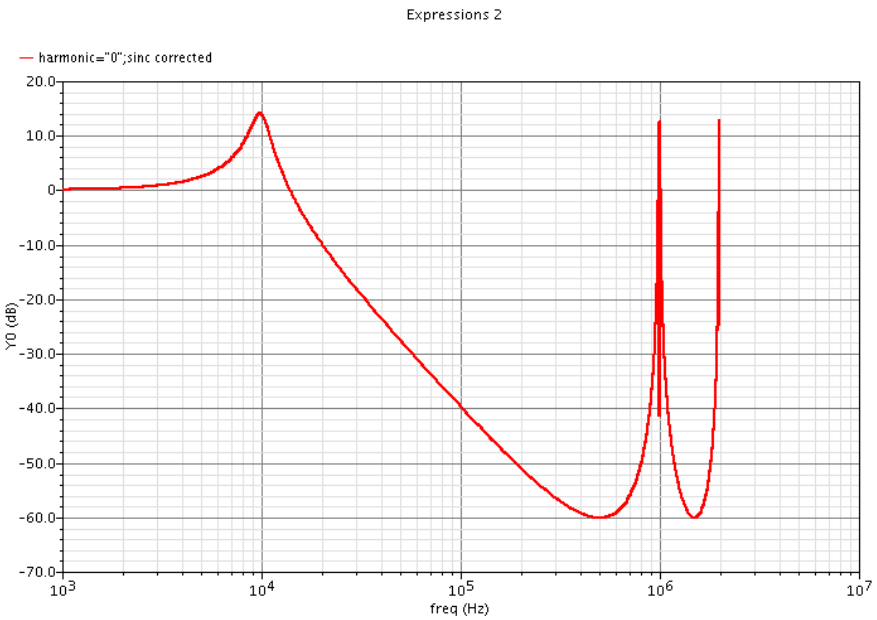
SC component values:

$C_{i2} := C = 10\cdot\text{pF}$ $C_{s1} := \frac{1}{f_s \cdot R_X} = 1\cdot\text{pF}$

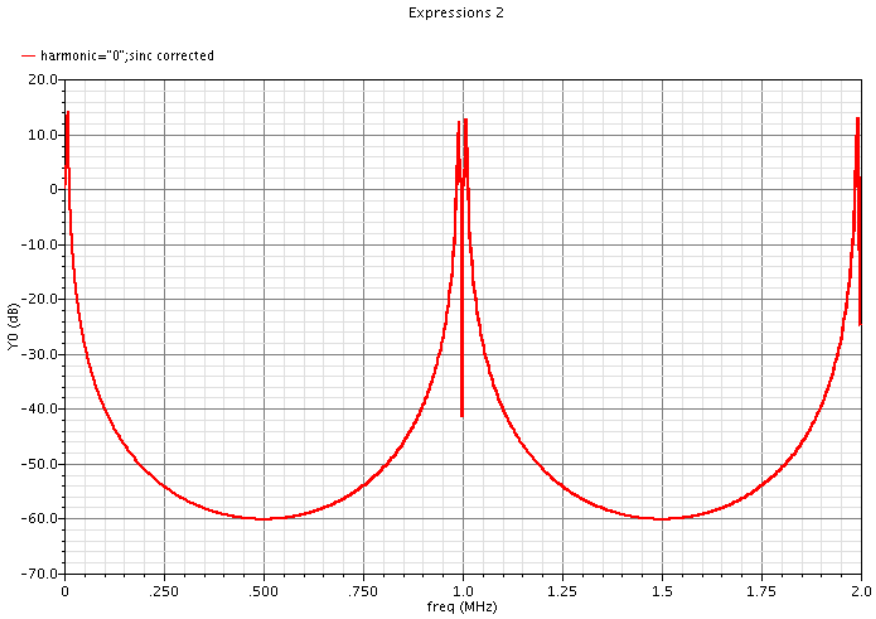
$C_{i1} := \frac{L}{R_X^2} = 25.33\cdot\text{pF}$ $C_{r1} := \frac{R}{f_s \cdot R_X^2} = 0.318\cdot\text{pF}$

$C_f := \frac{1}{f_s \cdot R_X} = 1\cdot\text{pF}$ $C_{s2} := \frac{1}{f_s \cdot R_X} = 1\cdot\text{pF}$

PAC Output



Linear Frequency Axis



High Frequency Behavior

- Our RLC prototype filter has two zeros at infinity
  - Where did these go in the SC realization?
- It would be great to have some zeros at high frequencies
  - E.g. $f_s/2$ would be a great place!
  - This can help improve the stopband attenuation, especially when we're trying to minimize f_s
- Need to think about how exactly frequencies are mapped from the continuous time prototype to the switched capacitor realization

CT – SC Integrator Comparison

- RC and SC (LDI) integrator transfer functions

$$H_{RC}(s) = \frac{1}{sRC} = \frac{1}{2\pi j f_{RC} RC} \qquad H_{SC}(z) = \frac{C_s}{C_i}\frac{z^{-1/2}}{1-z^{-1}} = \frac{C_s}{C_i}\frac{1}{2j\sin(\pi f_{SC} T_s)}$$

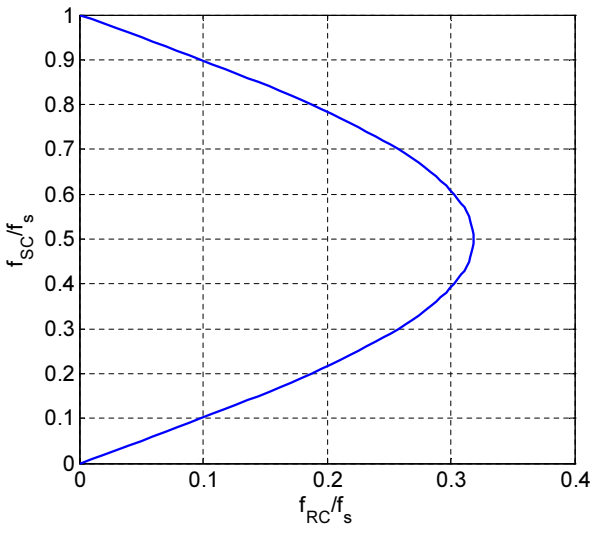
- In our LDI-based design, we set the RC time constant equal to the approximate SC time constant, i.e.

$$RC = \frac{C_i}{f_s C_s}$$

- Setting $H_{RC}(f_{RC}) = HSC(f_{SC})$ therefore gives

$$f_{RC} = \frac{f_s}{\pi}\sin\left(\pi\frac{f_{SC}}{f_s}\right)$$

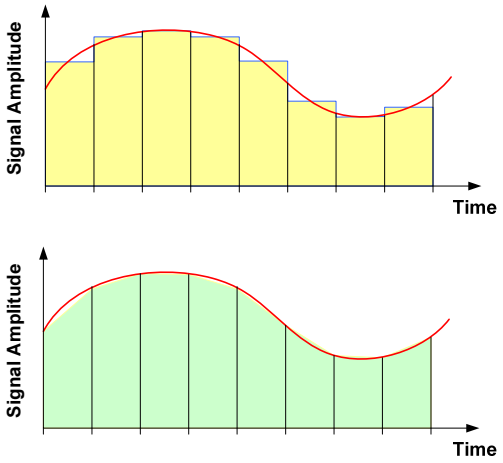
Frequency Warping (LDI)



$$f_{RC} = \frac{f_s}{\pi}\sin\left(\pi\frac{f_{SC}}{f_s}\right)$$

- Frequency mapping is accurate only for $f_{RC} << f_s$
- RC frequencies up to f_s/π map to "physical SC" frequencies
- Mapping is symmetric about $f_s/2$ (aliasing)

A Closer Look at Integration Methods



- LDI integrators apply a "midpoint integration
- A much more accurate way to integrate is using a trapezoidal ("bilinear") integration rule

$$v_o(nT_s) = v_o(nT_s - T_s) + \frac{T_s}{2}\left[v_i(nT_s) + v_i(nT_s - T_s)\right]$$

- Many others exist, e.g. Euler, Runge Kutta, Gear, …

Bilinear Integrator

$$v_o(nT_s) = v_o(nT_s - T_s) + \frac{T_s}{2}\left[v_i(nT_s) + v_i(nT_s - T_s)\right]$$

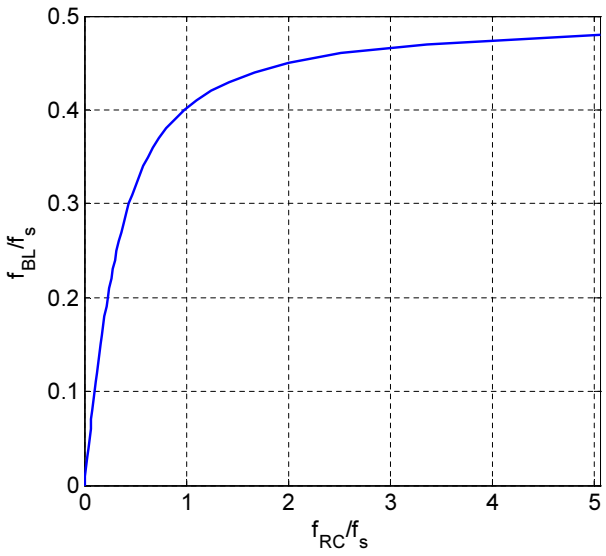
$$\left[1 - z^{-1}\right]V_o(z) = \frac{T_s}{2}\left[1 + z^{-1}\right]V_i(z)$$

$$H_{BL}(z) = \frac{V_o(z)}{V_i(z)} = \frac{T_s}{2}\frac{1 + z^{-1}}{1 - z^{-1}}$$

- Bilinear transform

$$s \rightarrow \frac{2}{T_s}\frac{1 - z^{-1}}{1 + z^{-1}}$$

Frequency Warping (Bilinear)



$$\left.\frac{1}{s}\right|_{s=2\pi j f_{RC}} = H_{BL}(z)\Big|_{z=e^{2\pi j f_{BL} T_S}}$$

$$\Rightarrow f_{RC} = \frac{f_s}{\pi} tan\left(\pi \frac{f_{BL}}{f_s}\right)$$

- No frequencies are lost
  - E.g. zeros at infinity will be mapped to $f_s/2$
- Can show that bilinear transform maps $j\omega$ axis in s plane onto unit circle in z-plane

Possible Design Procedure

- Pre-warp "important" frequencies, e.g. passband edge and/or stopband edge using

$$f_{RC} = \frac{f_s}{\pi} tan\left(\pi \frac{f_{BL}}{f_s}\right)$$

- Note that pre-warping is important mostly for filters that try to aggressively push toward minimum f_s
- Determine continuous time prototype filter function H(s) using pre-warped frequency specifications
- Substitute

$$s \rightarrow \frac{2}{T_s} \frac{1 - z^{-1}}{1 + z^{-1}}$$

- Implement z- transfer function using a known (and well-understood) Biquad realization, ladder, etc.

Alternative

- Let Matlab do all of this…
- Design filter in z-domain, e.g.

```
[B,A] = BUTTER(N, fc_fs)
```

- Matlab will then automatically
  - Pre-warp the frequency specifications
  - Carry out a bilinear transform (using function (“bilinear”)
  - Give you the z-transfer function of the filter

Martin-Sedra Biquad

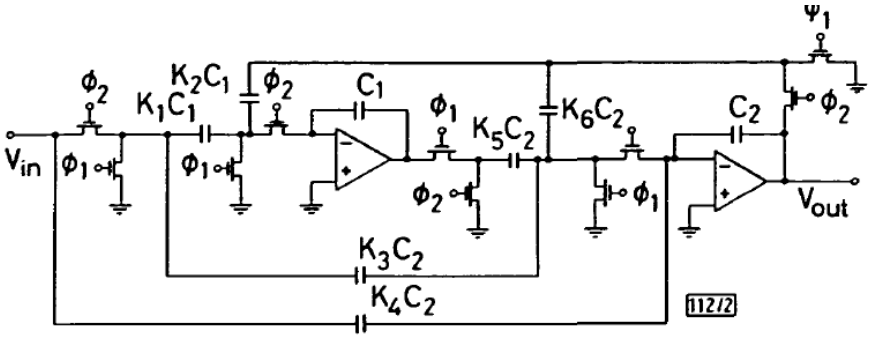
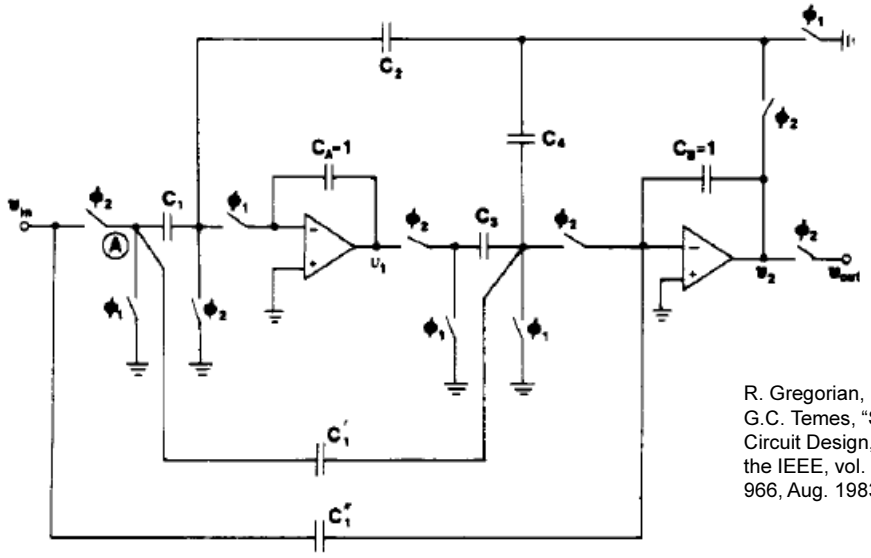


Fig. 2 *Circuit capable of realising all bilinear-transformed biquadratic transfer functions except for bandpass*

$$\frac{V_o(z)}{V_i(z)} = -\frac{z^2(K_3 + K_4) + z(K_1 K_5 - 2K_4 - K_3) + K_4}{z^2(1 + K_6) + z(K_2 K_5 - K_6 - 2) + 1}$$

K. Martin and A. S. Sedra, “Strays-insensitive switched-capacitor filters based on the bilinear z transform,” Electron. Lett., vol. 19, pp. 365-6, June 1979.

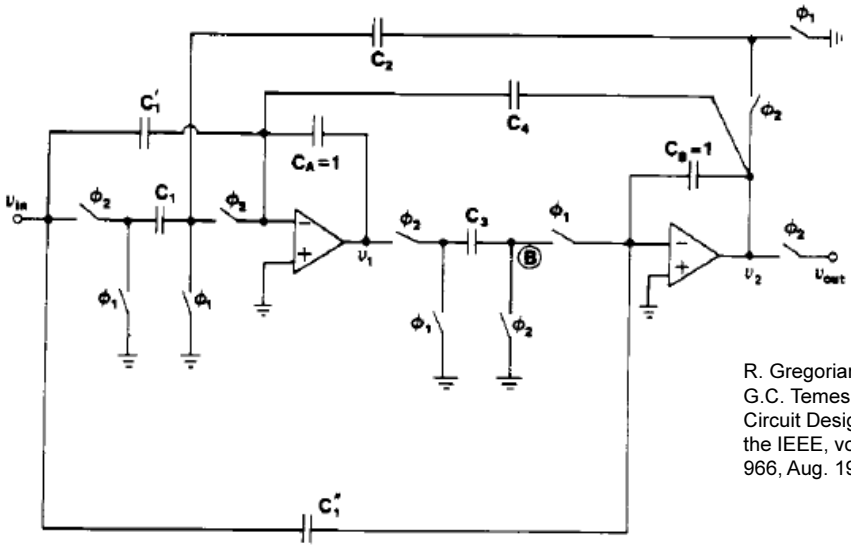
"Low-Q" Biquad



R. Gregorian, K.W. Martin, and G.C. Temes, "Switched-Capacitor Circuit Design," Proceedings of the IEEE, vol. 71, no. 8, pp. 941-966, Aug. 1983.

$$\frac{V_{out}(z)}{V_{in}(z)} = -\frac{(C_1' + C_1'')z^2 + (C_1C_3 - C_1' - 2C_1'')z + C_1''}{(1 + C_4)z^2 + (C_2C_3 - C_4 - 2)z + 1}$$

"Hi-Q" Biquad



R. Gregorian, K.W. Martin, and G.C. Temes, "Switched-Capacitor Circuit Design," Proceedings of the IEEE, vol. 71, no. 8, pp. 941-966, Aug. 1983.

$$H(z) = \frac{V_{out}}{V_{in}} = -\frac{C_1''z^2 + (C_1C_3 + C_1'C_3 - 2C_1'')z + (C_1'' - C_1'C_3)}{z^2 + (C_2C_3 + C_3C_4 - 2)z + (1 - C_3C_4)}.$$

Lowpass Example Using Bilinear Transform

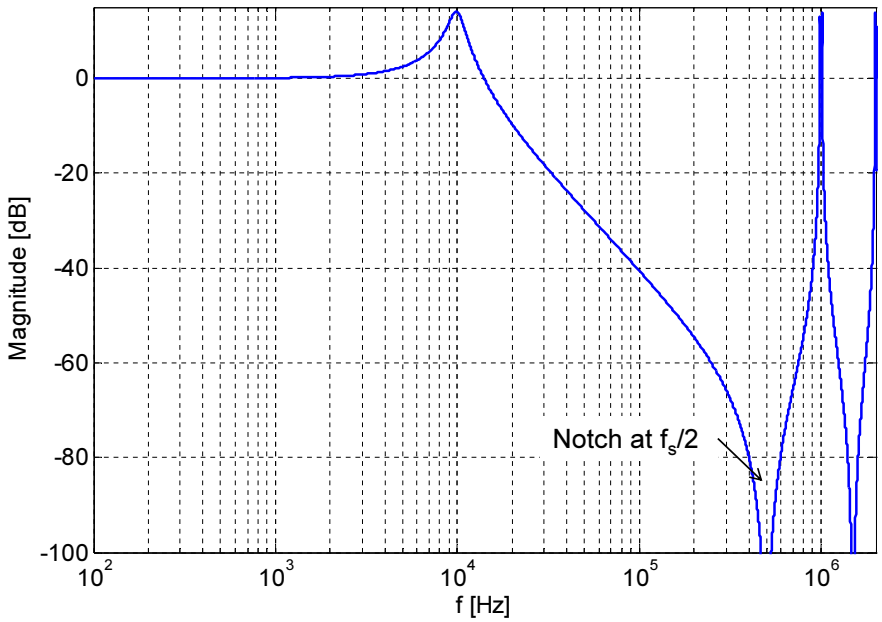
- Specs: f_{PBL}=10kHz, Q_P=5, f_s=1MHz
- Pre-warping (not all that significant in this example…)

$$f_{PRLC} = \frac{f_s}{\pi} tan\left(\pi \frac{f_P}{f_s}\right) = \frac{1MHz}{\pi} tan\left(\pi \frac{10kHz}{1MHz}\right) = 10.002MHz$$

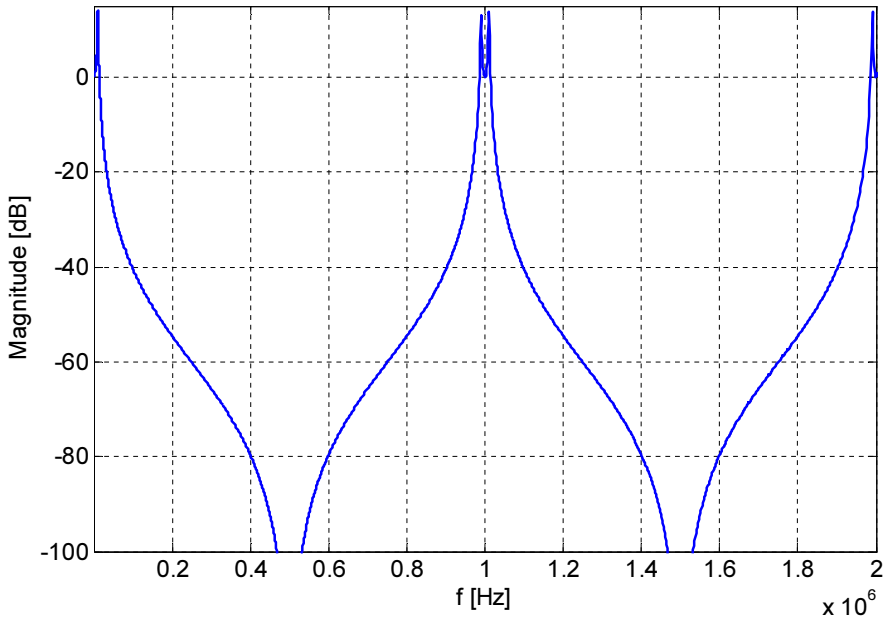
$$H(s) = \frac{1}{1 + \frac{s}{\omega_{PRLC} Q_P} + \frac{s^2}{\omega_{PRLC}^2}} \qquad s \to \frac{2}{T_s} \frac{1 - z^{-1}}{1 + z^{-1}}$$

- Compute H(z)
- Implement using Biquad
- Simulate, plot frequency response…

Frequency Response



Linear Frequency Axis



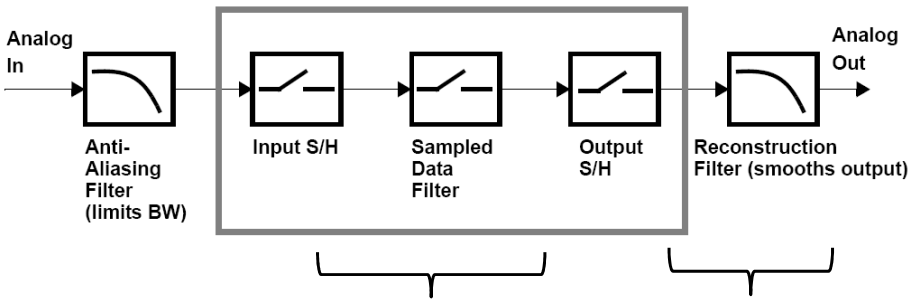
LDI versus Bilinear Transform

- LDI transform
  - Realized by “standard” SC integrators
  - High frequency zeros are lost
  - Simple filter synthesis
    - Replace RC integrators with SC integrators, ensuring proper delays around integrator loops ($z^{-1/2}$ per integrator)
- Bilinear transform
  - Does not lose high frequency zeros
  - Biquad-based synthesis
    - Direct coefficient comparison with known realizations
  - Ladders
    - See e.g. R.B. Datar and A.S. Sedra, “Exact design of strays-insensitive switched capacitor high-pass ladder filters,” Electronics Letters, vol. 19, no. 29, pp. 1010-1012, Nov. 1983.

Nonidealities in Switched Capacitor Filters

- Finite amplifier gain
- Finite amplifier bandwidth and slew rate
- Thermal noise
  - From SC resistor emulation
  - From amplifiers
- Parasitic capacitance
  - Use parasitic insensitive configurations
- Amplifier offset voltage and flicker noise
  - Often not an issue
  - If problematic use “correlated double sampling”
    - Covered later in this course
- Switch charge injection and clock feedthrough
  - Use “bottom plate sampling”
    - See EE315B

SC Filter Nonidealities



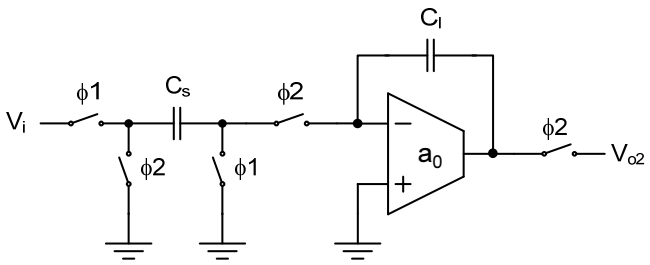
Sufficient to understand errors in the discrete time signal samples

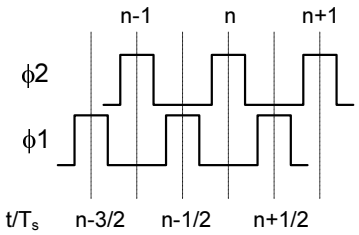
→ Focus mostly on this aspect in the following discussion

Must look at errors in the continuous time domain

→ Much more complicated; signals are sums of reconstruction pulses, continuous time feedthrough signals, etc.

Finite Gain (1)





t/T_s	Q_s	Q_I
n-1/2	$C_s \cdot V_i(n-1/2)$	$C_I \cdot V_{o2}(n-1) \cdot [1+1/a_0]$
n	$C_s \cdot V_{o2}(n)/a_0$	$C_I \cdot V_{o2}(n) \cdot [1+1/a_0]$ $= C_I \cdot V_{o2}(n-1) \cdot [1+1/a_0] + C_s \cdot V_i(n-1/2) - C_s \cdot V_{o2}(n)/a_0$

Finite Gain (2)

$$V_{o2}(z)C_I\left\{\left[1+\frac{1}{a_0}\right]\left[1-z^{-1}\right]+\frac{1}{a_0}\frac{C_s}{C_I}\right\}=V_i(z)C_s z^{-\frac{1}{2}}$$

$$\frac{V_{o2}(z)}{V_i(z)}=\frac{C_s}{C_I}\frac{z^{-\frac{1}{2}}}{\left[1+\frac{1}{a_0}\right]\left[1-z^{-1}\right]+\frac{1}{a_0}\frac{C_s}{C_I}}\cong\frac{C_s}{C_I}\frac{1}{\left[1+\frac{1}{a_0}\right]sT_s+\frac{1}{a_0}\frac{C_s}{C_I}}$$

$$\cong\frac{C_s}{C_I T_s}\frac{1}{\left[1+\frac{1}{a_0}\right]s+\frac{1}{a_0}\frac{C_s}{C_I T_s}}$$

Compare to active RC integrator with finite a_0:

$$A(s)=-\omega_0\frac{1}{s\left(1+\frac{1}{a_0}\right)+\frac{\omega_0}{a_0}}$$

Bottom line: approximately same gain requirements as active RC

Finite Bandwidth (1)

- First order result
  - SC filters have much smaller amplifier bandwidth requirements than active RC counterparts

K. Martin and A. Sedra, "Effects of the op amp finite gain and bandwidth on the performance of switched-capacitor filters," *IEEE Trans. Circuits and Systems,* vol. 28, no. 8, pp. 822-829, Aug. 1981.

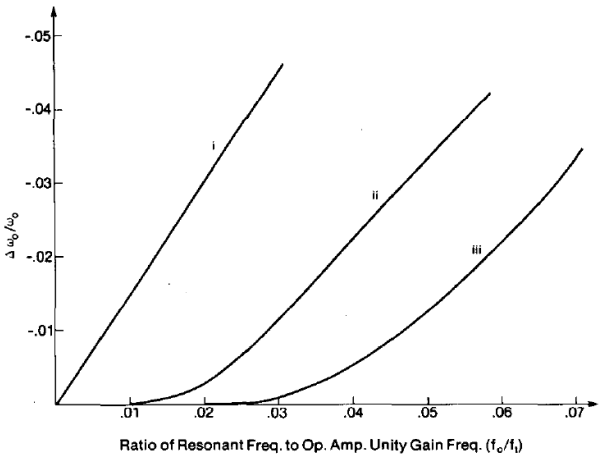
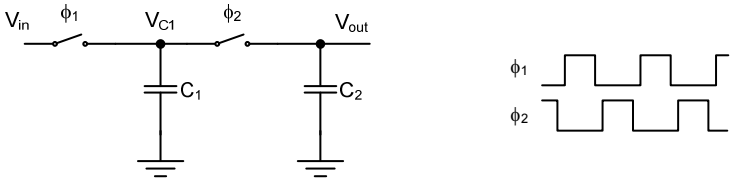


Fig. 4. A comparison of the deviation in pole frequency $\Delta\omega_0/\omega_0$ due to finite f_t for: (i) Tow–Thomas active-RC biquad, (ii) SC biquad with $f_0/f_c = 1/32$, and (iii) SC biquad with $f_0/f_c = 1/12$.

Finite Bandwidth (2)

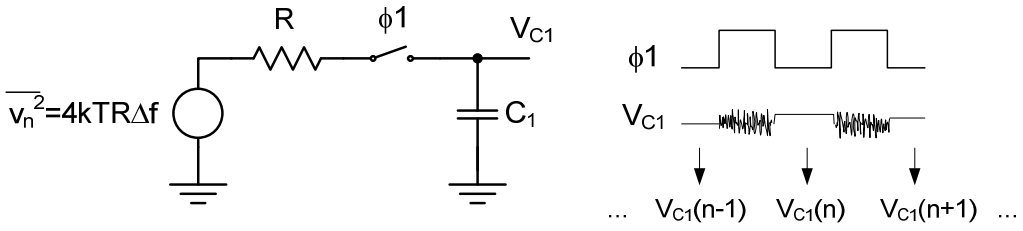
- Unfortunately, this first order result relies on perfectly linear behavior in the amplifiers
- As we will see later, the amplifiers do not settle linearly when large signals are present
- As a result, it turns out that the bandwidth must be overdesigned significantly to meet typical linearity requirements
- We will revisit this question once we have a better handle on the amplifier settling behavior (at the transistor level)
- Everything considered, it turns out that the bandwidth requirements in SC filters are comparable to those in active RC realizations

Noise Analysis Example



- Partition this problem into several steps
  - First understand noise in samples acquired during $\phi 1$
  - Next look at $\phi 2$
    - Average current into infinitely large C_2
    - Noise spectrum and total noise of $\phi 2$ samples with finite C_2

Sampling Circuit



- Questions
  - What is the rms noise in the V_{C1} samples?
  - What is the spectrum of the discrete time sequence representing these samples?

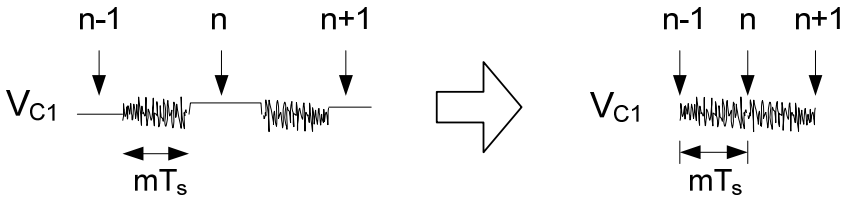
Noise Samples

- The sample values $V_{C1}(n)$ correspond to the instantaneous values of the noise process in $\phi 1$
- From Parseval's theorem, we know that the time-domain power of this process is equal to its power spectral density integrated over all frequencies

$$\frac{\overline{v_{C1}^2}}{\Delta f} = 4kTR \cdot \left| \frac{1}{1+sRC_1} \right|^2$$

$$var\left[V_{C1}(n)\right] = \overline{v_{C1,tot}^2} = \int_0^\infty 4kTR \cdot \left| \frac{1}{1+j2\pi f \cdot RC_1} \right|^2 df = \frac{kT}{C_1}$$

Spectrum of Noise Samples



- Strategy
  - Realize that discrete time noise samples are essentially instantaneous values (mT_s apart) of the continuous time noise process during $\phi 1$
  - Spectrum follows from Fourier transform of the process' autocorrelation function (Wiener-Khintchin)
    - Samples show no correlation → white spectrum
    - Samples are correlated → colored spectrum

Analysis (1)

- Calculate autocorrelation function

Autocorrelation of resistor noise (white) | Impulse response of RC filter | Autocorrelation of filtered noise

$$R_{xx}(\tau) = \delta(0) \cdot 2kTR \longrightarrow \boxed{h(t) = \frac{1}{RC} e^{-t/RC}} \longrightarrow R_{yy}(\tau) = R_{xx}(\tau) * h(\tau) * h(-\tau)$$

$$R_{yy}(\tau) = \frac{kT}{C_1} e^{-\frac{|\tau|}{RC}}$$

$$\therefore R_{yy}(n) = \frac{kT}{C_1} e^{-\frac{|n \cdot mT_s|}{RC}}$$

Covariance of samples separated by n clock cycles

Analysis (2)

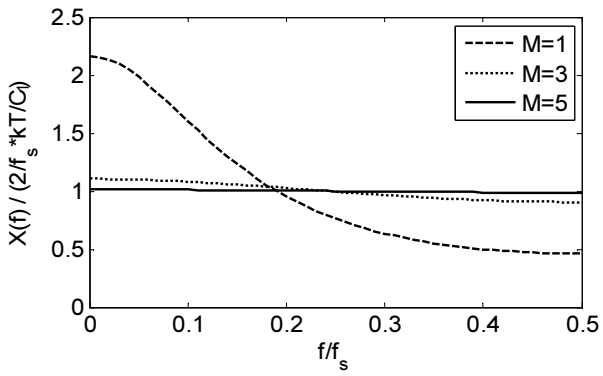
- Apply discrete time Fourier transform

$$X(\omega) = \sum_{-\infty}^{\infty} R_{yy}(n) e^{j\omega \cdot nT_s}$$

$$X(f) = \frac{2}{f_s} \frac{kT}{C_1} \frac{1 - e^{-2M}}{1 - 2e^{-M} \cos\left(2\pi \frac{f}{f_s}\right) + e^{-2M}}$$

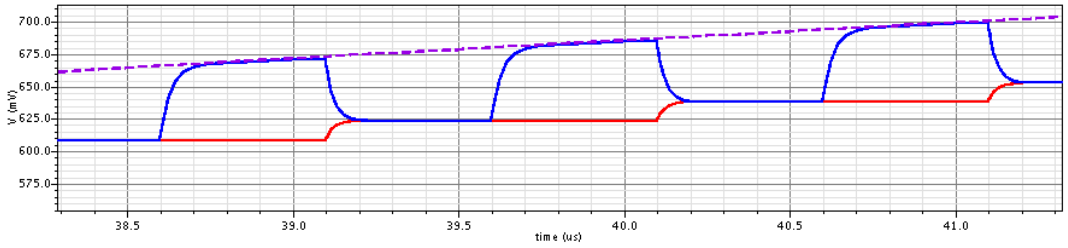
$$M = \frac{mT_s}{RC_1}$$

"number of time constants in mT_s"



Spectrum of noise samples is essentially "white" for M>3

Example Waveforms



$$M = \frac{mT_s}{RC_1} = \frac{0.4 \cdot 1\mu s}{100k\Omega \cdot 314fF} \cong 12$$

- Large M (small RC_1) means that the waveform "settles" accurately to the present input; the previous state is lost
- Means that noise from cycle to cycle is uncorrelated → white spectrum

"Noise Folding" (1)

- The noise PSD of the samples is approximately

$$PSD_S = \frac{2}{f_s}\frac{kT}{C_1}$$

- The noise PSD of the resistor that causes the noise is

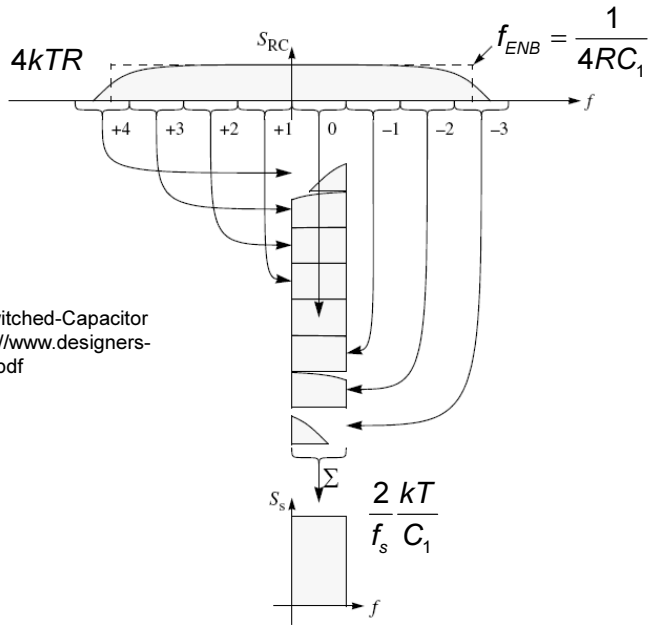
$$PSD_R = 4kTR$$

- The ratio of the two PSDs is

$$\frac{PSD_S}{PSD_R} = \frac{1}{2f_s}\frac{1}{RC_1} = \frac{M}{2m} = M \quad for \quad m = 0.5$$

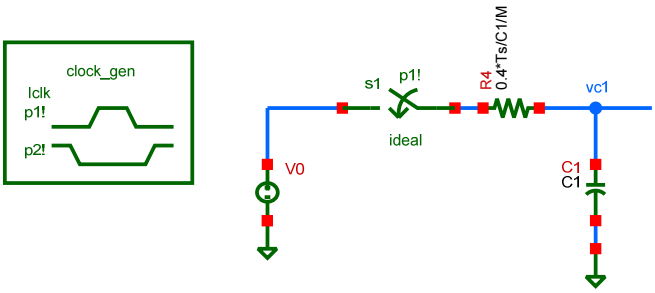
- This increase in the noise PSD is due to aliasing or "folding" of noise from higher frequencies into the band from 0…$f_s/2$

“Noise Folding” (2)



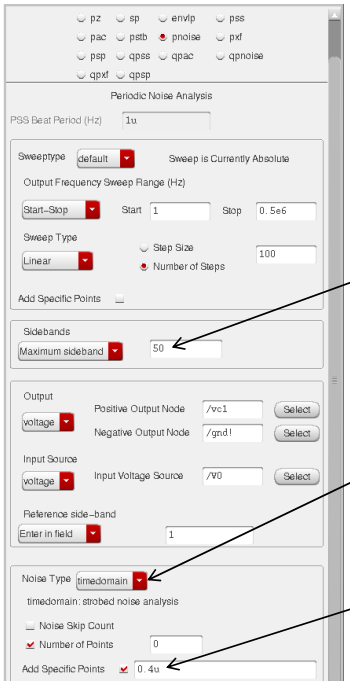
Ken Kundert, “Simulating Switched-Capacitor Filters with SpectreRF,” http://www.designers-guide.org/Analysis/sc-filters.pdf

Simulation Schematic



C_1 = 1pF
T_s = 1us
M = 1, 3, 5, 7

PNOISE Setup



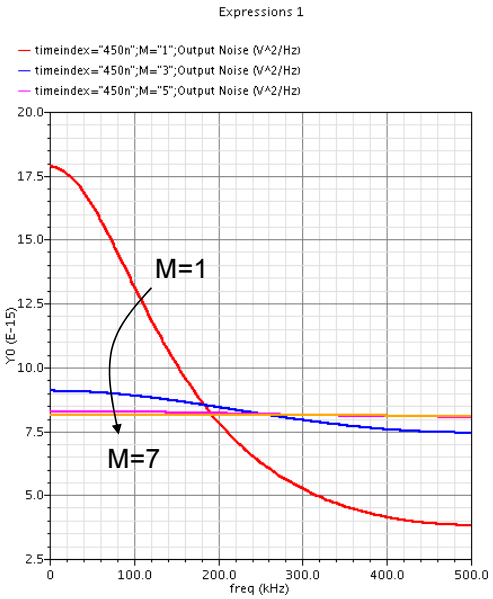
"Number of sidebands" – typically ~20…200 to handle noise folding properly. Fast switches → more sidebands needed. Be sure to set "maxacfrequency" in the PSS analysis options to a correspondingly large value.

"timedomain" means simulator computes spectrum of discrete time noise samples (no need to correct for "sinc")

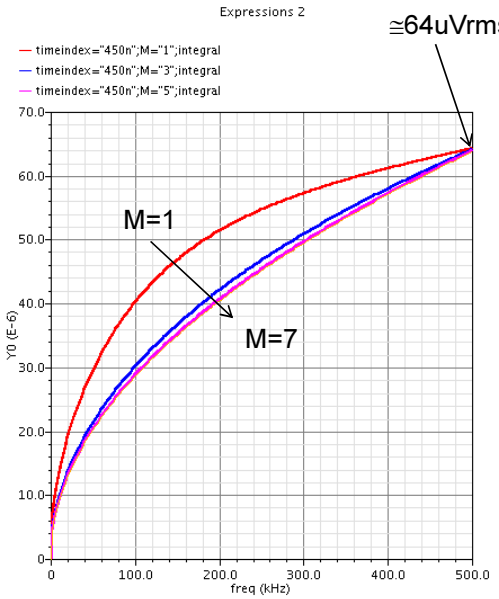
sampling instant

Simulation Result

Noise PSD

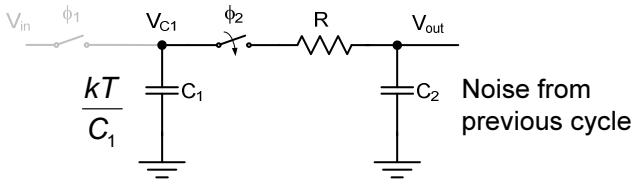


Noise Integral



Back to Lowpass Example

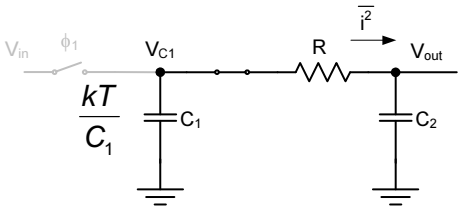
- Circuit in non-overlap phase between $\phi 1$ and $\phi 2$:



- During $\phi 2$, the following will happen
  - Noise charge on C_1 will redistribute
  - Noise from previous cycle stored on C_2 will redistribute
  - Noise generated by R will move charge back and forth between C_1 and C_2

Simplified Analysis (1)

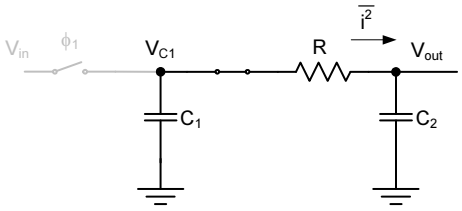
- Goal: Calculate rms noise current into C_2, assuming $C_2 \rightarrow$ infinity
  - V_{out} is essentially a "virtual ground"



- At the end of ϕ_2, C_1 will be completely discharged, and therefore

$$\overline{i_{C1}^2} = \frac{Q_{C1}^2}{T_s^2} = \frac{kTC_1}{T_s^2}$$

Simplified Analysis (2)



- The noise from R induces a noise charge of kTC_1 on C_1
  - This noise is separate and independent of the noise that was already stored on C_1 (from $\phi 1$)

$$\overline{i_R^2} = \frac{Q_{C1}^2}{T_s^2} = \frac{kTC_1}{T_s^2} \qquad \overline{i^2} = \overline{i_{C1}^2} + \overline{i_R^2} = 2kTC_1 f_s^2$$

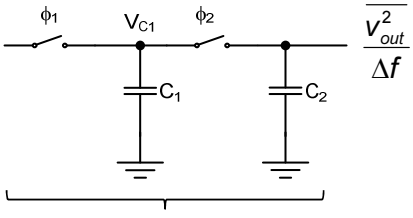
$$\frac{\overline{i^2}}{\Delta f} = 2kTC_1 f_s^2 \frac{2}{f_s} = 4kTC_1 f_s = 4kT\frac{1}{R_{avg}}$$

Noise PSD in $f_s/2$ is the same as that of a physical resistor!

Elaborate Analysis (1)

- The previous result indicates that (at least for $C_2 \rightarrow$ infinity) a switched capacitor behaves roughly like a resistor in terms of the average noise current
- In order to compute the spectrum of the noise samples taken at $\phi 2$ more work is needed
- First, take a closer look at the $\phi 1$ noise and realize that we can directly refer its PSD to the input
  - Allows us to re-use the transfer function that we already know

Input PSD $\frac{\overline{v_{in}^2}}{\Delta f} \cong \frac{kT}{C_1}\frac{2}{f_s}$



$\frac{\overline{v_{out}^2}}{\Delta f}$ Output PSD

noiseless

Elaborate Analysis (2)

$$H(j\omega) = \frac{v_{out}}{v_{in}} = \frac{e^{-j\omega\frac{T_s}{2}}}{1+\frac{C_2}{C_1}\left(1-e^{-j\omega T_s}\right)}$$

$$\frac{\overline{v_{out}^2}}{\Delta f} = \frac{\overline{v_{in}^2}}{\Delta f}\cdot\left|\frac{e^{-j\omega\frac{T_s}{2}}}{1+\frac{C_2}{C_1}\left(1-e^{-j\omega T_s}\right)}\right|^2 \cong \frac{\overline{v_{in}^2}}{\Delta f}\left|\frac{1}{1+j\omega R_{avg}C_2}\right|^2 \qquad R_{avg} = \frac{T_s}{C_1}$$

$$\overline{v_{out}^2} \cong \int_0^\infty \frac{\overline{v_{in}^2}}{\Delta f}\cdot\left|\frac{1}{1+j\omega R_{avg}C_2}\right|^2 df = \frac{\overline{v_{in}^2}}{\Delta f}\frac{1}{4R_{avg}C_2}$$

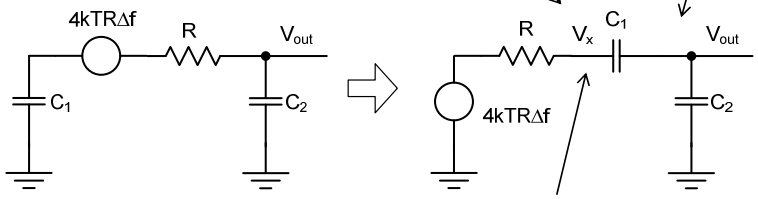
$$\cong \frac{kT}{C_1}\cdot\frac{2}{f_s}\cdot\frac{f_sC_1}{4C_2} = \frac{1}{2}\frac{kT}{C_2}$$

- At the output, the noise from $\phi 1$ is lowpass filtered and contributes a total output noise of approximately $1/2 \cdot kT/C_2$

Elaborate Analysis (3)

- Next look at noise introduced during $\phi 2$

$$\overline{v_x^2} = \frac{kT}{\left(\frac{C_1C_2}{C_1+C_2}\right)} \qquad \overline{v_{out}^2} = \frac{kT}{\left(\frac{C_1C_2}{C_1+C_2}\right)}\left(\frac{C_1}{C_1+C_2}\right)^2$$



$$\overline{q_x^2} = kT\left(\frac{C_1C_2}{C_1+C_2}\right)$$

Elaborate Analysis (4)

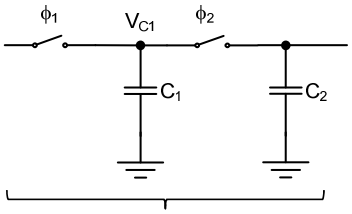
- The final noise charge q_x can be referred to an equivalent $\phi 1$ noise charge on C_1, and subsequently referred to the input

$$\overline{V_{C1}{}^2} = \frac{\overline{q_x{}^2}}{\left(\frac{C_2}{C_1+C_2}\right)^2}\frac{1}{C_1{}^2} = \frac{kT\left(\frac{C_1C_2}{C_1+C_2}\right)}{\left(\frac{C_2}{C_1+C_2}\right)^2}\frac{1}{C_1{}^2} = \frac{kT}{C_1}\left(\frac{C_1+C_2}{C_2}\right) \cong \frac{kT}{C_1}$$

- Complete model

$$\frac{\overline{v_{in}^2}}{\Delta f} \cong 2\frac{kT}{C_1}\frac{2}{f_s}$$

White input PSD



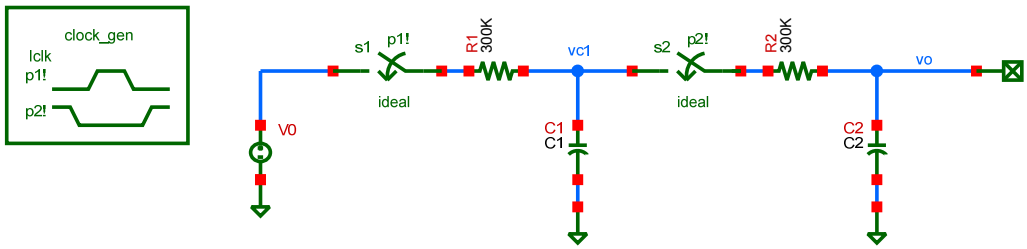
noiseless

$$\frac{\overline{v_{out}^2}}{\Delta f} \cong \frac{\overline{v_{in}^2}}{\Delta f}\left|\frac{1}{1+j\omega R_{avg}C_2}\right|^2$$

Colored output PSD

$$\Rightarrow \overline{v_{out}^2} = \frac{kT}{C_2}$$

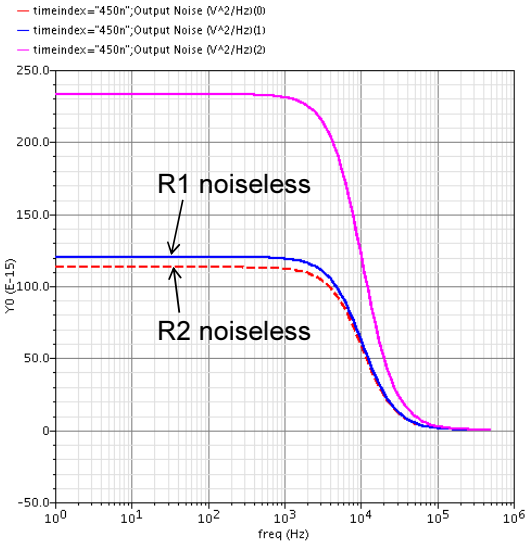
Lowpass Simulation Circuit



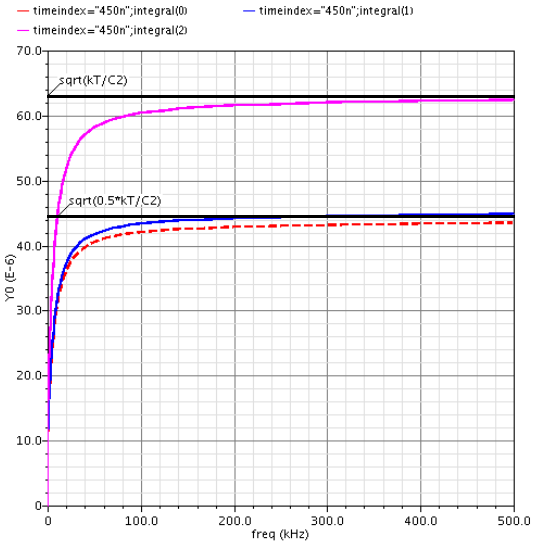
C_1 = 68.83 fF
C_2 = 1 pF
f_s = 1 MHz
f_{-3dB} = 10 kHz

Simulation Result

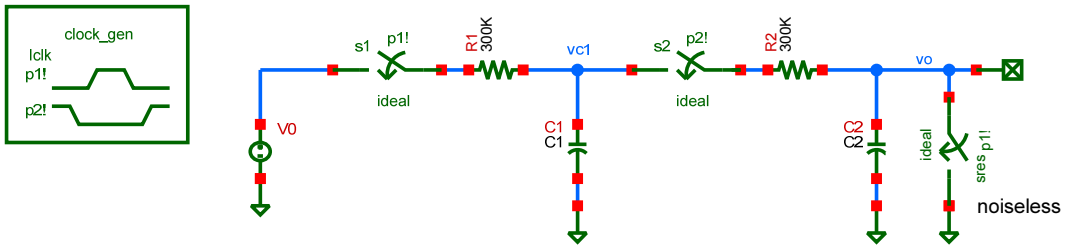
Noise PSD



Noise Integral



Experiment: Reset Output During $\phi 1$

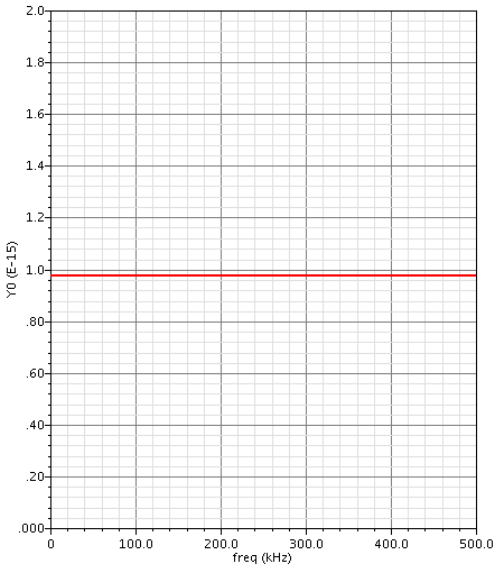


- Expecting to see
  - White noise spectrum
  - Total integrated noise power equal to

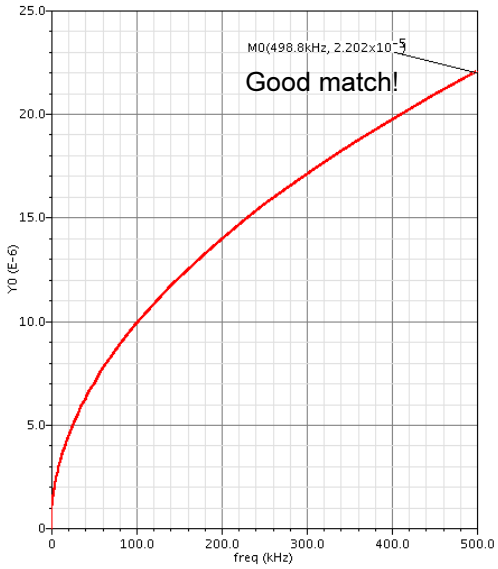
$$\overline{v_{out}^2} = \underbrace{\frac{kT}{C_1}\left(\frac{C_1}{C_1+C_2}\right)^2}_{\phi 1 \text{ noise referred to output}} + \underbrace{\frac{kT}{\left(\frac{C_1C_2}{C_1+C_2}\right)}\left(\frac{C_1}{C_1+C_2}\right)^2}_{\phi 2 \text{ noise}} = 21.7\mu Vrms$$

Simulation Result

Noise PSD



Noise Integral



SC Filter Summary

- Pole and zero frequencies are proportional to sampling frequency and capacitor ratios
  - High accuracy and stability in response
  - Large time constants realizable without large R, C
- Compatible with operational transconductance amplifiers; no need to drive resistive loads
- Amplifier gain and BW requirements comparable to active RC
- Noise
  - SC resistor emulation has same noise as an actual resistor
  - Arguing about amplifier noise requires detailed analysis
    - Special issue in SC circuits: noise aliasing
- SC filters typically require continuous time anti-aliasing and reconstruction filters
  - Sometimes first order RC will suffice, particularly for large f_s

References (1)

- **R. Gregorian, K.W. Martin, and G.C. Temes, “Switched-Capacitor Circuit Design,” Proceedings of the IEEE, vol. 71, no. 8, pp. 941-966, Aug. 1983**
- D.L. Fried, "Analog sample-data filters," IEEE J. Solid-State Circuits, vol. 7, no. 4, pp. 302-304, Aug. 1972
- D. Senderowicz et al., “A Family of Differential NMOS Analog Circuits for PCM Codec Filter Chip,” IEEE J. Solid-State Circuits, pp.1014-1023, Dec. 1982
- T.C. Choi, "High-Frequency CMOS Switched-Capacitor Filters," UC Berkeley, Ph.D. Thesis, May 1983 (ERL Memorandum No. UCB/ERL M83/31)
- B.-S. Song and P.R. Gray "Switched-Capacitor High-Q Bandpass Filters for IF Applications," IEEE J. Solid-State Circuits, pp. 924-933, Dec. 1986
- K. Martin and A. Sedra, "Effects of the op amp finite gain and bandwidth on the performance of switched-capacitor filters," IEEE Trans. Circuits and Systems, vol. 28, no. 8, pp. 822-829, Aug. 1981
- K.L. Lee, “Low Distortion Switched-Capacitor Filters," UC Berkeley, Ph.D. Thesis, Feb. 1986 (ERL Memorandum No. UCB/ERL M86/12)

References (2)

- K. Martin and A.S. Sedra, “Stray-insensitive switched-capacitor filters based on the bilinear z transform,” Electronics Letters, vol. 19, pp. 365-366, June 1979
- R. Castello, and P.R. Gray, "A high-performance micropower switched-capacitor filter," IEEE J. Solid-State Circuits, vol. 20, no. 6, pp. 1122-1132, Dec. 1985
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- C.-A. Gobet and A. Knob, "Noise analysis of switched capacitor networks," IEEE Trans. Circuits and Systems, vol. 30, no. 1, pp. 37-43, Jan 1983
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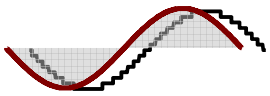
- R. Schreier, et al., "Design-oriented estimation of thermal noise in switched-capacitor circuits," IEEE Trans. Circuits and Systems I, vol. 52, no. 11, pp. 2358-2368, Nov. 2005
- K. Kundert, “Simulating Switched-Capacitor Filters with SpectreRF,” http://www.designers-guide.org/Analysis/sc-filters.pdf

Operational Transconductance Amplifier Design



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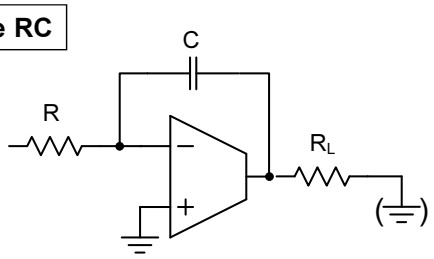
Outline

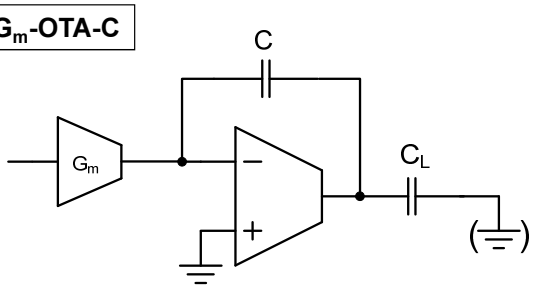
- Basic considerations
  - Application requirements for OTAs used in filters
  - The case for fully differential circuits
- Transistor models, g_m/I_D-based design
- Single-stage OTAs
  - Basic differential pair
  - Telescopic architecture
  - Folded cascode architecture
- Two-stage OTA
- Advanced techniques
  - Gain boosting
- Common mode feedback implementation

OTA Application in Filters

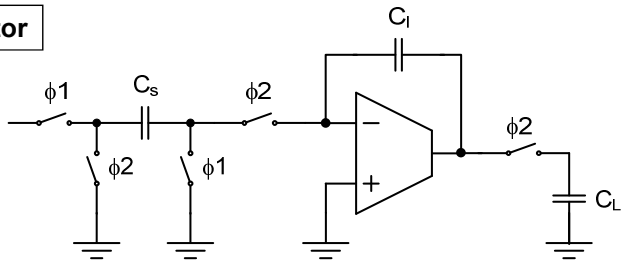
Active RC



G_m-OTA-C



Switched Capacitor



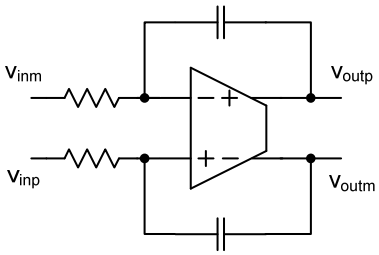
Requirements (1)

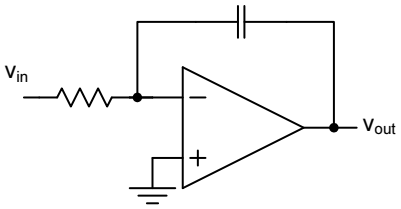
	Active RC	G_m-OTA-C	SC
High gain	X	X	X
Low noise	X	X	X
High BW	X	X	X
Capacitive loads	X	X	X
Resistive loads	X		
Fast settling			X

Requirements (2)

- Special requirements in active-RC and SC circuits
  - Tend to narrow design space
- Active RC → resistive loads
  - Difficult to achieve sufficient gain with a single-stage OTA
- SC → fast transient settling
  - Must stay away from “tricks” such as pole-zero cancellation
    - Pole zero doublets can cause long setting tails (more later)
  - Hard to achieve fast settling for three or more stages
- We will take these issues into account as we discuss the various OTA implementation styles

Fully Differential vs. Single Ended

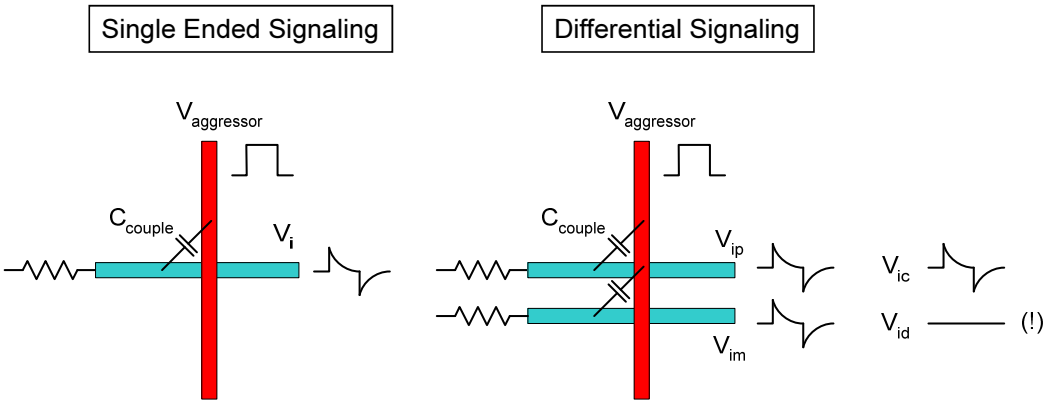




- Symmetrical
  - Immune to coupling and power supply noise
  - Easy to analyze
- Can invert signal via wire crossing
- Requires common mode feedback (CMFB)

- Lower complexity (component count)
- Can build non-inverting unity gain buffer without using any feedback components

Coupling Noise

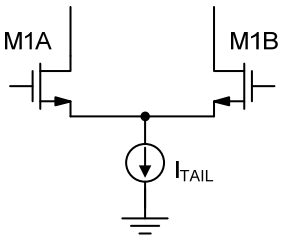


- Similar arguments can be made regarding the rejection of supply noise, ground bounce, substrate noise, etc.

Fully Differential vs. Single Ended

- Most precision analog integrated circuits are based on fully differential stages
  - Filters, data converters, etc.
- In contrast, printed circuit board circuits tend to be single ended
  - Want minimum complexity and component count
- Since this course (and also EE315B) emphasizes integrated circuit design, we will tailor our analyses toward fully differential implementations

Transistor Sizing

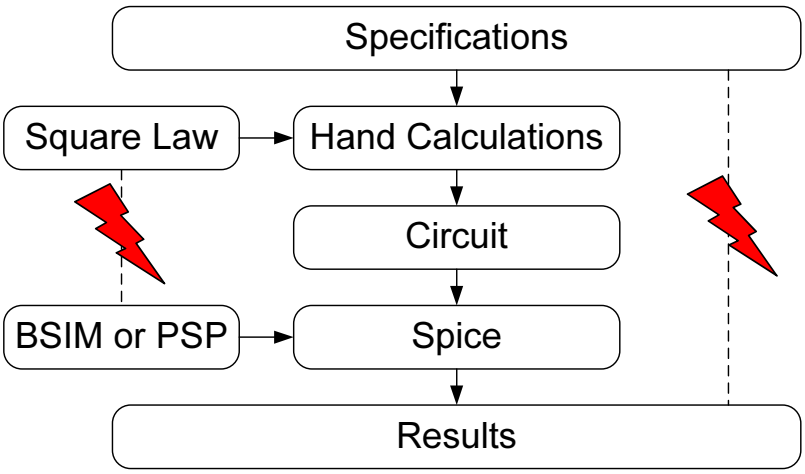


$$G_m = g_{m1a} = g_{m1b}$$

- Typical problem
  - Want to realize a certain amount of g_m
  - Need to determine W, L, I_{TAIL}
- Classical square-law equations are very inaccurate for modern technologies

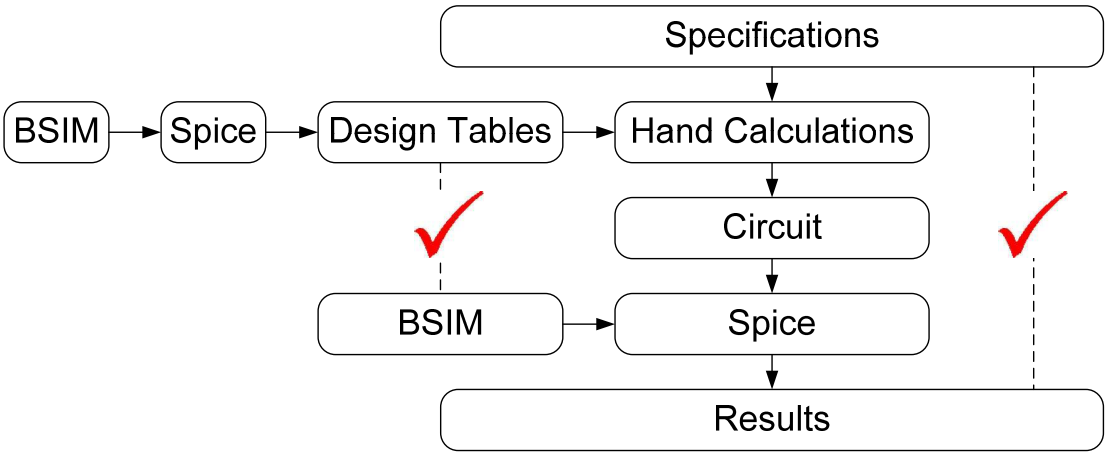
$$g_m = \sqrt{2 I_D \mu C_{ox} \frac{W}{L}}$$

The Problem



- Since there is a disconnect between actual transistor behavior and the simple square law model, any square-law driven design optimization will be far off from Spice results

The Solution



- Use pre-computed spice data in hand calculations

Simulation Data in Matlab

```
% data stored in /usr/class/ee315a/matlab
>> load 180nch.mat;
>> nch
nch =
     ID: [4-D double]
     VT: [4-D double]
     GM: [4-D double]
    GMB: [4-D double]
    GDS: [4-D double]
    CGG: [4-D double]
    CGS: [4-D double]
    CGD: [4-D double]
    CGB: [4-D double]
    CDD: [4-D double]
    CSS: [4-D double]
    VGS: [73x1 double]
    VDS: [73x1 double]
     VS: [11x1 double]
      L: [22x1 double]
      W: 5

>> size(nch.ID)

ans =
    22    73    73    11
```

Four-dimensional arrays

$$I_D(L, V_{GS}, V_{DS}, V_S)$$

$$V_t(L, V_{GS}, V_{DS}, V_S)$$

$$g_m(L, V_{GS}, V_{DS}, V_S)$$

...

Lookup Function (For Convenience)

```
>> lookup(nch, 'ID', 'VGS', 0.5, 'VDS', 0.5)
ans =
  8.4181e-006

>> help lookup

  The function "lookup" extracts a desired subset from the 4-dimensional
  simulation data. The function interpolates when the requested points lie off
  the simulation grid.

    There are three basic usage modes:
    (1) Simple lookup of parameters at given (L, VGS, VDS, VS)
    (2) Lookup of arbitrary ratios of parameters, e.g. GM_ID, GM_CGG at given
        (L, VGS, VDS, VS)
    (3) Cross-lookup of one ratio against another, e.g. GM_CGG for some GM_ID

    In usage scenarios (1) and (2) the input parameters (L, VGS, VDS, VS) can be
    listed in any order and default to the following values when not specified:

    L = min(data.L); (minimum length used in simulation)
    VGS = data.VGS; (VGS vector used during simulation)
    VDS = max(data.VDS)/2; (VDD/2)
    VS = 0;
```


Figures of Merit for Design

Square Law

- Transconductance efficiency
  - Want large g_m, for as little current as possible

$$\boxed{\frac{g_m}{I_D}} = \frac{2}{V_{OV}}$$

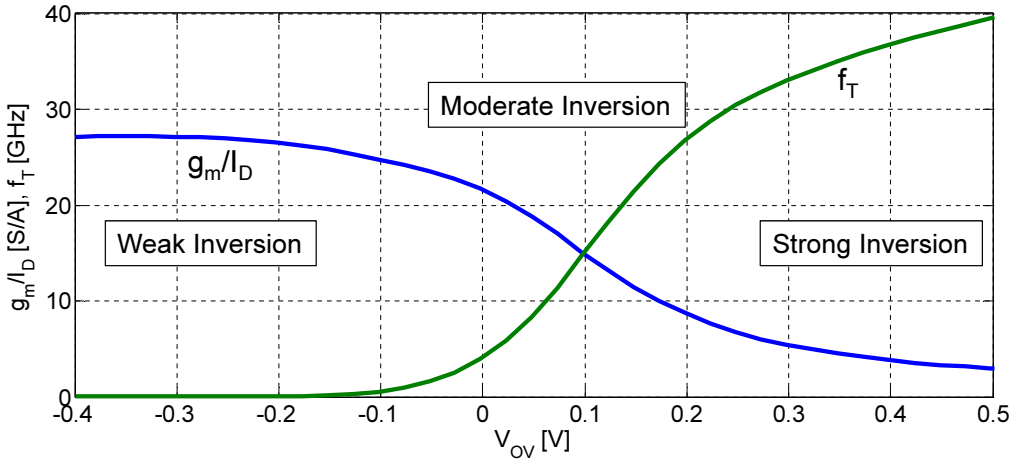
- Transit frequency
  - Want large g_m, without large C_{gg}

$$\boxed{\frac{g_m}{C_{gg}}} \cong \frac{3}{2}\frac{\mu V_{OV}}{L^2}$$

- Intrinsic gain
  - Want large g_m, but no g_o

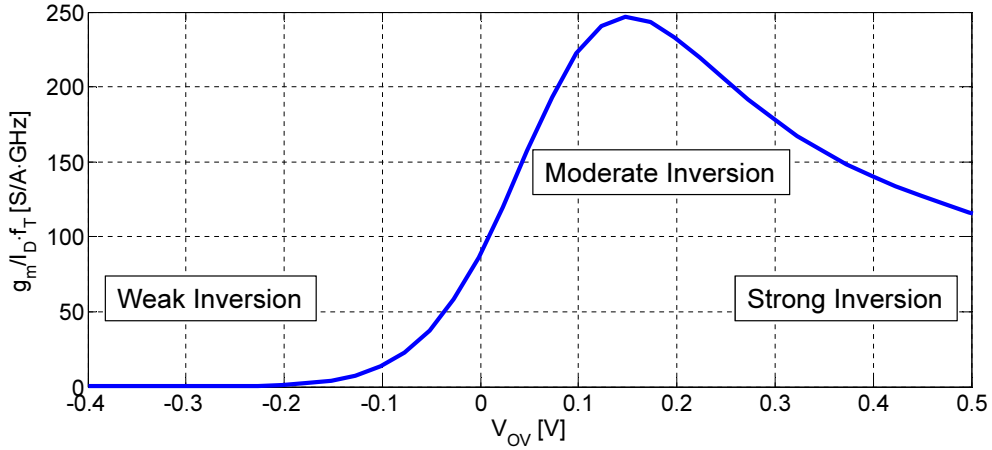
$$\boxed{\frac{g_m}{g_o}} \cong \frac{2}{\lambda V_{OV}}$$

Design Tradeoff: g_m/I_D and f_T



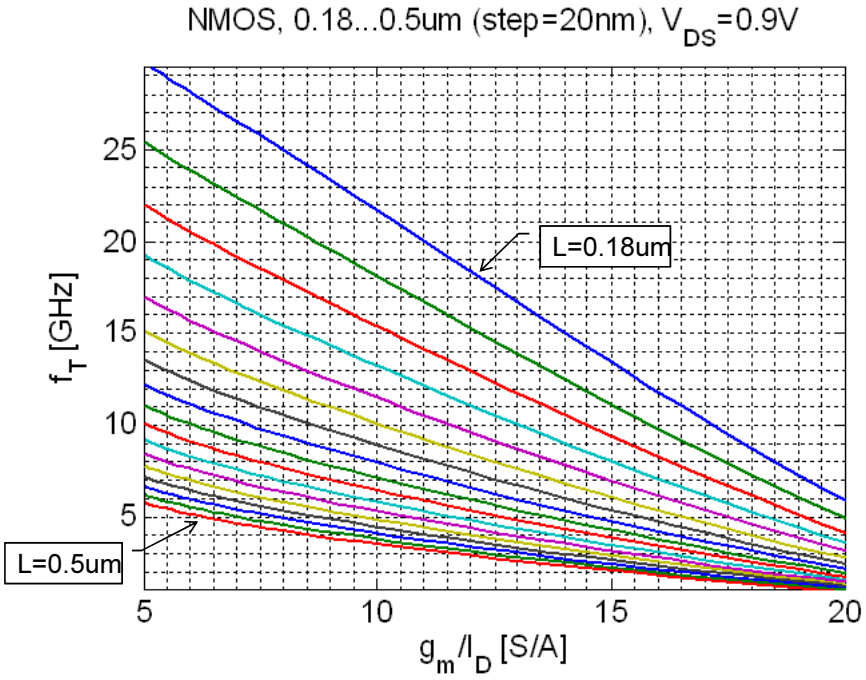
- Weak inversion: Large g_m/ID (>20 S/A), but small f_T
- Strong inversion: Small g_m/ID (<10 S/A), but large f_T

Product of g_m/I_D and f_T

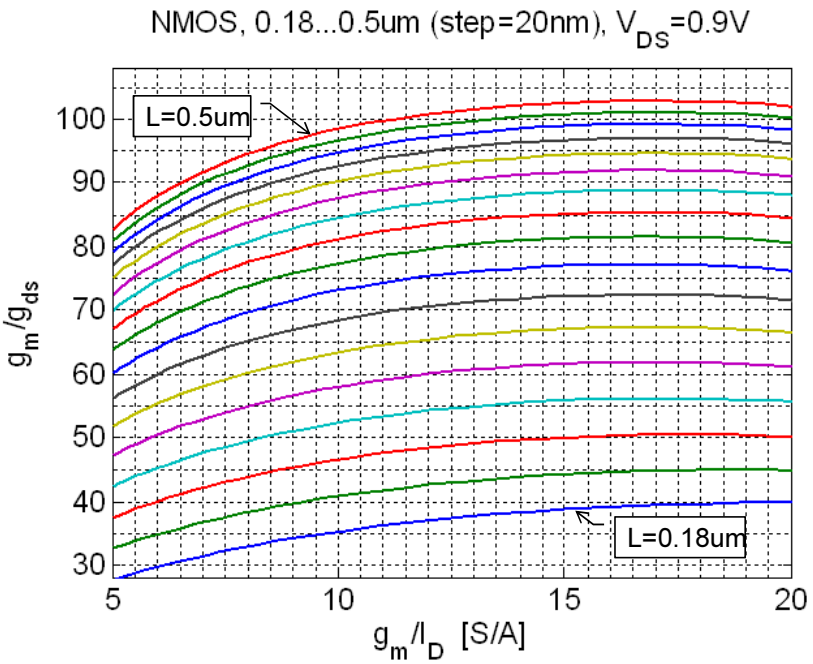


- Interestingly, the product of g_m/I_D and f_T peaks in moderate inversion
- Operating the transistor in moderate inversion is optimal when we value speed and power efficiency equally
  - Not always the case

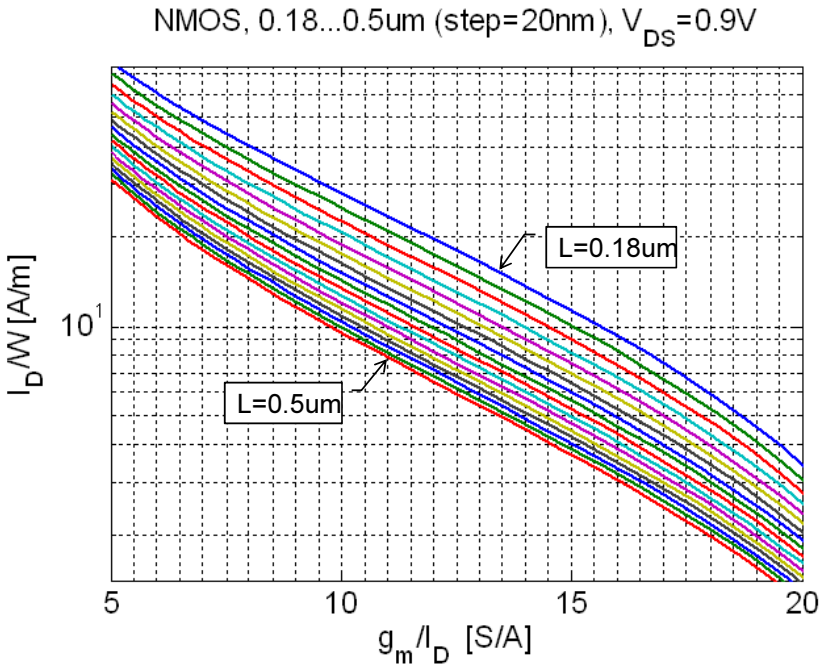
Transit Frequency Chart



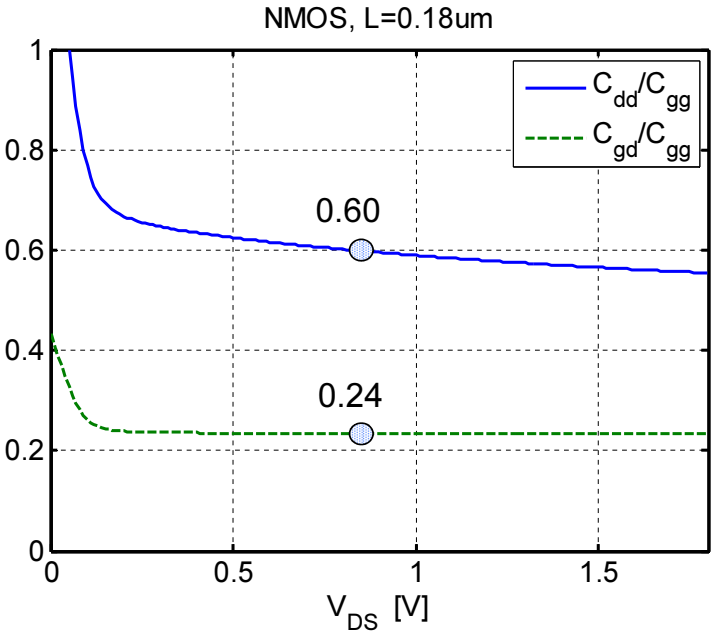
Intrinsic Gain Chart



Current Density Chart



Extrinsic Capacitances



- Typically OK to work with estimates taken at $V_{DD}/2$

Generic Design Flow

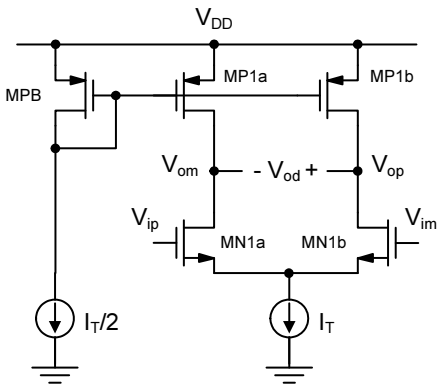
1) Determine g_m (from design objectives)
2) Pick L
   - Short channel → high f_T (high speed)
   - Long channel → high intrinsic gain
3) Pick g_m/I_D (or f_T)
   - Large g_m/I_D → low power, large signal swing, low $V_{DSsat} \cong 2/(g_m/I_D)$
   - Small g_m/I_D → high f_T (high speed)
4) Determine I_D (from g_m and g_m/I_D)
5) Determine W (from I_D/W)

Many other possibilities exist (depending on circuit specifics, design constraints and objectives)

Basic Differential Pair OTA

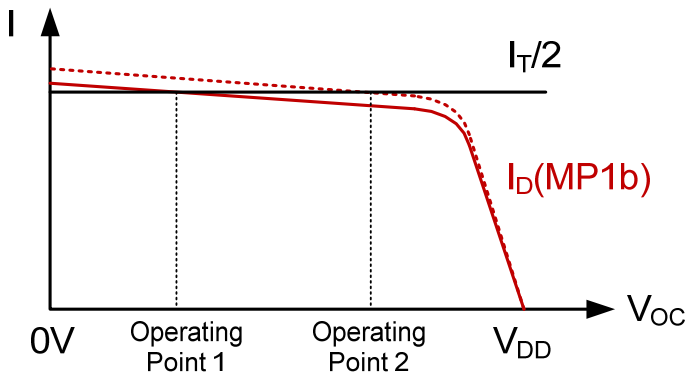
- Common mode feedback
- Half circuit model
- Return ratio analysis
  - Loop gain
  - Closed-loop gain
- Noise analysis
- Step response
  - Linear settling
  - Slewing

Basic Differential Pair OTA



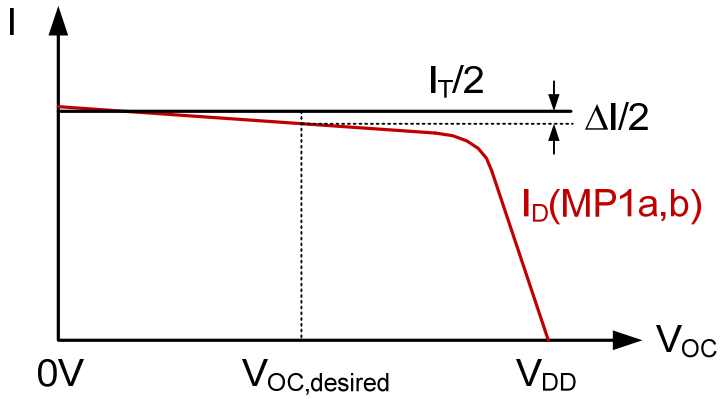
- Suppose that in the operating point $V_{ip}=V_{im}$, i.e. $V_{id}=0$
- What is the output common mode voltage $V_{oc} = (V_{om}+V_{op})/2$?

Operating Point Sensitivity



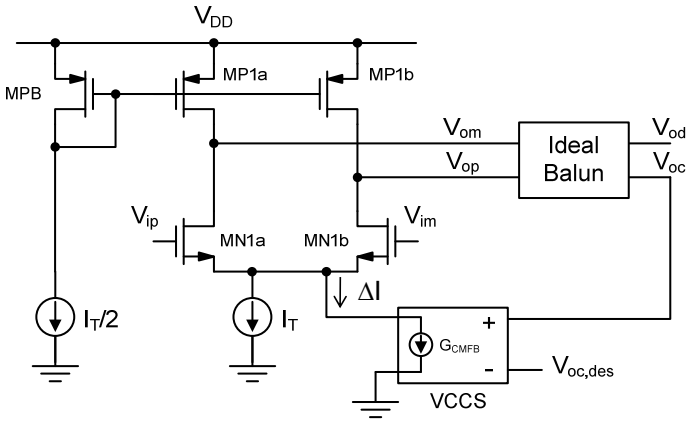
- The operating point is very sensitive to small changes in the device characteristics
- Solution: Common mode feedback (CMFB)

CMFB



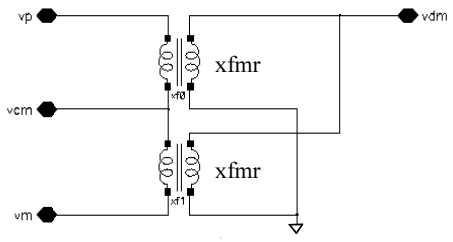
- Common mode feedback loop adjusts ΔI such that V_{OC} is very close to the desired voltage

Idealized CMFB Implementation



$$V_{oc} = V_{oc,des} + \frac{\Delta I}{G_{CMFB}} = V_{oc,des} \quad for \quad G_{CMFB} \rightarrow \infty$$

Ideal Balun

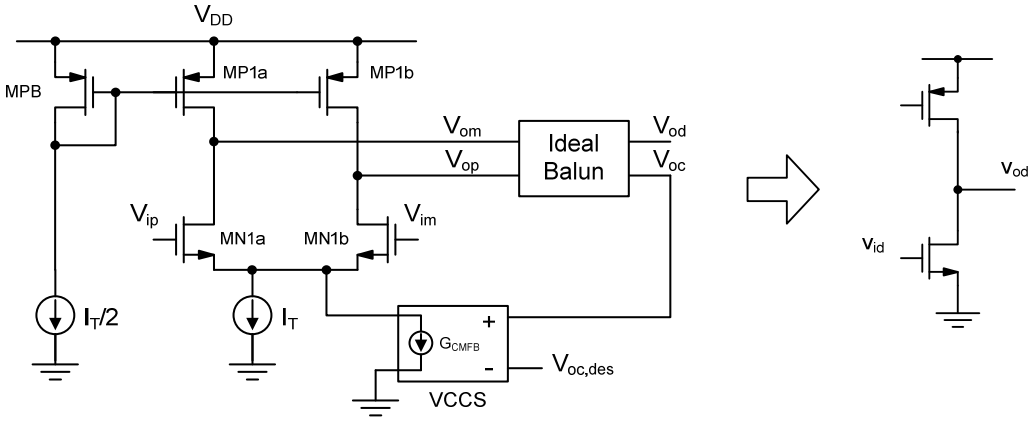


- Useful for separating common mode and differential mode signal components
- Bi-directional, preserves port impedances
- Uses ideal inductorless transformers that work down to DC

CMFB Implementation

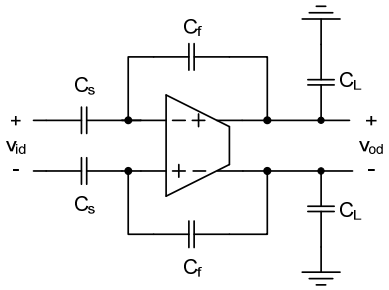
- In practice, we won't be able to let $G_{CMFB} \rightarrow \infty$ for loop stability
  - Nonetheless, the loop will get us to within a few mV of where we need to be
  - And most importantly help absorb variations in the device characteristics
- In the first few lectures on OTA design, we will use the idealized common mode feedback circuit (as shown previously) to avoid distraction from the main design task
- Practical CMFB implementation examples (using transistors) will follow later in this course

Differential Mode Small Signal Half Circuit



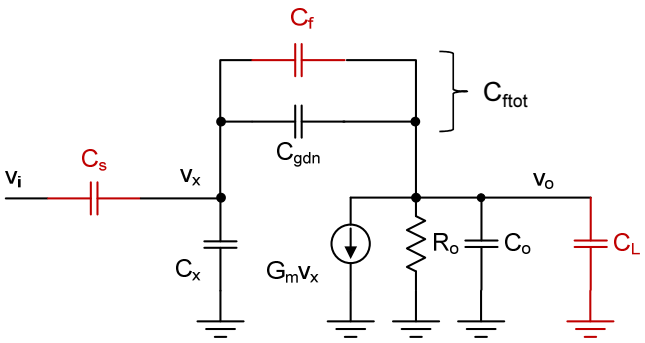
- With the circuit at the proper operating point, we can analyze its small-signal behavior using a differential mode half circuit model
- Note that (to first order) the CMFB loop does not influence the behavior of the differential mode signals

OTA with Capacitive Feedback



- Let's get started by placing our simple OTA into a capacitive feedback loop (as encountered e.g. in an SC circuit)
- Questions
  - What is the phase margin?
  - What is the closed loop transfer function?
  - What is the total integrated noise?
  - How fast does this circuit settle (in response to a step)?

Half Circuit Model



$$G_m = g_{mn}$$

$$R_O = r_{op} || r_{on}$$

$$C_O = C_{dbp} + C_{dbn}$$

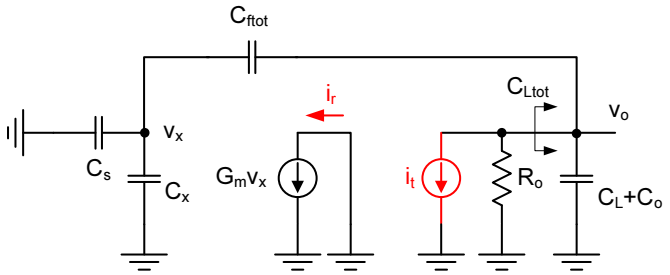
$$C_X = C_{gsn} + C_{gbn}$$

Return Ratio Analysis

$$v_X = \beta \cdot v_O$$

$$\beta = \frac{C_{ftot}}{C_{ftot} + C_S + C_X}$$

"Feedback factor"



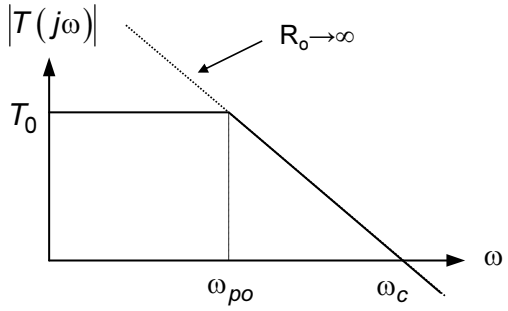
$$v_O = -i_t \cdot \left(R_O || \frac{1}{sC_{Ltot}} \right) \qquad C_{Ltot} = C_L + C_O + (1-\beta) C_{ftot}$$

$$T(s) = -\frac{i_r}{i_t} = \beta \cdot G_m \cdot \left(R_O || \frac{1}{sC_{Ltot}} \right) = \frac{\beta \cdot G_m R_O}{1 + sR_O C_{Ltot}} = \frac{\beta \cdot a_0}{1 + sR_O C_{Ltot}}$$

Frequency Response of T(s)

$$T_0 = \beta G_m R_o$$

$$\omega_{po} = \frac{1}{R_o C_{Ltot}}$$

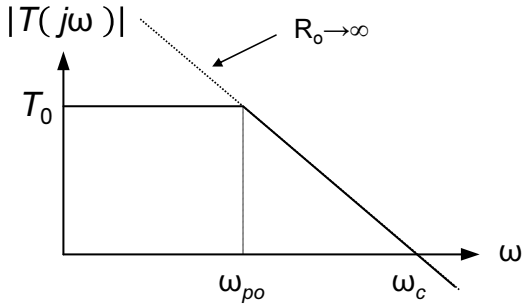


$$T(s) = \frac{\beta G_m R_o}{1 + sR_o C_{Ltot}} = \frac{\beta G_m}{\frac{1}{R_o} + sC_{Ltot}} \cong \frac{\beta G_m}{sC_{Ltot}} \quad for \quad R_o \gg \frac{1}{sC_{Ltot}} \Leftrightarrow \frac{\omega}{\omega_{po}} \gg 1$$

$$\left|\frac{\beta G_m}{j\omega_c C_{Ltot}}\right| = 1 \qquad \boxed{\Rightarrow \omega_c \cong \beta \frac{G_m}{C_{Ltot}}}$$

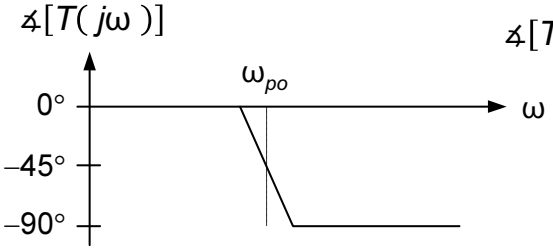
→ R_o is irrelevant for understanding high frequency behavior around ω_c

Phase Margin



$$T(j\omega) = \frac{\beta G_m R_o}{1 + j\frac{\omega}{\omega_{po}}}$$

$$T(j\omega_c) = \frac{\beta G_m R_o}{1 + j\frac{\omega_c}{\omega_{po}}}$$



$$\angle[T(j\omega)]|_{\omega=\omega_c} = -tan^{-1}\left(\frac{\omega_c}{\omega_{po}}\right) \cong -90°$$

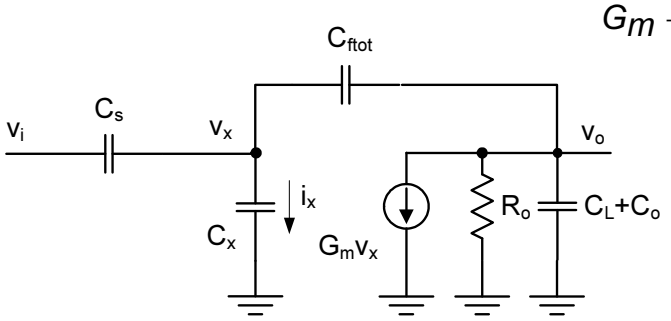
$$\boxed{PM \cong 180° - 90° \cong 90°}$$

Closed Loop Transfer Function

$$A(s) = \frac{v_o}{v_i} = A_\infty \frac{T(s)}{1 + T(s)} + \frac{d}{1 + T(s)}$$

- Need to find A_∞ and d
  - Let's start with A_∞

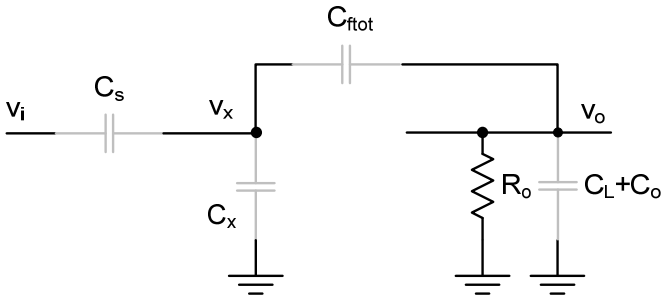
$$G_m \to \infty \quad \Rightarrow v_x \to 0 \quad \Rightarrow i_x \to 0$$



$$0 = v_i s C_S + v_O s C_{ftot}$$

$$A_\infty = \left.\frac{v_o}{v_i}\right|_{G_m \to \infty} = -\frac{C_S}{C_{ftot}}$$

Finding d at Low Frequencies



- Capacitors are open circuits

$$d_0 = \left.\frac{v_o}{v_i}\right|_{G_m=0} = 0$$

Low-Frequency Closed-Loop Gain

$$A_0 = A_\infty \frac{T_0}{1+T_0} + \frac{d_0}{1+T_0} \qquad A_\infty = -\frac{C_S}{C_{ftot}} \qquad T_0 = \beta G_m R_O \qquad d_0 = 0$$

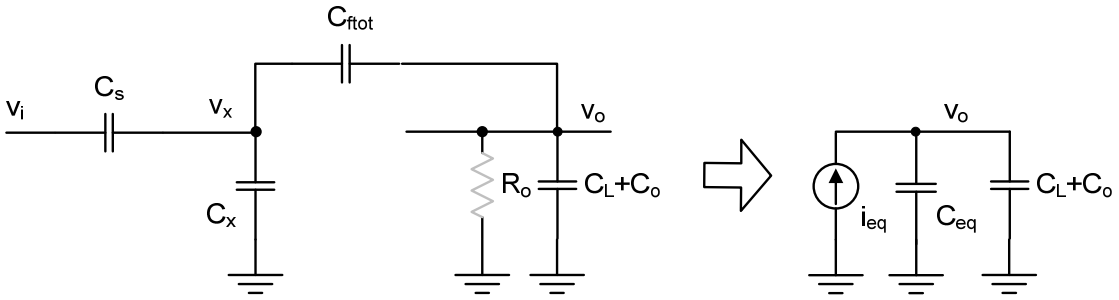
$$\Rightarrow A_0 = -\frac{C_S}{C_{ftot}}\left(\frac{1}{1+\frac{1}{\beta G_m R_O}}\right)$$

- Error in low-frequency closed-loop gain

$$\varepsilon_0 = \frac{A_0 - A_\infty}{A_\infty} = \frac{A_0}{A_\infty} - 1 = \frac{T_0}{1+T_0} - 1 = \frac{1}{1+\frac{1}{T_0}} - 1 \cong \left(1 - \frac{1}{T_0}\right) - 1 = -\frac{1}{T_0}$$

$$\boxed{|\varepsilon_0| \cong \frac{1}{T_0}}$$

d at High Frequencies



$$i_{eq} = v_i \frac{C_s}{C_s + C_x + C_{ftot}} \cdot sC_{ftot} = v_i \beta \cdot sC_s \qquad C_{eq} = (1-\beta)C_{ftot}$$

$$d = \left.\frac{v_o}{v_i}\right|_{G_m=0} = \frac{1}{v_i} \frac{i_{eq}}{s\left(C_{eq} + C_L + C_o\right)} = \beta \frac{C_s}{C_{Ltot}}$$

High-Frequency Closed-Loop Gain (1)

$$A(s) \cong A_\infty \frac{T(s)}{1+T(s)} + \frac{d}{1+T(s)}$$

$$\cong -\frac{C_s}{C_{ftot}} \frac{\frac{\beta G_m}{sC_{Ltot}}}{1+\frac{\beta G_m}{sC_{Ltot}}} + \frac{\frac{\beta C_s}{C_{Ltot}}}{1+\frac{\beta G_m}{sC_{Ltot}}} = -\frac{C_s}{C_{ftot}} \frac{1-s\frac{C_{ftot}}{G_m}}{1+s\frac{C_{Ltot}}{\beta G_m}} = -\frac{C_s}{C_{ftot}} \frac{1-\frac{s}{z}}{1-\frac{s}{p}}$$

- Pole frequency:

$$\omega_p \cong \frac{\beta G_m}{C_{Ltot}} \cong \omega_c \cong \frac{\beta G_m R_o}{R_o C_{Ltot}} \cong T_0 \cdot \omega_{po}$$ As expected.

High-Frequency Closed-Loop Gain (2)

$$A(s) = -\frac{C_s}{C_f} \frac{1-s\frac{C_{ftot}}{G_m}}{1+s\frac{C_{Ltot}}{\beta G_m}} = -\frac{C_s}{C_f} \frac{1-\frac{s}{z}}{1-\frac{s}{p}}$$

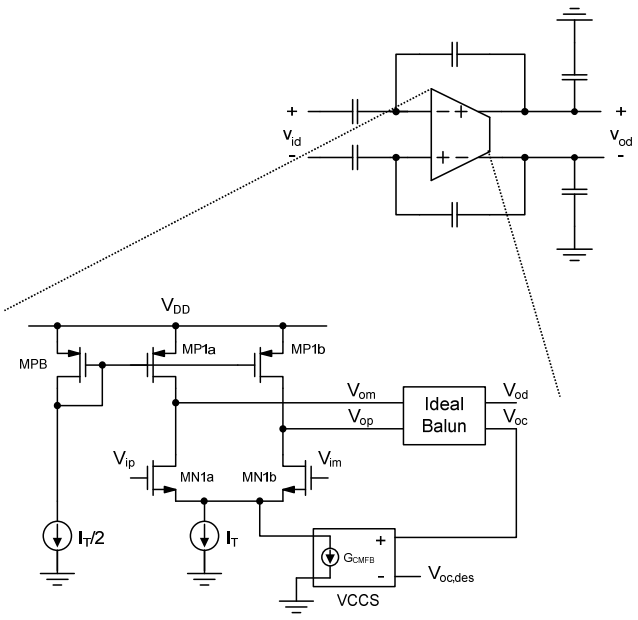
- Zero frequency:

$$\omega_z = \frac{G_m}{C_{ftot}} \qquad \frac{\omega_z}{\omega_p} = \frac{C_{Ltot}}{\beta C_{ftot}} \qquad \textit{usually} >> 1$$

- Therefore, the closed-loop -3dB frequency is approximately

$$\omega_{-3dB} \cong \omega_p \cong \frac{\beta G_m}{C_{Ltot}}$$

Putting it All Together



$$A(s) \cong -\frac{C_s}{C_f}\frac{1}{1+\frac{1}{T_0}}\frac{1-\frac{s}{z}}{1-\frac{s}{p}}$$

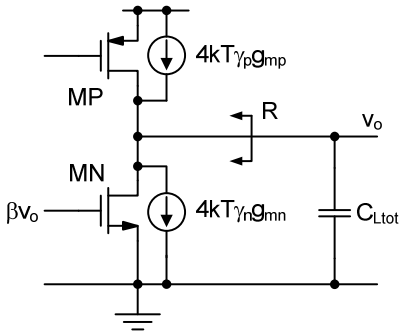
$$T_0 = \beta G_m R_0$$

$$p \cong -\frac{\beta G_m}{C_{Ltot}}$$

$$z \cong +\frac{G_m}{C_{ftot}}$$

$$\beta = \frac{C_{ftot}}{C_{ftot} + C_s + C_x}$$

Noise Analysis (1)



$$R \cong \frac{1}{\beta g_{mn}}$$

Neglecting finite output resistance of the MOSFETs

$$\frac{\overline{v_o^2}}{\Delta f} = 4kT\left(\gamma_n g_{mn} + \gamma_p g_{mp}\right)\cdot\left|R\right\|\frac{1}{j\omega C_{Ltot}}\Bigg|^2$$

$$= 4kT\gamma_n g_{mn}\left(1+\frac{\gamma_p g_{mp}}{\gamma_n g_{mn}}\right)\cdot\left|\frac{R}{1+j\omega RC_{Ltot}}\right|^2$$

Noise Analysis (2)

$$\overline{v_o^2} = \int_0^\infty 4kT\gamma_n g_{mn}\left(1+\frac{\gamma_p g_{mp}}{\gamma_n g_{mn}}\right)\cdot\left|\frac{R}{1+j\omega RC_{Ltot}}\right|^2 df$$

$$= 4kT\gamma_n g_{mn}\left(1+\frac{\gamma_p g_{mp}}{\gamma_n g_{mn}}\right)\cdot R^2\cdot\frac{1}{4RC_{Ltot}}$$

$$= 4kT\gamma_n g_{mn}\left(1+\frac{\gamma_p g_{mp}}{\gamma_n g_{mn}}\right)\cdot\frac{1}{\beta g_{mn}}\cdot\frac{1}{4C_{Ltot}}$$

$$= \frac{1}{\beta}\frac{kT}{C_{Ltot}}\gamma_n\left(1+\underbrace{\frac{\gamma_p g_{mp}}{\gamma_n g_{mn}}}\right)$$

Noise due to active load

Noise Analysis (3)

- For low noise
  - Make g_{mp} as small as possible, i.e. use small g_m/I_D for active load device
    - Issue: Smaller g_m/I_D means larger "V_{dsat}" i.e. less available voltage swing
  - Maximize feedback factor β

$$\beta = \frac{C_{ftot}}{C_{ftot}+C_s+C_x} = \frac{1}{1+\frac{C_s}{C_{ftot}}+\frac{C_x}{C_{ftot}}} \cong \frac{1}{1+|A_\infty|+\frac{C_{ggn}}{C_{ftot}}} = \frac{1}{1+|A_\infty|+\frac{g_{mn}}{C_{ftot}}\frac{1}{\omega_T}}$$

Want $\omega_t \rightarrow \infty$ (short channel)

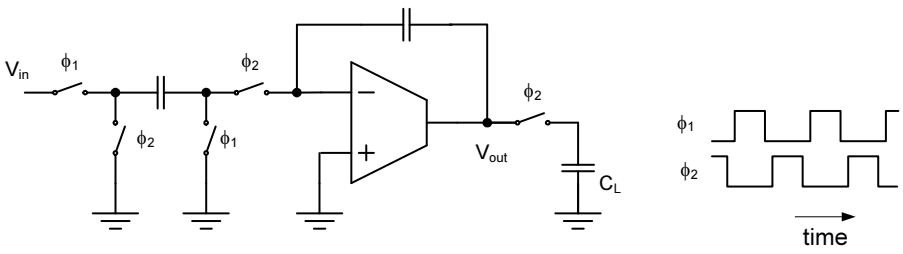
Noise in Differential Circuits

- In differential circuits, the noise power is doubled (because there are two half circuits contributing to the noise)
- But, the signal power increases by 4x
  - Looks like a 3dB win?

$$DR_{\text{single}} \propto \frac{\hat{V}_o^2}{\frac{kT}{C}} \qquad DR_{\text{diff}} \propto \frac{\left(2\hat{V}_o\right)^2}{2\frac{kT}{C}} = 2\frac{\hat{V}_o^2}{\frac{kT}{C}}$$

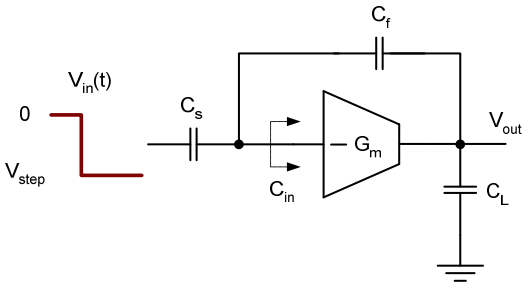
- Yes, there's a 3dB win in DR, but it comes at twice the power dissipation (due to two half circuits)
- Can get the same DR/power in a single ended circuit by doubling all cap sizes and g_m

Settling Performance



- In switched capacitor circuits the amplifier is subjected to transient pulses
- Output must "settle" within the ϕ_2 clock phase, so that a proper voltage level is sampled on C_L

Analysis



Note:
Replace C_f with $C_{ftot} = C_f + C_{gd}$ in all of the following expressions if there is extra feedback capacitance (due to C_{gd}) inside the OTA

- Assuming a single stage OTA, we have

$$A(s) = \frac{V_{out}(s)}{V_{in}(s)} \cong -\frac{C_s}{C_f}\frac{1}{1+\frac{1}{T_0}}\cdot\frac{1}{1+\frac{s}{\omega_c}} \qquad T_0 = \beta \cdot G_m R_o \qquad \beta = \frac{C_f}{C_f + C_s + C_{in}}$$

$$\omega_c \cong \beta \cdot \frac{G_m}{C_{Ltot}} \qquad C_{Ltot} = C_L + (1-\beta)\cdot C_f$$

Step Response

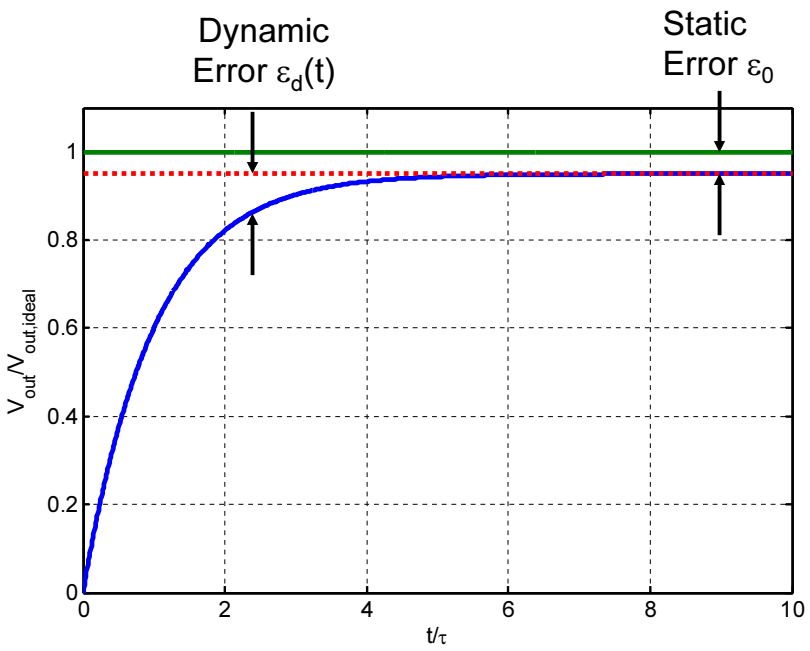
$$V_{out}(s) = A(s)\cdot V_{in}(s)$$

$$V_{out}(t) = L^{-1}\{A(s)\cdot V_{in}(s)\}$$

$$V_{out}(t) = L^{-1}\left\{A(s)\cdot\frac{V_{step}}{s}\right\} = \underbrace{-\frac{C_s}{C_f}\cdot V_{step}}_{\text{Ideal Response}}\cdot\underbrace{\frac{T_0}{1+T_0}}_{\text{Due to Finite DC Loop Gain}}\cdot\underbrace{\left(1-e^{-t/\tau}\right)}_{\text{Due to Finite Bandwidth}} \qquad \tau = \frac{1}{\omega_c}$$

- Finite DC loop gain results in a static error ε_0
- Finite bandwidth results in a dynamic error ε_d that decays with time

Graphical Illustration



Design Considerations (1)

- Need large DC loop gain for small static error
  - $|\varepsilon_0| \cong 1/T_0$
  - E.g. need $T_0 > 1000$ for better than 0.1% precision
- Need small τ (large bandwidth) for fast settling
- Can define "settling time" based on tolerable dynamic error

$$-\varepsilon_{d,tol} = -e^{-t_s/\tau}$$

$$\boxed{t_s = -\tau \cdot ln\left(\varepsilon_{d,tol}\right)}$$

Design Considerations (2)

$\varepsilon_{d,tol}$	t_s/τ
1%	4.6
0.1%	6.9
0.01%	9.2
10^{-6}	13.8

- Going from 1% dynamic precision to 10^{-6} necessitates only ~3x increase in settling time

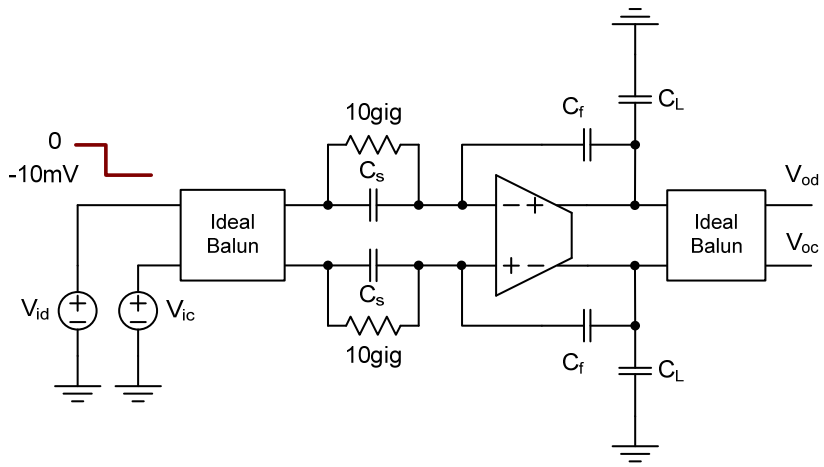
Design Considerations (3)

- A switched capacitor circuit operates in two clock phases
- Fitting the required number of time constants within ½ period lets us relate f_s to a minimum bandwidth requirement

$$t_s = -\frac{1}{2\pi \cdot f_c} \cdot ln\left(\varepsilon_{d,max}\right) < \frac{1}{2}\frac{1}{f_s} \qquad \frac{f_c}{f_s} > -\frac{1}{\pi} ln\left(\varepsilon_{d,max}\right)$$

ε_d	f_c/f_s
1%	1.5
0.1%	2.2
0.01%	2.9
10^{-6}	4.4

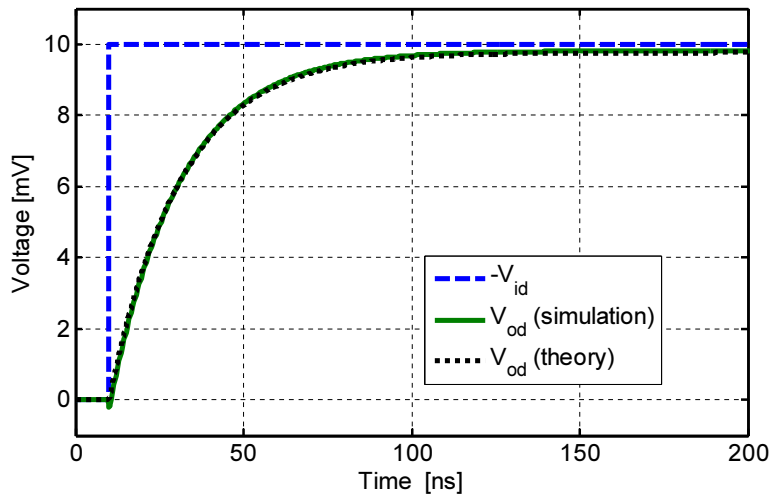
Simulation Example



- Using single stage OTA
- Parameters
  - C_s=C_f=500fF, C_L=10pF, β=0.48, G_m=1mS, G_mR_o=85, V_{idstep}=-10mV

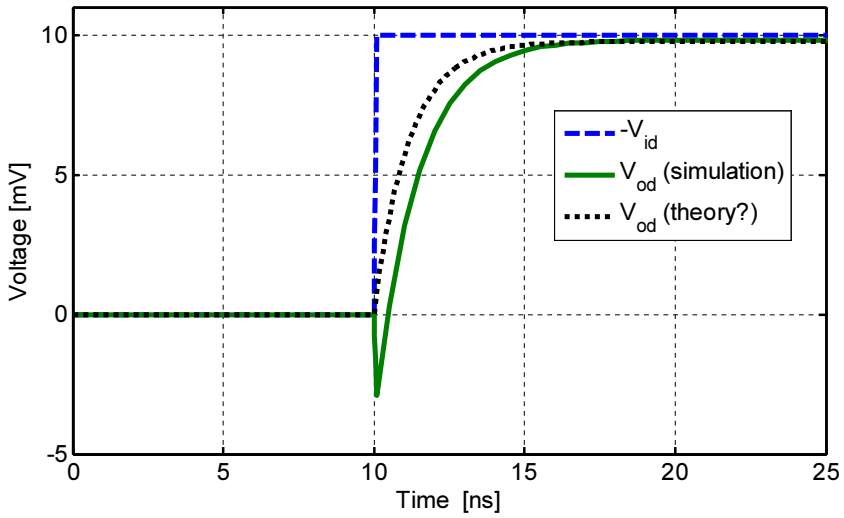
Result

$$\tau = \frac{1}{\beta}\frac{C_L + (1-\beta)C_f}{G_m} = 21ns \qquad V_{od,final} = -V_{idstep}\frac{\beta \cdot G_m R_0}{1+\beta \cdot G_m R_0} = 9.76mV$$



Another Run

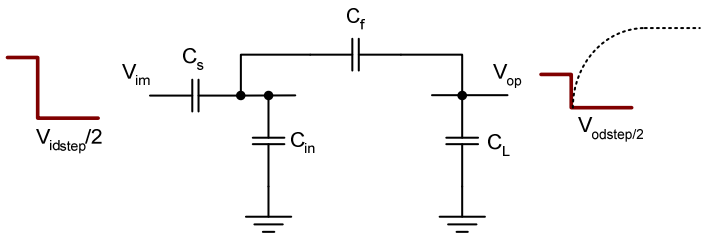
- Changed C_L from 10pF to 300fF



- What's this ?

Capacitive Feedforward

- In the first instant after the input step has been applied, the output is completely determined by capacitive voltage division
- Half circuit during initial transient



$$\frac{V_{odstep}}{V_{idstep}} = \frac{C_s}{C_s + C_{in} + \frac{C_f C_L}{C_f + C_L}} \cdot \frac{C_f}{C_f + C_L}$$

Analysis

- Can analyze this effect in two (equivalent) ways
  - Using capacitive divider to find new starting point of exponential
  - Using inverse Laplace transform of A(s) with high frequency zero included
- Recall that A(s) is more precisely given by

$$A(s) = -\frac{C_s}{C_f}\frac{1}{1+\frac{1}{T_0}}\frac{1-\frac{s}{z}}{1-\frac{s}{p}} \qquad z = \frac{G_m}{C_f} \qquad p = -\frac{\beta G_m}{C_{Ltot}}$$

New Result

$$V_{od}(t) = L^{-1}\left\{A(s)\cdot\frac{V_{step}}{s}\right\} = -\frac{C_s}{C_f}\cdot V_{idstep}\cdot\frac{T_0}{1+T_0}\cdot\left(1-\underbrace{\left[1-\frac{p}{z}\right]}_{\text{New}}e^{-t/\tau}\right)$$

$$1-\frac{p}{z} = \frac{C_L+(1-\beta)C_f+\beta C_f}{C_L+(1-\beta)C_f} = \frac{C_L+C_f}{C_L+(1-\beta)C_f} = \frac{1}{1-\beta\frac{C_f}{C_f+C_L}}$$

- For our example:

$$\frac{1}{1-0.48\frac{500fF}{500fF+300fF}} = 1.4 \quad \Rightarrow \quad V_{od}(t=0) \cong 10mV(1-1.4) = -4mV$$

- Good agreement with simulation

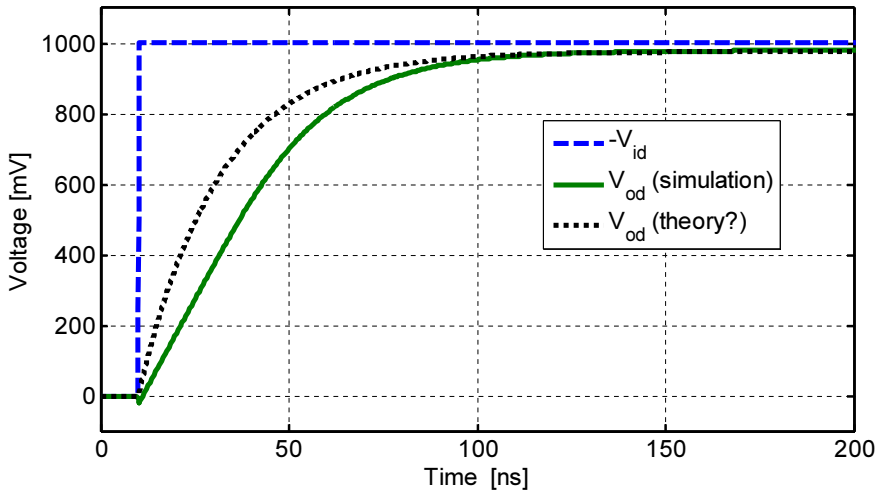
New Settling Time

$$t_s = -\tau \cdot ln\left(\varepsilon_{d,tol} \underbrace{\left[1 - \beta \cdot \frac{C_f}{C_f + C_L} \right]}_{<1} \right)$$

- Settling time for given precision increases due to feedforward, since the settling range is artificially enlarged
- E.g., in our simulation example, the time to settle within 0.1% dynamic error increases from 6.9τ to 7.3τ
  - Not all that significant, especially when β is low and C_L is at least comparable to C_f

Another Simulation

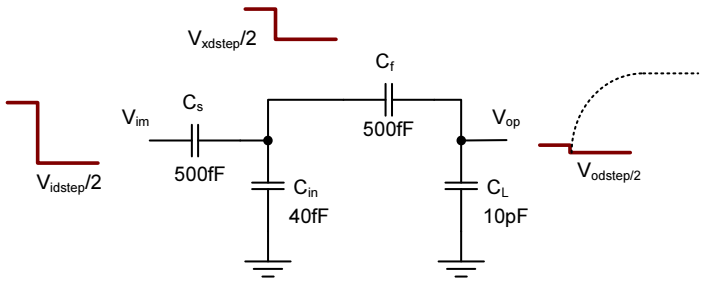
- Set V_{idstep}=-1V (C_L=10pF $\Rightarrow$ insignificant feedforward to output)



- What causes this discrepancy ?

Capacitive Divider at OTA Input

- Half circuit during initial transient:

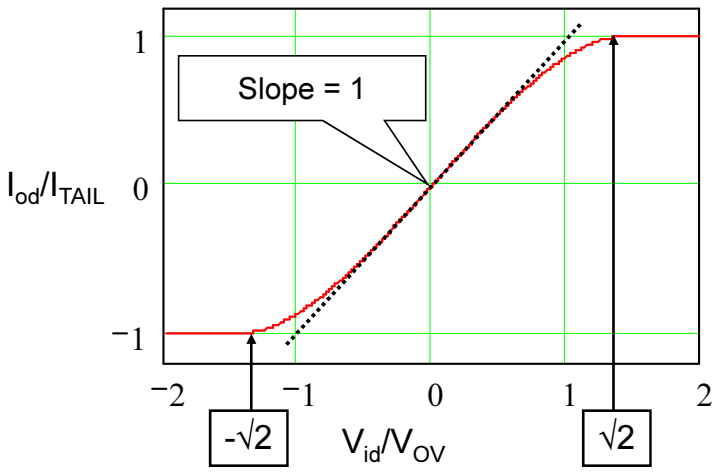


$$V_{xdstep} = V_{idstep}\frac{C_s}{C_s + C_{in} + \frac{C_f C_L}{C_f + C_L}} \cong -1V\frac{500fF}{500fF + 40fF + 500fF} = -480mV$$

- Initially -480mV across differential pair input!

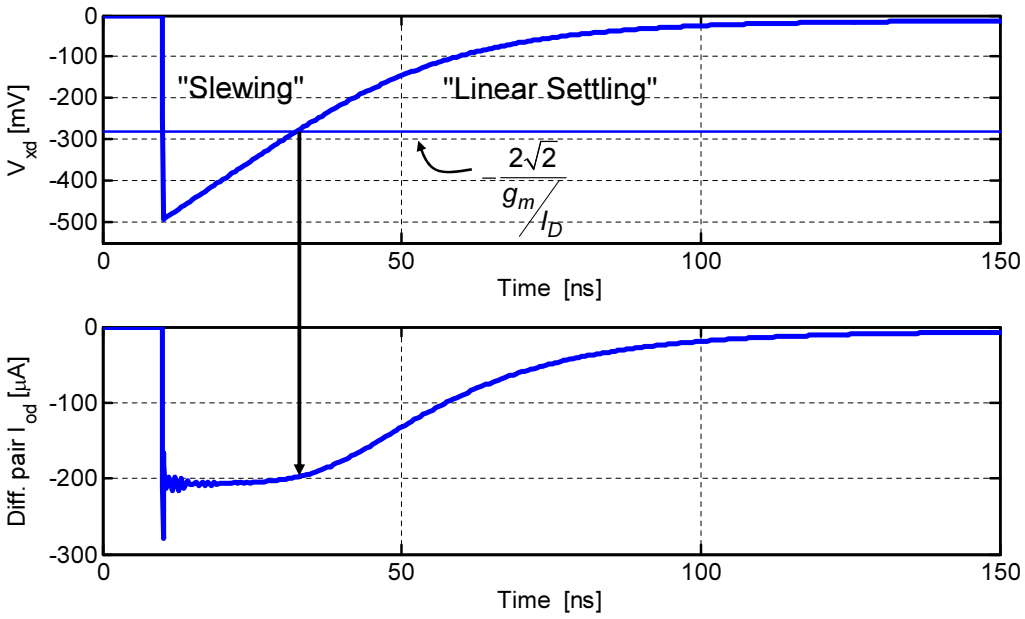
Differential Pair Characteristics

- Differential output current saturates for $|V_{id}| > \sqrt{2}\cdot V_{OV}$
- Beyond this point, current will be much less than that predicted by linear model (slope at origin)



$$V_{OV} = V_{GS} - V_t \cong \frac{2}{g_m / I_D}$$

Differential Pair Input Voltage vs. Output Current

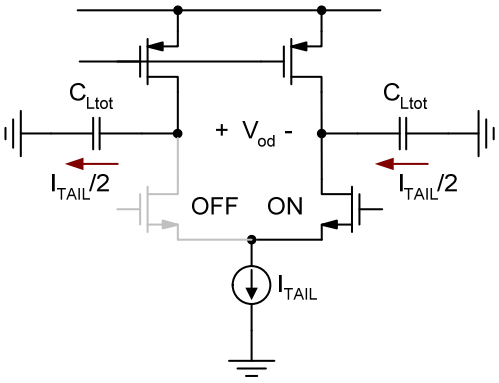


Slewing

- During "slewing", the amplifier drives its output with an approximately constant current (equal to tail bias)
- The slewing behavior ends when $|V_{id}|$ has become smaller than about $1.4 \cdot (2/g_m/I_D)$
  - This is the point when the differential pair re-enters its "linear region"
  - Hence, the remaining portion of the settling is often called "linear settling"
    - Note that this is not meant to say that the output changes with a constant rate during this time; it settles with a $(1-e^{t/\tau})$ relationship
- The total settling time of the amplifier in presence of slewing can be calculated as shown in the following derivation

Slew Rate

- In order to find the time it takes to complete slewing, we can first calculate the "ramp speed" at which the output changes
  - This quantity is called "Slew Rate" (SR)



$$SR = \frac{dV_{od}}{dt} = \frac{I_{TAIL}}{C_{Ltot}}$$

Slewing Time

- The input of the differential pair changes at a rate equal to $\beta \cdot SR$, where β is given by the usual capacitive feedback divider
- Hence, the time it takes to complete slewing is given by

$$t_{slew} \cong \frac{\left|V_{xstep}\right| - 2.8 / (g_m / I_D)}{\beta \cdot SR}$$

- In our example, we have

$$SR = \frac{I_{TAIL}}{C_{Ltot}} \cong \frac{200\mu A}{10pF} = 20\frac{V}{\mu s}$$

$$t_{slew} = \frac{480mV - 280mV}{0.48 \cdot 20\frac{V}{\mu s}} = 21ns$$

Subsequent Linear Settling

- Once slewing is completed, the differential output voltage is

$$V_{od,slew} = V_{od,final} - V_{od,lin} = t_{slew} \cdot SR = 420mV$$

- The final settling value in our example is roughly 1V
  - Almost half way there after slewing
- This means that the dynamic error budget for the remaining settling portion ($V_{od,lin}$) has increased
  - E.g. if we wanted to settle within 0.1% of the final value (~1V), we only need to complete the remaining transient to within 0.1%·1V/0.58V = 0.17%
  - Not a very big win, usually a negligible change in the number of required time constants
    - 0.1% → 6.9τ versus 0.17% → 6.4τ

Complete Expression for Settling Time

$$t_s = t_{slew} + t_{lin} \cong \frac{\left|V_{xdstep}\right| - 2.8/(g_m/I_D)}{\beta \cdot SR} - \tau ln\left(\varepsilon_{d,tol}\frac{V_{od,final}}{V_{od,lin}}\right)$$

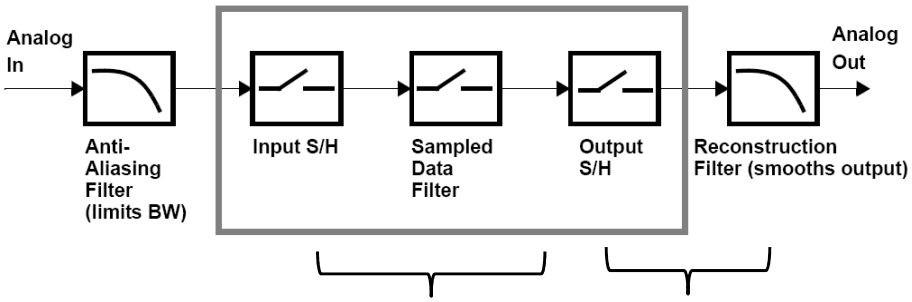
$$V_{xdstep} = V_{idstep}\frac{C_s}{C_s + C_{in} + \frac{C_f C_L}{C_f + C_L}} \cong V_{idstep}\underbrace{\frac{C_s}{C_s + C_{in} + C_f}}_{<1}$$

- Note that circuits with large closed loop gain tend to slew less
  - Since $V_{id,step}$ cannot be larger than $V_{od,final}$/Gain
  - E.g. $V_{od,final}$=2V, Gain =8 $\Rightarrow$ $V_{xdstep} < V_{idstep} < 250mV$
    - The circuit won't slew at all as long as $g_m/I_D < 2.8/250mV = 11.2$ S/A

Design Considerations

- When slewing is an issue, it can be mitigated by biasing the relevant transistors at lower g_m/I_D
  - Increase I_D, keep g_m constant
  - Slewing performance improves, because of larger I_D and also because the differential pair input range increases ($2.8/[g_m/I_D]$)
  - Small signal performance remains virtually unchanged or improves if f_T is a limiting factor (since f_T increases)
  - Issue
    - Lower g_m/I_D means higher power consumption

Slewing in SC Filters

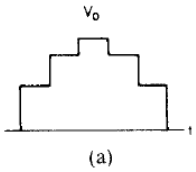


Slewing is not a problem provided that the waveform has settled accurately in the sampling instant

Slewing is usually detrimental

Slewing in Output Stage (1)

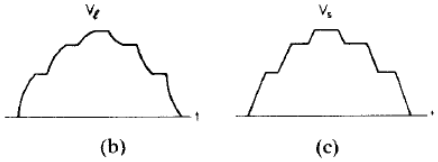
Ideal waveform



K.-L. Lee and R.G. Meyer, "Low-distortion switched-capacitor filter design techniques," IEEE J. Solid-State Circuits, vol. 20, no. 6, pp. 1103-1113, Dec. 1985.

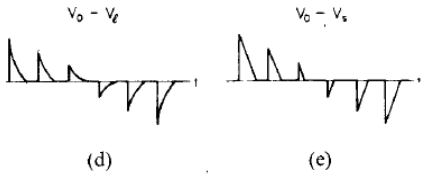
Linear settling

Initial slewing



Error proportional to signal

Error proportional to signal squared



Slewing in Output Stage (2)

K.-L. Lee and R.G. Meyer, "Low-distortion switched-capacitor filter design techniques," IEEE J. Solid-State Circuits, vol. 20, no. 6, pp. 1103-1113, Dec. 1985.

$$HD_k = \frac{Y'(k)}{V_0} = \frac{1}{2S_rT_c}\frac{4\left(2V_0\sin\frac{\omega_0 T_c}{2}\right)^2}{\pi k(k^2-4)}\frac{1}{V_0}$$

$$= \frac{8\left(\sin\frac{\omega_0 T_c}{2}\right)^2}{\pi k(k^2-4)}\frac{V_0}{S_rT_c}, \quad k=1,3,5,7,\cdots \quad (15)$$

For improved linearity:
Increase slew rate or reduce amplitude

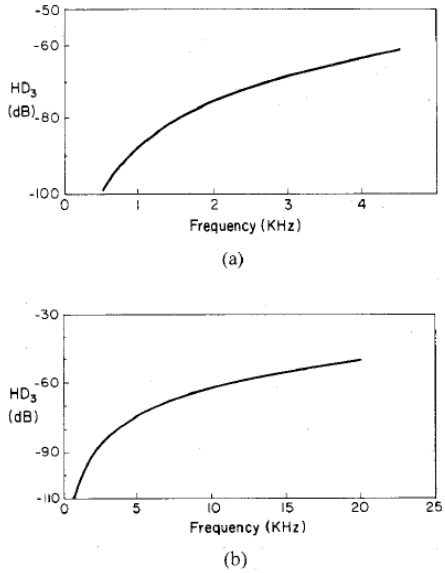


Fig. 4. Calculated third harmonic (worst case) caused by slewing distortion. $V_0 = 3$ V, $S_r = 1$ V/μs. (a) Sampling rate: 128 kHz. (b) Sampling rate: 500 kHz.

Bandwidth Requirements for Filter Core

- Initial slewing is not a problem provided that the waveform has settled accurately in the sampling instant
- Rough calculation
  - Assume amplifier slews for $T_s/4$
  - Assume remaining linear settling occurs for 10 time constants (precision ~0.01%)

$$10\tau = \frac{10}{2\pi f_c} = \frac{T_s}{4} = \frac{1}{4f_s} \qquad f_c = \frac{40}{2\pi} f_s \cong 6.4 f_s$$

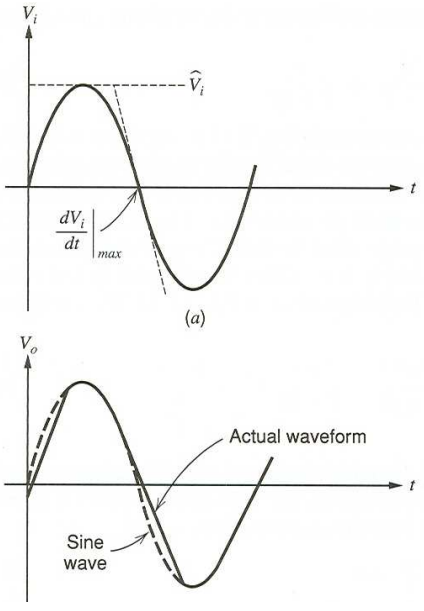
$$f_s = 10...100 \cdot f_0 \qquad f_c \cong 64...640 \cdot f_0$$

- Compare to CT filter (chapter 4)

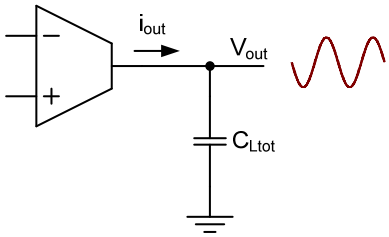
$$f_u \cong 50...1000 \cdot f_0$$ Roughly the same.

Slewing in a CT Filter (1)

- If slewing occurs in a continuous time filter it will introduce distortion
  - Similar to the case of the SC output stage
- Is this a real problem?



Slewing in a CT Filter (2)



$$v_{out}(t) = \hat{V}_{out}\sin(\omega t)$$

$$i_{out}(t) = C_{Ltot}\frac{dv_{out}}{dt} = \omega C_{Ltot}\cdot\hat{V}_{out}\cos(\omega t)$$

$$\hat{i}_{out} = \omega C_{Ltot}\cdot\hat{V}_{out}$$

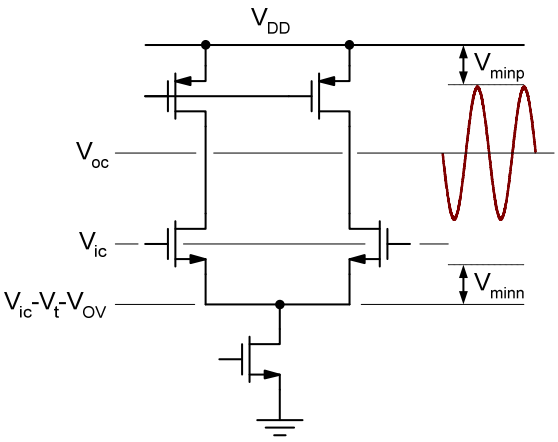
- To avoid slewing, we need

$$\omega < \frac{\hat{i}_{out}}{\hat{V}_{out}C_{Ltot}} = \frac{I_{TAIL}}{\hat{V}_{out}C_{Ltot}} = \frac{2I_D}{\hat{V}_{out}C_{Ltot}\cdot\beta\frac{g_m}{C_{Ltot}}}\omega_c = \frac{2}{\hat{V}_{out}\cdot\beta\frac{g_m}{I_D}}\omega_c$$

$$e.g.\quad \omega < \frac{2}{1V\cdot 0.5\cdot 10\frac{S}{A}}\omega_c = 0.4\cdot\omega_c$$

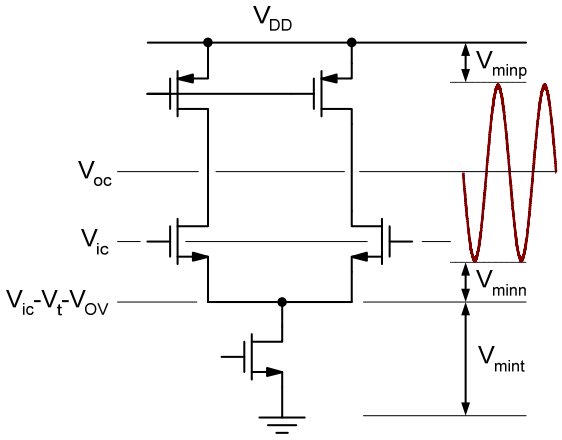
Not a significant constraint, since we need $\omega << \omega_c$ anyway

Output Swing of Simple OTA



- Available output swing depends on input and output common mode levels
- May be limited by headroom for differential pair device (V_{minn}) or active load (V_{minp})

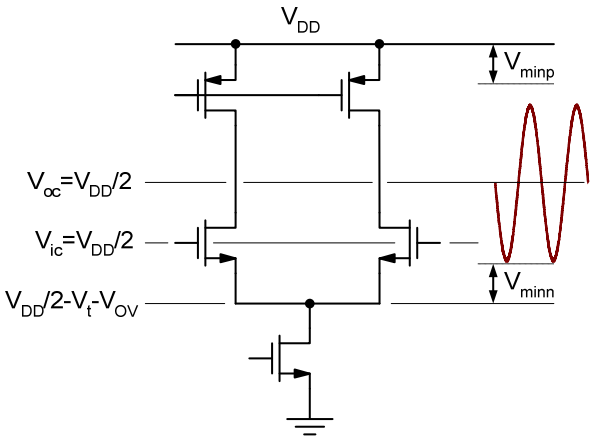
Maximum Available Swing



$$V_{odpp,max} = 2\left(V_{DD} - V_{min\,p} - V_{minn} - V_{mint}\right)$$

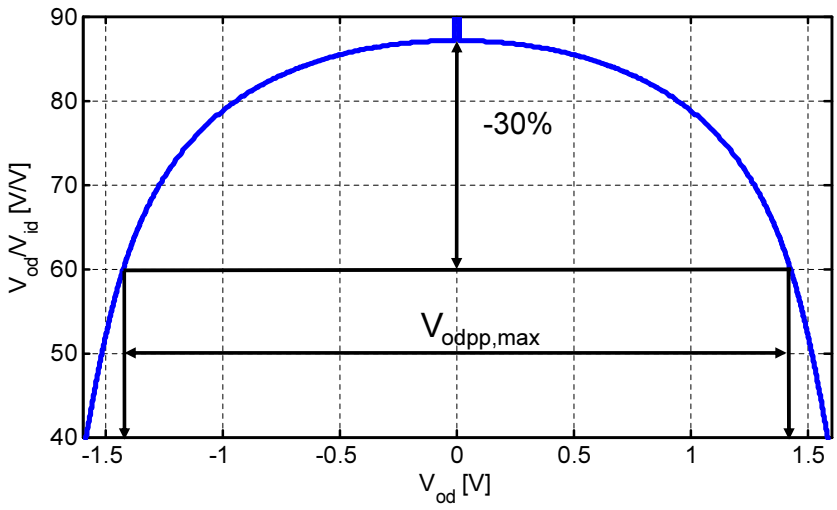
- Input and output common mode adjusted such that all devices operate at "edge" of active region
  - Well defined using long channel model, very gradual transition in short channels
- Unfortunately, the choice of V_{ic} and V_{oc} are often dictated by the circuits that interface with the amplifier
  - E.g. $V_{ic}=V_{oc}=1.5V$

Example $V_{ic}=V_{oc}=V_{DD}/2$



- Assuming that we are limited by V_{minn}, and V_{minn}~V_{OV}, the available differential peak-to-peak swing is ~$4V_t$
- Since the transition to triode is smooth, which criterion should we use find the "exact" output range of an amplifier?

Gain vs. Output Swing DC Simulation



- In EE315A, we arbitrarily define output range as the peak-to-peak swing that causes no more than 30% drop in V_{od}/V_{id}

How Much Gain Can We Get?

- Small signal gain (around $V_{id}=V_{od}=0$)

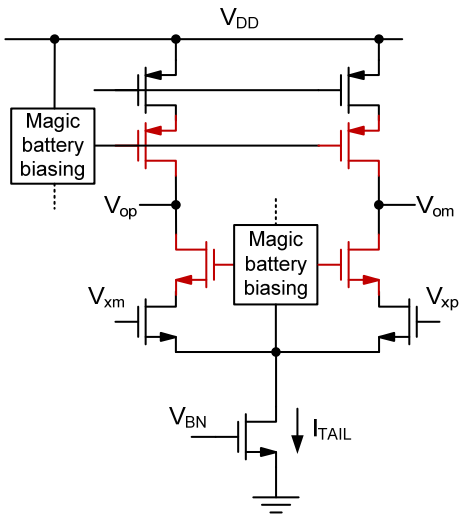
$$a_0 = g_{mn} \cdot \frac{r_{on} \cdot r_{op}}{r_{on} + r_{op}} = a_{0n} \frac{1}{1 + \frac{r_{on}}{r_{op}}} = a_{0n} \frac{1}{1 + \frac{g_{mp}}{g_{mn}} \frac{a_{0n}}{a_{0p}}}$$

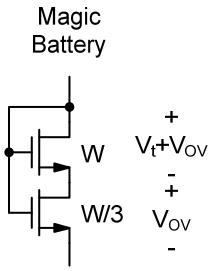
$$\boxed{a_0 = a_{0n} \frac{1}{1 + \frac{(g_m / I_D)_p}{(g_m / I_D)_n} \frac{a_{0n}}{a_{0p}}}}$$

$$\boxed{a_0 = a_{0n} \,||\, a_{0p}} \qquad \text{for} \quad (g_m / I_D)_p = (g_m / I_D)_n$$

- E.g. $a_{0n}=a_{0p}=50$, $(g_m/I_D)_n = (g_m/I_D)_p \Rightarrow a_0=25$
- Static gain error ~$1/T_o$ ~$1/a_0$ ~1/25 = 4%
  - Not precise enough for many applications

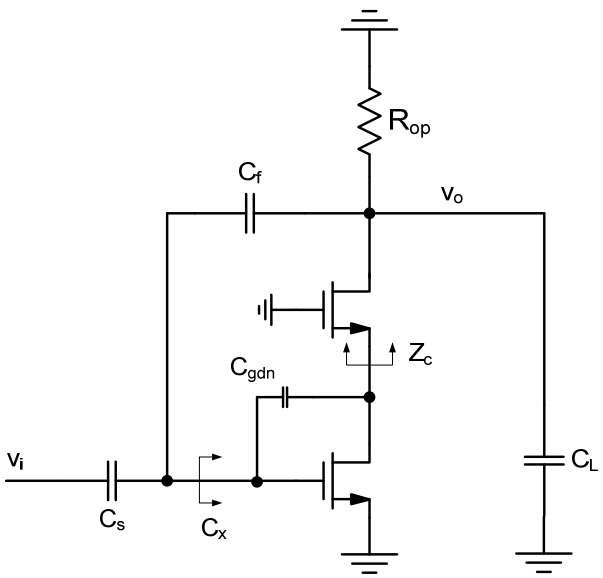
Telescopic OTA





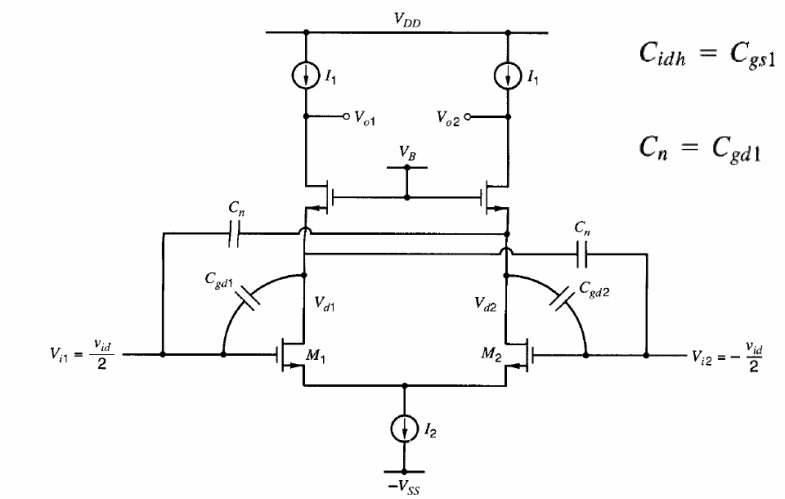
- Voltage gain ~ $(g_m r_o)^2$, but smaller output range

Half Circuit with Capacitive Feedback



- C_{gdn} sees significant Miller amplification at low frequencies
  - Since $Z_c \sim 1/g_m$ only at high frequencies
  - See EE114 for a detailed analysis
- Solution: Neutralization

Neutralization

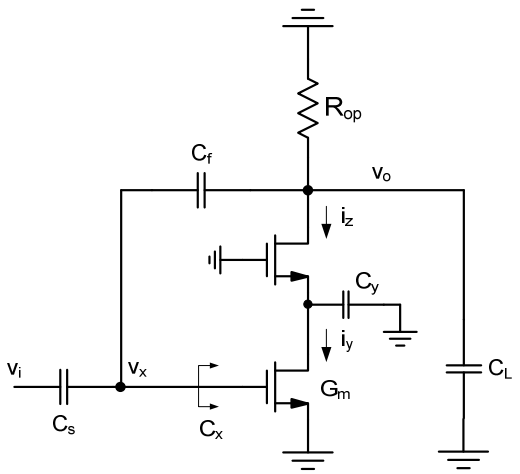


$$C_{idh} = C_{gs1} + C_{gd1}(1 - a_{dm1}) + C_n(1 + a_{dm1})$$

$$C_n = C_{gd1} \Rightarrow C_{idh} = C_{gs1} + 2C_{gd1}$$

Gray & Meyer, 5th ed., p.837

High Frequency Loop Gain



$$T(s) = -\frac{v_x}{v_o} \cdot \frac{i_y}{v_x} \cdot \frac{i_z}{i_y} \cdot \frac{v_o}{i_z}$$

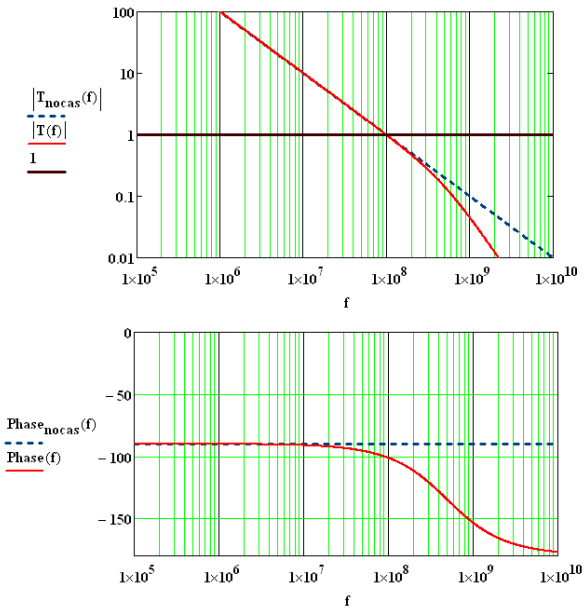
$$= -\beta \cdot G_m \cdot \frac{1}{1 - \frac{s}{p_2}} \cdot \frac{-1}{sC_{Ltot}}$$

$$p_2 = -\frac{g_m'}{C_y}$$

$$C_y \cong C_{gs} + 2C_{db} \cong 3C_{gs}$$

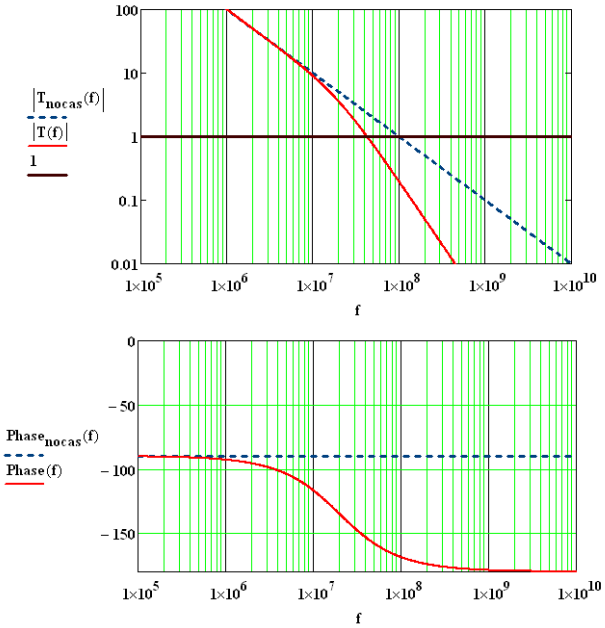
$$\Rightarrow \omega_{p2} \cong \frac{\omega_T}{3}$$

Example: $f_{p2} = 5f_c$



- Phase margin ~ 80 degrees
  - Non-dominant pole p_2 is not an issue in this case
- Since $\omega_{p2} \sim \omega_T/3$, this means that ω_c (and hence closed-loop BW) cannot be higher than $\sim\omega_T/15$ in this scenario

Example: $f_{p2} = f_c/5$

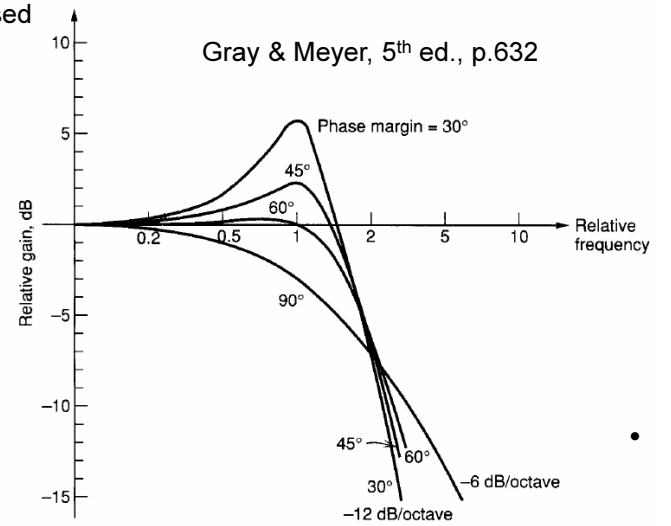


- Phase margin ~ 28 degrees
  - Not acceptable in practice
- How much phase margin should we design for?

Frequency Domain Perspective

Closed loop gain

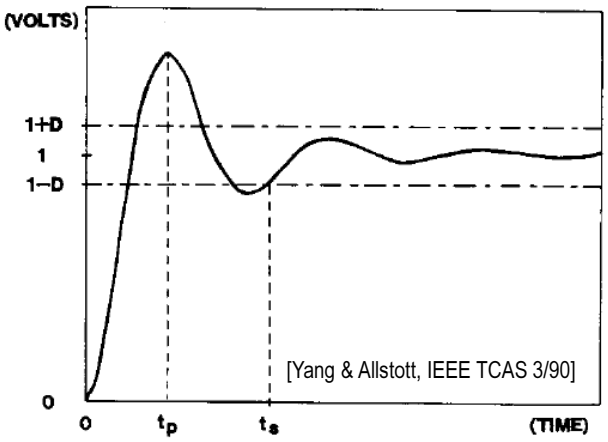
Gray & Meyer, 5th ed., p.632

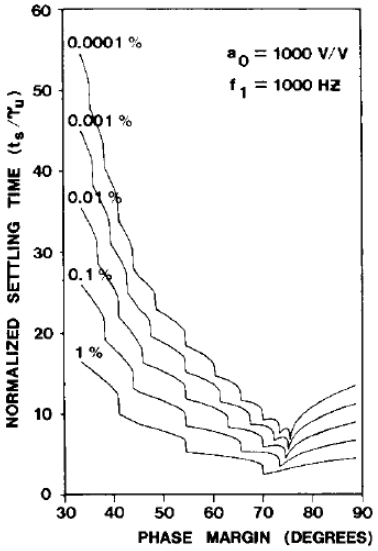


- Typically want phase margin ≥ 60 degrees

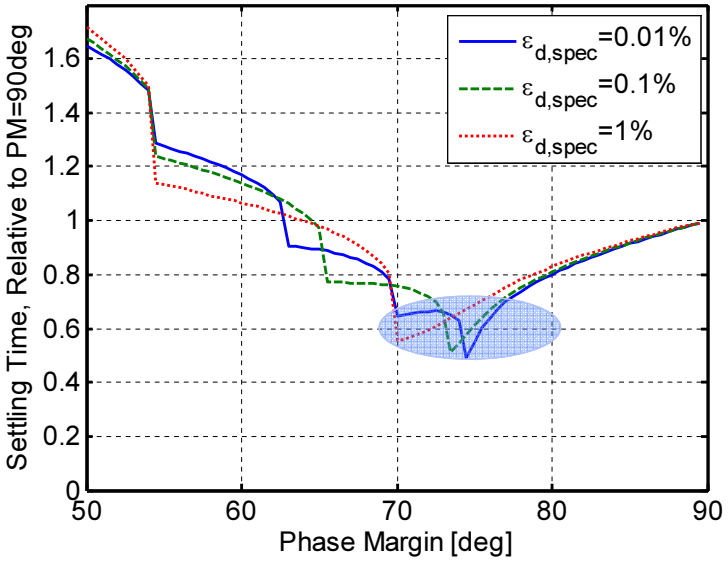
Time Domain Perspective (1)

Step Response





Time Domain Perspective (2)



- Typically want to shoot for phase margin ~70-75 degrees

Phase Margin as a Function of ω_{p2}

- At the crossover frequency, the dominant pole has shifted the phase by about -90°
- The non-dominant pole's phase at ω_c is given by $-\tan^{-1}(\omega_c/\omega_{p2})$

$$PM \cong 180° - 90° - \tan^{-1}\left(\frac{\omega_c}{\omega_{p2}}\right) \qquad \boxed{PM \cong \tan^{-1}\left(\frac{\omega_{p2}}{\omega_c}\right)}$$

ω_{p2}/ω_c	Approximate PM
1	45°
2	63°
3	72°
4	76°
5	79°

"Load Compensation"

- Nondominant pole is fixed at roughly $\omega_T/3$
- The loop crossover frequency is given by

$$\omega_c = \beta \frac{G_m}{C_{Ltot}}$$

- Increasing C_{Ltot} will lower ω_c and increase ω_{p2}/ω_c, which translates into larger phase margin
- A feedback circuit in which adding additional load capacitance improves stability is often called "load compensated"
  - Meaning that the load compensates or reduces the impact of phase shift from p_2

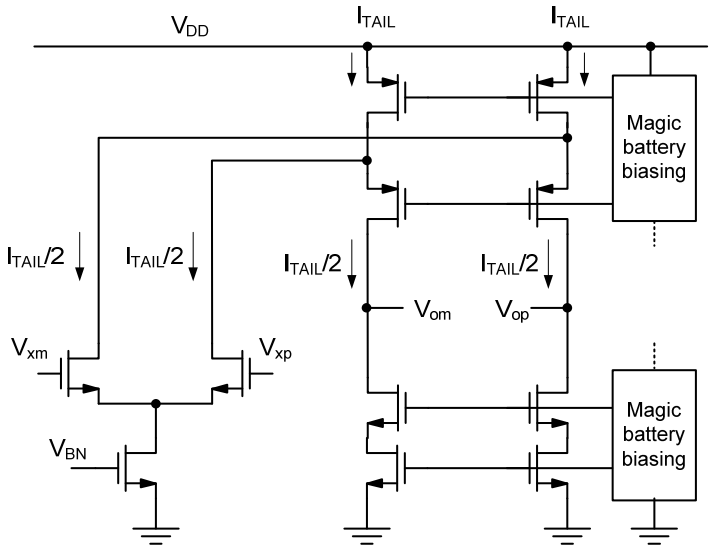
How Fast Can We Go?

- Let's say we design for $f_c \sim 1/3\ f_{p2} \sim 1/9\ f_T$
- At a reasonable bias, the NMOS transit frequency in 0.18um technology is roughly 20 GHz (nominal process and temperature)
- Assume 0.01% settling and no slewing

$$f_{s,max} = \frac{1}{2.9} \cdot \frac{f_T}{9} \cong \frac{f_T}{30} = \frac{20\ GHz}{30} = 666\ MHz$$

- In practice, it is hard to go any faster than 200 MHz in 0.18um technology
  - Slewing
  - Timing overhead (have somewhat less time than $T_s/2$)
  - Margins for process variation, wiring caps, etc.

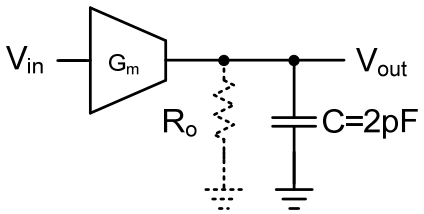
Folded Cascode OTA



(CMFB not shown)

- High- and low-frequency behavior similar to telescopic OTA
  - But noise is much worse
- Advantage: Input common mode can be chosen without taking away output signal range
- If slewing is not an issue, the current in the output branches can be reduced below $I_{TAIL}/2$

Design Example: Folded Cascode Stage for Gm-C Integrator



- Specs
  - Unity gain frequency = 100 MHz
  - HD3 = -50dB for 100 mV differential input amplitude
  - Low-frequency voltage gain = 300

Step 1

- Unity gain frequency spec determines G_m

$$f_u \cong \frac{1}{2\pi}\frac{G_m}{C} \qquad G_m = 2\pi f_u C$$

$$G_m = 2\pi \cdot 100MHz \cdot 2pF = 1.26mS$$

Step 2

- Distortion specification determines g_m/I_D of differential pair

$$HD_3 \cong \frac{1}{32}\left(\frac{\hat{v}_{id}}{V_{OV}}\right)^2 \qquad V_{OV} = \frac{\hat{v}_{id}}{\sqrt{32 \cdot HD_3}}$$

$$V_{OV} = \frac{100mV}{\sqrt{32 \cdot 10^{-50/20}}} = 314mV \qquad \frac{g_m}{I_D} \cong \frac{2}{V_{OV}} = 6.36\frac{S}{A}$$

- The tail current is now determined as

$$I_{TAIL} = 2I_D = 2\frac{G_m}{\left(\frac{g_m}{I_D}\right)} = 2\frac{1.26mS}{6.36\frac{S}{A}} = 396\mu A$$

Step 3

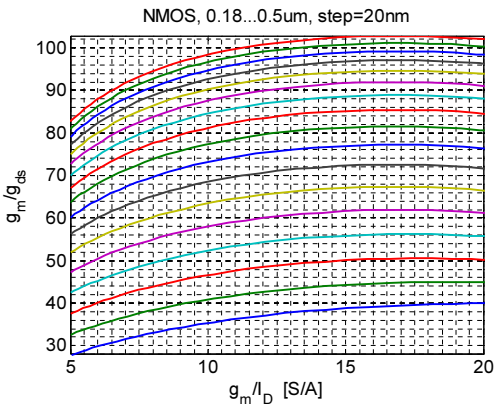
- The DC gain spec will determine the channel lengths
- In order to simplify the design, we choose the same intrinsic gain and g_m/I_D for all transistors (NMOS and PMOS)
  - This is subject to optimization and further constraints (e.g. required output swing)
- Given this simplification, the output resistance of the amplifier is

$$R_o = g_m r_o^2 \left\| \frac{1}{3} g_m r_o^2 = \frac{1}{4} g_m r_o^2 \right.$$

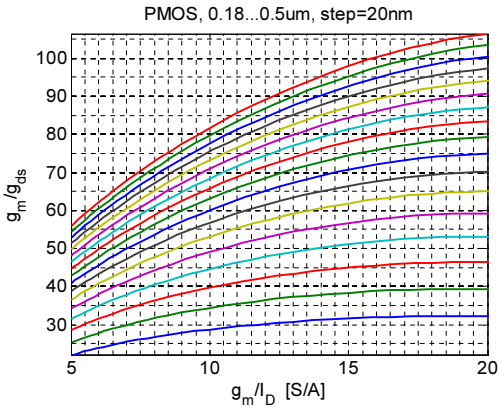
$$A_{v0} = G_m R_o = \frac{1}{4}\left(g_m r_o\right)^2 \qquad g_m r_o = \sqrt{4A_{v0}} = \sqrt{4 \cdot 300} = 34$$

Step 4

- We can now estimate channel lengths for the NMOS and PMOS devices
  - Use charts or lookup function to find L that yield $g_m r_o$~34 for g_m/I_D=6.36S/A
- Always need to overdesign in practice to account for model uncertainty, etc.



$\Rightarrow L_n \cong 0.26\mu m$



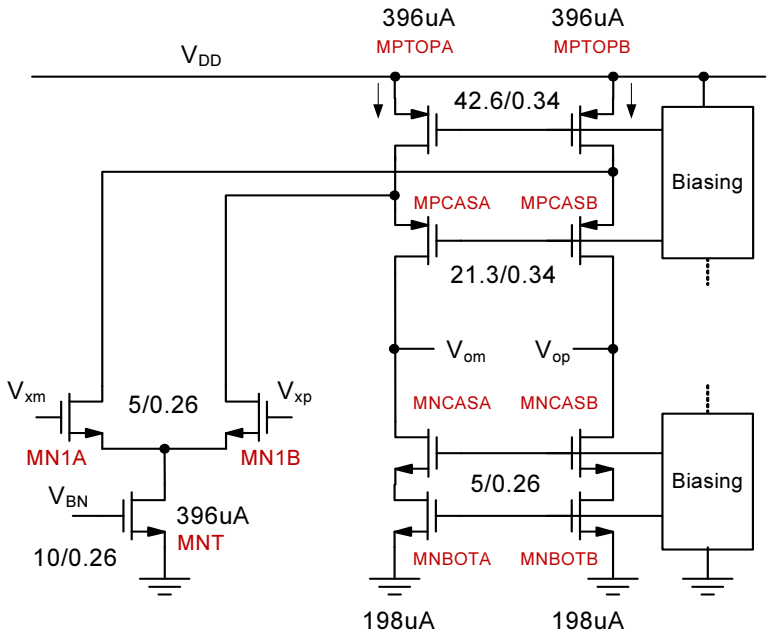
$\Rightarrow L_p \cong 0.34\mu m$

Step 5

- We can now determine all device widths using the current density charts or using the lookup function

$$W_n = \frac{I_D}{\left(\frac{I_D}{W}\right)} = \frac{\frac{396\mu A}{2}}{39.5\frac{\mu A}{\mu m}} = 5\mu m \qquad W_p = \frac{I_D}{\left(\frac{I_D}{W}\right)} = \frac{\frac{396\mu A}{2}}{9.3\frac{\mu A}{\mu m}} = 21.3\mu m$$

Amplifier Schematic



OP Output (1)

element	0:mn1a	0:mn1b	0:mnt	0:mbn	0:mnbota	0:mnbotb
model	0:nmos214	0:nmos214	0:nmos214	0:nmos214	0:nmos214	0:nmos214
region	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati
id	190.2597u	190.2597u	380.8886u	396.0000u	189.5109u	189.5109u
vgs	752.2426m	752.2426m	760.4818m	760.4818m	760.4818m	760.4818m
vds	810.9010m	810.9010m	497.7574m	760.4818m	440.1374m	440.1374m
vth	473.7197m	473.7197m	476.7170m	474.5689m	476.7964m	476.7964m
vdsat	198.8746m	198.8746m	202.5548m	203.7594m	201.7653m	201.7653m
vod	278.5229m	278.5229m	283.7648m	285.9129m	283.6854m	283.6854m
gm	1.2369m	1.2369m	2.4278m	2.4955m	1.2074m	1.2074m
gds	24.7544u	24.7544u	67.6983u	51.6464u	39.0347u	39.0347u
gmb	304.9489u	304.9489u	601.2780u	616.3676u	298.5179u	298.5179u
cdtot	6.1455f	6.1455f	12.5546f	12.1007f	6.4814f	6.4814f
cgtot	13.0810f	13.0810f	26.1930f	26.1782f	13.0936f	13.0936f
cstot	15.2437f	15.2437f	30.2189f	30.2241f	15.2409f	15.2409f
cbtot	10.7164f	10.7164f	21.3600f	20.9481f	11.0113f	11.0113f
cgs	10.0390f	10.0390f	20.0953f	20.0934f	10.0435f	10.0435f
cgd	2.3846f	2.3846f	4.7917f	4.7770f	2.3977f	2.3977f

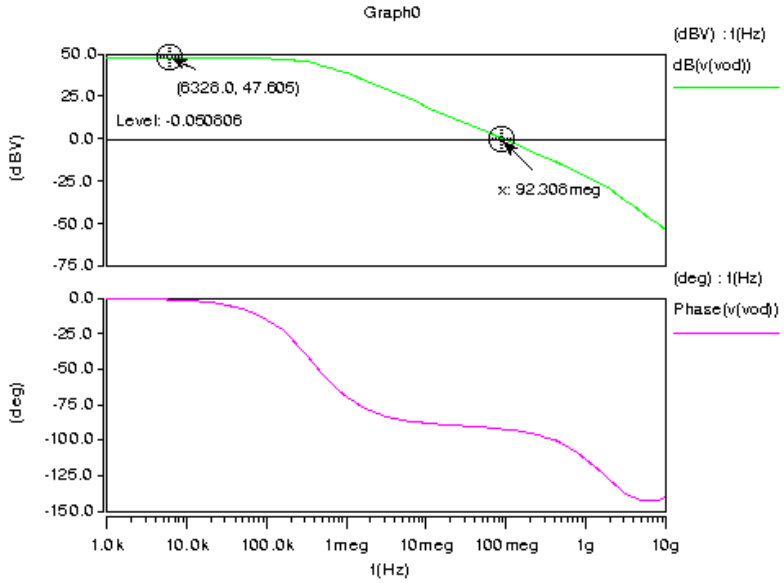
$\left(g_m r_o\right)_{MN1A} = 1.2369m / 24u = 51$ $\left(g_m r_o\right)_{MNBOTA} = 1.207m / 39u = 30.9$

$\left(g_m / I_D\right)_{MN1A} = 1.2369m / 190u = 6.5S / A$ $\left(g_m / I_D\right)_{MNBOTA} = 1.2074m / 189u = 6.4S / A$

OP Output (2)

element	0:mncasa	0:mncasb	0:mptopa	0:mptopb	0:mbp	0:mpcasa
model	0:nmos214	0:nmos214	0:pmos214	0:pmos214	0:pmos214	0:pmos214
region	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati
id	189.5109u	189.5109u	-379.7706u	-379.7706u	-396.0000u	-189.5109u
ibs	0.	0.	0.	0.	0.	0.
ibd	0.	0.	0.	0.	0.	0.
vgs	759.8626m	759.8626m	-741.7670m	-741.7670m	-741.7670m	-708.6585m
vds	459.8622m	459.8622m	-491.3415m	-491.3415m	-741.7670m	-408.6588m
vbs	0.	0.	0.	0.	0.	0.
vth	476.6327m	476.6327m	-453.0226m	-453.0226m	-452.8419m	-468.1349m
vdsat	201.5108m	201.5108m	-243.2913m	-243.2913m	-243.4279m	-207.1220m
vod	283.2299m	283.2299m	-288.7444m	-288.7444m	-288.9250m	-240.5235m
beta	6.5064m	6.5064m	10.4161m	10.4161m	10.4164m	7.3460m
gam eff	584.0576m	584.0576m	536.0450m	536.0450m	536.0450m	535.6122m
gm	1.2105m	1.2105m	2.4223m	2.4223m	2.5111m	1.4682m
gds	36.9367u	36.9367u	75.4521u	75.4521u	57.3564u	60.3266u
gmb	299.2095u	299.2095u	778.1057u	778.1057u	806.3873u	461.1078u
cdtot	6.4556f	6.4556f	62.4083f	62.4083f	59.9034f	31.7194f
cgtot	13.0917f	13.0917f	139.8713f	139.8713f	139.7711f	58.1141f
cstot	15.2410f	15.2410f	156.5909f	156.5909f	156.6170f	65.6594f
cbtot	10.9924f	10.9924f	100.0478f	100.0478f	97.8106f	47.0297f
cgs	10.0432f	10.0432f	108.1376f	108.1376f	108.0985f	42.7560f
cgd	2.3954f	2.3954f	28.0495f	28.0495f	27.9511f	13.9541f

AC Simulation



$A_{v0} = 10^{47.6/20} = 240$

$f_u = 92.3$ MHz

Distortion Simulation

- Input amplitude of 100mV at 1MHz
- Measuring output current into ac-grounded output

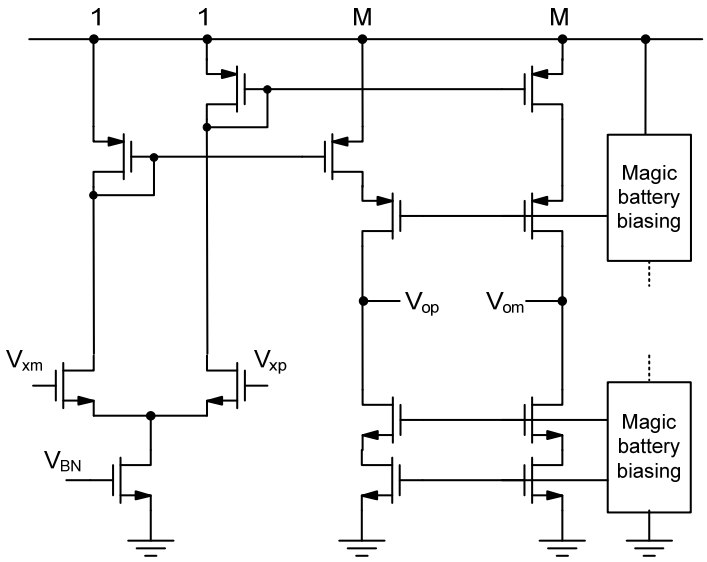
```
fourier components of transient response
dc component = 2.28983e-12

harmonic frequency fourier   normalized phase      normalized
no       (hz)      component component  (deg)      phase (deg)
1        1.00000x  115.121u  1.00000    -0.0261328 0
2        2.00000x  41.3954p  359.582n   97.067     97.0931
3        3.00000x  309.879n  2.69178m   -0.0343834 -0.00825056
4        4.00000x  13.5878p  118.031n   116.772    116.798
5        5.00000x  2.44211n  21.2135u   179.57     179.596
6        6.00000x  18.3837p  159.691n   -78.8736   -78.8475
7        7.00000x  83.4923p  725.258n   159.704    159.73
8        8.00000x  47.3039p  410.907n   108.197    108.223
9        9.00000x  92.1176p  800.182n   -85.6562   -85.63

total harmonic distortion =   0.269186  percent
```

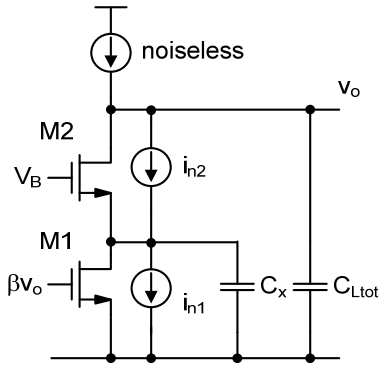
$$HD3 = 20\log\left(2.69 \cdot 10^{-3}\right) = -51.4dB$$

Current Mirror OTA



- No Miller effect issues
- $G_m = M \cdot g_m$
  - But non-dominant pole due to mirror scales as 1/M
- Useful for applications that don't demand bandwidths close to process limits
- Example
  - Yao, IEEE JSSC 11/2004

Noise Analysis of Basic Cascode Stage



- The detailed analysis on the next two slides shows

$$\overline{v_o^2} = \frac{1}{\beta}\frac{kT}{C_{Ltot}}\gamma\left(1+\frac{g_{m2}}{g_{m1}}\frac{\omega_c}{\omega_{p2}}\right)$$

$$\omega_c = \beta\frac{g_{m1}}{C_{Ltot}} \qquad \omega_{p2} = \frac{g_{m2}}{C_x}$$

- To minimize noise from M2
  - Maintain large phase margin (large ω_{p2}/ω_c)
  - Make g_{m2} as small as possible
    - Requires small g_m/I_D and costs headroom

Detailed Analysis (1)

KCL Analysis:

Given

$$g_{m1}\cdot\beta\cdot v_o + g_{m2}\cdot v_x + s\cdot C_x\cdot v_x + i_{n1} - i_{n2} = 0$$

$$-g_{m2}\cdot v_x + s\cdot C_{Ltot}\cdot v_o + i_{n2} = 0$$

$$\text{Find}(v_o, v_x) \rightarrow \begin{pmatrix} -\dfrac{g_{m2}\cdot i_{n1} + C_x\cdot i_{n2}\cdot s}{C_x\cdot C_{Ltot}\cdot s^2 + C_{Ltot}\cdot g_{m2}\cdot s + \beta\cdot g_{m1}\cdot g_{m2}} \\ \dfrac{C_{Ltot}\cdot i_{n2}\cdot s - C_{Ltot}\cdot i_{n1}\cdot s + \beta\cdot g_{m1}\cdot i_{n2}}{C_x\cdot C_{Ltot}\cdot s^2 + C_{Ltot}\cdot g_{m2}\cdot s + \beta\cdot g_{m1}\cdot g_{m2}} \end{pmatrix}$$

$$v_o = -\frac{g_{m2}\cdot i_{n1} + C_x\cdot i_{n2}\cdot s}{C_{Ltot}\cdot C_x\cdot s^2 + C_{Ltot}\cdot g_{m2}\cdot s + \beta\cdot g_{m1}\cdot g_{m2}} = -\frac{1}{\beta\cdot g_{m1}}\cdot\frac{\omega_c\cdot p_2}{s^2 + s\cdot p_2 + \omega_c\cdot p_2}\cdot\left(i_{n1} + i_{n2}\cdot\frac{s}{p_2}\right)$$

$$p_2 = \frac{g_{m2}}{C_x}$$

$$\omega_c = \beta\cdot\frac{g_{m1}}{C_{Ltot}}$$

Detailed Analysis (2)

Noise from M1:

$$N_1 = \int_0^\infty 4\cdot kT\cdot\gamma\cdot g_{m1}\cdot\left(\frac{1}{\beta\cdot g_{m1}}\right)^2\cdot\left(\left|\frac{\omega_c\cdot p_2}{s^2 + s\cdot p_2 + \omega_c\cdot p_2}\right|\right)^2 df$$

$$\int_0^\infty \left(\left|\frac{\omega_o^2}{s^2 + s\cdot\frac{\omega_o}{Q} + \omega_o^2}\right|\right)^2 df = \frac{\omega_o\cdot Q}{4}$$

$$N_1 = 4\cdot kT\cdot\gamma\cdot g_{m1}\cdot\left(\frac{1}{\beta\cdot g_{m1}}\right)^2\cdot\frac{\omega_c\cdot p_2}{p_2} = \frac{1}{\beta}\cdot\frac{kT}{C_{Ltot}}\cdot\gamma$$

Same result as without cascode

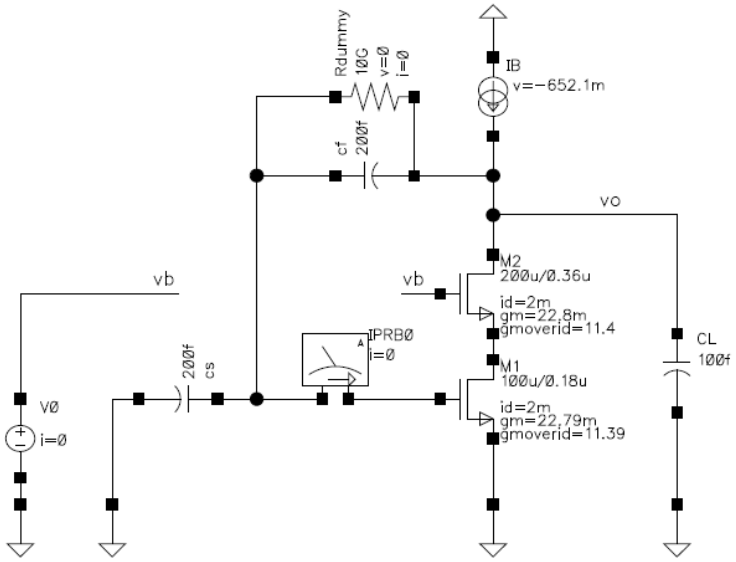
Noise from M2 (cascode device):

$$N_2 = \int_0^\infty 4\cdot kT\cdot\gamma\cdot g_{m2}\cdot\left(\frac{1}{\beta\cdot g_{m1}}\right)^2\cdot\left(\frac{\omega_c^2}{\omega_c\cdot p_2}\right)\cdot\left(\left|\frac{\sqrt{\omega_c\cdot p_2}\cdot s}{s^2 + s\cdot p_2 + \omega_c\cdot p_2}\right|\right)^2 df$$

$$\int_0^\infty \left(\left|\frac{\omega_o\cdot s}{s^2 + s\cdot\frac{\omega_o}{Q} + \omega_o^2}\right|\right)^2 df = \frac{\omega_o\cdot Q}{4}$$

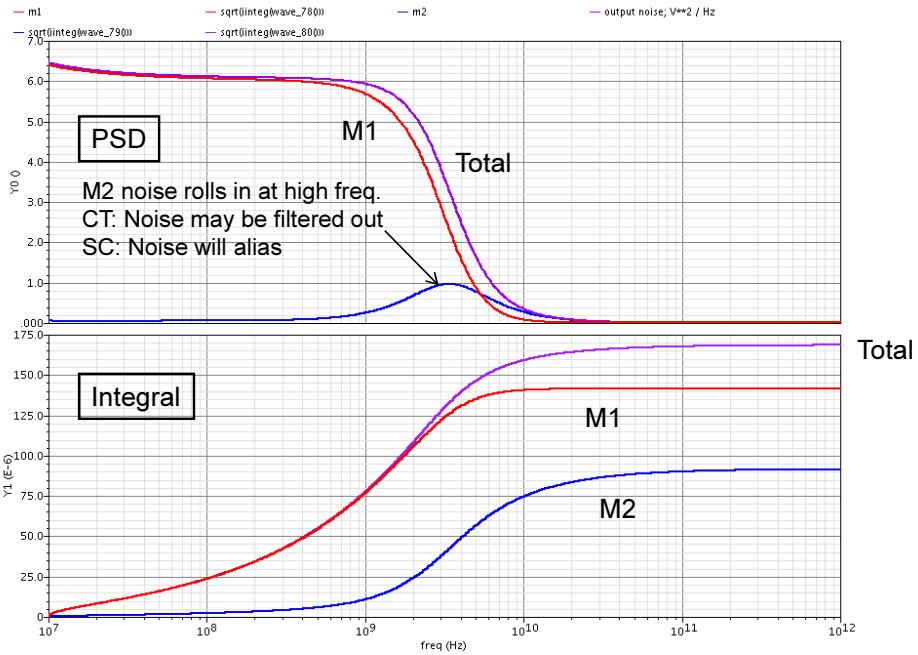
$$N_2 = N_1\cdot\frac{\omega_c}{p_2}\cdot\frac{g_{m2}}{g_{m1}}$$

Circuit Example



ω_c = 1.94 GHz
PM = 70.1 deg

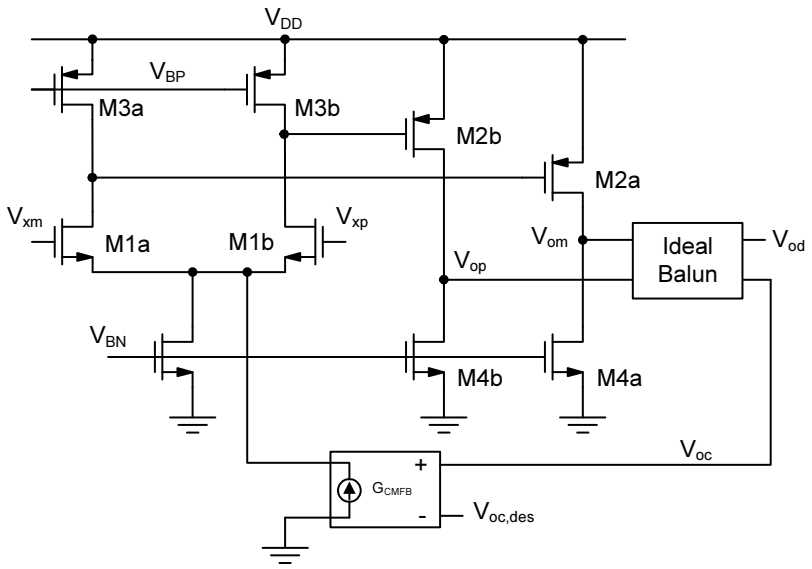
Noise Simulation



Two-Stage OTA

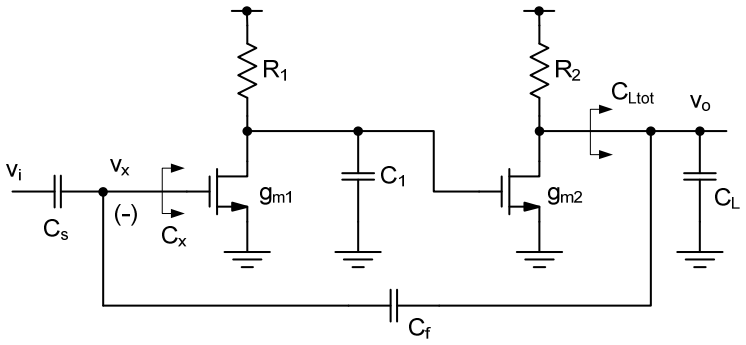
- Analysis of a basic two-stage OTA
  - Loop gain with capacitive feedback
  - Slewing
  - Noise
- Design example
  - Separate handout…

(Basic) Two-Stage OTA



- High gain ~ $(g_m r_o)^2$
- Large output range
- With cascodes in stage 1 the gain becomes ~$(g_m r_o)^3$

AC Model with Capacitive Feedback



$$R_1 = r_{o1} \| r_{o3}$$

$$R_2 = r_{o2} \| r_{o4}$$

$$\beta = \frac{C_f}{C_f + C_s + C_x}$$

$$C_x = C_{gs1} + C_{gb1} + 2C_{gd1}$$

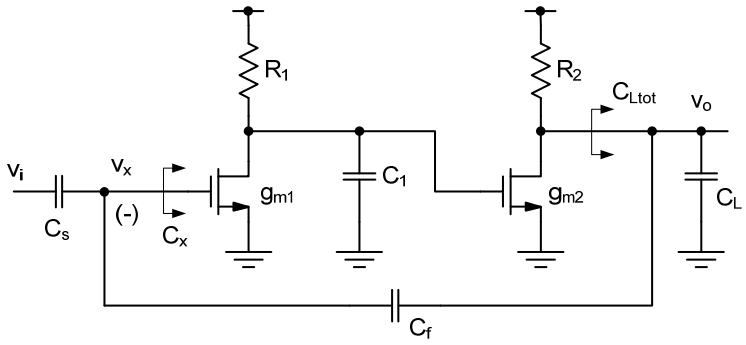
(assuming neutralization)

$$C_{Ltot} = C_L + (1-\beta)C_f + C_{db2} + C_{db4} + C_{gd4}$$

(ignoring C_{gd2} for the time being)

$$C_1 = C_{gs2} + C_{gb2} + C_{db1} + 2C_{gd1} + C_{db3} + C_{gd3}$$

Loop Gain

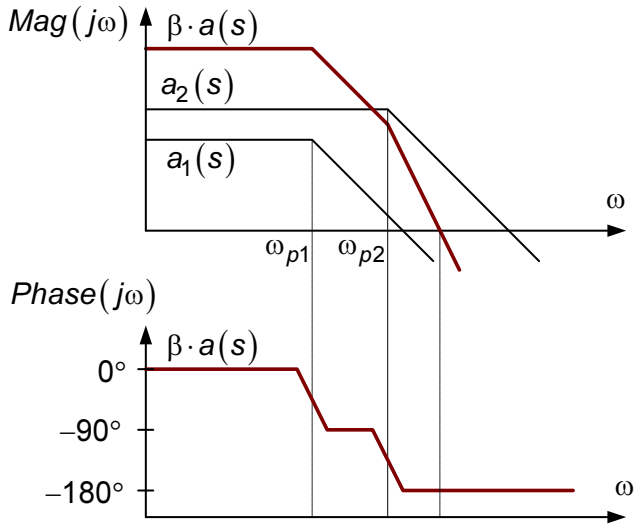


$$T(s) = \beta \frac{G_{m1}R_1 \cdot g_{m2}R_2}{\left(1 - \frac{s}{p_1}\right) \cdot \left(1 - \frac{s}{p_2}\right)} = \beta \cdot a_1(s) a_2(s) = \beta \cdot a(s)$$

$$p_1 = -\frac{1}{R_1 C_1}$$

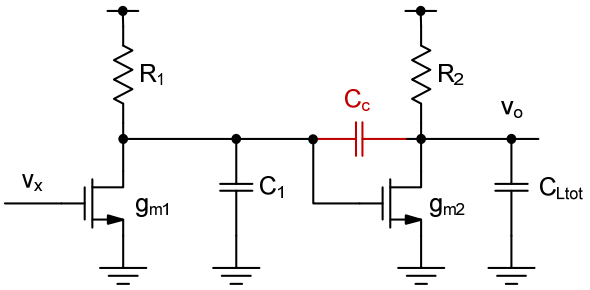
$$p_2 = -\frac{1}{R_2 C_2}$$

Bode Plot of Loop Gain



- If ω_{p1} and ω_{p2} are close to each other, the loop will have a very small phase margin

Miller Compensation



$$a(s)=\frac{v_o}{v_x}=\frac{g_{m1}R_1\cdot g_{m2}R_2\cdot\left(1-s\frac{C_c}{g_{m2}}\right)}{1+s\left[(C_{Ltot}+C_c)R_2+(C_1+C_c)R_1+g_{m2}R_2R_1C_c\right]+s^2R_1R_2\left(C_1C_{Ltot}+C_cC_{Ltot}+C_cC_1\right)}$$

- Very messy; need to simplify

Dominant Pole Approximation

- We can write the denominator as

$$D(s) = \left(1 - \frac{s}{p_1}\right) \cdot \left(1 - \frac{s}{p_2}\right) = 1 - s\left(\frac{1}{p_1} + \frac{1}{p_2}\right) + \frac{s^2}{p_1 p_2}$$

- Since in a practical design outcome we'll have $|p_1| << |p_2|$, we can approximate

$$D(s) \cong 1 - s\left(\frac{1}{p_1}\right) + \frac{s^2}{p_1 p_2}$$

- With this simplification, we can now easily identify p_1 and p_2 by comparing the coefficients with the expression from the previous slide

Result

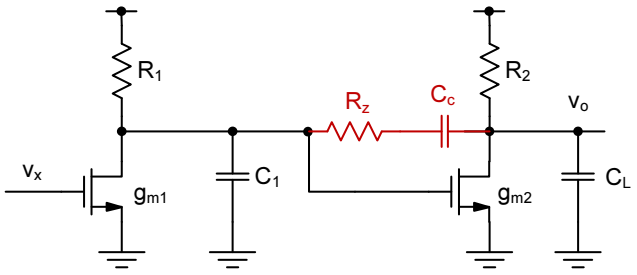
$$a(s) \cong a_0 \cdot \frac{\left(1 - \frac{s}{z}\right)}{\left(1 - \frac{s}{p_1}\right) \cdot \left(1 - \frac{s}{p_2}\right)} \qquad z = +\frac{g_{m2}}{C_c}$$

Right half plane (RHP) zero

$$p_1 \cong -\frac{1}{R_1(C_1 + C_c) + R_2(C_{Ltot} + C_c) + g_{m2}R_2R_1C_c} \cong -\frac{1}{g_{m2}R_2R_1C_c}$$

$$p_2 \cong -\frac{g_{m2}}{\frac{C_1C_{Ltot}}{C_c} + C_1 + C_{Ltot}} \qquad \frac{1}{\omega_{p2}} \cong \left(\frac{C_1}{g_{m2}} + \frac{C_{Ltot}}{g_{m2}}\right)\left(1 + \frac{\frac{C_{Ltot}C_1}{C_1 + C_{Ltot}}}{C_c}\right)$$

Nulling Resistor (1)

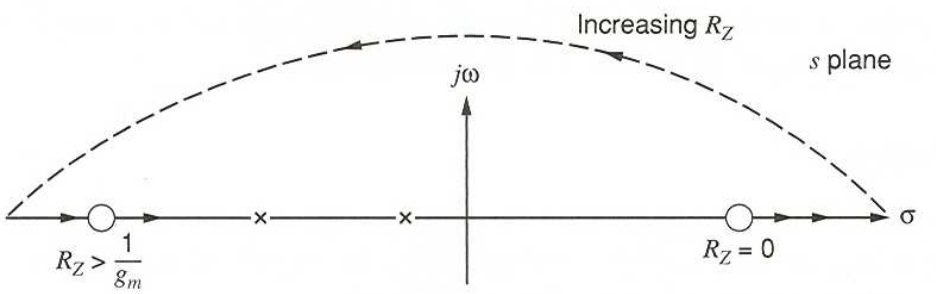


- New transfer function becomes

$$a(s) \cong a_0 \cdot \frac{1 - sC_c\left(\frac{1}{g_{m2}} - R_z\right)}{\left(1 - \frac{s}{p_1}\right)\cdot\left(1 - \frac{s}{p_2}\right)\cdot\left(1 - \frac{s}{p_3}\right)}$$

- p_1 and p_2 unchanged, new pole p_3, and a knob to tune the zero

Nulling Resistor (2)



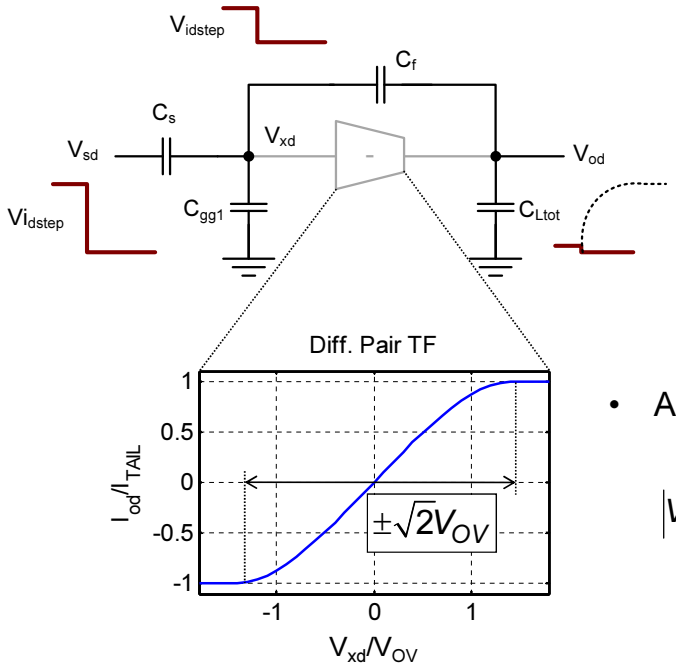
Gray & Meyer, 5th edition, page 647

- $R_z=1/g_{m2}$ pushes the zero to $+\infty$
- Can use a transistor in triode region to implement resistor
  - Helps track process variations

Resistive Load

- Can show that adding a resistive load at the output of stage 2 helps in splitting the two poles
  - For small R_2, smaller C_C needed to obtain good phase margin
- Cost
  - Lower loop gain, precision

Response to a Large Step

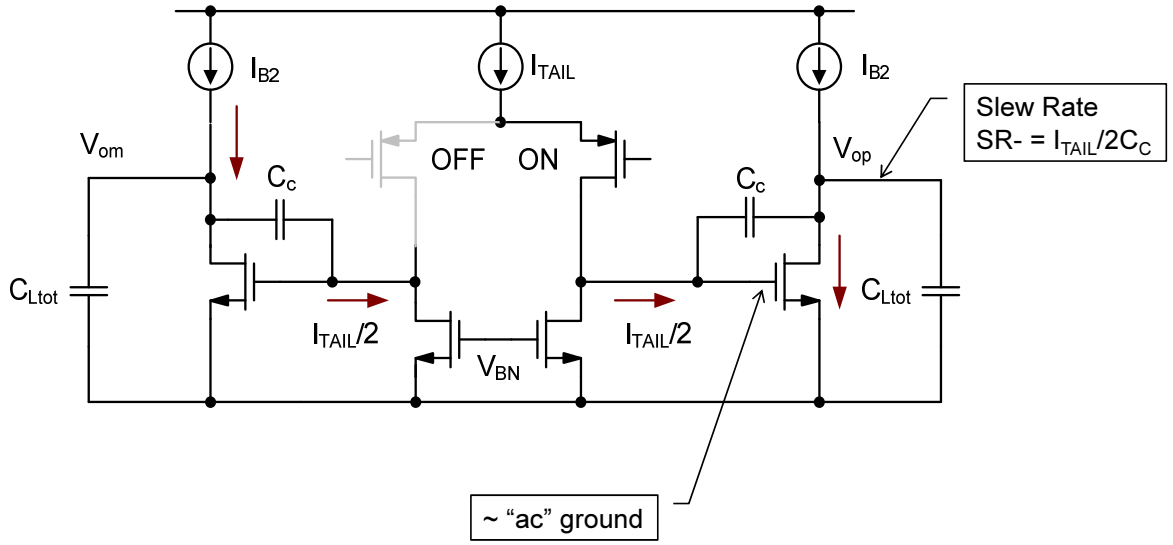


$$V_{xdstep} = \frac{V_{idstep} \cdot C_s}{C_s + C_{gg1} + \dfrac{C_f C_{Ltot}}{C_f + C_{Ltot}}}$$

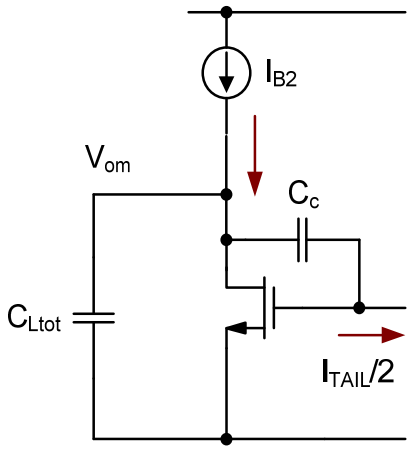
- Amplifier "slews" initially if

$$\left|V_{xdstep}\right| > \sqrt{2} V_{OV} \cong \frac{2\sqrt{2}}{g_m / I_D}$$

Slewing in a Two-Stage OTA (1)



Slewing in a Two-Stage OTA (2)



- Want V_{om} to slew up at the same rate that V_{op} slews down
  - Otherwise amplifier sees a large common mode and bias point disturbance
- This requires

$$\frac{I_{B2}}{C_{Ltot}+C_c} \geq \frac{I_{TAIL}/2}{C_c}$$

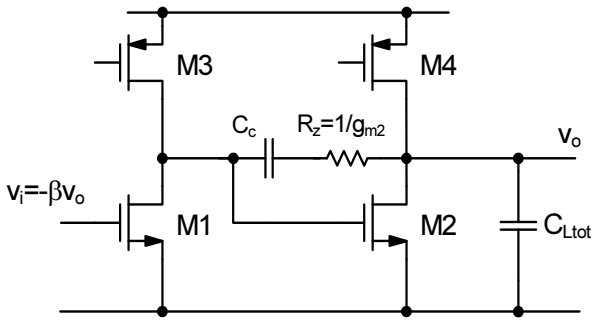
$$I_{B2} \geq \frac{I_{TAIL}}{2}\left(1+\frac{C_{Ltot}}{C_c}\right)$$

Slewing Time

$$SR = \frac{I_{TAIL}}{C_c}$$

$$t_{slew} = \begin{cases} 0 & for \quad |V_{xdstep}| < \dfrac{2\sqrt{2}}{g_m / I_D} \\ \dfrac{|V_{xdstep}| - \dfrac{2\sqrt{2}}{g_m / I_D}}{\beta \cdot SR} & else \end{cases}$$

Total Integrated Noise



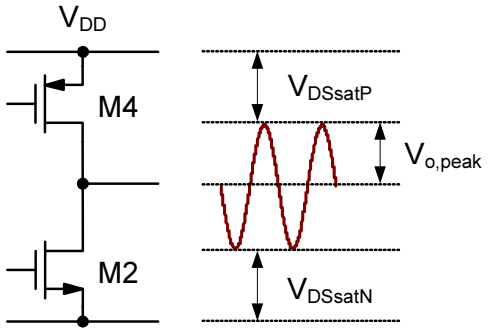
$$\overline{v_o^2} \cong \frac{1}{\beta} \cdot \frac{kT}{C_c} \gamma_n \left(1 + \frac{\gamma_p}{\gamma_n} \frac{g_{m3}}{g_{m1}} \right) + \frac{kT}{C_{Ltot}} \left[1 + \gamma_n \left(1 + \frac{\gamma_p}{\gamma_n} \frac{g_{m4}}{g_{m2}} \right) \right]$$

- Noise from 2nd stage may be significant for small C_{Ltot}
- Want to minimize g_{m3}/g_{m1} and g_{m4}/g_{m2} for low noise
  - Sometimes not possible due to swing constraints (small g_{m4} means small $(g_m/I_D)_4$, large V_{DSsat4})

A. Dastgheib and B. Murmann, "Calculation of total integrated noise in analog circuits," *IEEE Trans. on Circuits and Systems I,* Vol. 55, pp. 2988-2993, Nov. 2008

Dynamic Range

$$DR = \frac{P_{signal,max}}{P_{noise}} = \frac{0.5 \cdot V_{od,peak}^2}{\overline{v_{od}^2}}$$



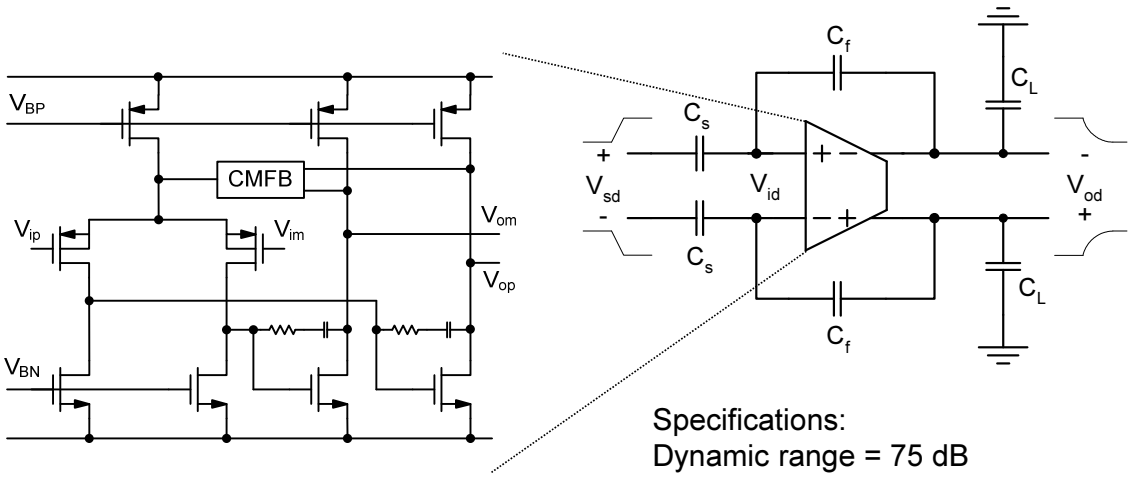
$$V_{o,peak} \le \frac{1}{2}(V_{DD} - V_{DSsatP} - V_{DSsatN})$$

$$V_{od,peak} \le (V_{DD} - V_{DSsatP} - V_{DSsatN})$$

$$\le \left(V_{DD} - \frac{2}{(g_m / I_D)_P} - \frac{2}{(g_m / I_D)_N} \right)$$

- For V_{DD}=1.8V, $V_{od,peak}$ ~ 1V is practical
  - Leaves 400mV headroom across loads, restricts $g_m/I_D > 5$

Design Example

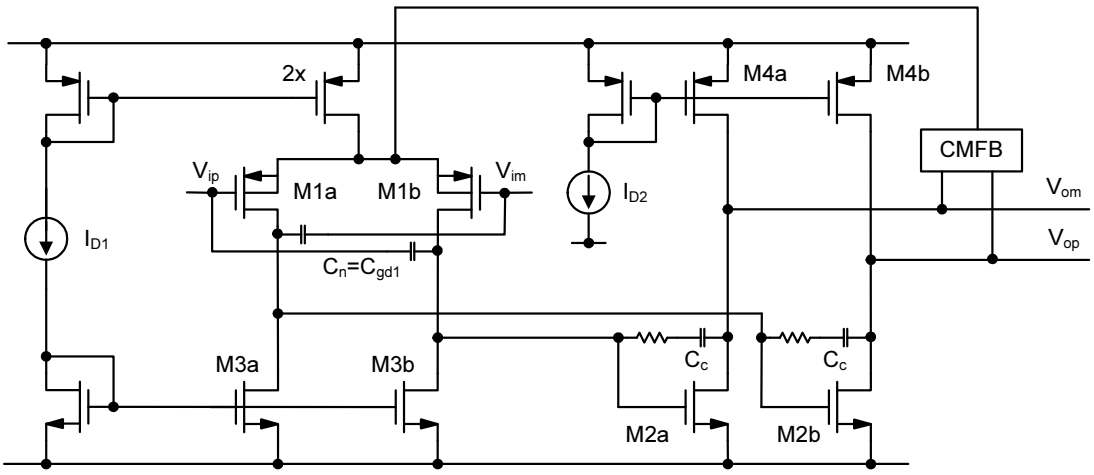


Specifications:
Dynamic range = 75 dB
Settling time = 10 ns
Dynamic Settling Error ≤ 0.1%
Static Settling Error ≤ 0.5%
C_L= 1pF, C_s = C_f = 1pF

Divide and Conquer Design Flow

- Optimization in Matlab
  - Step 1: Small-signal design
    - Ignore slewing; take into account only small-signal behavior
  - Step 2: Large-signal design
    - Compute slewing time; re-optimize design
- Simulation and implementation
  - Simplify simulation circuit as much as possible (while preserving all important signal path features)
    - Initially use ideal common mode feedback
    - Do not worry about exact finger partitioning of transistors
    - Do not worry about exact structure of bias network
    - …

Prototype Amplifier



- 11 Variables: I_{D1}, W_1, L_1, W_3, L_3, I_{D2}, W_2, L_2, W_4, L_4, C_c

Summary of Design Equations (Small-Signal)

$$DR = \frac{0.5 \cdot V_{od,peak}^2}{\overline{v_{od}^2}}$$

$$\overline{v_o^2} \cong \frac{1}{\beta} \cdot \frac{kT}{C_c} \gamma_n \left(1 + \frac{\gamma_p}{\gamma_n} \frac{g_{m3}}{g_{m1}} \right) + \frac{kT}{C_{Ltot}} \left[1 + \gamma_n \left(1 + \frac{\gamma_p}{\gamma_n} \frac{g_{m4}}{g_{m2}} \right) \right]$$

$$t_s \cong \frac{-0.7}{\omega_c} ln(\varepsilon_{d,spec})$$

(No slewing, PM≅75°)

$$\omega_c \cong \beta \frac{g_{m1}}{C_c} \qquad \beta = \frac{C_f}{C_s + C_f + C_{gg1}}$$

$$PM \cong tan^{-1}\left(\frac{\omega_{p2}}{\omega_c} \right) \qquad \omega_{p2} \cong \frac{g_{m2}}{\frac{C_1 C_{Ltot}}{C_c} + C_1 + C_{Ltot}}$$

$$|\varepsilon_s| \cong \frac{1}{T_0}$$

$$T_0 = \beta \cdot \frac{g_{m1}}{g_{ds1} + g_{ds3}} \cdot \frac{g_{m2}}{g_{ds2} + g_{ds4}}$$

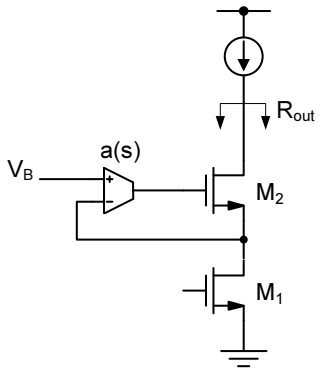
Optimization Approach

- Impossible to find a closed form solution to this design problem
  - Solution must be found iteratively
- Iterations can be easily done using a spreadsheet or Matlab
  - Using table-look-up of device parameters (g_m/I_D, f_T, …)
- Partition space into “primary” and “secondary” variables
  - Primary variables are the main knobs in your design; these have the largest impact on the critical tradeoffs
  - Secondary variables can be set using reasonable design choices and heuristics; subject to optimization in an “outer loop”
- See separate handout for examples…

More on OTAs: Outline

- Advanced OTA topologies
  - Making more gain
    - Gain boosting
    - Three+ stage amplification
- Common mode feedback implementation

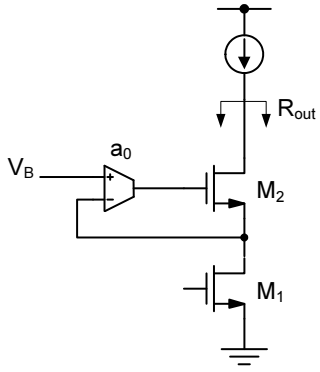
Gain Boosting



- Use an auxiliary feedback loop around cascode device to increase R_{out} and thus low-frequency gain of the overall cascode stage
  - Can be applied to either telescopic or folded cascode OTA architectures
- References
  - B. J. Hosticka, "Improvement of the gain of MOS amplifiers," IEEE J. Solid-State Circuits, pp. 1111-1114, Dec.1979.
  - K. Bult, G.J.G.M. Geelen, "A fast-settling CMOS op-amp for SC circuits with 90-dB DC gain," IEEE J. Solid-State Circuits, pp. 1379-1384, Dec. 1990.
  - D. Flandre et al., "Improved synthesis of gain-boosted regulated-cascode CMOS stages using symbolic analysis and g_m/I_D methodology," IEEE J. Solid-State Circuits, pp. 1006–1012, July 1997.
  - M. Das, "Improved design criteria of gain-boosted CMOS OTA with high-speed optimizations," IEEE Trans. Ckts. and Systems II, pp. 204-207, March 2002.

Basic Low Frequency Analysis

- Can use Blackman's impedance formula
  - See e.g. Gray & Meyer, 5th edition, p. 608



$$Z_{port} = Z_{port}(k=0) \cdot \frac{1+T(\text{port shorted})}{1+T(\text{port open})}$$

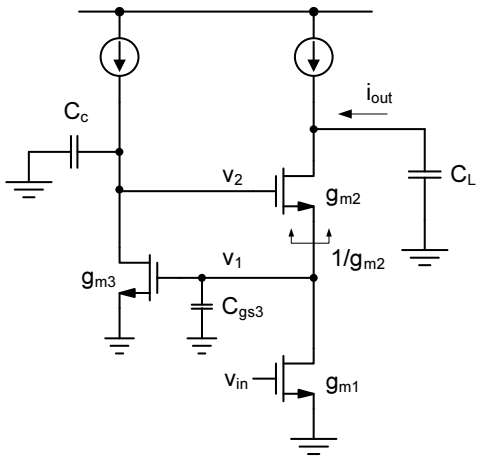
$$R_{out}(a_0 = 0) \cong r_{o2}(1+g_{m2}r_{01})$$

$$T(\text{port shorted}) \cong a_0 \frac{g_{m2}}{g_{m2}+g_{mb2}} \cong a_0$$

$$T(\text{port open}) = 0$$

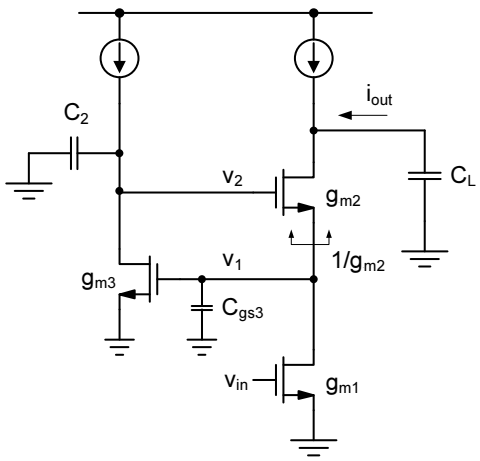
$$R_{out} \cong r_{o2}(1+g_{m2}r_{01}) \cdot (a_0+1)$$

High Frequency Analysis (1)



- Focus on simplest possible circuit first
- Assume $r_o \rightarrow \infty$
  - Finite r_o does not impact high frequency behavior
- Neglect backgate effect of M2
- Neglect C_{gs2} and all extrinsic capacitances for simplicity
- It turns out that the key issues are still retained with these simplifications

High Frequency Analysis (2)



- Loop gain

$$T(s) = \frac{g_{m3}}{sC_2}\frac{1}{1+s\dfrac{C_{gs3}}{g_{m2}}} = \frac{\omega_u}{s}\frac{1}{1+s\dfrac{C_{gs3}}{g_{m2}}}$$

- For reasonable phase margin, we need

$$\frac{g_{m2}}{C_{gs3}} = \omega_{p2} > \omega_u$$

$$\frac{g_{m2}}{C_{gs3}} = k\cdot\omega_u \qquad k = 2...4$$

High Frequency Analysis (3)

Given

$$0 = g_{m3}\cdot v_1 + s\cdot C_2\cdot v_2$$

$$0 = -g_{m2}\cdot(v_2 - v_1) + s\cdot C_{gs3}\cdot v_1 + v_{in}\cdot g_{m1}$$

$$i_{out} = (v_2 - v_1)\cdot g_{m2}$$

$$\text{Find}(v_1, v_2, i_{out})\ \text{simplify} \rightarrow \begin{bmatrix} -\dfrac{C_2\cdot g_{m1}\cdot s\cdot v_{in}}{C_2\cdot C_{gs3}\cdot s^2 + C_2\cdot g_{m2}\cdot s + g_{m2}\cdot g_{m3}} \\ \dfrac{g_{m1}\cdot g_{m3}\cdot v_{in}}{C_2\cdot C_{gs3}\cdot s^2 + C_2\cdot g_{m2}\cdot s + g_{m2}\cdot g_{m3}} \\ \dfrac{g_{m1}\cdot g_{m2}\cdot v_{in}\cdot(g_{m3} + C_2\cdot s)}{C_2\cdot C_{gs3}\cdot s^2 + C_2\cdot g_{m2}\cdot s + g_{m2}\cdot g_{m3}} \end{bmatrix}$$

$$G_m(s) = g_{m1}\cdot\frac{1 + s\dfrac{C_2}{g_{m3}}}{\dfrac{C_2}{g_{m3}}\cdot\dfrac{C_{gs3}}{g_{m2}}\cdot s^2 + \dfrac{C_2}{g_{m3}}\cdot s + 1} = g_{m1}\cdot\frac{1 + \dfrac{s}{\omega_u}}{\dfrac{s^2}{k\cdot\omega_u{}^2} + \dfrac{s}{\omega_u} + 1} = g_{m1}\cdot\frac{1 + \dfrac{s}{\omega_u}}{\dfrac{s^2}{\omega_P{}^2} + \dfrac{s}{\omega_P\cdot Q_P} + 1}$$

$$\omega_z = \omega_u$$

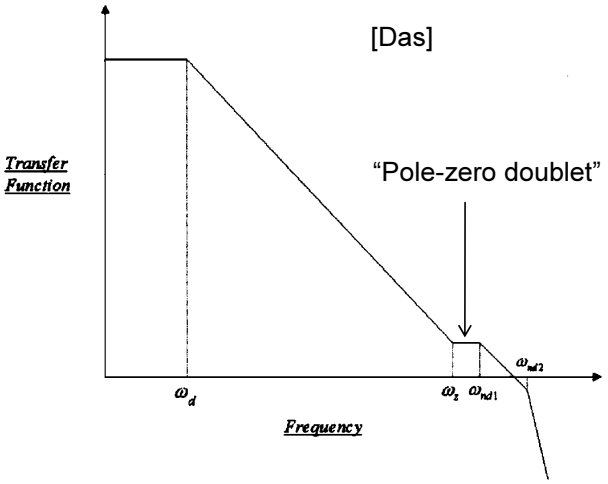
$$\omega_P = \sqrt{k}\cdot\omega_u$$

$$Q_P = \frac{1}{\sqrt{k}}$$

Voltage Transfer Function

$$a_{stage}(s) = \frac{v_{out}}{v_{in}} = \frac{G_m(s)}{sC_L}$$

$$= \frac{g_{m1}}{sC_L} \frac{1 + \frac{s}{\omega_u}}{1 + \frac{s}{\omega_u} + \frac{s^2}{k\omega_u^2}}$$



Issues with Pole-Zero Doublet (1)

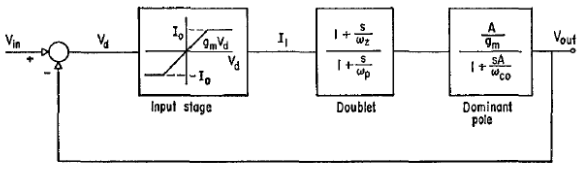
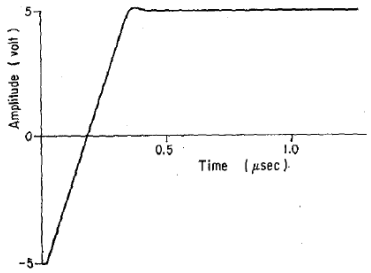


Fig. 1. Operational amplifier model for calculation of transient response.



$$V_{out}(t) \simeq V(1 - k_1 \exp[-\omega_{co}t] + k_2 \exp[-(t/\tau_2)]), \quad \text{for } t > T_s \qquad (1)$$

where

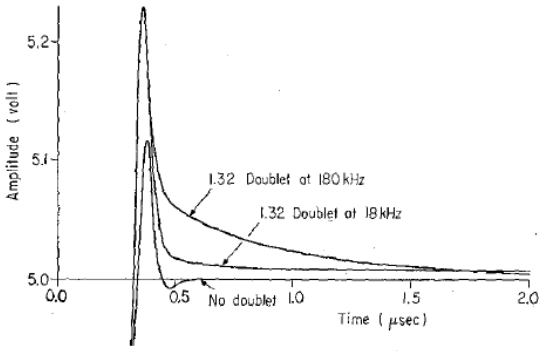
$$k_2 \simeq \frac{\omega_z - \omega_p}{\omega_{co}} \qquad (2)$$

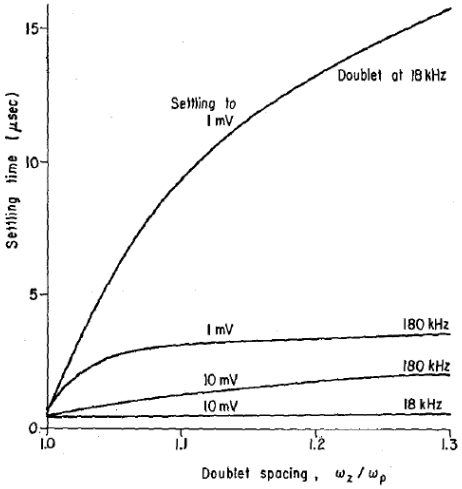
$$\tau_2 \simeq \frac{1}{\omega_z} \qquad (3)$$

T_s slewing period
ω_z doublet zero frequency
ω_p doublet pole frequency
ω_{co} $A \times$ (amplifier dominant pole) $\simeq$ unity-gain bandwidth
A open-loop low frequency gain.

B.Y.T. Kamath, R.G. Meyer and P.R. Gray, "Relationship between frequency response and settling time of operational amplifiers," IEEE JSSC, Vol. 9, No. 6, pp.347–352, Dec. 1974.

Issues with Pole-Zero Doublet (2)





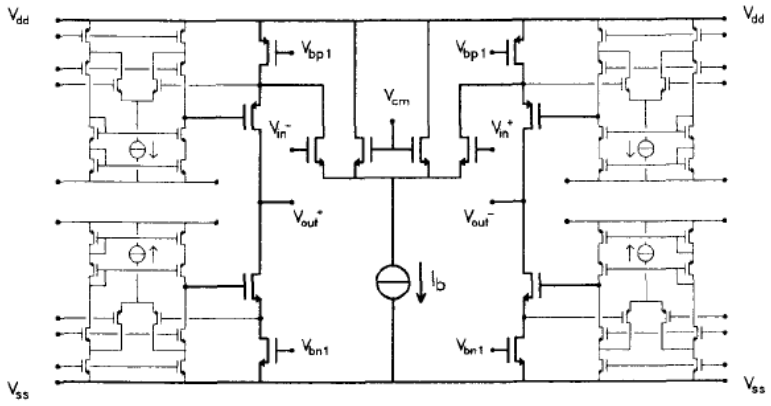
For fast and accurate settling, need either small pole-zero spacing or large ω_z

B.Y.T. Kamath, R.G. Meyer and P.R. Gray, "Relationship between frequency response and settling time of operational amplifiers," IEEE JSSC, Vol. 9, No. 6, pp.347–352, Dec. 1974.

Observations – Gain Boosting

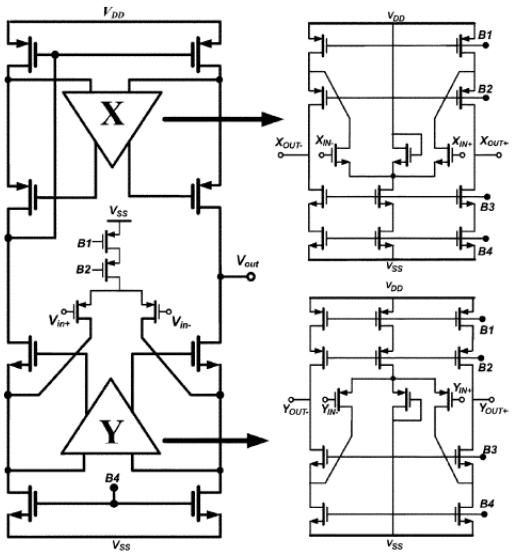
- Assuming that fast and accurate transient settling is required
  - The unity gain frequency of the auxiliary amplifier (ω_u) must be at a high frequency to avoid pole-zero doublet issues
  - On the other hand, we need $\omega_u < \omega_{p2} = g_{m2}/C_{gs3}$ for stability
- Rule of thumb
  - Place ω_u between unity gain frequency of overall feedback circuit (ω_c) and non-dominant pole (ω_{p2})
- Practical design outcomes have shown that gain boosting adds only about 20-30% to the total power dissipation of an OTA
  - Mostly because $C_2 < C_L$

Implementation Examples (1)



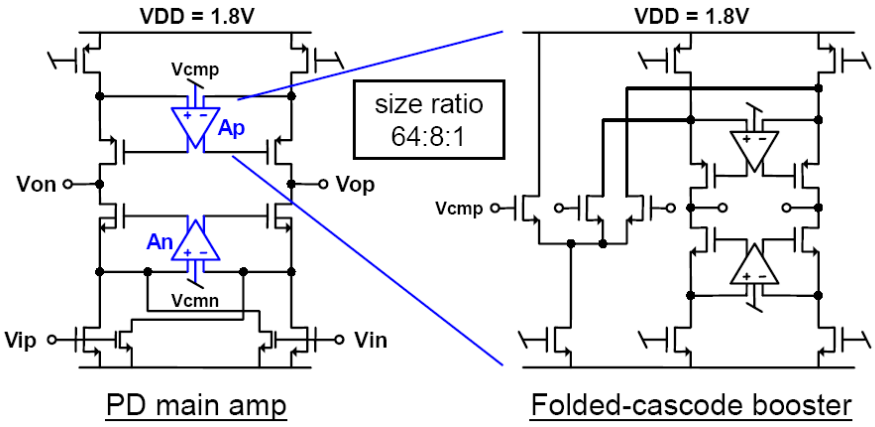
[Bult]

Implementation Examples (2)



M.M. Ahmadi, "A New Modeling and Optimization of Gain-Boosted Cascode Amplifier for High-Speed and Low-Voltage Applications," IEEE TCAS II, pp. 169-173, March 2006.

Implementation Examples (3)

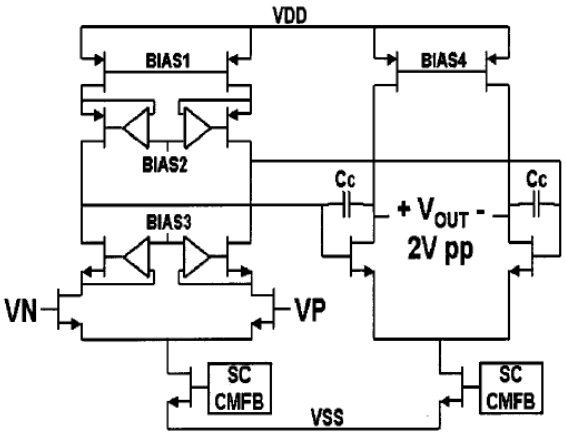


[Chiu et al., ISSC 2004]

- Gain boosted gain boosters!
- Gain ~ $g_m r_o^6$, design achieved a_{v0}=130dB in 0.18μm technology

Implementation Examples (4)

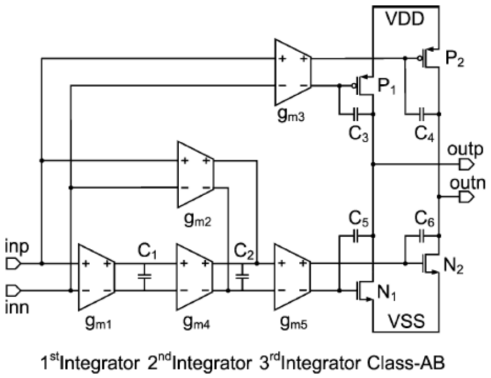
[Yang et al., JSSC 12/2001]



- Differential pair (instead of CS stages) and separate common mode feedback in second stage

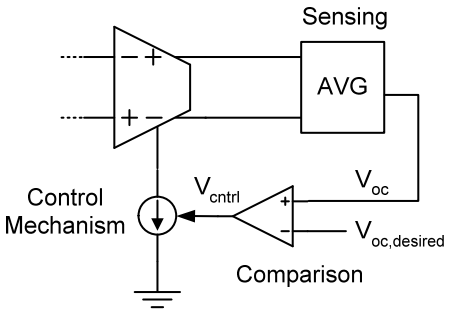
Four Stage Amplifier

[Mitteregger, ISSCC 2006]



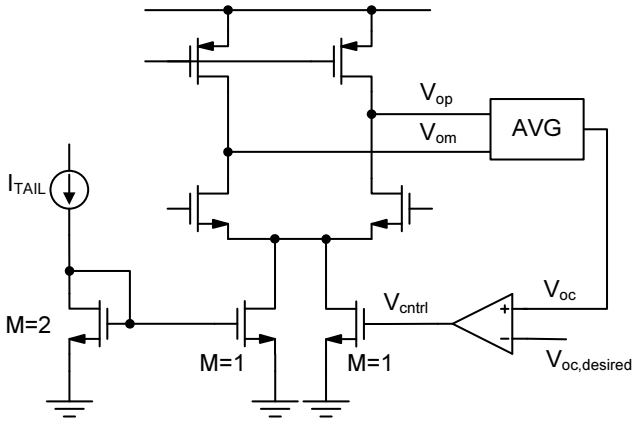
- Uses “nested Miller compensation”
  - See Gray & Meyer, chapter 9
- Manageable design problem for continuous time circuits
  - Very hard to design for applications that require fast settling
    - E.g. SC circuits

Common Mode Feedback



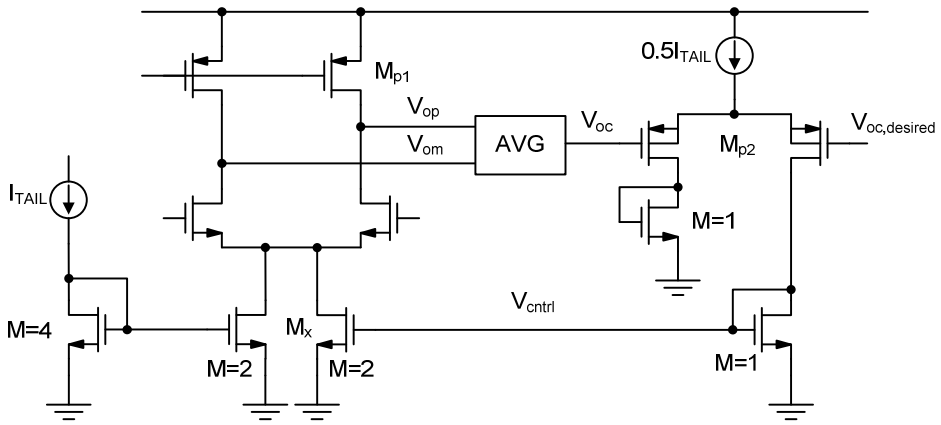
- Implementation aspects
  - How to sense
  - How to compare to desired value
  - How to provide a "knob" for adjusting V_{oc}

Knob



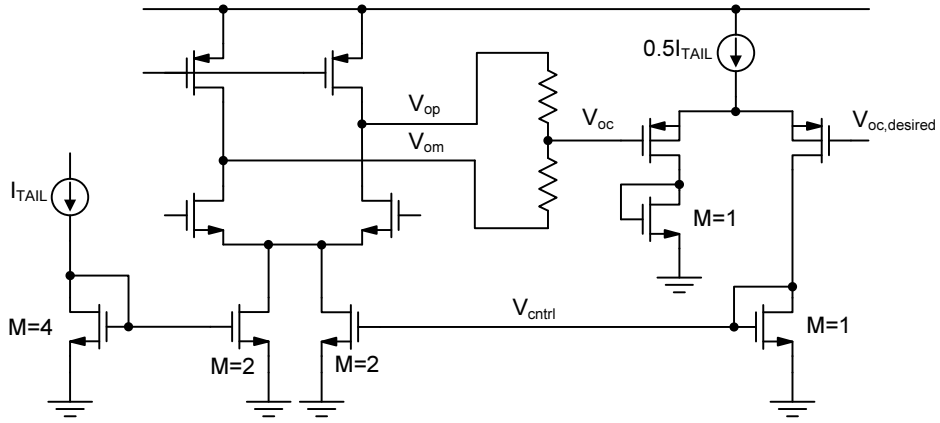
- Typically generate ~50% of tail current with fixed bias, leave remaining 50% as tuning range for CMFB loop

Comparison Circuit



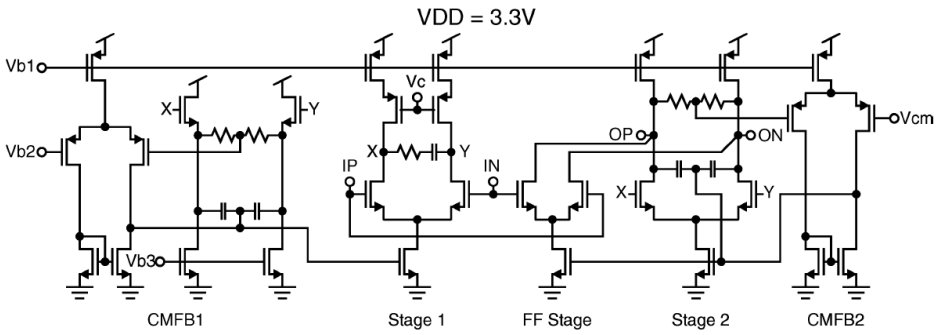
- Low frequency loop gain $T_0 \cong g_{mx} \cdot r_{op1}/2 \cdot (g_{mp2}/2)/(g_{mx}/2)$
  - Loop will control V_{oc} more accurately if M_{p1} is cascoded

Sensing



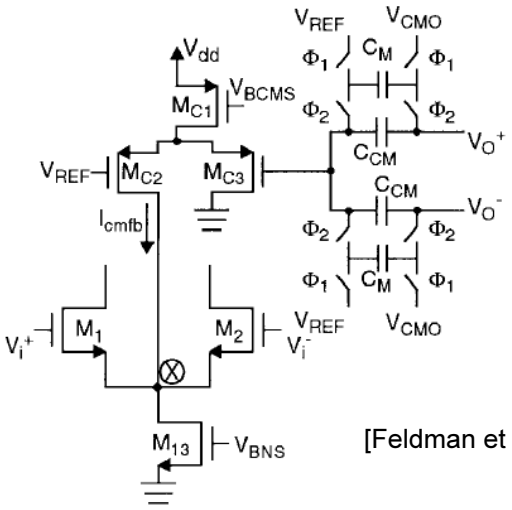
- Using a resistive divider may “destroy” differential gain
- Solutions
  - Use source followers to drive divider (headroom issue)
  - Purely capacitive sensing

Resistor-Based CMFB Example



R. Schreier, et al., "A 375-mW Quadrature Bandpass Delta Sigma ADC With 8.5-MHz BW and 90-dB DR at 44 MHz," IEEE J. *Solid-State Circuits,* vol. 41, no. 12, pp.2632-2640, Dec. 2006.

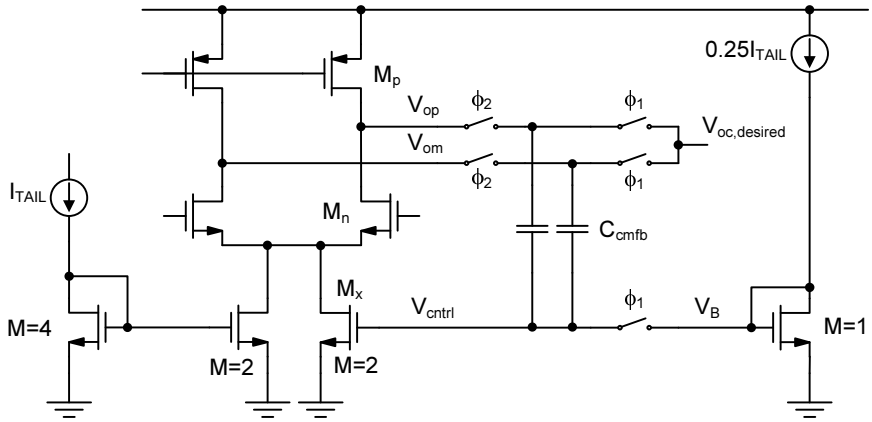
SC CMFB Implementation Example



- Circuit uses switched capacitors (C_M) to set the voltage across sensing capacitors (C_{CM})

[Feldman et al., JSSC 10/1998]

"Passive" CMFB (1)

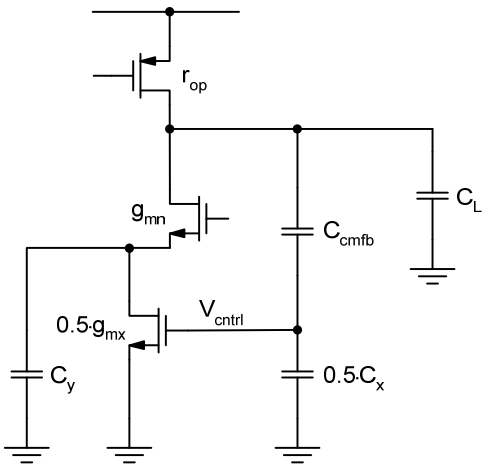


- During $\phi 1$: Initialize voltage across C_{cmfb} to $V_{oc,desired} - V_B$
- During $\phi 2$: Activate feedback loop
  - If $V_{oc} > V_{oc,desired}$, V_{cntrl} becomes $> V_B$ and lowers V_{oc}

"Passive" CMFB (2)

- OTA cannot be used during $\phi 1$, because the common mode feedback mechanism is inactive
  - Often not a problem in switched capacitor circuits, where the OTA is active only during one half-cycle
- Can use switched capacitor scheme shown on slide 181 to enable uninterrupted common mode feedback
- Unfortunately, this simple circuit cannot be used if an additional inversion is needed in the common mode feedback loop
  - E.g. won't work for a two-stage OTA that uses a single common mode feedback loop
  - Will work for the two-stage OTA with separate CMFB loops as shown on slide 171

Common Mode Half Circuit



- Low frequency loop gain

$$T_0 \cong \frac{g_{mx}}{2} r_{op} \cdot \frac{C_{cmfb}}{C_{cmfb} + \frac{C_x}{2}}$$

- Loop crossover frequency

$$\omega_c \cong \frac{1}{2} \frac{C_{cmfb}}{C_{cmfb} + \frac{C_x}{2}} \frac{g_{mx}}{C_L + \frac{C_{cmfb} \cdot 0.5C_x}{C_{cmfb} + 0.5C_x}}$$

- Nondominant pole

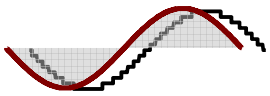
$$\omega_{p2} \cong \frac{g_{mn}}{C_y}$$

CMFB Design Considerations

- The required bandwidth of the common mode loop strongly depends on the amount of expected imbalance, common mode transients or ac components
  - In an ideal world, the common mode is not affected by the signal and hence stays constant
    - In this case, the bandwidth of the CMFB loop is unimportant
- For robustness in practical implementations, the bandwidth of the common mode loop is often chosen to be about 30% of the differential signal path bandwidth
  - In a typical switched capacitor circuit with 10 time constants differential settling, this means that the common mode has about 3 time constants to settle
    - Enough time to remove 95% of common mode disturbance

Precision Analog Circuit Techniques

Partly adapted from Kofi Makinwa's EE315A guest lecture in Spring 2009
[http://ei.ewi.tudelft.nl/people/biography/projectleaders/makinwa_kofi.htm]



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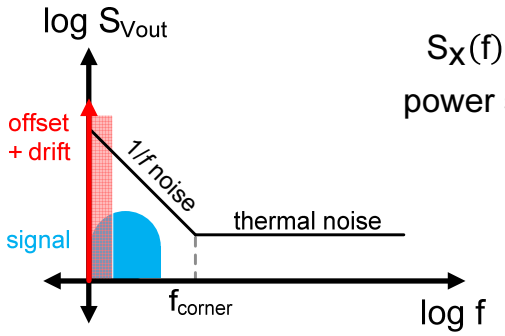
Outline

- Precision analog circuit techniques
  - Introduction, applications
- Fundamental circuit nonidealities
  - Mismatch/offset
  - Low frequency noise
- Circuit techniques
  - Autozeroing / Correlated double sampling (CDS)
  - Chopping
- Summary
- References

Precision Analog Circuit Techniques

- Techniques that mitigate low frequency circuit nonidealities
  - Autozeroing, correlated double sampling, chopping, dynamic element matching
  - Used to achieve high precision in spite of device limitations
    - Mismatch (leading to offset)
    - Low frequency noise (primarily 1/*f*)

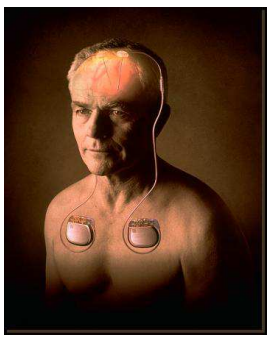


$S_X(f) \triangleq \mathcal{F}\{R_{XX}(\tau)\}$

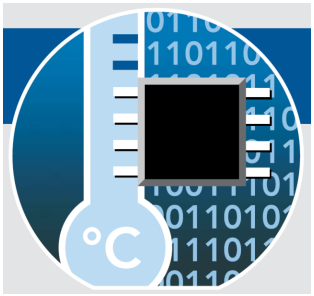
power spectral density

Where are these techniques useful?

- Sensor interfaces requiring DC accuracy (μV, nV level offsets)
- Low frequency signal conditioning (e.g. bio)
- Data converters (ADC, DAC)



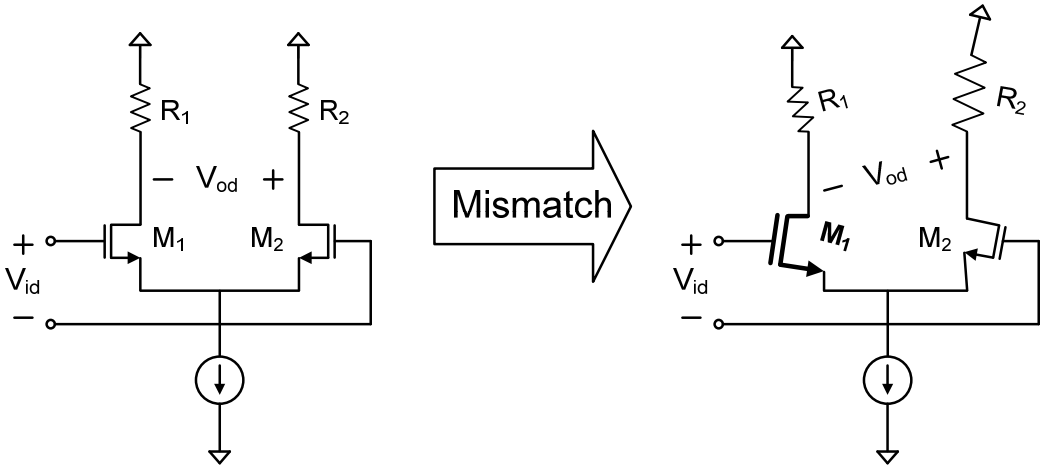
Medtronic



ZMDI

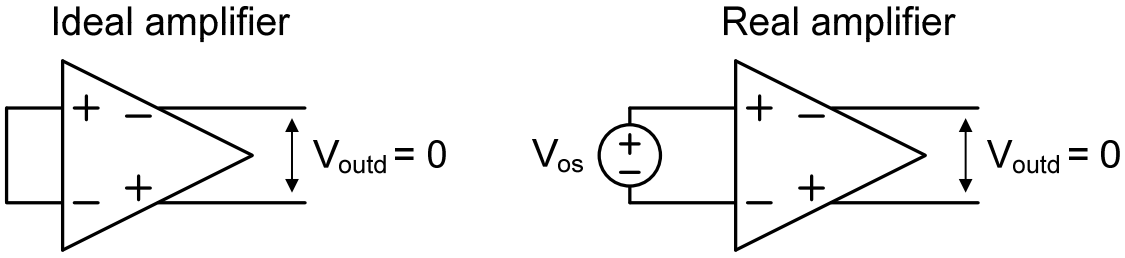
Mismatch

- Device mismatch results in circuit nonidealities
  - Incorrect ratios (e.g. current mirrors, feedback networks)
  - Asymmetry in differential circuits (e.g. amplifiers)



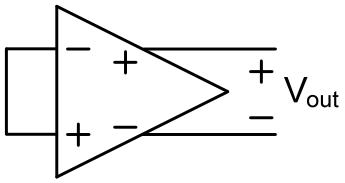
Offset

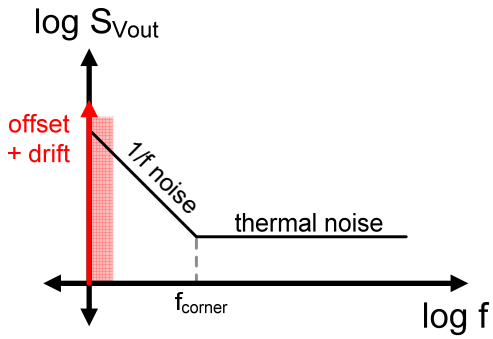
- Offset in amplifiers and comparators
  - The offset V_{os} is the input voltage required to zero the output
  - Equivalent to input-referring all internal sources of imbalance
  - Typically on the order of 1-10mV for CMOS



Low Frequency Nonidealities

- Amplifiers and other electronic systems deviate from ideal operation near DC
  - DC Offset resulting from component mismatch
  - Time varying offset (e.g. temperature induced)
  - Low frequency noise sources
    - 1/*f* noise (CMOS)





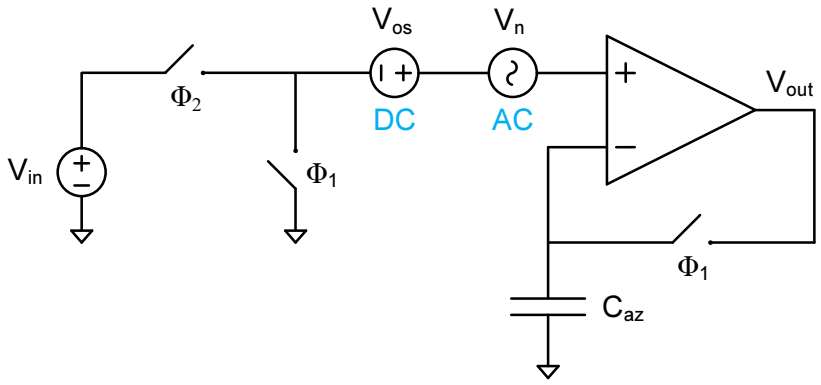
Dealing with these Nonidealities

- Using large devices improves offset and 1/*f* noise
  - Difficult/inefficient to achieve <100μV V_{os}, <1kHz 1/*f* corner
- Post fabrication circuit trimming
  - Can reduce V_{os} to <1μV, but still can have 100μV drift over temperature
- Precision analog circuit techniques are required for very high levels of accuracy
  - <1μV V_{os}, <10mHz 1/*f* corner
- Digital Calibration
  - Static offset cancellation is fairly common, high precision dynamic cancellation is difficult/inefficient

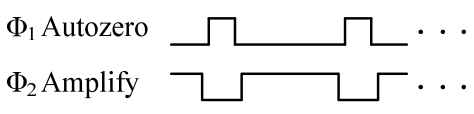
Precision Analog Circuit Techniques

- Precision analog circuit techniques can be used to
  - Reduce DC offsets (static)
  - Reduce time varying offset and low frequency noise (dynamic)
  - Improve PSRR and CMRR
- These techniques can be applied to amplifiers, sensors, at the system level etc..
- Major classifications
  - Autozeroing: measure the low frequency content and then subtract it from the signal path
  - Chopping: modulate the signal band to higher frequencies, far removed from the low frequency nonidealities
  - Dynamic Element Matching (DEM): periodically rotate elements to achieve higher precision on average

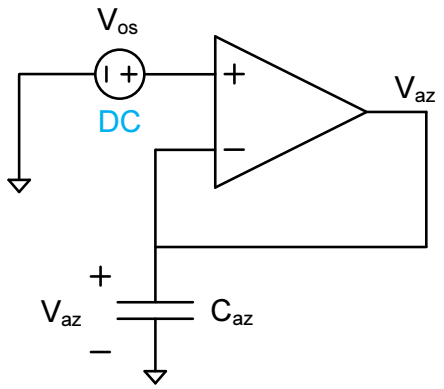
Input Autozeroed Amplifier



- Model the real (nonideal) amplifier by an ideal amp with input referred noise and offset sources
- Two phase nonoverlapping clocks
  - Autozero phase Φ_1
  - Amplification phase Φ_2



Φ_1 Autozero phase
DC Analysis



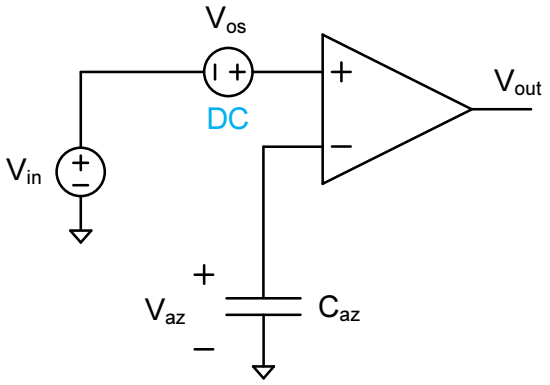
DC Analysis: $V_n \rightarrow 0$

$$V_{az} = A_0(V_{os} - V_{az})$$

$$\therefore V_{az} = \frac{A_0}{1 + A_0} V_{os}$$

- The amplifier's offset is stored on the autozero capacitor C_{az}
- Finite gain determines the maximum achievable accuracy
- The amplifier is unavailable for signal amplification

Φ_2 Amplification phase
DC Analysis



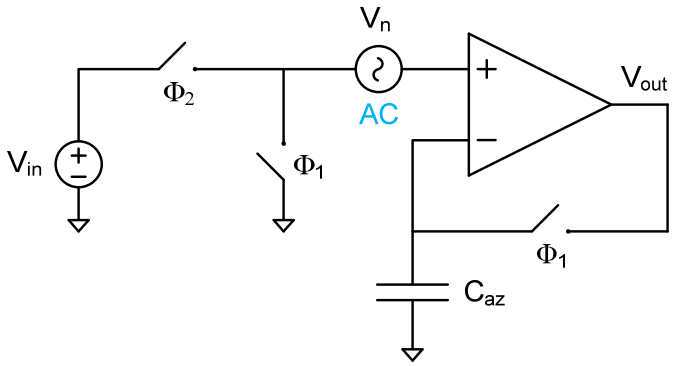
DC Analysis: $V_n \rightarrow 0$

$$V_{out} = A_0\left(V_{in} + V_{os} - \frac{A_0}{1 + A_0} V_{os}\right)$$

$$\therefore V_{out} = A_0\left(V_{in} + \frac{V_{os}}{1 + A_0}\right)$$

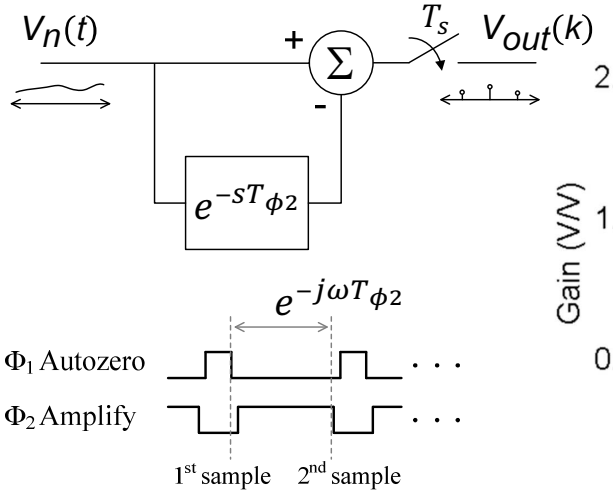
- The input signal is amplified, the amplifier's output is valid
- The offset is suppressed below the signal level by $(1+A_0)$
  - Imperfect cancellation due to finite gain during the AZ phase

Input Autozeroed Amplifier AC Analysis

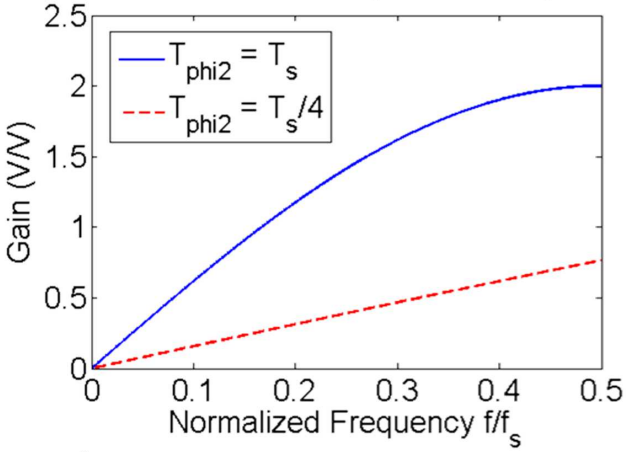


- The amplifier's noise and drift are sampled and held on C_{az}
  - The residual noise at V_{out} is the difference between the sampled noise and the 'present' value of the noise
  - Low frequency noise doesn't change rapidly → good rejection
  - High frequency noise is aliased, folds back into low freqs
  - If the output is discrete time this is correlated double sampling

Correlated Double Sampling



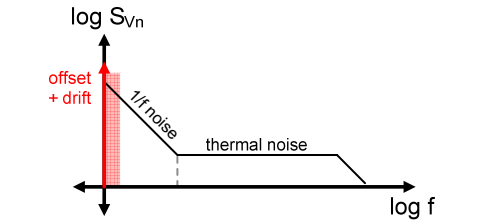
$$|H_{CDS}(s)| = |1 - e^{-sT_{\phi 2}}|$$

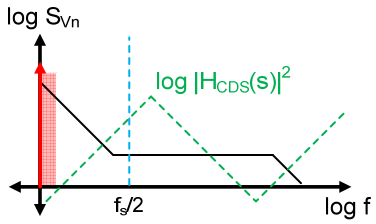


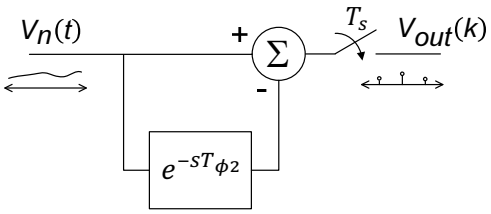
- The discrete time case of autozeroing
  - Common in switched capacitor circuits, data converters..
  - Analyze at the output sampling instant → end of Φ_2

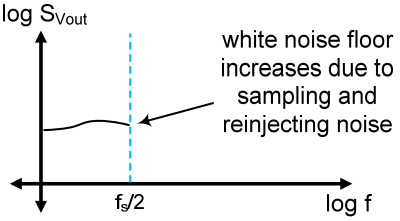
Noise Rejection and Aliasing

- Noise is filtered by $H_{CDS}(s)$ and folds into $f_s/2$
  - Residual noise spectrum is approximately flat given enough undersampling (see chapter 5)
  - Should have f_s >> 1/*f* corner for good supression of 1/*f* noise

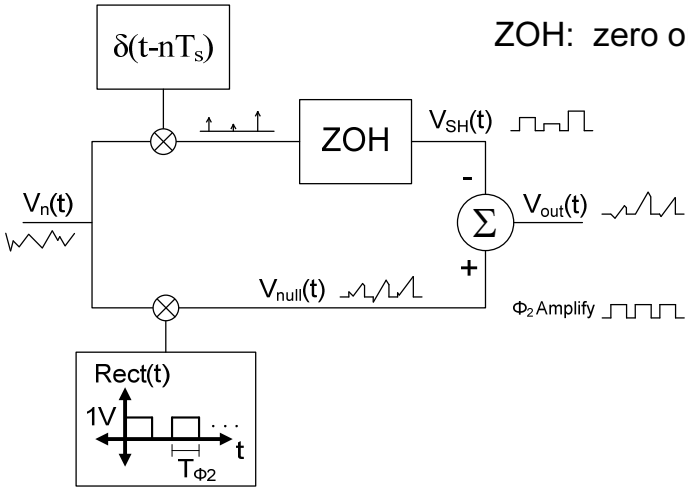








Continuous Time Autozero Analysis



- Continuous time analysis, similar to [Enz, Temes]
  - Low frequency noise sees a high pass filter
  - High frequency noise folds back into baseband and is shaped

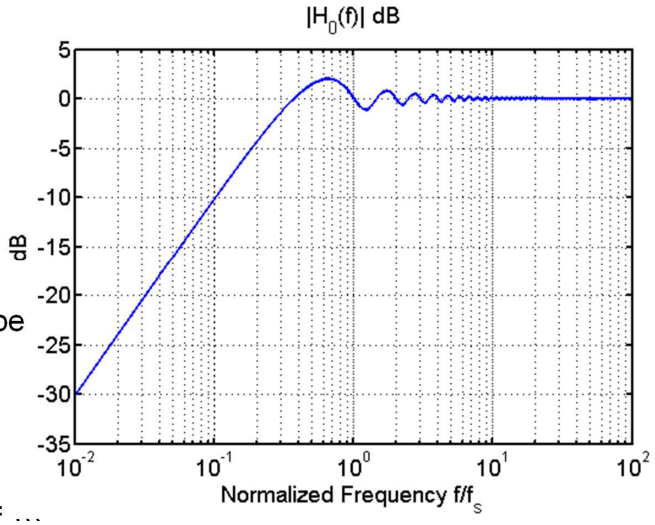
Baseband Noise Transfer Function

$$V_{SH}(f) = H_{ZOH}(f) \sum_{m=-\infty}^{m=\infty} V_n(f - mf_S)$$

$$V_{null}(f) = \sum_{m=-\infty}^{m=\infty} a_m V_n(f - mf_S)$$

$H_{ZOH}(f)$: Zero order hold sinc envelope

a_m : Rect function Fourier coefficients



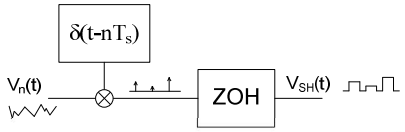
At baseband: m=0

$$V_{out}(f) = a_0 V_n(f) - H_{ZOH}(f) V_n(f) = \ldots$$

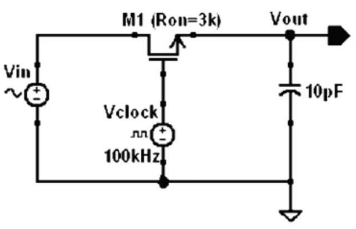
$$|H_0(f)|^2 = \left(\frac{T_{\Phi 2}}{T_S}\right)^2 \left(\left[1 - \frac{\sin(\omega T_{\Phi 2})}{\omega T_{\Phi 2}}\right]^2 + \left[\frac{1 - \cos(\omega T_{\Phi 2})}{\omega T_{\Phi 2}}\right]^2 \right)$$

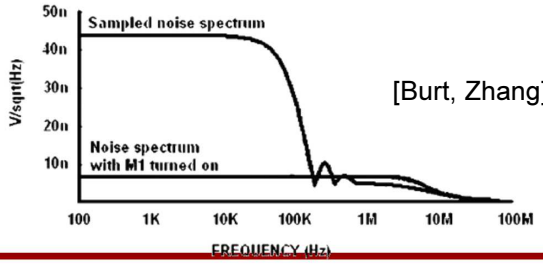
Noise Aliasing – Continuous Time

- High frequency noise is folded back as a result of sampling onto C_{az}
  - Noise samples are then held by the ZOH function
    - Leads to sinc shaping
- The held value is reinjected into the signal path during amplification
- Similar to noise in a track-and-hold for high undersampling ratios [2]



$$V_{SH}(f) = H_{ZOH}(f) \sum_{m=-\infty}^{m=\infty} V_n(f - mf_S)$$

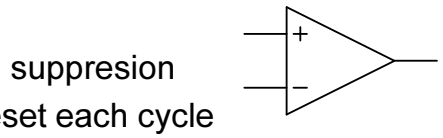




[Burt, Zhang]

Impact of Circuit Nonidealities

- Finite amplifier gain
  - Limits maximum suppresion for input-referred schemes
- Finite amplifier bandwidth
  - Dynamic settling errors degrade AC suppresion
    - Can be complicated, C_{az} isn't reset each cycle
- Charge injection from switches (discussed in EE315B)
  - Creates residual DC offset
  - Can be mitigated to some degree
    - Large C_{az} values, small switches
    - Fully differential design
    - Clock edge rates
    - Dummy switches



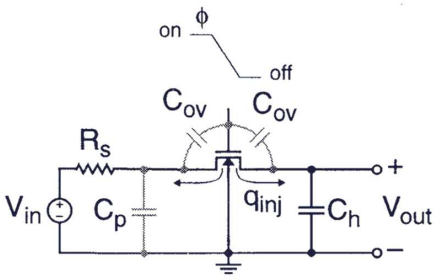
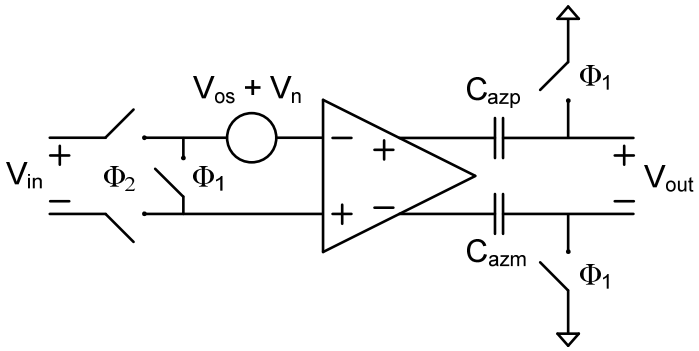


Fig. 18. Basic S/H circuit.

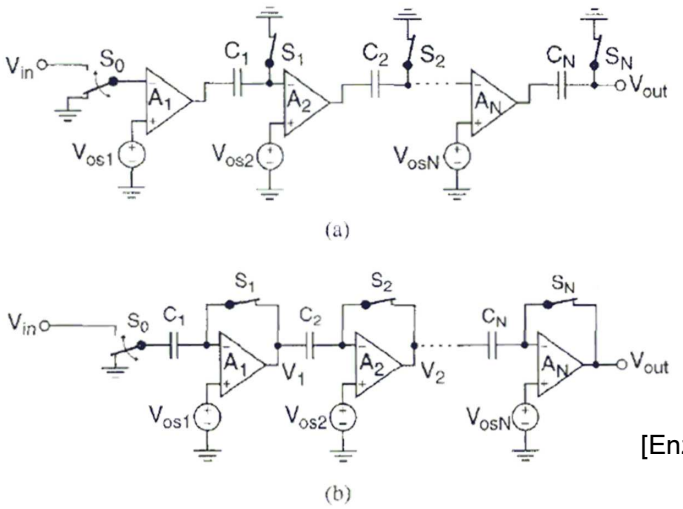
[Enz, Temes]

Output Referred Autozeroing



- Here finite gain doesn't limit the maximum supression
  - But maximum gain is limited, the amplified offset can rail the amp
- Charge injection from the autozero switches is less severe
  - Input refers through the amplifier's gain

Multistage Offset Cancellation



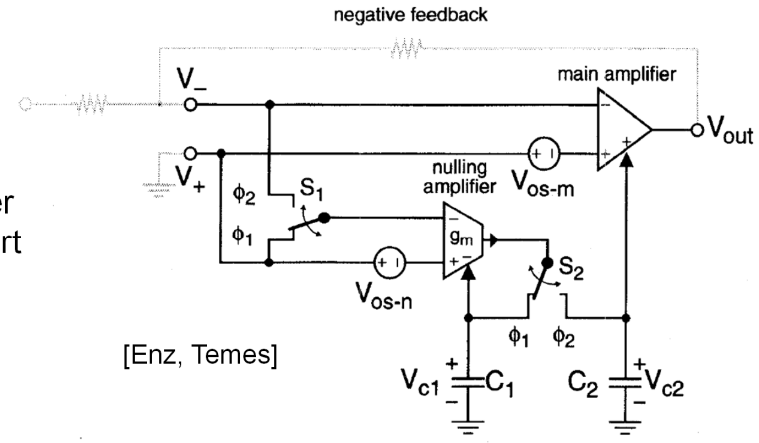
[Enz, Temes]

- Autozero each stage of a multi-stage design
  - High resolution comparator preamplifiers
  - Distributed gain stages

Offset Stabilized Amplifier

A_m gain of main amplifier
A_n gain of nulling amplifier
A_p gain through nulling port

$A_{overall} = A_m + A_n A_p$

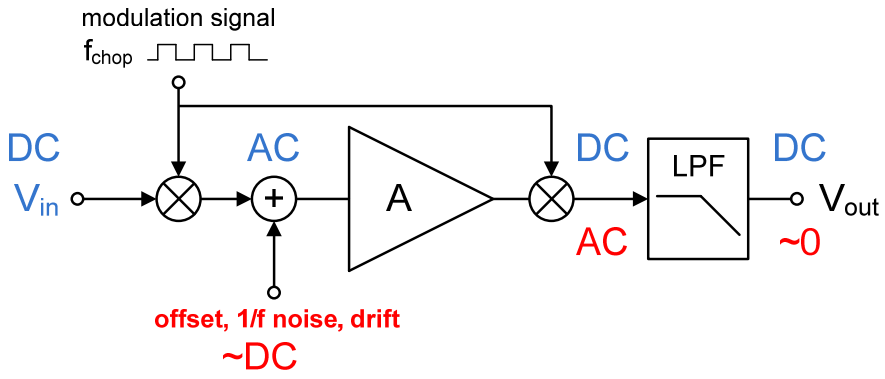


[Enz, Temes]

Fig. 26. Continuous-time AZ amplifier using feedforward technique.

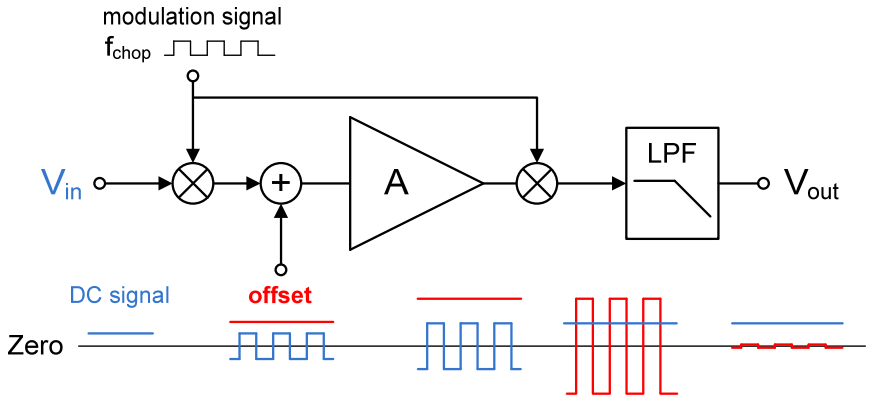
- Also called continous time autozero amplifier
  - Use an autozeroed amplifier in an auxillary path
  - Can achieve very high DC gain
    - Noise performance usually dictates large off-chip caps C_1,C_2

Chopping



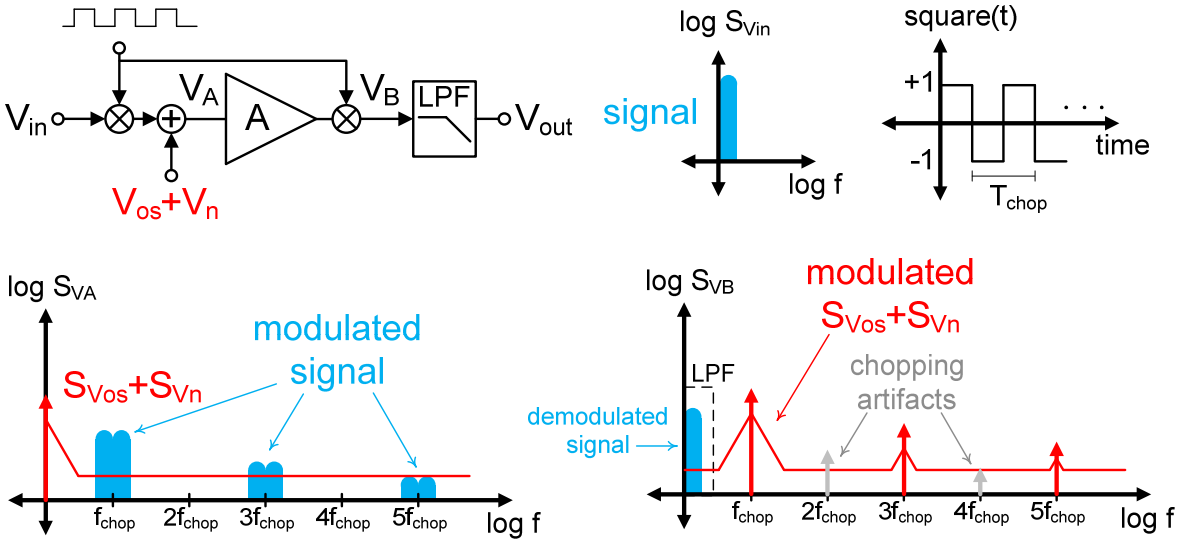
- Chopping is a modulation technique
  - The input signal is modulated to higher frequencies, amplified, then demodulated
  - Low frequency nonidealities at the amplifier output are modulated to higher frequencies by the output chopper, then are filtered out by the low pass filter

Chopping in the Time Domain



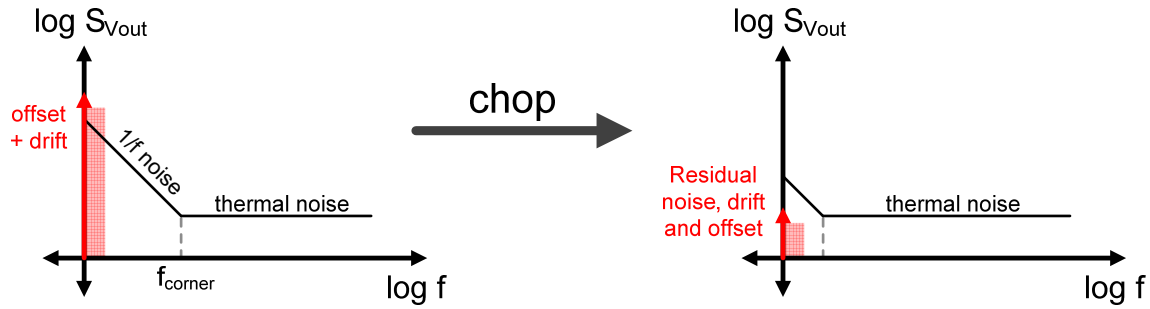
- An input signal at DC will pass through the amplifier as a square wave and get demodulated back to DC by the output chopper
- The amplifier's DC offset is amplified and modulated to a square wave at the output, filtered by the LPF (chopper ripple)
- Residual offset occurs if the modulation clock is not 50% duty cycle, can use a flip flop here

Chopping in the Frequency Domain



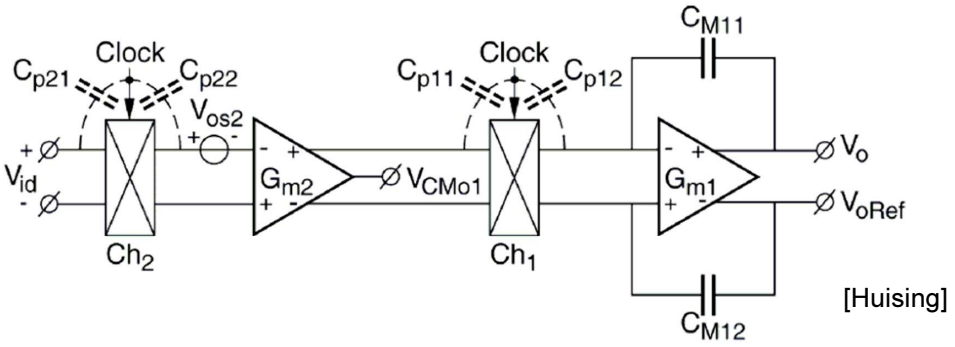
- Square wave modulation signal contains only odd harmonics
  - From symmetric positive and negative excursions

Residual Low Frequency Noise



- 1/*f* noise of chopped devices is completely removed for $f_{chop} >> f_{corner}$
  - Some residual inevitably remains
    - 1mHz f_{corner} has been reported [Wu, Makinwa]
- Thermal noise is not increased
  - No sampling, in contrast to autozero
  - Shuffled around in frequency but no net increase
    - High freq characteristics don't change significantly if BW >> f_{chop}

Chopped OTA Implementation

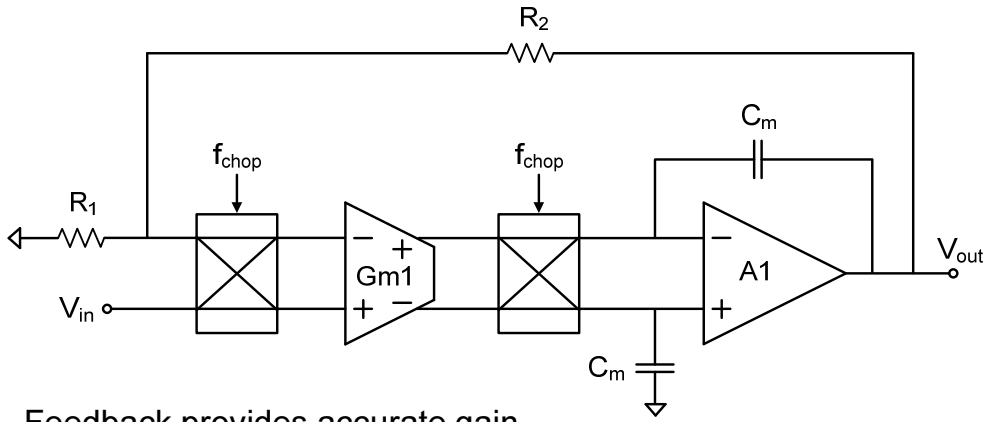


[Huising]

Fig. 17 Chopper OpAmp with cont-time transfer. Vos =~ 10 μV, Vrip =~ 10 mV

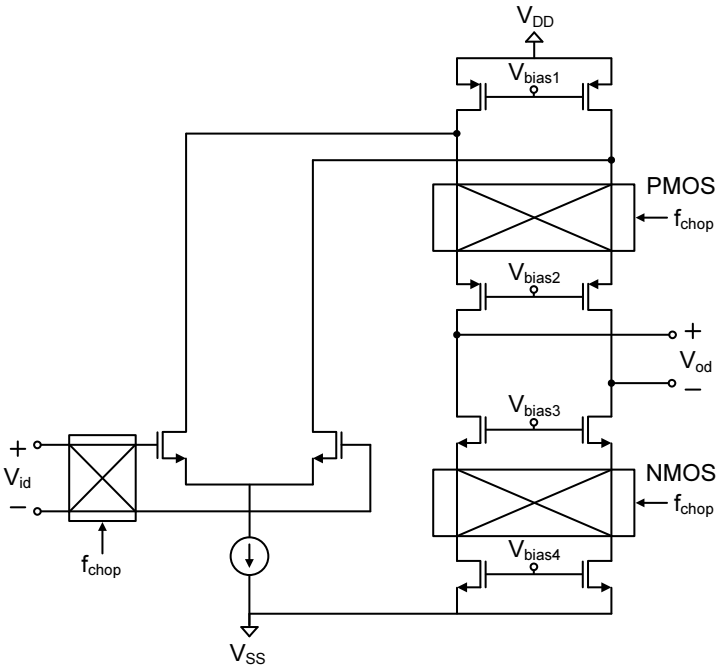
- Square wave modulators are easy to make in differential circuits
  - CMOS switches swap the plus/minus signal paths
- Miller compensation network can act as the low pass filter
  - Elegantly chop inside an amplifier

Chopper Op Amp with Feedback



- Feedback provides accurate gain
- Miller compensation filters out the high frequency components
  - Output ripple at f_{chop} can be large due to Gm1's modulated offset
  - High f_{chop} frequency minimizes chopper ripple
- High gain in Gm1 suppresses input referred offset due to A1

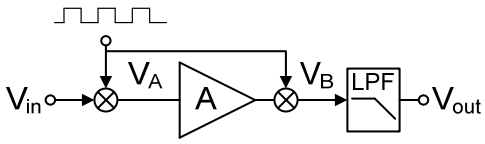
Chopped Folded Cascode Amplifier

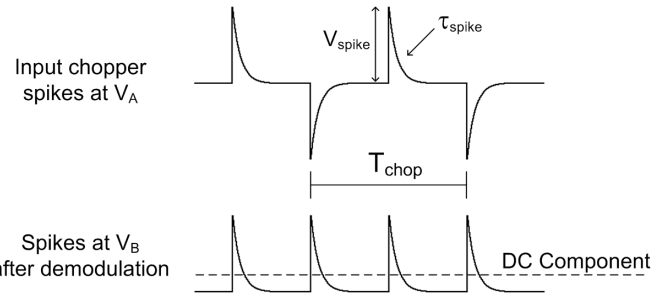


- Ubiquitous topology for chopped architectures
- Output choppers are placed at low impedance nodes (fast transients)
- PMOS choppers demodulate the signal
- NMOS choppers modulate the NMOS current sources

[Sanduleanu]

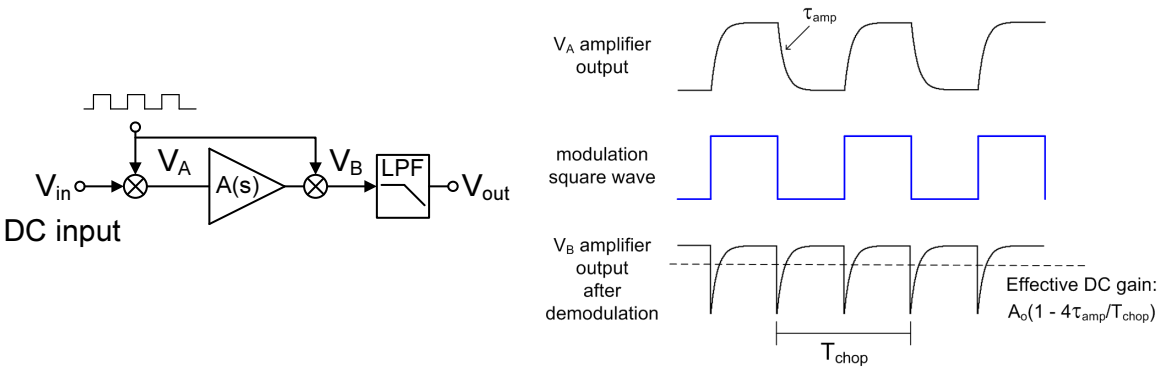
Residual Offset of Chopping





- Mismatched charge injection and clock feedthrough at the input chopper result in differential mode chopping artifacts [Enz, Temes]
  - Demodulation by the output chopper results in residual DC offset as well as chopping artifacts at even harmonics of f_{chop}
  - Residual offset = $2f_{chop}V_{spike}\tau_{spike}$
    - Can reduce by limiting the amplifier bandwidth → filters spikes
    - Causes a typical offset of 1-10μV
    - τ_{spike} depends on the source impedance (e.g. feedback resistors)

Amplifier Bandwidth



- Finite amplifier bandwidth reduces the effective DC gain
  - Effective gain = $A_0(1 - 4\tau_{amp}/T_{chop})$ [Makinwa]
  - Applying feedback compensates the gain error (slide 28)
  - Creates chopping artifacts at even harmonics of f_{chop}
- Phase response of the amplifier and phase between the two chopper signals also affect gain [Enz, Temes]

Design Considerations for Chopping

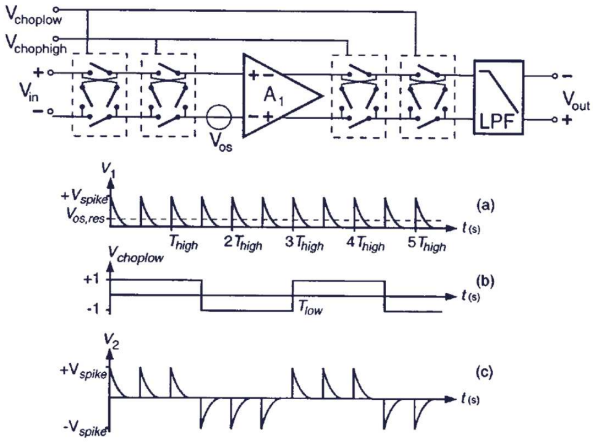
- The input chopper and associated nodes are key for minimizing residual offset
  - Minimum size switches for minimum charge injection
  - Highly symmetric layout to minimize differential mode charge injection and clock feedthrough
- Choice of f_{chop} is a tradeoff between chopper ripple and residual offset
  - Should be higher than 1/*f* corner
  - High frequency $f_{chop} \rightarrow$ need to make a fast amplifier
- Amplifier bandwidth is a tradeoff between gain error, spike filtering (residual offset), and even order chopping artifacts
  - Creating 'extra' bandwidth costs power
- Guarantee 50% chopping duty cycle with a flip flop

Advanced Techniques for Reducing Residual Offset and Ripple

- Residual offset is usually dominated by transient spike effects
  - Bandpass filtering the spikes reduces wideband spike energy
    - Fairly complicated implementation
  - Nested chopping: add an outer set of lower frequency choppers
  - Deadbanding the amplifier output during the spike transient

- AC ripple from modulated DC offset, finite amplifier BW, spikes
  - Filter the artifacts in analog or digital domains
    - Low cutoff frequency analog filters may be hard to realize on chip
  - Reduce the initial offset before it is modulated
    - Autozeroing, additional feedback, AC coupling
  - If the overall output is discrete time then filter the ripple and sample the output near the ripple‘s zero crossings

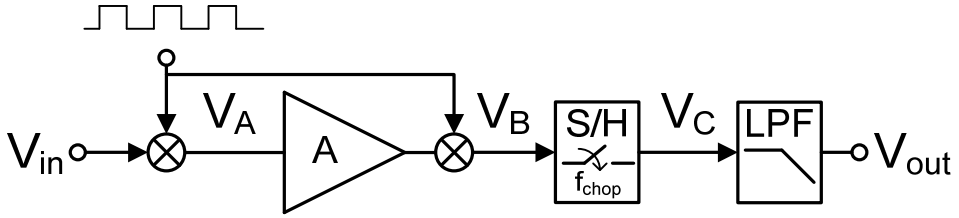
Reducing Residual Offset (1) Nested Chopping

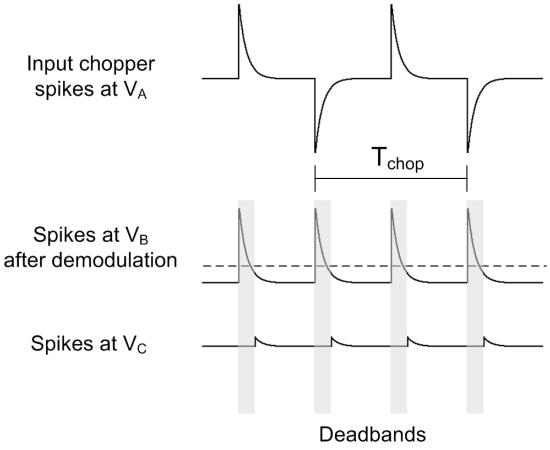


[Bakker]

- Inner choppers run at high frequency to remove 1/*f* noise
- Outer choppers modulate the inner spikes, remove DC content
  - Residual offset = $2f_{choplow}V_{spike}\tau$
- Can achieve ~100nV offset but bandwidth is limited ($f_{choplow}$)

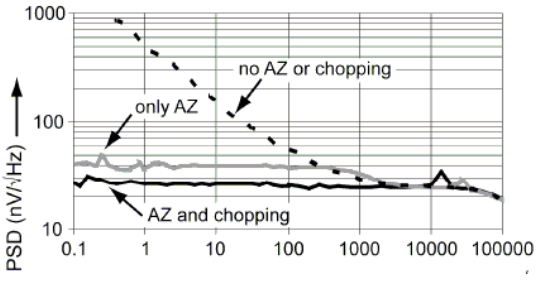
Reducing Residual Offset (2)
Dead-banding

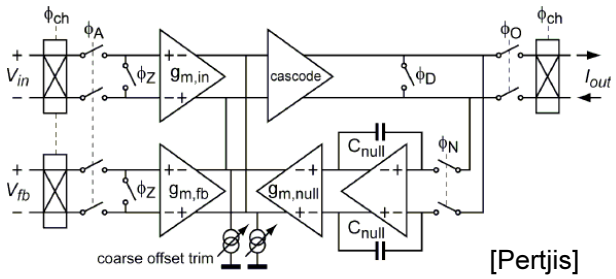




- Hold the output through the major portion of the spike transient
  - Reduces the DC component of the demodulated spikes
  - Some noise and gain degradation from S/H operation
- Can achieve ~200nV offset, don't have to sacrifice bandwidth [Menolfi]

Ripple Reduction (1)
Autozeroing and Chopping Together



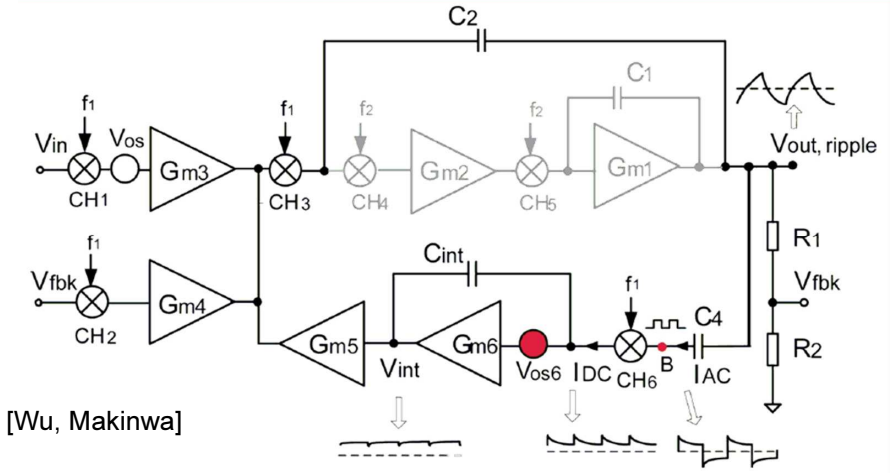


[Pertjis]

Figure 19.2.2: Circuit diagram of one of the input stages.

- Reduces chopper ripple by cancelling most of the offset before it is modulated
  - Low frequency noise penalty due to sampling
    - $f_{chop} = 2f_{az}$ mitigates aliased noise, averages residual offset
    - [Pertjis] avoids this by incompletely settling in the autozero phase
  - Need to use architectures like offset stabilization or ping-pong if the output must be continuously valid

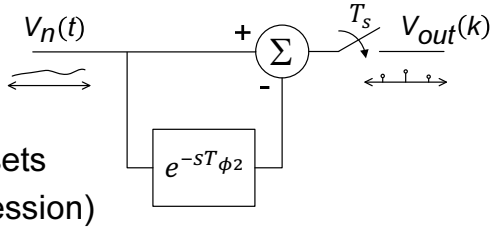
Ripple Reduction (2)
Additional Feedback



[Wu, Makinwa]

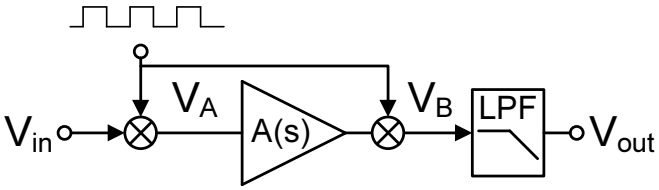
- Use an auxiliary feedback loop to sense the output ripple and null DC offset currents before they are chopped and filtered
  - Ripple can be suppressed below the amplifier's noise floor
  - Continuous time offset reduction → no noise aliasing

Precision Analog Summary



- Autozeroing and CDS
  - Can achieve 1-10μV residual offsets
  - Reduces 1/*f* noise (limited suppression)
  - Sampled data technique
    - Well suited to discrete time systems (data converters, SC filters)
    - Noise aliasing increases thermal noise floor
  - No loss of amplifier bandwidth with appropriate topology (offset stabilized, ping-pong)
  - Amplifier nonlinearity results in residual offset
  - Timing errors can generate noise (variable settling)

Precision Analog Summary



- Chopping
  - Can achieve 50nV-10μV residual offsets
  - Technique of choice when noise efficiency is most important
    - Eliminates 1/*f* noise of chopped devices
    - No sampling → no thermal noise penalty
  - Well suited to continuous time applications
    - The amplifier output is always valid/available
  - Amplifier nonlinearity results in residual offset
  - Some fundamental loss of amplifier bandwidth

References (1)

[1] C.C. Enz, and G.C. Temes, “Circuit techniques for reducing the effects of opamp imperfections: autozeroing, correlated double sampling and chopper stabilization,” Proc. IEEE, vol. 84, no. 11, p. 1584 -1614, Nov. 1996.

[2] K. Kundert, Simulating switched-capacitor filters with SpectreRF. The Designer’s Guide Community, 2005, http://www.designersguide.org/Analysis/sc-filters.pdf

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[6] J.H. Huising, “Dynamic Offset Cancellation in Operational Amplifiers and Instrumentation Amplifiers” Book Chapter, M. Steyaert et al. (eds.), Analog Circuit Design, Springer Science+Business Media B.V. 2009.

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[7] M. Sanduleanu et al., “A low noise, low residual offset, chopped amplifier for mixed level applications,” Proc. ICECS, Vol. 2, pp. 333-336, 1998.

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[10] A. Bakker, K. Thiele, and J.H. Huijsing, “A CMOS nested chopper instrumentation amplifier with 100nV offset,” JSSC, vol. 35, no. 12, p. 1877 -1883, Dec. 2000.

[11] C. Menolfi and Q.Huang, “A 200nV 6.5 nV/Hz noise PSD 5.6kHz chopper instrumentation amplifier,” Digest ISSCC, p. 362 - 363, Feb. 2000.

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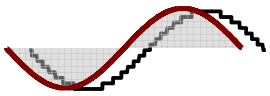
Sensor Interfaces

Partly adapted from Kofi Makinwa's EE315A guest lecture in Spring 2009
[http://ei.ewi.tudelft.nl/people/biography/projectleaders/makinwa_kofi.htm]



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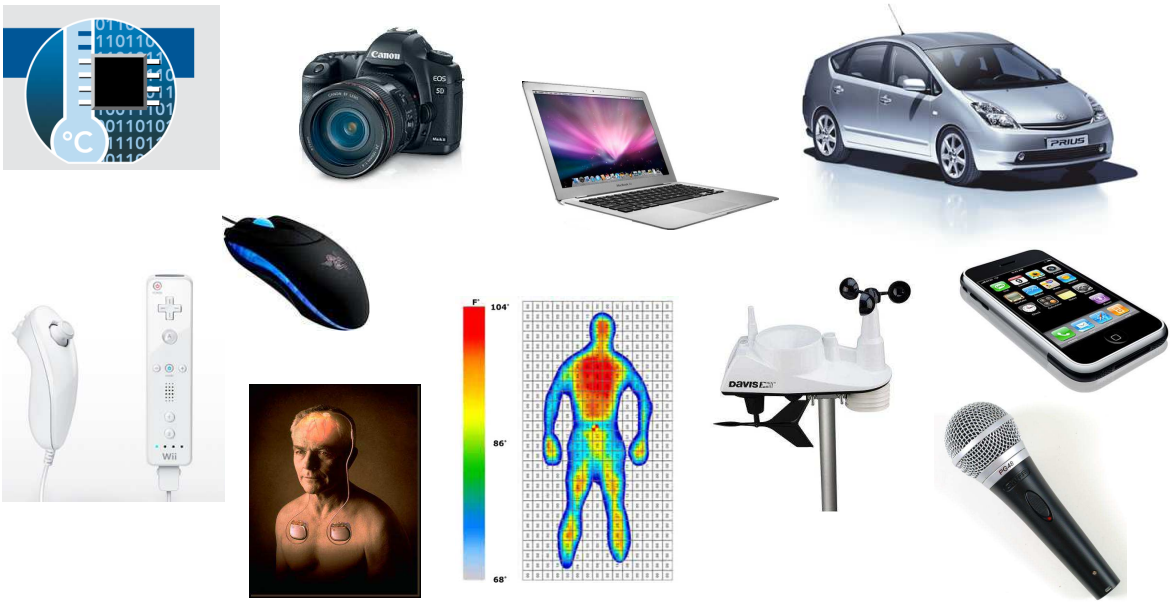
Outline – Part 1

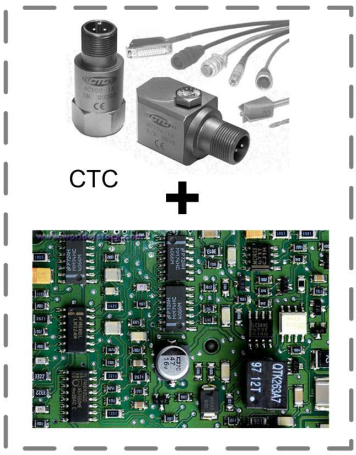
- Sensors
  - Trends
  - Types of sensors
- Sensor interfaces
  - High level description
  - Circuit techniques
- Sensor interface examples
  - Medtronic neural field potential measurement
  - Sony CMOS image sensor
  - CMOS temperature sensor
- Summary
- References

Sensors

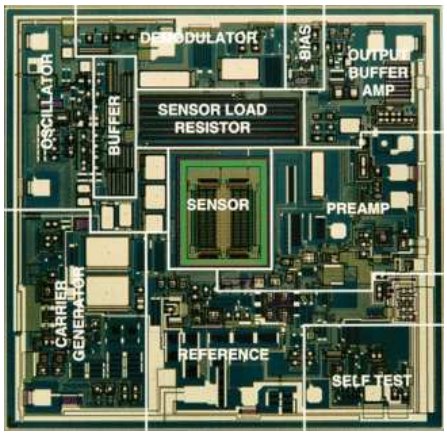
Sensors are in everything these days!



Evolution of Sensor Technology



Traditional Sensing System

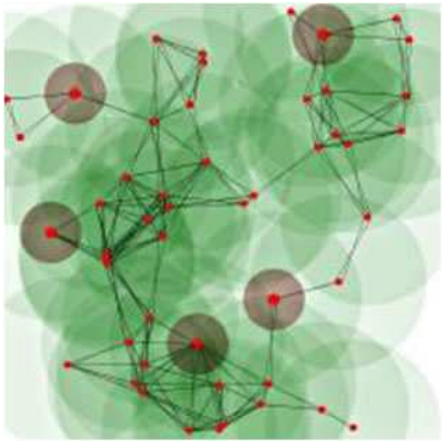


Analog Devices ADXL MEMS Accelerometer

- MEMS technology is fueling a movement toward more cost effective, highly integrated sensors
  - Sensor and interface electronics in one package
  - Precision is often reduced in integrated sensors

Ubiquitous/Distributed Sensing Trend

Berkeley Wireless Sensor Mote



MAIN lab

- Sensor networks
  - Building one 'macrosensor' out of many smaller sensors
    - Many sensor types in one platform, multiple modalities
    - Low power requirements for electronics, sleep/wake modes
    - Wireless interrogation (RFID)

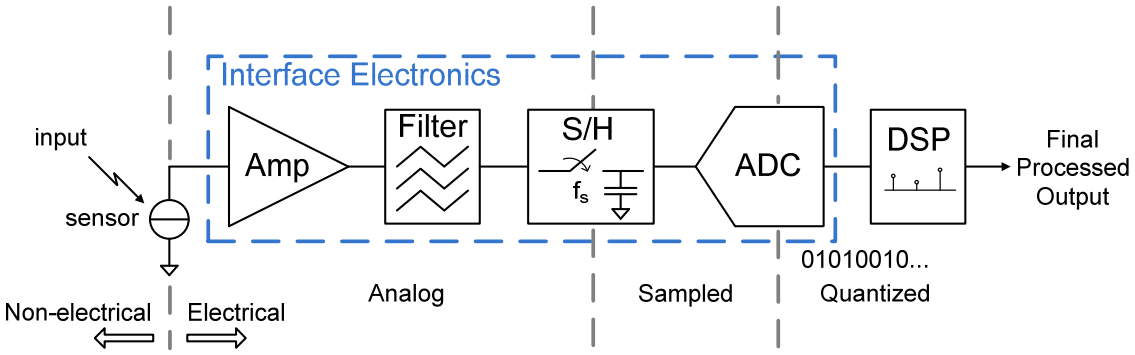
Types of Sensors (1)

- Sensors can be grouped by their input energy domain
  - Mechanical: inertial sensors, strain gauges, piezoelectric
  - Radiant: photodiodes, photocells
  - Thermal: thermopiles, bipolar transistors, thermoresistors
  - Chemical: ISFETs, thin films
  - Magnetic: Hall effect sensors, magnetotransistors, NMR, GMR
  - Electrical: electrodes
- Sensors can be grouped by the type of output
  - Voltage: thermopiles, piezoelectrics, NMR, electrodes
  - Current: photodiodes, Hall effect sensors, transistors
  - Resistance: strain gauges, photocells, GMR
  - Capacitance: inertial sensors, humidity sensors
  - Frequency: many MEMS sensors involve resonant mechanical structures, e.g. chemical sensors

Types of Sensors (2)

- Often differences between outputs are used as the ‘signal’
  - ‘light’ and ‘dark’ signals in image sensors
  - Temp differences between active sensor area and ambient
  - Capacitance differences in inertial sensors
- Overlap in sensor domains
  - May use temperature/heat flow to indirectly measure pressure (Pirani vacuum sensor)
  - Presence of chemical or biological quantities can cause mechanical changes in microstructures (e.g. resonance shifts)
- The designer chooses which domain to process information in
- The designer picks the best format for signal conditioning

Canonical Sensing System



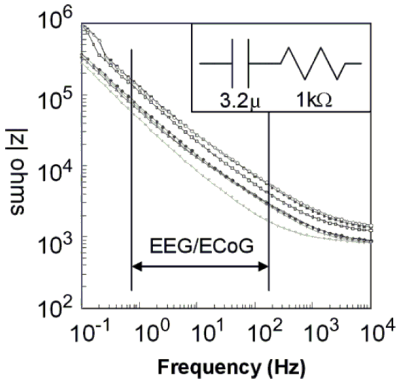
- Front-end amplification boosts the sensor’s signal above the noise floor of the interface electronics
- Filtering rejects interference, noise, provides antialiasing
- System level optimization is needed
  - Don’t want to waste power, money, area, accuracy, etc..

Sensor Attributes

- Typically low bandwidth, slow compared to FET switching speed
- Signal levels are usually small
  - Corrupted by noise, may be fighting for each dB of SNR
  - Can be mixed with undesired signals
- Sensors are sensitive to manufacturing variations, temperature, mechanical stress (e.g. from packaging)
- Environmental conditions may require operation at extremes of temp, humidity, pressure
- Dynamic compensation is often required to guarantee system specs over all required operating conditions

Sensor Electrical Modeling

Medtronic



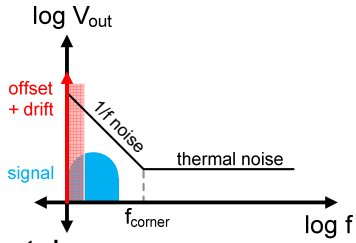
- An electrical model of the sensor is important for identifying an appropriate electronic interface
  - Usually model the sensor as a LTI system
    - Need to understand when this is valid and when it breaks down
    - May have memory or may be considered instantaneous
  - Can incorporate sensor input domain dynamics into the model

Sensor Interfaces

- Extract the desired features of the signal and convert them to a form that is easily processed
  - Includes special functions like biasing, tuning..
  - Processing usually occurs in the digital domain
    - Some analog processing may reduce overall system requirements
- The interface should not be a bottleneck
  - Typically want to perform near the sensor's intrinsic precision
  - In the words of Kofi: "Do no harm! Digitize early! Be dynamic!"
- System testing requires input stimulus in the sensor's domain
- Accuracy and resolution of the interface electronics are often referred back to the sensor input (e.g. +/-1° for an angle sensor)

Interface Circuit Techniques (1)

- Autozeroing, CDS, chopping
  - Reduce offset, drift, 1/f noise
  - Leverage the speed advantage of CMOS

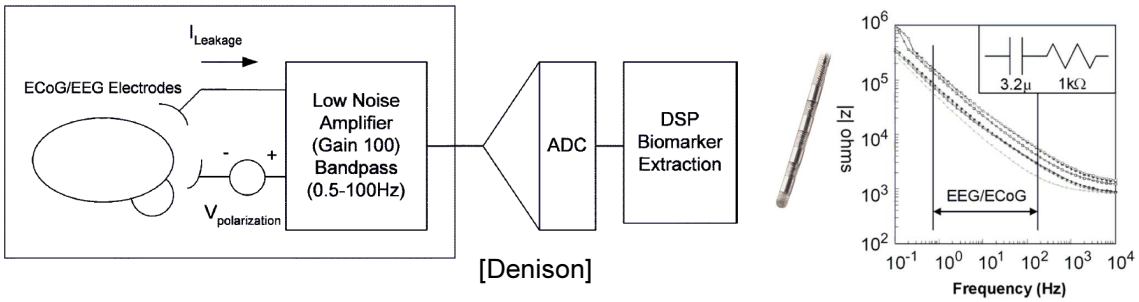


- Dynamic element matching (DEM)
  - Average out errors due to component mismatch
  - Can achieve accuracy beyond intrinsic device matching
- Modulating the sensor response to different frequencies
- Methods to improve SNR
  - Lock-in amplifiers
    - Isolate a narrowband signal from high noise levels
  - Signal auto-correlators and cross-correlators
  - Waveform averaging, integration

Interface Circuit Techniques (2)

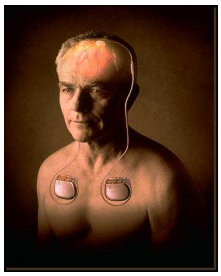
- Oversampling
  - Leverage the relatively high speed of CMOS transistors, trade bandwidth for higher resolution
  - Can achieve resolution beyond intrinsic matching of IC devices
  - Oversampling ADCs can have relaxed antialiasing requirements
- Feedback
  - Apply feedback to the sensor
    - Force feedback in inertial sensors
  - Use feedback in conditioning stages to set accurate gains and modify input/output impedances
- Replica tuning
- Post fabrication circuit trimming for static corrections

Sensor Interface Example #1
Medtronic Brain Sensing System



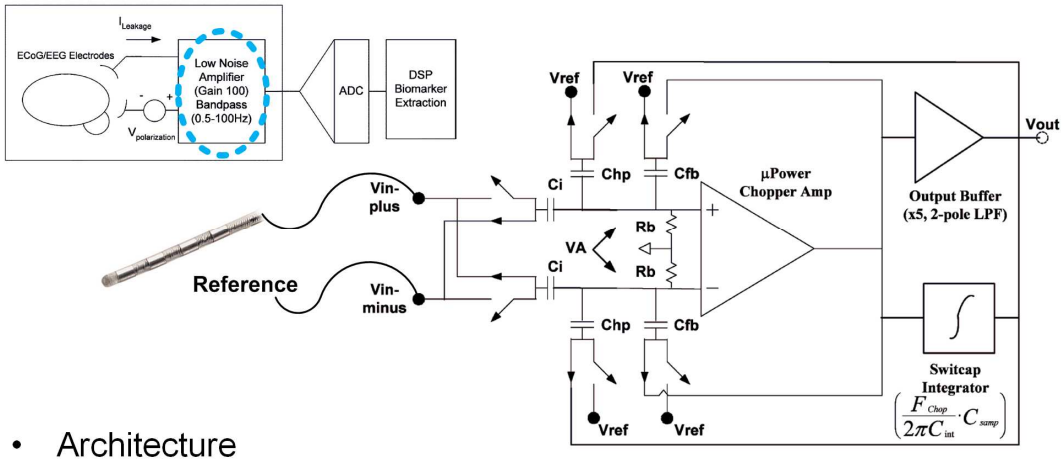
[Denison]

- Acquisition of neural field potential signals
  - Sensors are high impedance PtIr electrodes
  - 1-100Hz bandwidth, mV amplitudes
  - Signal is an average measure of brain activity
- Applications
  - Sense/stim deep brain stimulation systems
  - Brain machine interfaces for disabled individuals



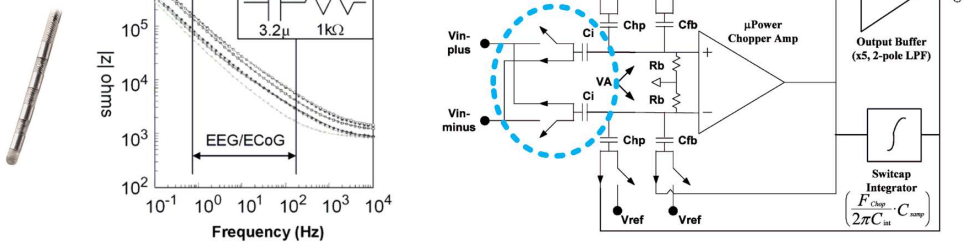
Medtronic

Front-end Amplification and Filtering



- Architecture
  - Multipath feedback chopper amplifier
  - 2nd order on-chip continuous time low pass filter output buffer
  - Switched capacitor feedback integrator for high pass filtering
- Noise/power efficiency optimization is a key requirement

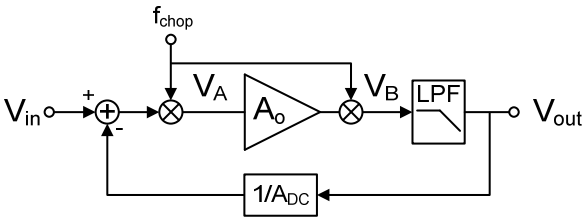
Switched Capacitor Input Impedance



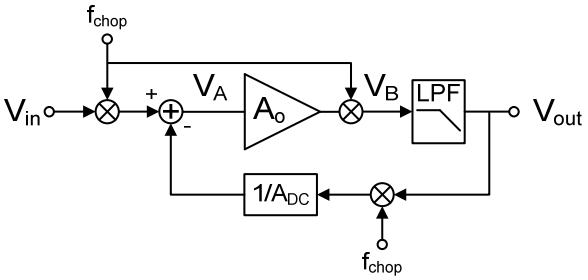
- Chopping the input caps results in a switched cap input impedance
  - Looks resistive at low frequencies
  - Need R_{in} large to avoid unwanted high pass filtering
    - Also need to minimize input current to avoid electrode corrosion
    - Constrains the choice of f_{chop}, C_{in}
- Unmodulated capacitive feedback suffers from a similar problem
  - The chopped input cap of the amp looks like a shunt resistance

Chopping with Modulated Feedback

Chopper Amp with Feedback

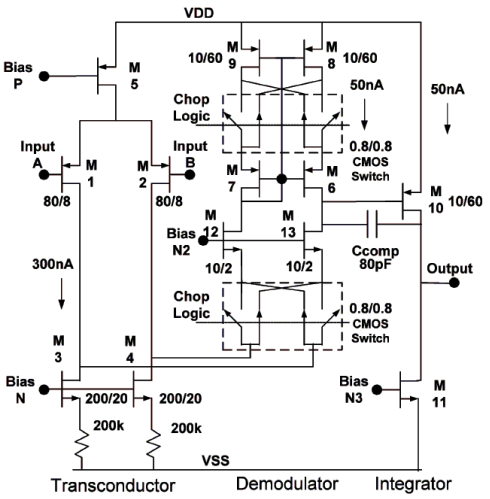


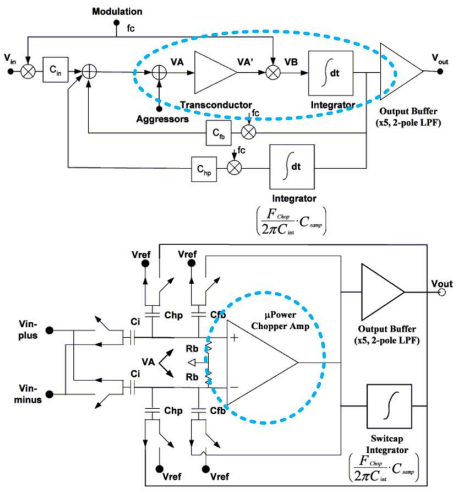
Chopper Amp with Modulated Feedback



- The input chopper is pushed through the summing node
  - The feedback path is modulated
  - Allows capacitive feedback instead of resistive for this design
    - Switched capacitor feedback is compatible with the impedances at the summing node
    - Easier to realize on-chip
    - Less distortion, noise, area, power than resistors

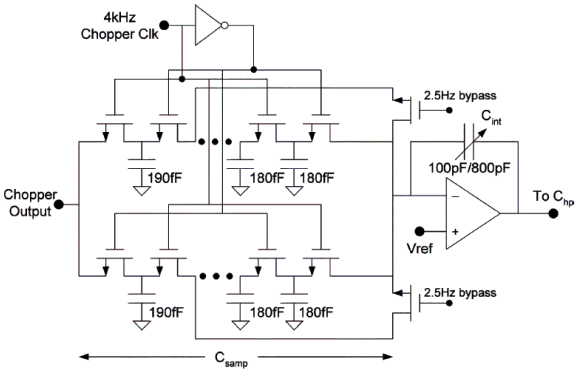
Chopped Transconductor

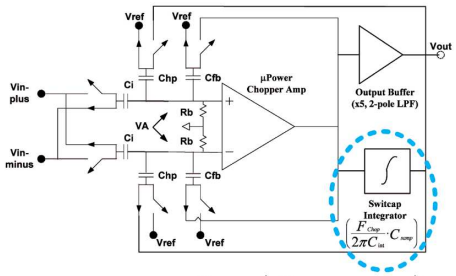




- Source degeneration attenuates noise from the nmos loads
- Input and folded branch currents are scaled for low noise
- Large compensation capacitor for noise and ripple reduction

Switched Capacitor Feedback Integrator

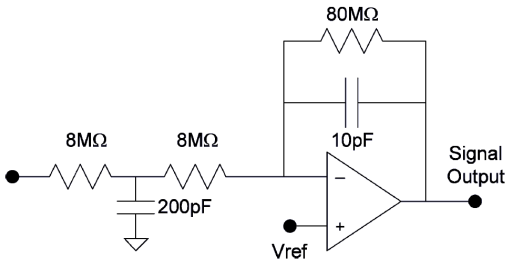


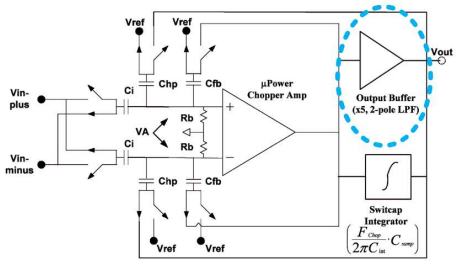


$$L(s) \approx \frac{C_{\mathrm{hp}}}{C_{\mathrm{fb}}} \cdot \left(\frac{F_{\mathrm{Chop}}}{2\pi C_{\mathrm{int}}} \cdot C_{\mathrm{samp}} \right)$$

- An integration in feedback results in a high pass corner (<0.1Hz !!)
  - Filters out DC polarization of the electrodes (up to 50mV max)
  - Unity gain frequency of this loop sets the corner frequency
- Bucket brigade of sampling caps for matching and programming
- Noise penalty from sampling is low here
  - In feedback, plus most of the sampled noise is low frequency

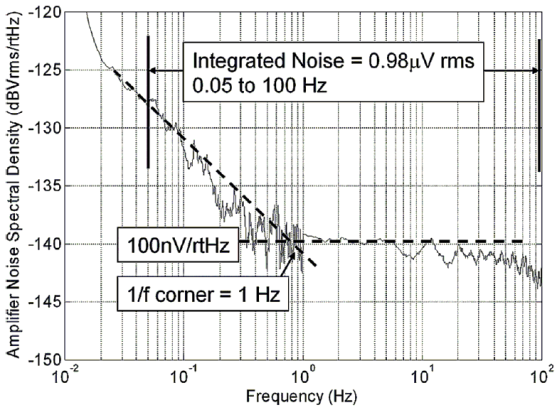
Output Buffer





- A continuous time filter is used to set the system's low pass corner frequency (180Hz) and to drive the ADC
  - Uses on-chip high resistance CrSi resistors (special process)
  - Suppresses chopper ripple
  - Partitioning of 5x gain here for system level optimization
    - Noise and DC rejection tradeoff, optimized with C_{hp} and C_{in}
  - Input resistor contributes significant noise at the system level

Noise Performance and Tradeoffs



Maximum HPF rejection

$$V_{\max} \triangleq \pm \frac{C_{\text{hp}}}{C_{\text{in}}} \bullet \frac{V_{\text{dd}}}{2}$$

Main amplifier noise

$$e_{\text{net,RTI}} = \left(\frac{C_{\text{in}} + C_{\text{hp}} + C_{\text{fb}} + C_{\text{amp}}}{C_{\text{in}}} \right) e_{n,\text{amp}}$$

Total noise PSD

$$e_n^2 = \left[\left(\frac{C_{\text{tot}}}{C_{\text{in}}} \right)^2 \left(\frac{4kT}{g_m} + \frac{4kTR_{\text{LPF}}}{\left(\frac{C_{\text{int}}}{C_{\text{fb}}} \right)^2} \right) + \frac{4kT}{R_{\text{eq}}} \cdot \left(\frac{1}{2\pi C_{\text{in}} F_{\text{chop}}} \right)^2 \right] \left[\frac{V^2}{Hz} \right]$$

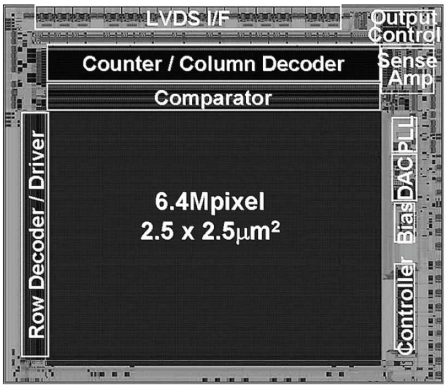
- Residual 1/*f* corner frequency from the unchopped output buffer
- Feedback scheme results in amplifier noise like a cap FB OTA
- Input biasing network and output buffer contribute excess noise

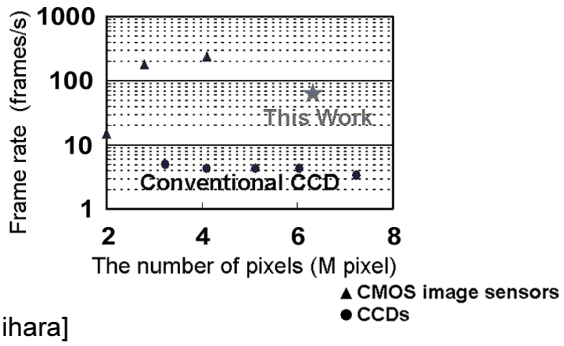
Measured Performance

TABLE II
KEY BIOPOTENTIAL AMPLIFIER RESULTS

Specification	Value	Units/Comments
Supply Voltage	1.8 to 3.3	Volts
Supply Current	1.0	uA
Gain	41, 50.5	dB (High polarization), (Diagnostic)
Noise	0.95	μV rms , 0.05 to 100Hz
CMRR	> 80 > 100	SE dB (DC to 60Hz) DE dB (DC to 100Hz)
Nonlinearity	< 0.1%	Harmonic Distortion (5 mV input)
Aliasing	< -50	dB (compared to baseband)
NEF	4.6 / 5.4	Diagnostic / Sense-Stim Modes
High-Pass Corners	0.05, 0.4, 2.5	Hz, digitally programmable No external components
Lowpass Corner	180	Hz (-6dB, 2-pole filter)

Sensor Interface Example #2
Sony CMOS Image Sensor (2006)

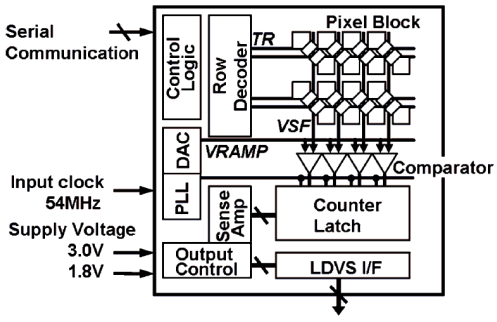


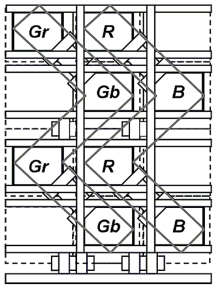


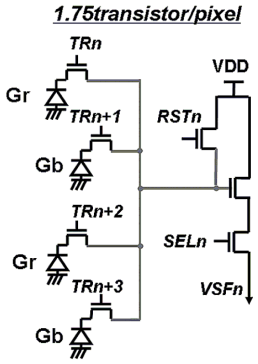
[Yoshihara]

- CMOS image sensor arrays with integrated interface electronics enable high performance digital imaging (6.4MPixel at 60fps)
  - Parallel readout of pixels is a key advantage over CCD
- Dual CDS scheme with column parallel architecture
  - First proposed by Sony 2006, dual CDS is now quite common

Sony Image Sensor Architecture

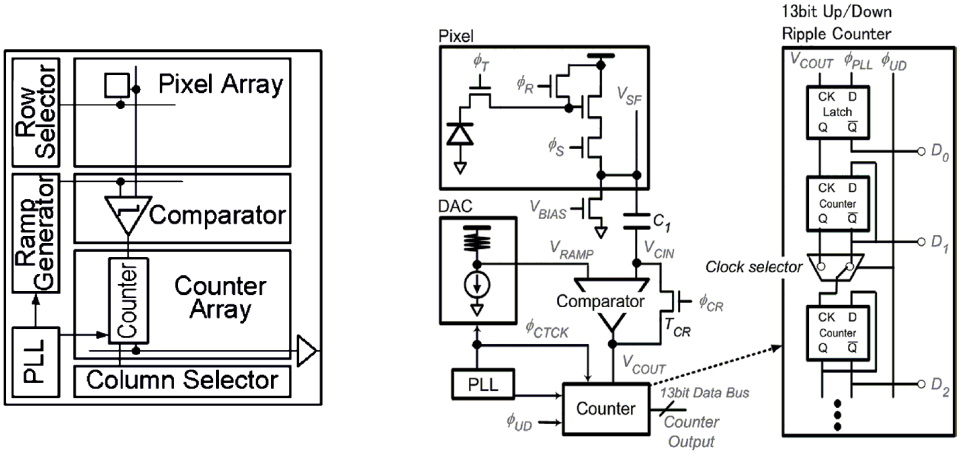






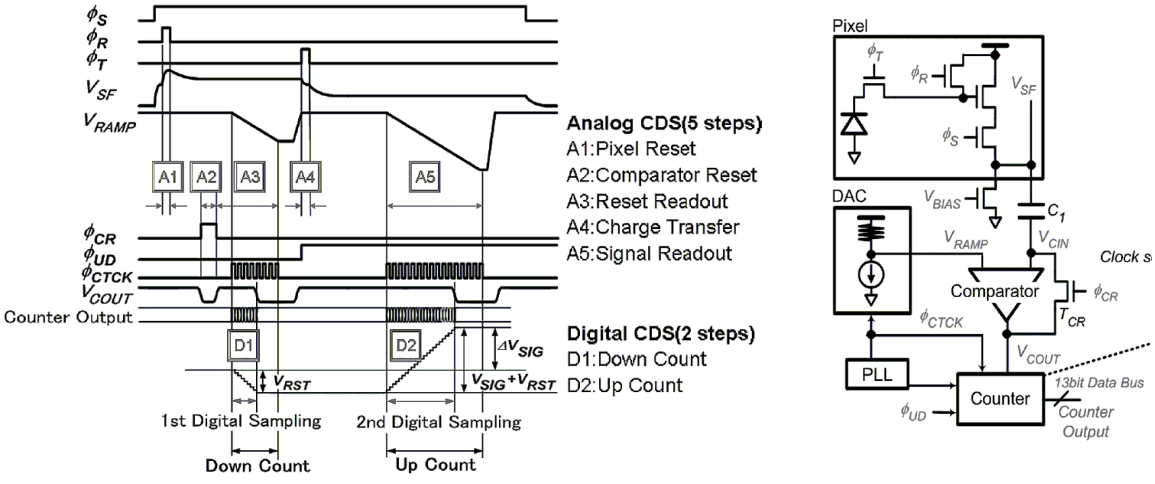
- Built around a high density array of photodiodes
  - On-chip microlenses focus light onto the active area
  - Primary color filters process the light before transduction
- Processing electronics are shared among the sensors
  - One set of source follower buffering for each 4 photodiodes
  - One bias current and one A/D converter per column of pixels

Column Parallel A/D Conversion



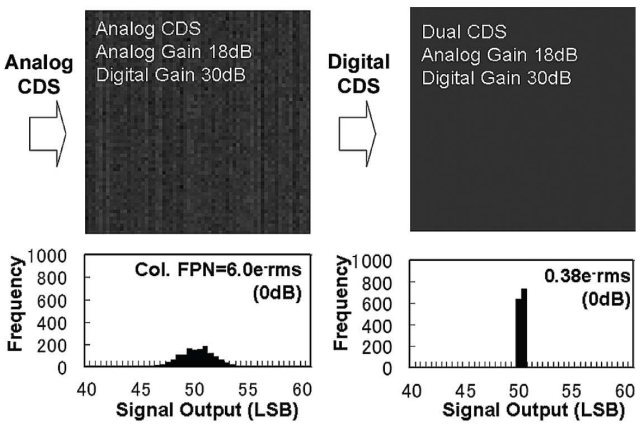
- The photodiode signals are accessed one row at a time with ϕ_S
- Columns within each row are converted in parallel
  - One single slope A/D converter for each column of pixels
  - Each of 4 shared photodiodes is accessed sequentially

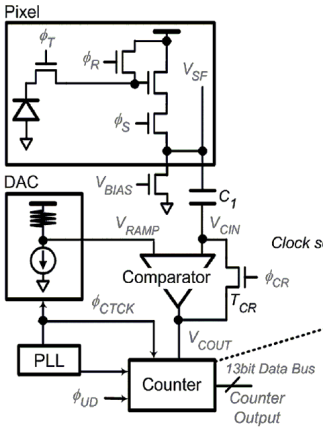
A Single Conversion Cycle



- Analog and digital CDS are both performed
- Single slope A/D conversion is performed by counting clock cycles before the comparator output flips

CDS Noise Reduction





- DC offsets and conversion errors result in fixed pattern noise (FPN)
- Analog CDS reduces offsets in the pixel and comparator, 1/*f* noise
- Digital CDS compensates for conversion errors resulting from clock skew, counter delay variation, comparator delay

Specs and Measured Performance

Specification

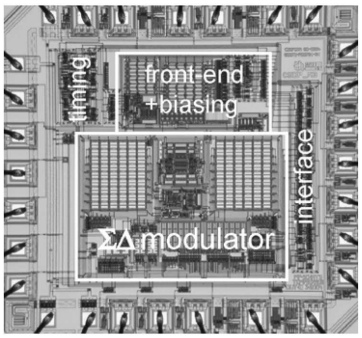
Item	Data
Process	0.18um 1P 3M
Pixel size	2.5um (H) X 2.5um (V)
Number of effective pixels	2928 (H) × 2184 (V)
Aperture ratio	38% without on-chip microlens
Supply voltage	3.0V / 1.8V
Input clock rate	54MHz
Max. Data rate	432MHz (216MHzDDR)
Output	12bit parallel LVDS
Mode	6.4Mpixel 60frames/s *1
	1.6Mpixel(2×2) 60frames/s *1
	1.2Mpixel (1/5 line readout) 300frames/s

*1 Seamless mode change

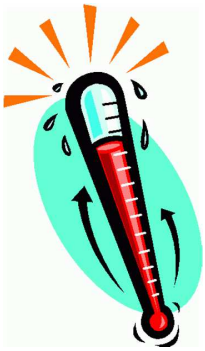
Characteristics

Item	Data
Quantum Efficiency	48% (at 550nm)
Sensitivity	14,000 electrons / lx*s At 3200K light source with IR cut filter of 650nm cut-off
Saturation signal	12,000e at 60C
Lag	Below measurement threshold
Dark current	15e/s at 60C
RMS Random Noise	7e rms At 60frames/s, Gain 0dB
RMS Vertical FPN	0.7e rms At 60frames/s, Gain 0dB
Dynamic range	64.7dB at 60frames/s
ADC resolution	10 bit at 6.4M 60frames/s 12bit at 6.4M 15frames/s
ADC INL	4LSB
ADC DNL	<0.5LSB
Conversion gain	40uV/e
Power consumption	360mW at 60frames/s

Sensor Interface Example #3
CMOS Temperature Sensor

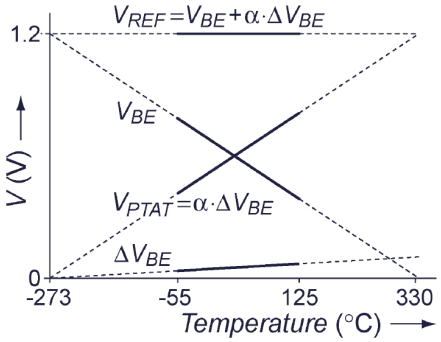


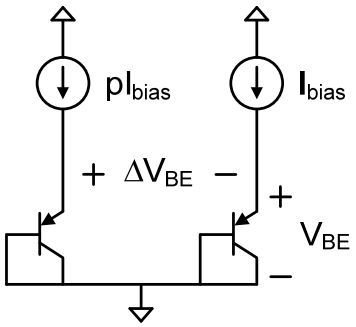
[Pertijs]



- High accuracy CMOS temperature sensor (2005)
  - 3σ inaccuracy of +/-0.1°C over -55°C to 125°C
  - Outperforms commercial offerings of CMOS temp sensors
- Based on substrate PNP band gap reference
- 'One shot' operation, the sensor is queried then goes back to sleep

Bandgap Reference Principle

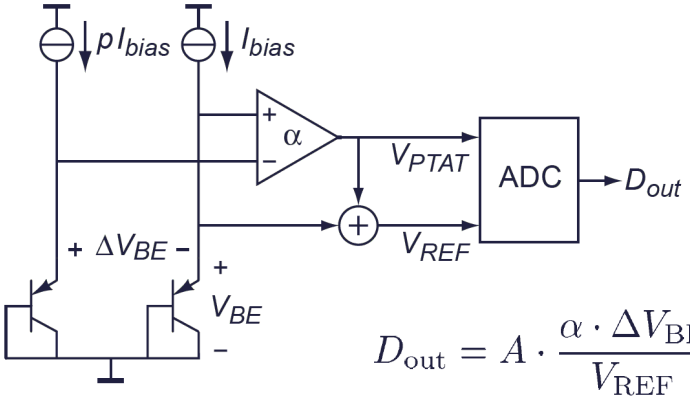




$$V_{\mathrm{BE}}(T) = \frac{kT}{q}\ln\left(\frac{I_{\mathrm{bias}}(T)}{I_S(T)}\right) \qquad \Delta V_{\mathrm{BE}}(T) = \frac{kT}{q}\ln(p)$$

- To 1st order V_{BE} and ΔV_{BE} are linearly related to temperature
  - V_{BE} is complementary to absolute temperature (CTAT)
  - ΔV_{BE} is proportional to absolute temperature (PTAT)
- $V_{BE} + \alpha\Delta V_{BE}$ is temperature independent given the right α

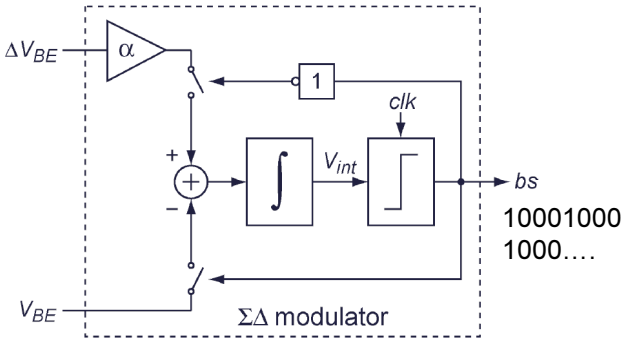
Temperature Sensor Principle



$$D_{\text{out}} = A \cdot \frac{\alpha \cdot \Delta V_{\text{BE}}}{V_{\text{REF}}} - B$$

- An ADC converts the V_{BE} and ΔV_{BE} information to digital format
- Compares PTAT ΔV_{BE} to temp independent $V_{REF} = V_{BE} + \alpha\Delta V_{BE}$
  - The resulting D_{out} is a digital thermometer

Sigma Delta Modulator

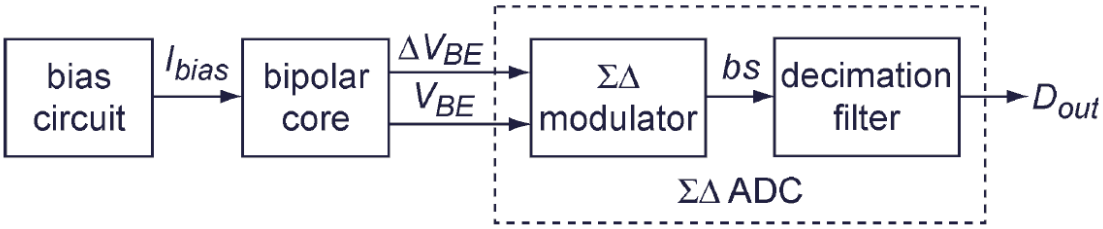


$$(1-\mu)\cdot\alpha\cdot\Delta V_{\text{BE}} = \mu\cdot V_{\text{BE}}$$

$$\mu = \frac{\alpha\cdot\Delta V_{\text{BE}}}{V_{\text{BE}}+\alpha\cdot\Delta V_{\text{BE}}} = \frac{\alpha\cdot\Delta V_{\text{BE}}}{V_{\text{REF}}}$$

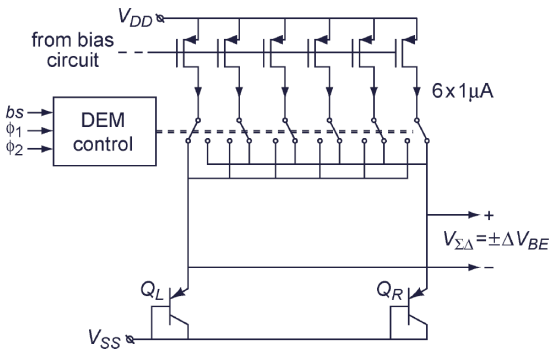
- A sigma delta modulator is used to compute the ratio (EE315B)
  - A clocked comparator selects whether to integrate $-V_{BE}$ or ΔV_{BE} in each clock cycle
  - Negative feedback drives the integrator output toward zero
- The average value 'μ' of the output bit stream is the desired ratio

Temp Sensor Block Diagram



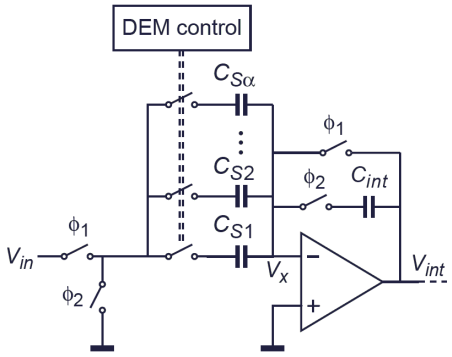
- An off-chip digital filter processes the bit stream to produce D_{out}
- Circuit errors are reduced to very low levels to achieve the full accuracy of the temperature sensor system
  - Their strategy is to reduce all circuit errors to 0.01°C level
    - Offset in ΔV_{BE} readout
    - Mismatch in 1:p current ratio and error in α factor
    - Offset in the sigma delta modulator
- A single temperature trim corrects for process spread of V_{BE}

DEM Current Source Rotation



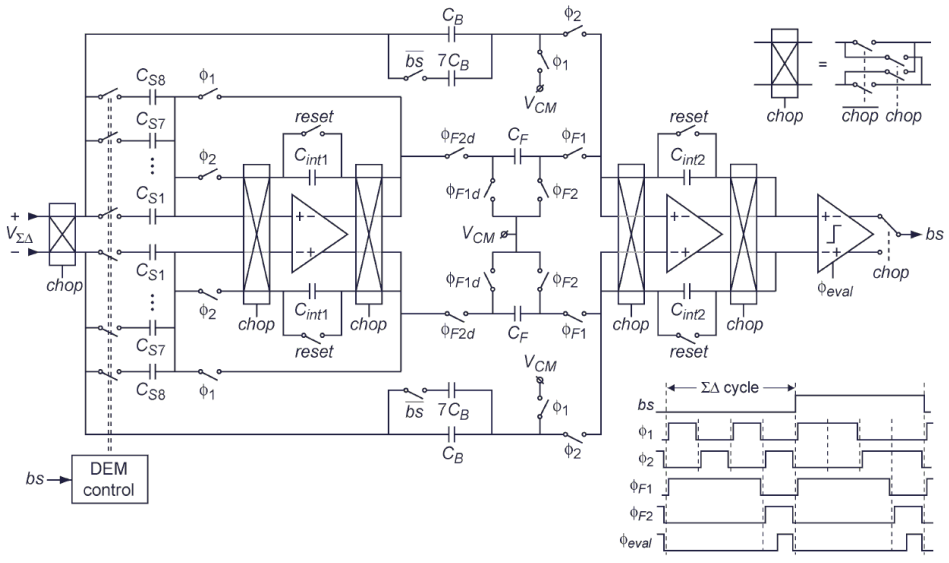
- Dynamic element matching is used to create accurate 1:p ratio
  - Need <0.011% error in the ratio for 0.01°C sensor referred error
  - Current sources are rotated each sample period, the sigma delta integrator averages out the error
- The $p \cdot I_{bias}$ and I_{bias} sources are also swapped between Q_L and Q_R to average out Q_L/Q_R offset from the ΔV_{BE} measurement

Sigma Delta Integrator



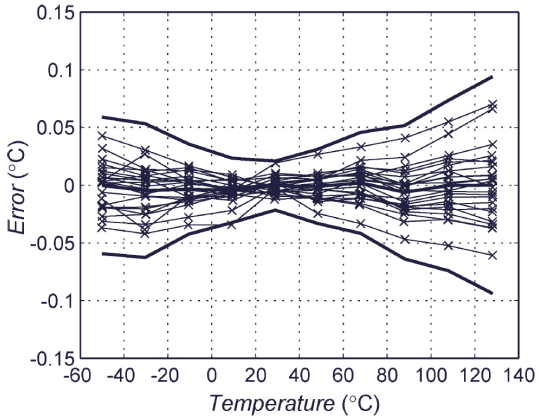
- Switched capacitor integrator used in the sigma delta loop
- DEM is used to create an accurate α gain factor for $\alpha \cdot \Delta V_{BE}$
  - Sampling capacitors are rotated each sample period
- Autozeroing during the sampling period ϕ_1 is used to cancel the offset of the integrator and reduce 1/*f* noise

Full Sigma Delta Architecture



- System level chopping reduces the total offset below 0.01°C

Final Measured Error of 24 Samples



- Several other techniques are needed to get the final performance
  - β insensitive I_{bias} generation
  - Curvature correct of the V_{BE} temperature response
    - Slightly PTAT V_{REF} reference voltage, nonlinear decimation filter
  - V_{BE} averaging between Q_L and Q_R

Summary

- Sensors and sensor interfaces are huge areas
  - Hard to be comprehensive (see [6])
- The trend is cheaper, highly integrated sensors and electronics
  - Sensor performance is degraded somewhat
    - Need to preserve sensor accuracy in the interface design
- Sensor interface examples show common techniques
  - Chopping, CDS, DEM, sensor modeling
- Important ideas not covered by the examples
  - Modulating the sensor
  - Feedback to the sensor
    - See example in part II of this chapter, slide 63

References

[1] Denison, T.; Consoer, K.; Santa, W.; Avestruz, A.-T.; Cooley, J.; Kelly, A.; , "A 2 μW 100 nV/rtHz Chopper-Stabilized Instrumentation Amplifier for Chronic Measurement of Neural Field Potentials," *Solid-State Circuits, IEEE Journal of* , vol.42, no.12, pp.2934-2945, Dec. 2007

[2] Yoshihara, S.; Nitta, Y.; Kikuchi, M.; Koseki, K.; Ito, Y.; Inada, Y.; Kuramochi, S.; Wakabayashi, H.; Okano, M.; Kuriyama, H.; Inutsuka, J.; Tajima, A.; Nakajima, T.; Kudoh, Y.; Koga, F.; Kasagi, Y.; Watanabe, S.; Nomoto, T.; , "A 1/1.8-inch 6.4 MPixel 60 frames/s CMOS Image Sensor With Seamless Mode Change," *Solid-State Circuits, IEEE Journal of* , vol.41, no.12, pp.2998-3006, Dec. 2006

[3] Yoshihara, S.; Kikuchi, M.; Ito, Y.; Inada, Y.; Kuramochi, S.; Wakabayashi, H.; Okano, M.; Koseki, K.; Kuriyama, H.; Inutsuka, J.; Tajima, A.; Nakajima, T.; Kudoh, Y.; Koga, F.; Kasagi, Y.; Watanabe, S.; Nomoto, T.; , "A 1/1.8-inch 6.4MPixel 60 frames/s CMOS Image Sensor with Seamless Mode Change," *Solid-State Circuits Conference, 2006. ISSCC 2006. Digest of Technical Papers. IEEE International* , vol., no., pp.1984-1993, 6-9 Feb. 2006

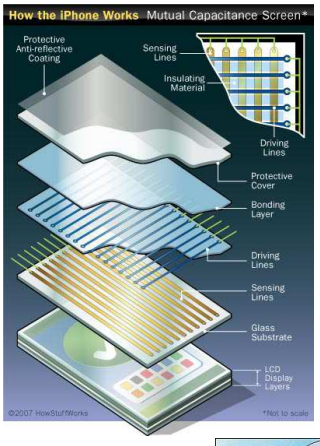
[4] Pertijs, M.A.P.; Makinwa, K.A.A.; Huijsing, J.H.; , "A CMOS smart temperature sensor with a 3σ inaccuracy of ±0.1°C from -55°C to 125°C," *Solid-State Circuits, IEEE Journal of* , vol.40, no.12, pp. 2805- 2815, Dec. 2005

[5] Pertijs, M.A.P.; Huijsing, J.H.; , "Precision interface electronics for a CMOS smart temperature sensor," *Sensors, 2005 IEEE* , vol., no., pp.4 pp., Oct. 30 2005-Nov. 3 2005

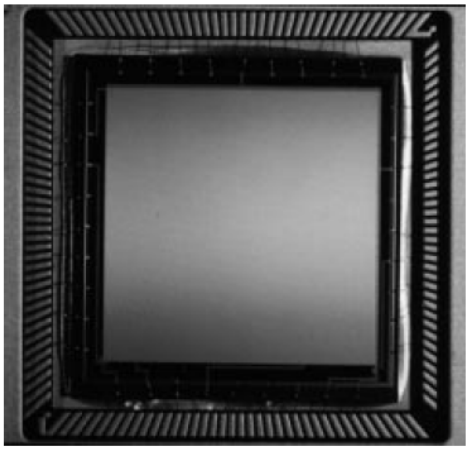
[6] C. Falconi, E. Martinelli, C. Di Natale, A. D'Amico, F. Maloberti, P. Malcovati, A. Baschirotto, V. Stornelli, G. Ferri: "Electronic Interfaces"; Sensors and Actuators, B, Vol. 121, 2007, pp. 295-329.

Part II – Capacitive Sensing

- Touchpad sensors
- Fingerprint sensors
- Flow rate measurement
- Biosensors
- Inertial sensors
  - Accelerometers
  - Gyroscopes
- …



Fingerprint Sensor (1)



[Tartagni, JSSC 1/1998]

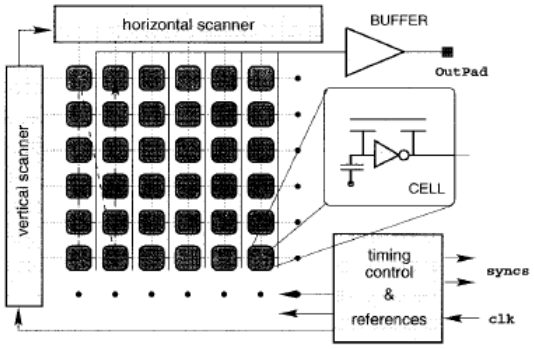
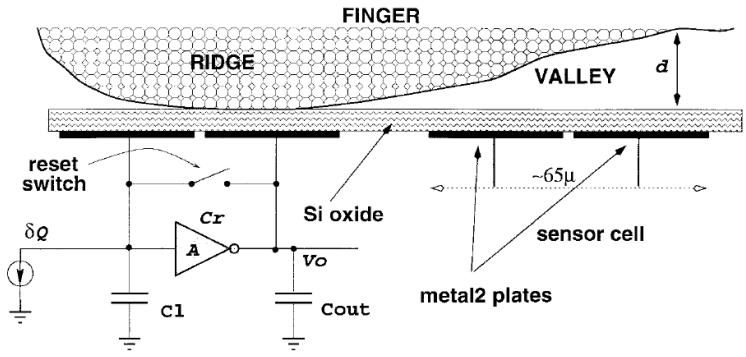


TABLE I
CHARACTERISTICS OF THE SENSOR

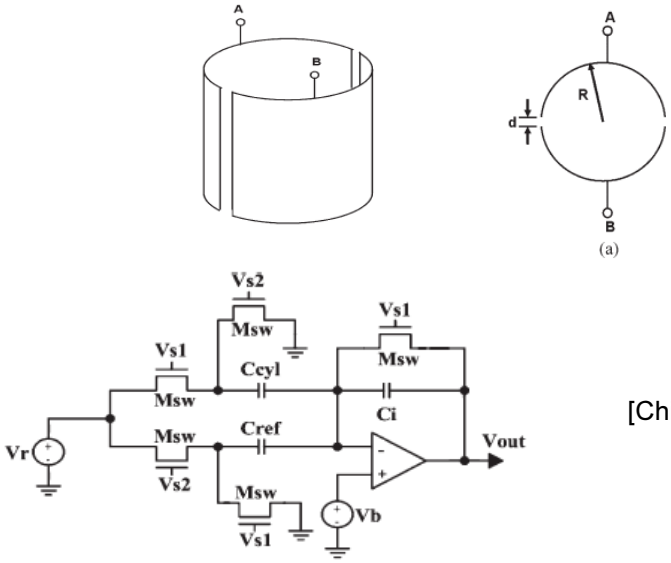
technology	2-metal $0.7\mu m$ digital cmos
die size	$15 \times 15mm^2$
array size	200×200
pixel pitch	$65\mu m$
frame rate	~ 10 F/s
energy consumption	$\sim 250\mu J$/acquisition

Fingerprint Sensors (2)



[Tartagni, JSSC 1/1998]

Flow Rate Measurement



[Chiang, JSSC 12/2006]

Capacitive DNA Detection (1)

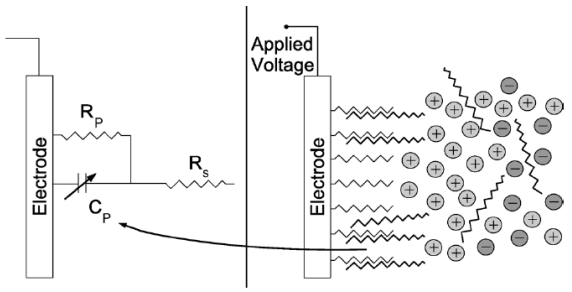
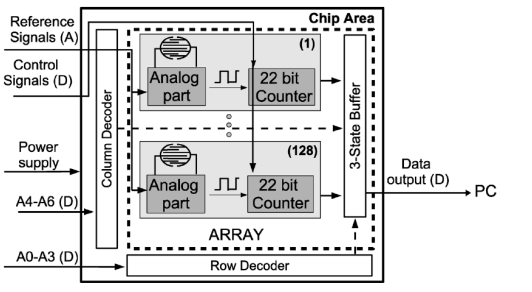
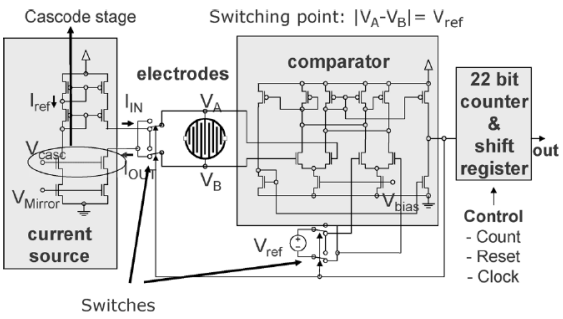


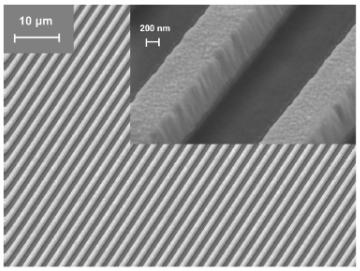
Fig. 1. Left: electrical metal/solution interface model. Right: DNA hybridization process and displacement of counterions.

[Stagni, JSSC 12/2006]





Capacitive DNA Detection (2)



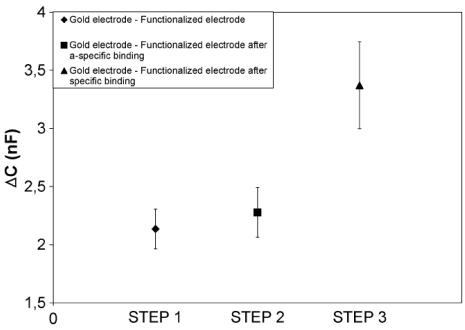


Fig. 15. The average behavior of all the pixels confirms that nonspecific and specific binding are distinguishable.

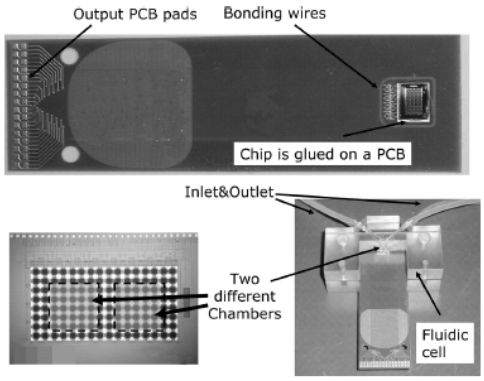
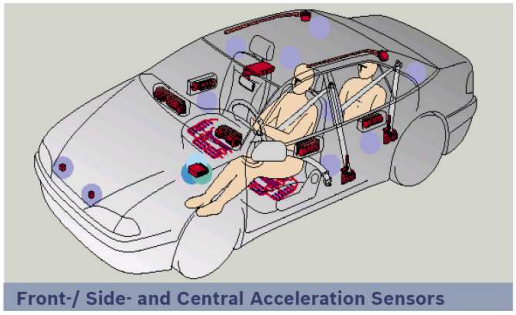


Fig. 8. Photo of the PCB used to contact pads with the glued chip, bonding wires (top) and the applied fluidic cell (bottom right). The cell determines two separated areas on the chip (bottom left) which can be functionalized with different probes.

[Stagni, JSSC 12/2006]

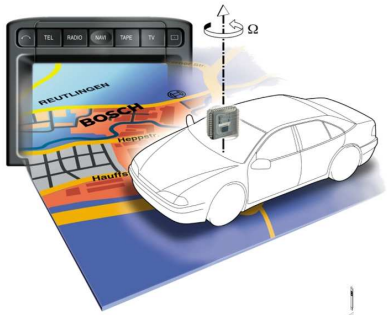
Automotive Inertial Sensor Applications

Accelerometers for Airbags

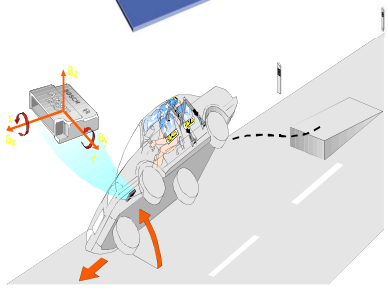


http://www.semiconductors.bosch.de/pdf/SMB120_170_Product_Info.pdf

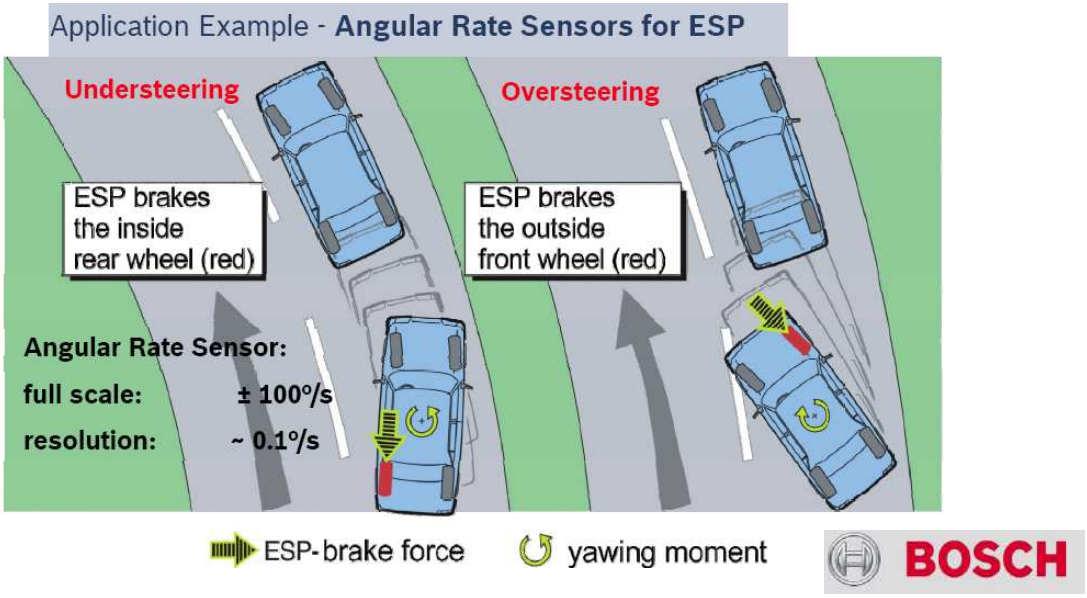
Accelerometers and Gyroscopes for Navigation



Gyroscope for Rollover Detection



Electronic Stability Program (ESP)



Consumer-Grade Accelerometer

BMA145
Analog, triaxal acceleration sensor

Bosch Sensortec

BOSCH
Invented for life

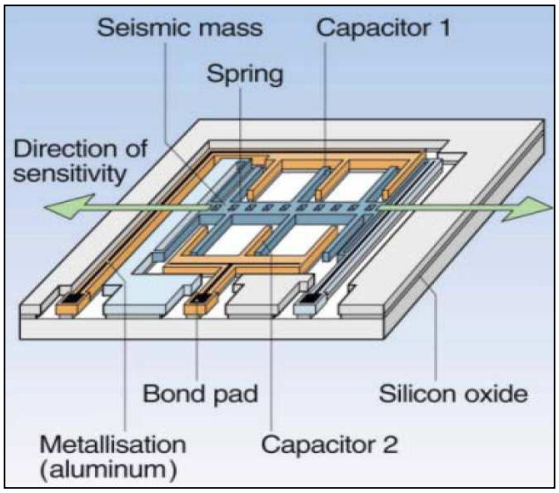
Leveraging its ultra-low power consumption and its wake-up feature the BMA145 senses tilt, motion, shock and vibration in advanced gaming console applications and all kind of mobile, personal communication and entertainment devices.

BMA145 applications based on low-g sensing

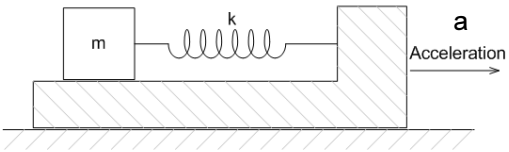
- Gaming
- Virtual reality
- Sports- and life-style wear
- Handhelds
- Healthcare
- Cell phones
- Navigation
- Electronic compass compensation

Technical data	BMA145
Sensitive axes	x/y/z
Measurement range	±4g
Package	LGA, 4 mm x 4 mm x 0.9 mm
Sensitivity (factory trimmed) Non-linearity	V_{DD}/10 [V/g]
	±0.5 % FS (typ.)
Cross axis sensitivity	0.2 % (typ.)
Zero-g offset (factory trimmed)	±150 mg (max.)
Zero-g offset temperature drift	±1 mg/K (typ.)
RMS-noise	220 µg/√Hz
Bandwidth (1st order LP filtering)	1.5 kHz
Supply voltage	1.8 ... 3.5 V
Current consumption	200 µA (typ., normal mode)
Idle current	0.9 µA (max.,stand-by mode)
Wake-up time	1 msec (typ.)
Temperature range	-40 °C ... +85 °C

A Closer Look at Accelerometers



http://www.semiconductors.bosch.de/pdf/SMB120_170_Product_Info.pdf



$$F = m \cdot a$$

$$x = \frac{F}{k}$$

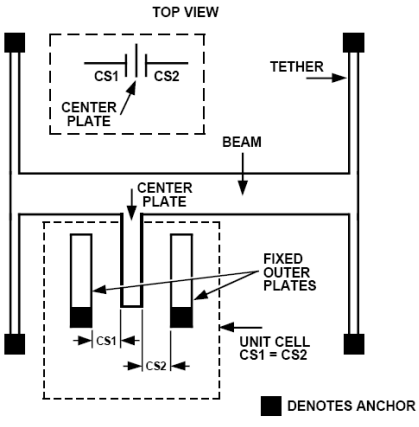
$$\frac{x}{a} = \frac{m}{k}$$

mass

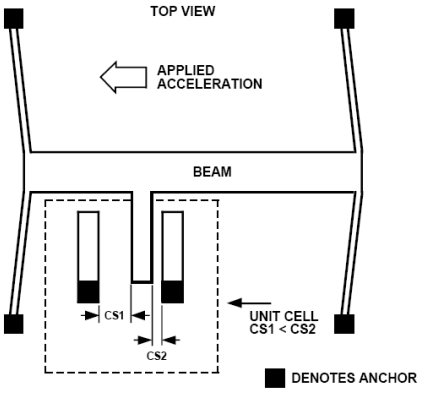
spring constant

Displacement → Capacitance Change

Structure at Rest

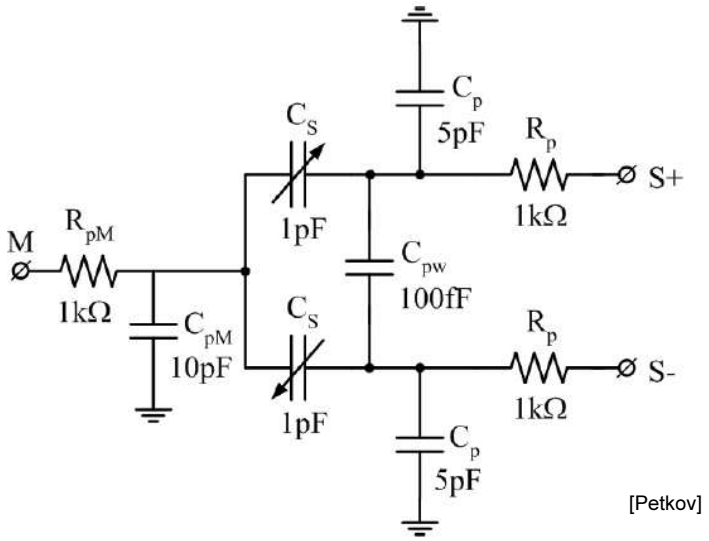


With Applied Acceleration



[ADXL50 datasheet]

Model of a Typical Sensor Element

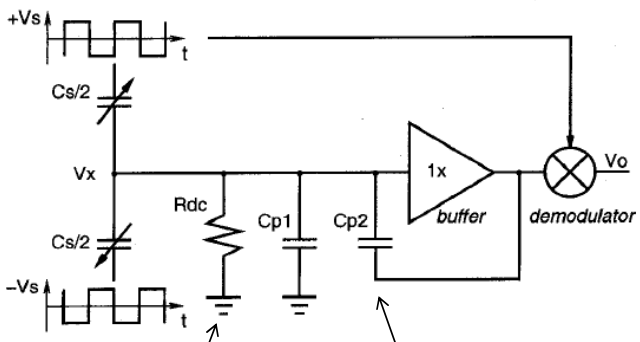


[Petkov]

High-Impedance Readout Circuit

[Boser & Howe, JSSC 3/1996]

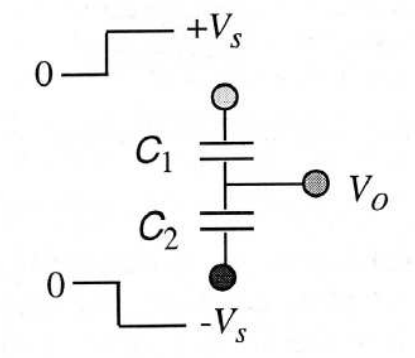
- Use chopper stabilization to mitigate offset and 1/f noise issues
- C_P is often comparable to sense capacitance
  - Introduces undesired attenuation



Need several MΩ

Bootstrapping of parasitic capacitance (shield)

Sense Voltage



$$C_1 = C\frac{x_0}{x_0 + \delta x} \qquad C_2 = C\frac{x_0}{x_0 - \delta x}$$

For small displacement:

$$C_1 - C_2 = C\left(\frac{x_0}{x_0 + \delta x} - \frac{x_0}{x_0 - \delta x}\right)$$

$$= C\frac{-2x_0\delta x}{x_0^2 - \delta x^2} \approx -C\frac{2}{x_0}\delta x$$

$$C_1 + C_2 \approx 2C$$

$$V_0 = -V_S + \frac{C_1}{C_1 + C_2}\cdot 2V_S$$

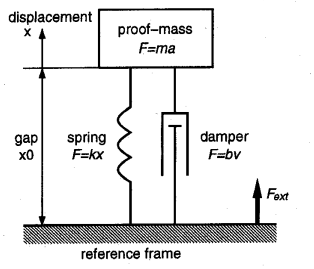
$$= \frac{C_1 - C_2}{C_1 + C_2}V_S$$

$$\boxed{V_0 \approx -\frac{\delta x}{x_0}V_S}$$

Output voltage is linearly proportional to the displacement

http://www.ee.ucla.edu/~wu/ee250b/Case%20study-Capacitive%20Accelerometer.pdf

How Much Signal Can We Get?



[Boser & Howe, JSSC 3/1996]

$$m\frac{d^2x}{dt^2} + b\frac{dx}{dt} + kx = F_{\text{ext}} = ma.$$

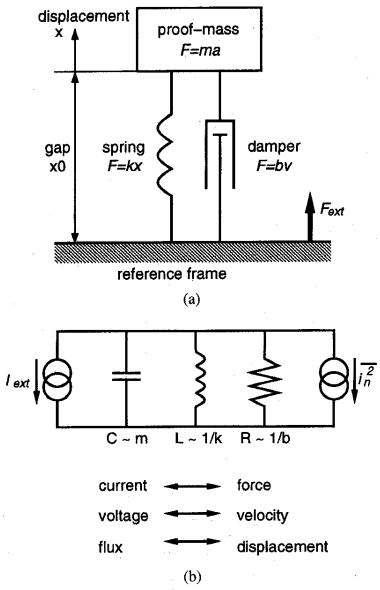
$$\frac{X(s)}{A(s)} = \frac{1}{s^2 + s\frac{\omega_r}{Q} + \omega_r^2}$$

$$\omega_r = \sqrt{k/m}$$

$$Q = \omega_r m/b$$

- At low frequencies $\frac{x}{a} = \frac{m}{k} = \frac{1}{\omega_r^2}$
- Want low ω_r
  - But this limits the usable bandwidth
    - Unless special “tricks” (like feedback) are used
- Let’s assume $\omega_r = 2\pi\cdot 5$kHz and a=1mg
  - Displacement will be only ~10pm (~x_0/100,000 for x_0=1μm)
  - Assuming C=1pF and x_0=1μm, capacitance change is only 10aF
  - Assuming V_s=2.5V, and 2x attenuation output voltage is 2.5V/100,000/2 = 12.5μV

Noise (1)



[Boser & Howe, JSSC 3/1996]

- Damping "b" introduces noise
  - Due to Brownian motion of air molecules

$$\sqrt{\frac{\overline{a_n^2}}{\Delta f}} = \frac{\sqrt{4k_BTb}}{m} = \sqrt{\frac{4k_BT\omega_r}{mQ}}$$

- For $\omega_r = 2\pi \cdot 5\text{kHz}$, m=0.25μg and Q=0.5, we have

$$\sqrt{\frac{\overline{a^2}}{\Delta f}} \cong 200\frac{\mu g}{\sqrt{Hz}}$$

$$\sqrt{\frac{\overline{v_x^2}}{\Delta f}} \cong 200\frac{\mu g}{\sqrt{Hz}} \cdot 12.5\frac{\mu V}{mg} = 2.5\frac{\mu V}{\sqrt{Hz}}$$

Noise (2)

- For vacuum packaged devices much higher Q can be achieved
- Suppose $\omega_r = 2\pi \cdot 5\text{kHz}$, m=0.25μg and Q=50,000; we then have

$$\sqrt{\frac{\overline{a^2}}{\Delta f}} \cong 1\frac{\mu g}{\sqrt{Hz}} \qquad \sqrt{\frac{\overline{v_x^2}}{\Delta f}} \cong 1\frac{\mu g}{\sqrt{Hz}} \cdot 12.5\frac{\mu V}{mg} = 12.5\frac{nV}{\sqrt{Hz}}$$

- MOS thermal noise

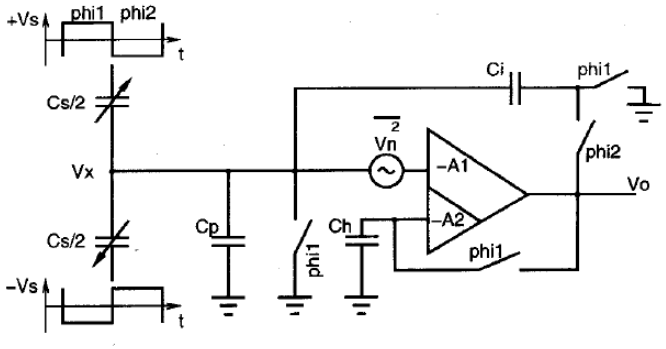
$$\frac{\overline{v_n^2}}{\Delta f} = 4kT\gamma\frac{1}{g_m}$$

- Assuming γ=1, equal noise from sensor and amplifier and no other noise source

$$g_m = \frac{4kT}{\left(12.5\frac{nV}{\sqrt{Hz}}\right)^2} \cong 100\mu S$$

Readout Circuit Variants (1)

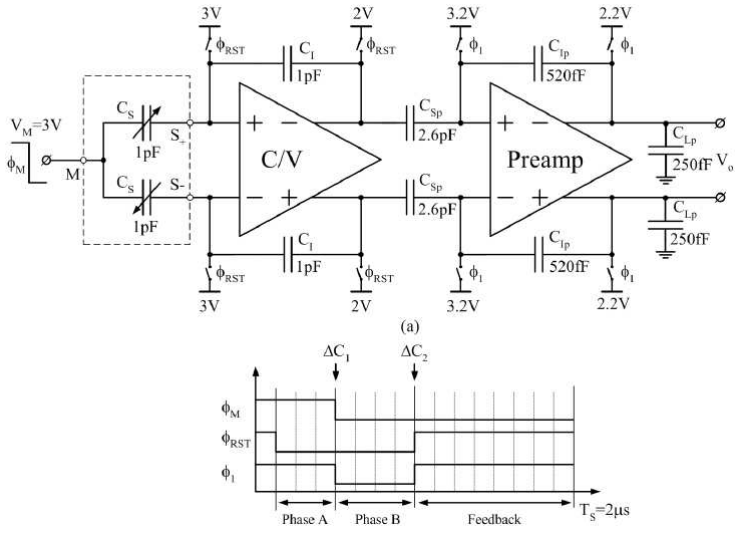
- Correlated double sampling
- Eliminates large bias resistor and demodulator
- Noise folding penalty due to output sampling



[Boser & Howe, JSSC 3/1996]

Readout Circuit Variants (2)

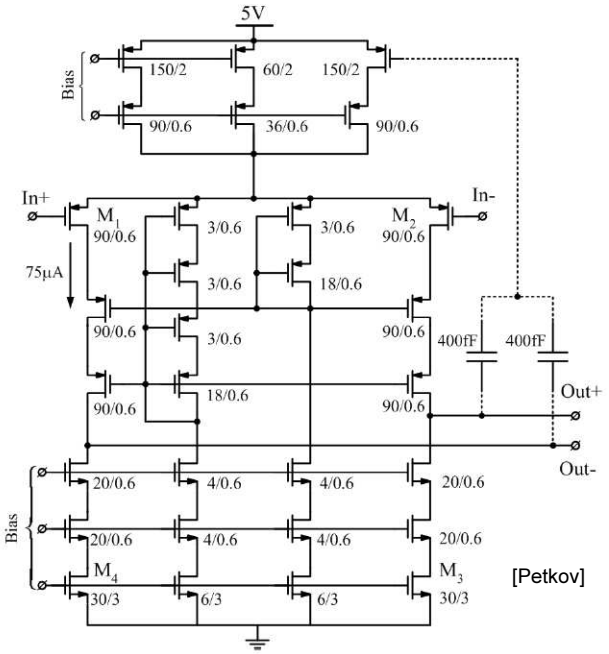
- Correlated double sampling at output of first amplifier
- Differential signal path comes with usual benefits (PSRR, …)
- kT/C noise on C_s is cancelled along with offset and flicker noise of the amplifier



[Petkov]

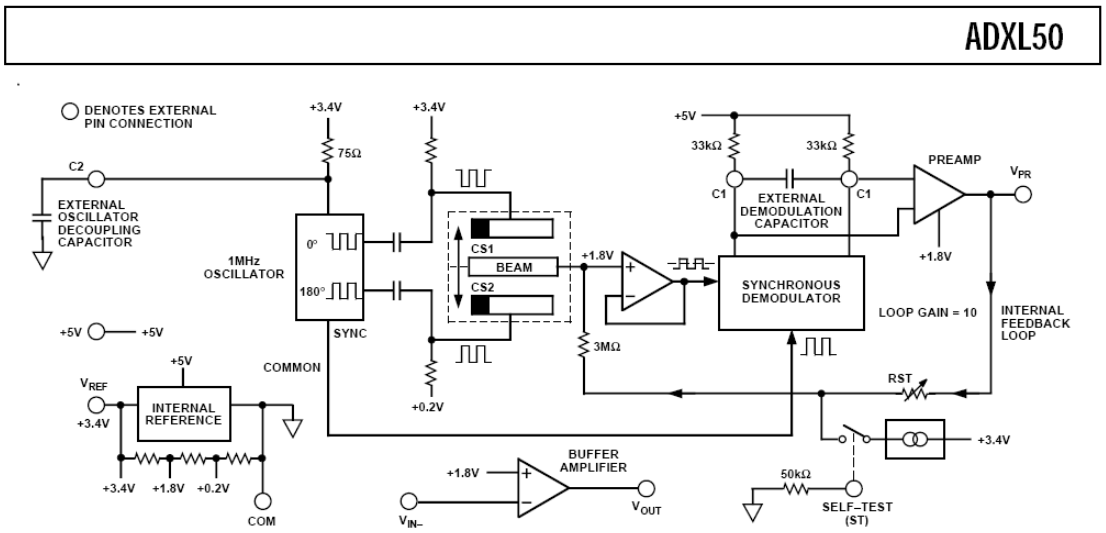
C/V Amplifier Implementation

- Small signals, 5V supply→ plenty of headroom for cascodes



[Petkov]

Continuous Time Force Feedback

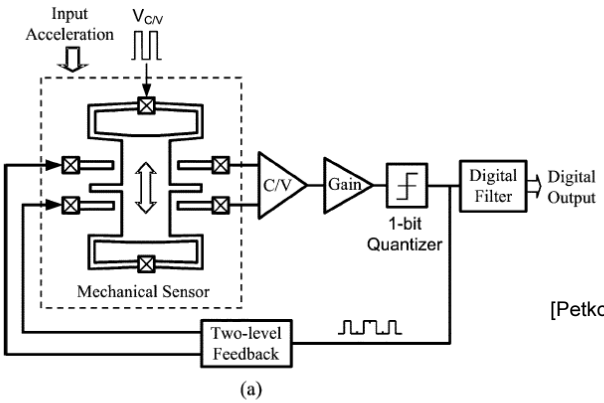


Benefits of Feedback

- Sensing fingers are kept near zero displacement
  - Improves linearity
  - Prevents structure from pull-in/stiction when excited near resonance (important for high Q, vacuum)
- Usable bandwidth increased by loop gain
  - Can reduce sensor resonance frequency to improve sensitivity
- Reduces drift
  - Gain no longer set by sensor parameters

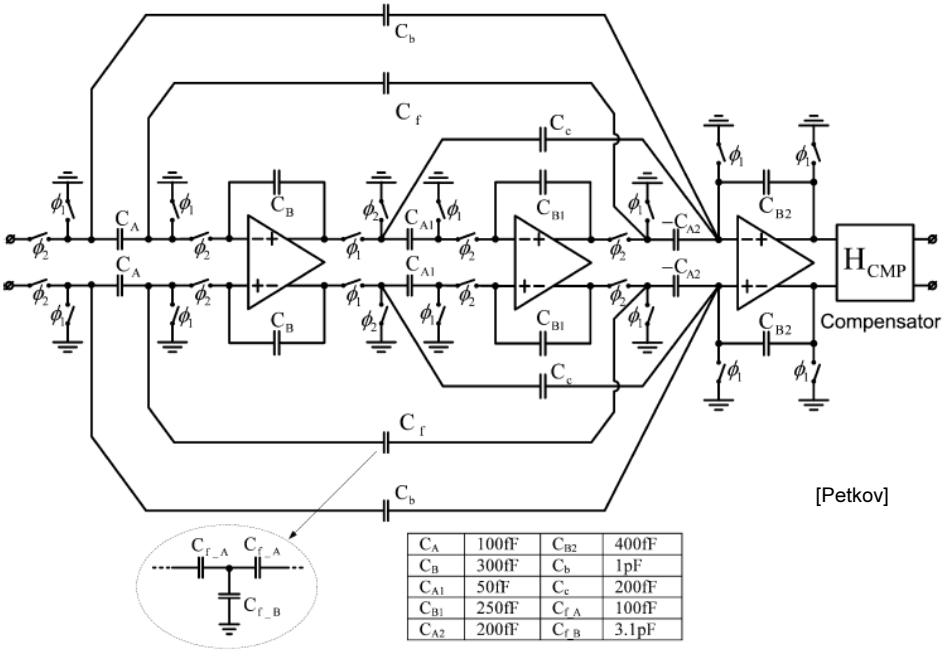
Digital Force Feedback (1)

- Provides inherent A/D conversion
- Output is a pulse density modulated bit stream
  - Sigma-delta modulation, see EE315B



[Petkov]

Digital Force Feedback (2)



[Petkov]

C_A	100fF	C_{B2}	400fF
C_B	300fF	C_b	1pF
C_{A1}	50fF	C_c	200fF
C_{B1}	250fF	C_{f_A}	100fF
C_{A2}	200fF	C_{f_B}	3.1pF

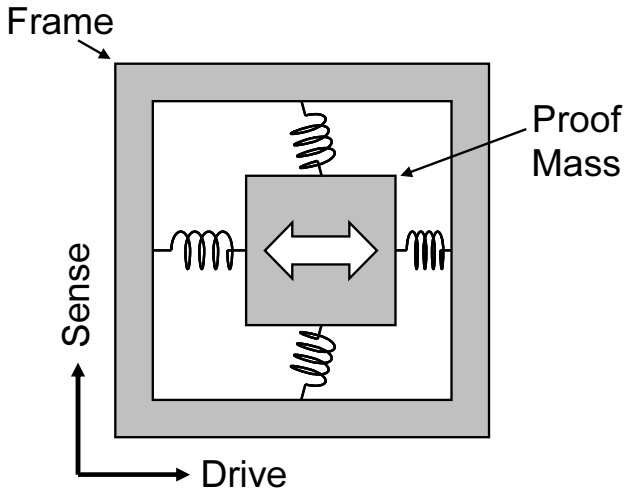
Architecture Comparison (1)

Interface type	Advantages	Disadvantages
Chopper-stabilized, open-loop	• High resolution – no aliasing, minimal number of noise sources. • Low front-end power – SNR not limited by capacitor size. • Suitable for discrete-component implementation.	• Low bandwidth and dynamic range, sensitive to process and ambient variations (open-loop). • Requires additional filtering and ADC for digital output. • Requires large biasing resistors.
Discrete-time (CDS), open-loop	• Compatible with standard VLSI CMOS process. • Output can be digitized directly.	• Large capacitors needed for low kT/C noise. • Low bandwidth and dynamic range, sensitive to process and ambient variations (open-loop).

Architecture Comparison (2)

Interface type	Advantages	Disadvantages
Continuous-time force-feedback	• High resolution • Large bandwidth and dynamic range – scaled by the loop-gain. • Reduced sensitivity to process and ambient variations.	• Requires additional filtering and ADC for digital output. • Requires linearization of voltage-to-force feedback. • System stability affected by high-order dynamics in the mechanical element.
Digital force-feedback (sigma-delta modulation)	• Analog-to-digital conversion performed by the feedback loop. • Intrinsically linear with two-level feedback. • Large bandwidth and dynamic range, low sensitivity to process and ambient variations.	• Quantization noise affects resolution in second-order modulators. • System stability affected by loop delay and high-order dynamics in the mechanical element.

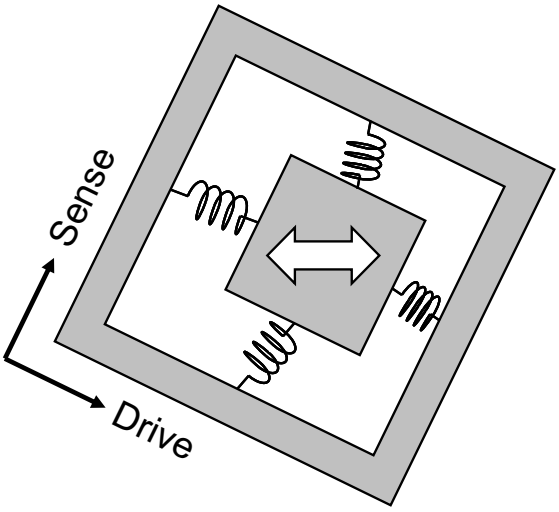
Gyroscope Principle (1)



[Chinwuba D. Ezekwe]

Gyroscope Principle (2)

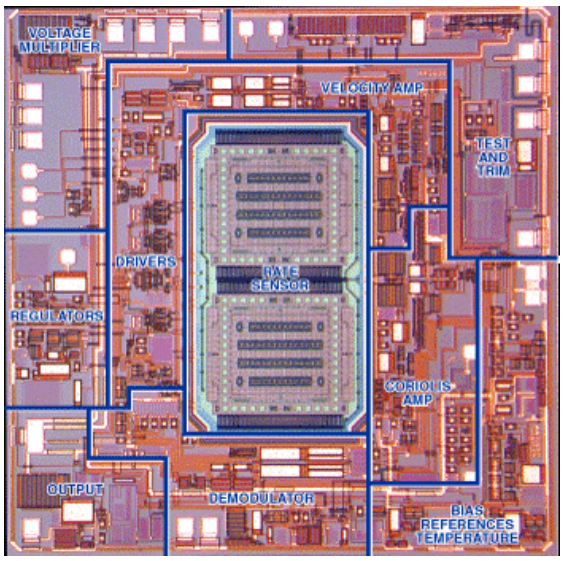
- Proof mass oscillates ~10μm
- Rotation causes sub pico-meter displacement in sense direction
- Displacement is measured through capacitive readout, similar to accelerometer



Clockwise rotation

[Chinwuba D. Ezekwe]

Example: ADXRS150/300



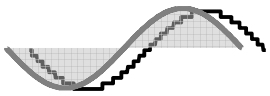
- Resolves a capacitance change of 10^{-20} F in a BW of 1 Hz
- Corresponding displacement is 10^{-14} m
  - Classical radius of an electron (!)

http://www.analog.com/library/analogDialogue/archives/37-03/gyro.html

References

- Bernhard Boser's MEMS notes, http://www.eecs.berkeley.edu/~boser/pdf/index.htm
- V. P. Petkov and B. E. Boser, "Capacitive interfaces for MEMS," in Enabling technology for MEMS and Nanodevices, Baltes, Brand, Fedder, Hierold, Korvink, Tabata, eds., Wiley-VCH, 2004, pp. 49-92.
- N. Yazdi, F. Ayazi, and K. Najafi, "Micromachined inertial sensors," Proceedings of the IEEE, vol. 86, pp. 1640-1659, 1998.
- V.P. Petkov and B.E. Boser, "A fourth-order ΣΔ interface for micromachined inertial sensors," IEEE J. Solid-State Circuits, vol.40, no.8, pp. 1602-1609, Aug. 2005.

Physical Layout

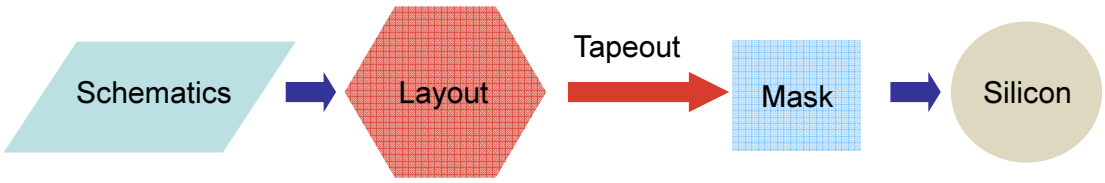


David Su & Boris Murmann
Stanford University

Part I – Physical Layout Basics

- Floorplanning
  - blocks, power/ground
  - metal density rule
- Passives: resistors, capacitors,
- Transistors

Basics



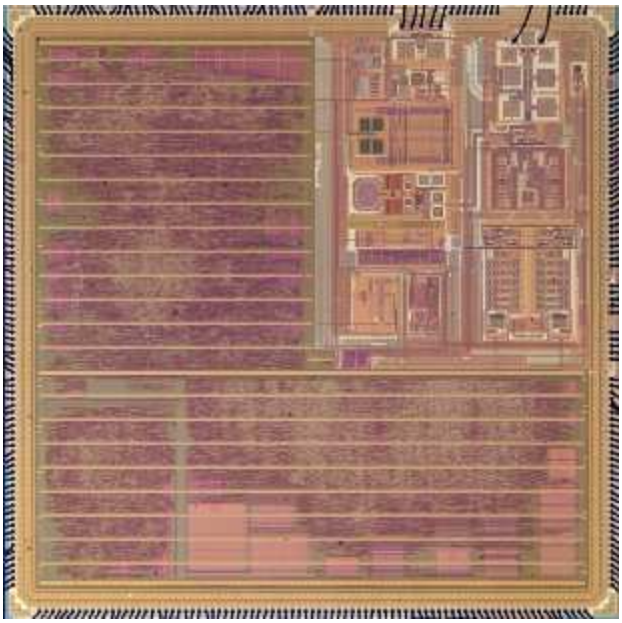
- DRC: Design Rule Check
- LVS: Layout Vs Schematics
- LPE: Layout Parasitic Extraction

Tapeout

- Layout database is stored in gds format
- Transfer to foundry was done on magnetic tape (Tapeout)
- Tape is not used today.

Photo from wikimedia.org

Chip micrograph



Design Rules

- Design rules defines geometry in x-y dimension
  - Width, spacing, overlap
- z dimension is pre-determined by the foundry/process
- Understand design rules
  - Design rules: must
  - Recommended rules: want
  - Guidelines: nice to have
- Following design rules ensures functionality and yield

Floorplanning

- Do planning before layout of cells
  - Estimate area and package pins
  - Organize block placement
  - Package choice:
    - Size of package vs die
    - Length of bond wire and package trace (esp. for power/gnd)
    - Coupling between adjacent bond wire and package pins
    - Avoid a large output signal coupling back to weak input signal
- Iterative process

Block Level Layout

- For each block:
  - Determine pin location of each block including power/gnd
    - Where are the signals coming and going
  - Place the transistors
  - Plan power routing (current path)
    - A “ground” or “vdd” label on a metal line does not change parasitic resistance or inductance
    - “vdd” needs decoupling capacitors to “ground”
  - Routing of sensitive nodes
    - Separate noisy (digital, clock, …) and quiet (input, bias, …) signals
    - Shield signal signals using ground, vdd, digital control signals that are not toggling
    - Decouple (add capacitors) sensitive dc signals (bias, supply)
- Iterative process

Reminders

- Resistance (including metal / poly)
  $V = I R$
- Inductance (long metal traces, bond wire)
  $V = L \, di/dt$
- Capacitance (charging current)
  $I = C \, dv/dt$

Metal Routing

- Width of metal:
  - Electro-migration: ~1mA/um
  - IR drop: ~50-100mohms/square/layer
  - Wide metal rule < ~10um (process dependent) but use multiple layers or parallel lines
- Establish metal routing ground rules to ease layout
  - Example: M1, M3 horizontal; M2, M4 vertical

Routing Signals

- Use low impedance node
  - Example: route current instead of high impedance voltage nodes
- Watch for IR drop in current
  - Voltage headroom
- Shield sensitive signals
  - Use return path shields
  - Choose vdd or gnd
- Shielding adds capacitance
  - Consider spacing to reduce coupling

CMP Effect

- Chemical-Mechanical Polishing (CMP) process planarizes wafer surface after each metal layer; Otherwise, unevenness of one layer that may affect the next layer
- Relative hardness of metal and oxide affects the polishing
- Solution:
  - Metal coverage rule: Keep relatively uniform density of metal/oxide over ~100um diameter
  - Metal density rule to avoid large area without metal → dummy metal fill
  - Limit the width of metal to avoid large area with only metal → metal slot rules

Dummy Metal Fill

- Automatic generation of small rectangles in “empty” space to provide more uniform density
- Dummy metal can impact parasitic capacitance.
- Can block the automatic generation of dummy metal (with a dummy block layer) for critical circuits

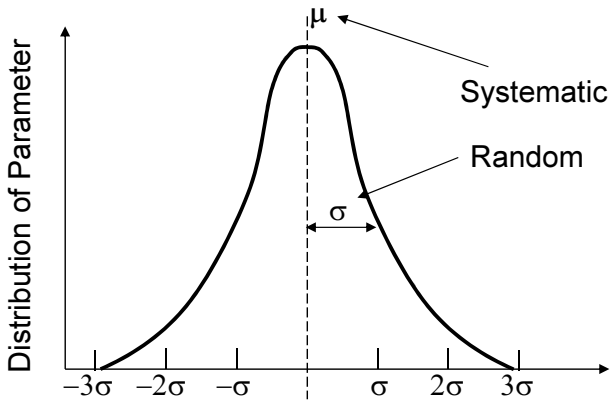
Wide Metal

- Metal width can not be too wide
  - Copper is softer than oxide.
  - CMP can over polish the copper, reducing its thickness (increasing resistance) and making the overall surface less planar (more difficult for higher layer metal)
- Add slots to metal width to increase the density of oxide
  - Or, avoid using very wide metal, use several narrower metal lines in parallel

Matching

- A major advantage of VLSI design is device matching:
  - Fully differential circuits → CMRR, offset
  - Current mirrors
  - Ratioed devices: capacitors, resistors, transistors
- Random mismatch:
  - Process: geometry, implant dose, …
- Systematic:
  - Mask gradient
  - Thermal gradient

Systematic vs Random Mismatch



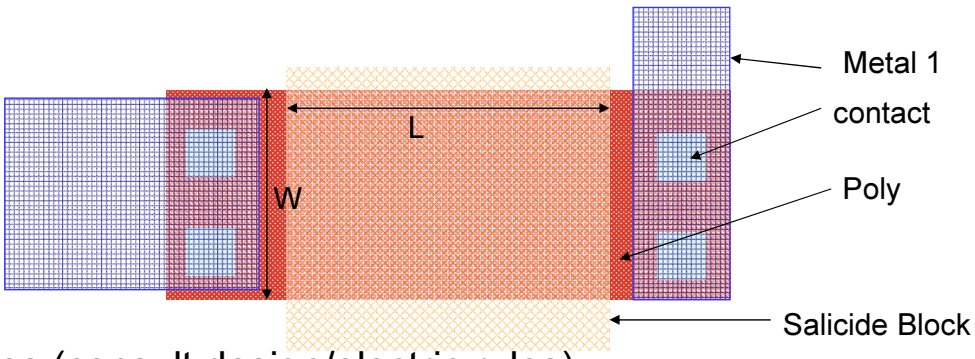
- Systematic mismatch changes the average
- Random mismatch leads to fluctuation/spread

Intrinsic Resistor

- Ohms/square, $R_{\square}$; voltage coefficient
- Types:
  - Poly (salicided vs non-salicided)
  - Diffusion (salicided vs non-salicided)
  - Nwell for kohm/square

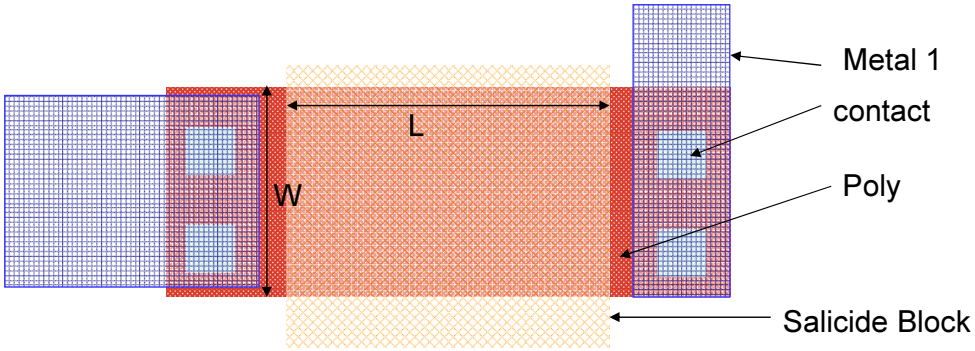
$$R_{intrinsic} = \#\ of\ Squares\left(\frac{L}{W}\right) \times R_{\square}$$

Poly Resistor 1



- Types (consult design/electric rules)
  - p or n doped
  - salicided or non-salicided
  - Recommended width > minimum poly width
  - Choice: $R_{\square}$, voltage coefficient, matching

Poly Resistor 2

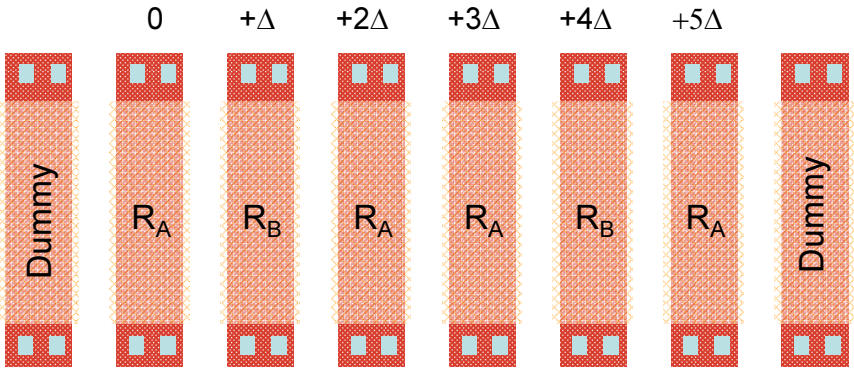


- Resistance = 2 X R_{end} + $R_{intrinsic}$
- Keep W large to reduce R_{end}
- Keep L large to reduce voltage dependency

Resistor Matching

- Systematic Mismatch
  - Use identical unit elements
  - Keep same orientation, environment
    - Use dummy resistors
    - Minimize metal routing over resistors (keep all metal routing identical) to reduce noise coupling
  - Watch out for mask gradient, temperature gradient, pressure gradient
    - Keep devices in close proximity
    - Use interdigitated layout
- Random Mismatch
  - Keep W and L large to reduce random mismatch
  - Reduce the contribution of R_{end}

Interdigitated Resistor Layout



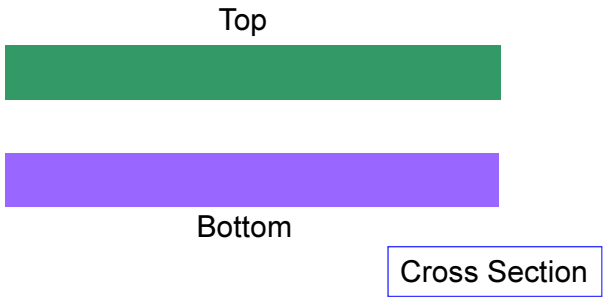
Top View

- Interdigitated: ABAABA
- Remove linear gradient in temperature, mask CD, pressure

Capacitor

- Metal sandwich capacitor
  - Small fF/um^2
- MiM: Metal-insulator-Metal (process option)
  - 1-2 fF/um^2
  - Best matching
- Interdigitated metal capacitor
  - Standard process
  - Almost as high density as standard MiM
  - Matching is not as good as MiM
- MOS capacitors
  - High density
  - Poor voltage coefficient

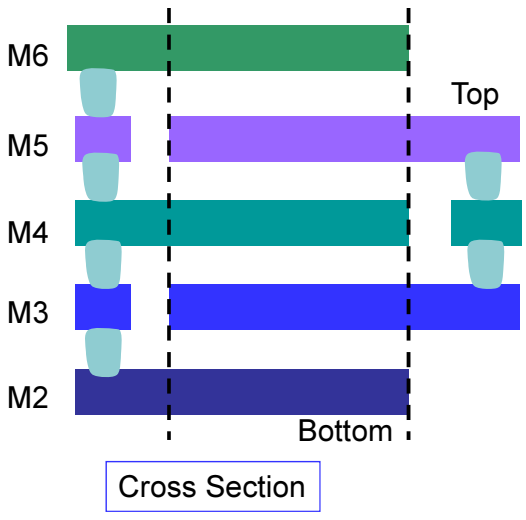
Intrinsic Capacitor

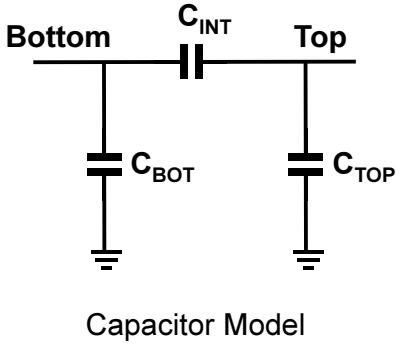


- Assume no fringing effect

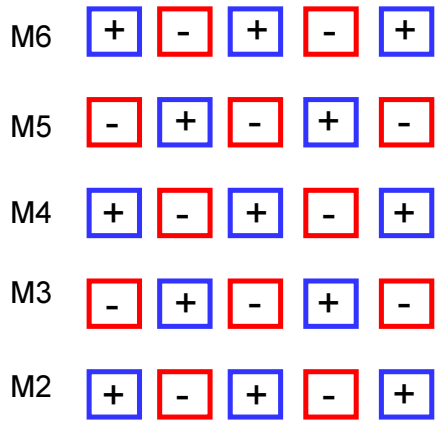
$$C_{INT} = \frac{\varepsilon}{t_{ox}} \text{Area}$$

Sandwich Capacitor





Interdigitated Capacitor



Cross-section

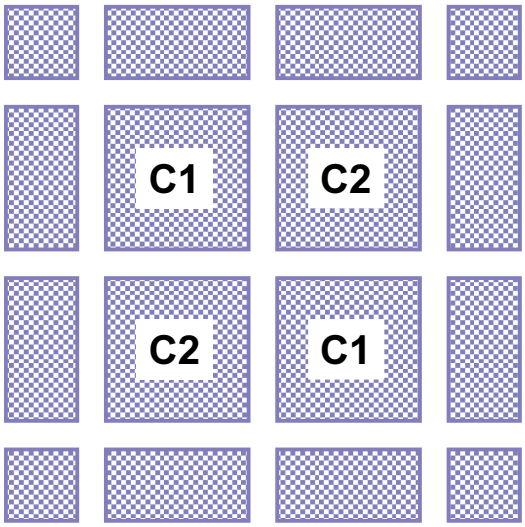
- Alternating fingers of capacitors
- Vertical separation is larger than horizontal separation; most capacitance from lateral flux
- Other permutations are possible (see references)

H. Samavati, et al, "Fractal Capacitors," JSSC, Dec 1998.
R. Aparicio, A. Hajimir, "Capacity limits & matching properties of integrated capacitors, JSSC, March 2002.

Capacitor Matching

- Systematic Mismatch
  - Use identical unit elements in an array
  - Keep same environment
    - Use dummy capacitors
  - Watch out for mask, temperature, pressure gradient
    - Keep devices in close proximity
    - Use common centroid layout
  - Keep routing parasitics small and matched
- Random Mismatch
  - Use large area to reduce random mismatch

Common Centroid Capacitor

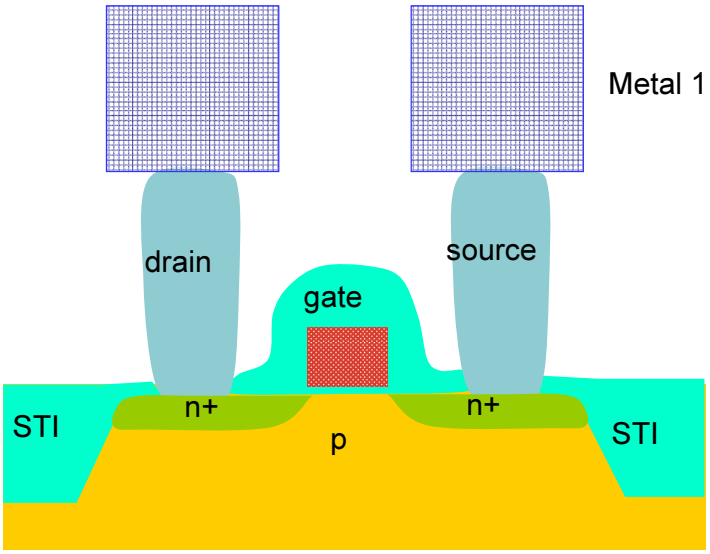


Top View

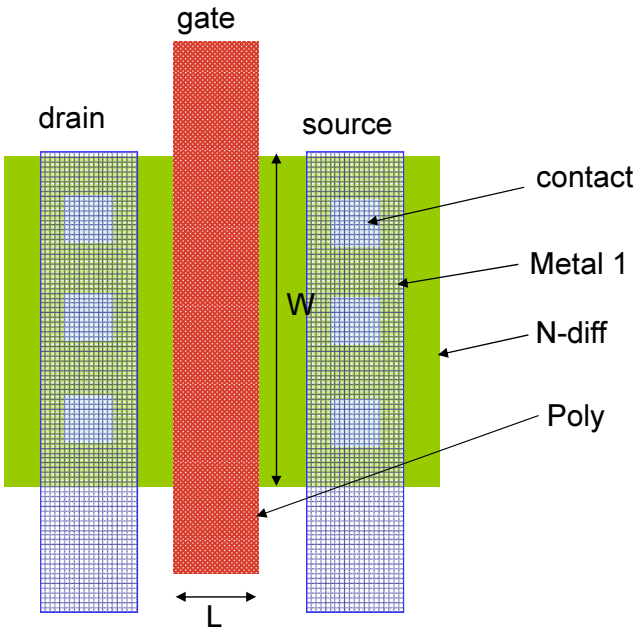
MOS Transistors

- Layout
- Random Mismatch
  - Process tolerance → Large W and L
  - Vt, beta → keep Vgs-Vt large
- Systematic Mismatch
  - Gradient: Common centroid layout
  - Implant angle: Step symmetry vs mirror symmetry
  - Neighbor effect: add dummies

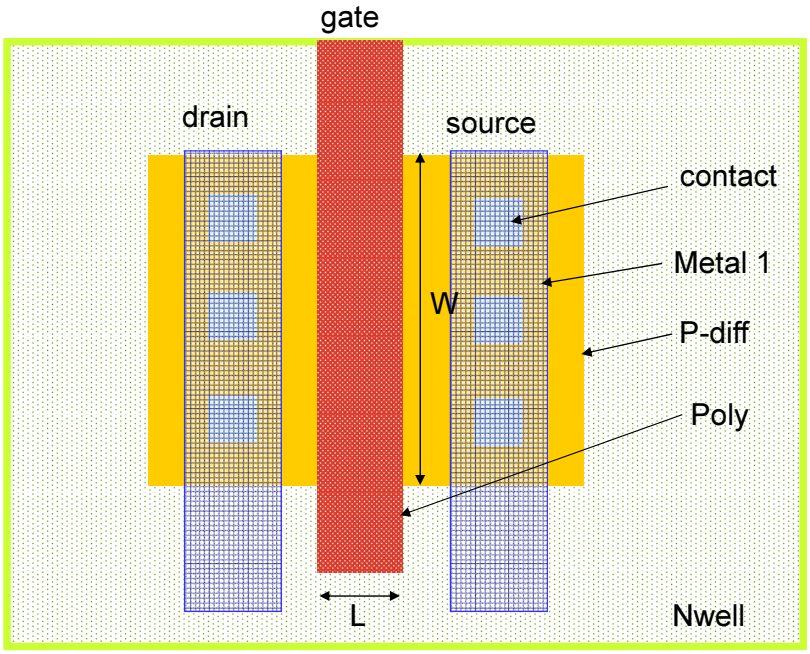
NMOS Transistor Cross-Section



NMOS Transistor Top View

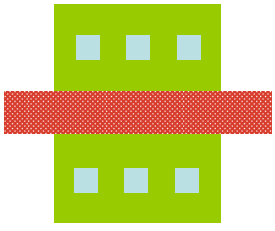


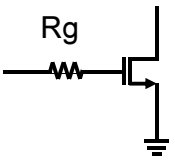
PMOS Transistor Top View



Gate Resistance

- Gate resistance:
  - Keep W short
  - Connect on one end: Rg = 1/3 x (W/L) x $R_{\square}$
  - Connect on both ends: Rg = 1/12 x (W/L) x $R_{\square}$





Ref: Razavi et al, "Impact of distributed gate resistance on the performance of MOS devices," IEEE Trans circuits & systems I, Nov 1994.

Random Transistor Mismatch

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_T)^2$$

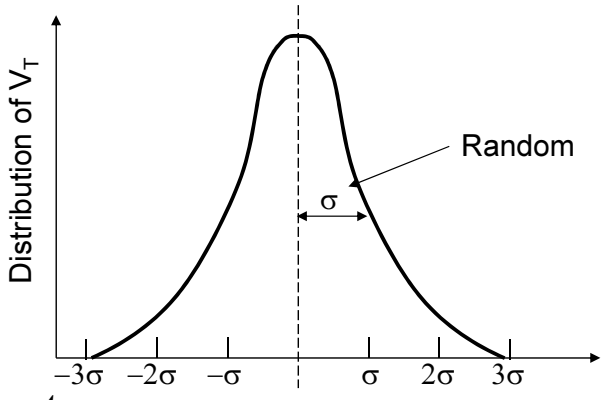
$$I_D = \frac{\beta}{2}(V_{GS} - V_T)^2$$

Random Mismatch in: V_T and β

$$\sigma^2_{\Delta I_D / I_D} = \frac{4\sigma^2_{\Delta V_t}}{(V_{GS} - V_T)^2} + \sigma^2_{\Delta\beta/\beta}$$

Ref: Pelgrom et al, "Matching Properties of MOS Transistors," JSSC, Oct. 1989.

Random Threshold Mismatch



$$\sigma_{\Delta V_t} \approx \frac{A_{VT}}{\sqrt{W \times L}}$$

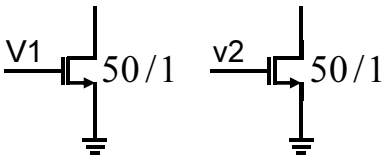
Ignoring distance effect

A_{VT} = 3 – 10 mV μm

Process Dependent

Ref: Pelgrom et al, "Matching Properties of MOS Transistors," JSSC, Oct. 1989.

Example: Threshold Mismatch



If $A_{VT} = 5mV\mu m$

$$\sigma_{\Delta(V1-V2)} \approx \frac{A_{VT}}{\sqrt{W \times L}} = \frac{5mV\mu m}{\sqrt{50\mu m \times 1\mu m}} = 0.71mV$$

Ignoring distance effect

Ref: Pelgrom et al, "Matching Properties of MOS Transistors," JSSC, Oct. 1989.

β Mismatch

$$\sigma\Delta_{\Delta\beta/\beta} \approx \frac{A_\beta}{\sqrt{W \times L}}$$

Ignoring distance effect

$$A_\beta \approx 0.5 - 3\,\%$$

V_t Matching Data

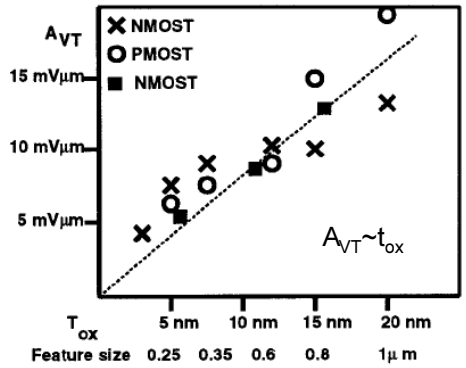


Fig. 3. Evolution of matching coefficient over process generation. Squares are derived from[4], the other measurements are by the authors.

[Pelgrom, IEDM 1998]

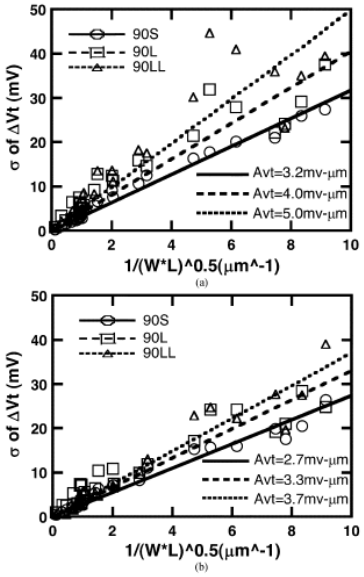
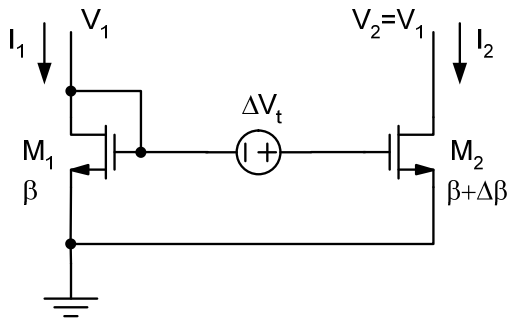


Fig. 5. (a) NMOS and (b) pMOS mismatch performance for 90S, 90L, and 90LL devices.

90nm data

[Chang, Trans. Electron Devices, 7/2005]

Mirror Inaccuracy Due to Mismatch



$$\Delta I = I_1 - I_2 \cong -g_m \Delta V_t + I_1 \frac{\Delta\beta}{\beta}$$

$$\frac{\Delta I}{I_1} \cong -\frac{g_m}{I_1}\Delta V_t + \frac{\Delta\beta}{\beta}$$

$$\sigma^2_{\frac{\Delta I}{I_1}} \cong \frac{g_m}{I_1}\sigma^2_{\Delta V_t} + \sigma^2_{\frac{\Delta\beta}{\beta}}$$

- Example: W=10μm, L=0.35μm, g_m/I_D=10S/A, A_{VT} = 7mV/um, A_β=1%

$$\sigma_{\frac{\Delta I}{I_1}} = \sqrt{\left(10\frac{S}{A}\cdot 3.7mV\right)^2 + (0.53\%)^2} = \sqrt{(3.7\%)^2 + (0.53\%)^2} = 3.74\%$$

- Threshold mismatch usually dominates

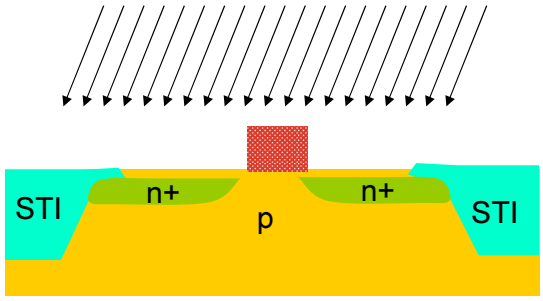
Systematic Mismatch

- Gradient: Thermal, Mask, Pressure
  - Common centroid layout
- Implant angle: Step symmetry vs mirror symmetry
- Neighbor effect: add dummies

Gradient Cancellation

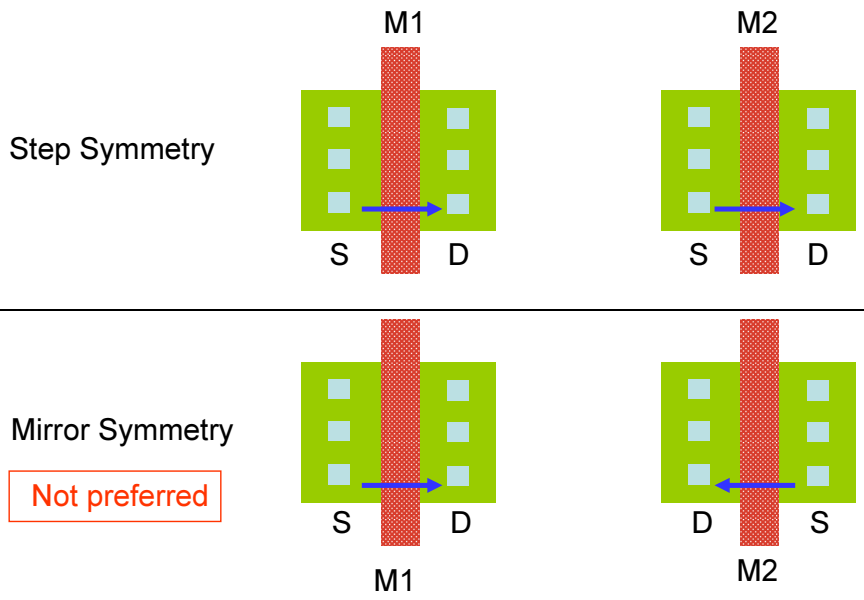
- Gradient: Thermal, Mask, Pressure
- Linear gradient is easy to cancel
  - Common centroid layout
- Other techniques exist for higher order gradient cancellation
  - Ref: G. Van der Plas, et al, JSSC, Dec 1999

Implant Angle

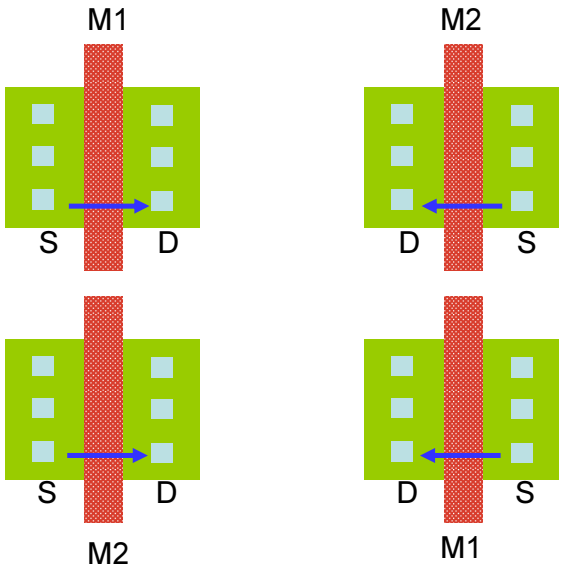


- A small angle of 7 deg in implant results in slight different in implant; modern processes will compensate for this but ...
- Keep same orientation/direction of current for matched devices
  - Step symmetry vs mirror symmetry

Step vs Mirror Symmetry

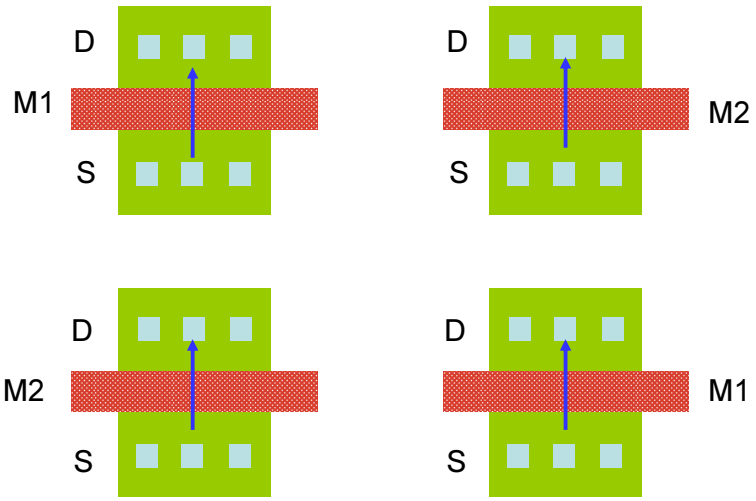


Common Centroid Transistors 1



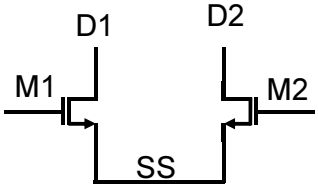
Cancellation of offset due to current flow direction

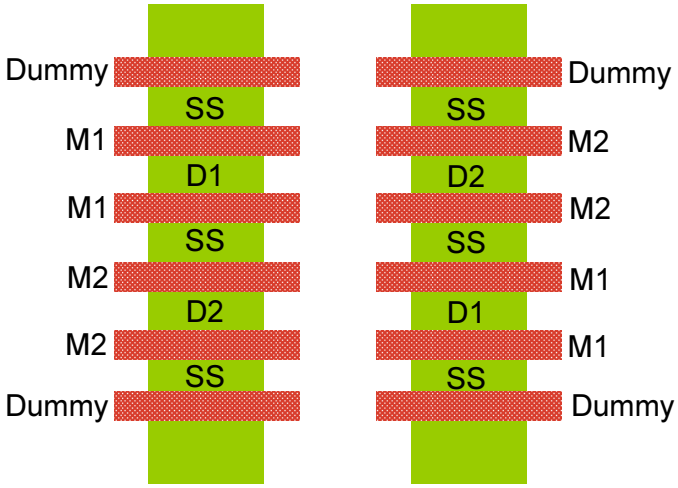
Common Centroid Transistors 2



Same current flow direction

Differential Pair





Neighbor Effects

- Keep the “neighborhood” of matched transistors identical
- Add dummy transistors for the “edged” devices
- Watch out for z-direction as well
  - Metal layers must also match
  - Avoid Metal-1 overlap

Second order effects

- Second order effects of MOS transistors
  - Antenna rule
  - Strained silicon
  - Well proximity

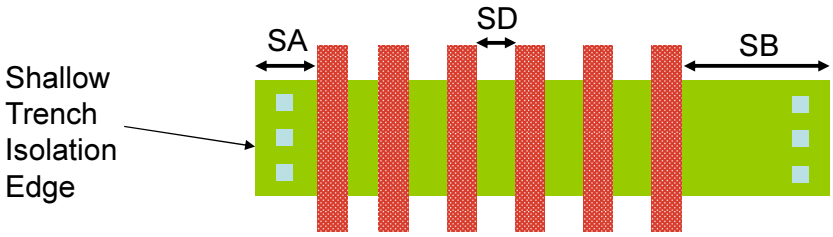
Antenna Rule

- Implant/deposition process can induce charge on metal and create voltage stress on gate capacitance
- Q=CV; If C is small, V is large → Damage! Large V_T shift
  - Q depends on area (Copper) and perimeter (Aluminum) of metal
  - C depends on the W x L (area) of the transistor gate

$$V \propto \text{Metal - Gate Ratio} = \frac{\text{Area/Perimeter of Metal}}{\text{Gate area of transistor}}$$

- "Antenna rule" violation when induced voltage V exceeds safe limits.
- Solution: Add "antenna" (reverse-biased) diodes to shunt charge

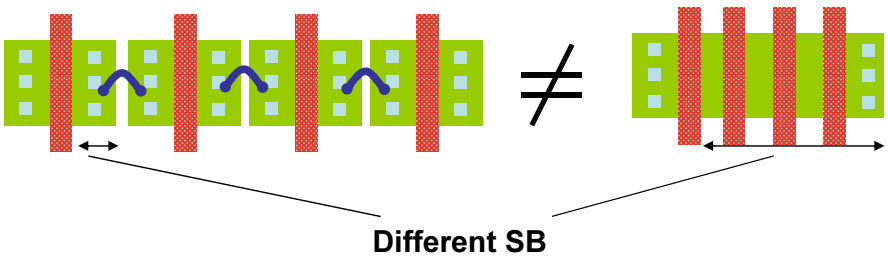
Length of Diffusion (LOD) Effect



Source: Sally Liu, ISSCC 2006 SET

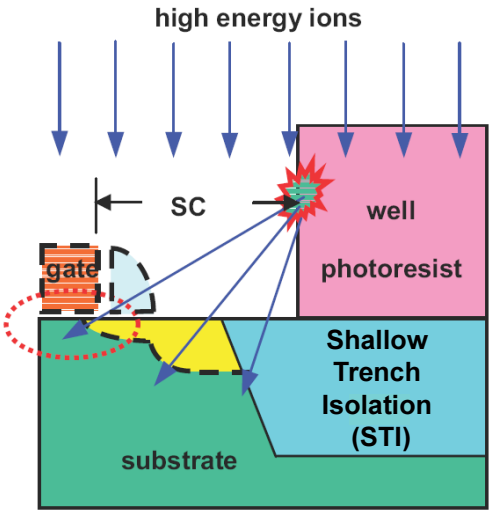
- STI (shallow trench isolation) induces mechanical stress effect on transistor → strained device
- Starting with 130nm/90nm and modulated by the distance between poly and OD/STI edge (SA, SB)
- Applies to both NMOS and PMOS (see DRC)
- Effect can be extracted in Layout Parasitic Extraction (LPE) simulations.

Minimizing LOD Effect



- Use unit devices for best matching
- Avoid using irregular diffusion shape
- Use dummy transistors on both ends of a multi-finger device to keep the same SA and SB for matching

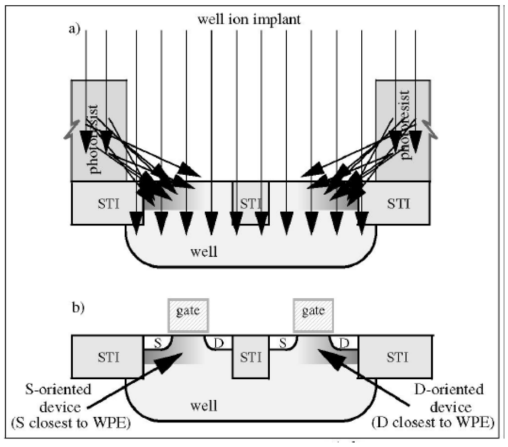
Well Edge Proximity Effect 1



Y-M Sheu et al, CICC 2005

- Well proximity ions scatter at well photo resist edge, bounce into the active region and thus increase the device threshold voltage
- Affects device matching
- Important for Well to gate spacing: SC of 1um or less
- Should be modeled by LPE extraction
- Well proximity effect reduced by guard ring

Well Edge Proximity Effect 2



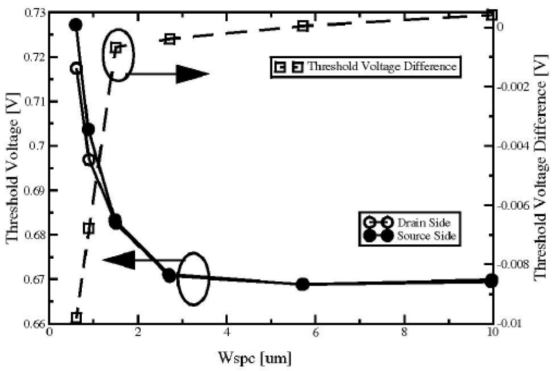
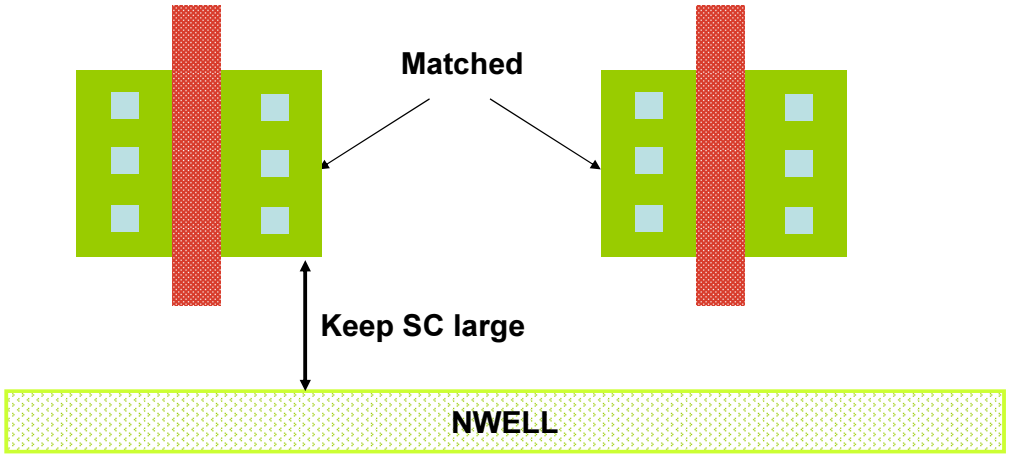


Fig. 3: Vt versus well-edge distance for 3.3V nMOS device on a 0.13um technology.

- P. G. Drennan et al., "Implications of Proximity Effects for Analog Design," Proc. CICC, pp.169-176, Sep. 2006.

Minimizing WPE Effect



- Keep distance between gate to well as large as possible (>> 1um; see DRC)
- For matching, keep SC equal and large

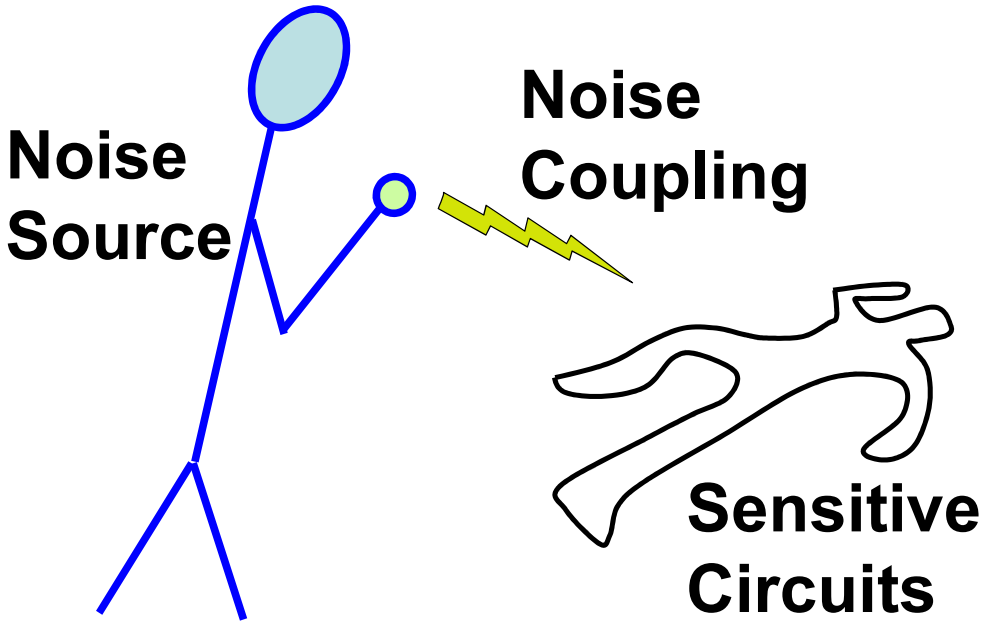
Transistor Matching

- Keep transistor area large
- Use same size, shape, orientation, and in close proximity
- Keep same voltage, current, temperature
- Minimize gradient effect: common centroid
- Keep neighbors (up to >10um) identical in x, y, and z directions
  - Use dummy devices
  - Avoid edge of chip

Part II: Design Related Issues

- Noise coupling effects
- Latchup
- ESD

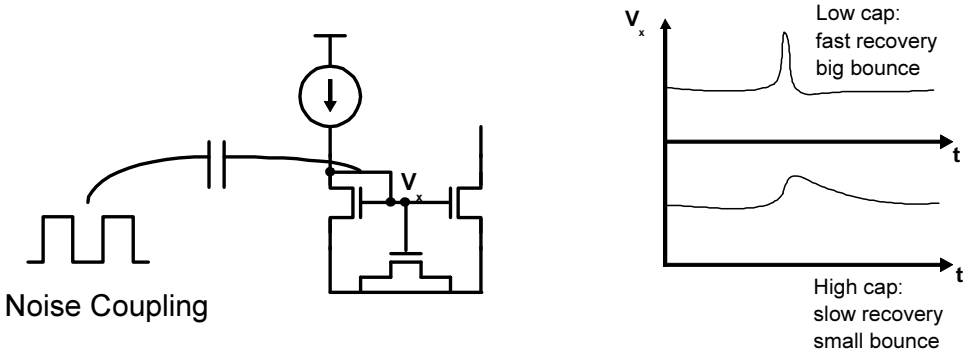
Noise Interference



Noise Coupling Mechanisms

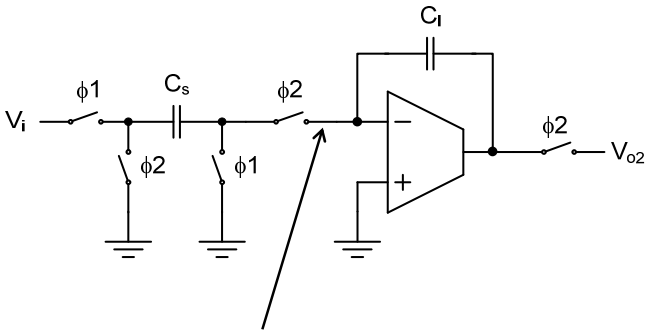
- Capacitive
  - E.g. through on-chip wire crosstalk
- Inductive
  - E.g. through bond wires
- Supply coupling
  - Modulation of supplies due to IR or Ldi/dt drop
- Substrate coupling

Capacitive Coupling -- Bias



- Can use decoupling capacitors to reduce the amplitude of noise coupling into bias nodes
- If noise is "deterministic" and occurs at a “don’t care” point in time, you might be better off not decoupling, but making the bias node "fast" (small mirror ratio, no decoupling cap) so it can recover quickly
- Must go for either extreme case: no decoupling or large decoupling

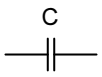
Capacitive Coupling -- SC



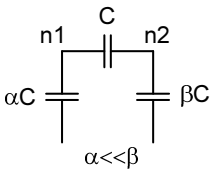
- Must minimize coupling into charge conservation node
  - Proper placement of "bottom plate" parasitics
  - Substrate shielding

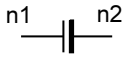
Capacitor Parasitics

Ideal Capacitor

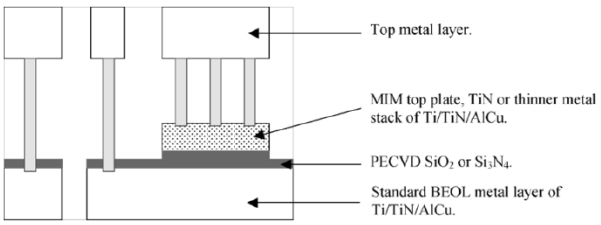


Typical Integrated Circuit Capacitor



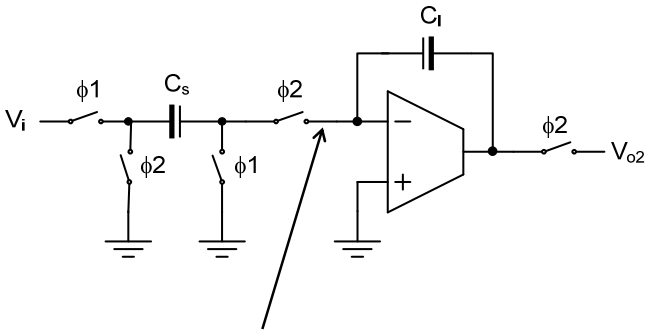


E.g. α~1%, β~10% for a MIM capacitor



[Ng, Trans. Electron Dev., 7/2005]

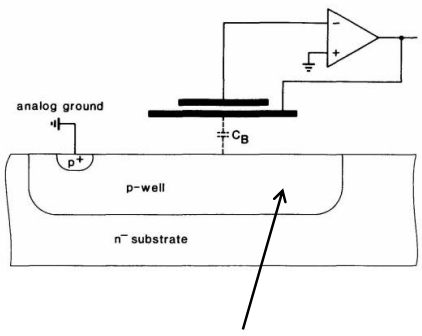
Proper Configuration



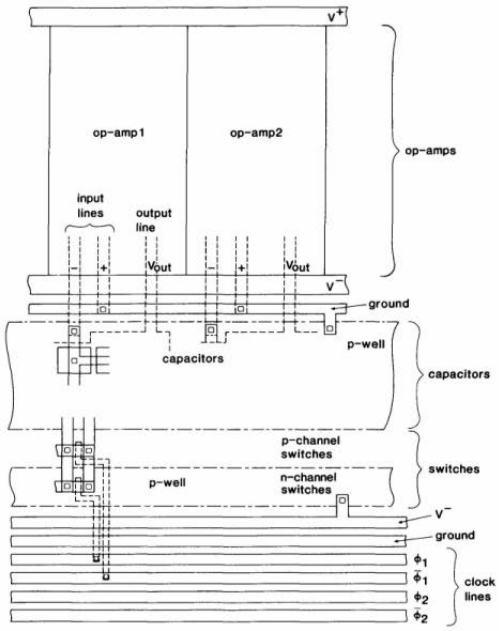
Keep wiring as short as possible and do not cross with any other signal
May want to place a “clean” shield between wires and substrate

Layout

Gregorian & Temes, pp. 518, 524



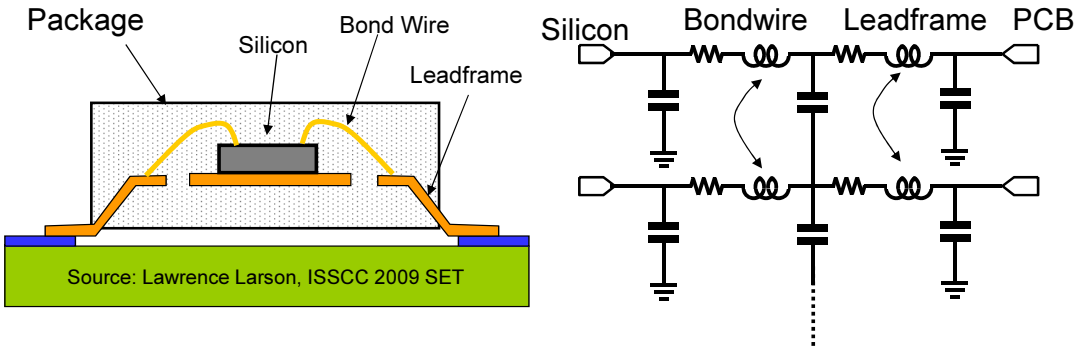
Can use metal shield in a modern process to protect coupling to output. Such a shield is usually not needed when the signals are differential



Floorplanning

- A common mistake is to do a great job of laying out lots of little cells but then make a big mess when pulling the design together
- A good floorplan is essential to being able to quickly make a good layout with few iterations
- A floorplan is an evolving document that helps the designer organize the chip into pieces that fit together well
  - Don't be afraid to change it as you go along and discover new issues, just start out with one so you don't miss the obvious things that can be very painful later
- Know when to stop! You can easily get so carried away with these issues that your layout takes a very long time to complete
- The key is to do what is right for the application
  - An RF mixer should minimize capacitance
  - A 14-bit A/D converter needs well a very balanced layout
  - …

Inductive Coupling through Bondwires



- **The leadframe/wirebond interface may require careful modeling**
- **Ground pin is not "ground" (~1 nH/mm)**
- **Significant mutual coupling between two adjacent traces (K ~ 0.4)**
  - **Parallel ground bonds is not very effective (reduction to ~0.7L)**
- **Sometimes better off keeping sensitive signals on chip**
  - **E.g. VCO control voltage**

Test/Application Board

- Planning begins with chip pin-out
  - Uhps, my analog pin is right next to a digital output...
- Not "black magic", but weeks of design time and "thinking"
- Key aspects
  - Supply/ground routing
  - Bypass capacitors
  - Coupling between signals
- Good idea to look at vendor datasheets for example layouts/schematics/application notes
- For good practices on how to avoid issues see e.g.
  - Analog Devices Application Note 345: "Grounding for Low-and-High-Frequency Circuits“
  - A Practical Guide to High-Speed Printed-Circuit-Board Layout, http://www.analog.com/library/analogDialogue/archives/39-09/layout.html
  - http://www.hottconsultants.com/techtips/split-gnd-plane.html

Vendor Eval Bord Layout

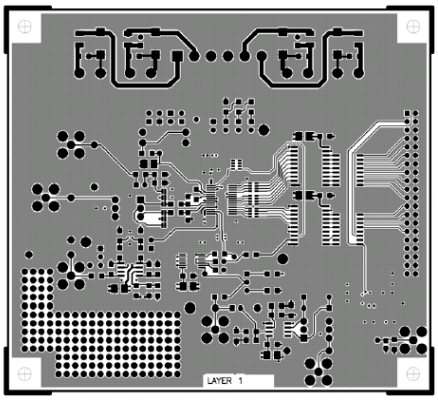


Figure 21. TSSOP Evaluation Board Layout, Primary Side

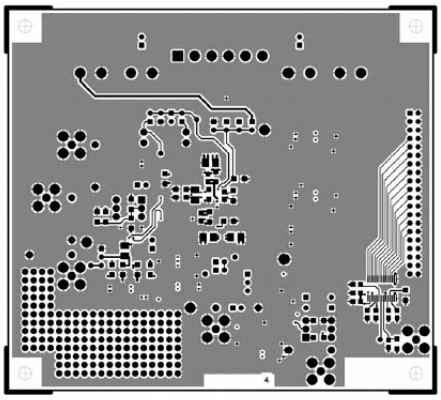


Figure 22. TSSOP Evaluation Board Layout, Secondary Side

[Analog Devices AD9235 Data Sheet]

Supply Noise

- Typical culprits
  - Digital logic
  - Clocks
  - IO pads
- Preventive measures
  - Reduce noise by turning off unused digital logic
    - Clock gating, etc.
  - Avoid oversized digital buffers (large current spikes, high frequency content)
  - Stagger digital switching in time; try to minimize activity at certain instants (e.g. when sampling switch opens)
- Avoid large number of digital pads switching simultaneously
  - Work with “current mode” outputs where possible

LVDS Outputs

Helps minimize dynamic currents due to I/O

Cost: additional pin

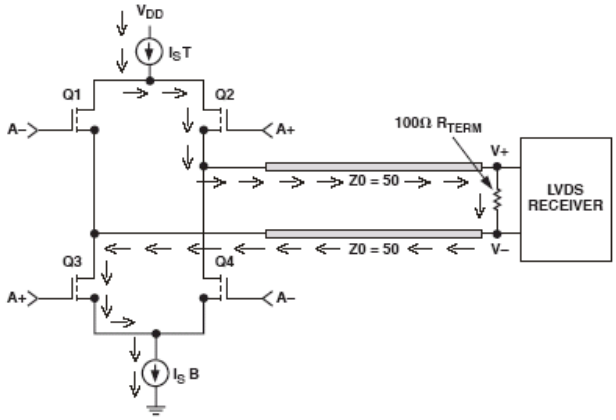
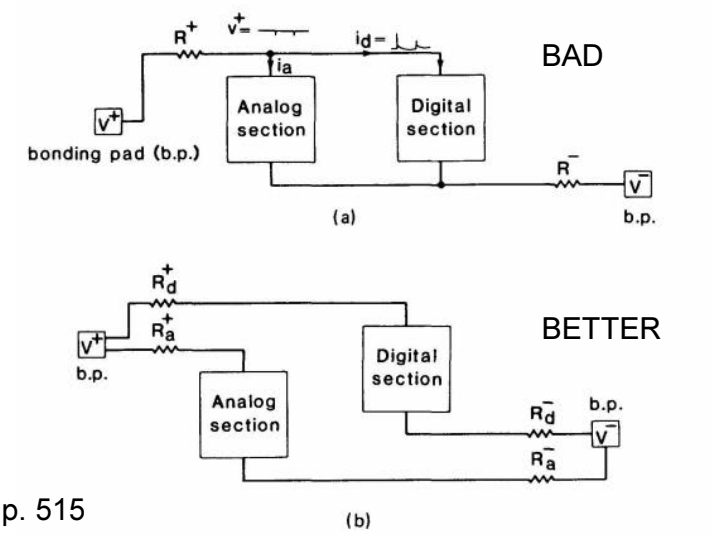


Figure 4. LVDS Output Current

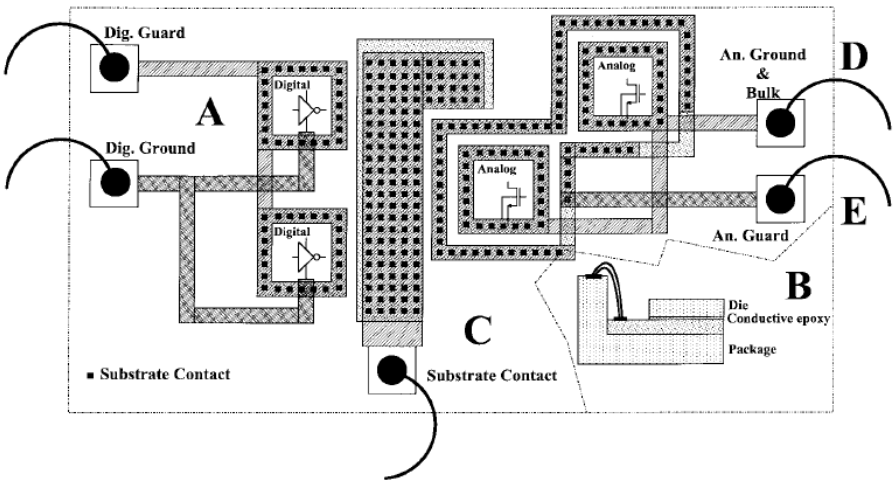
Analog Devices Application Note 586: "LVDS Data Outputs for High Speed ADCs"

Basic View of Supply Noise



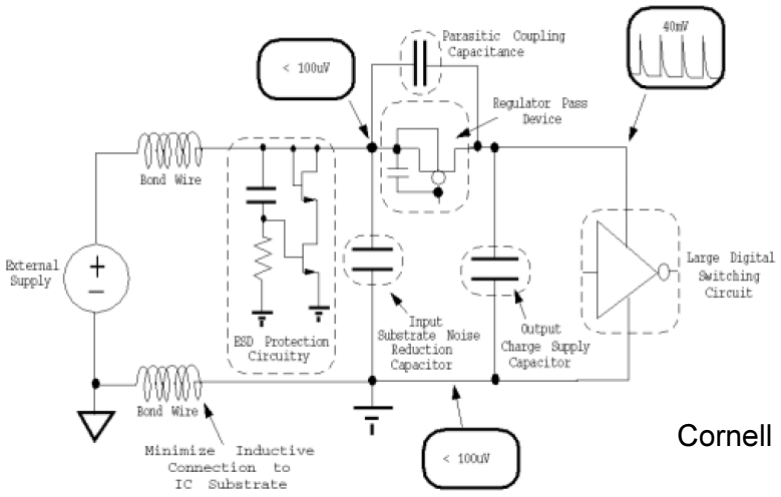
Gregorian & Temes, p. 515

Proper GND Separation



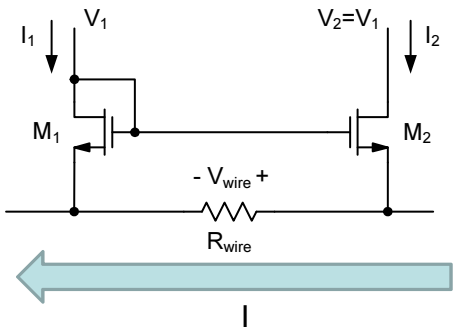
M. Ingels and M.S.J. Steyaert, "Design strategies and decoupling techniques for reducing the effects of electrical interference in mixed-mode IC's," IEEE J. Solid-State Circuits, pp.1136-1141, July 1997.

On-Chip Decoupling



Cornell et al, ISSCC 2002

IR Drop Issues – Mirror Example



$$\Delta I = I_1 - I_2 \cong g_m V_{wire}$$

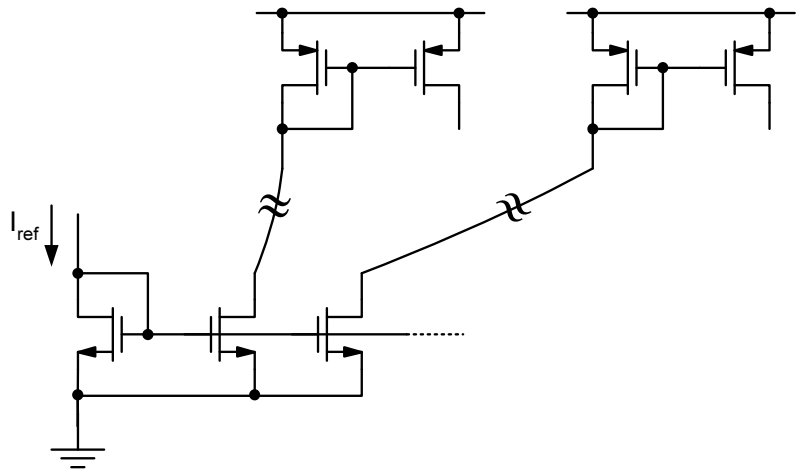
$$\frac{\Delta I}{I_1} \cong \frac{g_m}{I_1} V_{wire}$$

- Want small g_m/I_D ("large gate voltage overdrive") to mitigate errors due to wire IR drop
  - Unfortunately this means large V_{min}

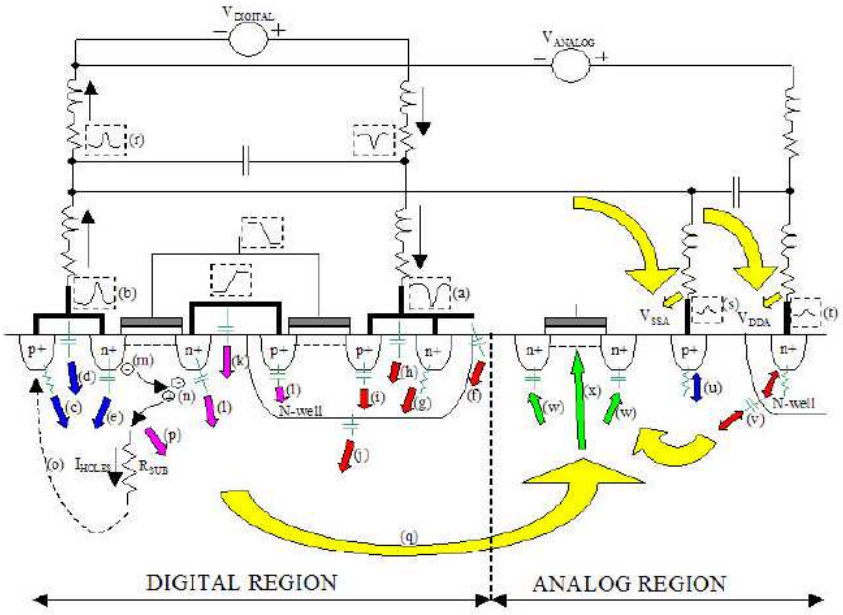
Current Distribution (1)

- Typically, we'll only have one single reference current generator on a chip
- Can generate/distribute currents across chip in two different ways
  - Distribute gate voltage
    - Can cause big problems due to IR drop and process gradients
    - Usually limited to local distribution
  - Distribute currents
    - Have one global bias cell close to reference that sends currents into local biasing sub-circuits
    - Disadvantage: consumes additional current

Current Distribution (2)

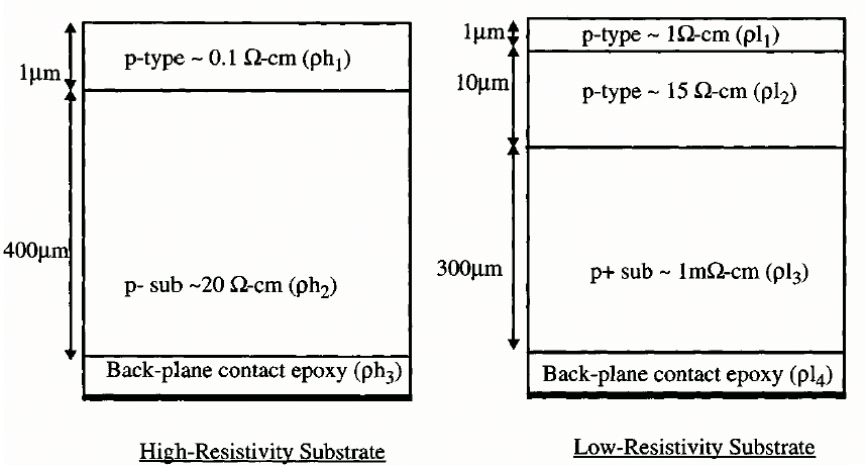


Substrate Noise



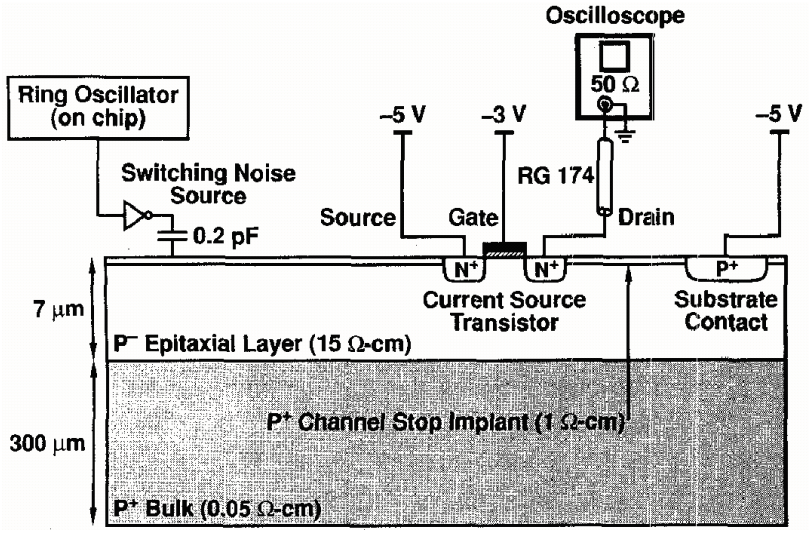
http://www-tcad.stanford.edu/tcad/pubs/theses/iorga.pdf

Substrate Types



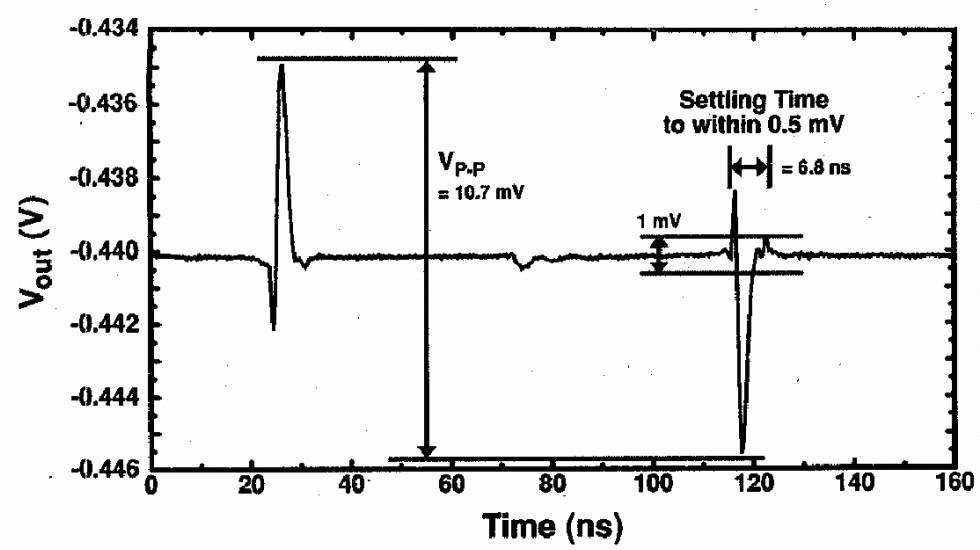
"Epi Substrate"

Epitaxial Substrate



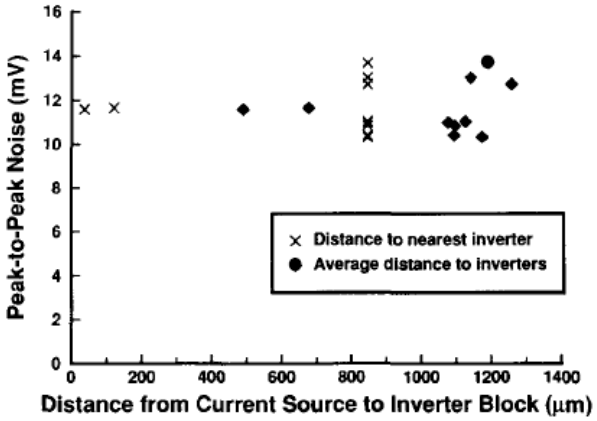
D. K. Su, M. J. Loinaz, S. Masui, and B. A. Wooley, "Experimental results and modeling techniques for substrate noise in mixed-signal integrated circuits," *IEEE Journal of Solid-State Circuits,* vol. 28, pp. 420 - 430, April 1993.

Observed Waveforms



- Current disturbance roughly ± 1%

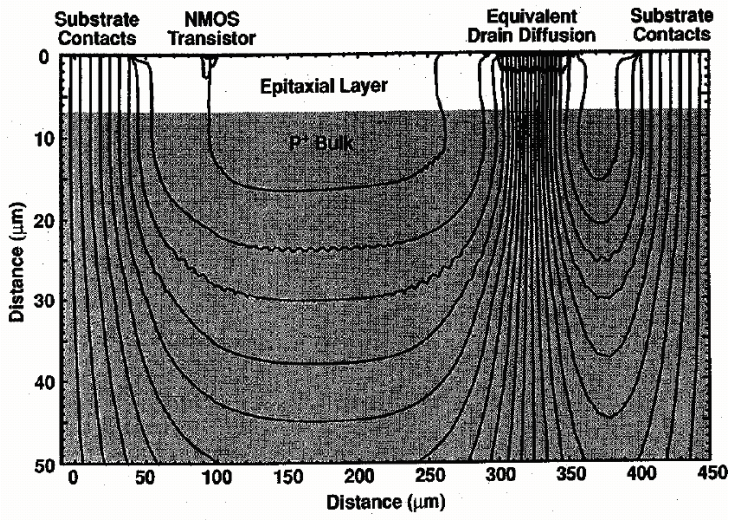
Coupling vs. Distance



- Essentially independent of distance!
  - Why?

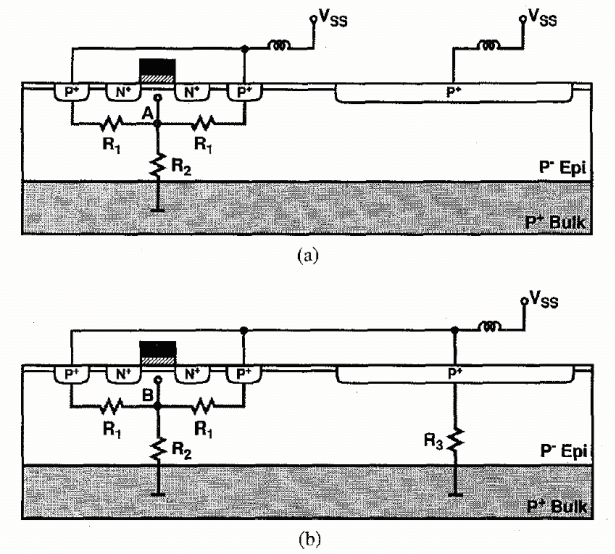
Current Flow in Epi-Substrate

(Setup as in slide 77)

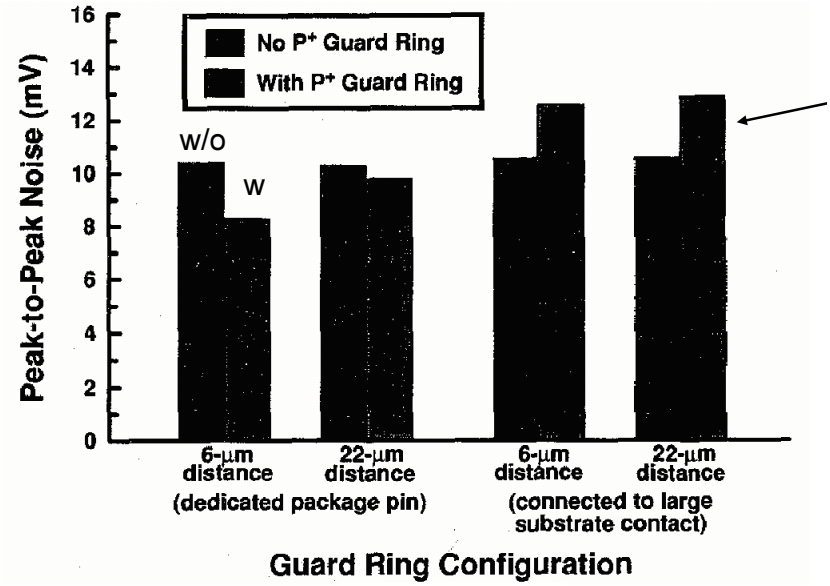


- Majority of current flows in low-resistivity wafer
- Coupling is very weak function of distance

Guard Ring



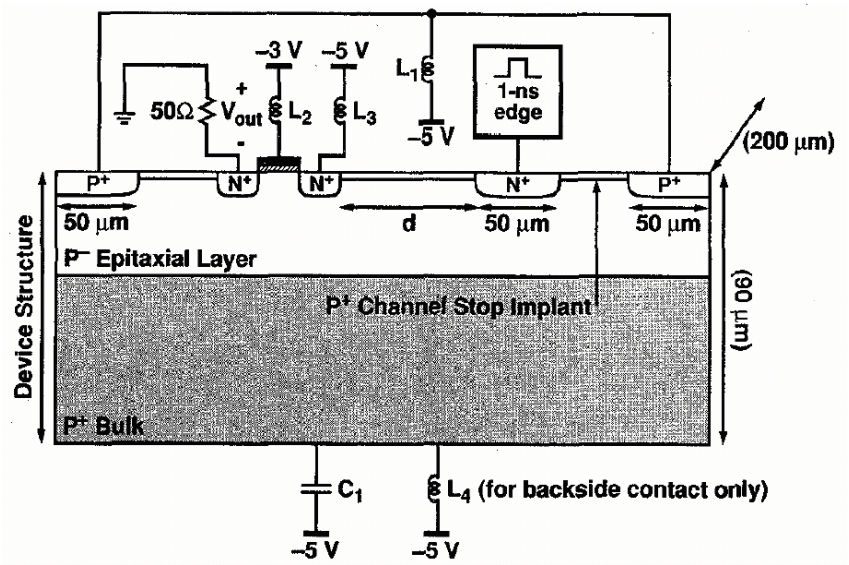
Effect of Guard Ring



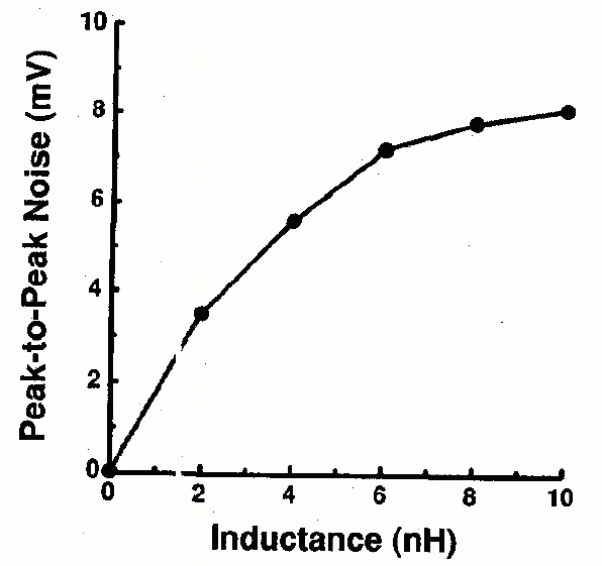
Large guard rings increase coupling!

Epi substrate

Backside Contact



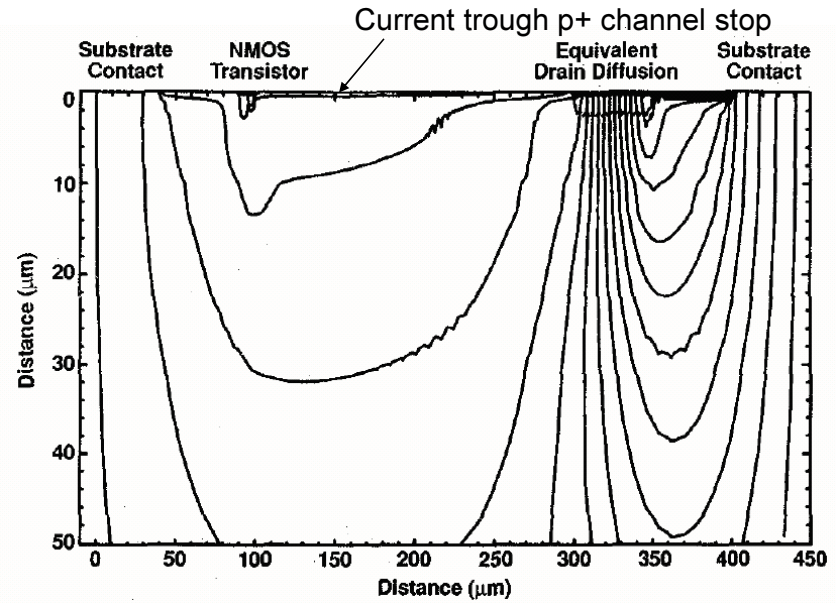
Noise vs. L_4



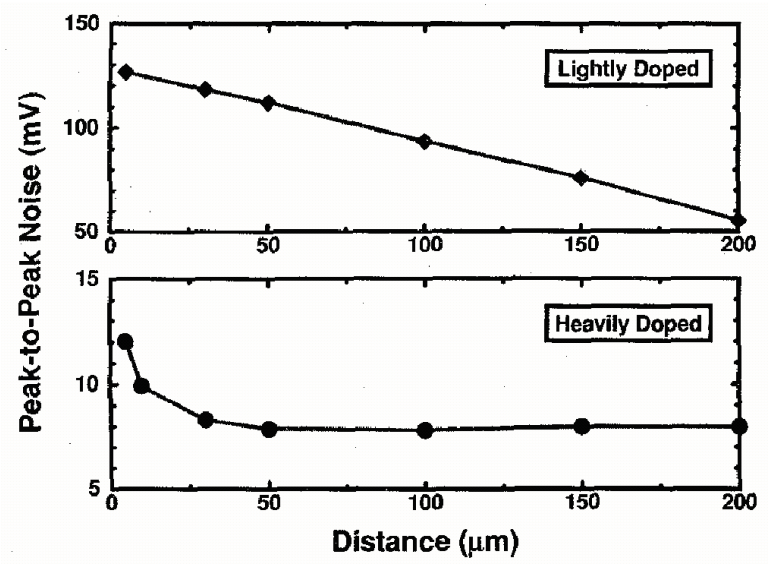
Summary (Epi-Substrate)

- Closely modeled by a "single node"
- The most effective way to reduce coupling in Epi-substrates to is to provide a good, low inductance backside contact
- Unfortunately distance and guard rings don't help much in reducing coupling
- If you decide to use guard rings, make sure to use dedicated guard ring potentials
  - Otherwise guard rings may increase coupling!

Current in High Resistivity Substrate



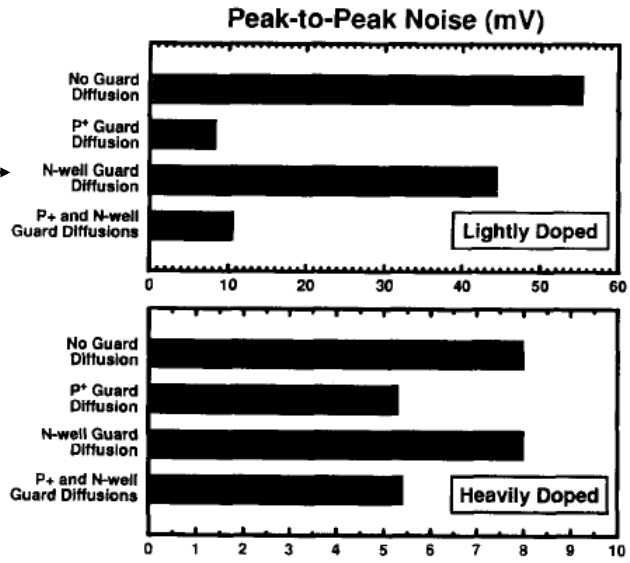
Coupling vs. Distance



(Epi)

Effect of Guard Rings

Breaks p+ channel stop implant →



(Epi)

Example

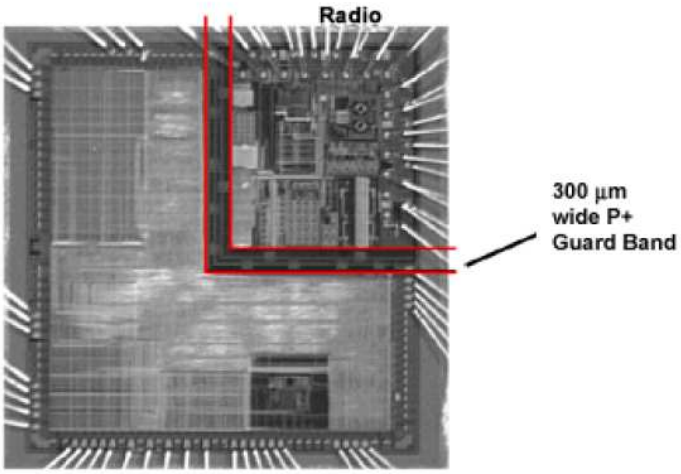


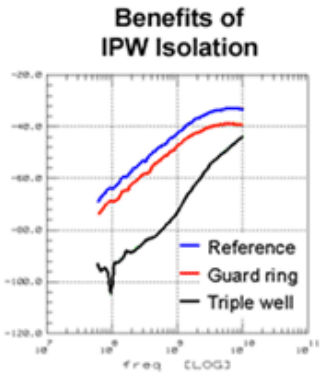
Figure 7: Ericsson single-chip Bluetooth design with a 300-micron-wide, guard band isolation.

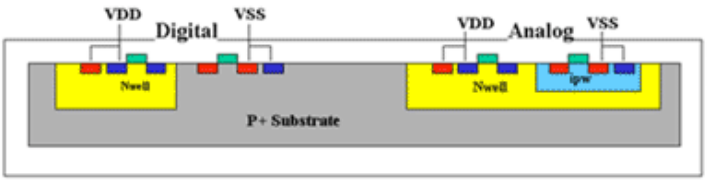
http://www.commsdesign.com/showArticle.jhtml?articleID=192200561

Deep N-Well

Process technology Hip7lp
Compatible with TSMC

Gate length L*poly*	0.13µm
Single gate Ox	30A
Dual gate Ox	50A
Supply voltage	1.6 to 3.0V
Metal	5 layer Cu
Substrate	P+
Nwell resistors	700 ohm/sq.
Salicided Poly res.	7.0 ohm/sq.
Metal Cap	0.8 fF/um^2





http://www.commsdesign.com/showArticle.jhtml?articleID=192200561

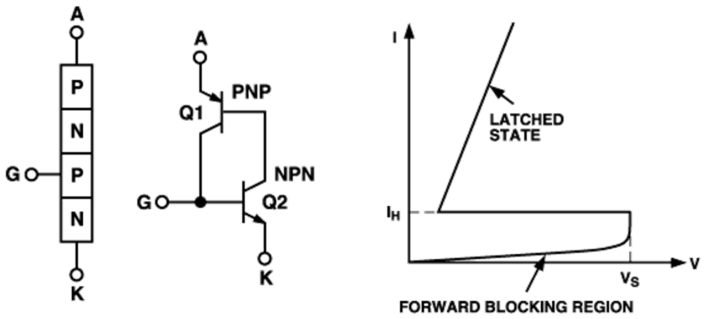
Summary (Lightly doped substrate)

- Distance and guard rings can help reduce coupling significantly
- Must connect guard rings to quiet, dedicated potentials
  - Otherwise they may inject noise!
- Isolation and coupling effects are highly layout dependent
  - If substrate coupling is critical, the designer should invest a good amount of time to think about potential issues and solutions
- CAD tools?
  - Still being developed/finding commercial use

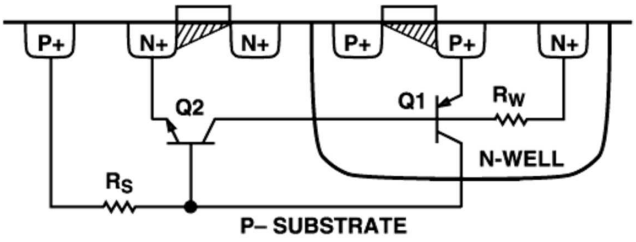
Selected References

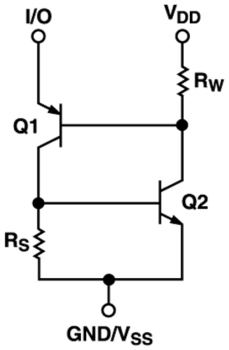
- R. Gharpurey and R. G. Meyer, "Modeling and analysis of substrate coupling in integrated circuits," IEEE Journal of Solid-State Circuits, vol. 31, pp. 344 - 353, March 1996.
- Balsha R. Stanisic, Nishath Verghese, Rob A. Rutenbar, L. Richard Carley, David J. Allstot,"Addressing substrate coupling in mixed-mode ICs: Simulation and power distribution synthesis," IEEE Journal of Solid-State Circuits, vol. 29, pp. 226 - 238, March 1994.
- Kuntal Joardar, "A simple approach to modeling cross-talk in integrated circuits," IEEE Journal of Solid-State Circuits, vol. 29, pp. 1212 - 1219, October 1994.
- Nishath Verghese and David J. Allstot, "Computer-aided design considerations for mixed-signal coupling in RF integrated circuits," IEEE Journal of Solid-State Circuits, vol. 33, pp. 314 - 323, March 1998.
- A. Samavedam, A. Sadate, K. Mayaram, and T. S. Fiez, "A scalable substrate noise coupling model for design of mixed-signal ICs," IEEE Journal of Solid-State Circuits, vol. 35, pp. 895 - 904, June 2000.
- Tallis Blalack et al., “On-Chip RF-Isolation Techniques,” http://www.commsdesign.com/showArticle.jhtml?articleID=192200561

Latchup



Minimize R_S and R_W using proper guard rings!

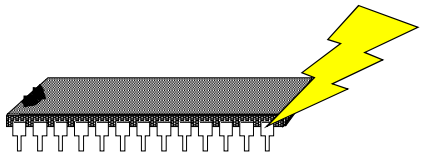




http://www.analog.com/library/analogDialogue/archives/35-05/latchup/

What is ESD?

- Electrostatic discharge
- Example: Charge built up on human body while walking on carpet...
- Charged objects near or touching IC pins can discharge through on-chip devices
- Without dedicated protection circuitry, ESD events are destructive



Models

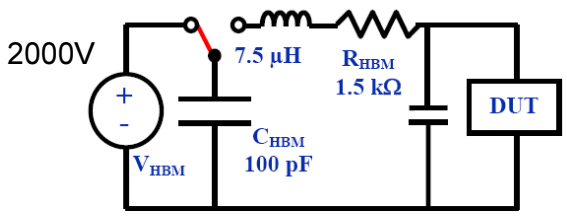


Figure 2.1: Human Body Model (HBM)

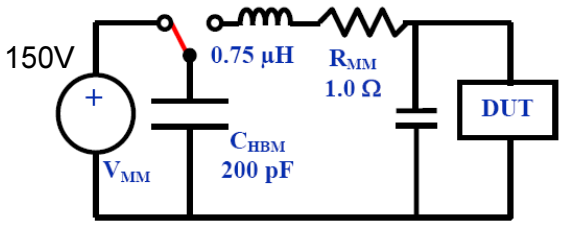


Figure 2.2: Machine Model (MM)

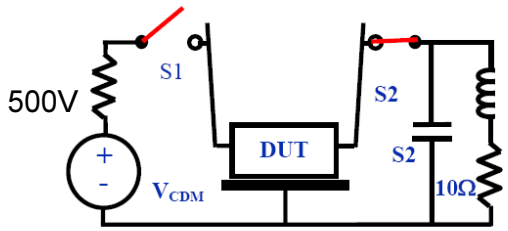
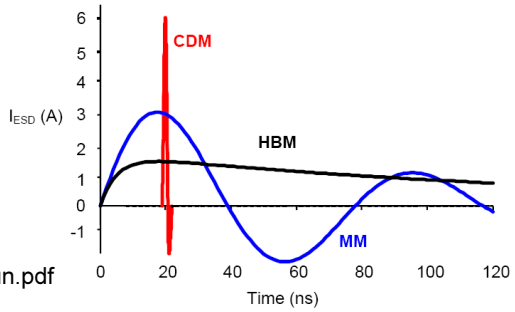
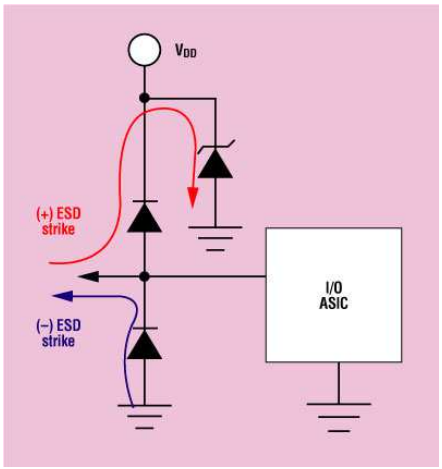


Figure 2.3: Charged Device Model (CDM)



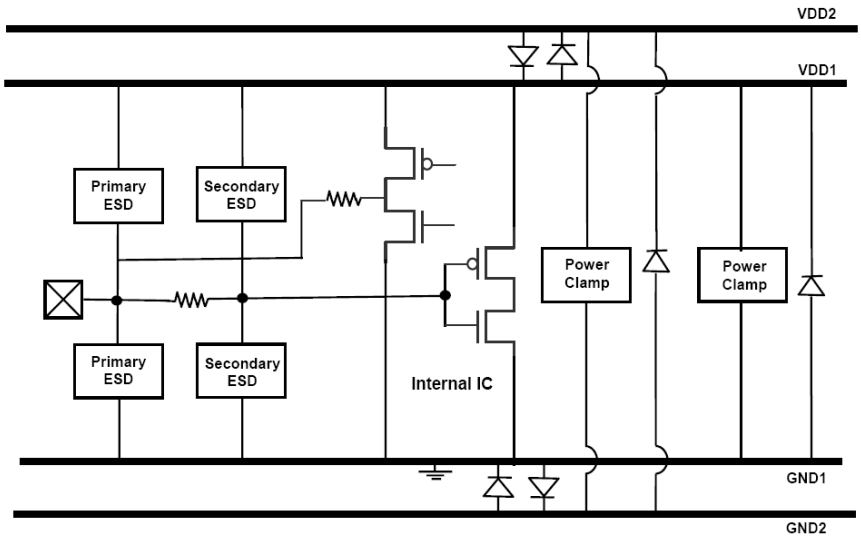
http://www-tcad.stanford.edu/tcad/pubs/theses/chun.pdf

Basic Protection Circuit



[http://www.ce-mag.com/archive/03/ARG/dunnihoo.html]

General Architecture



http://www-tcad.stanford.edu/tcad/pubs/theses/chun.pdf

Rail Clamp Approach

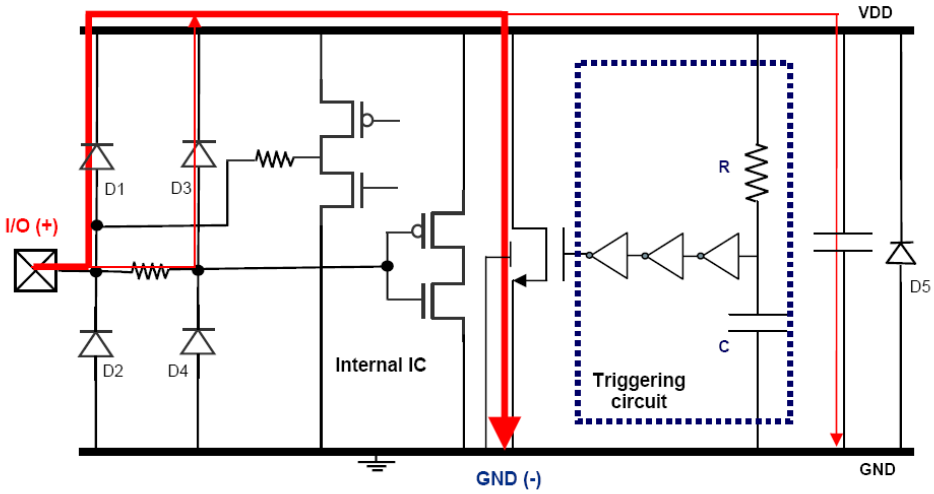


Figure 2.9: Concept of rail-based ESD Protection. ESD current is redirected to the V_{DD} power rail and then shunted to GND by a power clamp.

Testability

- How to test an SoC?
- Test circuits
  - Probe pads
  - Post fabrication: cut and short?