Noise Analysis of Regenerative Comparators for Reconfigurable ADC Architectures

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***Abstract*—The need for highly integrable and programmable analog-to-digital converters (ADCs) is pushing towards the use of dynamic regenerative comparators to maximize speed, power efficiency and reconfigurability. Comparator thermal noise is, however, a limiting factor for the achievable resolution of several ADC architectures with scaled supply voltages. While mismatch in these comparators can be compensated for by calibration, noise can irreparably hinder performance and is less straightforward to be accounted for at design time. This paper presents a method to estimate the input referred noise in fully dynamic regenerative comparators leveraging a reference architecture. A time-domain analysis is proposed that accounts for the time varying nature of the circuit exploiting some basic results from the solution of stochastic differential equations. The resulting symbolic expressions allow focusing designers' attention on the most influential noise contributors. Analysis results are validated by comparison with electrical simulations and measurement results from two ADC prototypes based on the reference comparator architecture, implemented in 0.18-μm and 90-nm CMOS technologies.**

***Index Terms*—Noise analysis, reconfigurable analog-to-digital converter (ADC), regenerative comparator, stochastic differential equation.**

I. Introduction

ANALOG-TO-DIGITAL converters (ADCs) are being continuously pushed towards their performance limits as technology scales down and system specifications become more challenging. The ultra-low power consumption requirements originating from "wearable computing" appliances and the increasing sampling rates in modern communication systems—among the rest—pose daunting challenges on ADC design. Moreover, the overall complexity is even augmented by reconfigurability requirements, an essential feature to achieve substantial power reductions and comply with multiple standards. To cope with these issues, dynamic comparators have proved very suitable for high-speed and low power ADC implementation [1], [2], since current flows are only present during regeneration and reset, and power consumption can be minimized without sacrificing speed. By exploiting latched comparators without static biasing and pre-amplification, we have recently demonstrated a high-speed low-power flash architecture [3], [4], which allows offset removal through independent threshold setting. The same comparator architecture was also exploited in an extremely low power 9-bit successive approximation ADC [5].

In flash ADCs, reconfigurability of the LSB is heavily affected by the amount of noise inserted by front-end comparators on each reference voltage. The absence of linear analog components, such as preamplifiers, further increases the importance of the dynamic latch noise. A minimum step-size up to 6 times the RMS noise should be theoretically guaranteed to reasonably limit the error probability [6]. The problem can be so important that in [5] comparator noise is also reported as the main source of the more than 1 bit degradation in the effective number of bits (ENOB). This issue is exacerbated by voltage scaling so that comparator noise has to be considered from the very beginning of the design process in these architectures. In fact, comparator noise is a more general issue than pure ADC design. Mixed-signal design in scaled CMOS technologies is increasingly favoring the adoption of compact, power efficient, almost completely "digital" topologies as implementations for analog components (e.g., comparator-based sampled circuits [7]). As a result, traditional "analog" problems, such as thermal noise, become important also for "digital" circuits and should be analyzed in a large signal context.

While noise estimation in strobed comparators with biased pre-amplification is a well understood problem [8], noise analysis for fully dynamic structures is complicated by the different phases of operation and no analytical results are currently available. As a consequence, low-noise comparators are achievable only through empirical considerations and painstaking iterations with the simulator. In this paper, we present a noise analysis technique which provides an accurate yet simple noise model to guide designers when sizing a regenerative comparator, based on the comparator presented in [3]. Compact expressions are computed for the input noise power as a function of circuit capacitances and transistor small-signal parameters. We perform noise analysis in the time domain exploiting some elegant results from stochastic differential equations (SDEs), following the approach used in [9] for noise analysis in sampling mixers, or in [10] for phase noise estimation in ring oscillators. Input referred noise is then computed based on the variation of the comparator output probability as a function of the input voltage. Results are validated with simulations and measurements from a 0.18-μm and a 90-nm

Manuscript received April 3, 2007; revised August 8, 2007. Published July 10, 2008 (Porjected). This work was supported in part by the Italian Research Program PRIN protocol 2005093524_002. This paper was recommended by Associate Editor P. Carbone.

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Digital Object Identifier 10.1109/TCSI.2008.917991

comparator implementations used in the ADCs reported in [3] and [4].

This paper is organized as follows. In Section II we review the necessary analytical tools for noise analysis. Section III briefly illustrates the reference comparator architecture and the comparator noise model used for measurements. Noise analysis and results are then described in Section IV and validated in Section V, where some design examples are presented. Finally, in Section VI some conclusions are drawn.

II. Time-Domain Noise Analysis and SDE

Computing circuit noise in the time domain is a problem analogous to the brownian motion problem, affordable through SDEs [11]. In this section, we review some basic results of stochastic calculus that will be used in the analysis to follow. The circuit in Fig. 1 (a parallel R-C network with a noise current source i) will be used to illustrate results. The generic noise source in Fig. 1 is assumed as white to model thermal noise, with power $E[i^2]$ over a bandwidth Δf and autocorrelation function $E[i(\tau)i(\tau')]$ shown in the same Figure. R is a noiseless resistor whereas R_n is the equivalent noise resistance of i, which for an MOS transistor in saturation would assume the expression

$$R_n = \frac{1}{\gamma g_m} \tag{1}$$

where γ is the noise factor, typically equal to 2/3. The capacitor voltage at $t = 0$ is assumed to be a Gaussian random variable with zero mean and a variance of σ_0^2. The problem we want to address is how to compute the variance of this voltage as a function of time. The system can be captured as a linear SDE whose solution is analogous to that of an ordinary differential equation (ODE). A compact, yet rigorous, derivation of the output noise statistics is reported in Appendix I. The resulting expression for the output noise voltage is

$$v_{Cn}(t) = \frac{\mathrm{e}^{-t/RC}}{C} \int_0^t \mathrm{e}^{\tau/RC} i(\tau)\mathrm{d}\tau + v_{Cn}(0)\mathrm{e}^{-t/RC}. \tag{2}$$

We notice that if i and $v_{Cn}(0)$ are Gaussian processes with zero mean then $v_{Cn}(t)$ is also a Gaussian process with zero mean. The variance of $v_{Cn}(t)$ can be expressed as

$$E\left[v_{Cn}^2(t)\right] = \frac{kTR}{CR_n}(1 - \mathrm{e}^{-2t/RC}) + \sigma_0^2\mathrm{e}^{-2t/RC} \tag{3}$$

which, when R is neglected $(R \to +\infty)$, turns into

$$E\left[v_{Cn}^2(t)\right] = \frac{2kT}{C^2R_n}t + \sigma_0^2. \tag{4}$$

Equation (4) shows that the variance of v_C increases linearly with time. Although (4) does not accurately model a real physical system ($E[v_{Cn}^2(t)]$ diverges as $t \to +\infty$), it provides a reasonable approximation when the time interval in which a circuit is observed is small if compared to the circuit time constant. This is usually the case for clocked circuits in which fast transitions between different phases are determined by "external" conditions (e.g., a clock edge, or the reaching of a threshold). Equations (3) and (4) are the fundamental results from SDE theory that will be exploited in the derivation of the proposed noise model in Section IV. The analysis results shown for the scalar case can be easily extended to multidimensional problems as is the case for systems of ODEs (see Appendix I).

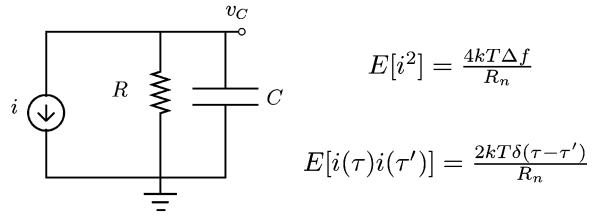

Fig. 1. Simple network for illustration of basic stochastic calculus results.

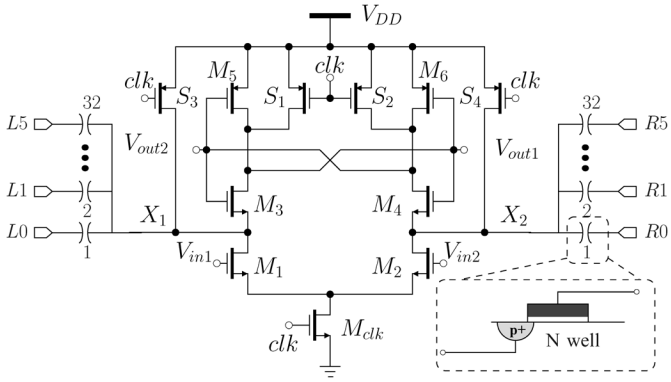

Fig. 2. Regenerative comparator used as a reference for noise analysis. Small MOS capacitances enable threshold calibration.

III. Reference Comparator Architecture

The comparator architecture we exploit for our analysis is shown in Fig. 2 and is based on the structure reported in [1]. The comparator is very suitable to implement fast and power-efficient ADCs, such as in the architecture proposed in [3], as well as sense amplifiers for SRAMs [12].

Comparator noise analysis is very important when high resolution, low-voltage ADCs are required, but it also determines the effectiveness of the calibration schemes exploited to improve linearity and enable reconfigurability, such as the one reported in [13]. The time-varying, strongly nonlinear operation of this circuit makes noise analysis not straightforward if a compact, interpretable relation is sought. As in other periodically time-varying systems, we argue that noise analysis can be remarkably simplified if performed in the time domain, by using the basic results of stochastic calculus summarized in Section II. In this work, emphasis is posed on analytical solutions to provide a deeper insight in the most influential noise sources.

A. Circuit Description

The reference comparator consists of an input differential pair feeding current into a latch composed by two cross-coupled inverters. Current is supplied through transistor M_{clk}. Comparison and reset phases are controlled by the clock signal clk. When clk is low, no current is drawn as M_{clk} is off. The input signal is tracked on the input capacitances of M_1 and M_2

(differentially). The output nodes, as well as the regenerative inverter pair M_3-M_6 are linked to $V_{\rm DD}$ through S_1-S_4. When clk goes high, M_1-M_2 force currents through the inverters M_3-M_5 and M_4-M_6. As i_{D1} and i_{D2} depend on the input signal, the input capacitances of the regenerative inverter pair are discharged with different rates triggering regeneration and latching of the result. After the decision has been taken, no current is drawn in the circuit as either the n or the p transistor will be off in the inverters.

The comparator input offset V_{io} is programmable by exploiting the fact that any load difference $\Delta C = C_{X_1} - C_{X_2}$ at the drains of M_1 and M_2 causes a shift in the trip point given by the following first-order expression:

$$V_{io} = \frac{I_D}{g_{m1}}\frac{\Delta C}{C_X} = \frac{V_{\rm ov1}}{2}\frac{\Delta C}{C_X} \tag{5}$$

where C_X is the load capacitance in the balanced case, I_D, g_{m1} and $V_{\rm ov1}$ are the (average) current, transconductance, and overdrive, respectively, of the input pair in saturation during the initial drain node discharging phase. Binary sized array of MOS capacitors are inserted on both sides of the comparator with the possibility of digitally changing the value of each single capacitance. If the control voltage Rx in Fig. 2 is low, a channel exists and a c_{gs} is inserted on one side. Otherwise, the same parasitic capacitances are only present on both sides. As a result, the comparator can be calibrated both to compensate random mismatch and to configure the comparator threshold.

B. Comparator Noise and Calibration

The calibration procedure consists of digitally inserting capacitances at the drain nodes of the input pair, denoted with X_{1-2} in Fig. 2, so as to set the threshold to zero [13]. To achieve this, the comparator input is shortened and capacitance is repeatedly added until the output toggles between high and low values. Because of comparator noise, however, the calibration algorithm has to "average" measurements to obtain useful information. The input comparator noise RMS value σ_n determines the number of observations that have to be averaged to achieve a given confidence level on threshold estimation, hence deciding how fast the calibration procedure can be.

The digital output of a noisy comparator can be modeled, for a given input, as a *Bernoulli stochastic variable* $\mathcal{B}(1,p)$ giving 0 (i.e., $-V_{\rm DD}$) or 1 (i.e., $V_{\rm DD}$) according to the law

$$v_o = \mathrm{sign}(V_{\rm out2} - V_{\rm out1}) = \frac{1+\mathrm{sign}(v_{din}-v_n)}{2} \tag{6}$$

where v_n is the input noise voltage and $v_{din} = V_{in1} - V_{in2}$. This model assumes that the decision result at each clock cycle is only a function of the comparator threshold and the input and noise signal at the latching instant. This is equivalent to neglecting pathological situations in which correlation between consecutive decisions is present, e.g., due to parasitics creating a feedback between the output and the input nodes. If the input noise v_n is assumed to be a white Gaussian process, then the probability of getting 1 as a function of v_{din} coincides with the comparator output mean and can be easily computed as

$$p(v_{din}) = \mathrm{E}[v_o] = \frac{1}{\sqrt{2\pi}\sigma_n}\int_{-\infty}^{+\infty} v_o \mathrm{e}^{-\frac{v_n^2}{2\sigma_n^2}}\mathrm{d}v_n = \frac{1+\mathrm{erf}\left(\frac{v_{din}}{\sqrt{2}\sigma_n}\right)}{2} \tag{7}$$

where

$$\mathrm{erf}(z) = \frac{2}{\sqrt{\pi}}\int_0^z \mathrm{e}^{-x^2}\mathrm{d}x.$$

With the basic assumptions above, also verified by measurements, the model in (7) has been used to extract the noise sigma from experimental results based on the variation of the output probability as a function of the input voltage [8], as reported in Section V.

IV. Comparator Input Referred Noise

To compute the comparator noise, we assume that the input signal voltage is zero and the circuit has a finite number of *operating phases*, where the circuit is linearized and analyzed. Transitions between phases are assumed instantaneous, thus neglected. Since in each region of operation the comparator noise model can be reduced to simplified equivalent configurations similar to the one discussed in Section II, we can exploit the results presented earlier. The evolution of the output voltage statistics is obtained by solving the equations governing the equivalent circuit in each phase and joining results with continuity so that the starting point of each phase coincides with the final point of the previous one. This method can be similarly extended to characterize noise in other time-varying circuits verifying the assumptions stated above. In the next subsections, we will use the convention $A_{i,j}$ to denote the parameter A_i in phase j.

A. Comparator Operation Phases

The operation phases for noise analysis are derived based on the transitions of some of the transistors in the comparator from one operating region to another. Clear isolation of these phases necessarily produces strong approximations since a rigorous definition of the edges is hard to be provided. However, we can still determine some time intervals in which a certain circuit configuration can be practically "frozen", although small-signal parameters are continuously varying. Three main operating phases can be distinguished, as visualized in Fig. 3 and Fig. 4, representing a typical transient evolution of some circuit voltages and small-signal parameters, respectively.

Phase 1 is defined as the time interval during which the reset switches are turned off and only transistors $M_{\rm clk}$, M_1, and M_2 are on, as captured by the following relations:

$$\begin{cases} clk \geq 0.75V_{\rm DD} \\ v_{X_{1-2}} \geq V_{\rm DD} - V_{Tn3}. \end{cases} \tag{8}$$

The initial instant t_0 is therefore marked as the time in which M_{1-2} start conducting in saturation (first relation in (8)); the final instant t_1 occurs when voltages $v_{X_{1-2}}$ discharge down to $V_{\rm DD} - V_{Tn3}$ thus turning M_3 and M_4 on [second relation in (8)].

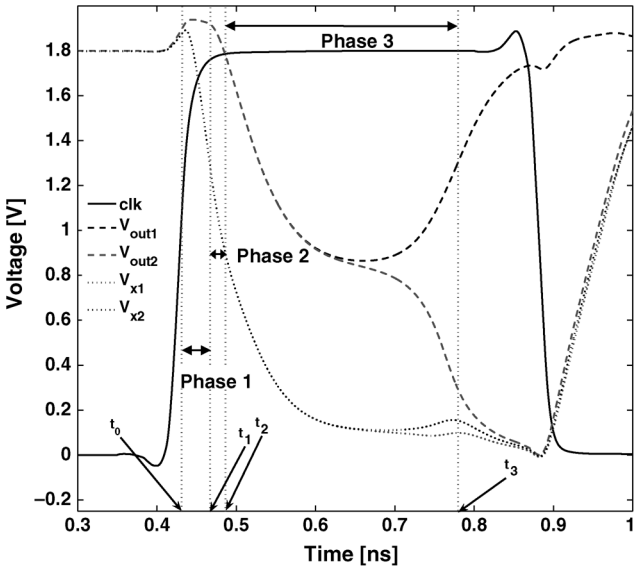

Fig. 3. Large signal transient denotes three basic operating phases: phase 1 (t_0-t_1), phase 2 (t_1-t_2) and phase 3 (t_2-t_3). Different circuit configurations approximate the comparator behavior in each phase.

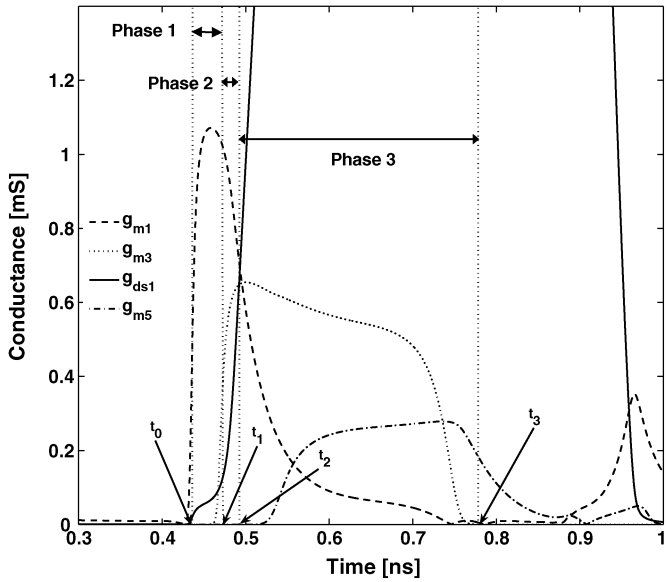

Fig. 4. Typical small-signal parameter evolution with time. The behavior in different operation phases is highlighted.

Overall, the voltage change on nodes X after the first phase is practically equal to

$$\Delta v_{X,1} = v_{X_{1-2}}(t_0) - v_{X_{1-2}}(t_1) \approx V_{Tn3}. \tag{9}$$

Phase 2 is the time interval during which M_{1-4} are all in saturation and can be defined by

$$v_{X_{1,2}} \geq V_{\rm CM} - V_{Tn1} \tag{10}$$

$V_{\rm CM}$ denoting the input common-mode voltage of the comparator. Equation (10) defines the final instant t_2, corresponding to M_{1-2} going out of saturation. When working with small-signal parameters (Fig. 4) it may be more convenient to use the relation $g_{m1} \leq g_{ds1}$ instead of (10) to denote this phase as the time instants defined by the two conditions are very close to each other. Overall, the voltage change on node X in phase 2 will be

$$\begin{aligned}\Delta v_{X,2} &= v_{X_{1-2}}(t_1) - v_{X_{1-2}}(t_2) \\ &= (V_{\rm DD} - V_{Tn3} - V_{\rm CM} + V_{Tn1}) \\ &\approx (V_{\rm DD} - V_{\rm CM})\end{aligned} \tag{11}$$

where V_{Tn1} and V_{Tn3}, threshold voltages of M_1 and M_3, can be considered approximately equal if the bulk effect is neglected.

Phase 3 is finally defined as the time interval during which only the cross-coupled inverters are active since the influence of the input pair can be neglected ($v_{X_{1,2}} \approx 0$). The final instant t_3 can be thought as the end of the exponential regenerative phase of the latch, when some devices in the inverters enter the triode, and then cutoff, regions. This transitions mark the latching state and are indicated, in Fig. 3, by a change of concavity in the $V_{\rm out1}$ and $V_{\rm out2}$ waveforms. We end the noise analysis at t_3 since, after that time, the final decision is practically taken and no additional noise contribution can have a significant impact on it.

Since both noise and signal exhibit the same transient after t_2, we define the input-referred comparator noise as the RMS signal level that generates a transient value at t_3 equal to the output noise standard deviation at the same time. This will provide the input noise RMS value σ_n of the input Gaussian noise v_n, as defined in Section III-B. We note that no mathematical relation is needed to define t_3 since the final input noise expression will be independent of it, as will be shown in Section IV-E. In fact, with the assumptions in our analysis (Section IV-D and Section IV-E), the exponential dependence on t_3 will be present as a multiplying factor in both the output noise variance and the "equivalent signal gain" expressions and will cancel out when noise is referred to the input.

The analysis in each phase is described in the following sections.

B. Noise Analysis in Phase 1

In phase 1 $M_{\rm clk}$ is in its linear region while M_1 and M_2 are in saturation and impose currents to discharge nodes X_{1-2}. In Fig. 5 the equivalent half-circuit for noise analysis is represented. The half-circuit is sufficient to compute the variance of the output *differential* noise voltages v_{dO} and v_{dX}. However, contributions to the noise variance arising from noise sources must be doubled since sources on both sides of the differential circuit are uncorrelated.

The current source power due to M_{1-2} is $E[i_{n1}^2] = 8kT\gamma g_{m1,1}\Delta f$, γ being the MOS noise factor. Since M_{3-6} are off, the output node O follows node X through a capacitive divider made up of the circuit parasitics. C_O denotes the total capacitance on each output node, including the load and parasitics from the devices connected to that node. C_X represents the total capacitance on each X node, made up by the calibration capacitors together with the connected device parasitics and capacitances (e.g., $c_{gd1,1}$ and $c_{db1,1}$ in phase 1). The comparator is assumed to be balanced for noise analysis. All circuit parameters are considered to be constant in this phase or, equivalently, average values can be taken as an approximation. To simplify, we also assume that C_O and C_X have the same values in all the phases for a given circuit, since we

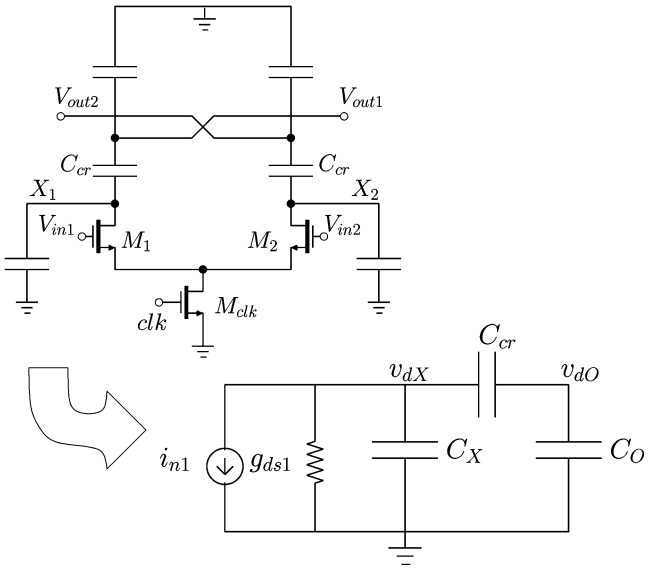

Fig. 5. Equivalent half-circuit for noise analysis in phase 1.

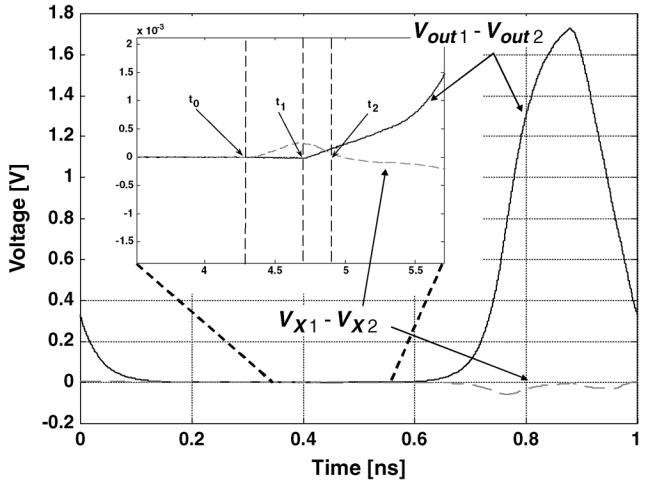

Fig. 6. Differential signal transient behavior: the output difference is zero in phase 1 meaning that negligible coupling is present between v_{dO} and v_{dX}.

observed negligible variations in simulations. C_{cr} models the cross-coupling parasitic capacitance between the output and X nodes, which is also expected to be negligible since all devices between these two nodes are off. This can also be checked from Figs. 3 and 6, where both the output nodes in phase 1 are shown to stay at V_{DD} and their difference sticks to zero, meaning that C_{cr} is practically zero.

The initial condition on the variance of v_{dO} and v_{dX} is provided by noise sampled by the switches at the end of the reset phase. At time $t_0 = 0$, the switch channel noise is sampled on the output capacitance C_O (providing a power contribution equal to $\sigma_O^2 = 2kT/C_O$) and the capacitance C_X at node X (providing a $\sigma_X^2 = 2kT/C_X$ term). Since C_X and C_O have no substantial interaction, only noise from the output reset switches will be present at the output. With $C_{cr} \approx 0$, the circuit becomes similar to the one in Fig. 1. Moreover, by neglecting $g_{ds1,1}$ with respect to the capacitive impedance, noise variance can be assumed to increase linearly as in (4). At t_1, the variance of both

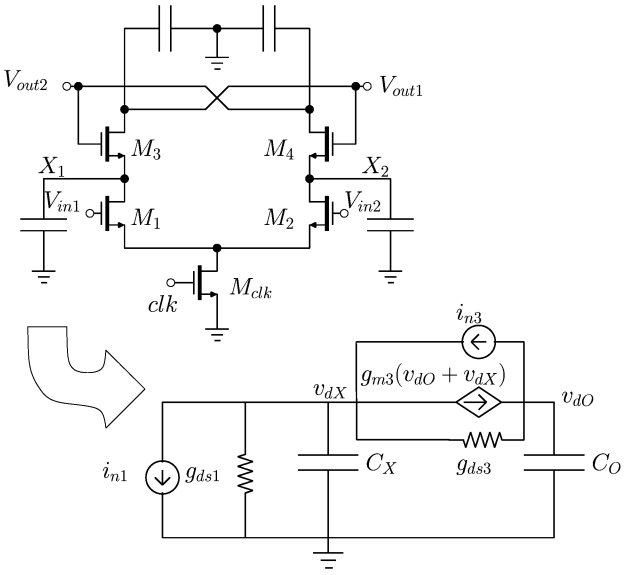

Fig. 7. Equivalent half-circuit for noise analysis in phase 2.

nodes can be finally calculated to reach the following values:

$$E\left[v_{dO}^2(t_1)\right] = \frac{2kT}{C_O} \tag{12}$$

$$E\left[v_{dX}^2(t_1)\right] = \frac{2kT}{C_X} + \frac{4kT\gamma g_{m1,1} t_1}{C_X^2}. \tag{13}$$

C. Noise Analysis in Phase 2

The equivalent circuit in this phase is shown in Fig. 7 where initial conditions are set by phase 1. Being a two pole system, noise analysis would require solving a two-dimensional SDE with initial conditions on both nodes. For brevity, we report here only the final result. The complete analysis is detailed in Appendix II leveraging the time-domain tools in Section II.

A positive feedback starts to operate due to M_{3-4} conduction. Since one of the system poles is

$$p_{2,2} = -\frac{1}{\tau_2} \approx -\frac{g_{m3,2}(C_O - C_X)}{C_X C_O} \tag{14}$$

different behaviors will be observed based on the relationship between C_O and C_X (Appendix II). However, the most meaningful case is when $C_X \approx C_O$ (i.e., $|\tau_2| \to +\infty$) or, equivalently, if the duration of phase 2 is much smaller than the small-signal time constant $|\tau_2|$ (i.e., $|\tau_2| \gg t_2 - t_1$). In this case, a compact approximation can be obtained via second-order Taylor expansion, when $(t_2 - t_1)/|\tau_2| \to 0$. Then, independently of the relationship between C_X and C_O, the different variance expressions converge to the unique formula

$$\begin{aligned} E\left[v_{dO}^2(t_2)\right] = {} & \frac{C_X^2}{(C_O - C_X)^2} \frac{(t_2 - t_1)^2}{\tau_2^2} E\left[v_{dX}^2(t_1)\right] \\ & + \frac{\left(C_O - C_X + C_X \frac{t_2 - t_1}{\tau_2}\right)^2}{(C_O - C_X)^2} E\left[v_{dO}^2(t_1)\right] \\ & + \frac{4kT\gamma g_{m3,2}(t_2 - t_1)}{C_O^2}. \end{aligned} \tag{15}$$

As evident from (15), the first two terms are due to the initial conditions set in phase 1 whereas the last term is due to the M_{3-4} current source power $E[i_{n3}^2] = 8kT\gamma g_{m3,1}\Delta f$ producing a linearly increasing contribution (corresponding to (4)). No noise contribution appears from $i_{n1,2}$ since $i_{n1,2}$ generates only third-order (and higher) terms. Equation (15) has been validated by simulations and will be referred in further computations. In practical situations, phase 2 is indeed quite short, or, equivalently, C_X and C_O are very likely to assume similar values.

D. Noise Analysis in Phase 3

The equivalent circuit in this phase is represented in Fig. 8. Since M_{1-2} are now in the linear region, $g_{ds1,3}$ is much larger than the other conductances in the circuit and contribution of $i_{n1,3}$ becomes negligible. Since nodes X_{1-2} can be practically assumed short circuited to ground, the initial condition on these nodes as well as the related time constant can be neglected. Noise is basically determined by M_{3-4} and M_{5-6}, which also turn on during this phase. Under these hypotheses, (3) can be directly applied to the circuit in Fig. 8 but this time the equivalent resistance seen at the output node is negative and generates a positive exponential behavior. Denoting with t_3 the end of the exponential regeneration region, we have that the integrated noise becomes

$$E\left[v_{dO}^2(t_3)\right] = \frac{2kT\gamma|R_3|(g_{m3,3}+g_{m5,3})}{C_O}\left(\mathrm{e}^{\frac{2(t_3-t_2)}{\tau_3}}-1\right) + E\left[v_{dO}^2(t_2)\right]\mathrm{e}^{\frac{2(t_3-t_2)}{\tau_3}} \quad (16)$$

where the regeneration time constant is given by

$$\tau_3 = |R_3|C_O = \frac{C_O}{g_{m3,3}+g_{m5,3}}. \quad (17)$$

The output integrated noise variance increases exponentially until the decision is taken. Under the hypothesis $\tau_3 \ll (t_3 - t_2)$, and using that the output equivalent resistance R_3 is approximately $-1/(g_{m3,3}+g_{m5,3})$, we can write

$$E\left[v_{dO}^2(t_3)\right] = \left(\frac{2kT\gamma}{C_O} + E\left[v_{dO}^2(t_2)\right]\right)\mathrm{e}^{\frac{2(t_3-t_2)}{\tau_3}}. \quad (18)$$

Finally, by merging (12) and (15) into (18) the total output variance at t_3 can be obtained including contributions from all devices and all phases.

E. Input Referred Noise

In order to refer noise to the input, the global input–output "equivalent gain" is computed considering that a deterministic input signal (initial imbalance) is present during the same circuit phases considered for noise analysis (Fig. 5, Fig. 7 and Fig. 8). Therefore, the same equivalent circuits can be exploited, this time solicited by a constant (RMS) input signal v_{din} thus obtaining, in the various phases

$$v_{dX}(t_1) = -\frac{v_{din}g_{m1,1}t_1}{C_X} \quad v_{dO}(t_1) = 0 \quad (19)$$

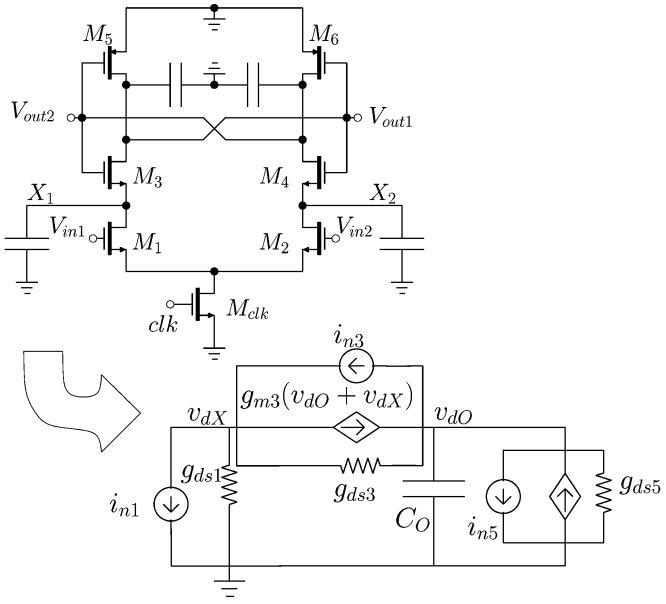

Fig. 8. Equivalent half-circuit for noise analysis in phase 3.

$$v_{dO}(t_2) = \frac{C_X\left(1-\mathrm{e}^{-\frac{t_2-t_1}{\tau_2}}\right)}{C_O-C_X}v_{dX}(t_1) + \frac{g_{m1,2}v_{din}}{C_O-C_X} \times \left[\tau_2\left(1-\mathrm{e}^{-\frac{t_2-t_1}{\tau_2}}\right)-(t_2-t_1)\right] \quad (20)$$

$$v_{dO}(t_3) = v_{dO}(t_2)\mathrm{e}^{\frac{t_3-t_2}{\tau_3}} \quad (21)$$

By merging (19) and (20) with (21) and using the same Taylor approximation as for (15) in phase 2, we get the following compact expression, linking the output voltage to the input signal in the time domain:

$$v_{dO}(t_3) = -v_{din}\frac{g_{m1,1}t_1g_{m3,2}(t_2-t_1)}{C_XC_O}\mathrm{e}^{\frac{t_3-t_2}{\tau_3}}. \quad (22)$$

From (22) a global input–output "equivalent gain" G_{eq} can be directly defined as

$$G_{eq} = -\frac{g_{m1,1}t_1g_{m3,2}(t_2-t_1)}{C_XC_O}\mathrm{e}^{\frac{t_3-t_2}{\tau_3}} \quad (23)$$

and the input referred noise can be finally found by dividing the output noise variance by the square of the "equivalent gain" as

$$\sigma_n^2 = E\left[v_{din}^2\right] = \frac{E\left[v_{dO}^2(t_3)\right]}{G_{eq}^2}. \quad (24)$$

After substituting (18) and (23) into (24), with simple algebra, we can isolate four main noise contributions by grouping together those terms that originate from the same devices in the different phases: the noise from the input pair transistors M_{1-2} during phase 1 and 2; the noise from the inverter transistors M_{3-6} in phase 2 (M_{3-4}) and 3 (M_{5-6}); the noise sampled on the output nodes and on nodes X_{1-2} by the switches S_{1-2} and

S_{3-4}, respectively, at the onset of phase 1. Therefore, the input noise power can be finally expressed as follows:

$$\sigma_n^2 = \sigma_{M_1}^2 + \sigma_{S_1}^2 + \sigma_{M_{3-5}}^2 + \sigma_{S_3}^2. \tag{25}$$

The first term in (25) denotes the contribution of M_{1-2}

$$\sigma_{M_1}^2 = \frac{4kT\gamma}{g_{m1,1}t_1}. \tag{26}$$

The contribution of S_{1-2} (switch noise sampled on C_O) is

$$\sigma_{S_1}^2 = \frac{2kTC_X^2}{g_{m1,1}^2 t_1^2 C_O} + \frac{4kTC_X^2}{g_{m1,1}^2 t_1^2 C_O g_{m3,2}(t_2 - t_1)} + \frac{2kTC_X^2 C_O}{g_{m1,1}^2 t_1^2 g_{m3,2}^2 (t_2 - t_1)^2}. \tag{27}$$

Contributions from M_{3-6} are

$$\sigma_{M_{3-5}}^2 = \frac{4kT\gamma C_X^2}{g_{m1,1}^2 t_1^2 g_{m3,2}(t_2 - t_1)} + \frac{2kT\gamma C_X^2 C_O}{g_{m1,1}^2 t_1^2 g_{m3,2}^2 (t_2 - t_1)^2}. \tag{28}$$

Finally, the effect of noise sampled by switches S_{3-4} on C_X as an initial condition in phase 1 is quantified as

$$\sigma_{S_3}^2 = \frac{2kTC_X}{g_{m1,1}^2 t_1^2}. \tag{29}$$

F. Result Discussion

As detailed in Section V, validation of (26)–(29) was performed by directly extracting MOS small-signal parameters from simulation. In this Section, we rearrange (26)–(29) leveraging a square law model, so that we can gather more insight expressing results in terms of capacitances and overdrive voltages, defined as $V_{\rm ov} = V_{GS} - V_T$. This may limit accuracy but provides more interpretable expressions.

The product $g_{m1,1}\cdot(t_1 - t_0)$ can then be obtained as a function of the X node capacitance and input pair overdrive from the equation

$$\frac{g_{m1,1}V_{\rm ov1,1}}{2} = \frac{C_X \Delta v_{X,1}}{t_1 - t_0} \tag{30}$$

where $\Delta v_{X,1}$ is the voltage change on node X in the first phase as in (9). Analogously, the product $g_{m3,2}\cdot(t_2 - t_1)$ can be written as

$$g_{m3,2}\cdot(t_2 - t_1) = \frac{2I_{D3,2}}{V_{\rm ov3,2}} \cdot C_X \frac{\Delta v_{X,2}}{I_{D1,2} - I_{D3,2}} \tag{31}$$

where $\Delta v_{X,2}$ is the voltage change on node X in the second phase, as in (11). To get more compact expressions, we define two dimensionless factors, $\mathcal{F}$ and $\mathcal{H}$ as follows:

$$\mathcal{F} = \frac{V_{Tn3}}{V_{\rm ov1,1}} \tag{32}$$

$$\mathcal{H} = \frac{V_{\rm DD} - V_{\rm CM}}{V_{\rm ov3,2}} \frac{I_{D3,2}}{I_{D1,2} - I_{D3,2}}. \tag{33}$$

With the approximations (30) and (31) and the definitions in (32) and (33), (26)–(29) can be rewritten as follows:

$$\begin{aligned}
\sigma_{M_1}^2 &= \frac{2kT\gamma}{C_X\mathcal{F}} \\
\sigma_{S_1}^2 &= \frac{kT}{2C_O\mathcal{F}^2} + \frac{kT}{2C_X\mathcal{F}^2\mathcal{H}} + \frac{kTC_O}{8C_X^2\mathcal{F}^2\mathcal{H}^2} \\
\sigma_{M_{3-5}}^2 &= \frac{kT\gamma}{2C_X\mathcal{F}^2\mathcal{H}} + \frac{kT\gamma C_O}{8C_X^2\mathcal{F}^2\mathcal{H}^2} \\
\sigma_{S_3}^2 &= \frac{kT}{2C_X\mathcal{F}^2}.
\end{aligned} \tag{34}$$

From noise expressions in (34) we can draw the conclusion that noise terms have the usual kT/C-form with the addition of some additional factors. Some of noise terms (the ones due to M_{1-2} and S_{3-4}) only depend on C_X and $\mathcal{F}$ while the others depend also on C_O and $\mathcal{H}$. In addition to the obvious strategy of increasing capacitance values or the whole comparator size, the main design guideline is that to lower noise, we should make $\mathcal{F}$ and $\mathcal{H}$ as high as possible. The latter strategy, directly focusing on the most influential parameters, may also result in less power consumption than the first ones.

To increase $\mathcal{F}$ we should size the *input pair* with the minimum possible overdrive voltage. This can be done by:

- increasing the input transistor W/L;
- decreasing the discharging current flowing in phase 1 by acting on $M_{\rm clk}$ size;
- decreasing the input common-mode voltage $V_{\rm CM}$.

We should note that reducing the input pair overdrive also reduces the programmable calibration range, as evident from (5), and this trade-off should be considered as well.

$M_{\rm clk}$ has also a key role in determining the noise level, since it influences the input pair overdrive. To show this, we assume again a square law for the input pair transistors in phase 1. To account for (first-order) bulk effect, the threshold voltage for M_1 and M_3 is described through a first-order model as

$$V_{Tn} = V_{Tn0} + n_0 V_{sb} \tag{35}$$

where V_{Tn0}, the threshold voltage for zero V_{sb}, and n_0 can be extracted from simulations or MOS models. In addition, we assume that, at t_0, $M_{\rm clk}$ immediately enters the linear region and behaves as a resistor equal to $R_{\rm clk} = 1/(\beta_{\rm clk}(V_{\rm DD} - V_{Tn0}))$ where β is defined as $\mu C_{ox} W/L$. The input pair overdrive $V_{\rm ov1,1}$ in (32) can then be computed under these hypotheses, by solving the following system:

$$\begin{cases} I_{D1,1} = \frac{\beta_1}{2} V_{\rm ov1,1}^2 \\ V_{\rm ov1,1} = V_{\rm CM} - V_{Tn0} - 2(1+n_0)R_{\rm clk} I_{D1,1}. \end{cases} \tag{36}$$

If we define

$$\rho = \frac{\beta_1}{\beta_{\rm clk}} = \frac{W_1/L_1}{W_{\rm clk}/L_{\rm clk}} \tag{37}$$

also equal to $W_1/W_{\rm clk}$ for transistors with the same channel length, an analytical expression for $\mathcal{F}$ can be obtained as

$$\mathcal{F} = \frac{2(n_0 V_{\rm DD} + V_{Tn0})\rho}{V_{\rm DD} - V_{Tn0}} \cdot \frac{1}{\left(-1 + \sqrt{\frac{V_{\rm DD} + 4(1+n_0)V_{\rm CM}\rho - V_{Tn0}(1+4(1+n_0)\rho)}{V_{\rm DD} - V_{Tn0}}}\right)}. \tag{38}$$

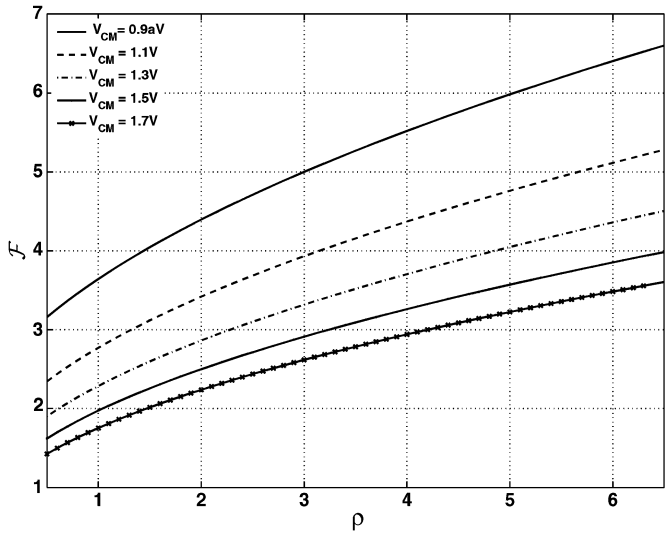

Fig. 9. Behavior of $\mathcal{F}$ as predicted by the analytical model. Increasing $\rho = \beta_1/\beta_{\rm clk}$ will increase $\mathcal{F}$ and then decrease the input noise. The smaller the common mode $V_{\rm CM}$ the larger the effect.

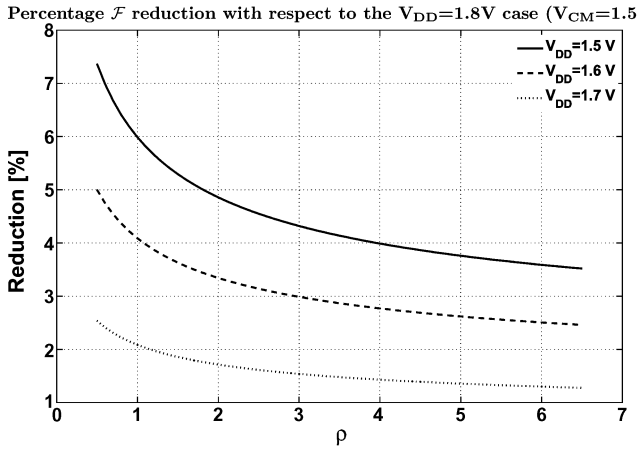

Fig. 10. Sensitivity of the $\mathcal{F}$ factor to supply voltage as predicted by the analytical model. $V_{\rm DD}$ scaling exerts a deleterious effect on input noise since it reduces $\mathcal{F}$. The relative reduction with respect to 1.8 V decreases with increasing $\rho = \beta_1/\beta_{\rm clk}$.

In Fig. 9 the behavior of $\mathcal{F}$ as predicted by this simplified model is shown as a function of ρ for different $V_{\rm CM}$ levels ($V_{\rm DD} = 1.8$ V) using device models from a 0.18-μm comparator design. Fig. 10 represents the impact of $V_{\rm DD}$ scaling on $\mathcal{F}$ by providing the percentage reduction of $\mathcal{F}$ for different levels of $V_{\rm DD}$ with respect to the case $V_{\rm DD} = 1.8$ V. Increasing ρ will increase $\mathcal{F}$ and then decrease the input noise. The smaller the common mode $V_{\rm CM}$ the larger the effect. Conversely, decreasing the supply voltage reduces $\mathcal{F}$ and cause the input noise to increase. The percentage reduction in $\mathcal{F}$ with respect to the 1.8-V case is, however, smaller for larger ρ values.

As evident from (32), bulk effect on M_{3-4}, which are turned on after the first phase, is beneficial for noise since it increases the threshold voltage V_{Tn3} at the numerator. Seemingly a second-order effect, this could produce up to 200 mV increase in V_T from its standard value of 400 mV in a 0.18-μm CMOS technology, as observed in simulations. Finally, $\mathcal{F}$ decreases as

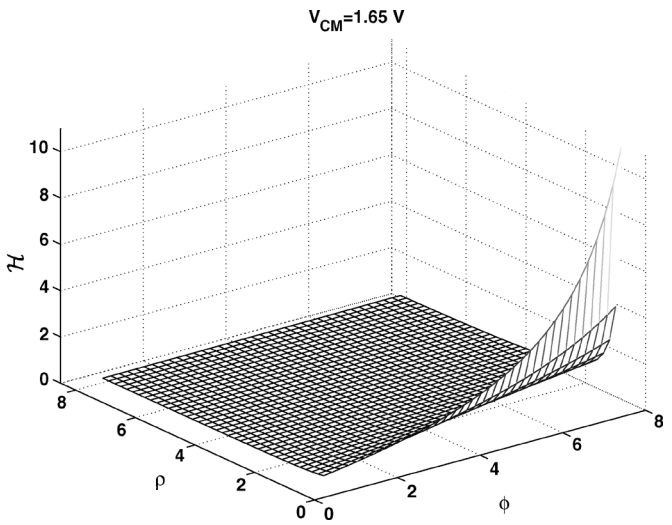

Fig. 11. Behavior of $\mathcal{H}$ as predicted by the analytical model ($V_{\rm DD} = 1.8$ V, $V_{\rm CM} = 1.65$ V). $\mathcal{H}$ increases by increasing ϕ and, less effectively, by decreasing ρ. In practical cases $\mathcal{H}$ is always smaller than 1.

$V_{\rm ov1}$ increases, possibly becoming smaller than 1, which may cause the contribution $\sigma^2_{S_1} + \sigma^2_{M_{3-5}} + \sigma^2_{S_3}$ in (34) to be larger than $\sigma^2_{M_1}$. Unexpectedly, noise estimations solely based on the input pair, quite accurate for continuous time linear circuits, might lead to errors larger than 50% in estimations, as shown in Section V.

Similar considerations may be applied in order to relate $\mathcal{H}$ to the bias point of M_{1-2} and the inverter transistors M_{3-6}. The ratio

$$\phi = \frac{\beta_3}{\beta_{\rm clk}} = \frac{W_3/L_3}{W_{\rm clk}/L_{\rm clk}} \tag{39}$$

can be also defined, but the final expression is not compact. Therefore, we simply report some plots of $\mathcal{H} = \mathrm{f}(\rho, \phi, V_{\rm CM})$ in Figs. 11 and 12. It turns out that $\mathcal{H}$ can be increased by reducing the overdrive of M_{3-4}, or by increasing the current. Therefore, increasing ϕ, decreasing $V_{\rm CM}$ or decreasing ρ are viable solutions for noise reduction. However, the last solution should be avoided since it produces at the same time a decrease in $\mathcal{F}$, with a negative global effect on noise.

Notice that, unless very small values for ρ are used (which is not advisable because of its impact on $\mathcal{F}$) increasing $\mathcal{H}$ is less effective (since only small variations are predicted in most interesting cases) than raising $\mathcal{F}$.

To demonstrate the effectiveness of our analysis we present several comparator sizing examples in which our design guidelines are applied. Starting from the reference design used for the 0.18-μm ADC in [3], in Figs. 13 and 14 we show how noise can be decreased by acting on ρ and ϕ. For instance, input referred noise is halved if W_1 is made 5 times larger than $W_{\rm clk}$ for transistors having the same (minimum) channel length L. Noise is also decreased by acting on ϕ although sensitivity on ϕ is apparently lower. All simulated designs are also compared with predictions from the model. To evaluate our model equations, parameters have been extracted from simulations as detailed in

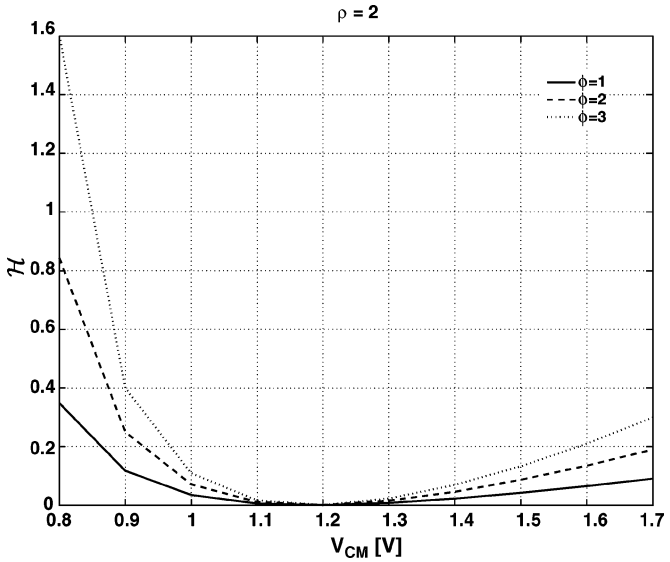

Fig. 12. Behavior of $\mathcal{H}$ as predicted by the analytical model ($V_{\rm DD} = 1.8$ V, $\rho = 2$). $\mathcal{H}$ is higher for lower $V_{\rm CM}$ and has a minimum.

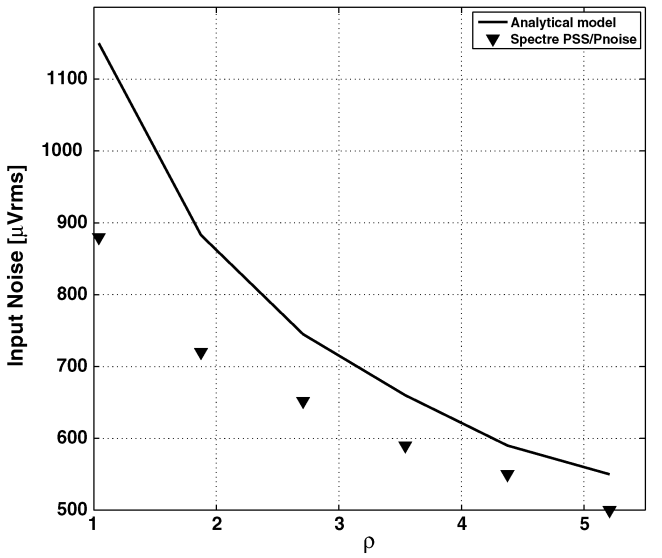

Fig. 13. Input referred noise as a function of ρ ($\phi = 1.33$, $V_{\rm CM} = 1.65$ V). In spite of the heavy approximations in order to obtain compact formulas, the noise behavior is tracked by the analytical model with a maximum 20% over-estimation.

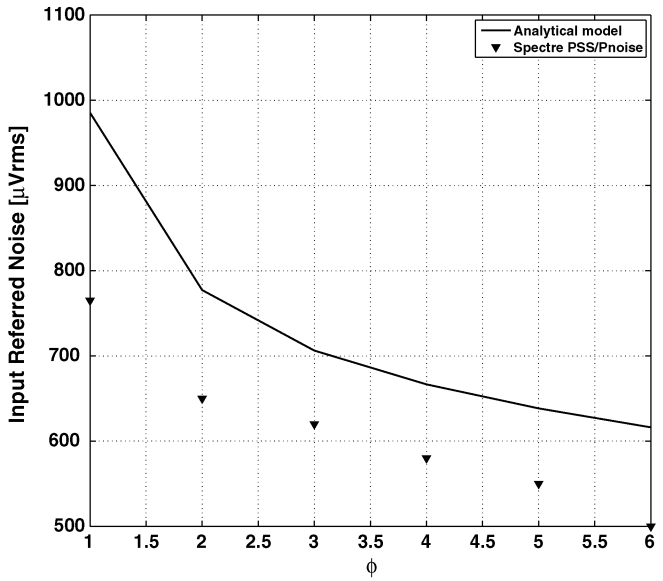

Fig. 14. Input referred noise as a function of ϕ ($\rho = 2.7$, $V_{\rm CM} = 1.65$ V). In spite of the heavy approximations in order to obtain compact formulas, the noise behavior is tracked by the analytical model with a maximum 20% over-estimation.

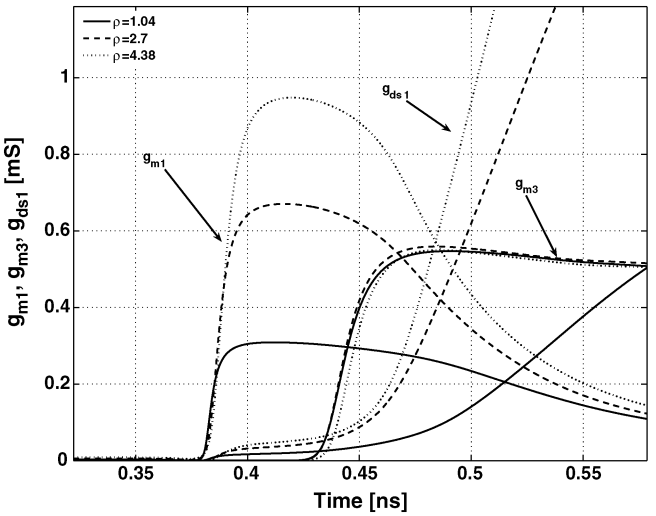

Fig. 15. Effect of ρ on small-signal parameters used for noise analysis.

Section V. The noise behavior is tracked by the analytical model with a maximum 20% over-estimation.

Further insight is gained if the impact of the different design choices on small-signal transistor parameters is analyzed. For this purpose, we express $\mathcal{F}$ and $\mathcal{H}$ in terms of $g_{m1,1}$ and $g_{m3,2}$ by introducing the definitions (32) and (33) into (30) and (31), thus obtaining

$$\mathcal{F} = \frac{g_{m1,1}(t_1 - t_0)}{2C_X} \tag{40}$$

$$\mathcal{H} = \frac{g_{m3,2}(t_2 - t_1)}{2C_X} \tag{41}$$

In Fig. 15 the most important small-signal parameters are represented for a 0.18-μm comparator ($V_{\rm DD} = 1.8$ V, $V_{\rm CM} = 1.65$ V), after simulating three designs corresponding to different ρ values. Fig. 16 visualizes the same parameters for different ϕ values. We observe that by increasing ρ we increase the average value of $g_{m1,1}$ and the input pair transconductance while t_0, t_1 and $g_{m3,2}$ undergo only minor variations (Fig. 15). Moreover, changing ρ also shifts the intersection between g_{m1} and g_{ds1}, hence the instant t_2 in which M_1 exits saturation, thus decreasing the difference $(t_2 - t_1)$ in (41). Overall, this will largely increase $\mathcal{F}$ from (40) and only slightly decrease $\mathcal{H}$ (from (41)) thus having a beneficial effect on noise.

Conversely, increasing ϕ will increase $g_{m3,2}$ as well as the difference $(t_2 - t_1)$, while other parameters undergo minor variations (Fig. 16). Therefore, from (40) and (41) we conclude that increasing ϕ mostly affects $\mathcal{H}$ and is almost orthogonal to $\mathcal{F}$. Figs. 15 and 16 provide an intuitive motivation of the design guidelines in this paper while underlining the most inter-

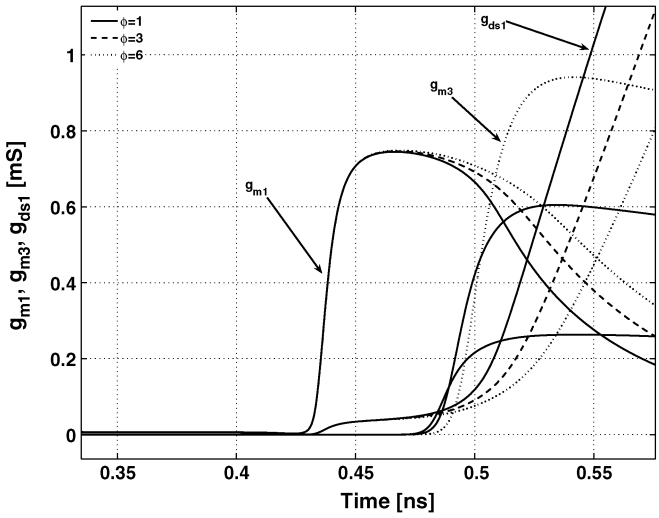

Fig. 16. Effect of ϕ on small-signal parameters used for noise analysis.

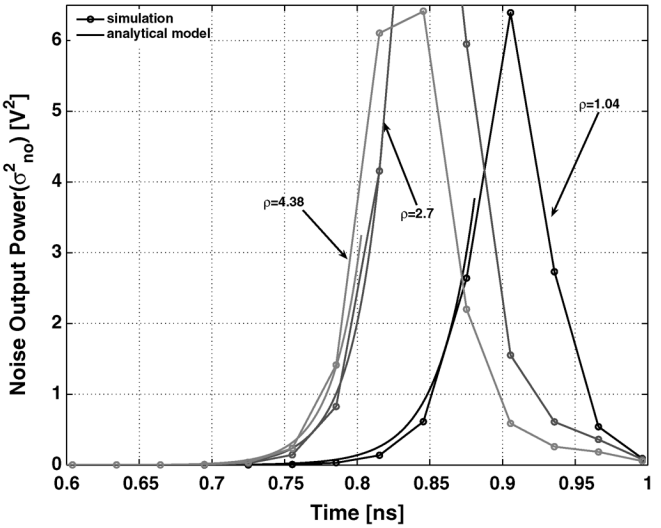

Fig. 17. The piecewise-linear analytical model for the output noise power is able to track the simulated behavior (PSS+Pnoise). Increasing ρ makes the output referred noise higher, but the input referred noise is decreased.

esting parameters (e.g., g_ms and timings) with a higher impact on noise.

V. Analysis Validation and Measurement Results

The presented analysis has been validated with simulations and measurements. We initially compared the output integrated noise as a function of time as computed from (12)–(16) and through simulation using Spectre PSS and Pnoise analyses [14]. To evaluate (12)–(16), device parameters have been extracted from simulations and averaged with respect to time when required since, because of the time varying nature, the circuit is never biased in a traditional sense. A noise factor γ of 2/3 has been selected based on noise simulations of single nMOS and pMOS devices in saturation.

Importantly, an efficient procedure need to be devised to get clean capacitance estimations from simulations, including device parasitics. To estimate capacitance C_X we leverage the large signal waveforms in phase 1 (Fig. 3). In this phase the voltage slope on nodes X_{1-2} can be approximately linked to C_X and the average current I_{D,M_1} flowing in M_{1-2} as follows:

$$\frac{\Delta v_X}{\Delta t} = \frac{I_{D,M_1}}{C_X}. \tag{42}$$

By extracting the slope and I_{D,M_1} from simulations, C_X can then be found from (42). Conversely, to estimate C_O we use the regenerative behavior in phase 3. By evaluating τ_3, $g_{m3,3}$ and $g_{m5,3}$ from simulations, C_O can then be easily derived from (17) (Section IV-D). Finally, time instants t_0-t_3 have been evaluated according to definitions in Section IV-A.

Although relative errors on the output noise may be as high as 50%, the piecewise-linear approximation we have proposed tracks the behavior of the output noise power, as shown in Fig. 17. The high relative errors, especially in phase 3, are mainly due to a nonlinear time-varying circuit nature, which is not completely captured by a first-order model using a constant (averaged) τ_3 in analytical formulas. In fact, the small-signal time constant, and hence the slope of the exponential curve, is a function of the devices that are active at every instant. However, being independent of τ_3, the input referred noise expression is much less sensitive to this error source. As shown in Fig. 13 and Fig. 14, the maximum error in the input noise becomes less than 20%.

To probe further, in Fig. 18 we report the relative importance of the various contributions in determining the output noise power for a reference comparator design in 0.18 μm, as predicted by the analytical model. The conclusion is that at least two sources must be taken into account to avoid underestimations in this case, i.e., the input pair and the noise sampled from the switches on C_O after the reset phase. However, as implied by Fig. 11 and (34), for very small values of ϕ (e.g., $\phi \ll 1$), $\mathcal{H}$ might also assume such a small value that the inverters contribution increases in importance and even exceeds the input pair contribution, which is only dependent on $\mathcal{F}$. In Tables I and II, the relative contributions in percentages are compared with simulations for different values of ρ and ϕ, respectively. When sweeping ϕ, both pMOS and nMOS transistors in the cross-coupled inverters have been properly scaled. Our analytical model is indeed able to correctly weigh the various components for different circuit configurations. Noticeably, a standard transient simulation is all that we need to find the noise level and the main contributors, which was not straightforward without our analysis.

As a final verification step, we compared both simulation and analytical results with noise measurements. We measured comparators from our reference flash ADC designs fabricated in both 180-nm 1.8-V and 90-nm 1.2-V digital CMOS processes. Comparator test structures were also placed on chip, as shown in Fig. 19, for testing and characterization purpose. The ADC were nominally calibrated for a 200 mV input dynamic range ($\mathrm{LSB} = 12.5\ \mathrm{mV}$), and an input common-mode voltage V_{CM} of 1.65 V (in 180 nm) and 1.1 V (in 90 nm). With the same input common mode we measured the input noise sigma by acquiring and averaging the comparator output solicited by an input ramp across the decision window (Fig. 20). The averaged output represents the probability of getting "output high" as a function of

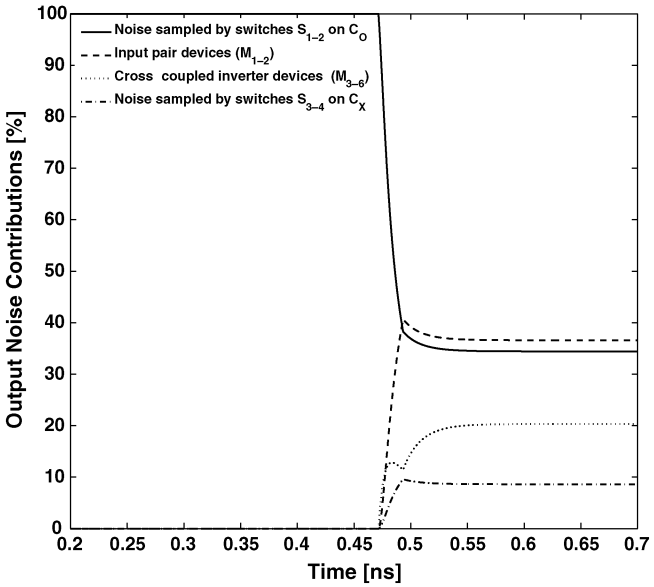

Fig. 18. Contributions of the different components on the output noise power for a reference design ($\rho = 2.5/1.2, \phi = 1.6/1.2, V_{\rm CM} = 1.65$ V, 0.18-μm 1.8-V, $C_X \approx 11$ fF, $C_O \approx 14$ fF) as predicted by the analytical model. Together with the input pair transistors, noise sampled on the output capacitance has also a key role in determining the output noise power.

TABLE I
PREDICTED AND SIMULATED CONTRIBUTIONS TO THE OUTPUT NOISE POWER AS A FUNCTION OF ρ

	Sim.	Mod.	Sim.	Mod.	Sim.	Mod.
ρ	1.04	1.04	2.08	2.08	5.2	5.2
ϕ	1.33	1.33	1.33	1.33	1.33	1.33
M_{1-2}	50.5%	45.4%	41%	41%	52.6%	55%
S_{1-2}	28.6%	24.9%	35%	32%	28.6%	23.8%
M_{3-6}	9.7%	9.7%	18.2%	19%	14.5%	12.7%
S_{3-4}	11.2%	20%	5.8%	8%	4.3%	8.5%

TABLE II
PREDICTED AND SIMULATED CONTRIBUTIONS TO THE OUTPUT NOISE POWER AS A FUNCTION OF ϕ

	Sim.	Mod.	Sim.	Mod.	Sim.	Mod.
ρ	2.7	2.7	2.7	2.7	2.7	2.7
ϕ	1	1	2	2	6	6
M_{1-2}	39%	31.3%	49.5%	47.6%	55.7%	63.4%
S_{1-2}	36%	39.7%	30.3%	28.4%	27.7%	16.5%
M_{3-6}	20.5%	22.4%	14.7%	14%	11%	13%
S_{3-4}	4.5%	6.6%	5.5%	10%	5.6%	7.1%

the input voltage, as explained in Section III-B. The less noise is present in the circuit, the narrower the transition region is between the high and low probability zones, so that the spreading of the obtained function can be used in estimation. We exploited (7) to directly fit σ_n from available measurements for $p(v_{din})$, as shown in Fig. 21 (see also [8], [15]).

Results and comparison are reported in Table III and demonstrate that our analysis achieves estimations very close to both simulation and measurements. Early noise estimation allowed flexible ADC design for reconfigurable input dynamic range. For instance, calibration for an input range as low as 100 mV was feasible still guaranteeing, in theory, a very low output error probability due to noise [6].

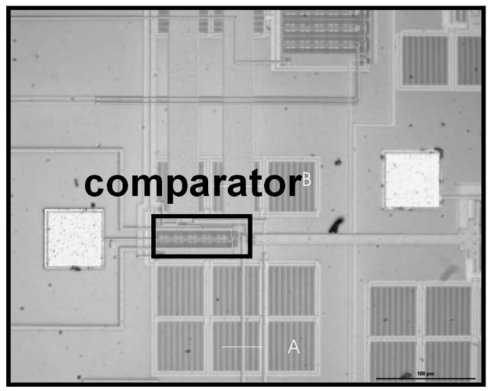

Fig. 19. A comparator test structure photograph on the ADC chip.

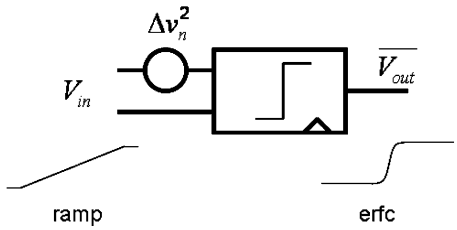

Fig. 20. Measurement setup for noise variance estimation.

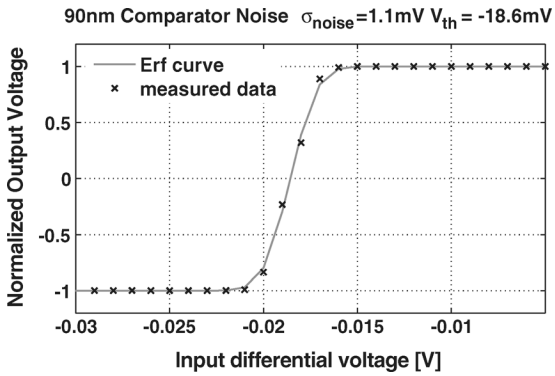

Fig. 21. Fitting of σ_n from experimental data.

TABLE III
COMPARISON BETWEEN PREDICTED, SIMULATED AND MEASURED INPUT NOISE σ

Design	σ_{eqn}	σ_{sim}	σ_{fit}
0.18μm	0.93mV	0.8mV	1.2mV
90nm	1.18mV	1mV	1.1mV

VI. CONCLUSION

Comparator noise characterization in converter design has become a key factor to figure out and select architectures that offer moderate resolutions at low voltage operation and increased input range reconfigurability. This paper presented a first attempt to develop an analytical noise model for a regenerative comparator, which allows designers to have an accurate functional dependency between circuit parameters and comparator noise. The basic analytical tools, exploiting simple results of stochastic calculus, are also described to enable extension of our methodology to similar comparator topologies used in today's designs. Our approach allows capturing major

effects with simple expressions involving only a few terms. Therefore, results yield insight into the principal mechanisms, and give a meaningful strategy for design optimization. They have been finally validated with simulations and the silicon implementation of high speed and low power ADCs based on the comparator analyzed here.

APPENDIX I
BACKGROUND ON SDE

To make this paper as self-contained as possible we provide here some useful concepts on stochastic differential calculus in order to give some background for (3) and (4). A *stochastic differential equation* (SDE) is a problem formally expressed (in one dimension) as follows:

$$\begin{cases} \mathrm{d}X = b(X,t)\mathrm{d}t + B(X,t)\mathrm{d}W \\ X(0) = X_0 \end{cases} \tag{43}$$

where $X(t)$ is the state of a system for $t \geq 0$, b and B are generic functions of t and X, and W is a *Wiener Process* or *Brownian Motion*, i.e., the integral of a white noise process $\xi(t)$ [11]. Since white noise is not a physical process (because of its infinite power), its integral is generally defined to treat with it rigorously, so that $\mathrm{d}W$ is formally equivalent to $\xi \mathrm{d}t$. A Wiener process has a continuous sample path and independent Gaussian increments, and can be approximated by physical processes. An SDE is said to be *linear* if

$$\begin{aligned} b(X,t) &\triangleq C(t) + D(t)X \\ B(X,t) &\triangleq H(t) + F(t)X \end{aligned} \tag{44}$$

and, in case $F \equiv 0$ it is *linear in the narrow sense*. Moreover, if b is homogeneous (i.e., $C(t) \equiv 0$) and $D(t)$, $H(t)$ are constant, the equation has an even more simplified form, also known as *Langevin's equation*

$$\begin{cases} \mathrm{d}X = DX\mathrm{d}t + H\mathrm{d}W \\ X(0) = X_0. \end{cases} \tag{45}$$

If we suppose to formally integrate the SDE in (43), the right-hand side consists of two types of integrals. The integral with respect to time, defined for each sample path, is straightforward. The integral with respect to a Wiener process W is more problematic since sample paths of a Wiener process have unbounded variation (or infinite length). This can be solved by resorting to the stochastic integral in Ito's sense. However, when SDE are linear in the narrow sense, they can be *formally* solved as an ODE. The problems tackled in this paper belong to the last category, as is typical for linearized circuits with constant parameters (capacitances, conductances, transconductances,...).

A. Solution of Linear SDE in the Narrow Sense

The solution of linear SDEs in the narrow sense follows formally from standard formulas in ODE theory if we write $HdW = H\xi dt$, ξ denoting white noise, and regard $H\xi$ as an inhomogeneous term driving the ODE

$$\dot{X} = C(t) + D(t)X + H(t)\xi.$$

The equivalent ODE provides the deterministic trajectory of the system while the random term represents the noisy perturbations of this trajectory. In particular, solution for (45) can be expressed as

$$X(t) = \mathrm{e}^{Dt}X_0 + H\int_0^t \mathrm{e}^{D(t-\tau)}\mathrm{d}W \quad (t \geq 0). \tag{46}$$

Using (46), the Wiener process properties and the definition of Ito's integral [11], we conclude that $X(t)$ is Gaussian if X_0 is also Gaussian.

Stochastic integrals have a number of properties. We here list two of them useful to derive $E[X]$ and $E[X^2]$. For an arbitrary real-valued progressively measurable stochastic process G such that

$$E\left[\int_0^t G^2\mathrm{d}\tau\right] < +\infty$$

we have

$$E\left[\int_0^t G\mathrm{d}W\right] = 0 \tag{47}$$

$$E\left[\left(\int_0^t G\mathrm{d}W\right)^2\right] = E\left[\left(\int_0^t G^2\mathrm{d}\tau\right)\right]. \tag{48}$$

A rigorous definition of progressively measurable stochastic processes is out of the scope of this work. The interested readers can refer to [11]. To simplify, this hypothesis basically refers to the fact that, at each moment of time, G depends only upon the past history of the Brownian motion, and is generally verified in our systems.

Principal statistics of $X(t)$ can be rigorously computed by applying properties in (47) and (48) to (46)

$$\begin{aligned} E[X(t)] &= \mathrm{e}^{Dt}E[X_0] + H\mathrm{e}^{Dt}E\left[\int_0^t \mathrm{e}^{-D\tau}\mathrm{d}W\right] \\ &= \mathrm{e}^{Dt}E[X_0] \end{aligned} \tag{49}$$

$$\begin{aligned} E\left[X^2(t)\right] &= E\left[\mathrm{e}^{2Dt}X_0^2 + 2H\mathrm{e}^{Dt}X_0\left(\int_0^t \mathrm{e}^{D(t-\tau)}\mathrm{d}W\right)\right. \\ &\qquad \left. + H^2\left(\int_0^t \mathrm{e}^{D(t-\tau)}\mathrm{d}W\right)^2\right] \\ &= \mathrm{e}^{2Dt}E\left[X_0^2\right] + 2H\mathrm{e}^{Dt}E[X_0]E\left[\int_0^t \mathrm{e}^{D(t-\tau)}\mathrm{d}W\right] \\ &\quad + H^2\int_0^t \mathrm{e}^{2D(t-\tau)}\mathrm{d}\tau \\ &= E\left[X_0^2\right]\mathrm{e}^{2Dt} + \frac{H^2}{2D}(\mathrm{e}^{2Dt} - 1). \end{aligned} \tag{50}$$

From (49) we conclude that if X_0 has zero mean, $X(t)$ will also have zero mean. Consequently, the fluctuation properties of X are completely conveyed by its variance simply computed as $E[X(t)^2]$ for a zero mean process, as in this paper.

B. Higher Order SDE

When more complex circuits (with more than one pole) have to be analyzed, then a multidimensional extension of the proposed solution is needed. This is, however, smooth under some assumptions generally verified in most practical situations. In particular, a multi-dimensional SDE can be expressed as

$$\begin{cases} \mathrm{d}\mathbf{X} = \mathbf{b}(\mathbf{X},t)\mathrm{d}t + \mathbf{B}(\mathbf{X},t)\mathrm{d}\mathbf{W} \\ \mathbf{X}(0) = \mathbf{X_0} \end{cases} \tag{51}$$

where $\mathbf{X}$ is an n-dimensional state vector, $\mathbf{W}$ is a m-dimensional Wiener process, made up by a vector of m one-dimensional Wiener processes, $\mathbf{b} \in \mathbb{R}^n$ and $\mathbf{B} \in \mathbb{R}^{m\times n}$. Analogously, linear SDE can be defined as well as Langevin's SDE, the solution of which is

$$\mathbf{X}(t) = \mathrm{e}^{\mathbf{D}t}\mathbf{X_0} + \mathbf{H}\int_0^t \mathrm{e}^{\mathbf{D}(t-\tau)}\mathrm{d}\mathbf{W} \quad (t \geq 0). \tag{52}$$

Again, starting from (52), for each state variable in $\mathbf{X}$ the mean and the variance can be found by applying the results found in (48)–(50).

Appendix II
Derivation of the Output Noise Power in Phase 2

Noise calculations in phase 2 are less straightforward than in the other phases, since (2) and (3) cannot be immediately applied. We refer to the small-signal half-circuit in Fig. 7. Dealing with a 2 pole system we need to set up and solve a linear system of two SDE as discussed in Appendix I. Based on KCL on both nodes, the following multi-dimensional equation need to be solved

$$\mathrm{d}\mathbf{X} = \mathbf{D}\mathbf{X}\mathrm{d}t + \mathbf{H}\mathrm{d}\mathbf{W} \tag{53}$$

$$\mathbf{D} = \begin{bmatrix} -\frac{g_{m3,2}}{C_X} & -\frac{g_{m3,2}}{C_X} \\ \frac{g_{m3,2}}{C_O} & \frac{g_{m3,2}}{C_O} \end{bmatrix} \quad \mathbf{H} = \begin{bmatrix} -\frac{1}{C_X} & \frac{1}{C_X} \\ 0 & -\frac{1}{C_O} \end{bmatrix} \tag{54}$$

where $\mathbf{X} = [v_{dX}\ v_{dO}]^T$, $\mathrm{d}\mathbf{W} = [i_{n1,2}\ i_{n3,2}]^T\mathrm{d}t$, $g_{ds1,2}$ and $g_{ds3,2}$ have been neglected. The initial condition vector is $\mathbf{X_0} = [v_{dX}(t_1)\ v_{dO}(t_1)]^T$, T denoting the transpose operation. As in an ODE, the system behavior is determined by the two eigenvalues of $\mathbf{D}$, i.e., the system poles

$$p_{1,2} = 0 \quad p_{2,2} = -\frac{1}{\tau_2} = -\frac{g_{m3,2}(C_O - C_X)}{C_X C_O}. \tag{55}$$

Different behaviors are then observed based on the relationship between C_O and C_X. If $C_O > C_X$ the system is stable and no regeneration starts (negative pole). If $C_O < C_X$ a pole in the right half-plane is present and regeneration starts. If $C_X = C_O = C$ both poles are in 0.

Focusing on v_{dO} (similar considerations can be done for v_{dX}), when $C_X \neq C_O$, (53) leads to the following result valid in both cases of positive and negative pole:

$$\begin{aligned} v_{dO} = {} & \frac{C_X\left(1-\mathrm{e}^{-\frac{t-t_1}{\tau_2}}\right)}{C_O - C_X} v_{dX}(t_1) + \frac{\left(C_O - C_X\mathrm{e}^{-\frac{t-t_1}{\tau_2}}\right)}{C_O - C_X} v_{dO}(t_1) \\ & - \frac{\mathrm{e}^{-\frac{t-t_1}{\tau_2}}}{C_O}\int_{t_1}^{t} \mathrm{e}^{\frac{\tau}{\tau_2}} i_{n3,2}(\tau)\mathrm{d}\tau \\ & + \frac{1}{C_O - C_X}\int_{t_1}^{t}\left(\mathrm{e}^{-\frac{t-t_1-\tau}{\tau_2}} - 1\right) i_{n1,2}(\tau)\mathrm{d}\tau. \end{aligned} \tag{56}$$

Conversely, when $C_X = C_O = C$ the behavior is then described by

$$\begin{aligned} v_{dO} = {} & \frac{g_{m3,2}(t-t_1)}{C} v_{dX}(t_1) + \left(1 + \frac{g_{m3,2}(t-t_1)}{C}\right) v_{dO}(t_1) \\ & - \frac{1}{C}\int_{t_1}^{t} i_{n3,2}(\tau)\mathrm{d}\tau - \frac{g_{m3,2}}{C^2}\int_{t_1}^{t}(t - t_1 - \tau) i_{n1,2}(\tau)\mathrm{d}\tau. \end{aligned} \tag{57}$$

To compute noise power, we exploit the fact that random variables $v_{dX}(t_1)$, $v_{dO}(t_1)$ and random processes $i_{n1,2}$ and $i_{n3,2}$ are all uncorrelated, thus generating contributions that can be summed. No correlation between initial conditions on nodes X and O need to be considered since cross-coupling in phase 1 is negligible. By applying the property (48) of stochastic integrals in Appendix I the output variance can be found for the different possible combinations of C_X and C_O based on comparator sizings and loads. As an example, the variance computed at time t_2 from (56) can be seen in (58)

$$\begin{aligned} E\left[v_{dO}^2(t_2)\right] = {} & \frac{C_X^2\left(1 - \mathrm{e}^{-\frac{t_2-t_1}{\tau_2}}\right)^2}{(C_O - C_X)^2} E\left[v_{dX}^2(t_1)\right] \\ & + \frac{\left(C_O - C_X\mathrm{e}^{-\frac{t_2-t_1}{\tau_2}}\right)^2}{(C_O - C_X)^2} E\left[v_{dO}^2(t_1)\right] \\ & + \frac{2kT\gamma C_X\left(1 - \mathrm{e}^{-\frac{2(t_2-t_1)}{\tau_2}}\right)}{C_O(C_O - C_X)} \\ & + \frac{4kT\gamma g_{m1,2}(t_2 - t_1)}{(C_O - C_X)^2} + \frac{2kT\gamma C_X C_O g_{m1,2}}{(C_O - C_X)^3 g_{m3,2}} \\ & \times \left(4\mathrm{e}^{-\frac{t_2-t_1}{\tau_2}} - \mathrm{e}^{-2\frac{t_2-t_1}{\tau_2}} - 3\right). \end{aligned} \tag{58}$$

However, since in typical circuits phase 2 is quite short or C_X and C_O are very similar in values, (15) in Section IV-C can be practically used. This can be obtained for instance from (58) through second-order Taylor expansion when $(t_2 - t_1)/|\tau_2| \to 0$. It can be easily verified that the final result is also independent of the relationship between C_X and C_O.

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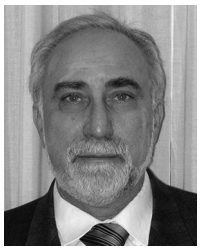

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