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# 14

## Bipolar Junction Transistor (BJT) Circuits

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### 14.1 Introduction

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The *bipolar junction transistor* (or BJT) was the workhorse of the electronics industry from the 1950s through the 1990s. This device was responsible for enabling the computer age as well as the modern era of communications. Although early systems that demonstrated the feasibility of electronic computers used the vacuum tube, the element was too unreliable for dependable, long-lasting computers. The invention of the BJT in 1947<sup>1</sup> and the rapid improvement in this device led to the development of highly reliable electronic computers and modern communication systems.

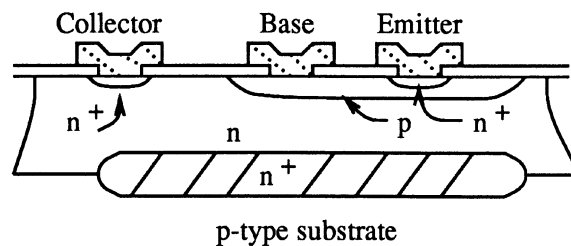
Integrated circuits, based on the BJT, became commercially available in the mid-1960s and further improved the dependability of the computer and other electronic systems while reducing the size and cost of the overall system. Ultimately, the microprocessor chip was developed in the early 1970s and the age of small, capable, personal computers was ushered in. While the metal-oxide-semiconductor (or MOS) device is now more prominent than the BJT in the personal computer arena, the BJT is still important in larger high-speed computers. This device also continues to be important in communication systems and power control systems.

Because of the continued improvement in BJT performance and the development of the heterojunction BJT, this device remains very important in the electronics field, even as the MOS device becomes more significant.

## 14.2 Physical Characteristics and Properties of the BJT

Although present BJT technology is used to make both discrete component devices as well as integrated circuit chips, the basic construction techniques are similar in both cases, with primary differences arising in size and packaging. The following description is provided for the BJT constructed as integrated circuit devices on a silicon substrate. These devices are referred to as “junction-isolated” devices.

The cross-sectional view of a BJT is shown in [Fig. 14.1](#).<sup>2</sup>



**FIGURE 14.1** An integrated npn BJT.

This device can occupy a surface area of less than  $1000 \mu\text{m}^2$ . There are three physical regions comprising the BJT. These are the emitter, the base, and the collector. The thickness of the base region between emitter and collector can be a small fraction of a micron, while the overall vertical dimension of a device may be a few microns.

Thousands of such devices can be fabricated within a silicon wafer. They may be interconnected on the wafer using metal deposition techniques to form a system such as a microprocessor chip or they may be separated into thousands of individual BJTs, each mounted in its own case. The photolithographic methods that make it possible to simultaneously construct thousands of BJTs have led to continually decreasing size and cost of the BJT.

Electronic devices, such as the BJT, are governed by current–voltage relationships that are typically nonlinear and rather complex. In general, it is difficult to analyze devices that obey nonlinear equations, much less develop design methods for circuits that include these devices. The basic concept of modeling an electronic device is to replace the device in the circuit with linear components that approximate the voltage–current characteristics of the device. A model can then be defined as a collection of simple components or elements used to represent a more complex electronic device. Once the device is replaced in the circuit by the model, well-known circuit analysis methods can be applied.

There are generally several different models for a given device. One may be more accurate than others, another may be simpler than others, another may model the dc voltage–current characteristics of the device, while still another may model the ac characteristics of the device.

Models are developed to be used for manual analysis or to be used by a computer. In general, the models for manual analysis are simpler and less accurate, while the computer models are more complex and more accurate. Essentially, all models for manual analysis and most models for the computer include only linear elements. Nonlinear elements are included in some computer models, but increase the computation times involved in circuit simulation over the times in simulation of linear models.

## 14.3 Basic Operation of the BJT

In order to understand the origin of the elements used to model the BJT, we will discuss a simplified version of the device as shown in Fig. 14.2. The device shown is an npn device that consists of a p-doped material interfacing on opposite sides to n-doped material. A pnp device can be created using an n-doped central region with p-doped interfacing regions. Since the npn type of BJT is more popular in present construction processes, the following discussion will center on this device.

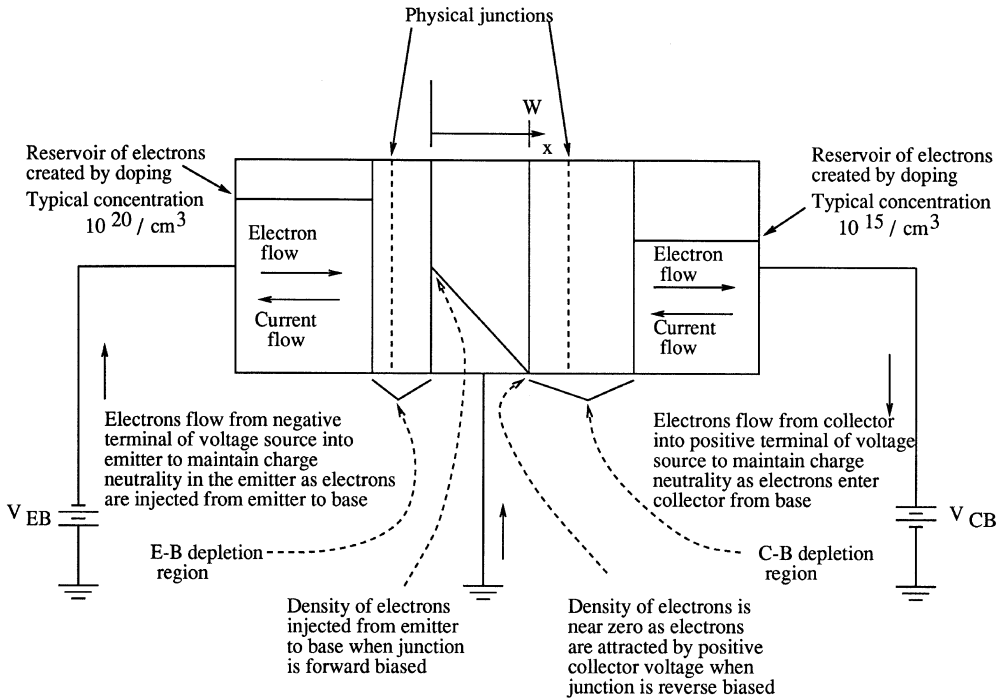


FIGURE 14.2 Distribution of electrons in the active region.

The geometry of the device implied in Fig. 14.2 is physically more like the earlier alloy transistor. This geometry is also capable of modeling the modern BJT (Fig. 14.1) as the theory applies almost equally well to both geometries. Normally, some sort of load would appear in either the collector or emitter circuit; however, this is not important to the initial discussion of BJT operation.

The circuit of Fig. 14.2 is in the active region, that is, the emitter–base junction is forward-biased, while the collector–base junction is reverse-biased. The current flow is controlled by the profile of electrons in the p-type base region. It is proportional to the slope or gradient of the free electron density in the base region. The well-known diffusion equation can be expressed as<sup>3</sup>:

$$I = qD_n A \frac{dn}{dx} = -\frac{qD_n A n(0)}{W} \quad (14.1)$$

where  $q$  is the electronic charge,  $D_n$  is the diffusion constant for electrons,  $A$  is the cross-sectional area of the base region,  $W$  is the width or thickness of the base region, and  $n(0)$  is the density of electrons at the left edge of the base region. The negative sign reflects the fact that conventional current flow is opposite to the flow of the electrons.

The concentration of electrons at the left edge of the base region is given by:

$$n(0) = n_{bo} e^{qV_{BE}/kT} \quad (14.2)$$

where  $q$  is the charge on an electron,  $k$  is Boltzmann's constant,  $T$  is the absolute temperature, and  $n_{bo}$  is the equilibrium concentration of electrons in the base region. While  $n_{bo}$  is a small number,  $n(0)$  can be large for values of applied base to emitter voltages of 0.6 to 0.7 V. At room temperature, this equation can be written as:

$$n(0) = n_{bo} e^{V_{BE}/0.026} \quad (14.3)$$

In Fig. 14.2, the voltage  $V_{EB} = -V_{BE}$ .

A component of hole current also flows across the base–emitter junction from base to emitter. This component is rendered negligible compared to the electron component by doping the emitter region much more heavily than the base region.

As the concentration of electrons at the left edge of the base region increases, the gradient increases and the current flow across the base region increases. The density of electrons at  $x = 0$  can be controlled by the voltage applied from emitter to base. Thus, this voltage controls the current flowing through the base region. In fact, the density of electrons varies exponentially with the applied voltage from emitter to base, resulting in an exponential variation of current with voltage.

The reservoir of electrons in the emitter region is unaffected by the applied emitter-to-base voltage as this voltage drops across the emitter–base depletion region. This applied voltage lowers the junction voltage as it opposes the built-in barrier voltage of the junction. This leads to the increase in electrons flowing from emitter to base.

The electrons injected into the base region represent electrons that were originally in the emitter. As these electrons leave the emitter, they are replaced by electrons from the voltage source,  $V_{EB}$ . This current is called emitter current and its value is determined by the voltage applied to the junction. Of course, conventional current flows in the opposite direction to the electron flow.

The emitter electrons flow through the emitter, across the emitter–base depletion region, and into the base region. These electrons continue across the base region, across the collector–base depletion region, and through the collector. If no electrons were “lost” in the base region and if the hole flow from base to emitter were negligible, the current flow through the emitter would equal that through the collector. Unfortunately, there is some recombination of carriers in the base region. When electrons are injected into the base region from the emitter, space charge neutrality is upset, pulling holes into the base region from the base terminal. These holes restore space charge neutrality if they take on the same density throughout the base as the electrons. Some of these holes recombine with the free electrons in the base and the net flow of recombined holes into the base region leads to a small, but finite, value of base current. The electrons that recombine in the base region reduce the total electron flow to the collector. Because the base region is very narrow, only a small percentage of electrons traversing the base region recombine and the emitter current is reduced by a small percentage as it becomes collector current.

In a typical low-power BJT, the collector current might be  $0.995I_E$ . The current gain from emitter to collector,  $I_C/I_E$ , is called  $\alpha$  and is a function of the construction process for the BJT. Using Kirchhoff's current law, the base current is found to equal the emitter current minus the collector current. This gives:

$$I_B = I_E - I_C = (1 - \alpha)I_E \quad (14.4)$$

If  $\alpha = 0.995$ , then  $I_B = 0.005I_E$ . Base current is very small compared to emitter or collector current. A parameter  $\beta$  is defined as the ratio of collector current to base current resulting in:

$$\beta = \frac{\alpha}{1 - \alpha} \quad (14.5)$$

This parameter represents the current gain from base to collector and can be quite high. For the value of  $\alpha$  cited earlier, the value of  $\beta$  is 199.

## 14.4 Use of the BJT as an Amplifier

Figure 14.3 shows a simple configuration of a BJT amplifier. This circuit is known as the *common emitter configuration*.

A voltage source is not typically used to forward-bias the base–emitter junction in an actual circuit, but we will assume that  $V_{BB}$  is used for this purpose. A value of  $V_{BB}$  or  $V_{BE}$  near 0.6 to 0.7 V would be appropriate for this situation. The collector supply would be a large voltage, such as 12 V. We will assume that the value of  $V_{BB}$  sets the dc emitter current to a value of 1 mA for this circuit. The collector current entering the BJT will be slightly less than 1 mA, but we will ignore this difference and assume that  $I_C = 1$  mA also. With a 4-k $\Omega$  collector resistance, a 4-V drop will appear across  $R_C$  leading to a dc output voltage of 8 V. The distribution of electrons across the base region for the steady-state or quiescent conditions is shown by the solid line of Fig. 14.3(a).

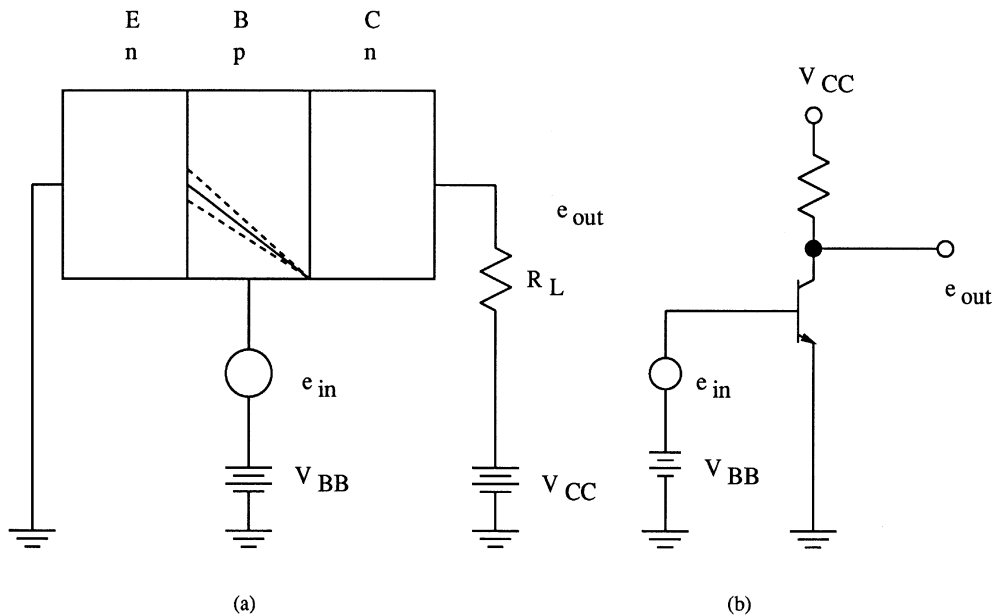


FIGURE 14.3 A BJT amplifier.

If a small ac voltage now appears in series with  $V_{BB}$ , the injected electron density at the left side of the base region will be modulated. Since this density varies exponentially with the applied voltage (see Eq. 14.2), a small ac voltage can cause considerable changes in density. The dashed lines in Fig. 14.3(a) show the distributions at the positive and negative peak voltages. The collector current may change from its quiescent level of 1 mA to a maximum of 1.1 mA as  $e_{in}$  reaches its positive peak, and to a minimum of 0.9 mA when  $e_{in}$  reaches its negative peak. The output collector voltage will drop to a minimum value of 7.6 V as the collector current peaks at 1.1 mA, and will reach a maximum voltage of 8.4 V as the collector current drops to 0.9 mA. The peak-to-peak ac output voltage is then 0.8 V. The peak-to-peak value of  $e_{in}$  to cause this change might be 5 mV, giving a voltage gain of  $A = -0.8/0.005 = -160$ . The negative sign occurs because when  $e_{in}$  increases, the collector current increases, but the collector voltage decreases. This represents a phase inversion in the amplifier of Fig. 14.3.

In summary, a small change in base-to-emitter voltage causes a large change in emitter current. This current is channeled across the collector, through the load resistance, and can develop a larger incremental voltage across this resistance.

## 14.5 Representing the Major BJT Effects by an Electronic Model

The two major effects of the BJT in the active region are the diode characteristics of the base-emitter junction and the collector current that is proportional to the emitter current. These effects can be modeled by the circuit of Fig. 14.4.

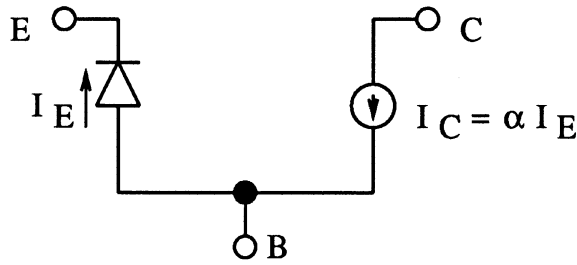


FIGURE 14.4 Large-signal model of the BJT.

The simple diode equation represents the relationship between applied emitter-to-base voltage and emitter current. This equation can be written as

$$I_E = I_1(e^{qV_{BE}/kT} - 1) \quad (14.6)$$

where  $q$  is the charge on an electron,  $k$  is Boltzmann's constant,  $T$  is the absolute temperature of the diode, and  $I_1$  is a constant at a given temperature that depends on the doping and geometry of the emitter-base junction.

The collector current is generated by a dependent current source of value  $I_C = \alpha I_E$ .

A small-signal model based on the large-signal model of Fig. 14.4 is shown in Fig. 14.5. In this case, the resistance,  $r_d$ , is the dynamic resistance of the emitter-base diode and is given by:

$$r_d = \frac{kT}{qI_E} \quad (14.7)$$

where  $I_E$  is the dc emitter current.

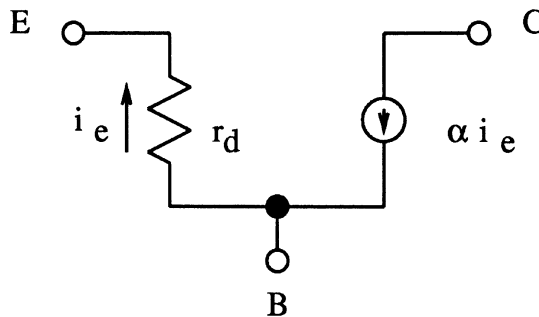


FIGURE 14.5 A small-signal model of the BJT.

## 14.6 Other Physical Effects in the BJT

The preceding section pertains to the basic operation of the BJT in the dc and midband frequency range. Several other effects must be included to model the BJT with more accuracy. These effects will now be described.

### Ohmic Effects

The metal connections to the semiconductor regions exhibit some ohmic resistance. The emitter contact resistance and collector contact resistance is often in the ohm range and does not affect the BJT operation in most applications. The base region is very narrow and offers little area for a metal contact. Furthermore, because this region is narrow and only lightly doped compared to the emitter, the ohmic resistance of the base region itself is rather high. The total resistance between the contact and the intrinsic base region can be 100 to 200  $\Omega$ . This resistance can become significant in determining the behavior of the BJT, especially at higher frequencies.

### Base-Width Modulation (Early Effect)

The widths of the depletion regions are functions of the applied voltages. The collector voltage generally exhibits the largest voltage change and, as this voltage changes, so also does the collector–base depletion region width. As the depletion layer extends further into the base region, the slope of the electron distribution in the base region becomes greater since the width of the base region is decreased. A slightly steeper slope leads to slightly more collector current. As reverse-bias decreases, the base width becomes greater and the current decreases. This effect is called *base-width modulation* and can be expressed in terms of the Early voltage,<sup>4</sup>  $V_A$ , by the expression:

$$I_C = \beta I_B \left( 1 + \frac{V_{CE}}{V_A} \right) \quad (14.8)$$

The Early voltage will be constant for a given device and is typically in the range of 60 to 100 V.

### Reactive Effects

Changing the voltages across the depletion regions results in a corresponding change in charge. This leads to an effective capacitance since

$$C = \frac{dQ}{dV} \quad (14.9)$$

This depletion region capacitance is a function of voltage applied to the junction and can be written as<sup>4</sup>:

$$C_{dr} = \frac{C_{Jo}}{(\phi - V_{app})^m} \quad (14.10)$$

where  $C_{Jo}$  is the junction capacitance at zero bias,  $\phi$  is the built-in junction barrier voltage,  $V_{app}$  is the applied junction voltage, and  $m$  is a constant. For modern BJTs,  $m$  is near 0.33. The applied junction voltage has a positive sign for a forward-bias and a negative sign for a reverse-bias. The depletion region capacitance is often called the *junction capacitance*.

An increase in forward base–emitter voltage results in a higher density of electrons injected into the base region. The charge distribution in the base region changes with this voltage change, and this leads to a capacitance called the *diffusion capacitance*. This capacitance is a function of the emitter current and can be written as:



$$C_D = k_2 I_E \quad (14.11)$$

where  $k_2$  is a constant for a given device.

## 14.7 More Accurate BJT Models

Figure 14.6 shows a large-signal BJT model used in some versions of the popular simulation program known as SPICE.<sup>5</sup> The equations for the parameters are listed in other texts<sup>5</sup> and will not be given here.

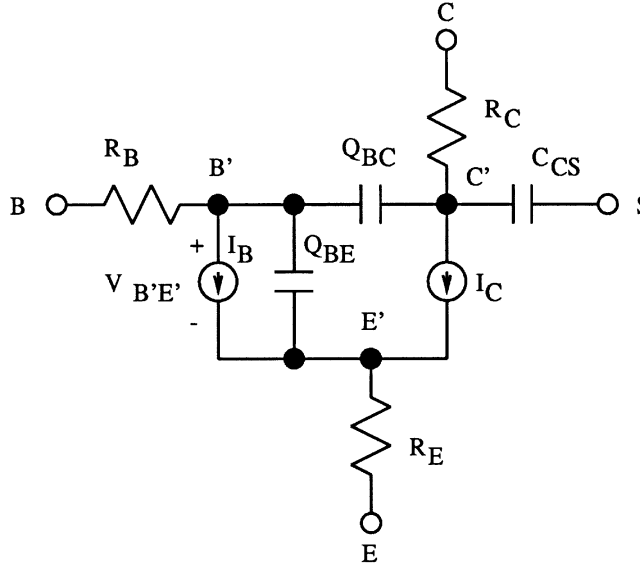


FIGURE 14.6 A more accurate large-signal model of the BJT.

Figure 14.7 shows a small-signal SPICE model<sup>5</sup> often called the hybrid- $\pi$  equivalent circuit. The capacitance,  $C_{\pi}$ , accounts for the diffusion capacitance and the emitter-base junction capacitance. The collector-base junction capacitance is designated  $C_{\mu}$ . The resistance,  $r_{\pi}$ , is equal to  $(\beta + 1)r_d$ . The transconductance,  $g_m$ , is given by:

$$g_m = \frac{\alpha}{r_d} \quad (14.12)$$

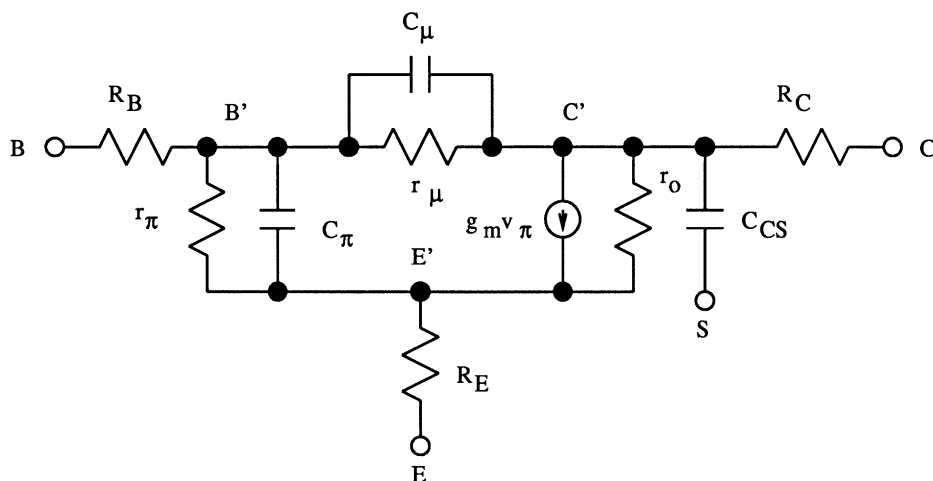
The impedance,  $r_o$ , is related to the Early voltage by:

$$r_o = \frac{V_A}{I_C} \quad (14.13)$$

$R_B$ ,  $R_E$ , and  $R_C$  are the base, emitter, and collector resistances, respectively. For hand analysis, the ohmic resistances  $R_E$  and  $R_C$  are neglected along with  $C_{CS}$ , the collector-to-substrate capacitance.

## 14.8 Heterojunction Bipolar Junction Transistors

In an npn device, all electrons injected from emitter to base are collected by the collector, except for a small number that recombine in the base region. The holes injected from base to emitter contribute to emitter junction current, but do not contribute to collector current. This hole component of the emitter



**FIGURE 14.7** The hybrid- $\pi$  small-signal model for the BJT.

current must be minimized to achieve a near-unity current gain from emitter to collector. As  $\alpha$  approaches unity, the current gain from base to collector,  $\beta$ , becomes larger.

In order to produce high- $\beta$  BJTs, the emitter region must be doped much more heavily than the base region, as explained earlier. While this approach allows the value of  $\beta$  to reach several hundred, it also leads to some effects that limit the frequency of operation of the BJT. The lightly doped base region causes higher values of base resistance, as well as emitter–base junction capacitance. Both of these effects are minimized in the *heterojunction BJT* (or HBJT). This device uses a different material for the base region than that used for the emitter and collector regions. One popular choice of materials is silicon for the emitter and collector regions, and a silicon/germanium material for the base region.<sup>6</sup> The difference in energy gap between the silicon emitter material and the silicon/germanium base material results in an asymmetric barrier to current flow across the junction. The barrier for electron injection from emitter to base is smaller than the barrier for hole injection from base to emitter. The base can then be doped more heavily than a conventional BJT to achieve lower base resistance, but the hole flow across the junction remains negligible due to the higher barrier voltage. The emitter of the HBJT can be doped more lightly to lower the junction capacitance. Large values of  $\beta$  are still possible in the HBJT while minimizing frequency limitations. Current gain-bandwidth figures exceeding 60 GHz have been achieved with present industrial HBJTs.

From the standpoint of analysis, the SPICE models for the HBJT are structurally identical to those of the BJT. The difference is in the parameter values.

## 14.9 Integrated Circuit Biasing Using Current Mirrors

Differential stages are very important in integrated circuit amplifier design. These stages require a constant dc current for proper bias. A simple bias scheme for differential BJT stages will now be discussed.

The diode-biased current sink or *current mirror* of Fig. 14.8 is a popular method of creating a constant-current bias for differential stages.

The concept of the current mirror was developed specifically for analog integrated circuit biasing and is a good example of a circuit that takes advantage of the excellent matching characteristics that are possible in integrated circuits. In the circuit of Fig. 14.8, the current  $I_2$  is intended to be equal to or “mirror” the value of  $I_1$ . Current mirrors can be designed to serve as sinks or sources.

The general function of the current mirror is to reproduce or mirror the input or reference current to the output, while allowing the output voltage to assume any value within some specified range. The current mirror can also be designed to generate an output current that equals the input current multiplied by a scale factor  $K$ . The output current can be expressed as a function of input current as:

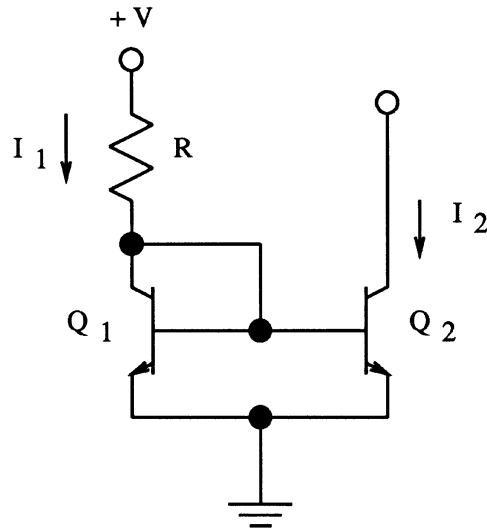


FIGURE 14.8 Current mirror bias stage.

$$I_O = KI_{IN} \quad (14.14)$$

where  $K$  can be equal to, less than, or greater than unity. This constant can be established accurately by relative device sizes and will not vary with temperature.

Figure 14.9 shows a multiple output current source where all of the output currents are referenced to the input current. Several amplifier stages can be biased with this multiple output current mirror.

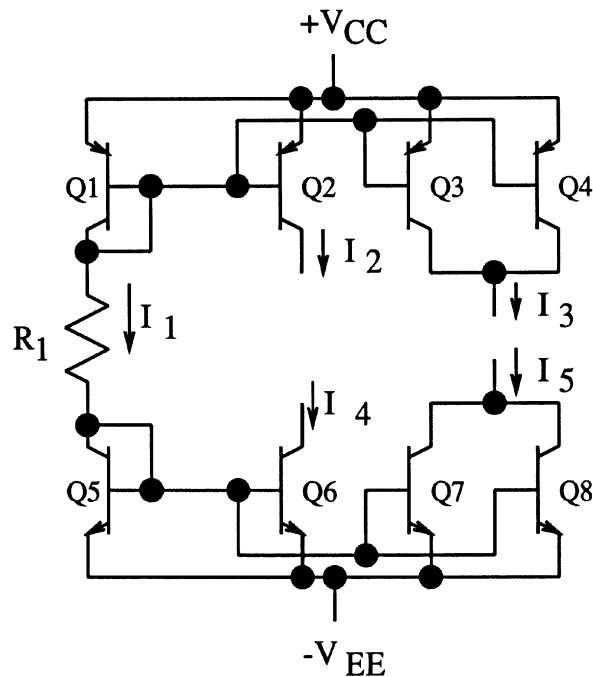


FIGURE 14.9 Multiple output current mirror.

## Current Source Operating Voltage Range

Figure 14.10 shows an ideal or theoretical current sink in (a) and a practical sink in (b). The voltage at node A in the theoretical sink can be tied to any potential above or below ground without affecting the value of  $I$ . On the other hand, the practical circuit of Fig. 14.10(b) requires that the transistor remain in the active region to provide a current of:

$$I = \alpha \frac{V_B - V_{BE}}{R} \quad (14.15)$$

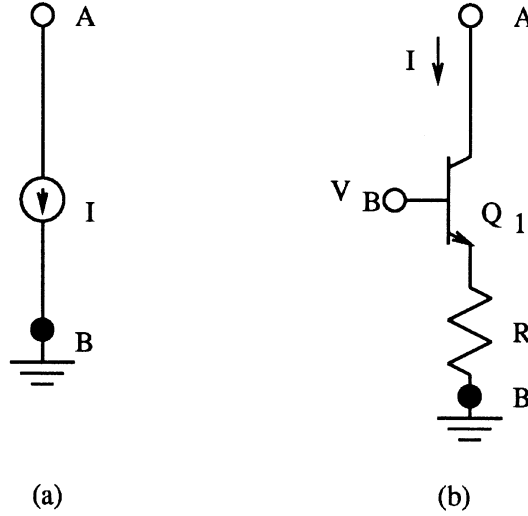


FIGURE 14.10 Current sink circuits: (a) ideal sink, (b) practical sink.

This requires that the collector voltage exceed the voltage  $V_B$  at all times. The upper limit on this voltage is determined by the breakdown voltage of the transistor. The output voltage must then satisfy:

$$V_B < V_C < (V_B + BV_{CE}) \quad (14.16)$$

where  $BV_{CE}$  is the breakdown voltage from collector to emitter of the transistor. This voltage range over which the current source operates is called the *output voltage compliance range* or the *output compliance*.

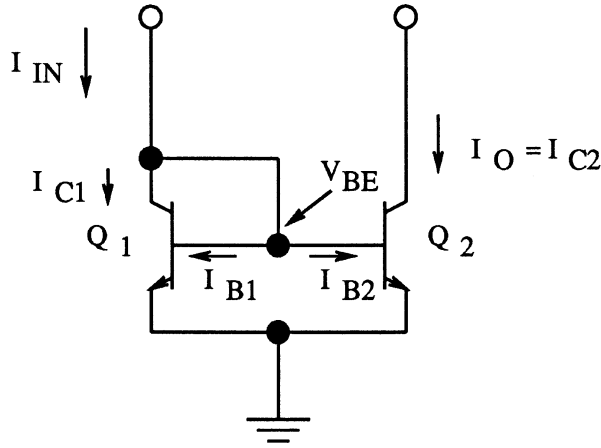
## Current Mirror Analysis

The current mirror is again shown in Fig. 14.11. If devices  $Q_1$  and  $Q_2$  are assumed to be matched devices, we can write:

$$I_{E1} = I_{E2} = I_{EO} e^{V_{BE}/V_T} \quad (14.17)$$

where  $V_T = kT/q$ ,  $I_{EO} = AJ_{EO}$ ,  $A$  is the emitter area of the two devices, and  $J_{EO}$  is the current density of the emitters. The base currents for each device will also be identical and can be expressed as:

$$I_{B1} = I_{B2} = \frac{I_{EO}}{\beta + 1} e^{V_{BE}/V_T} \quad (14.18)$$



**FIGURE 14.11** Circuit for current mirror analysis.

Device  $Q_1$  operates in the active region, but near saturation by virtue of the collector–base connection. This configuration is called a *diode-connected transistor*. Since the collector-to-emitter voltage is very small, the collector current for device  $Q_1$  is given by Eq. 14.8, assuming  $V_{CE} = 0$ . This gives:

$$I_{C1} = \beta I_{B1} \approx \frac{\beta}{\beta + 1} I_{EO} e^{V_{BE}/V_T} \quad (14.19)$$

The device  $Q_2$  does not have the constraint that  $V_{CE} \approx 0$  as device  $Q_1$  has. The collector voltage for  $Q_2$  will be determined by the external circuit that connects to this collector. Thus, the collector current for this device is:

$$I_{C2} = \beta I_{B2} \left( 1 + \frac{V_{C2}}{V_A} \right) \quad (14.20)$$

where  $V_A$  is the Early voltage. In effect, the output stage has an output impedance given by Eq. 14.13. The current mirror more closely approximates a current source as the output impedance becomes larger.

If we limit the voltage  $V_{C2}$  to small values relative to the Early voltage,  $I_{C2}$  is approximately equal to  $I_{C1}$ . For integrated circuit designs, the voltage required at the output of the current mirror is generally small, making this approximation valid.

The input current to the mirror is larger than the collector current and is:

$$I_{IN} = I_{C1} + 2I_B \quad (14.21)$$

Since  $I_{OUT} = I_{C2} = I_{C1} = \beta I_B$ , we can write Eq. 14.21 as:

$$I_{IN} = \beta I_B + 2I_B = (\beta + 2)I_B \quad (14.22)$$

Relating  $I_{IN}$  to  $I_{OUT}$  results in:

$$I_{OUT} = \frac{\beta}{\beta + 2} I_{IN} = \frac{I_{IN}}{1 + 2/\beta} \quad (14.23)$$

For typical values of  $\beta$ , these two currents are essentially equal. Thus, a desired bias current,  $I_{OUT}$ , is generated by creating the desired value of  $I_{IN}$ . The current  $I_{IN}$  is normally established by connecting a resistance  $R_1$  to a voltage source  $V_{CC}$  to set  $I_{IN}$  to:

$$I_{IN} = \frac{V_{CC} - V_{BE}}{R_1} \quad (14.24)$$

Control of collector/bias current for  $Q_2$  is then accomplished by choosing proper values of  $V_{CC}$  and  $R_1$ .

Figure 14.12 shows a multiple-output current mirror.

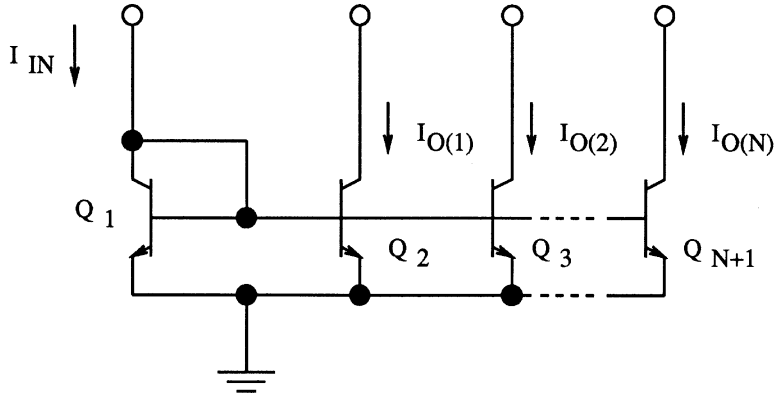


FIGURE 14.12 Multiple-output current mirror.

It can be shown that the output current for each identical device in Fig. 14.12 is:

$$I_O = \frac{I_{IN}}{1 + \frac{N+1}{\beta}} \quad (14.25)$$

where  $N$  is the number of output devices.

The current sinks can be turned into current sources by using pnp transistors and a power supply of opposite polarity. The output devices can also be scaled in area to make  $I_{OUT}$  be larger or smaller than  $I_{IN}$ .

### Current Mirror with Reduced Error

The difference between output current in a multiple-output current mirror and the input current can become quite large if  $N$  is large. One simple method of avoiding this problem is to use an emitter follower to drive the bases of all devices in the mirror, as shown in Fig. 14.13.

The emitter follower,  $Q_0$ , has a current gain from base to collector of  $\beta + 1$ , reducing the difference between  $I_O$  and  $I_{IN}$  to:

$$I_{IN} - I_O = \frac{N+1}{\beta+1} I_B \quad (14.26)$$

The output current for each device is:

$$I_O = \frac{I_{IN}}{1 + \frac{N+1}{\beta(\beta+1)}} \quad (14.27)$$



# 14.10 The Basic BJT Switch

In digital circuits, the BJT is used as a switch to generate one of only two possible output voltage levels, depending on the input voltage level. Each voltage level is associated with one of the binary digits, 0 or 1. Typically, the high voltage level may fall between 2.8 V and 5 V while the low voltage level may fall between 0 V and 0.8 V.

Logic circuits are based on BJT stages that are either in cutoff with both junctions reverse-biased or in a conducting mode with the emitter–base junction forward-biased. When the BJT is “on” or conducting emitter current, it can be in the active region or the saturation region. If it is in the saturation region, the collector–base region is also forward-biased.

The three possible regions of operation are summarized in Table 14.1.

TABLE 14.1 Regions of Operation

Region	Cutoff	Active	Saturation
C–B bias	Reverse	Reverse	Forward
E–B bias	Reverse	Forward	Forward

The BJT very closely approximates certain switch configurations. For example, when the switch of Fig. 14.15(a) is open, no current flows through the resistor and the output voltage is +12 V. Closing the switch causes the output voltage to drop to zero volts and a current of  $12/R$  flows through the resistance. When the base voltage of the BJT of Fig. 14.15(b) is negative, the device is cut off and no collector current flows. The output voltage is +12 V, just as in the case of the open switch. If a large enough current is now driven into the base to saturate the BJT, the output voltage becomes very small, ranging from 20 mV to 500 mV, depending on the BJT used. The saturated state corresponds closely to the closed switch. During the time that the BJT switches from cutoff to saturation, the active region equivalent circuit applies. For high-speed switching of this circuit, appropriate reactive effects must be considered. For low-speed switching, these reactive effects can be neglected.

Saturation occurs in the basic switching circuit of Fig. 14.15(b) when the entire power supply voltage drops across the load resistance. No voltage, or perhaps a few tenths of volts, then appears from collector to emitter. This occurs when the base current exceeds the value

$$I_{B(sat)} = \frac{V_{CC} - V_{CE(sat)}}{\beta R_L} \tag{14.28}$$

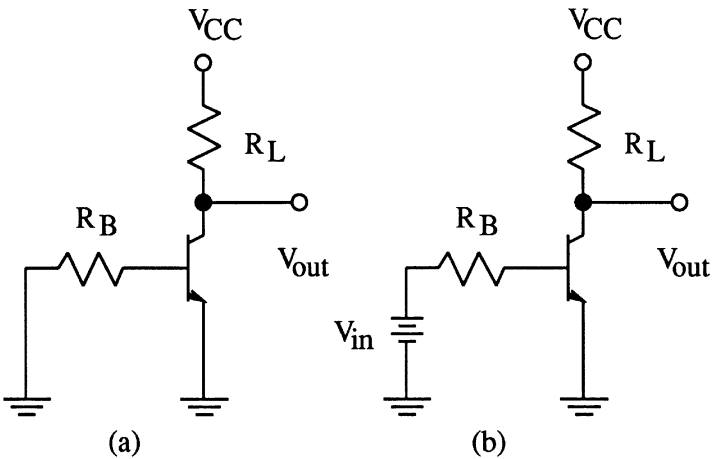


FIGURE 14.15 The BJT as a switch: (a) open switch, (b) closed switch.



When a transistor switch is driven into saturation, the collector–base junction becomes forward-biased. This situation results in the electron distribution across the base region shown in Fig. 14.16. The forward-bias of the collector–base junction leads to a non zero concentration of electrons in the base that is unnecessary to support the gradient of carriers across this region. When the input signal to the base switches to a lower level to either turn the device off or decrease the current flow, the excess charge must be removed from the base region before the current can begin to decrease.

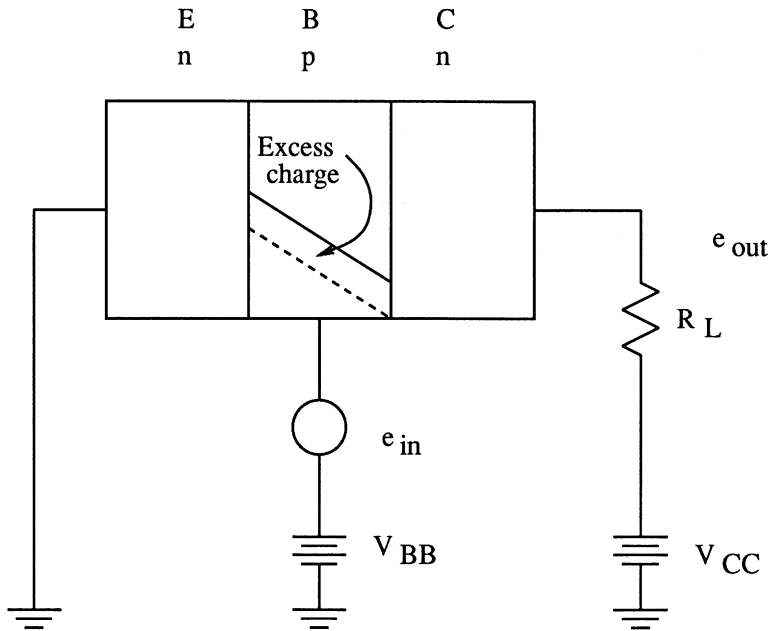


FIGURE 14.16 Electron distribution in the base region of a saturated BJT.

## 14.11 High-Speed BJT Switching

There are three major effects that extend switching times in a BJT:

1. The depletion-region or junction capacitances are responsible for delay time when the BJT is in the cutoff region.
2. The diffusion capacitance and the Miller-effect capacitance are responsible for the rise and fall times of the BJT as it switches through the active region.
3. The storage time constant accounts for the time taken to remove the excess charge from the base region before the BJT can switch from the saturation region to the active region.

There are other second-order effects that are generally negligible compared to the previously listed time lags.

Since the transistor is generally operating as a large-signal device, the parameters such as junction capacitance or diffusion capacitance will vary as the BJT switches. One approach to the evaluation of time constants is to calculate an average value of capacitance over the voltage swing that takes place. Not only is this method used in hand calculations, but most computer simulation programs use average values to speed calculations.

### Overall Transient Response

Before discussing the individual BJT switching times, it is helpful to consider the response of a common-emitter switch to a rectangular waveform. Figure 14.17 shows a typical circuit using an npn transistor.

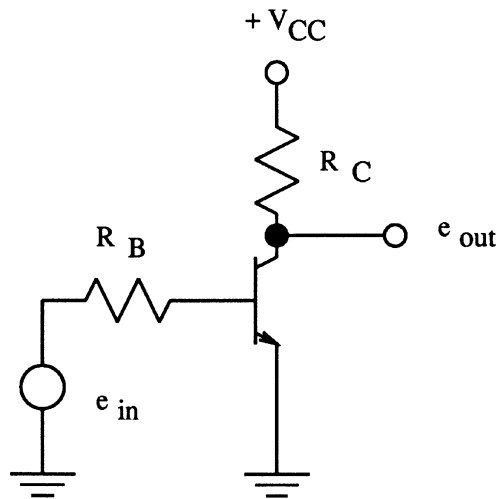


FIGURE 14.17 A simple switching circuit.

A rectangular input pulse and the corresponding output are shown in Fig. 14.18. In many switching circuits, the BJT must switch from its “off” state to saturation and later return to the “off” state. In this case, the delay time, rise time, saturation storage time, and fall time must be considered in that order to find the overall switching time.

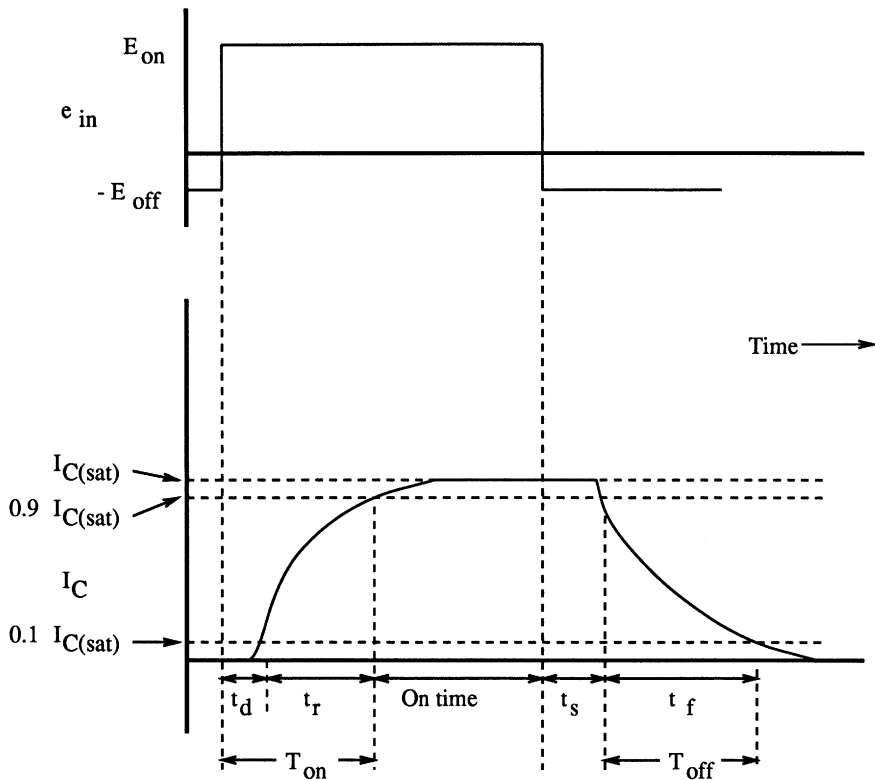


FIGURE 14.18 Input and output waveforms.

The total waveform is made up of five sections: delay time, rise time, on time, storage time, and fall time. The following list summarizes these points and serves as a guide for future reference:

- $t'_d$  = Passive delay time; time interval between application of forward base drive and start of collector-current response.
- $t_d$  = Total delay time; time interval between application of forward base drive and the point at which  $I_C$  has reached 10% of the final value.
- $t_r$  = Rise time; 10- to 90-% rise time of  $I_C$  waveform.
- $t'_s$  = Saturation storage time; time interval between removal of forward base drive and start of  $I_C$  decrease.
- $t_s$  = Total storage time; time interval between removal of forward base drive and point at which  $I_C = 0.9I_{C(sat)}$ .
- $t_f$  = Fall time; 90- to 10-% fall time of  $I_C$  waveform
- $T_{on}$  = Total turn-on time; time interval between application of base drive and point at which  $I_C$  has reached 90% of its final value.
- $T_{off}$  = Total turn-off time; time interval between removal of forward base drive and point at which  $I_C$  has dropped to 10% of its value during on time.

Not all applications will require evaluation of each of these switching times. For instance, if the base drive is insufficient to saturate the transistor,  $t_s$  will be zero. If the transistor never leaves the active region, the delay time will also be zero.

The factors involved in calculating the switching times are summarized in the following paragraphs.<sup>8</sup> The passive delay time is found from:

$$t'_d = \tau_d \ln \left( \frac{E_{on} + E_{off}}{E_{on} - V_{BE(on)}} \right) \quad (14.29)$$

where  $\tau_d$  is the product of the charging resistance and the average value of the two junction capacitances.

The active region time constant is a function of the diffusion capacitance, the collector–base junction capacitance, the transconductance, and the charging resistance. This time constant will be denoted by  $\tau$ . If the transistor never enters saturation, the rise time is calculated from the well-known formula:

$$t_r = 2.2\tau \quad (14.30)$$

If the BJT is driven into saturation, the rise time is found from<sup>8</sup>:

$$t_r = \tau \ln \left( \frac{K - 0.1}{K - 0.9} \right) \quad (14.31)$$

where  $K$  is the overdrive factor or the ratio of forward base current drive to the value needed for saturation. The rise time for the case where  $K$  is large can be much smaller than the rise time for the nonsaturating case ( $K < 1$ ). Unfortunately, the saturation storage time increases for large values of  $K$ .

The saturation storage time is given by:

$$t'_s = \tau_s \ln \left( \frac{I_{B1} - I_{B2}}{I_{B(sat)} - I_{B2}} \right) \quad (14.32)$$

where  $\tau_s$  is the storage time constant,  $I_{B1}$  is the forward base current before switching, and  $I_{B2}$  is the current after switching and must be less than  $I_{B(sat)}$ . The saturation storage time can slow the overall switching time significantly. The higher speed logic gates utilize circuits that avoid the saturation region for the BJTs that make up the gate.

## 14.12 Simple Logic Gates

Although the resistor-transistor-logic (RTL) family has not been used since the late 1960s, it demonstrates the concept of a simple logic gate. Figure 14.19 shows a four-input RTL NOR gate.

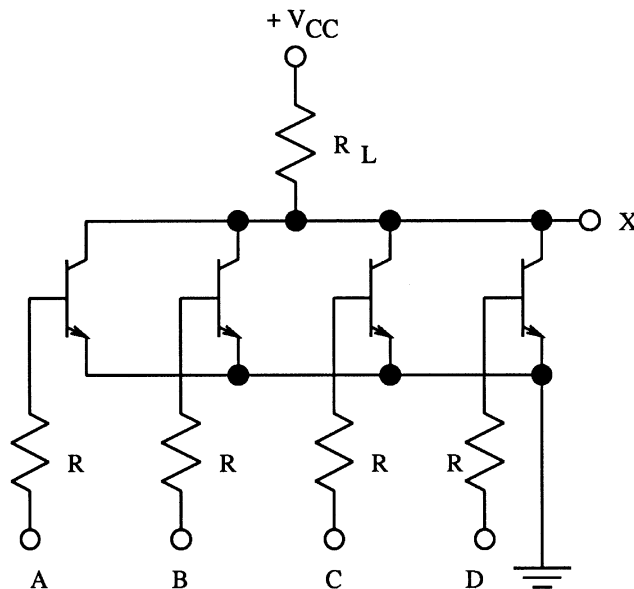


FIGURE 14.19 A four-input RTL NOR gate.

If all four inputs are at the lower voltage level (e.g., 0 V), there is no conducting path from output to ground. No voltage will drop across  $R_L$ , and the output voltage will equal  $V_{CC}$ . If any or all of the inputs moves to the higher voltage level (e.g., 4 V), any BJT with base connected to the higher voltage level will saturate, pulling the output voltage down to a few tenths of a volt. If positive logic is used, with the high voltage level corresponding to binary “1” and the low voltage level to binary “0,” the gate performs the NOR function. Other logic functions can easily be constructed in the RTL family.

Over the years, the performance of logic gates has been improved by different basic configurations. RTL logic was improved by diode-transistor-logic (DTL). Then, transistor-transistor-logic (TTL) became very prominent. This family is still popular in the small-scale integration (SSI) and medium-scale integration (MSI) areas, but CMOS circuits have essentially replaced TTL in large-scale integration (LSI) and very-large-scale integration (VLSI) applications.

One popular family that is still prominent in very high-speed computer work is the emitter-coupled logic (ECL) family. While CMOS packs many more circuits into a given area than ECL, the frequency performance of ECL leads to its popularity in supercomputer applications.

## 14.13 Emitter-Coupled Logic

Emitter-coupled logic (ECL) was developed in the mid-1960s and remains the fastest silicon logic circuit available. Present ECL families offer propagation delays in the range of 0.2 ns.<sup>9</sup> The two major disadvantages of ECL are: (1) resistors which require a great deal of IC chip area, must be used in each gate, and (2) the power dissipation of an ECL gate is rather high. These two shortcomings limit the usage of ECL in VLSI systems. Instead, this family has been used for years in larger supercomputers than can afford space and power to achieve higher speeds.



## A Closer Look at the Differential Stage

Figure 14.21 shows a simple differential stage similar to the input stage of an ECL gate.<sup>2</sup> Both transistors are biased by a current source,  $I_T$ , called the *tail current*. The two input signals  $e_1$  and  $e_2$  make up a differential input signal defined as:

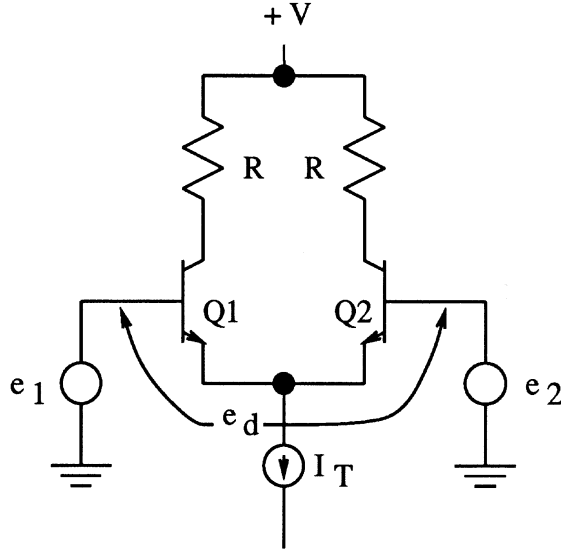


FIGURE 14.21 A simple differential stage similar to an ECL input stage.

$$e_d = e_1 - e_2 \quad (14.33)$$

This differential voltage can be expressed as the difference between the base-emitter junction voltages as:

$$e_d = V_{BE1} - V_{BE2} \quad (14.34)$$

The collector currents can be written in terms of the base-emitter voltages as:

$$I_{C1} = \alpha I_{EO} e^{V_{BE1}/V_T} \approx I_{EO} e^{V_{BE1}/V_T} \quad (14.35)$$

$$I_{C2} = \alpha I_{EO} e^{V_{BE2}/V_T} \approx I_{EO} e^{V_{BE2}/V_T} \quad (14.36)$$

where matched devices are assumed.

A differential output current can be defined as the difference of the collector currents, or

$$I_d = I_{C1} - I_{C2} \quad (14.37)$$

Since the tail current is  $I_T = I_{C1} + I_{C2}$ , taking the ratio of  $I_d$  to  $I_T$  gives:

$$\frac{I_d}{I_T} = \frac{I_{C1} - I_{C2}}{I_{C1} + I_{C2}} \quad (14.38)$$

Since  $V_{BE1} = e_d + V_{BE2}$ , we can substitute this value for  $V_{BE1}$  into Eq. 14.35 to write:

$$I_{C1} = I_{EO} e^{(e_d + V_{BE2})/V_T} = I_{EO} e^{e_d/V_T} e^{V_{BE2}/V_T} \quad (14.39)$$

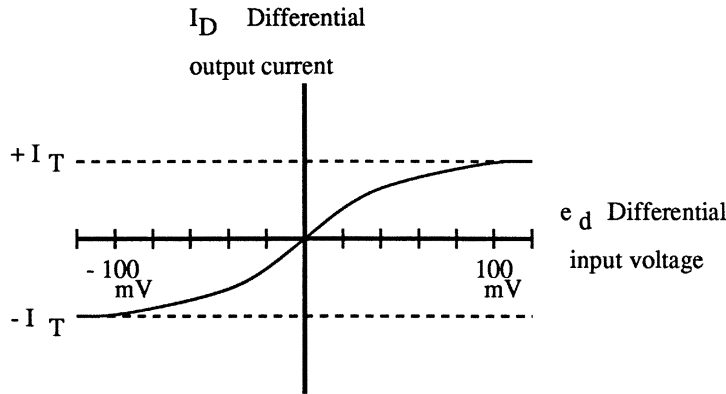
Substituting Eqs. 14.36 and 14.39 into Eq. 14.38 results in:

$$\frac{I_d}{I_T} = \frac{e^{e_d/V_T} - 1}{e^{e_d/V_T} + 1} = \tanh \frac{e_d}{2V_T} \quad (14.40)$$

or

$$I_d = I_T \tanh \frac{e_d}{2V_T} \quad (14.41)$$

This differential current is graphed in Fig. 14.22.

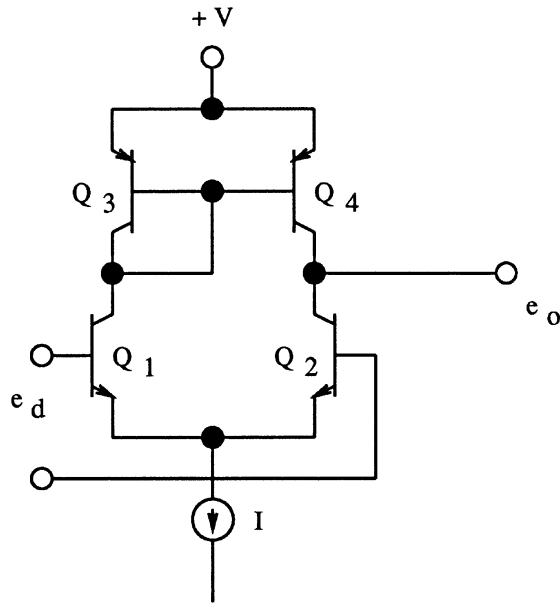


**FIGURE 14.22** Differential output current as a function of differential input voltage.

When  $e_d$  is zero, the differential current is also zero, implying equal values of collector currents in the two devices. As  $e_d$  increases, so also does  $I_d$  until  $e_d$  exceeds  $4V_T$  at which time  $I_d$  has reached a constant value of  $I_T$ . From the definition of differential current, this means that  $I_{C1}$  equals  $I_T$  while  $I_{C2}$  is zero. As the differential input voltage goes negative, the differential current approaches  $-I_T$  as the voltage reaches  $-4V_T$ . In this case,  $I_{C2} = I_T$  while  $I_{C1}$  goes to zero.

The implication here is that the differential stage can move from a balanced condition with  $I_{C1} = I_{C2}$  to a condition of one device fully off and the other fully on with an input voltage change of around 100 mV or  $4V_T$ . This demonstrates that a total voltage change of about 200 mV at the input can cause an ECL gate to change states. This small voltage change contributes to smaller switching times for ECL logic.

The ability of a differential pair to convert a small change in differential base voltage to a large change in collector voltage also makes it a useful building block for analog amplifiers. In fact, a differential pair with a pnp transistor current mirror load, as illustrated in Fig. 14.23, is widely used as an input stage for integrated circuit op-amps.



**FIGURE 14.23** Differential input stage with current mirror load.

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